Study of Radiation Effects on 28nm UTBB FDSOI Technology

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By

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ABSTRACT

With the evolution of modern Complementary Metal-Oxide-Semiconductor (CMOS) technology, transistor feature size has been scaled down to nanometers. The scaling has resulted in tremendous advantages to the integrated circuits (ICs), such as higher speed, smaller circuit size, and lower operating voltage. However, it also creates some reliability concerns. In particular, small device dimensions and low operating voltages have caused nanoscale ICs to become highly sensitive to operational disturbances, such as signal coupling, supply and substrate noise, and single event effects (SEEs) caused by ionizing particles, like cosmic neutrons and alpha particles. SEEs found in ICs can introduce transient pulses in circuit nodes or data upsets in storage cells. In well-designed ICs, SEEs appear to be the most troublesome in a space environment or at high altitudes in terrestrial environment. Techniques from the manufacturing process level up to the system design level have been developed to mitigate radiation effects. Among them, silicon-on-insulator (SOI) technologies have proven to be an effective approach to reduce single-event effects in ICs. So far, 28nm ultra-thin body and buried oxide (UTBB) Fully Depleted SOI (FDSOI) by STMicroelectronics is one of the most advanced SOI technologies in commercial applications. Its resilience to radiation effects has not been fully explored and it is of prevalent interest in the radiation effects community. Therefore, two test chips, namely ST1 and AR0, were designed and tested to study SEEs in logic circuits fabricated with this technology.

The ST1 test chip was designed to evaluate SET pulse widths in logic gates. Three kinds of the on-chip pulse-width measurement detectors, namely the Vernier detector, the Pulse Capture detector and the Pulse Filter detector, were implemented in the ST1 chip. Moreover, a Circuit for Radiation Effects Self-Test (CREST) chain with combinational logic was designed to study both SET and SEU effects. The ST1 chip was tested using a heavy ion irradiation beam source in Radiation Effects Facility (RADEF), Finland. The experiment results showed that the cross-section of the 28nm UTBB-FDSOI technology is two orders lower than its bulk competitors. Laser tests were also applied to this chip to research the pulse distortion effects and the relationship between SET, SEU and the clock frequency. Total Ionizing Dose experiments were carried out at the University of Saskatchewan and European Space Agency with Co-60 gammacell radiation sources.

The test results showed the devices implemented in the 28nm UTBB-FDSOI technology can maintain its functionality up to 1 Mrad(Si).

In the AR0 chip, we designed five ARM Cortex-M0 cores with different logic protection levels to investigate the performance of approximate logic protecting methods. There are three custom-designed SRAM blocks in the test chip, which can also be used to measure the SEU rate. From the simulation result, we concluded that the approximate logic methodology can protect the digital logic efficiently.

This research comprehensively evaluates the radiation effects in the 28nm UTBB-FDSOI technology, which provides the baseline for later radiation-hardened system designs in this technology.

ACKNOWLEDGEMENTS

My Ph.D. research is finished under the help from all the professors, research staffs and specialists. Without the guidance, assistance and suggestions from you, it would be impossible for me to complete the project and publish papers in journals and conferences.

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LIST OF ABBREVIATIONS

ARM	Advanced RISC Machine
CMOS	Complementary Metal-Oxide Semiconductor
CTS	Clock Tree Synthesis
DICE	Dual Interlocked Storage Cell
DUT	Device Under Test
ESA	European Space Agency
FDSOI	Fully Depleted Silicon On Insulator
FPGA	Field Programmable Gate Array
GCR	Galactic Cosmic Rays
HI	Heavy Ion
IC	Integrated Circuit
LET	Linear Energy Transfer
LVDS	Low-Voltage Differential Signaling
MSB	Most Significant Bit
NRL	Naval Research Laboratory
PC	Personal Computer
PLL	Phase-locked loops
PVT	Process, Voltage and Temperature
RAM	Random Access Memory
RO	Ring Oscillator
SEE	Single Event Effect

SET	Single Event Transient
SEU	Single Event Upset
SPICE	Simulation Program with Integrated Circuit Emphasis
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
TPA	Two Photon Absorption
UTBB	Ultra-Thin Body and Buried oxide
UVM	Universal Verification Methodology

Chapter 1: INTRODUCTION

1.1 Introduction

A single particle with high energy may cause unexpected effects in integrated circuits (ICs), which is known as Single Event Effects (SEEs). An SEE may result in disastrous consequences in an electronic system.

In 1975, Binder and his colleagues reported that the unexpected triggering of digital circuits had caused anomalies in communication satellite operation [1]. Some JK flip-flops were triggered unexpectedly, which caused the malfunctioning of the satellite. In 1980, two spacecraft, Pioneer 10 and Pioneer 11, were launched to explore Jupiter and Saturn. These two spacecraft were observed abnormal behavior in the acceleration stages. Their velocity decreased more than expected, which appeared to cause a constant acceleration towards sun for both of them [2]. In 1991, malfunctions occurred on a Japanese communications satellite, Superbird-A [3]. Following a wrong operation, the satellite fuel tank leaked and finally caused the satellite total loss, which induced a 1.5-million-dollar loss. In 2003, it was reported that Cisco 12000 line cards reset without expectation [4]. The system engineers found out that the line cards need 2-3 minutes to be recovered because of the digital logic error or ECC memory parity error.

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Engineers and researchers investigated the accidents or malfunctions mentioned above. The results indicated that SEEs were the root cause of these events. When exposed to radiation environments, semiconductor material may be ionized by energetic particles, and electron-hole pairs are created along the particle path in the semiconductor. If a semiconductor device absorbs these generated carriers, it will lead to current/voltage transients of the affected nodes. This is called a Single Event Transient (SET). If the transient is propagated into a sequential circuit unit such as a flip-flop or a memory cell, then a Single Event Upset (SEU) occurs. These kinds of effects can introduce errors into an electronic system, and cause significant costs to a company, or even an entire society.

Since the 1970s, it is reported that SEEs have impacted numerous spacecraft (Table 1.1). In recent years, with the growth of IC complexity, SEEs have become a serious problem not only for the electronics in radiation environments, but also for many ground-level applications as demonstrated by the aforementioned Cisco line card failures and other reported malfunctions.

Table 1.1 Spacecraft for Which SEEs Have Had an Impact [3]

For the Period 1970-1982			
DE-1	Galileo	INSAT-1	Intelsat - IV
Landsat-D	LES 8	LES 9	Pioneer Venus
SMM	Tiros-N	Voyager	
For the Period 1982–1990			
AMTE/CCE	DSCS	ERBS	Galileo Lander
GEOS-6	GEOS-7	Geosat	GPS 9521
GPS 9783	GPS 9794	HUT	IUS
MOS-1	OPEN	Shuttle	SPOT-1
TDRS-1	TDRS-4	UOSAT-2	
For the Period 1990–1997			
COBEERS-1 (SEL)	ETS-V (SEL)	ADEOS	
EUVE	HST	HST-STIS	Kitsat-1
NATO-3A	PoSAT-1	S80/T	SOHO
Spot-2	SPOT-3	STS-61	Superbird
TDRS-5	TDRS-6	TDRS-7	Topex/Poseidon
UoSAT-2	UoSAT-3	UoSAT-5	WIND
Yahkoh-BCS			
Amateur Radio Satellite Experiments			
AO-16	LO-19	I0-26	Spartan/OAST/SPRE

One of the major sources of high-energy particles that cause SEEs is cosmic rays that are mainly from the Sun and sources outside of the solar system (galactic cosmic rays, GCR). The major radiation particles in GCR are protons (85%), neutrons, alpha particles and heavy ions. As can be seen in Figure 1.1, the flux of H (proton) particles is more than two orders higher than the flux of heavy ions.

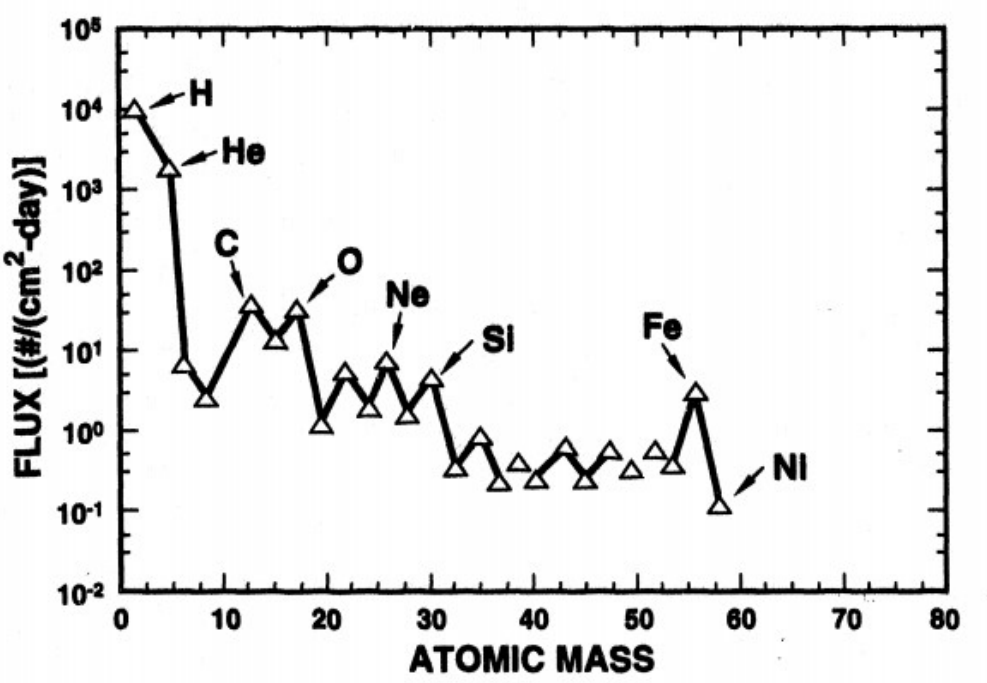


Figure 1.1 The Flux of GCR Particles [9]

Solar cosmic rays greatly depend on solar activity. A solar flare involves a very broad spectrum of emissions with typically a $1*10^{20}$ energy release [6, 7]. When a solar flare occurs, an excessive amount of protons, alpha particles and heavy ions are emitted by the Sun, and can last for several days to a week [6, 7]. These particles can arrive at Earth within tens of minutes. Normally, the particles emitted in a solar flare are mostly proton and alpha particles. Heavy ions contribute only a small portion, which is less significant compared to GCR. In a large solar flare, the proportion of heavy ions can reach up to 50% of the space background, and the number of alpha and proton particles can increase to thousands of times over the cosmic background [5] [6]. Figure 1.2 shows the Linear Energy Transfer (LET) spectrum variation in solar activities.

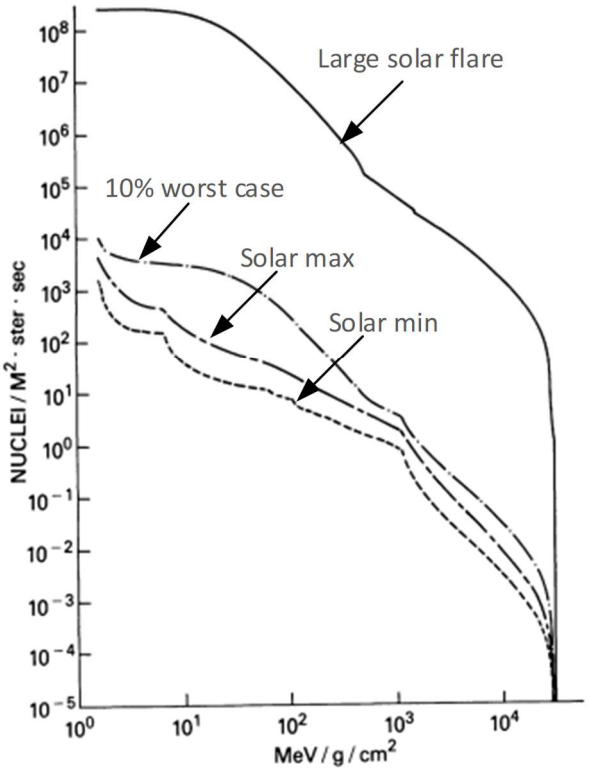


Figure 1.3 LET Spectra at Geosynchronous [6]

When semiconductor materials interact with the particles in cosmic rays, extra charges are generated and they can create SEEs.

Although comprising only a small portion of cosmic rays, heavy ions, such as Ne, Ar, Fe, Kr, can cause significant SEEs in electronics because they can deposit more energy in a material than lighter particles. When a single heavy ion passes through a semiconductor material, ions are deposited along its track. Most of the heavy ions in space are energetic enough to travel through a semiconductor device, leaving huge amount of ions on its track, which can potentially cause SEEs.

Protons are another source of SEEs. As shown in Figure 1.1, protons comprise the main portion of space rays (85% in GCR and more than 90% in solar rays). A proton is a subatomic particle with one positive electric charge. Although a proton is ionized, only a small amount of charge is

deposited into silicon materials along its track. In other words, its passage is not easy to produce SEEs. However, a small portion ($1/10^5$) of protons will have nuclear reactions with the atoms inside the silicon material, generating various secondary ion particels. These secondary particles can be energetic enough to produce SEEs. Because of the large number of protons in cosmic rays, they can trigger even more SEEs than heavy ions in space electronics.

Neutrons were discovered in the 1930s. They are subatomic particles with no electric charge. Consequently, they do not react with semiconductor materials to generate electron-hole pairs directly. Nuclear reaction is their only way to generate SEEs. When a neutron collides into a nucleus in the material, secondary charged particles may be generated, and then cause SEEs. When cosmic rays enter the atmosphere, the primary particles react on average 12 times with molecules in the air before reaching ground level, a phenomenon called an air shower [8]. As shown in Figure 1.3, neutrons along with muons and pions are generated in an air shower. Recent work has revealed that the generated neutrons and the thermal (low energy) neutrons can be the main sources of SEEs at ground level [10-15]. This imposes significant challenges to ground-level commercial electronic systems for reliable operations, especially for small feature-size silicon technologies.

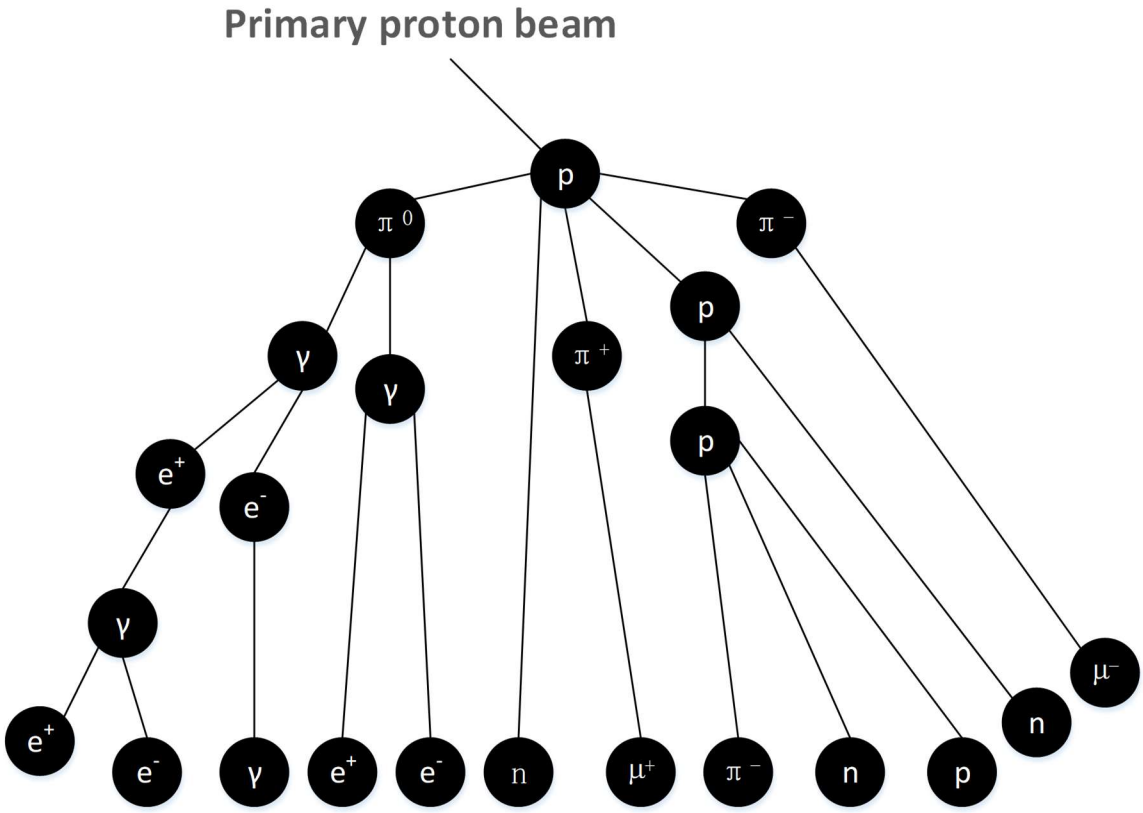


Figure 1.5 Air shower [8]

Primary proton beam

An alpha particle is equal to a helium nucleus with no electron. With two protons in its atomic nucleus, an alpha particle has two positive electric charges. Consequently, alpha particles can also generate extra charges when interacting with semiconductor materials. Alpha particles comprise 14% of cosmic rays, which can cause errors in space-borne circuits [7]. On the ground level, neutron nuclear reactions in silicon can also generate alpha particles as a by-product. Moreover, some IC packaging materials can also emit alpha particles, which may result in SEEs in digital systems.

1.2 Motivation

To reduce SEEs and increase system reliability, researchers have proposed numerous methods, circuit structures and technologies in the past thirty years. Recent research has proved that Fully Depleted Silicon On Insulator (FDSOI) technologies are more reliable than their bulk competitors in harsh radiation environments, since their charge collection volume is extremely small [16-24]. It is reported that the soft error rate of the SRAM chip based on ST 28nm UTBB-FDSOI is two orders lower than a similar 28nm bulk technology [25, 26]. Moreover, FDSOI technologies are virtually immune to a Single Event Latchup (SEL), which could be destructive event, causing a direct current path between power and ground in an IC. Because of these merits, FDSOI is a good option for applications in high-radiation environments, such as space applications.

FDSOI technologies are attractive due to their high-speed and low-power features, and their applications are well suited to high-clock frequency systems. However, when clock frequency increases, transient errors from combinational logic circuits may become dominant. In [27], it was predicted that the soft error rate (SER) caused by SETs from combinational logic circuits would increase linearly with the clock frequency, while the SER induced by SEUs from sequential logic circuits generally remains the same. As a result, at a certain frequency point, SETs would outstrip

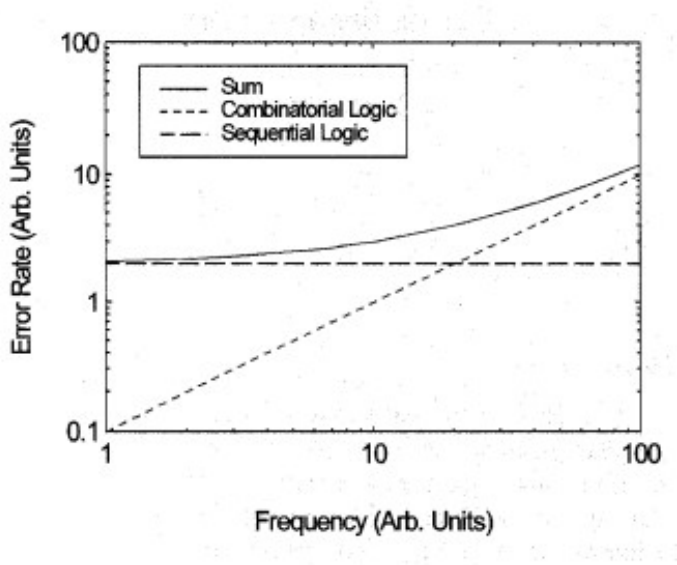


Figure 1.7 Error Rate as a Function of Frequency for Combinational and Sequential Logic Elements as well as their Sum [27]

SEUs and become the major source of soft errors. Therefor, for high-speed applications, more attention should be paid to the investigation of SET characterization and mitigation methods.

For FDSOI technologies, Total Ionizing Dose (TID) effects also need to be investigated. Because of the additional oxide layer between the body and substrate, FDSOI is expected to be more sensitive to TID. In a space environment, TID effects are another major source that cause device failure. Since the TID effects impact on the transistor electrical characteristics, the transistor threshold voltage will be influenced as well. As a result, the TID effects will influence the operating clock frequency of the devices. Moreover, the cumulative yield charge in the insulator lays will increase the leakage current and power consumption of the devices.

Currently, some research works focusing on nano-scale FDSOI technologies have been performed to evaluate the radiation effects on them. The studies of TID effects on single transistors have been performed to measure their leakage currents and threshold voltages [28]. The SEU effects on flip-flops and latches were also evaluated with various irradiation sources [29-32]. Based on the SEU evaluation results, some hardened flip-flop designs based on different techniques have been proposed [33, 34]. Back-gate voltage effect research was also performed [35]. However, all of the works mentioned above did not focus on the high-speed applications of the 28nm FDSOI technologies. Due to the increase of clock frequency, SETs could become the dominant soft error source, it is important to evaluate the SET effects for high-speed applications. Moreover, how the TID influences the circuit speed is also crucial. In this dissertation, the research is mainly focused on the SET and circuit-level TID investigations. The research objectives of the thesis are defined as follows:

1. Investigate and evaluate different types of on-chip SET pulse measurement circuits;
2. Measure the SET pulse width in various standard cell logic gates with 28nm FDSOI technology;
3. Evaluate the approximate logic soft error mitigation method using an ARM Cortex-M0 processor fabricated with ST 28nm UTBB-FDSOI technology;
4. Study the TID tolerance of ST 28nm UTBB-FDSOI technology.

To carry out the radiation effects investigation mentioned above, two test chips were designed and implemented, using ST 28nm UTBB-FDSOI technology. The first chip (ST1) focuses on the SET measurement. There are 96 combinational logic chains for the SET capture and three kinds of pulse-width measurement circuits in the chip. There is also one CREST chain with parallel

combinational logic between each stage, in order to research the relationship between the SER and the clock frequency. The second chip (AR0) is designed mainly for the SET mitigation research. There are five ARM Cortex-M0 processors implemented in the chip. All of these five cores have identical functionality; however, they have different SET-tolerant levels. By comparing the SER in the irradiation experiments, we can evaluate the performance of mitigation methods.

1.3 Thesis Organization

This thesis is organized as follows:

Chapter 1 briefly introduces radiation environments. Some of the incidents potentially caused by SEEs are listed to emphasize the influence of radiation in different electronic systems. The space radiation beam sources, solar rays and GCR, and the composition are described briefly. Then, there is a demonstration of the motivation for the project, emphasizing the significance of SET investigation in modern technologies.

Chapter 2 illustrates the basic SEE mechanisms. Three types of single event effects, Single Event Upset, Single Event Transient and Single Event Latchup are introduced in this chapter. The chapter also gives an overview of ST UTBB-FDSOI technology, showing the reason for a low Soft Error Rate. The photon effects in the semiconductor materials are also demonstrated to show that pulsed laser is a useful method for SEE research.

Chapter 3 presents the SET pulse measurement chip that was designed at the University of Saskatchewan. The top-level specification, infrastructure circuits, SET detectors, test chains and circuit layout are described, showing that this chip can be used to investigate various single event effects.

Chapter 4 first compares the SPICE simulation results of the different SET detector responses with different pulse inputs. Then, the PVT corner simulation results are used to illustrate the significance of the calibration ring-oscillators (ROs). The chapter also discusses how the pulse broadening and narrowing effects inside the delay chains of the detectors can be a risk in measurement accuracy. Chapter 4 also provides radiation test results on the ST1 chip. In the heavy-ion test, OR2X8 chains were observed to be more sensitive than other circuits. A laser test was performed to investigate the reason. Then the chapter discusses the influence of transistor

mismatch on pulse distortion effects, using the SPICE simulation result. The TID test results (both at the University of Saskatchewan and at the European Space Agency) are also introduced in this section. Finally, the laser test results at the Naval Research Lab are attached to prove the pulse broadening effect in the OR2X8 chains. The SET soft error rate vs. clock frequency is also investigated.

Chapter 5 investigates the second chip, AR0, designed in this project. The AR0 chip includes five ARM cores with different level of circuit protection. The details of the chip are discussed, including the peripheral circuits, the control logic, the support instruction, the operating frequencies, the logic protection method and the test schemes. The fault injection simulation result is also shown to prove the performance of the approximate logic protection method.

The whole work has been summarized in chapter 6, which also outlines the future research work in this project.

Chapter 2: BACKGROUND INFORMATION

2.1 Single Event Effects

2.1.1 Charge Deposition and Collection

As introduced in the first chapter, various kinds of energetic particles can cause SEEs. However, the basic mechanism in SEEs generation is quite similar, among which charge deposition and charge collection play key roles [35-40]. When an energetic particle travels through a semiconductor material, extra electron and hole pairs are generated along the particle track (Figure 2.1). There are two ways an energetic particle generates charges in semiconductor materials, namely direct ionization and indirect ionization [41-43].

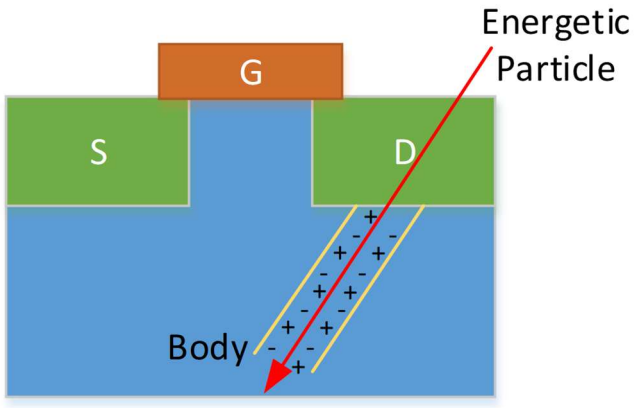


Figure 2.1 Charge Track in MOS Device [3]

If the incidence particle, such as a heavy ion has a charge, when passing through the material, it can generate extra charge pairs while losing its energy. Before it loses all its energy and stops, it will release the charge pairs within a range of area along its track. Heavy ions deposit their energy in the material and generate SEEs mainly in this way.

Light particles normally cannot generate enough charge to produce SEEs directly. However, they can still induce SEEs in devices through indirect ionization [44, 45]. When an energetic particle such as a proton or neutron, travels through semiconductor material, it may have either an elastic

or inelastic collision with a semiconductor nucleus. The nuclear reactions may generate secondary charged particles, which can generate charge along their tracks.

If the generated electron-hole pairs concentrate near a node, which has high electric field, the extra charges will drift towards the electric field and get absorbed efficiently. With the separation of the electrons and holes, a current turbulence can be observed at the node. There are two phases in the generated current spike: a sharp leading edge which can last in the scale of tens of picoseconds, and a tailing edge that can last hundreds of nanoseconds or even longer [3]. The first part, the leading edge, occurs because of the charge that is collected at the original depletion area and the funnel region. The delayed part is due to the charge collection from the diffusion area in the silicon body. Figure 2.2 shows the charge deposition and collection flow when a particle strikes at the inversed PN junction. Figure 2.3 shows the current spike waveform.

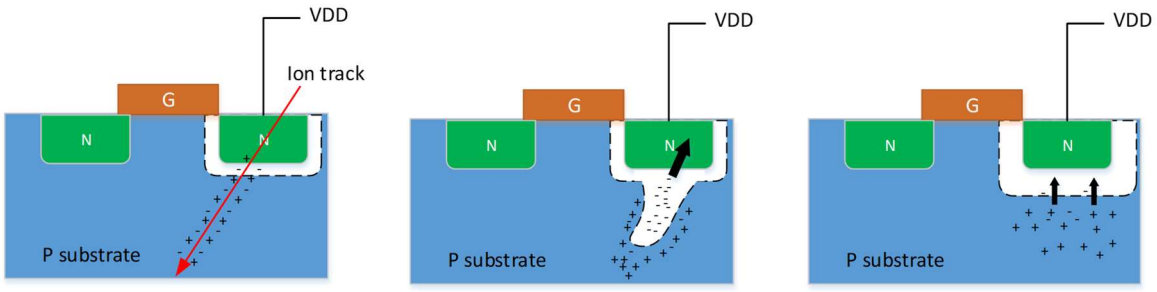


Figure 2.2 Charge Deposition and Collection Flow [41]

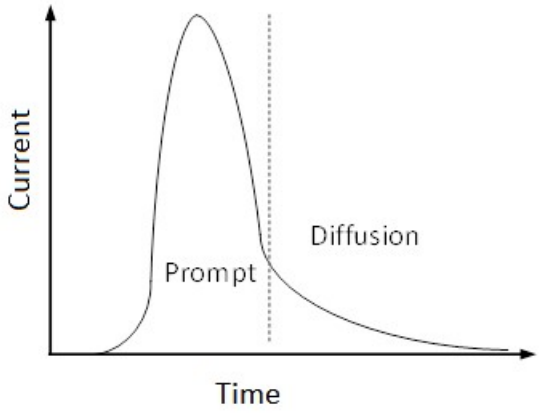


Figure 2.3 Current Pulse in an Inversed PN junction [41]

2.1.2 Single Event Upset

The current spike at an inversed PN junction may cause voltage fluctuation at the electrode. If the energy of the striking particle is large enough, the voltage at the node may be flipped in a short time, which means a voltage pulse is generated.

When the radiation-induced pulse occurs in a digital storage cell, such as a flip-flop or an SRAM cell, the stored value can be flipped by the particle hit, which is called Single Event Upset (SEU). Figure 2.4 shows two back-to-back invertors, which are the basic element of the storage structure in SRAMs and latches. As discussed above, the inversed PN junctions can effectively collect the extra charge when hit by a particle. As a result, the drain nodes of transistors M1 and M4 are the sensitive nodes, which are susceptible to SEEs. If an ion strikes at either of these nodes, a transient voltage pulse can be generated due to the current spike. With the increase of the ion LET, the voltage pulse is larger. If the pulse is wide enough, it will flip the signal level in the invertor loop, and cause an upset in the storage cell (shown in Figure 2.5).

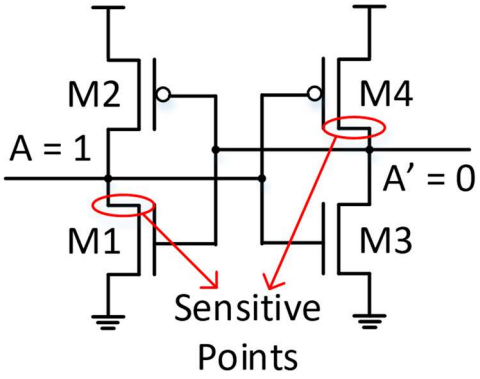


Figure 2.4 Back-to-back Invertor Sensitive Points [3]

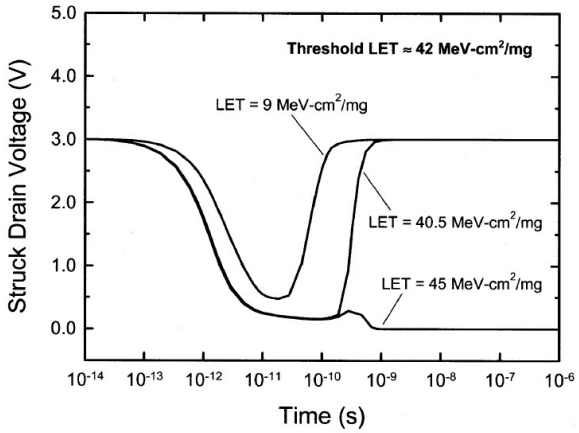


Figure 2.5 Transient Pulses with Different LET Ion Strike in a SRAM Cell [3]

2.1.3 Single Event Transient

Different from an SEU, which happens in a sequential cell, a Single Event Transient (SET) is the single event effect related to the combinational circuits in a digital system. Since the combinational logic itself cannot store a value, if a transient is not captured by a flip-flop or latch in later stage, it will not influence the system functionality. Consequently, the soft error rate caused by SETs is a function of the clock speed and other factors. Figure 2.6 shows a simple example of how the clock frequency influences the SET soft error rate. When an ion strikes the buffer in Figure 2.6, it generates a transient pulse at the output, BF_OUT. Then the pulse propagates to two flip-flops which belong to different clock domains. Since the frequency of CLK_B is twice the frequency of CLK_A, flip-flop B has more possibility to capture the transient pulse. If an SET pulse is caught by a flip-flop, the wrong output may impact on the functionality of the circuit or even the whole digital system. Moreover, if an SET happens in the system clock tree, it will generate an extra clock edge, which will scramble the sequential logic and cause a system failure.

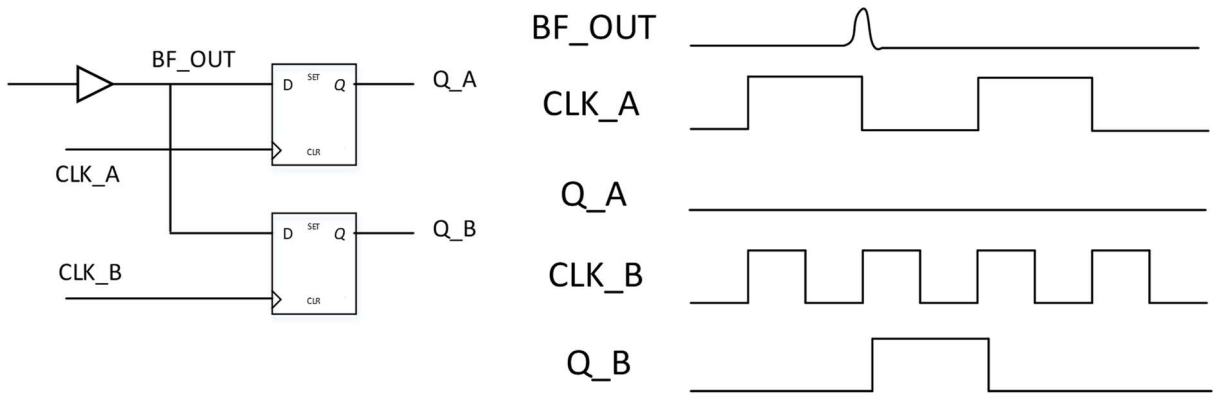


Figure 2.6 Clock Frequency Influence on SET Soft Error Rate

2.1.4 Single Event Multiple Transient and Multiple Bits Upset

Recently, with the evolution of technologies, ICs have been reported as more susceptible to radiation particles. The explanation for this phenomenon is multiple cells (combinational or sequential) are influenced due to multiple node charge collection. Because of the downscale of modern technologies, the electron-hole pairs generated by an incident particle are collected by the striking node as well as the adjacent nodes. This effect is known as multiple node charge collection or charge sharing. If the ion is energetic enough to generate charges which can flip the striking node and the nearby nodes, multiple transients may happen in the circuits, an occurrence which is call Single Event Multiple Transient (SEMT). When the transients cause more than one bit upset in a memory or storage array circuits, multiple bits upset (MBU) happens [46]. Observing SEMTs was also an initial purpose in an earlier project (chapter 3).

2.1.5 Single Event Latchup

In 1979, another single event effect called Single Event Latchup was reported in [47]. In modern CMOS technologies, PMOS devices are fabricated in the n-well and share the same substrate with the NMOS transistors. As shown in Figure 2.7, there are two parasitic transistors in a CMOS device. The n-type active area, the p-substrate and the n-well construct a parasitic NPN transistor (T1), and the p active area, the n-well and the p-substrate form a lateral PNP transistor (T2). The p-substrate and the n-well also have their equivalent resistors in this structure (R1 and R2 in Figure

2.7). When a current spark occurs in the p-sub, the NPN transistor will open, and the current in the n-well transistor (R2) will be enlarged, which can increase the IR drop in the n-well. When the voltage drop in R2 is high enough to turn on the T1 NPN transistor, there is a direct path from power to ground, which can cause the latchup effect in the device.

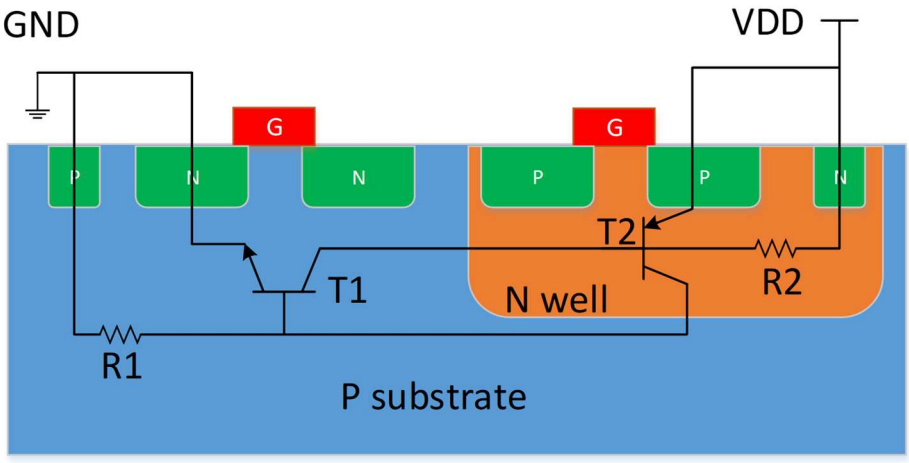


Figure 2.7 Parasitic Structure in a CMOS Device [48]

Different from the SEEs discussed above, the SEL may result in a hard error since there is a short path between VDD and GND. The large current may damage the device if no proper protection is in place.

2.2 SEE Test Methodologies

Since SEEs can impact system reliability, various kinds of irradiation tests have been introduced to investigate the SEE influence on ICs. The ideal test method is to launch the digital systems into space to perform the testing, but it is very costly and time consuming. Thus, ground-level accelerated irradiation experiments are usually adopted.

2.2.1 Particle Tests

To imitate the irradiative environments, such as in space or in a nuclear power plant, particle accelerators are used for particle tests. There are many particle accelerator facilities around the world which can be used for SEE experiments. The 88-Inch Cyclotron facility in the Lawrence

Berkeley National Lab (LBNL) can provide both heavy-ion and light-ion particle beams. It can provide four standard ion cocktails with 4.5, 10, 16 and 30 MeV/nucleon. The Radiation Effects Facility (RADEF) is located at the University of Jyväskylä, Finland (JYFL). RADEF provides proton and heavy-ion beam lines in the same cave and the electron beam from a linear accelerator. TRIUMF is an accelerator-based research center in Canada for energetic particle and nuclear science study [49]. The 500 MeV cyclotron facility can provide four proton beam lines with an energy range from 20 to 500 MeV [50, 51]. Thermal (low-energy) and high-energy neutron tests can also be performed at TRIUMF.

2.2.2 Pulsed Laser Test

A laser can also be used for SEE investigation because of the charge generation by the photon effects. There are three kinds of the photon effects: the photoelectric effect, the Compton effect and pair production [52].

The photoelectric effect is related to low-energy photons. When a low-energy photon interacts with an atom in semiconductor materials, it will free an inner electron from the atom by losing all its energy. It produces an ionized atom and a free electron. When the electron in an outer shell falls into the inner orbit, a low-energy photon is generated.

When a high-energy photon strikes semiconductor materials, it frees charges through the Compton effect, which is also known as the Compton scattering. When a photon has a collision with the target atom, the photon transfers part of its energy to free an electron from the atom and also generates a low-energy photon.

A pair production is generated by an extremely high-energy photon. The photon hits a target atom, generating an electron-positron pair. A positron is similar to an electron but it has an opposite polarity of charge.

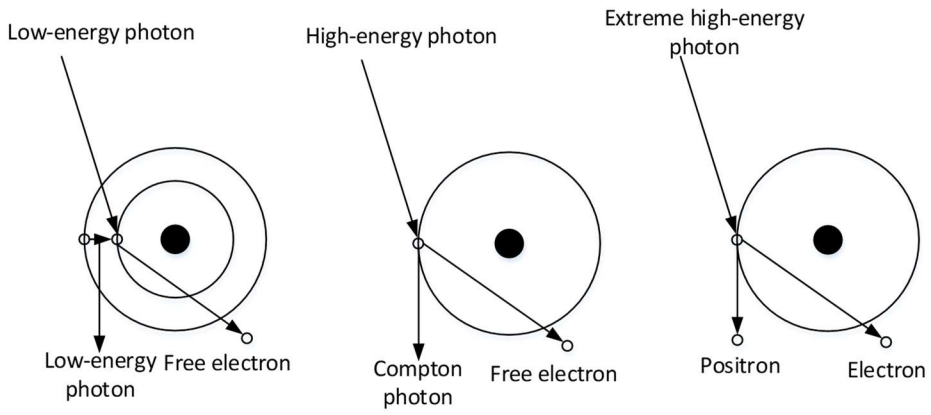


Figure 2.8 Photon Effects [7]

Because of the cost and the ease of access, the pulsed laser test is widely used in single event effects research [53-60]. Compared to the ion or proton test, the pulsed laser test is much simpler. A laser pulse with around 1 um diameter is focused or scanned on a device, and the laser energy is increased to test the relationship between the soft error rate and the pulse energy.

There are two main types of pulsed lasers: Single Photon Absorption Laser (SPA) and Two Photon Absorption Laser (TPA). The wavelength of SPA is relatively short, which makes it difficult to penetrate the silicon and reach the active area. Therefore, TPA is preferable in modern laser test methodology.

2.3 Total Ionizing Dose

The total ionizing dose effect [61-68] is the degradation that is caused by large number of high-energy particles over a long period expose. In the irradiative environment, the TID effect can potentially cause a device hard failure. When exposing a device to a radiation beam, the energetic particles can generate charged pairs in the SiO_2 layer when depositing enough energy to free electrons from semiconductor nucleus. If the generated electron-hole pairs get trapped at the Si-SiO_2 interface, they will form an electric field inside the SiO_2 layer, which can gradually degrade the electric character of the device. Figure 2.9 shows this process. When a high-energy particle travels through the SiO_2 layer, it will generate charged pairs along its track. The charge density depends on the irradiation type. After the initial recombination, the un-recombined charges are pulsed to the material interface by the electric field. These charges may be trapped at the Si-SiO2

interfaces and form a reversed electric field. With the accumulation of the trapped charges, the generated electric field can finally degrade the electric characteristics of the device.

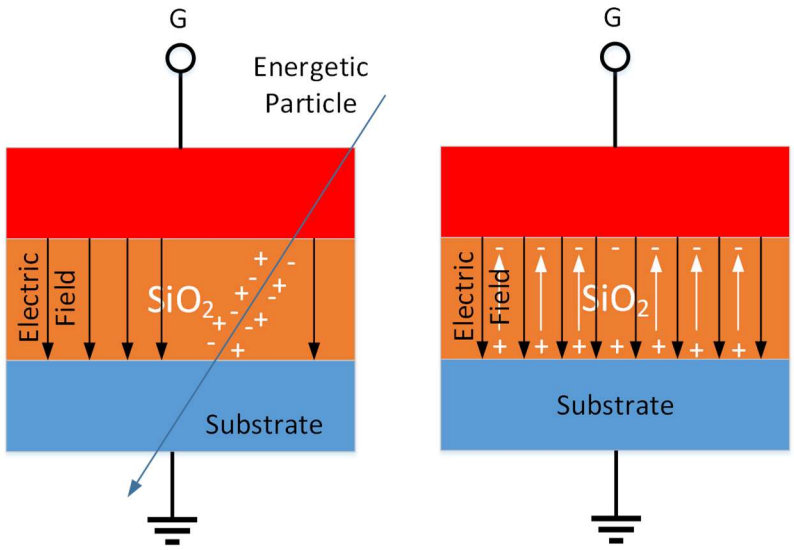


Figure 2.9 Charge Injection Process in SiO_2

The accumulative charges can result in a decrease of the NMOS threshold voltage and an increase of the PMOS threshold voltage, which means the transistor becomes slower and the gate delay gets higher. In addition, the transistor leakage current can be enlarged when it is in the off state. In the extreme case, the PMOS can be off permanently in the nominal operation voltage, which will result in the malfunction of the circuits.

In modern technologies, the gate oxide layer is down to nanometer scale, which can effectively relieve the TID effects [33]. However, in SOI technologies, except for the gate oxide and the Shallow trench isolation (STI), there is an additional isolation layer (Buried Oxide) between the substrate and body, which makes the TID analysis of SOI devices much more complex.

2.4 UTBB-FDSOI Technology

In the 1960s, Silicon-On-Insulator technologies were developed for military and space [16], [35]. Compared to bulk technologies, SOI technologies have an additional dielectric isolation between the substrate and the silicon body, which can prevent latchup by totally separating the transistors. Initially, SOI technologies were less attractive because of the introduction of a series of parasitic

structures. Since the 1990s, because of the significant improvement in SOI wafer quality, they have become widely used, especially in hard irradiation environment applications.

The Fully Depleted Silicon-On-Insulator (FDSOI) is an innovative technology based on the planner process. There are mainly two innovative technics in state-of-the-art FDSOI technologies. The first innovation is a very thin insulator layer, which is also known as buried oxide, positioned between the base silicon and the active area. Secondly, the transistor channel is implemented by a super-thin silicon film. Ultra-Thin Body and Buried Oxide (UTBB) Fully Depleted SOI (FDSOI) technologies are known as a combination of these two innovations together.

Compared to its bulk competitor, FDSOI technologies have much better transistor electrostatic

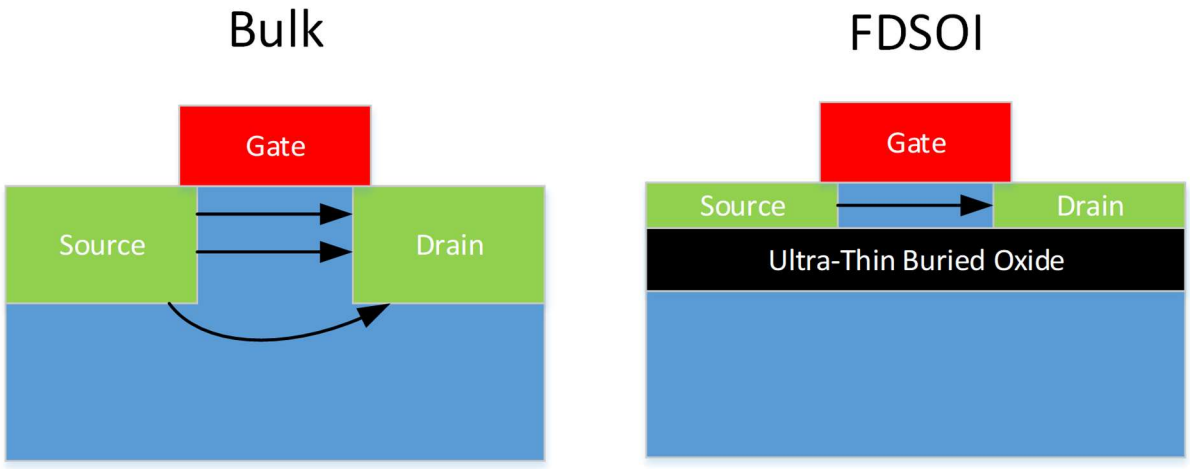


Figure 2.10 FDSOI Cross Section [16]

characteristics. Because the buried oxide lowers the parasitic between the source and the drain, the transistor switching speed increases and the leakage current decreases dramatically. Also thanks to the ultra-thin insulator layer, back-gate biasing voltage can transmit more efficiently than in bulk technologies, which makes it possible to control the transistor by polarizing the substrate. In other words, the transistor performance can be controlled dynamically through adjusting the back-gate voltage.

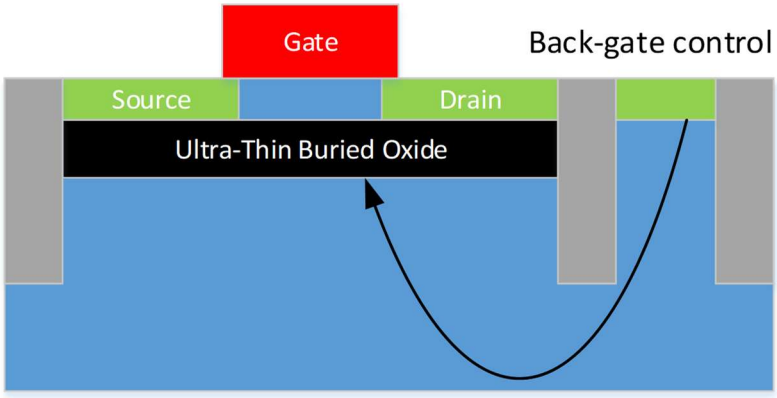


Figure 2.11 FDSOI Back-gate Control [82]

Chapter 3: SET Pulse Measurement Chip (ST1)

The first test chip was designed to study Single Event Transient (SET) pulse characterization. When researching the SEUs, we focus mostly on the cross-section, in other words, error rate vs. irradiation beam fluence. However, in the SET research, besides the error rate, the pulse width distribution is also an area of interest.

Generally, there are two methods for doing the pulse measurement: on-chip and off-chip. Considering the SET pulse width is at the magnitude of picosecond, a precise off-chip measurement is hard to implement. As a result, the on-chip measure circuits were implemented in the ST1 chip.

Three kinds of the SET pulse detectors were implemented: a Pulse Capture detector, a Vernier detector and a Pulse Filter detector. To study SET event rate vs. clock frequency, a high-speed CREST chain with 4096 stages was also implemented in the ST1 chip. In this chip, there are also four types of Ring Oscillators (ROs) which can be used to study TID effects. The ST1 test chip focuses on SET characterization research. The research result can be used to estimate the influence of SETs in actual complex digital circuits. Moreover, the appropriate mitigation method can use the ST1 chip radiation test result as a reference.

3.1 Top-Level Specification

A top-level diagram of the test chip is shown in Fig. 3.1. The main part of the test chip consists of 96 experiment circuits for measuring transients. In addition to the experiments, there is a common infrastructure which is used for configuration, for reset and clock management, and for error reporting.

There are three main clock regions in the chip. The configuration logic consists of shift registers that are clocked through the external serial input interface and designed to operate at low speed (nominally 10MHz). The logic for the experiments is driven by the test clock which is created by

the clock generation module. Finally, there is a control clock (nominally 10MHz) which is used to control the logic for error reporting (Table 3.1).

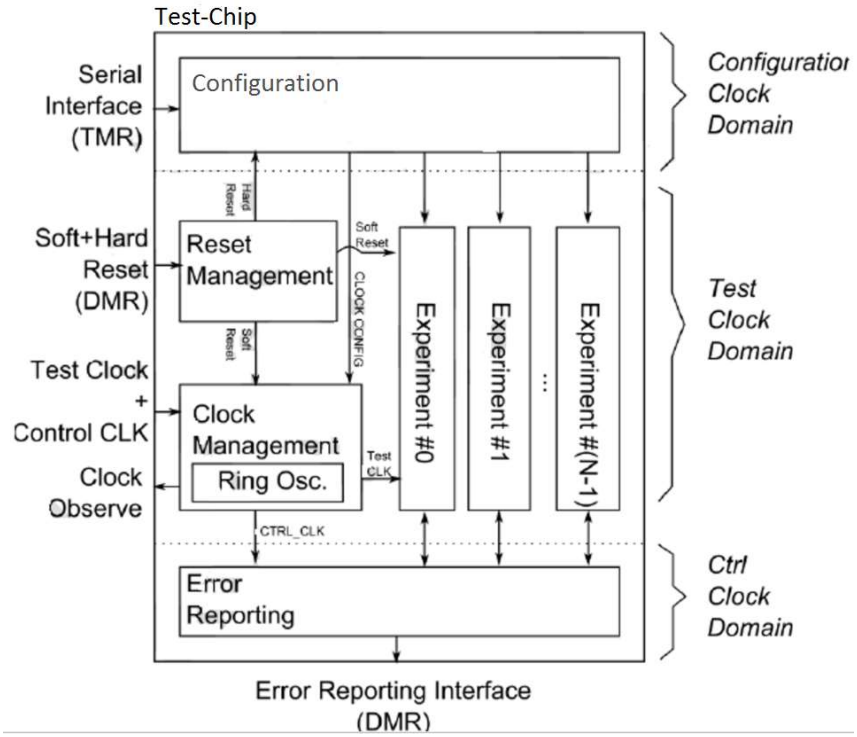


Figure 3.1 SET Test-Chip Top-Level Logical View

Table 3.1 ST1 Test Chip Pinout

Pin Name	Direction	Type	Description
Configuration Interface (8 Signals)			
CONF_CLK	IN – CLK	1.8V CMOS	Configuration CLK
CONF_DIN	IN	1.8V CMOS	Configuration Data
CONF_EN	IN	1.8V CMOS	Configuration Enable
CONF_XFER_A	IN	1.8V CMOS	DMR – Transfer Enable (shift -> in)
CONF_XFER_B	IN	1.8V CMOS	
CONF_DOUT	OUT	1.8V CMOS	Configuration Data Output (debug)
CONF_IN_OK	OUT	1.8V CMOS	Configuration In Parity Check
CONF_LIVE_OK	OUT	1.8V CMOS	Configuration Live Parity Check
Clock and Reset (5 Signals)			
TEST_CLK_IN	IN – CLK	1.8V CMOS	CREST Test CLK
CTRL_CLK_IN	IN – CLK	1.8V CMOS	Control Circuitry CLK
CLK_OBS_OUT	OUT	1.8V CMOS	Clock Observation Signal
RESET_A	IN	1.8V CMOS	DMR – Global Reset
RESET_B	IN	1.8V CMOS	
Error Reporting Interface (17 Signals)			
ERR_VLD_A	OUT	1.8V CMOS	DMR – Error Valid Indication
ERR_VLD_B	OUT	1.8V CMOS	
SEL_NUM_DAT	IN	1.8V CMOS	Choose NUM or DAT Output
ERR_ACK	IN	1.8V CMOS	Error report acknowledge
ERR_NUM_DAT [7]	OUT	1.8V CMOS	Either the Current Event Reporting Test Number or the Reported Data for a selected sensor
ERR_NUM_DAT [6]	OUT	1.8V CMOS	
ERR_NUM_DAT [5]	OUT	1.8V CMOS	
ERR_NUM_DAT [4]	OUT	1.8V CMOS	
ERR_NUM_DAT [3]	OUT	1.8V CMOS	
ERR_NUM_DAT [2]	OUT	1.8V CMOS	
ERR_NUM_DAT [1]	OUT	1.8V CMOS	
ERR_NUM_DAT [0]	OUT	1.8V CMOS	
ERR_DAT_SEL [2]	IN	1.8V CMOS	Signals to Select Error Data (if it is more than 8 bits)
ERR_DAT_SEL [1]	IN	1.8V CMOS	
ERR_DAT_SEL [0]	IN	1.8V CMOS	
ERR_CLR_A	IN	1.8V CMOS	DMR – Clears the Current Error
ERR_CLR_B	IN	1.8V CMOS	
Analog Power (2 Pins)			
VDD_{analog}	IN	0.6V – 1V	Power for Variable Voltage SET Sensors

An approximate floorplan of the SET test chip is shown in Figure 3.2.

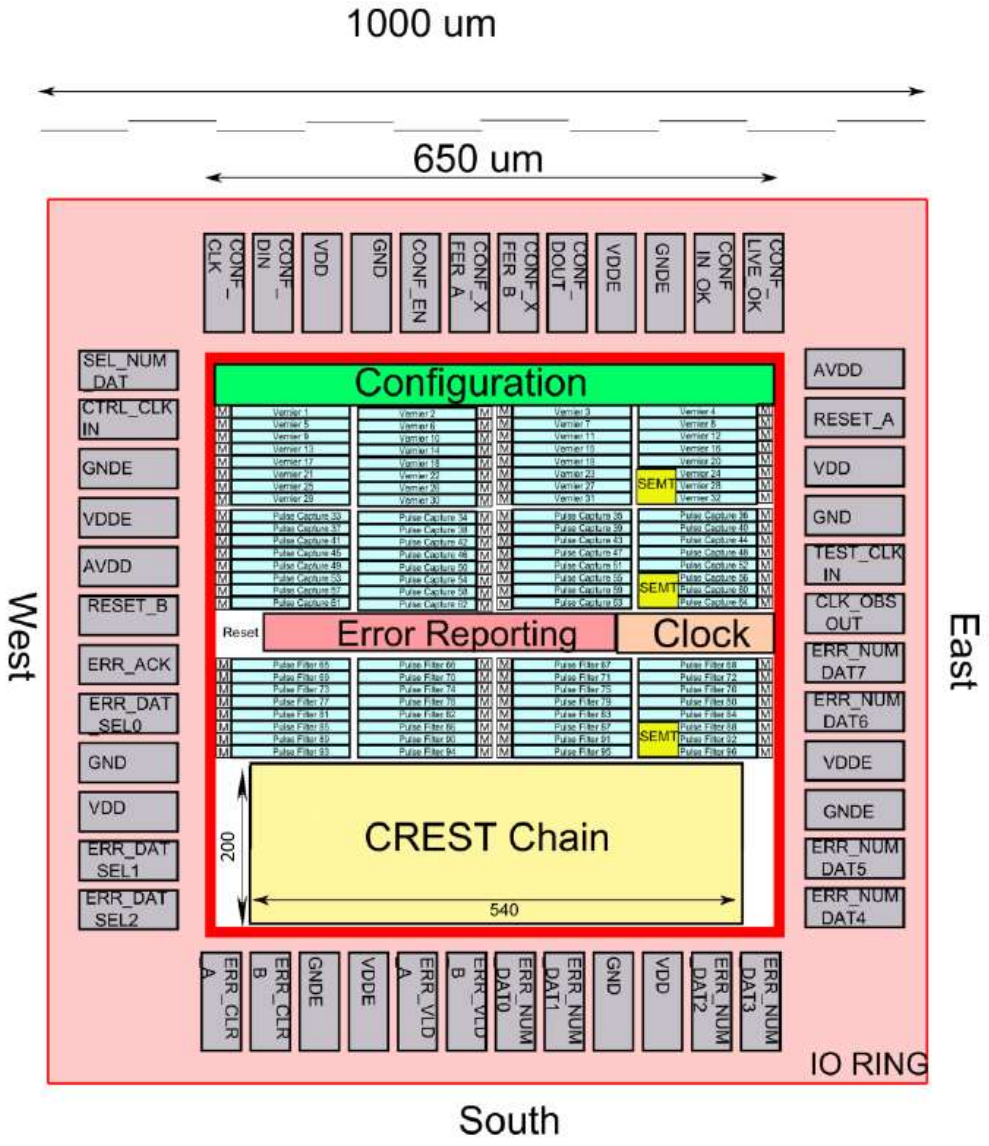


Figure 3.2 ST1 Test Chip Floor Plan

3.2 Configuration Interface

Many aspects of the test chip require configuration. For example, the clocking modes are configurable and some of the sensors have modes which can be enabled. The configuration is input to the chip using a serial shift interface. All the input signals on this interface are TMR and the

interface is designed so that the device can be reconfigured during radiation. However, normally the radiation would be stopped during reconfiguration.

The configuration interface is clocked using an independent TMR serial clock (CONF_CLK_{A, B, C}) and can thus function in the absence of other clocks. In total, there are 192 bits of configuration data. Internally every 16 bits of configuration data is protected with an odd parity bit (16D+1P). The parity of the configuration data is continuously checked (18 groups of 16+1 bits). The outputs of the 12-parity checkers are ANDed together, and this is made available on a primary output, providing an indication that the configuration data is stored correctly. A high-level view of the configuration interface is shown in Figure 3.3.

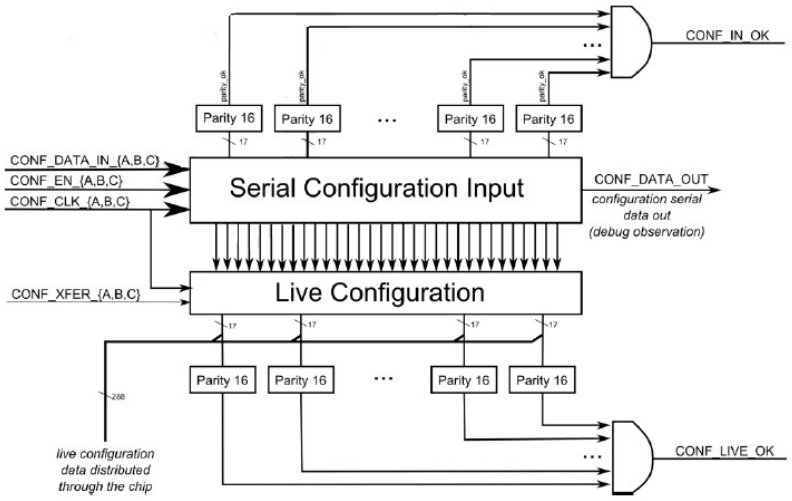


Figure 3.3 High-level View of Configuration Interface

In order to enable live reconfiguration, two copies of the configuration data are stored. One copy is shifted in serially (Serial Configuration Input) and the other, the live configuration, is distributed in the chip. The live configuration can be updated when CONF_XFER_{A, B, C} are asserted on a rising edge of the configuration clocks. In this way, the full configuration data can be updated automatically. The live configuration is unaffected during the time the new configuration is being shifted in.

The detailed structure of the serial input configuration interface is shown in Figure 3.4. The clock and the data input are independent for each of the TMR chains (A, B, C). When CONF_EN_{A, B, C} is asserted (1), the input data (CONF_DATA_IN_{A, B, C}) is shifted into the chains on

the rising edge of the configuration clock (CONF_CLK_{A, B, C}). When CONF_EN_{A, B, C} is de-asserted (0), then the contents of each stage is recirculated through a TMR voter.

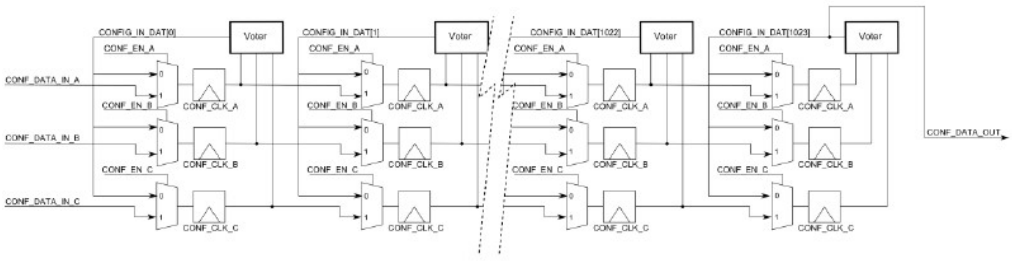


Figure 3.4 TMR Input Configuration Shift Register

The live copy of the configuration data is loaded in parallel from the input shift register. This transfer occurs on a rising clock edge (CONF_CLK_{A, B, C}) when CONF_XFER_{A, B, C} are asserted. When CONF_XFER_{A, B, C} are not asserted, the configuration is recirculated. Separate voters are used for recirculating the configuration for each copy (A, B, C). In this way, an error in the voter does not cause the configuration to be permanently corrupted. One of the voter outputs (C – chosen arbitrarily) drives the actual configuration data to the rest of the chip. The live configuration storage chain is illustrated in Figure 3.5.

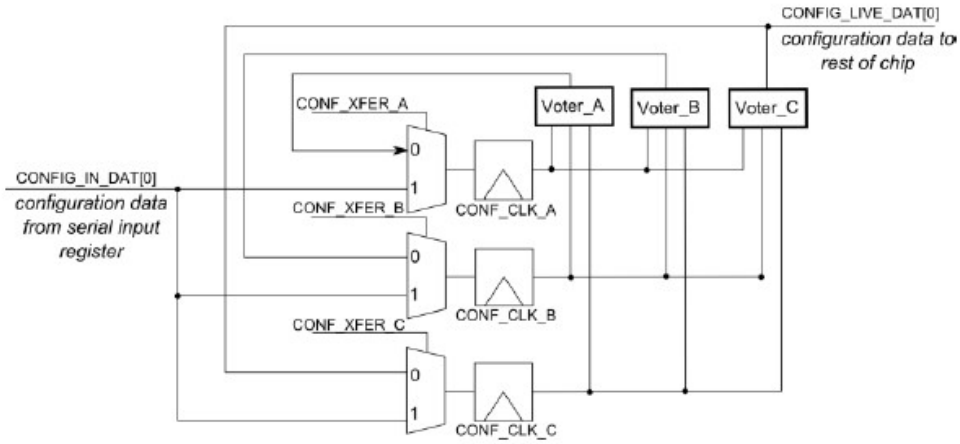


Figure 3.5 TMR Input Configuration Shift Register

3.3 On-Chip Clock Generation

3.3.1 Clock Generation logic

Many of the experiments on the chip require a test clock and, in most cases, it is necessary to vary the frequency of the test clock. A Phase-Lock Loop (PLL) is not available for this design, and there are limits on the bandwidth through the pads. For this reason, there is the option to generate an on-chip clock using a programmable Ring Oscillator (RO). An overview of the clock generation circuitry is shown in Figure 3.6.

Two techniques are used to reduce the sensitivity of the clock generation circuitry to radiation effects. The first is the use of the largest possible invertors in the Ring Oscillator (RO). Using larger cells in the RO has two main advantages. First, larger cells are less sensitive to transients. Second, larger cells have a higher inertial delay and will filter transients. This filtering effect greatly reduces the probability that the ring oscillator will start to oscillate at a harmonic frequency due to a transient.

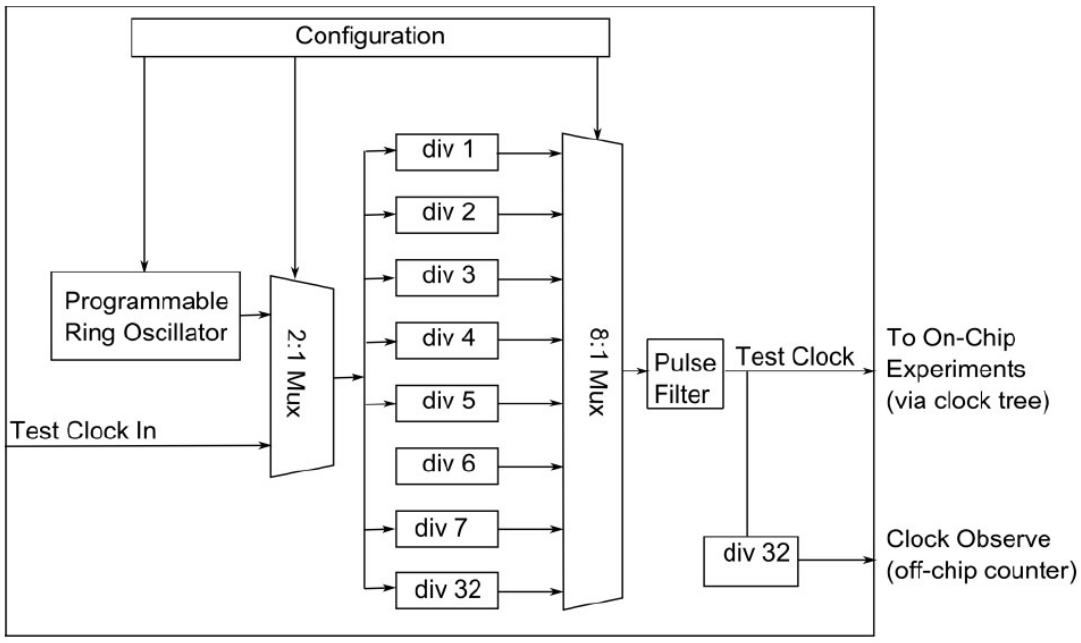


Figure 3.6 High-level View of Clock Generator

The second SEE mitigation technique is the Pulse Filter placed at the output of the clock generation circuitry. This filter must block both positive and negative transients and this is achieved with the circuit shown in Figure 3.7.

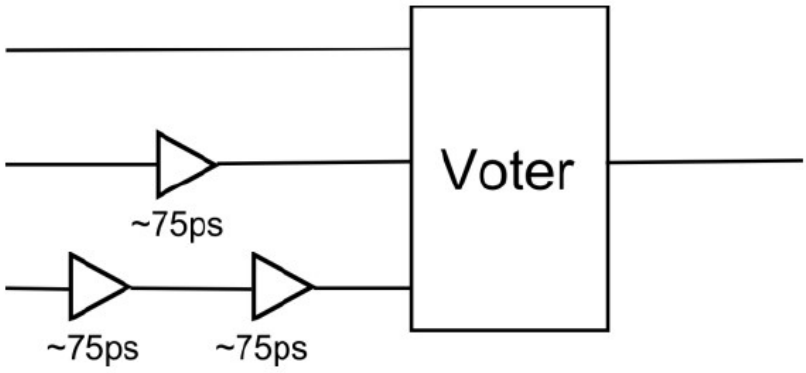


Figure 3.7 Pulse Filter for Clock Generator

The clock for the experiments either comes from the external test clock (Test Clock In) or is generated from the programmable RO, and this is controlled by the configuration bit EXT_CLK_SEL. In either case, it can be selectively divided by either 1, 2, 3, 4, 5, 6, 7, or 32. The selection of divisors is chosen to give the broadest range for the resulting frequencies, and this is controlled by the configuration bits DIV_SEL[2:0]. The division-by-32 option is provided as a contingency in case it is necessary to run the circuits at very low frequencies. For the CREST experiments, when the chain is clocked with the division-by-32 clock, the frequency will be so low that effectively only the SEU component will be measured. In all cases, a divided version of the selected test clock is made available on a dedicated output pin (clock observation). During operation, this is sent to a counter in the off-chip FPGA tester and is used to measure the frequency of the test chip.

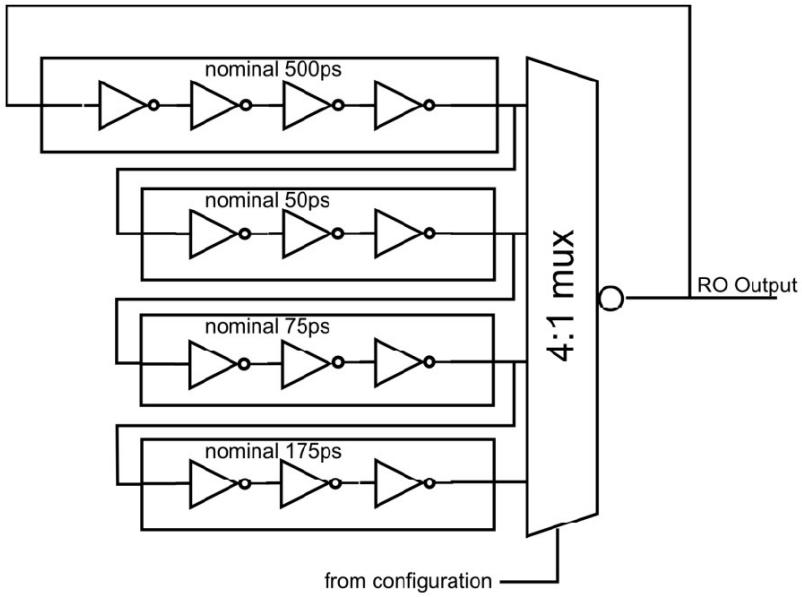


Figure 3.8 Programmable Ring Oscillator

The design of the programmable RO is shown Figure 3.8. There is an initial chain with a nominal delay of 500ps (2GHz frequency). Then, through a 4:1 mux, additional delay can be added in increments of 50ps, 75ps and 175ps, and this selection is made by the control bits RO_SEL. Taken together, the programmable RO and the programmable divider make it possible to generate a wide range of frequencies for the on-chip test clock, as shown in Table 3.2.

Table 3.2 Available On-Chip Clock Frequencies

RO Delay (ps)	RO Freq (MHz)	DIV 1 (MHz)	DIV 2 (MHz)	DIV 3 (MHz)	DIV 4 (MHz)	DIV 5 (MHz)	DIV 6 (MHz)	DIV 7 (MHz)	DIV 32 (MHz)
500	2000	2000	1000	667	500	400	333	286	63
550	1818	1818	909	606	454	364	303	260	57
625	1600	1600	800	533	400	320	267	229	50
800	1250	1250	625	417	313	250	208	179	39

3.3.2 Clock Observation Circuitry

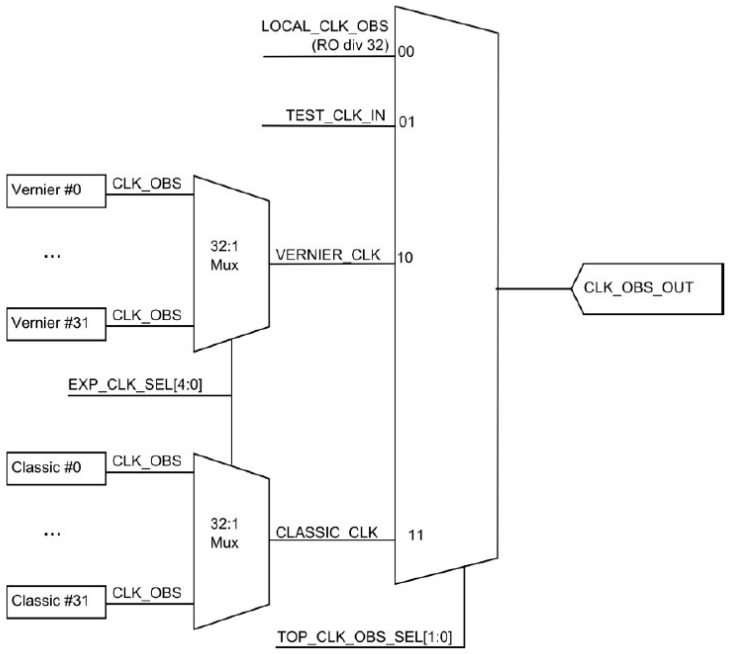


Figure 3.9 Clock Observation Muxing

For debugging and calibration purposes, the on-chip clocks can be observed on the output pin CLK_OBS_OUT. The clock that is output on this pin can come from one of four sources, selected by TOP_CLK_OBS_SEL configuration bits:

1. the clock from the local ring-oscillator (divided by 32);
2. the externally provided clock (TEST_CLK_IN);
3. the clock from one of the selected Vernier detectors (selected by EXP_CLK_SEL[4:0]);
4. the clock from one of the selected classic detectors (selected by EXP_CLK_SEL[4:0]).

The clock observation muxing hierarchy is shown in Figure 3.9.

3.4 Error Reporting Interface

When an error is detected in the test chip, it is reported to the tester through the error reporting interface. The chip is designed such that all the experiments are active in parallel. When any one

of them detects an error, the error number (N) is reported on the error reporting interface. Figure 3.10 shows the timing diagram for an error reporting event from the test chip to the tester.

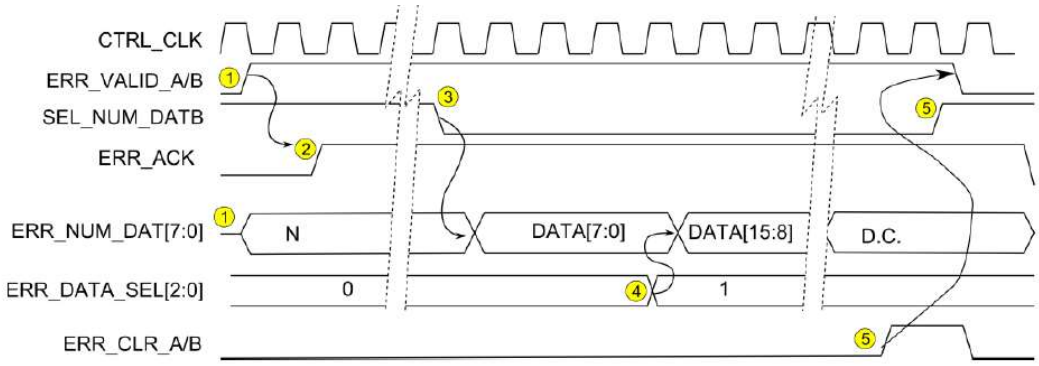


Figure 3.10 Timing Diagram for Error Reporting Event

Most of the control signals are duplicated (DMR) to enable the detection of erroneous transactions. In the figure, the replicated signals (A/B) are only shown once. When an error occurs, the first step (1) is that the test chip signals the error to the tester by asserting ERR_VALID_A/B and by indicating the error number on the ERR_NUM_DAT[7:0] bus.

Note that the ERR_NUM_DAT[7:0] bus is multiplexed to perform two functions. If SEL_NUMDATB is 1, then the current error number is output on the bus. If SEL_NUM_DATB is 0, then the bus (ERR_NUM_DAT[7:0]) outputs eight bits of data from the currently selected experiment. By default (e.g., in the absence of an error), the tester drives the SEL_NUM_DATB to 1 so that the error number is output.

After the tester observes an error (based on ERR_VALID_A/B), it acknowledges the error (2) by asserting ERR_ACK. This has the effect of locking the error number (N), so that it will no longer change. At this point, the tester records the error number and is now ready to access the data associated with that error.

To do this, the tester de-asserts SEL_NUM_DATB in order to start reading the data from the experiment. Each experiment can output up to 40 bits of data. The data is multiplexed, 8 bits at a time, onto the ERR_NUM_DAT[7:0] bus. The selection of which 8 of the 40 bits is output comes from ERR_DATA_SEL[2:0]. After the tester has read the first byte of data, it can select the subsequent bytes, by updating ERR_DATA_SEL[2:0], as shown in step (4).

Finally, in step (5), when the last piece of data has been read, the tester clears the error by asserting ERR_ACK_A/B. This causes ERR_VALID_A/B to be de-asserted (assuming no other errors are present). The tester should also clear SEL_NUM_DATB, so that when the next error occurs, the error number can be recorded. At this point, the test chip is ready to process the next error.

It is, of course, possible that a second experiment may record an error before the previous error has been processed. In this case, the second error is recorded by the tester after the first error has been fully logged. In this situation, after ERR_CLR_A/B is pulsed, instead of ERR_VALID_A/B being cleared, it would stay asserted. In this case, a new error number then would appear on ERR_NUM_DAT[7:0], and it would be processed in the same way.

The circuit diagram of the main portion of the error reporting logic is shown in Figure 3.11. On the left of this figure, we can see that each experiment outputs a signal, “EVENT_DETECTED”, indicating whether it has detected an error. These are bit-wise ANDed with the enable bits which come from the configuration array (DET_ENABLE[127:0]). A 128-bit priority encoder selects which experiment will report its error. The resulting 7-bit value is captured in a register (protected with TMR). If the primary input SEL_NUM_DATAB is asserted, this flows to the output pins as ERR_NUM_DAT[7:0].

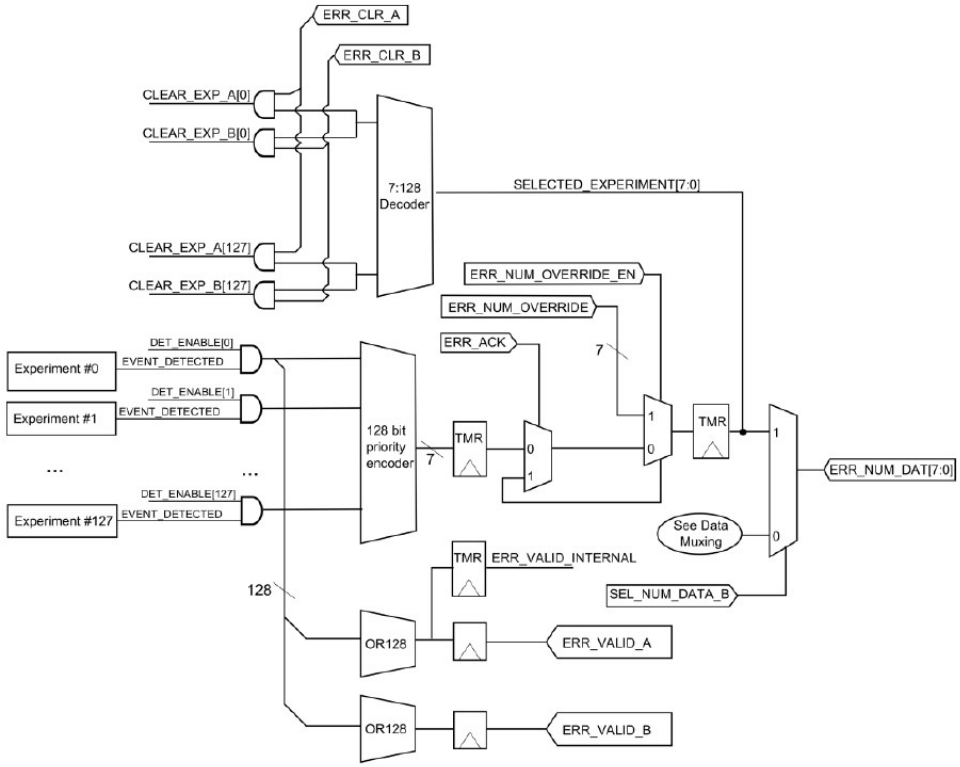


Figure 3.11 Circuit Diagram of Control Logic for Error Reporting

The primary input pin, ERR_ACK, is used to lock the SELECTED_EXPERIMENT. When ERR_ACK is low, the newly selected error number is loaded into SELECTED_EXPERIMENT, and when it is high, the selected experiment is locked. The only state elements in the error reporting logic are the output of the priority encoder and the selected experiment. Both of these 7-bit registers will be implemented using TMR. The error reporting interface operates at a low frequency so SETs in the combinatorial logic have a very low chance of being captured and will almost certainly be filtered through the IO pads. The flops for the ERR_VALID_A/B signals are DMR. The external test logic (FPGA) will only react if both ERR_VALID_A and ERR_VALID_B are asserted.

There is a small risk that a transient could cause a glitch on the CLEAR_EXP signals. If this occurs when the selected experiment has not currently detected an error, it is benign, as no error information is stored. In the unlikely event that an SET did occur and cleared an experiment that has currently logged an error, then the data read from that experiment would be invalid. Potentially, this could be detected by the external FPGA if the ERR_VALID_A/B outputs de-asserted before

the FPGA actively cleared the results, and in this case, the FPGA could ignore the partial data that had been read.

As an emergency backup feature, the SELECTED_EXPERIMENT can be manually loaded using the configuration interface. If the configuration bit, ERR_NUM_OVERRIDE_EN, is set to 1, then the SELECTED_EXPERIMENT is loaded directly from the configuration bits ERR_NUM_OVERRIDE[6:0]. In this way, it possible for the external FPGA to directly poll the experiments rather than reacting to the reported errors.

Once an experiment has reported that it has an error (ERR_VALID_INTERNAL=1) and it has been selected, the associated data from that experiment must be read. This is performed by first having the external FPGA set SEL_NUM_DATA_B to 0, which selects the data-path portion, shown in Figure 3.12. Internally, each experiment can have up to 40 bits of data to report. However, each experiment has a 5:1 mux1 controlled by the primary inputs ERR_DATA_SEL[2:0], which selects only 8-bits of data. The 8-bits of output data from each experiment feed to a central 128:1 mux (8-bits wide). This mux is controlled based on the SELECTED_EXPERIMENT. The selected 8-bits of data flow out to the output pins. In this way, under the control of the FPGA, the full 40-bits of data in each experiment can be read, one byte at a time, as illustrated in Figure 3.10.

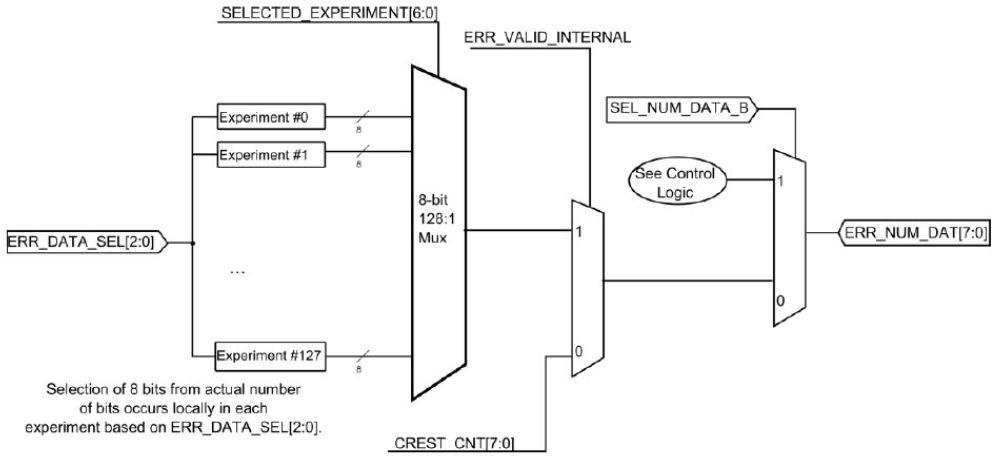


Figure 3.12 Circuit Diagram of Data Muxing Logic for Error Reporting

Note that the CREST experiment is slightly different. In the absence of an error being reported by any of the experiments (ERR_VALID_INTERNAL=0), the default data driven to the 8-bit output

bus is the contents of the CREST error counter (CREST_CNT[7:0]). In this way, it is possible for the external FPGA to monitor “continuously” the count from the CREST experiment.

3.5 Self-Test Experiment

It is essential that the chip can be functionally tested prior to any radiation testing. For this reason, two identical test experiments have been included. These test experiments can be triggered under the control of the FPGA, by programming SELF_TEST_[0|127] to 1. When they are triggered, these experiments cause the chip to report an error as if a radiation event had occurred. The FPGA can then follow the regular sequence to read out 40 bits of data, one byte at a time and then clear the experiment. The structure of the self-test experiments is very simple and is shown in Figure 3.13. Note that through configuration (SELF_TEST_[0|127]_DATA), one of two different data patterns can be selected.

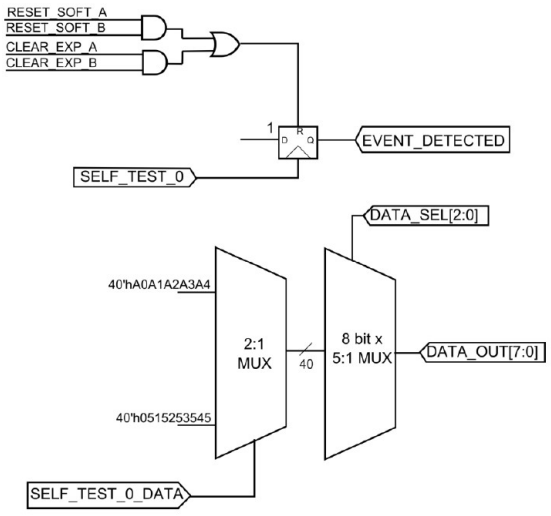


Figure 3.13 Circuit Diagram of Data Muxing Logic for Error Reporting

3.6 SET Test Circuits

3.6.1 Components

The SET test chip contains 128 different experiments which are divided into six categories. In addition to the actual experiments, two pseudo-experiments are included for self-test purposes.

The tester can artificially trigger events from the self-test experiments. The categories of experiments are enumerated in Table 3.3. A detailed list of the 32 SET experiments for each detector is shown in Table 3.4.

Table 3.3 Types of Experiments

Category	Experiments Number
Self Test	0
Vernier Measurement of SETs	1..32
Pulse Capture Measurement of SETs	33..64
Pulse Filter Measurement of SET1	65..96
CREST	97
Self Test	127

3.6.2 Vernier SET Detector

The Vernier SET detector [16] is able to provide extremely accurate pulse-width measurements. The circuit is illustrated in Figure 3.14.

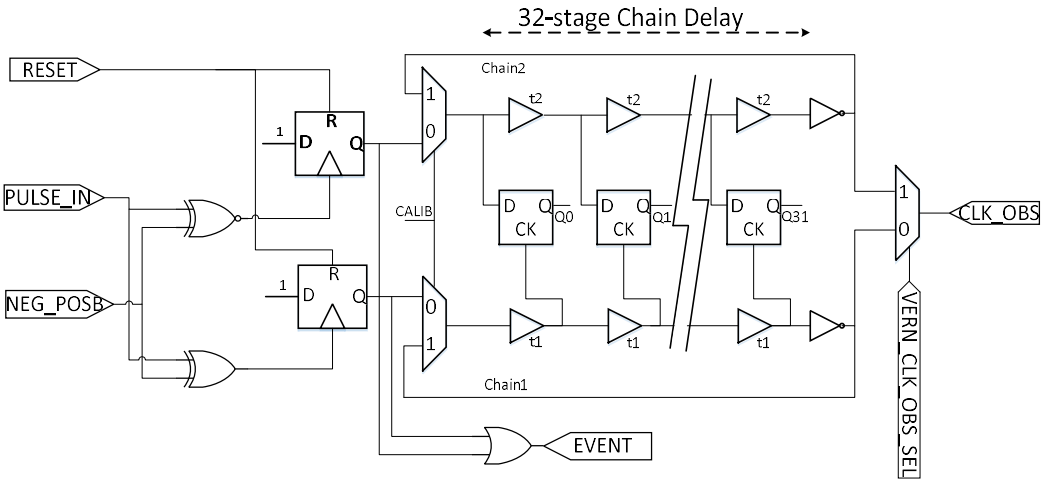


Figure 3.14 Vernier Detector

Table 3.4 SET Test Chip List of SET Experiments

Experiment Index	Details	Bits Config.
1/33/65 (VER/PC/PF)	IVX4 chain – 26 cells – identical with the combinational logic of the CREST chain for comparison	0
2/34/66 (VER/PC/PF)	BFX4 chain – 32 cells – study broadening	1 DET_BUF_INP
3/35/67 (VER/PC/PF)	BFX4 chain – 64 cells – study broadening	
4/36/68 (VER/PC/PF)	BFX8 chain – 64 cells – study drive strength	
5/37/69 (VER/PC/PF)	BFX16 chain – 64 cells – study drive strength	
6/38/70 (VER/PC/PF)	BFX25 chain – 64 cells – study drive strength	
7/39/71 (VER/PC/PF)	BFX33 chain – 64 cells – study drive strength	
8/40/72 (VER/PC/PF)	BFX42 chain – 64 cells – study drive strength	
9/41/73 (VER/PC/PF)	BFX50 chain – 64 cells – study drive strength	
10/42/74 (VER/PC/PF)	BFX67 chain – 64 cells – study drive strength	
11/43/75 (VER/PC/PF)	IVX4 chain – 64 cells – study drive strength	0
12/44/76 (VER/PC/PF)	IVX6 chain – 64 cells – study drive strength	
13/45/77 (VER/PC/PF)	IVX8 chain – 64 cells – study drive strength	
14/46/78 (VER/PC/PF)	IVX17 chain – 64 cells – study drive strength	
15/47/79 (VER/PC/PF)	BFX4 LVT chain – 64 cells – study V_T	1 DET_BUF_INP
16/48/80 (VER/PC/PF)	BFX8 LVT chain – 64 cells – study V_T	
17/49/81 (VER/PC/PF)	BFX16 LVT chain – 64 cells – study V_T	
18/50/82 (VER/PC/PF)	IVX4 LVT chain – 64 cells – study V_T	0
19/51/83 (VER/PC/PF)	IVX6 LVT chain – 64 cells – study V_T	
20/52/84 (VER/PC/PF)	IVX8 LVT chain – 64 cells – study V_T	
21/53/85 (VER/PC/PF)	AND2X8 chain – 64 cells – study gate type	0
22/54/86 (VER/PC/PF)	OR2X8 chain – 64 cells – study gate type	0
23/55/87 (VER/PC/PF)	NAND2X3 chain – 64 cells – study gate type	0
24/56/88 (VER/PC/PF)	BFX4 chain A – 64 cells – study SEMT	1 DET_BUF_INP
25/57/89 (VER/PC/PF)	NOR2X3 chain – 64 cells – study gate type	0
26/58/90 (VER/PC/PF)	XOR2X4 chain – 64 cells – study gate type	1 DET_XOR_INP
27/59/91 (VER/PC/PF)	MUX21X8 chain – 64 cells – study gate type	3 DET_MX_INP
28/60/92 (VER/PC/PF)	BFX4 chain B – 64 cells – study SEMT	1 DET_BUF_INP
29/61/93 (VER/PC/PF)	LDHQX8 chain – 64 cells – study gate type	1 DET_LAT_INP
30/62/94 (VER/PC/PF)	IVX4 LVDD chain – 64 cells – study low voltage	0
31/63/95 (VER/PC/PF)	BFX4 LVDD chain – 64 cells – study low voltage	1 DET_BUF_INP
32/64/96 (VER/PC/PF)	BFX4 chain C – 64 cells – study SEMT	1 DET_BUF_INP

The incoming transient drives the clock inputs of two flip-flops. Both flip-flops are cleared to zero by the reset. The rising edge of the transient causes the start flip-flop to clock in a 1 which can generate a rising edge. The positive edge propagates through the delay chain 1 (the bottom chain in Figure 3.14) which is made by a series of delay buffers (or equivalent) with a delay of t1. Later, the negative edge of the pulse will trigger the clock pin of the stop latch whose D pin is connected to signal 1 (VDD). As a result, the falling edge of the transient can generate a rising edge at the stop latch and this edge can propagate through delay chain 2 whose delay elements have a delay of t2. The delay elements are selected such that t2 < t1, and thus, the edge in delay chain 2 moves faster than the edge in chain1, and if the transient is not large enough, the edge in t2 chain will finally catch up the edge in chain 1. Then, the pulse width can be calculated by $N_{stage}*(t2-t1)$. Table 3.5 shows the Vernier detector port list.

Table 3.5 Vernier Detector Port List

Port Name	Direction	Description
PULSE_IN	INPUT	Transient pulse to be measured
RESET_A	INPUT	DMR version of global reset
RESET_B	INPUT	
CLEAR_EXP_A	INPUT	DMR version of local clear signal
CLEAR_EXP_B	INPUT	
EVENT_DETECTED	OUTPUT	Indicates SET detected. Active high
VERN_CLK_OBS_SEL	INPUT	Signal to choose the calibration output. 0 = T_1 Chain 1 = T_2 Chain
DATA_OUT[7:0]	OUTPUT	Selected output data
DATA_SEL[2:0]	INPUT	Selects 8 bits of output data from the total 34 bits 000 = CAPTURE_LATCH[7:0] 001 = CAPTURE_LATCH[15:8] 010 = CAPTURE_LATCH[23:16] 011 = CAPTURE_LATCH[31:24] 1xx={6'b00000, START,STOP}
CALIB	INPUT	Enable both ring oscillators
CLK_OBS	OUTPUT	Divided by 32 output of RO on chain T_1/T_2
NEG_POSB	INPUT	Selects the pulse polarity

Figure 3.15 shows the layout of the Verner detector.

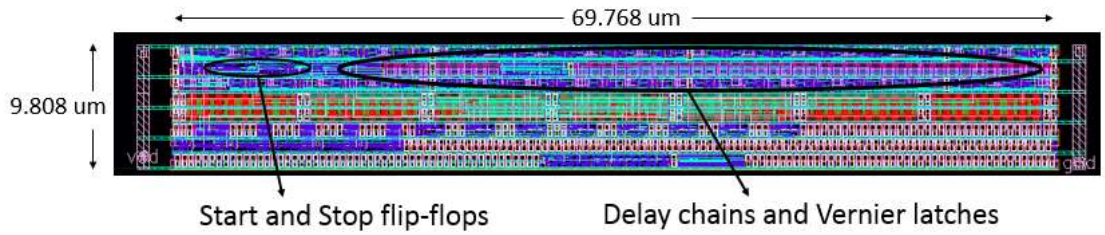


Figure 3.15 Layout of Vernier Detector

3.6.3 Classic Pulse Capture Detector

Another approach to measuring SETs consists of taking a "snapshot" of the SET as it propagates down a chain [82]. An example of such a circuit is shown in Figure 3.16. In this implementation, the pulse propagates through a chain of buffers. The output of each stage of buffers feeds the D-input of a latch that is normally transparent.

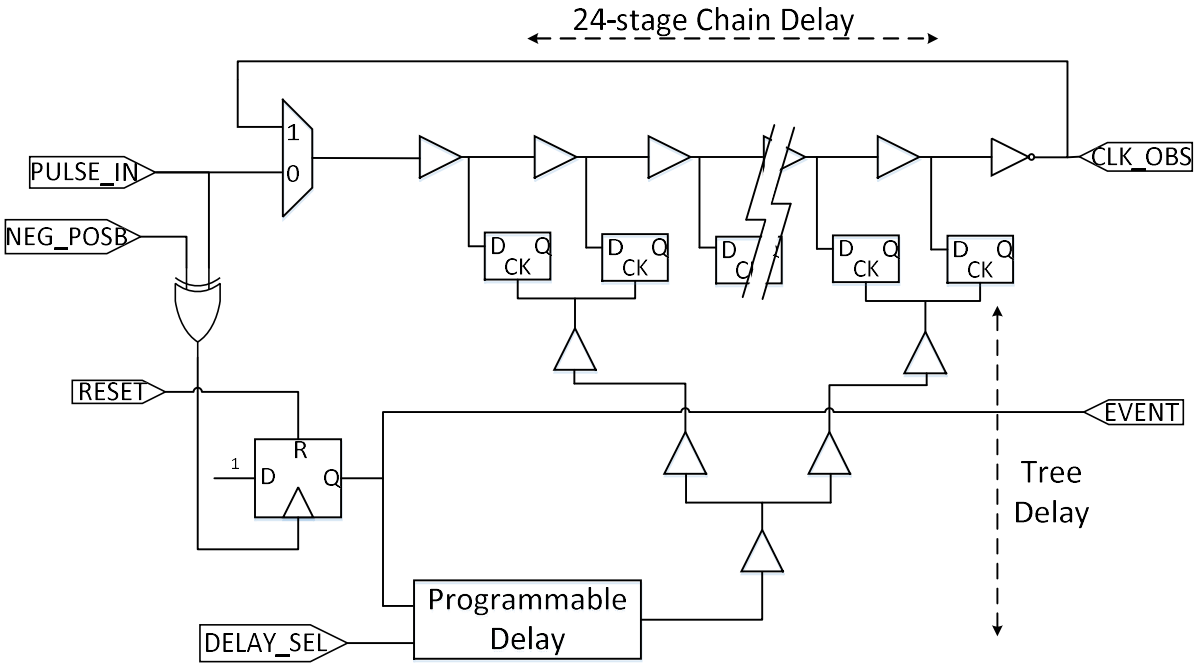


Figure 3.16 Pulse Capture Detector

The leading edge of the transient causes the Trigger Flip-Flop to load a 1. After a delay, this causes the capture latches to close and the transient to be saved in the capture latches. The delay between the leading edge of the transient and the closing of the capture latches should be adjusted so that

the leading edge of the transient has propagated to the head of the delay chain. This delay can be programmed using the configuration DELAY_SEL[1:0], as shown in Figure 3-16. Generally, the delays should be selected such that: $t_{trigger}+t_{tree} \approx (t_{chain} - 2$ gate delays). In this way, the transient will also be observed towards the tail of the chain.

In order to capture both positive (0->1) and negative (1->0) transients, the detector can be configured to invert the pulse that feeds the clock input of the Trigger Flip-Flop, using the NEG_POSB input. Note that the XOR gate that performs this inversion is subject to SETs. Such an SET may cause a false triggering of the SET detector; however, in this case, the capture latches would contain all zeroes (or all ones in the case of negative transients).

Figure 3.17 shows the layout the Pulse Capture detector.

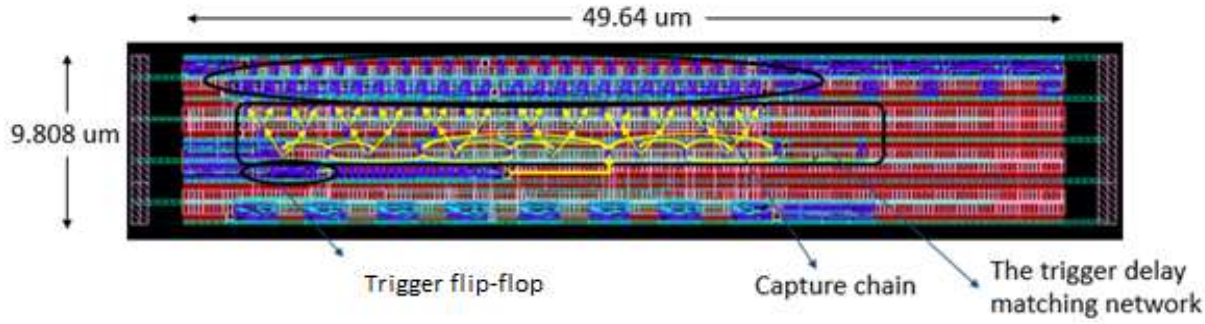


Figure 3.17 Layout of Pulse Capture Detector

Table 3.6 shows the port list of the Pulse Capture detector.

Table 3.6 Pulse Capture Detector Port List

Port Name	Direction	Description
PULSE_IN	INPUT	Transient pulse to be measured
RESET_A	INPUT	DMR version of global reset
RESET_B	INPUT	
CLEAR_EXP_A	INPUT	DMR version of local clear signal
CLEAR_EXP_B	INPUT	
EVENT_DETECTED	OUTPUT	Indicates SET detected. Active high
DATA_OUT[7:0]	OUTPUT	Selected output data
DATA_SEL[1:0]	INPUT	Selects which byte of data to output 00 = CAPTURE_LATCH[7:0] 01 = CAPTURE_LATCH[15:8] 10 = CAPTURE_LATCH[23:16] 11 = {7'b0000000, TRIGGER}
NEG_POSB	INPUT	Selects the pulse polarity
DELAY_SEL[1:0]	INPUT	Adjusts delay from trigger to capture
CALIB	INPUT	Enables both ring oscillators
CLK_OBS	OUTPUT	Divided by 32 output of RO on chain T_1/T_2

3.6.4 Pulse Filter Detector

Another method for measuring SETs is based on using a series of pulse filters with increasingly larger filter delays [83]. A transient of a given width will only pass through those filters whose delay is less than the width of the transient. As with other SET measurement techniques, it is necessary to design a circuit where SEUs in the flip-flops can be differentiated from SETs. The circuit shown in Figure 3.18 has a series of 15 pulse filters. The output of each of the pulse filters drives the clock input of a pair of flip-flops. If a transient arrives on the input and passes through the pulse filter, it should trigger both flip-flops. If an SEU occurs, only one flip-flop will be upset.

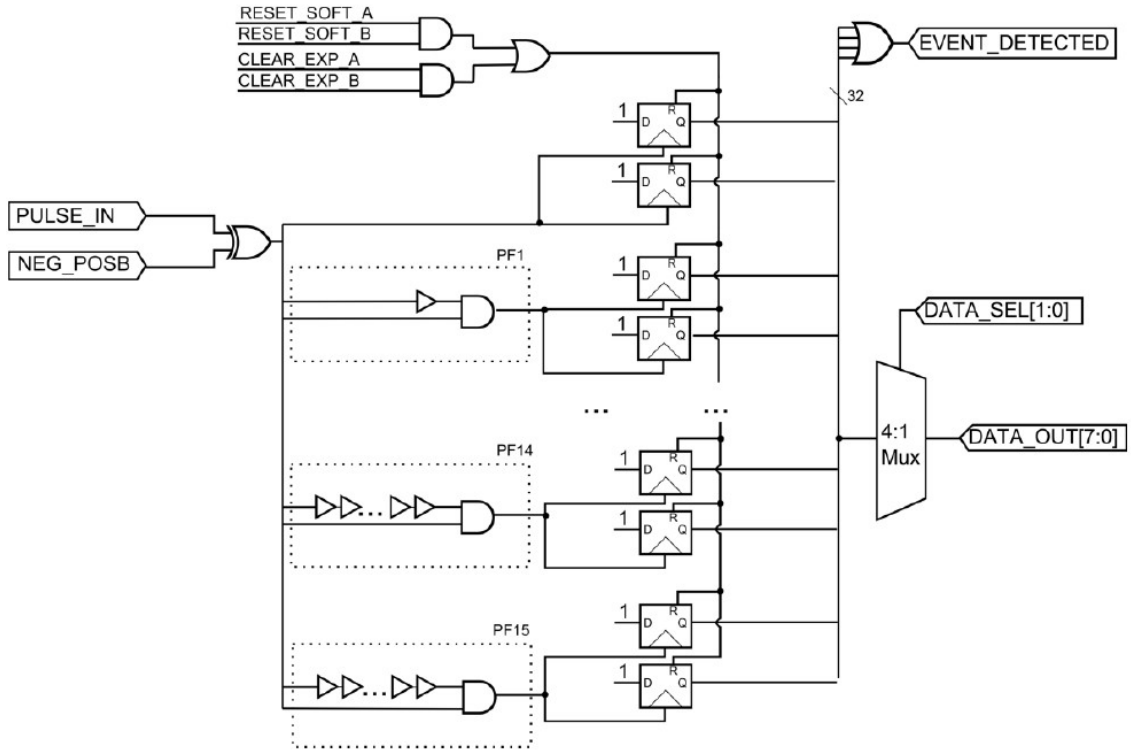


Figure 3.18 Pulse Filter Detector

In total, this circuit has 32 flip-flops, and if any one of them is set to 1, then the "EVENT_DETECTED" output is set. Using the error reporting logic, the contents of the flip-flops can be read, one byte at a time, using the DATA_SEL[1:0] to select which byte.

Figure 3.19 shows the layout of the Pulse Filter detector.

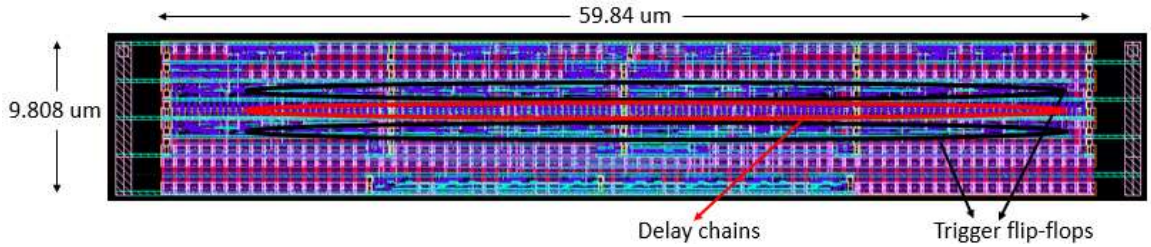


Figure 3.19 Layout of Pulse Filter Detector

Table 3.7 shows the port list of the pulse filter circuit.

Table 3.7 Pulse Filter Detector Port List

Port Name	Direction	Description
PULSE_IN	INPUT	Transient pulse to be measured
RESET_A	INPUT	DMR version of global reset
RESET_B	INPUT	
CLEAR_EXP_A	INPUT	DMR version of local clear signal
CLEAR_EXP_B	INPUT	
EVENT_DETECTED	OUTPUT	Indicates SET detected. Active high
DATA_OUT[7:0]	OUTPUT	Selected output data
DATA_SEL[1:0]	INPUT	Selects which byte of data to output 00 = CAPTURE_LATCH[7:0] 01 = CAPTURE_LATCH[15:8] 10 = CAPTURE_LATCH[23:16] 11 = {7'b0000000, TRIGGER}
NEG_POSB	INPUT	Selects the pulse polarity

3.6.5 CREST Circuit

The CREST circuit is based on having a chain of flip-flops with a small amount of combinatorial logic between each stage of flip-flops. The input to the chain can either be static 0, static 1, or a checkerboard (0101…). The clock for the chain comes from the on-chip clock generator (see Section 3.2) and it can operate at up to 2 GHz (nominal). When the chain is operated at low frequency, the observed cross section comes almost entirely from SEUs. When the chain is operated at increasingly higher frequencies, the contribution of SETs grows, due to the reduced latch window masking. The basic structure of the CREST chain is shown Figure 3.20.

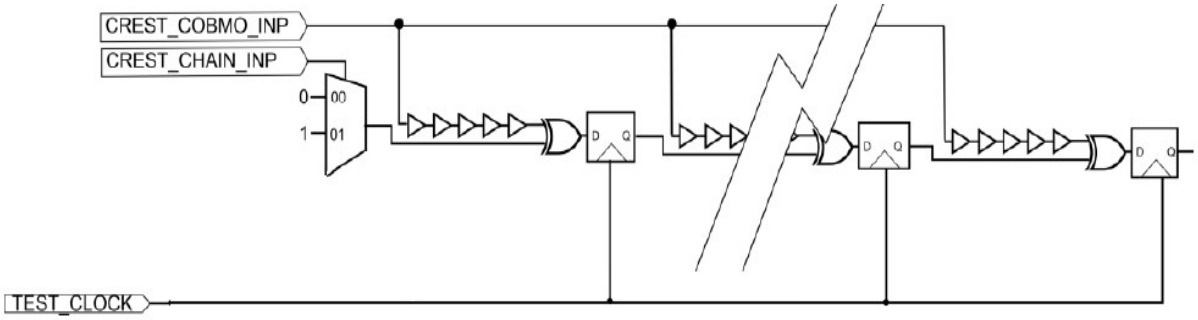


Figure 3.20 Basic Structure of CREST Circuit

At the output of the basic CREST chain, there is a comparator that checks for errors and this feeds into an 8-bit counter. This is a synchronous counter where each flip-flop is protected with TMR. Because the counter must operate at up to 2 GHz (nominal), the implementation is pipelined. A high-level view of the output of the CREST detector is shown in Figure 3.21.

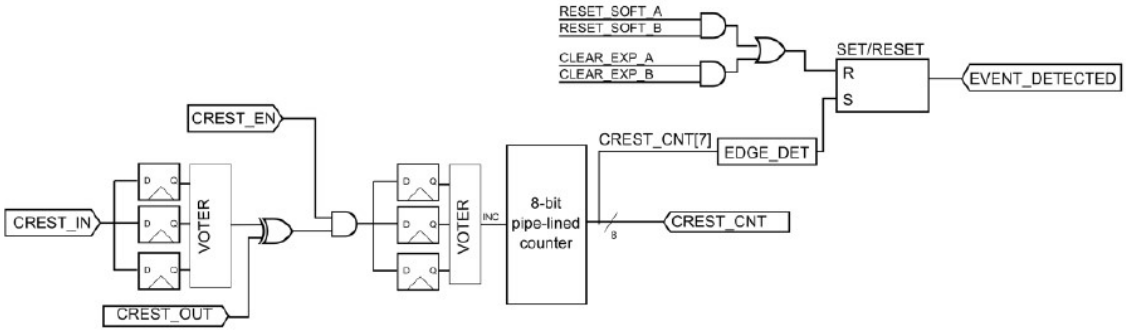


Figure 3.21 High-level View of CREST Experiment

Because the CREST circuit is clocked at a much higher rate than the control interface to the FPGA, it is not possible to inform the FPGA of each event. For this reason, the notification to the FPGA (EVENT_DETECTED) is only triggered on the rising edge of the MSBit (7) of the 8-bit counter. When the FPGA receives a notification from the CREST circuit, it reads the value of the 8-bit counter (which will typically be at 128 or slightly above). In this way, the FPGA can keep a tally of the total error count. At the end of the experiment (or periodically), the FPGA must read the CREST counter to get the remaining counts that have not yet been reported. Note that it is possible for the FPGA to read the CREST count at any time, as shown in Figure 3.21.

An on-chip 8-bit counter is needed to track the number of the events occurring in the high-speed CREST chain. The counter is designed using the TMR mode, to eliminate the influence of an SEU. For reference, the approximate gate delays for those gates required to build the 8-bit counter are shown in Table 3.8. Note that these are the worst-case delays (0.7V, 125°C) for the slowest path through the gate. Also note that the nominal clock period at 2 GHz is 500 ps. However, 45 ps is budgeted for duty-cycle errors due to transients on the clock network, 45 ps is budgeted for clock uncertainty in the clock tree and an additional 79 ps is budgeted for setup time. This leaves approximately 331 ps available for the combinatorial logic.

Table 3.8 Gate Delays for 8-Bit Counter

FA (full adder)	100 ps
HA (half adder)	92 ps
AO222 (used for voter)	146 ps

For these reasons, the 8-bit counter is built by cascading 2-bit counters. The basic 2-bit counter is shown in Figure 3.22. Note that the critical path is shown in red and its delay is 330ps, just fitting in the available budget. Care will be required to ensure this circuit meets timing.

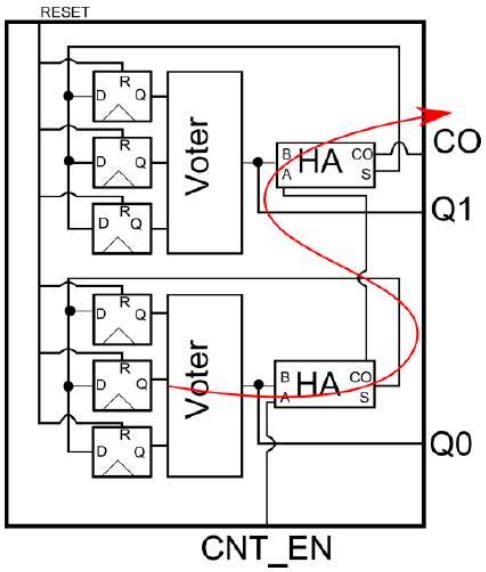


Figure 3.22 2-Bit Counter

Finally, four of the 2-bit counters are assembled to build an 8-bit counter as shown in Figure 3.23. Note that because the counter is pipelined, not all output bits will transition at the same time, potentially making it difficult to read the contents. In reality, this is not a problem. During the radiation period, the FPGA will react to the EVENT_DETECTED signal which occurs each time the MSBit (7) of the counter transitions. At the end of the experiment, the count will be static and it can be read out.

In the event the count must be stopped to read it out, then there is a configuration bit, CREST_EN, which disables the counter (see Figure 3.21).

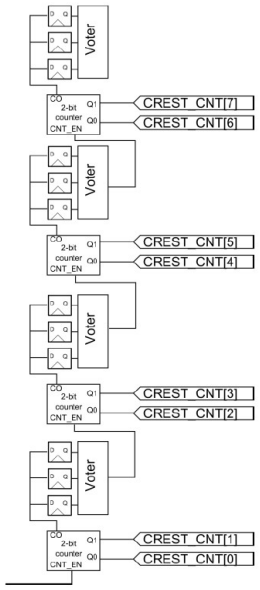


Figure 3.23 8-Bit Pipelined Counter

3.7 Gate Chains for SET Measurement

3.7.1 Normal SET Capture Gate Chains

The chains of gates for SET measurement consist of linear chains of a given gate type, the output of which is connected to an SET detector. The input to the chain may be connected to a configuration bit in order to study the impact of the input state. We note that for some gates, such

as an OR2, there is only one state in which the gate can be configured to propagate transients (2'b00). In the case of some gates, such as XOR gates, multiple configurations are possible. In Figure 3.24, the actual XOR chain topology is shown, and in Figure 3.25 the topology of the MUX chains is shown.

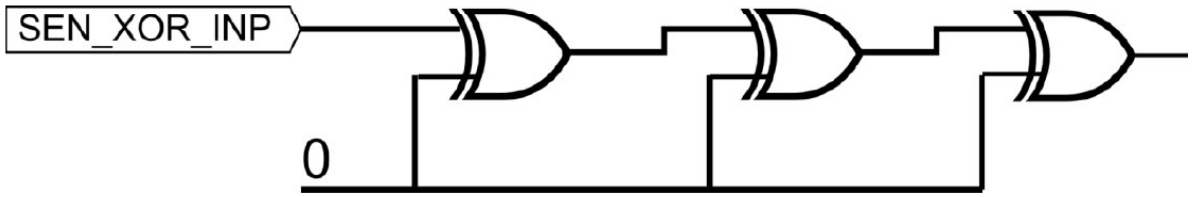


Figure 3.24 Topology of XOR Gate Chain

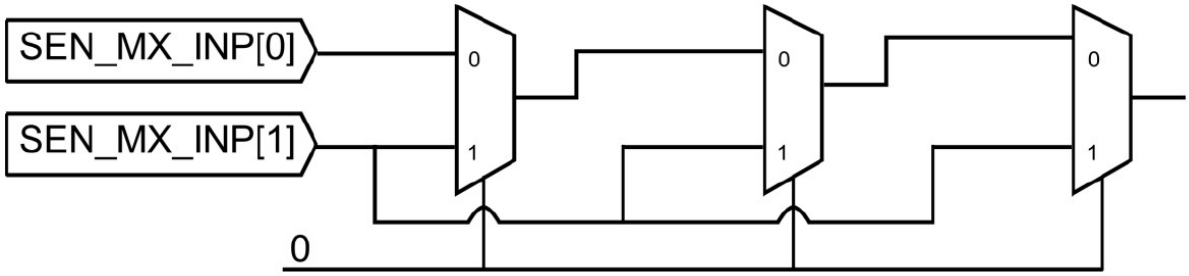


Figure 3.25 Topology of MUX Chain

3.7.2 Static SEMT Measurement

In the test chip, there are also chains designed for the Single Event Multiple upsets (SEMT) measurement. The purpose of the SEMT experiments is to observe whether single events can produce transients in physically adjacent cells. The study will investigate the probability of such SEMT events and their rate of occurrence as a function of the size of the cells. The intent is also to investigate whether the effect is limited to two adjacent cells or whether it can span three or four cells. One part of the SEMT investigation is performed using the three pulse-measurement circuits (Vernier, Pulse Capture, Pulse Filter). Logically, three chains are connected to three independent SET detectors, as shown in Figure 3.26(a). The cells in the three chains are physically placed in an interleaved fashion, as shown in Figure 3.26(b). In the event that an SEMT occurs, two or three transients will be recorded. Using the detectors, not only will the events be recorded, but all of the

pulse widths will be measured. The events will be correlated by the fact that they occur nearly simultaneously.

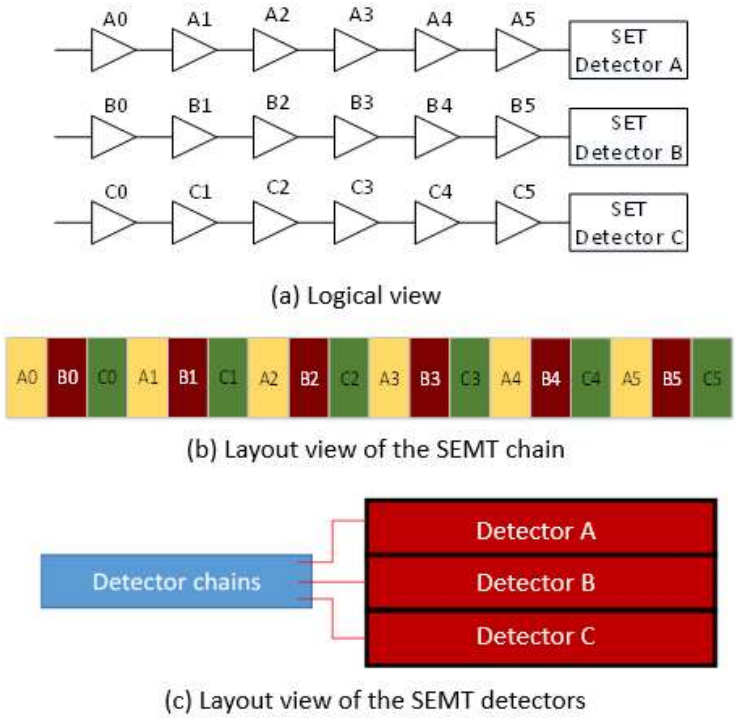


Figure 3.26 SEMT Capture Chains

The physical layout of the SEMT gate chains is shown in Figure 3.27. Between each group of three gates (ABC), an empty space is left so that the groups of gates can be tested under a pulsed laser. The spot size of the laser is expected to be approximately 1.5 µm in diameter.

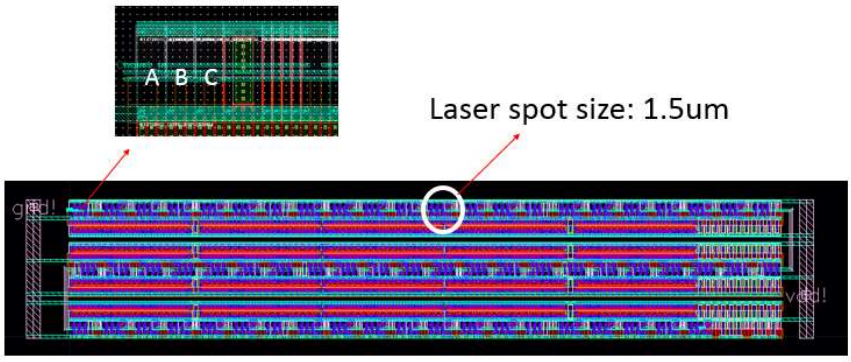


Figure 3.27 Layout of SEMT Capture Chains

3.7.3 Low-voltage SET Capture Chain

Selected sensor chains can be operated at a lower voltage in order to study the effect of voltage on SETs. This allows the detector circuits (Vernier, Pulse Capture) to operate at their nominal voltage (1.0v), and thus have, good detection capability. These special chains requires a level shifter at the output before the detector. The level shifter for going from the lower to the higher voltage (at the output) is custom designed, based on an existing design. This is illustrated in Figure 3.28.

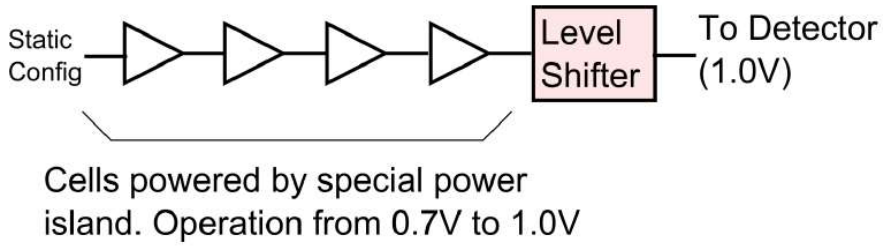


Figure 3.28 Sensor Chain with Level Shifter

3.8 Final Chip Layout

Figure 3.29 shows the final layout and the block division of the ST1 chip.

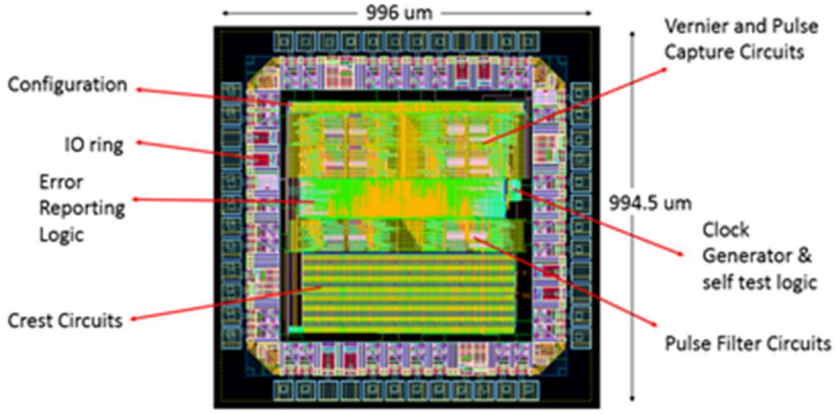


Figure 3.29 Final Chip Layout and Block Level Division

Figure 3.30 shows the chip fabricated by ST Microeclectronics.

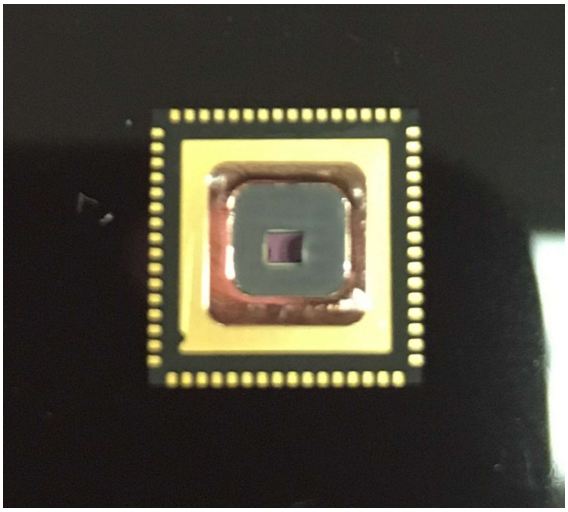


Figure 3.30 Chip picture

3.9 Test Board Design

The DUT test board was designed to support both ST1 and AR0 test chips. For getting as much data as possible in the limited time of a heavy-ion test, each test board can have 4 DUT chips mounted on it. In these 4 DUT positions, 2 of them are opened on the bottom, which enables the Two Photon Absorption (TPA) laser test from the back. Additionally, the board can instantiate 2 SAMTEC connectors (each with 80 signals), 20 jumpers to select which 28nm chip is instantiated on the QFN64 footprints and 8 power banana connectors. The whole board is 17cm x 15cm in width and height respectively and is fixed to the stage using 4 M4 screws. Table 3.9 shows the signal list for the 2 test chips.

Table 3.9 Signal List of the ST1 Chips

Pin	SET chip name	Processor chip name	Board Signal name	Usage	SAMTEC pin
1	NC	NC	NC	NC	
2	NC	NC	NC	NC	
3	SEL_NUM_DAT	GO	{A-B}_SEL_N_D	Shared	1

4	CTRL_CLK_IN	DONE	DUT{1-4}_CT_CK	Dedicated	40, 66
5	GNDE	GNDE	GND	GND	
6	VDDE	VDDE	VDDE28	VDDE28	
7	AVDD	CONF_DIN	DUT{1-4}_AVDD_CONF_I	Jumper : AVVD28 / Dedicated	71, 75
8	RESET_B	RESET_B	{A-B}_RESET_B	Shared	3
9	ERR_ACK	CONF_DOUT	DUT{1-4]_ERR_ACK	Dedicated	38, 64
10	ERR_DAT_SEL0	CONF_EN	{A-B}_ER_DAT_S	Shared	5
11	GND	GND	GND	GND	
12	VDD	VDD	VDD28	VDD28	
13	ERR_DAT_SEL1	Diode 1	{A-B}_DAT_S1	Shared with jumper	10
14	ERR_DAT_SEL2	Diode 2	{A-B}_DAT_S2	Shared with jumper	8
15	NC	NC	NC	NC	
16	NC	NC	NC	NC	
17	NC	NC	NC	NC	
18	NC	NC	NC	NC	
19	ERR_CLR_A	Diode 3	DUT{1-4}_ER_CL_A	Dedicated with jumper	15, 35
20	ERR_CLR_B	GPO[0]	DUT{1-4}_ER_CL_B	Dedicated	28, 48
21	GNDE	GNDE	GND	GND	
22	VDDE	VDDE	VDDE28	VDDE28	
23	ERR_VLD_A	GPO[1]	DUT{1-4}_ER_VAL_A	Dedicated	30,50
24	ERR_VLD_B	GPO[2]	DUT{1-4}_ER_VAL_B	Dedicated	32,58
25	ERR_NUM_DAT0	GPO[3]	DUT{1-4}_NU_DAT0	Dedicated	34,60
26	ERR_NUM_DAT1	GPO[4]	DUT{1-4}_NU_DAT1	Dedicated	36, 62
27	GND	GND	GND	GND	
28	VDD	VDD	VDD28	VDD28	
29	ERR_NUM_DAT2	GPO[5]	DIT{1-4}_NU_DAT2	Dedicated	26, 46

30	ERR_NUM_DAT3	GPO[6]	DUT{1-4}_NU_DAT3	Dedicated	24, 44
31	NC	NC	NC	NC	
32	NC	NC	NC	NC	
33	NC	NC	NC	NC	
34	NC	NC	NC	NC	
35	ERR_NUM_DAT4	GPO[7]	DUT{1-4}_NU_DAT4	Dedicated	20, 42
36	ERR_NUM_DAT5	STATUS_DOUT	DUT{1-4}_NU_DAT5	Dedicated	18, 55
37	GNDE	GNDE	GND	GND	
38	VDDE	VDDE	VDDE28	VDDE28	
39	ERR_NUM_DAT6	STATUS_EN	DUT{1-4}_NU_DAT6	Dedicated	16, 53
40	ERR_NUM_DAT7	STATUS_XFER_A	DUT{1-4}_NU_DAT7	Dedicated	31, 51
41	CLK_OBS_OUT	CONF_CLLK	DUT{1-4}_CK_O	Dedicated	29, 49
42	TEST_CLK_IN	RESET_A	{A-B}_TE_CK	Shared	7
43	GND	GND	GND	GND	
44	VDD	VDD	VDD28	VDD28	
45	RESET_A	TEST_CLK_IN	{A-B}_RST_A	Shared	9
46	AVDD	CLK_OBS_OUT	DUT{1-4}_AVDD_CK_O	Jumper : AVVD28 / Dedicated	73, 79
47	NC	NC	NC	NC	
48	NC	NC	NC	NC	
49	NC	NC	NC	NC	
50	NC	NC	NC	NC	
51	CONF_LIVE_OK	CONF_LIVE_OK	DUT{1-4}_CONF_LIVE	Dedicated	27, 47
52	CONF_IN_OK	CONF_IN_OK	DUT{1-4}_CONF_IN	Dedicated	25, 45
53	GNDE	GNDE	GND	GND	
54	VDDE	VDDE	VDDE28	VDDE28	
55	CONF_DOUT	CHAIN_DOUT2	DUT{1-4}_CONF_O	Dedicated	23, 43
56	CONF_XFER_B	CHAIN_DOUT1	DUT{1-4}_CONF_X_B	Dedicated	21, 41
57	CONF_XFER_A	CHAIN_DIN	{A-B}_CONF_X_A	Shared	2
58	CONF_EN	STATUS_XFER_B	{A-B}_CONF_E	Shared	4

59	GND	GND	GND	GND	
60	VDD	VDD	VDD28	VDD28	
61	CONF_DIN	CONF_XFER_B	DUT{1-4}_CONF_I	Dedicated	17, 37
62	CONF_CLK	CONF_XFER_A	{A-B}_CONF_CK	Shared	6
63	NC	NC	NC	NC	
64	NC	NC	NC	NC	

Note: NC means Not Connected

Chapter 4: ST1 CHIP SIMULATION AND IRRADIATION TEST RESULTS

When designing the ST1 chip, a large number of SPICE simulations were performed to select the best trigger latches/flip-flops and delay cells. After freezing the design of the detectors, we also did the detector response simulation with different pulse inputs in several PVT (Process, Voltage and Temperature) conditions. In the simulation, we observed the pulse width distortion along the delay chains. If the distortion effect is large, it will influence the test result and the SET event rate significantly, which is observed in the radiation tests.

4.1 Detector Response with Different Pulse Inputs

The sensitivity of the detector circuits was studied using SPICE simulation based on post-layout extracted parasitic. Since this technology has been well characterized, it is expected that the transistor models are accurate and that these simulations provide a very good indication of the actual detection capabilities of the circuits that have been designed.

In Figure 4.1, the response for each of the detectors is shown. On the x-axis is the width of the injected pulse and on the y-axis is the measured pulse width. As expected, the Vernier detector, (in dark blue) has a smaller step size, than the Pulse Capture (in green) and the Pulse Filter (in red), due to its better pulse-width measurement precision.

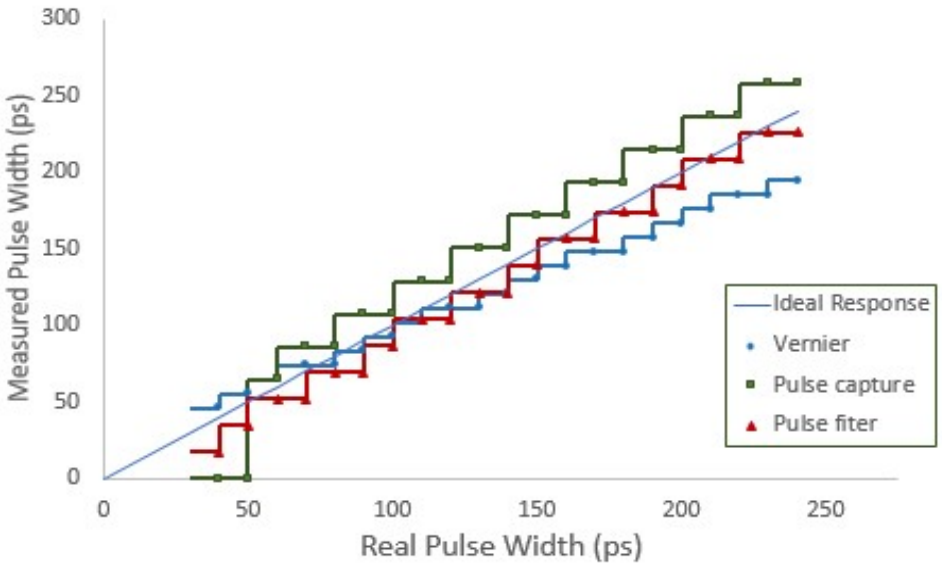


Figure 4.1 Simulated Sensitivity of SET Detectors

Although the Vernier circuit is calibrated, for larger pulse widths the measured value deviates from the ideal response. The deviation grows to 45 ps for wide pulses (240 ps). The reason for this deviation is the significant asymmetry between the rising and falling edges. An RO is used for the delay calibration, and the delay of each cell is calculated based on the RO frequency. It is assumed that the RO waveform has a 50% duty cycle. However, in fact, the rising and falling edges are not balanced, thus creating an error in the estimated per-stage delay (t2-t1). This problem could have been reduced through the design of a custom cell with rise and fall times that were better balanced. Despite this shortcoming, for short pulse widths (<100 ps), which are what are expected to be measured, the Vernier detector is very precise.

The Pulse Capture detector has a good response when the pulse width is wider than 50ps. However, when the input pulse width is smaller than this value, it is limited by the setup time and hold time of the capture latches. The resolution of the Pulse Filter detector is similar to the Pulse Capture detector, as in both cases this resolution is limited by a single gate delay. The limiting factor, in terms of detected minimum pulse width, for the Pulse Filter detector is the "minimum clock pulse width," which is slightly shorter than the minimum setup and hold window; thus it can detect SETs down to 40 ps.

4.2 Detector Response at Different PVT Conditions

In Table 4.1, we show the per-stage delay (in ps) in three PVT conditions (0.9V SS, 1.0V TT, 1.1V FF). We observe that the delays can vary by over a factor of two, highlighting the importance of on-die calibration when performing pulse-width measurement.

Table 4.1 Stage Delay at Different PVT Conditions

	FF @ 1.1V	TT @ 1V	SS @ 0.9V
Pulse Capture	2.2	2.7	3.6
Vernier T2	3.2	3.9	5.2
Vernier T1	3.9	5.1	7.1
Vernier T2-T1	0.8	1.2	1.9

Figure 4.2 shows the variation of the three detectors in three different PVTs conditions. These graphs show how each detector responds to a range of input pulses when it is simulated at each PVT condition. Due to the calibration circuit, the variation of Vernier and Pulse Filter detectors are around 30 ps. In contrast, the variation of the Pulse Filter detector is more than 100 ps. We also see that at the slow process corner, the performance of the Pulse Capture detector is significantly degraded for small pulse widths, largely due to the increased pulse narrowing that occurs as the pulse propagates along the delay chain. Table 4.2 shows the maximal overestimation and underestimation in percentage in the worst case.

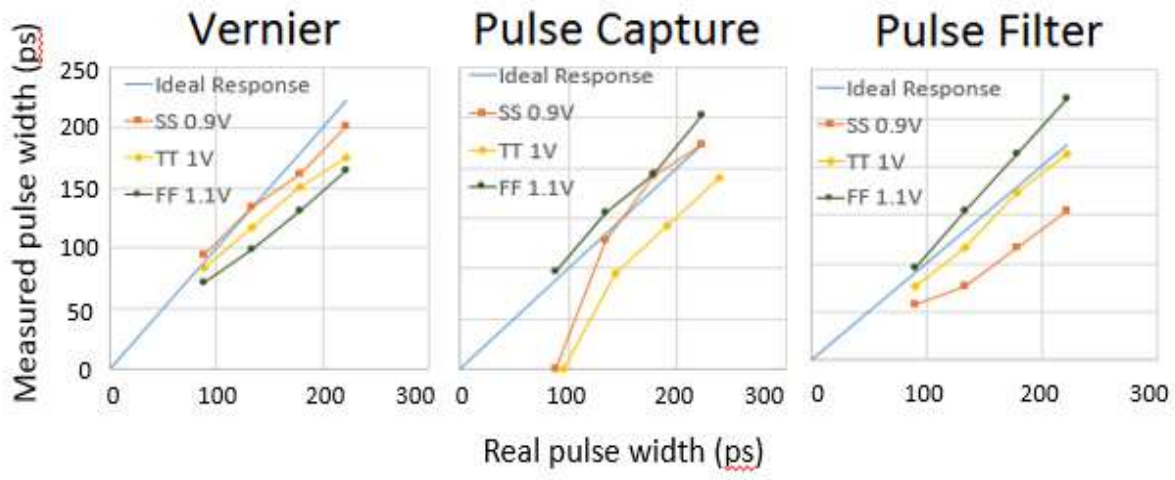


Figure 4.2 SET Detector Response at three PVT Conditions

Table 4.2 Stage Delay at Different PVT Conditions

	Overestimation	Underestimation
Vernier	N/A	26%
Pulse Capture	13%	9%
Pulse Filter	21%	43%

4.3 Simulated Pulse Narrowing and Broadening Effects

Our simulations showed that pulse narrowing/broadening is significant in this technology. In Figure 4.3, the propagation of a positive pulse through an X4 buffer gate is shown in a typical process, and it is seen how it progressively narrows. Conversely, in Figure 4.4, we see the widening of a negative pulse as it propagates through the same gate.

Based on our simulations, it was observed that a rising pulse is narrowed by 1.81ps (SS), 2.03ps (TT), 2.25ps (FF) per gate, and a negative edge pulse is broadened by 1.89ps (SS), 2.16ps (TT), 2.37ps (FF) per stage of gate.

It is important to understand that the broadening/narrowing effect significantly influences the measured pulse width for the Pulse Capture detector since the detector works by taking a snapshot of the transient as it propagates. This effect also comes into play in the capture chains. The detector observes the sum of all the transients produced in the chain after they have been narrowed or broadened as they propagate.

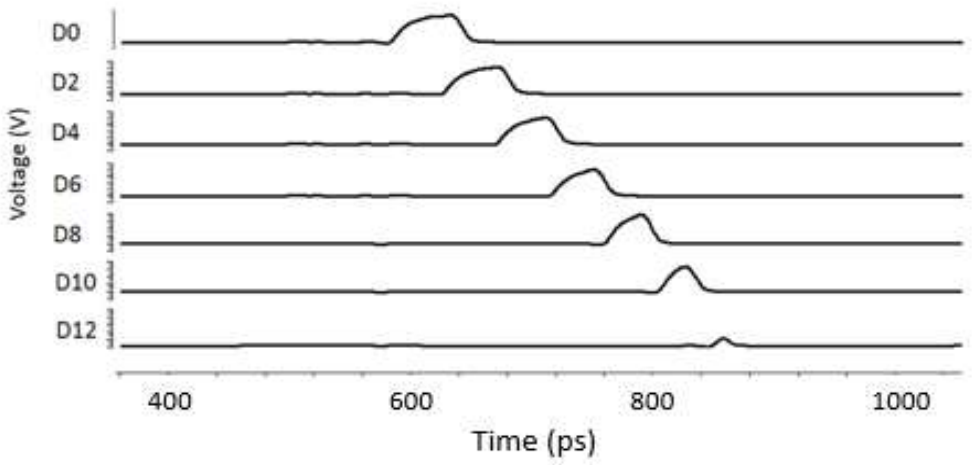


Figure 4.3 Narrowing of a Positive Transient

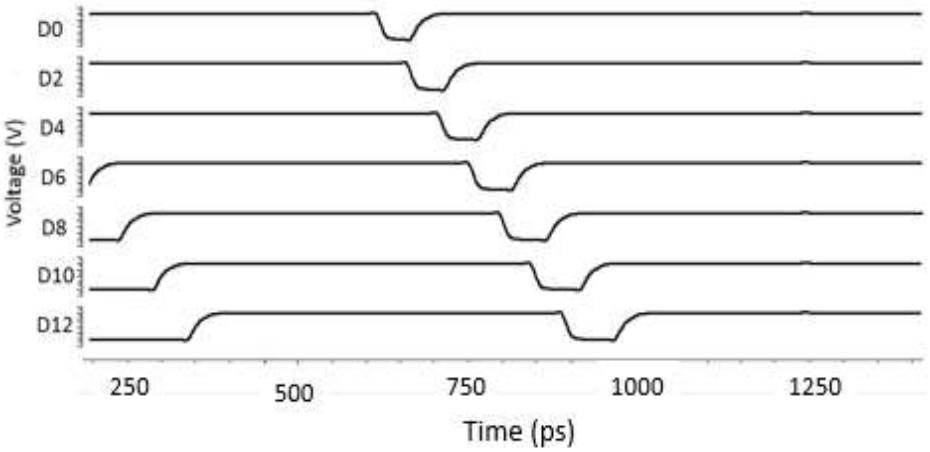


Figure 4.4 Broadening of a Negative Transient

4.4 Testing System introduction

The ST1 chip testing system was developed with the cooperation of the University of Saskatchewan and IRoC technologies. An initial testing system was designed to be implemented in the test vehicles for the heavy-ion test (IRoC). Then a wrapper was designed to make the system suitable to the FPGA system for the TID and pulsed laser test (U of S).

The testing system was implemented based on an FPGA. The FPGA was used to configure the circuit, readout the error data from the DUT and log the data to a control PC. Figure 4.5 shows a hierarchical view of the tester FPGA.

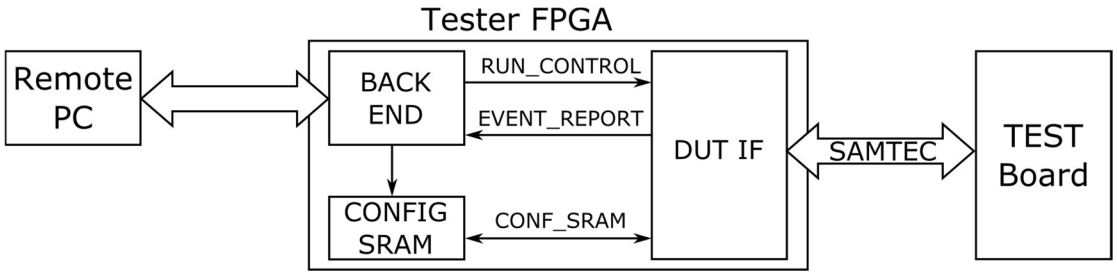


Figure 4.5 Hierarchical view of the testing system

The tester has three main modules:

1. The DUT interface is in charge of interfacing with the test board. This module is used to configure the DUT and read out the SET events from them;
2. The back-end is in charge of setting the run parameters and logging the error reported by the DUT interface to the remote PC; and
3. A configuration SRAM is used by the DUT interface to load DUT configuration chains. This memory will be written by the back-end module.

Table 4.3 shows the signal list of the testing system.

Table 4.3 FPGA Testing System Signal List

I/O	Width	Name	Description
General Signals			
IN	1	CLK	Main control clock (25MHz)
IN	1	RST	Reset the DUT interface, active high
Configuration SRAM Interface (Read-only)			
IN	16	CONFMEM_DATA	Data read from the configuration memory
IN	1	CONFMEM_RDV	Read data valid from the configuration memory
OUT	8	CONFMEM_ADD	Address to read from the configuration memory
OUT	1	CONFMEM_RE	Configuration memory read enable
Run Control Interface			
IN	1	START_TEST	Sample the run parameter, calibrate the chip (if needed) and start the test
IN	4	TC_EN	Enable for each DUT
IN	4	TEST_CONF_ADD	Address of the test configuration in the configuration memory
IN	4	CALIB_CONF_ADD	Address of the calibration configuration in the configuration memory
IN	1	CALIB_EN	Enable the calibration of the experiments
IN	7	CALIB_FIRST	First experiment to calibrate
IN	7	CALIB_LAST	Last experiment
IN	2	TEST_CLK_DIV	Define the frequency divider of the test clock based on the main clock
IN	1	TEST_CLK_EN	Enable the test clock
IN	1	STOP_TEST	Stop the test run
Event Reporting Interface			
OUT	1	EVENT_VALID	Flag to report that data is valid and should be logged
IN	1	EVENT_ACK	Acknowledge that the STB has logged the data
OUT	4	EVENT_TYPE	Type of event reported
OUT	2	EVENT_DUT	DUT index
OUT	7	EVENT_EXP	Experiment index
OUT	2	EVENT_SUBEXP	Sub-experiment index
OUT	64	EVENT_DATA	Event data

Figure 4.6 shows the testing system structure in details.

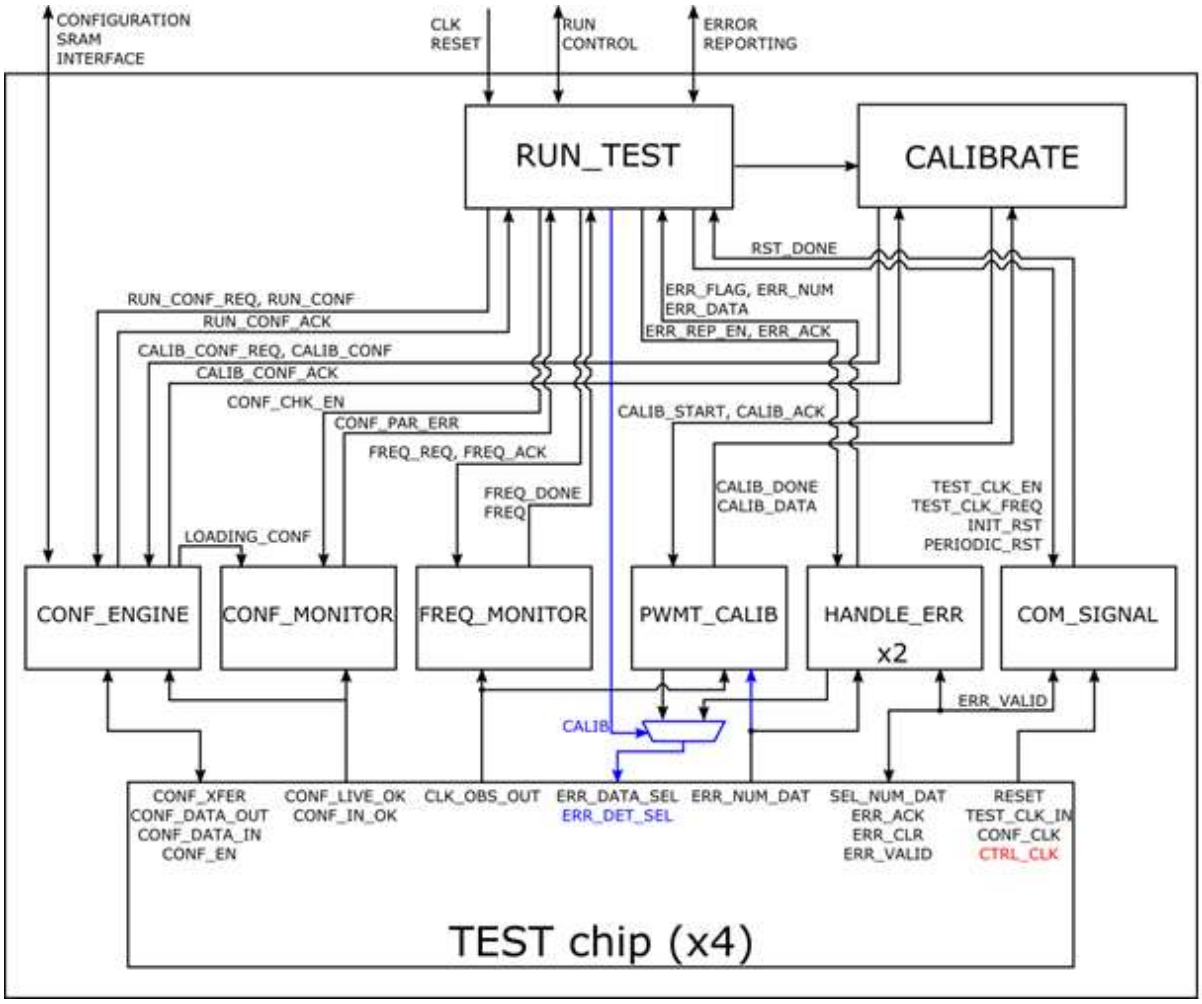


Figure 4.6 Testing System Structure

4.5 Heavy-Ion Test Result and Analysis

Heavy-ion testing was performed at the RADEF facility in Jyväskylä, Finland. A total of 19 parts on five cards were tested with Ne (3.63 MeV•cm2/mg), Ar (10.2 MeV•cm2/mg), Fe (18.5 MeV•cm2/mg), Kr (32.2 MeV•cm2/mg) and Xe (60 MeV•cm2/mg). The DUT chips were also irradiated by Xe ions with the DUT tilted at 45º angle, which resulted in an equivalent LET of 84 MeV•cm2/mg. Each card was irradiated to fluences of 1×109 ions/cm2, corresponding to exposed TID in the range of 500 to 1000 krad(Si). Despite such long runs and due to the low SEE sensitivity

of the technology, relatively few SETs were observed, making it difficult to draw extensive conclusions about the SET sensitivity of individual gates. No hard failures and no SEL were observed. The CREST circuit was operated with a checkerboard pattern at 500 MHz and 1 GHz. No anomalous events (bursts) were observed, which suggests that no SETs impacting the clock tree or TMR counter logic occurred. The cross-section can be calculated by formula 4.1.

$$\text{Cross} - \text{Section} = \frac{error\_count}{fluence \times cell\_count} \qquad 4.1$$

The overall measured cross section for the CREST circuit, SETs from the logic gates, and indirect SEUs from the flip-flops in the detector circuits are plotted in Figure 4.7. The cross section for the CREST circuit is a combination of the two operating frequencies (500 MHz and 1 GHz). There are two SET cross sections, one is for all of the logic gates combined and the second plot excludes the events on the OR2 gate. Error bars are calculated based on statistical uncertainty and a dosimetry accuracy of 10%. It is observed that the SET cross section is nearly two orders of magnitude lower than the SEU cross section. In addition, it is noted that the CREST sensitivity is very close to the static SEU sensitivity, which shows that SEUs are the dominant source of upsets in the CREST. We note that at low LET, the sensitivity of the CREST (built using X8 cells) is slightly higher than the static SEU sensitivity (measured in X17 cells), which is because the smaller transistors are more sensitive.

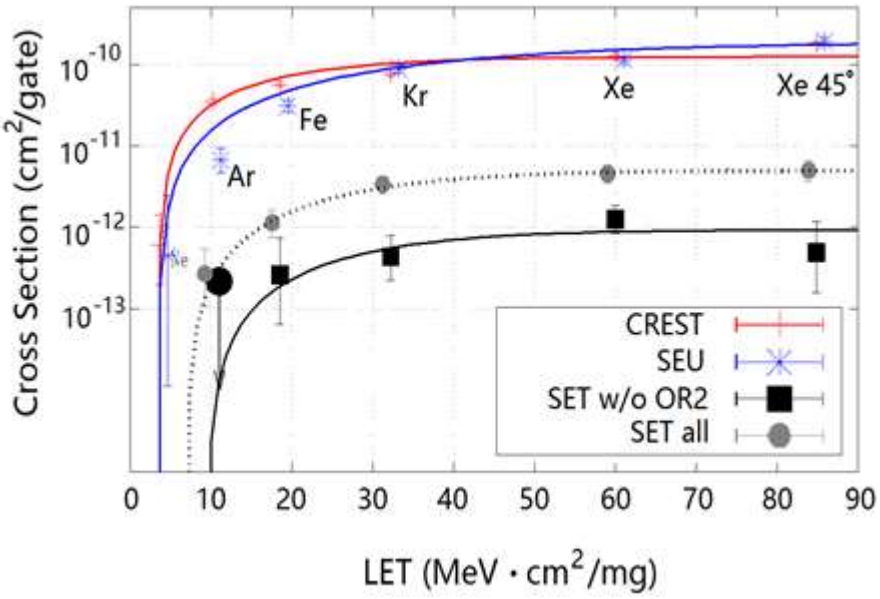


Figure 4.7 CREST, SEU, SET Cross Section versus LET, VDD=1V

In simulation, we observed that the OR2X8 gate induces significant broadening, and a 50 ps pulse at the start of the chain of 64 gates reaches a width of 940 ps at the end. This has a significant impact on the measured SET rate for this chain. The total SET cross section when events on the OR2 chain are excluded is an order of magnitude lower, as shown in Figure 4.7.

To find out the reason for the extreme pulse broadening effect of the OR2X8 gate, we took the post layout SPICE simulation on this gate. In the SPICE simulation, I gave a 50 ps pulse to port A and kept port B at 0, which was the same configuration as in the heavy-ion test. Figure 4.8 and Figure 4.9 show the schematic of the OR2X8 gate and the pulse injection simulation result. As can be found from Figure 4.9 and Table 4.4, the leading and tailing slew of the pulse at Port Z are quite close to each other, which means the N and P size of the invertor is quite balanced. However, the output of the NOR2 part is problematic. The tailing edge (0->1) slew is 36ps, which is the cause of the pulse distortion.

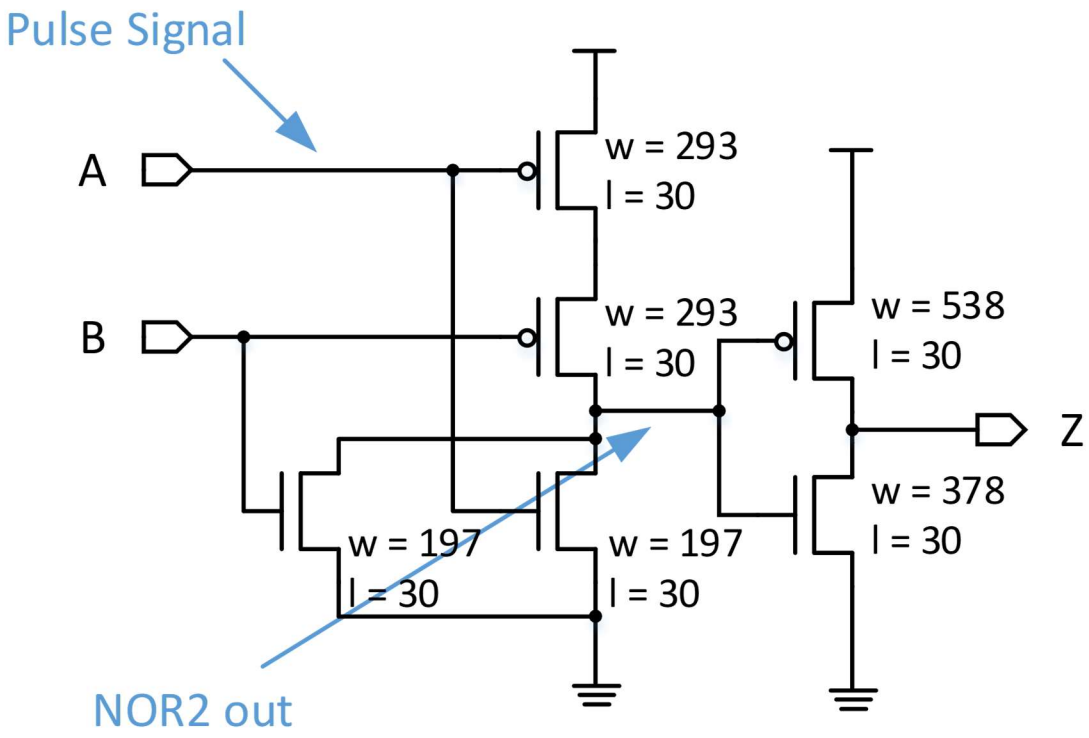


Figure 4.8 OR2X8 Schematic

Since the later stage invertor is quite balanced, the balanced PN ratio can be assumed as 538/378=1.42. So, giving the logic effort, the proper size of M5 and M6 should be 197*2.84=561n.

However, the size of M5 and M6 are just 293n which is just half of the balanced size. In other words, the driving ability of the pull-up network is not adequate to generate a sharp edge. That is the reason for the large slew of the rising edge.

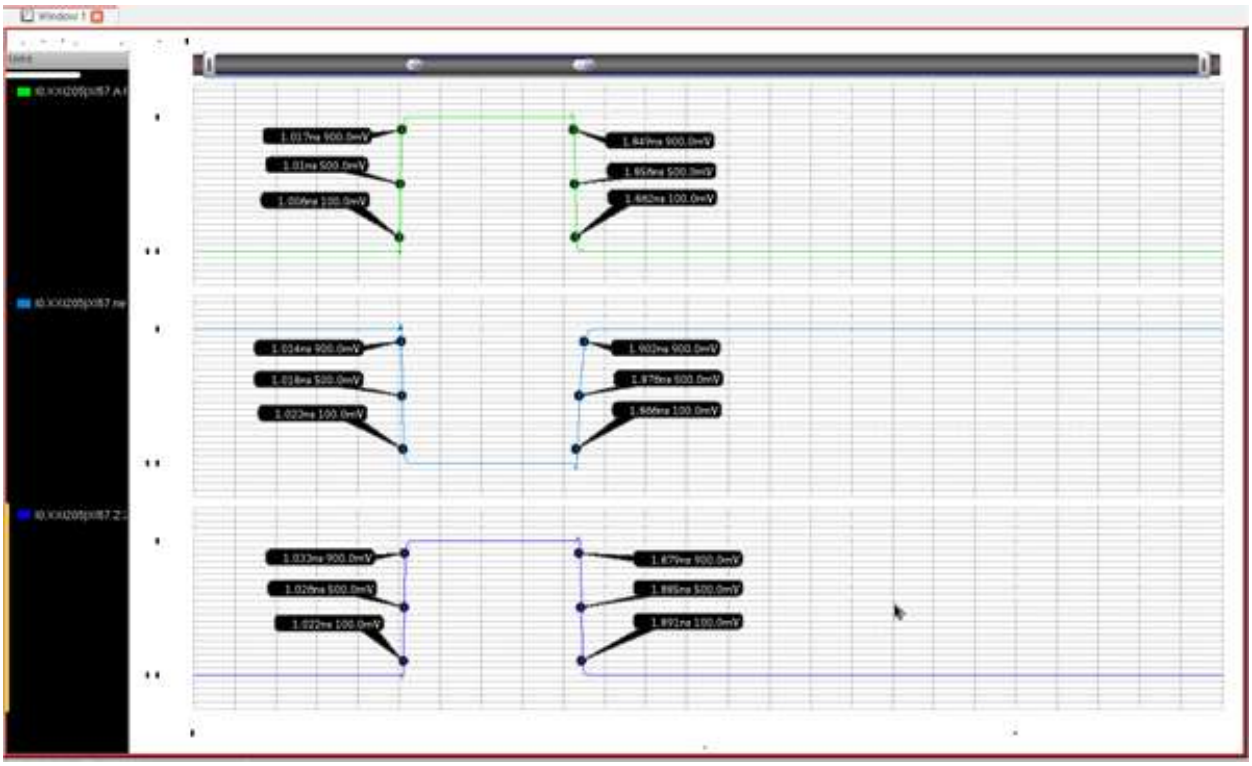


Figure 4.9 OR2X8 Post-Layout Simulation result

Table 4.4 Simulation Conclusion

	Pulse Width	Leading Slew	Tailing Slew
Port A	846	11	13
NOR2 out	858	9	36
Port Z	859	11	12

Based on the rise / fall delay calculation, the mechanism of pulse broadening is analyzed in detail to give a reasonable explanation for the heavy-ion and laser-radiation results. First, the basic principle of the pulse broadening is described using the 1-stage invertor as an example. For a "010"

pulse, after a 1-stage invertor, it becomes a "101" pulse, assuming the width of the input and output pulses is t_{in} and tout. Then the width of the pulse broadening ΔT_{010} can be given by equation 4.1, as shown in Figure 4.10.

$$\Delta T_{010} = t_{out} - t_{in} = t_{PLH} - t_{PHL} \qquad 4.2$$

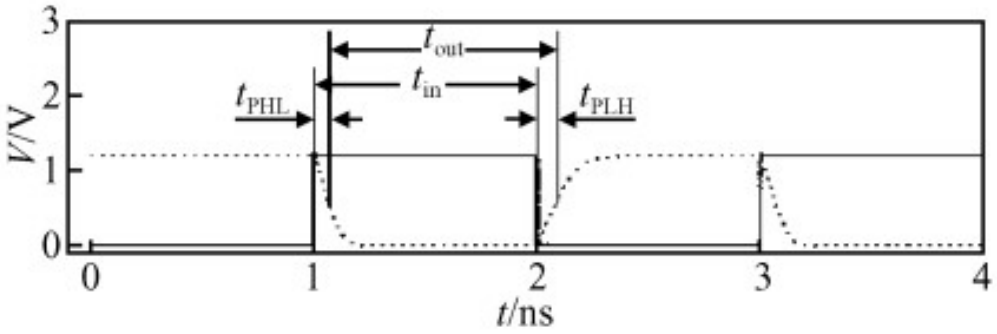


Figure 4.10 Example of pulse broadening

Similarly, $\Delta T_{101} = t_{PHL} - t_{PLH}$, where t_{PHL} and t_{PLH} are the rise and fall propagation delays of the invertors, respectively, and it can be seen that the prime reason for the pulse broadening is the invert0rs rise / fall delays, which are not equal.

In the first-order analysis, tPLH and tPHL can be given by formula 4.2, where k_p and k_n are the gain factors of the PMOS and NMOS transistors, respectively. With the condition that the PMOS and NMOS transistor lengths are equal, the relationship of k_p and k_n can be given by formula 4.3, where W_p and W_n are the gate width of the pMOS and nMOS transistors, and μp and μn are the hole and electron mobility, respectively.

$$t_{PLH} = \frac{C_L}{k_p V_{DD}} \quad t_{PHL} = \frac{C_L}{k_n V_{DD}} \qquad 4.3$$

$$\frac{k_p}{k_n} = \frac{W_p}{W_n} \times \frac{\mu_p}{\mu_n} \qquad 4.4$$

The following analysis shows the "010" pulse propagating through the case of two invertors. After the "010" pulse passes through the first-stage invertor, the pulse width is $\Delta T\ (1) = t_{PLH1} - t_{PHL1}$, and the pulse becomes a "101" pulse. After passing through the second-stage invertor, the pulse is further stretched to $\Delta T(2) = t_{PHL2} - t_{PLH2}$. Therefore, the total amount expansion of the "010" pulse after the two-stage invertor is:

$$\Delta T = \Delta T(1) + \Delta T(2) = (t_{PLH1} - t_{PHL1}) + (t_{PLH2} - t_{PHL2})$$

$$= \left(\frac{C_{L1}}{k_p V_{DD}} - \frac{C_{L1}}{k_p V_{DD}}\right) + \left(\frac{C_{L2}}{k_p V_{DD}} - \frac{C_{L2}}{k_p V_{DD}}\right) \qquad 4.5$$

where CL1 and CL2 are the output loads of the first- and second-stage invertors, respectively. Under the load balancing condition, CL1 = CL2 so that tPHL1 = tPHL2 and tPHL1 = tPHL2. Thus, ΔT (1) and ΔT (2) are the same size, in the opposite direction. The "010" pulse passes through the two-stage invertor, broadening zero. This is reasonable that under the balance load conditions, INVX8, BUFX8, NOR2X8 and NAND2X8 logic chains do not incur significant pulse broadening.

Under the condition that the load is not equal, $C_{L1} \neq C_{L2}$. If $k_p \neq k_n$, according to equation 4.4, when SET pulse passes through the two-stage invertors, the expansion amount of T is not zero. In the invertor chain, the pulse passing through each of the two invertors will experience a net pulse broadening or compression accumulating multiple times, which may create a significant broadening effect. This load imbalance theory may explain why the pulse expansion effect in the AND2X8, OR2X8 chain is more pronounced. As shown in Figure 4.11, compared with the NOR2X8 and NAND2X8 chain, there is an interval of invertor with the OR2X8 and AND2X8 chain. An unbalanced current drive strength and load capability cause a significant pulse broadening effect in the logic chain.

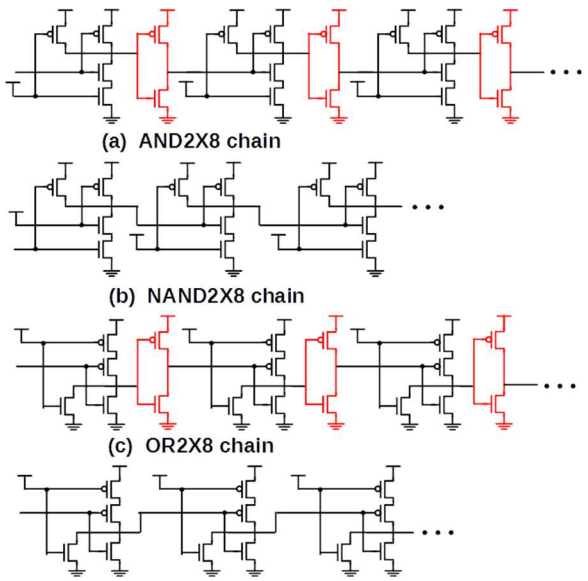


Figure 4.11 NOR2X8, OR2X8, NAND2X8 and AND2X8 Chain Schematic

We use logic effort G concept to describe the logic gate's ratio of current drive strength to load capability, which can easily evaluate the pulse broadening effect of different logic gates. As shown in Figure 4.12, the logic effort of the invertor, two-input NAND gate and two-input NOR gate are calculated. The logic effort of the two-input NAND gate is 4/3 and the NOR gate is 5/3. The larger logic effort means the greater the difference in the ratio of the pull-up / pull-down current drive strength to the load capability. By applying this concept to analyze the logic chains, we can easily evaluate the pulse broadening effect of different logic gates. The OR gate chain has the largest ratio of logic effort, so the OR2X8 logic chain pulse broadening is the most obvious.

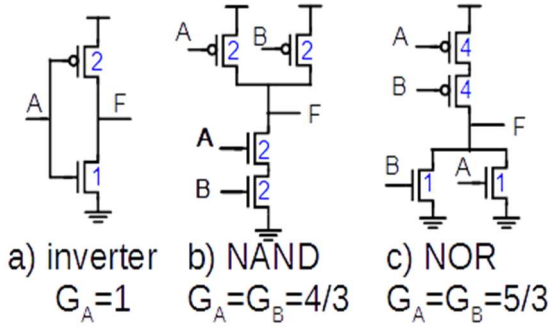


Figure 4.12 Logic Effort of the Invertor, Two-input NAND and NOR Gates

The distribution of the measured pulse widths for the OR2 gate is shown in Figure 4.13. The pulse width of the OR2 increases to over 1 ns, which is consistent with significant broadening along the chain. The peak is close to 0 ps and represents the short transients that triggered the detector but that were too narrow to be measured accurately. Another peak occurs around 1100 ps, which is the saturation point of the detector. This data suggests that the use of non-inverting gate chains or chains with significant broadening or narrowing is not an effective means for increasing the overall cross section for SET measurements.

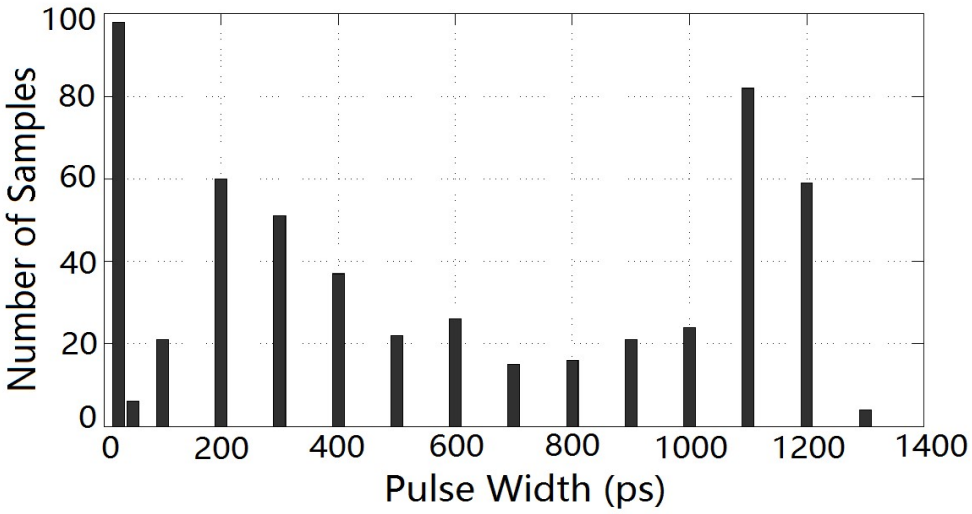


Figure 4.13 SET Pulse Width Distribution –OR2X8, VDD=1V

We also measured the cross section versus supply voltage for the buffer chains as shown in Figure 4.14. Note that at 0.55 V, the SET cross section is nearly an order of magnitude higher than at 1.0V.

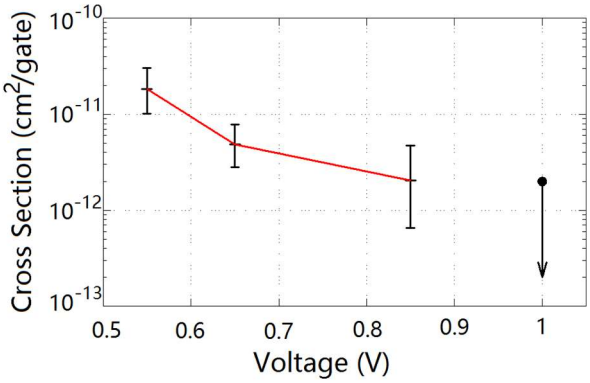


Figure 4.14 BUFX4 SET Cross-Section Showing Voltage Sensitivity

4.6 Pulsed-Laser Experimental Results at U of S

In order to further validate the pulse broadening effect, pulsed-laser experiments were carried out at the two-photon laser facility at the University of Saskatchewan (Figure 4.15) [69]. The wavelength of the pulsed laser is 1210 nm and the spatial resolution of the laser spot is approximately 1.5 µm.

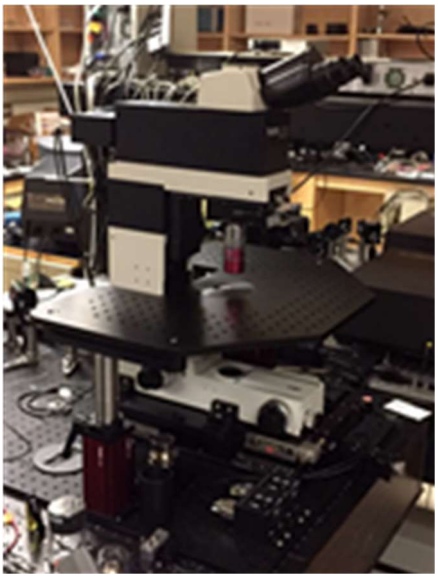


Figure 4.15 Two-photon Pulsed-Laser Facility at University of Saskatchewan

Table 4.5 Laser Test Result on OR2X8 Chain

Gate#	Energy (pJ)	Average Pulse Width (ps)	Number SET Events
36	100	423.9	86
	60	428.9	49
	40	419.3	11
31	100	352.5	90
	60	355.6	59
	40	357.7	17
26	100	289.3	63
	60	291.2	22
	40	279.9	9

The laser beam was focused on each individual gate in the chain, and in this way, the broadening/narrowing effects on a single logic gate should be accurately characterized [70]. In the experiments, three logic-gate positions (#36, #31 and #26) in the OR2X8 chains were selected, where the numbers indicate how many stages from the detector to the specific gate. At each selected gate, three laser energies, 100 pJ, 60 pJ and 40 pJ, were applied. Table 4.5 lists the laser

test result of the gate in these three positions. As seen in the table, the average pulse width was determined by the gate location along the chain. The pulse energy mainly influences the SET event rate rather than the pulse width. This observation is consistent with the observations in previous works [44]. The average measured pulse broadening per gate is 13.6 ps per stage, which closely matches the value of 13.9 ps obtained from simulations.

4.7 TID Experiment at U of S and Result Discussions

Since SOI has an additional parasitic structure, its TID response is more complex than bulk devices. Compared to its bulk counterpart, FDSOI has an additional Buried Oxide layer which introduces a two-dimensional coupling effect between the front and back interfaces. This coupling becomes the major contribution to the ionizing response of FDSOI devices. As a result, FDSOI technologies are expected to be more sensitive to TID than their bulk counterparts [71]. In previous work, the TID response is measured by the threshold voltage or drain current shift [72], [73]. In our work, each chip contained four types of ROs (see Table 4.6) whose frequency versus dose was monitored. In the following, we describe the results of the TID response for heavy-ion and Co-60 irradiation.

Table 4.6 Embedded Ring Oscillators

Name	Instances per Chip	Num. Stages	Gate Type	Nom Freq (MHz)
Main	1	44	IVX67	1000
Vern Fast	32	33	BFX4	483
Vern Slow	32	33	NOR2+NOR3	332
PC	32	24	BFX4	740

4.7.1 TID Test Result in Heavy-ion test

The impact of TID on the Main RO frequencies in the heavy-ion test is shown by the blue curves in Figure 4.16 and Figure 4.17. Error bars show the range between the highest and lowest observed frequencies, across four chips on the same board. The RO frequencies slow down at a rate between 0.8% and 1.3% per 100 krad(Si). The dispersion in frequencies grows significantly with total absorbed dose.

In addition to the impact of TID on the switching speed of the transistors, it was observed that the CREST SEU sensitivity increased at a rate of approximately 4×10-11 cm2 per Mrad, which is relatively smaller than that observed from previous bulk and SOI technologies [74].

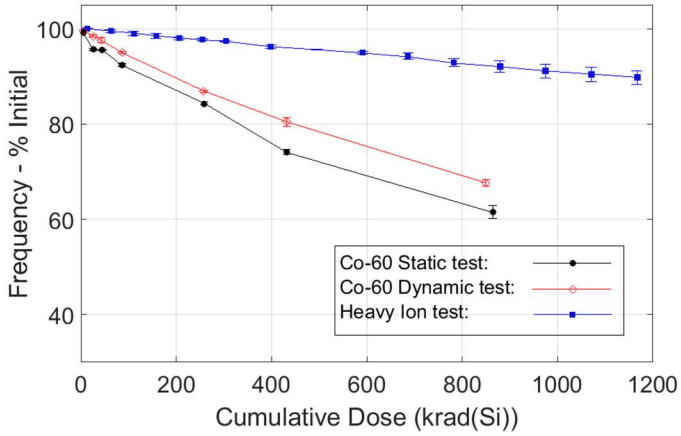


Figure 4.16 Impact of TID on Main RO Frequency

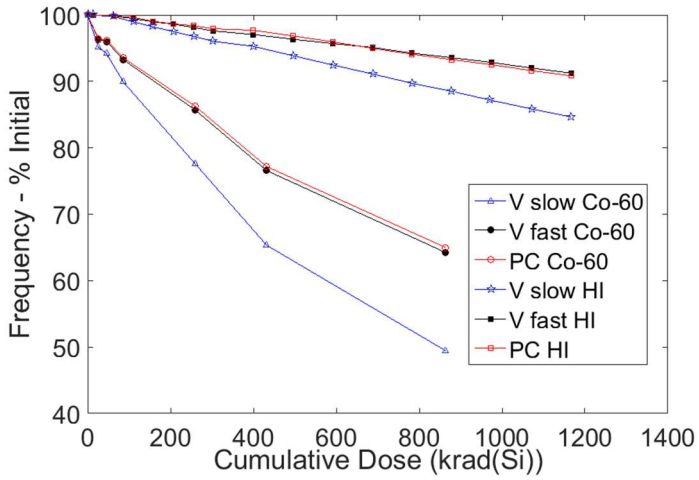


Figure 4.17 RO Frequency versus TID in Vernier(V) Slow, Vernier(V) Fast and Pulse Capture (PC) Detectors for HI and Co-60 Experiments

4.7.2 TID Test Result from Co-60 Irradiation

TID experiments were also performed by using a Gammacell 220 Co-60 facility (Figure 4.18) at the University of Saskatchewan. The Gammacell 220 can provide an irradiation rate of 240 rad/min.

The radiation chamber has dimensions of 15.2 cm (diameter) by 20.6 cm (high), which make it feasible to monitor all of the test chip signals during irradiation.

Figure 4.18 Gammacell 220 Co-60 Irradiator in University of Saskatchewan

Two test chips were mounted on one board for one irradiation experiment. Two sets of experiments were carried out. In the first experiment, the DUT chips were only powered with 1.0V supply voltage and all of the ROs were held in a static state (static mode). During the second experiment, the chips were in mission mode, which means that the Main RO was always active in the test (dynamic mode). For both sets of tests, the SET detectors were in the standby mode The TID impact on the Main RO in the Co-60 test is presented by red (dynamic) and black (static) curves in Figure 4.16. At the end of irradiation, in both cases, the Main RO frequencies had dropped to less than 70% of the initial frequency. The frequency decreased at a rate between 2.5% and 7.5% per 100 krad(Si). Table 4.7 shows the frequency decrease of the ROs in the chips during the test. Figure 4.17 shows the frequency of the other three types of ROs versus TID during the Co-60 test. After 1000 krad(Si) irradiation, the frequencies of the Vernier Slow RO, Vernier Fast RO and Pulse Capture RO respectively were reduced to 55%, 70% and 71% of their initial values, which is the same condition as in the heavy-ion test.

Table 4. 7 Frequencies VS. Total Absorbed Dose

Cumulative Dose krad(Si)	Vern Slow	Vern Fast	PC	Main
100	92%	95%	96%	95%
500	70%	82%	83%	81%
1000	55%	70%	71%	68%

4.7.3 Analysis of Static and Dynamic Result Discrepancy

In the two sets of Co-60 TID tests, the Main RO frequencies' degradation in the static test is around 5% more than in the dynamic test, which is mainly caused by two factors. The first reason is Radiation-Induced Charge Neutralization (RICN), which has been reported and verified in many previous works [75], [76], [77], [78]. The RICN effect happens when applying switched gate bias to devices in a radiation environment. Figure 4.19 shows the basic mechanism by which the charge neutralization happens. Taking an NMOS SOI transistor as an example, when a positive voltage, VDD, is applied at the gate, there will be an electric field, E_{ox}, in the buried silicon dioxide layer pointing from the silicon film to the substrate. The radiation-induced electron-hole pair is separated by an E_{ox}, and the positive charge is trapped at the oxide/substrate interface (Figure 4.19(a)). If the gate bias changes to VSS, the E_{ox} direction will reverse because of the trapped holes. Then, the radiation-induced negative charge will sweep down to the oxide/substrate interface and be neutralized with the trapped holes (Figure 4.19(b)). As a result, there are fewer trapped holes in the buried oxide layer when applying switched-bias in the TID test. Finally, the frequency shift in the dynamic test is less than that in the static test. A second factor that may contribute to the dispersion is the core logic power supply of the static test, which is 0.9% lower than in the dynamic test.

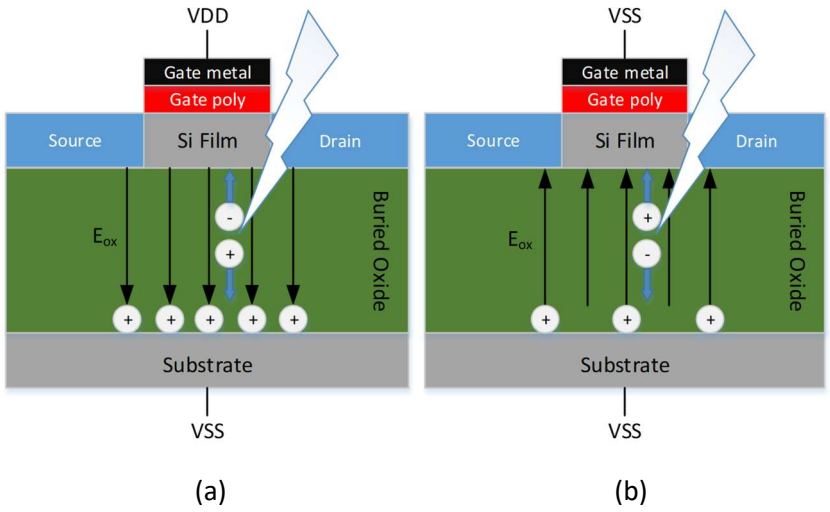


Figure 4. 19 Mechanism of RICN

4.7.4 Analysis of Heavy-ion and Co-60 TID Test Result Differences

Figure 4.16 and 4.17 show that the frequency degradation in the Co-60 test is much greater than that in the heavy-ion test. To explain the dispersion, we need to look into the mechanism of TID degradation in SOI technology. For advanced technologies, due to the use of a High-K dielectric gate, the radiation-induced voltage shift in the gate insulator may be negligible. However, radiation-induced charge buildup in shallow trench isolation oxide (STI) and in SOI buried oxides can lead to device degradation and failures.

When high-energy ionizing radiation is applied to a device, electron-hole pairs are generated in the oxide layers. Most of the electrons and holes quickly recombine before the electrons leave, which is called initial recombination. A fraction of the holes that escape recombination will be trapped at the Si/SiO2 interface forming a positive oxide-trap charge (charge yield). In this process, the initial recombination plays a key role in the charge yield. It is mainly determined by two factors: the electric field in the oxide, which is acting to separate the electron-hole pairs, and the initial line density of the charge pairs created by the incident radiation particles. The LET of the ionizing dose determines the initial line density. High LET particles, such as heavy ions, can generate high-density charge pairs along their tracks. So the possibility of initial recombination is relatively high. With low LET particles, i.e., high-energy secondary Compton electrons generated by Co-60

gamma irradiation, the charge pair line density is low. Compared to heavy ion irradiation, fewer electron-hole pairs will recombine, which makes the final charge yield higher. In other words, the gamma radiation from the Co-60 source is more efficient than heavy ion in creating the trapped charge in the oxide layer. The charge yield created by Co-60 source and heavy ions have been reported in [79] and [73] respectively. The fraction of un-recombined holes created by heavy ions is much lower than that generated by the Co-60 source (Figure 4.20), which is consistent with the above analysis. Because of the high-charge yield, the threshold voltage shift in the Co-60 test is more than that in the heavy-ion test, and it leads to more significant RO frequency degradation in the Co-60 test.

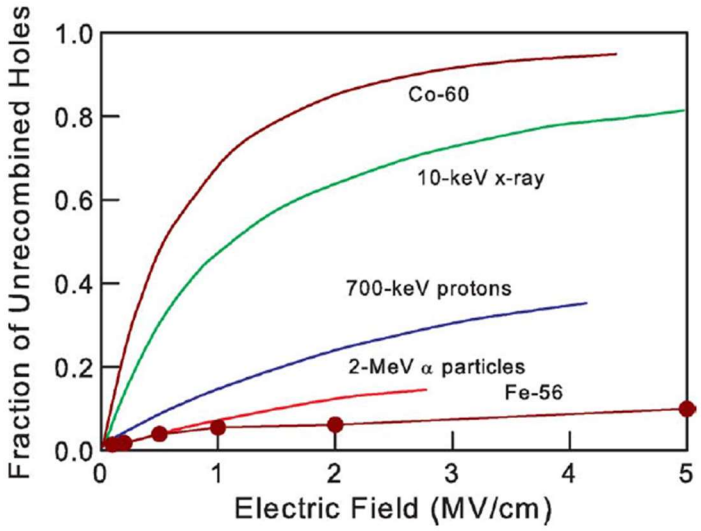


Figure 4.20 Charge Yield vs Electric Field [53]

4.8 TID Experiment at ESTEC

To verify the Co-60 Test result at the University of Saskatchewan, another TID test was performed at ESTEC, NL. The TID test at ESTEC also focused on the RO frequency drop versus the cumulative radiation amount.

The radiation facility at ESTEC is equipped with a 2000 Ci Co-60 gamma source which was reloaded on May 2016. The facility consists mainly of two parts, a radiation cell and a large external control room. The control room has 14 feedthrough holes, which enable remote control

and real-time data acquisition. The layout of the radiation cell and the cross-section of the feedthrough holes are shown in Figure 4.21.

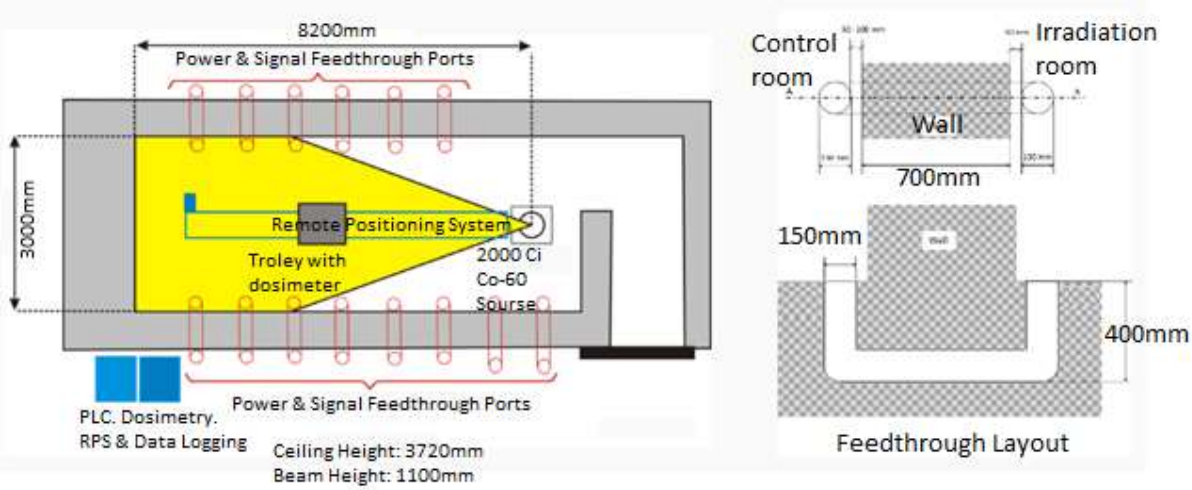


Figure 4.21 Radiation Facility Layout [81]

4.8.1 Test Setup

As is shown in Figure 4.21, there is a cart inside the radiation room, which can move along a rail. By changing the position of the cart, the dose rate on the device side can be controlled. Thus, the DUT card can be placed on the cart for accurate dose-rate control. The total distance between the DUT card and the nearest feedthrough hole is around 2m. Taking the distance of the feed-through hole into consideration, the connecting cable length must be more than 4m, which introduces some challenges to the experiment.

One challenging problem is the signal speed. The signal frequencies we observed are tens of megahertz. A normal flat ribbon cable cannot transmit the signals at this speed for 4 meters. Even with the HD68 ribbon cable (Figure 4.24, shielded and twisted), the maximum frequency will be only 5MHz. To solve this problem, an LVDS signal type was used to pass the high frequency signals.

Another problem is the signal quality after such long-distance transmission. The CONF_CLK and CTRL_CLK_IN signals are critical to the testing system since they control the communication interface between the DUT chips and the FPGA. After long-distance transmission, the clock

signals will be distorted and the slopes will be increased. Without a sharp and clear clock edge, the data sampled will be incorrect. To make the clock edge clear, after the long-distance transmission, each of the clock signals is connected to a Schmitt trigger before fed into the DUT chip.

The third problem was introduced by the LVDS signal. Our controlling FPGA, Virtex5, can only support a LVDS25 signal type. If a set of signals in the FPGA IO bank is set to this type, the other signals in the same bank can only be set to LVDS25 or LVCMOS25 which is the 2.5V standard. However, the signal level at the DUT chip side is 1.8V which is incompatible with the LVCOMS25 standard. So, the related signals need to go through a level shifter chip to shift the signal level to a range between 1.8V and 2.5V.

Taking all the above factors into consideration, the TID test setup at ESTEC was more complicated than the test setup at the University of Saskatchewan. Figure 4.22 shows the ESTEC TID test scheme. Figure 4.23 shows the whole setup of the ESTEC TID experiment.

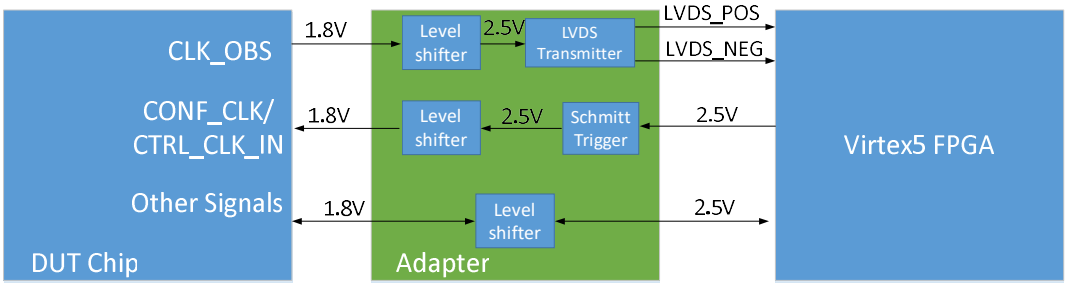


Figure 4.22 ESTEC TID Test Scheme

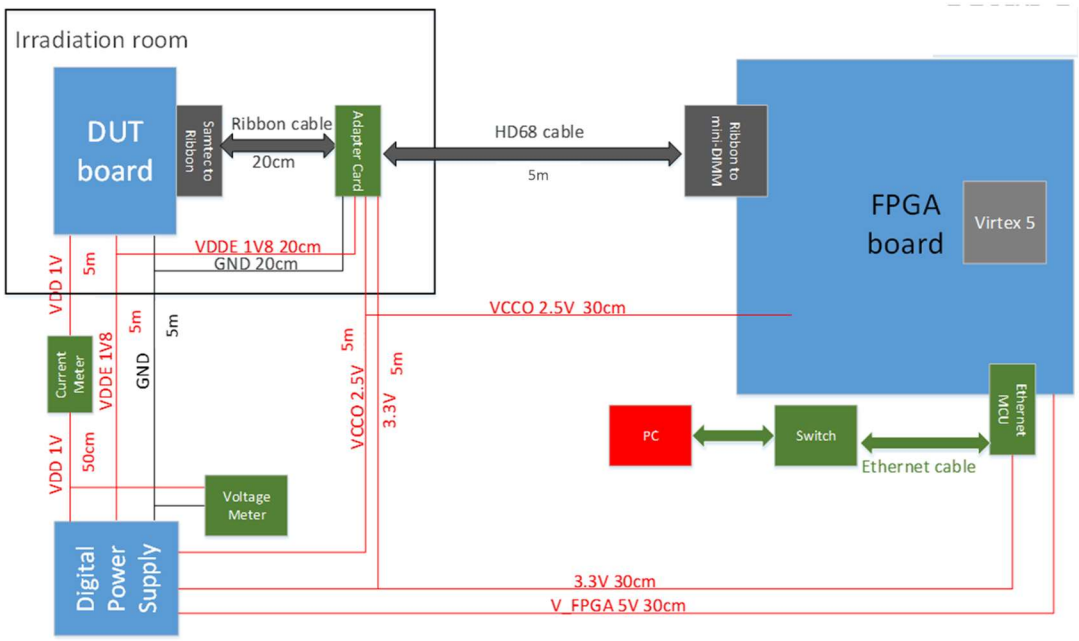


Figure 4.23 ESTEC TID Test Setup

Figure 4.24 shows the adapter cards and the HD68 ribbon cable.

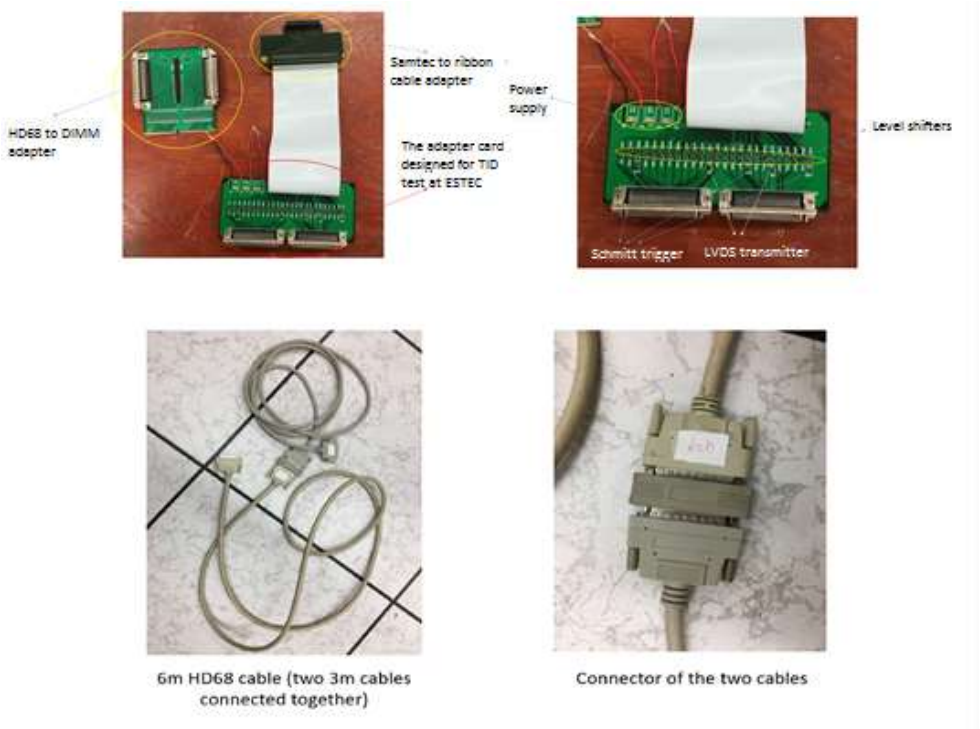


Figure 4.24 Adapter Cards and HD68 Ribbon Cable

Figure 4.25 shows the LVDS signals waveform.

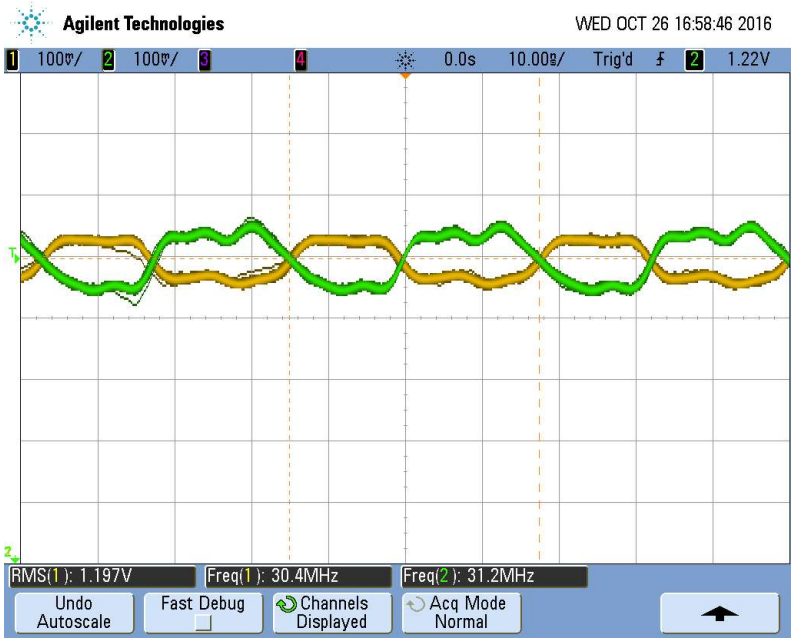


Figure 4.25 Adapter Cards and HD68 Ribbon Cable

4.8.2 Test Procedure

The TID experiment procedure at ESTEC was similar as TID test at the University of Saskatchewan. Two DUT chips were mounted on the test card and they were exposed to the irradiation simultaneously. In the test, both DUT chips were biased and the main ROs were enabled. After the desired accumulative dose amount, the chips were reconfigured and all the RO frequencies were read out. Then the whole system was restarted and kept running until the next test point.

4.8.3 Test Result

Table 4.8 shows the summary of the TID test result at ESTEC.

Table 4.8 TID Experiment Test Points

Target Total Dose (krad(Si))	VT1 (MHz)	VT1 - %	VT2 (MHz)	VT2 - %	PC (MHz)	PC - %	Main RO (MHz)	Main RO - %
Initial	315.6	100	463.0	100	693.2	100	1068.8	100
10	311.7	98.8	459.9	99.3	689.0	99.4	1062.7	99.4
30	304.3	96.4	454.1	98.1	680.9	98.2	1049.6	98.2
50	297.1	94.1	448.6	96.9	673.8	97.2	1035.9	96.9
100	281.7	89.3	428.5	92.5	648.8	93.6	1006.8	94.2
300	230.4	73.0	382.0	82.5	579.7	83.6	884.2	82.7
444	203.4	64.4	354.8	76.6	539.1	77.8	814.3	76.2
632	174.9	55.4	323.8	69.9	491.1	70.8	733.2	68.6
748	161.3	51.1	308.0	66.5	466.9	67.4	693.5	64.9
799	155.6	49.3	301.1	65.0	456.4	65.8	677.3	63.4
967	137.7	43.6	278.6	60.2	422.2	60.9	624.0	58.4
1000	134.6	42.6	274.4	59.3	416.2	60.0	615.4	57.6

The Co-60 test result at ESTEC was similar to the result obtained at the U of S. After 1Mrad(Si) irradiation, all the ROs dropped to less than 60% of the original frequencies. Because of the gate type, the VT1 RO dropped the most to around 40 percent, which is consistent with the previous U of S result. The comparison between the results from ESTEC and the U of S is shown in Figure 4.26.

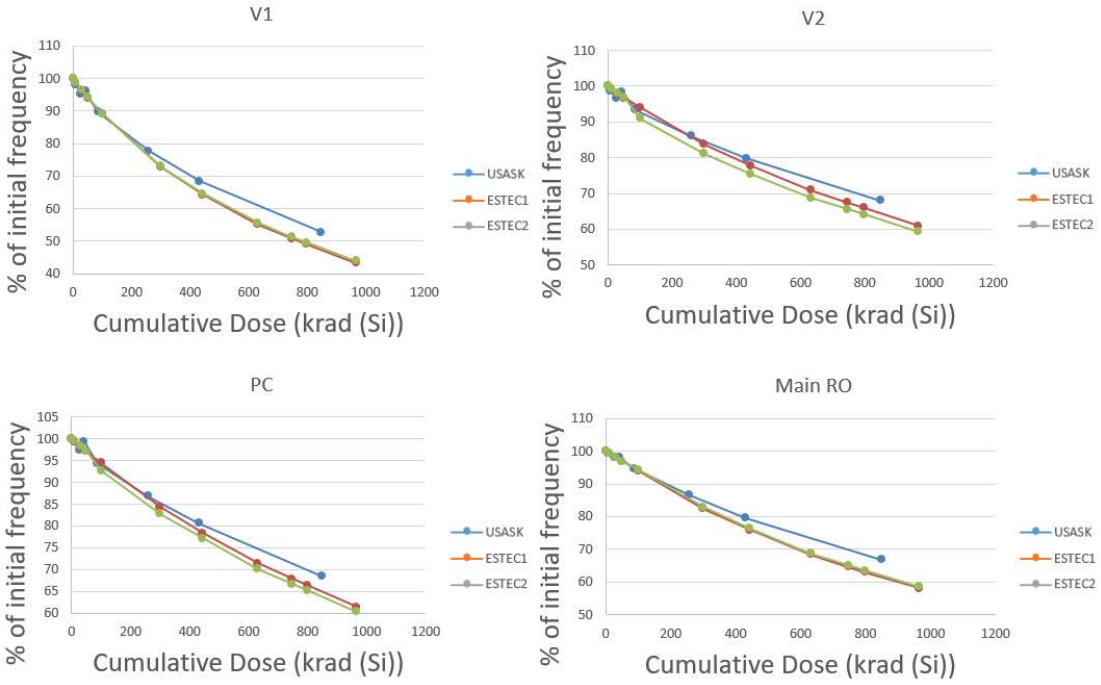


Figure 4.26 TID test results comparison

From Figure 4.26, we can see that with an increase in the dose amount, the discrepancy in the two tests increases. When the dose amount is more than 800 krad(Si), all four types of ROs have around a 5% difference. Since the Co-60 facility at the U of S does not have the on-site dose meter, the dose rate calibration at the U of S might be the reason for the differences.

Figure 4.27 shows the dose rate calibration chart at the U of S. The red circle shows the approximate location of the DUT chips where they received around 90%-95% of the maximum dose rate. Taking the calibration into consideration, we can draw the comparison graphs shown in Figure 4.28.

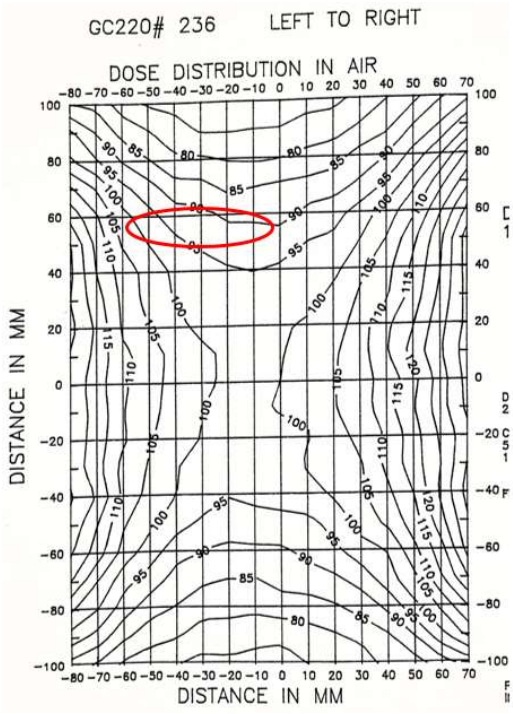


Figure 4.27 TID Facility Calibration Chart at the U of S

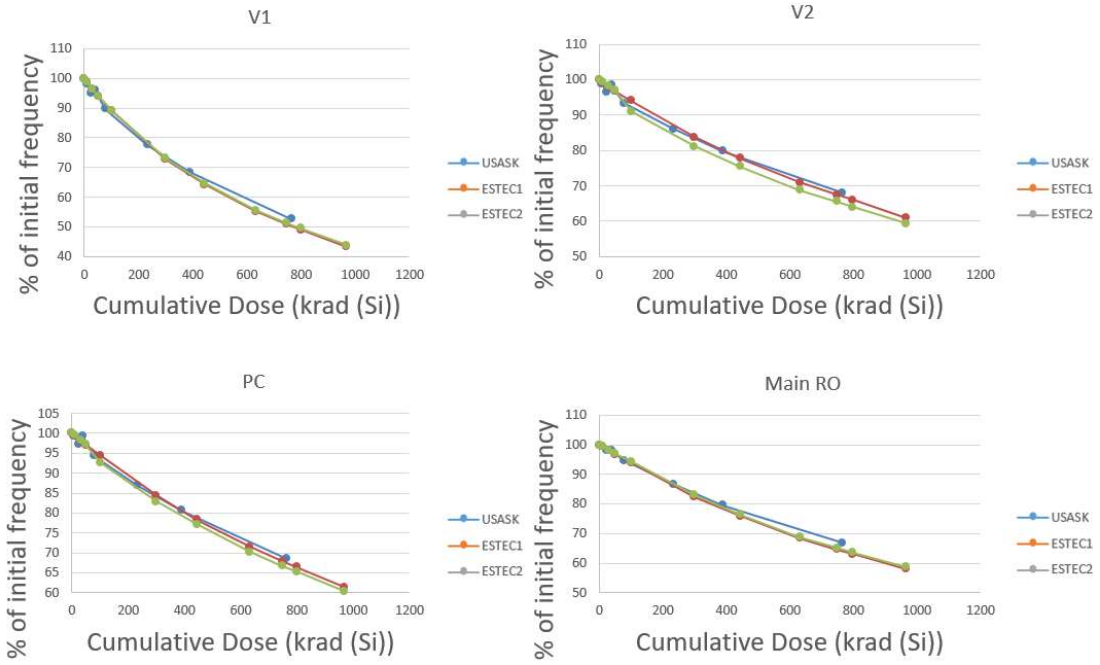


Figure 4.28 Calibrated TID Test Results Comparison

As can be seen from Figure 4.28, after calibration, the two Co-60 TID test results are nearly the same.

After the test chips received 1 Mrad(Si) total dose irradiation, another functionality test was performed. Both chips worked properly with a low-frequency clock signal. Because the transistor speed decreased with the dose accumulation, the configuration and event reporting interface could not work at a speed of 25MHz speed. However, if the frequency of these two clock signals were slowed down to 5MHz, most of the functionalities were satisfactory. Only the CREST chain in chip 2 keeping report event. It is assumed that the CREST chain also could not work at high speed after irradiation.

4.8.4 ESTEC TID Test Conclusion

The result of the Co-60 TID test at ESTEC is consistent with the result obtained at the U of S. We can conclude that the gamma source can generate a more significant TID effect than the heavy-ion test with the same amount of accumulated dose. After 1 Mrad(Si) irradiation, the RO frequencies dropped significantly, which means the speed decreased in the RO invertors. In addition, most of the circuits in the test chips were still functioning properly except the CREST circuit in test chip 2. Since UTBB-FDSOI technology can adjust the back gate voltage, we can some how counterweight the influence of TID effect by changing the back gate voltage. Considering the low SER of ST 28nm UTBB FDSOI technology, it could be a candidate for various radiation environments where high speed, low power and low SER are required.

In the TID test at ESTEC, we also saw the importance of monitoring the on-site dose amount. Without this facility, the test result would have a 5%-10% error bar.

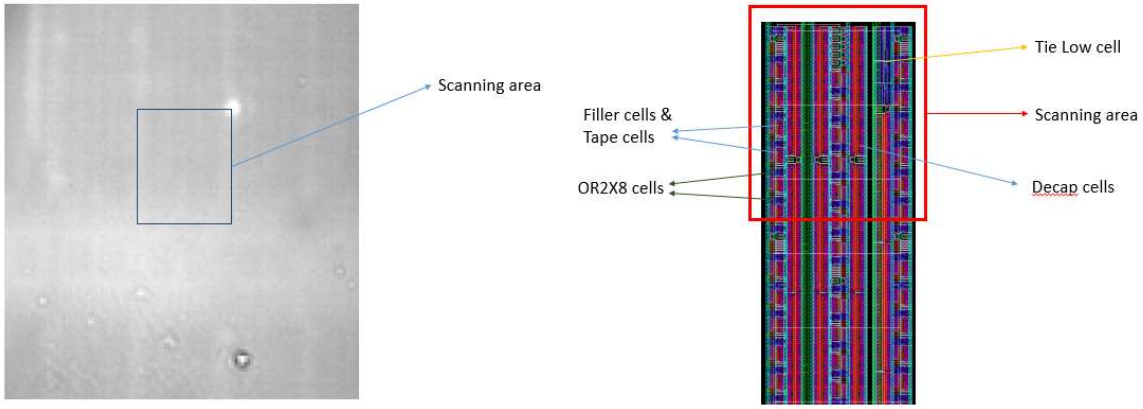
4.9 Laser Test at NRL

To study the pulse broadening effect and the SET event rate versus clock frequency, another laser test was performed at the Naval Research Laboratory (NRL), Washington DC. The NRL laser system can generate laser pulses with a pulse width of 1ps. The laser wave length is 590nm and the spot size is around 1um. Unlike the laser system at the University of Saskatchewan, the NRL laser system can output the laser pulse position information in real time. This feature allows the

test of to scan the area of interest, since the error count versus location information can be correlated.

4.9.1 Laser Test on OR2 chain

To verify the U of S laser test result on the OR2 chain, we scanned the pulsed laser on a large area of the OR2 chains with three detectors. As shown in Figure 4.29, the scanning area covered one third of the whole OR chain, and it covered various kinds of gates, including the OR2 gates, filler cells, tape cells, decoupling caps and tie low cell which gives the OR chain a fixed 0 input.



(a) Scan area under image laser (b) Scan area in layout

Figure 4.29 OR2 Chain Scanning Area

The scanning test results of the three kinds of detectors are shown in Figures 4.30 to 4.32.

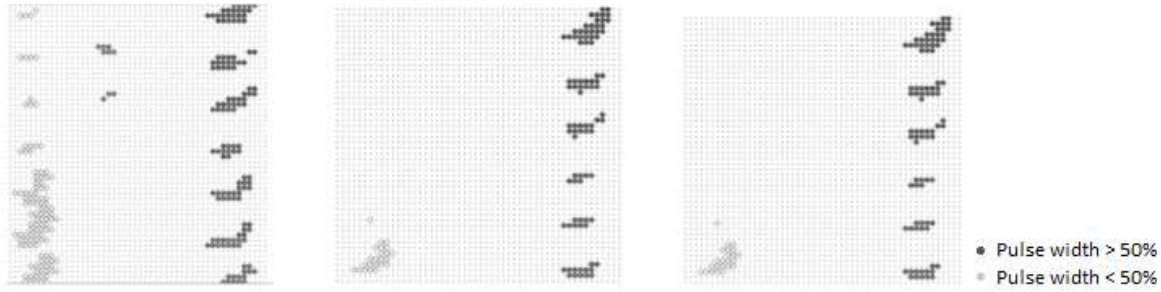


Figure 4.30 OR2 Chain with Vernier Detector Laser Scanning Results

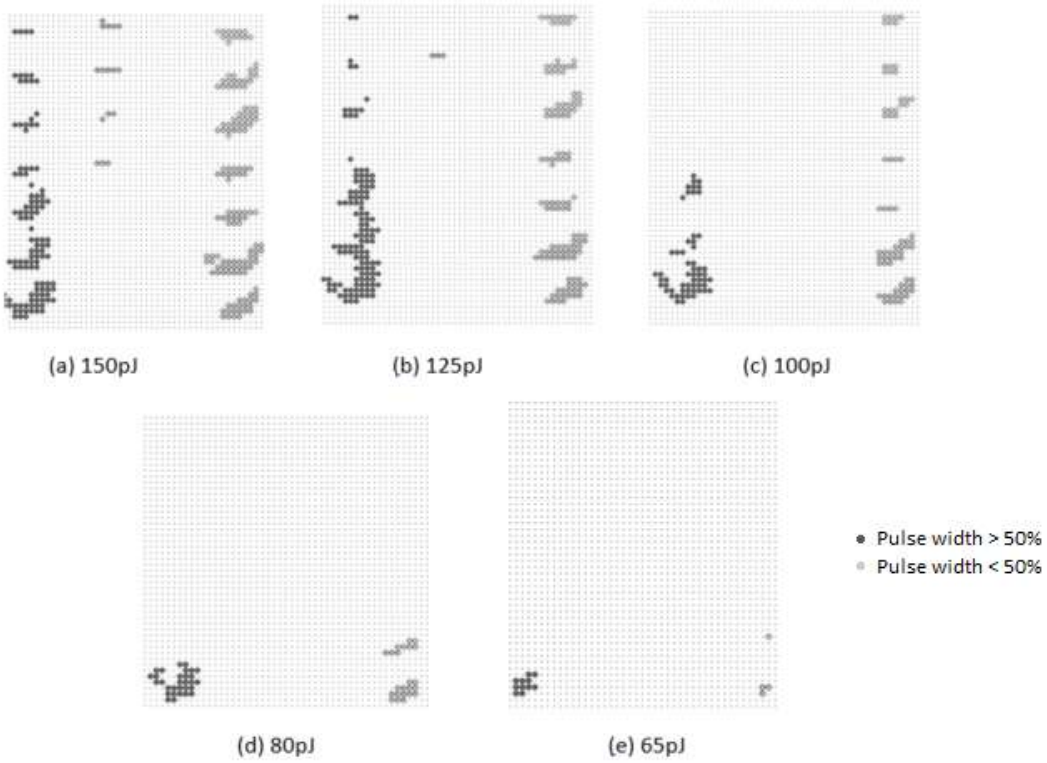


Figure 4.31 OR2 Chain with Pulse Capture Detector Laser Scanning Results

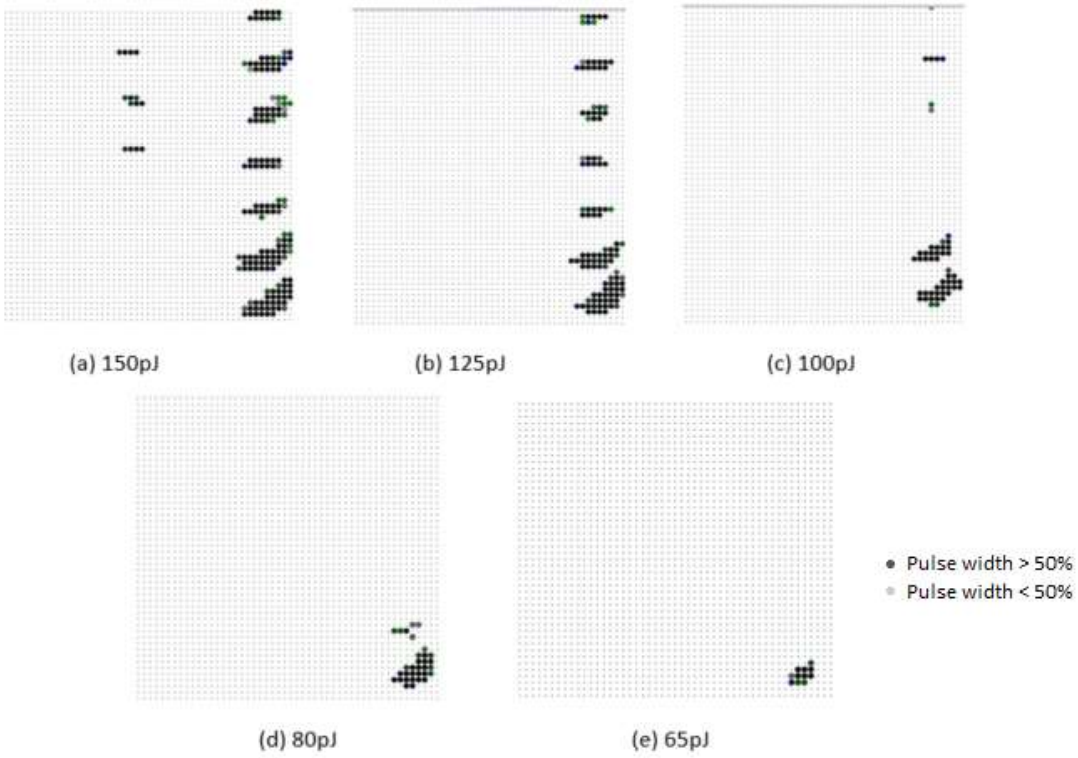
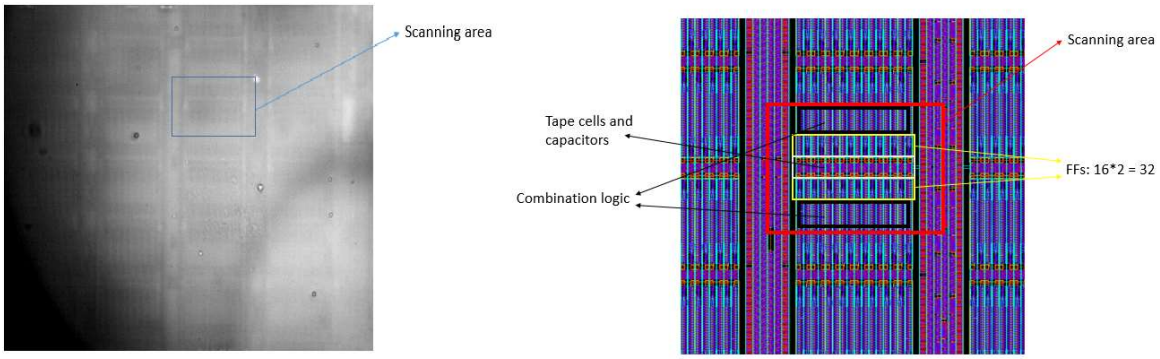


Figure 4.32 OR2 Chain with Pulse Filter Detector Laser Scanning Results

From the figures, we can clearly see the pulse broadening effect. The gates which are far from the end of the chain had events with larger pulse widths and the event rate of these gates are much higher than the gates close to the chain tail. With a decrease in the pulse energy, the event rate dropped dramatically (fewer dots) but the detected pulse widths were similar to the ones generated by the high-energy laser pulses (the color of the dots at the same position remained the same), which is consistent with the observation at the U of S.

4.9.2 Laser Test on CREST circuits

In another laser test performed on the CREST circuits, the test focused on studying the SET event rate versus the clock frequency. In this test, we kept the laser pulse energy at 150pJ and continuously kept the data input to the CREST chain at 0. As shown in Figure 4.33, we chose an area with 32 basic CREST cell structures (1FF + combinational logic). By changing the CREST chain clock frequency, we took the research in how the clock frequency influenced the SET rate.



(a) CREST scan area under image laser (b) CREST scan area in layout

Figure 4.33 Crest Circuits Scanning Area

Figures 4.34, 4.35 and 4.36 show the laser scanning test results at 580MHz, 750MHz and 1GHz, respectively. In the illustration, the red dots represent the high-event rate locations and the other dots represent the locations with a lower event rate. In the three illustration, the red dots concentrate horizontally in the middle of the picture. Comparing to the scanning area shown in Figure 4.33, we can see these red dots correspond to the flip-flop areas. As a result, the events that occurred in this area were SEU events, and they were not influenced by the clock frequency. Therefore, the densities of red dots in Figures 4.34, 4.35 and 4.36 are similar. In contrast, the dot densities and

colors at the top of each illustration i.e., the combinational logic area, are quite different. With the increase of the clock frequency, the SET event rates increased, which is consistent with the previous prediction.

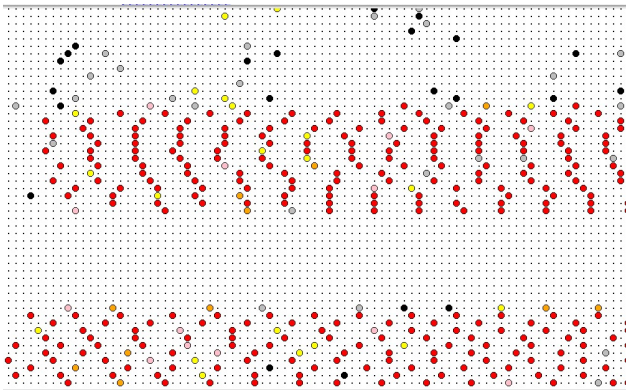


Figure 4.34 CREST Circuits Scanning Result at 580MHz

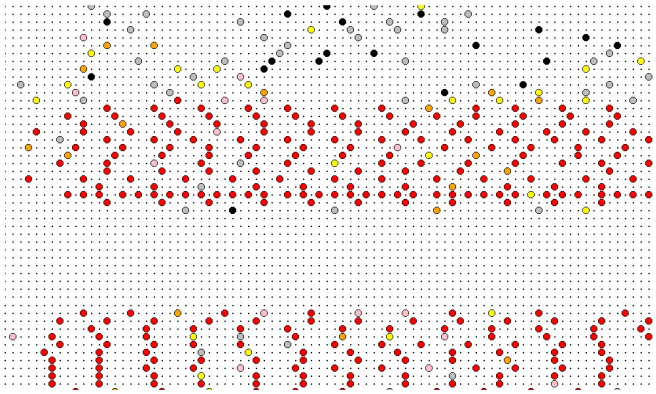


Figure 4.35 CREST Circuits Scanning Result at 750MHz

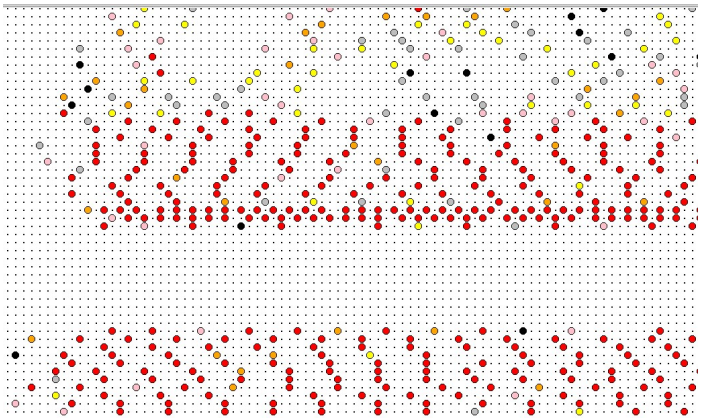


Figure 4.36 CREST Circuits Scanning Result at 1GHz

Chapter 5: ARM SET Test Chip (AR0)

5.1 Top-Level Specification

The main goals for the AR0 test chip are to study the impact of SEUs and SETs on different versions of a hardened processor. The ARM Cortex-M0 core is used as the sample processor design for performing these studies. Table 5.1 shows the primary information of M0 core.

Table 5.1 ARM Cortex M0 Design Information

Flip-Flop Count	840
Area Estimate (28nm FDSOI Library)	17 000 um^2

To achieve the design goals, five instances of the ARM-M0 are implemented on the die. There is a reference variant implemented with regular flip-flops and normal logic. During radiation testing, this will serve as a baseline. A second variant is implemented using custom-designed DICE flip-flops. This variant will serve as a baseline for the combinatorial (SET) sensitivity, including SETs in the clock tree and SETs in the data-path. There will be three other variants (4,5,6) where the combinatorial logic will be protected with increasing levels of approximate logic (low, medium, high). Please refer to [84] for the details of approximate logic The five processor versions are enumerated in Table 5.2.

Table 5.2 Processor Core Variants

1	Reference Version: Regular flip-flops, regular combinatorial logic.
2	DICE Version: DICE flip-flops, regular combinatorial logic, regular clock tree.
3	Approximate Logic – Low: DICE flip-flops. Low effort approximate combinatorial logic
4	Approximate Logic – Medium: DICE flip-flops. Medium effort approximate combinatorial logic.
5	Approximate Logic – High: DICE flip-flops. High effort approximate combinatorial logic

In addition to the five processors, there is a region on the die that contains two long flip-flop chains. One chain is built using the reference flip-flop and the other chain is built using the DICE flip-flop. These two chains share a common input and a common clock; however, they have separate outputs. All processors will share the same on-chip memory (4KB – 32 bit X 1024 entries) which will be implemented using TMR. The intent is that the embedded memory should be fully radiation

tolerant and not cause any failures during testing. For debug or non-radiation testing conditions, the memory can operate in one of five modes. Only one processor can be enabled to run at a time and this processor will be the sole master of the memory. The external memory controller can also access the memory, and it has strict priority over the processors. A tentative floor plan of test chip #2 is shown in Figure 5.1. A single instance of the RAM will be allocated approximately 150 um x 300um or 45 000 um^2 in the center of the die. The memory will contain 3x1024x32=98 304 bits.

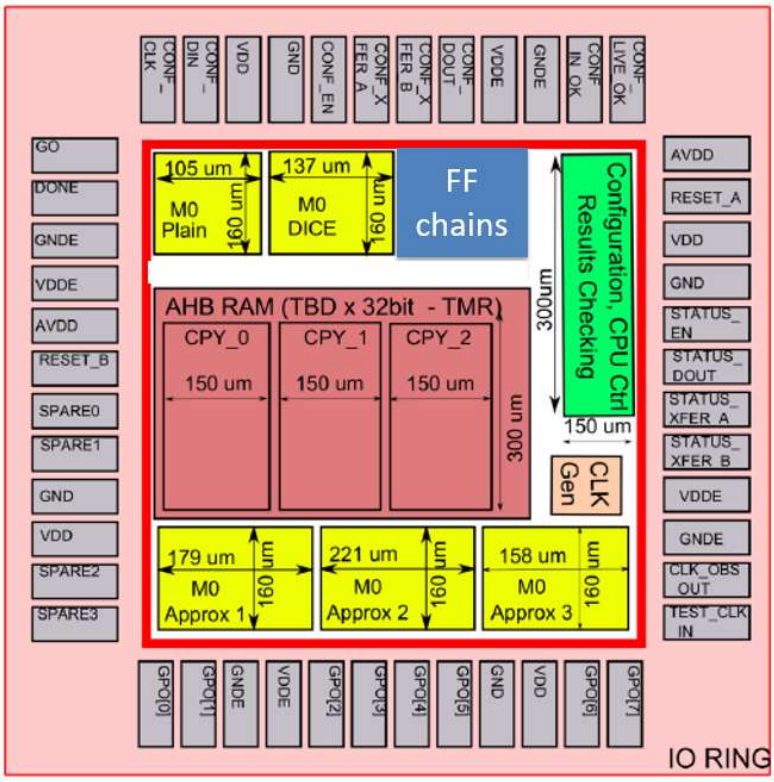


Figure 5.1 AR0 test-chip floor plan

5.2 Configuration, Clock Generation, and Status Interface

5.2.1 Configuration Interface

A serial configuration interface will be used to shift in configuration information. This will control the selected clock frequency, tune parameters for the RAM, select the processor and configure debug circuitry. The AR0 chip configuration interface structure is quite similar to the one in the ST1 chip, which is described in detail in section 3.2.

5.2.2 Clock Generation Logic

The clock will be provided with an on-chip Ring Oscillator. The Ring Oscillator will have a maximum frequency of approximately 1 GHz and will be controllable in steps of approximately 50 MHz to 200 MHz. It will also be possible to provide an external clock source, but this will be used primarily for debugging as the IO pads will limit the maximum frequency to approximately 200 MHz. The basic design of the programmable Ring Oscillator will be the same as for the ST1 test chip; however, the delays will be tuned to obtain the desired frequency ranges for the AR0 chip. The configuration and status logic operates with its own, lower speed (e.g., 10-50 MHz) clock which is independent from the high-speed clock. Table 5.3 shows the designed and required clock frequencies in the AR0 chip.

Table 5.3 Available On-Chip Clock Frequencies

RO Delay (ps)	RO Freq (MHz)	DIV 1 (MHz)	DIV 2 (MHz)	DIV 3 (MHz)	DIV 4 (MHz)	DIV 5 (MHz)	DIV 6 (MHz)	DIV 8 (MHz)	DIV 32 (MHz)
302	3311	3311	1655	1104	828	662	552	414	103
320	3125	3125	1562	1042	781	625	521	391	98
330	3030	3030	1515	1010	758	606	505	379	95
350	2857	2857	1429	952	714	571	476	357	89

5.2.3 Status Interface

A second serial interface is used to shift status information out of the processor core. The status interface is used to read back information from inside the chip, including performing read operations to the memory.

The status interface is conceptually similar to the control interface; however, its purpose is to shift out status information. The configuration and status interface share the same serial clock (CONF_CLK), however, they have separate enables (CONF_EN and STATUS_EN). There are also two versions of the status information, a live version and a shifted-out version. When STATUS_XFER_A and STATUS_XFER_B are high on the rising edge of CONF_CLK, then the live status information is transferred to the serial shift register. The serial shift register is clocked on the rising edge of CONF_CLK when STATUS_EN=1. Each time it is clocked, one bit of status

information is output on STATUS_DOUT. In total, there are 48 bits of status information. Internally, the status information is protected by an odd parity over every 16 data bits. The status information is shifted out MSB first, and the parity can be checked by the control FPGA after the full 48+3=51 bits have been shifted out.

5.3 Command Protocol

The AR0 test chip can be controlled by issuing commands using the configuration interface and then retrieving the status using the status interface. There is a controller which takes its commands using the configuration interface, which then processes the commands and reports the response, using the status interface, as shown in Figure 5.2.

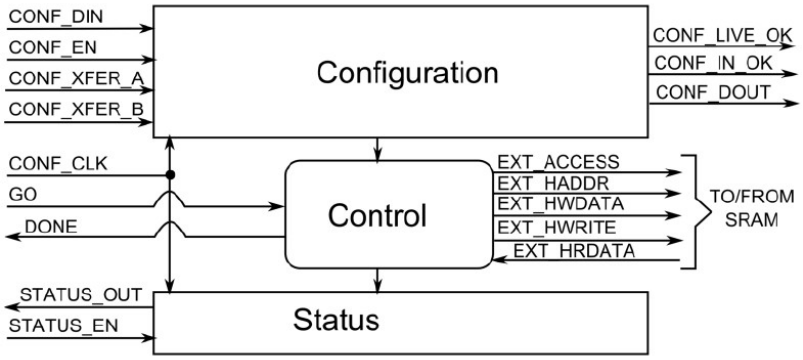


Figure 5.2 High-level Control Structure

The configuration interface contains the following fields (Table 5.4) which specify which command to execute and the arguments for that command.

Table 5.4 List of Configuration Fields

Field	Width	Description
COMMAND	4 bits	Operation to perform. See Table 5.5.
ADDR	12 bits	Address for reads.
WDATA	32 bits	Data for write / fill operations.
TADDR	12 bits	Address for writes.
LENGTH	16 bits	Number of operations.

Table 5.5 lists the available commands, their encoding, and the arguments for each command.

Table 5.5 On-Chip Commands

Command	ADDR	WDATA	TADDR	LENGTH	Description
NOOP: 4'b0000					Dummy command. Controller does nothing.
READ: 4'b0001	x				Memory read at address ADDR.
WRITE: 4'b0010		x	x		Writes WDATA to address TADDR.
FILL: 4'b0011		x	x	x	Fills LENGTH addresses starting at TADDR with WDATA.
CSUM: 4'b0100	x			x	Computes a checksum value for LENGTH words starting at ADDR.
CPY: 4'b0101	x		x	x	Copies LENGTH words from ADDR to TADDR.
RUN: 4'b0111				x	Runs program on one core. Timeout after LENGTH clocks.

After a command is shifted in using the configuration interface, it is activated by the rising edge of the "GO" input. When the command has completed executing, this is indicated by the rising edge of the "DONE" output. At this point in time, the status can be loaded into the status interface and shifted our serially. A timing diagram for the typical command sequence is shown in Figure 5.3.

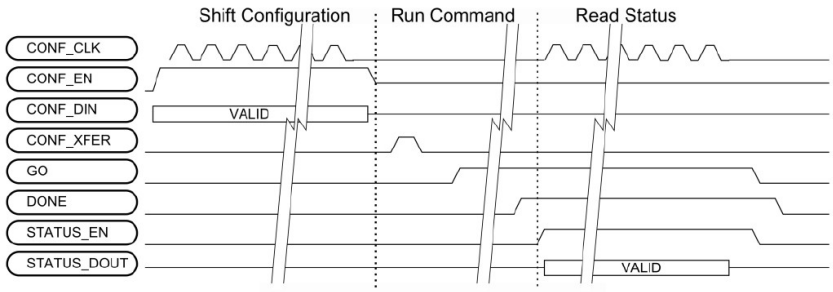


Figure 5.3 Typical Command Execution Sequence

5.4 ARM M0 Utilization

Not all features of the ARM M0 will be used in this test chip. Specifically, the interrupts will not be connected (IRQ and NMI), there will be no bus errors and the RXEV feature is not used. All memory accesses are made in units of 32 bits. All peripherals will respond to reads in the next clock (no wait state) and writes in two clocks (one wait state). For this reason, many of the inputs

to the standard M0 core can be tied off and many of the outputs will not be used (see Table 5.6). The connections on the periphery of the wrapper are shown in Figure 5.4.

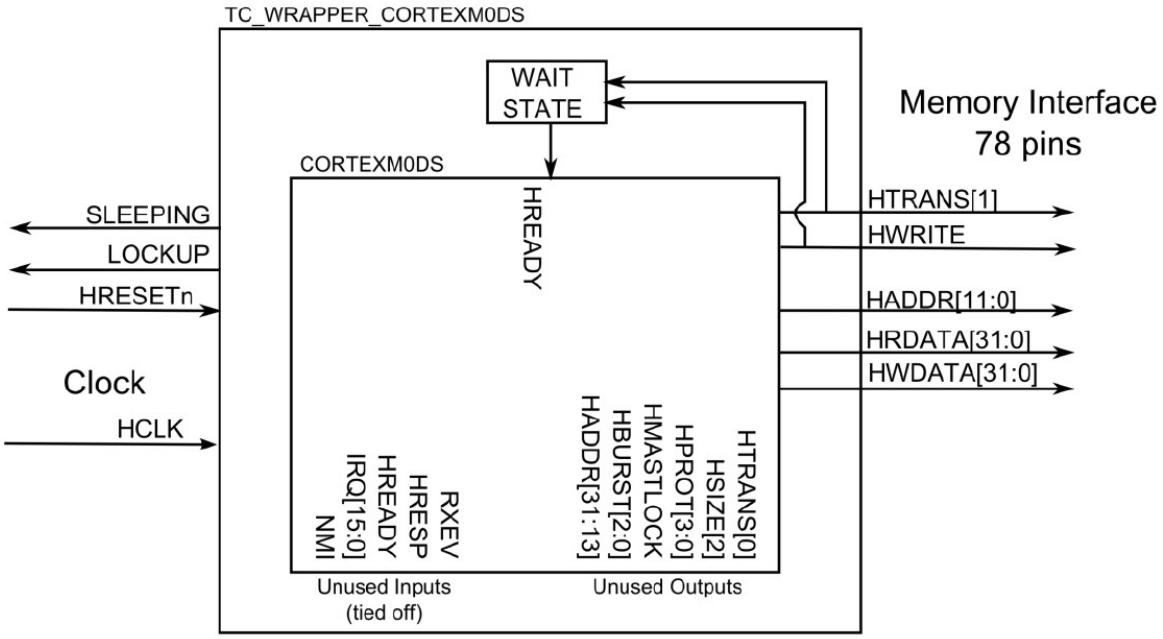


Figure 5.4 Wrapper Around ARM M0 Core

Table 5.6 ARM M0 Port Connections

Ports	Direction	Comment
HCLK	Input	Clock Input
HADDR[31:0]	Output	The test chip will have a maximum of 8 KB of external memory. Thus only HADDR[12:0] are used.
HBURST[2:0]	Output	This output is not used in this application.
HMASTLOCK	Output	This output is not used in this application.
HPROT[3:0]	Output	This output is not used in this application.
HRDATA[31:0]	Input	Used for memory read data.
HREADY	Input	This input is tied to a small circuit which automatically generates one wait state for all write operations.
HRESETn	Input	Control input that will be driven by local CPU controller.
HRESP	Input	This input will be tied to zero in our application. There are no data phase errors.
HSIZE[2:0]	Output	This output is not used in this application.
HTRANS[1:0]	Output	HTRANS[0] is not used. HTRANS[1] is used as a qualifier on writes.
HWDATA[31:0]	Output	This contains the memory write data.
HWRITE	Output	This is the qualifier for write transactions.
IRQ[15:0]	Input	We do not support interrupts in this application. These inputs are tied to zero.
NMI	Input	We do not support interrupts in this application. This input is tied to zero.
LOCKUP	Output	This output is fed to the local CPU controller.
RXEV	Input	This feature is not used in this application. Tied to zero.
TXEV	Output	This feature is not used in this application. Tied to zero.
SLEEPING	Output	This output is fed to the local CPU controller.
SYSRESETREQ	Output	This feature is not used in this application.

5.5 Memory Interface

There is a small on-chip memory which is used to hold the program and data. The memory is protected using TMR for: (i) simplicity, (ii) simple SET immunity, and (iii) high-speed operation. During radiation testing, the intent is to use the memory with TMR protection. However, for bring-up and test, there are five different modes of operation which are controlled by the configuration bits CONF_MEM_MODE[2:0]:

1. TMR mode (3'b111);
2. RAM0 – in this mode, only RAM0 is accessed (3'b001);
3. RAM1 – in this mode, only RAM1 is accessed (3'b010);
4. RAM2 – in this mode, only RAM2 is accessed (3'b100); and

5. Depth expand – in this mode the three memories are expanded in depth to make a 12 KB memory (3'b000).

The RAM operating mode is selected using the CONF_MEM_MODE[2:0] configuration bits. The memory interface follows the AMBA AHB bus protocol. All read operations occur in one cycle (zero wait state) and all write operations occur in two cycles (one wait state). The timing diagrams in Figure 5.5 and Figure 5.6 show the sequence for memory read and write operations, respectively. Note that in Figure 5.6, the HREADY signal is shown for reference, but in fact this signal is generated locally at the processor core.

For simplicity, the processor is the only bus master and the memory is the only slave. The memory only supports 32-bit operations and programs must be written and compiled with this constraint in mind.

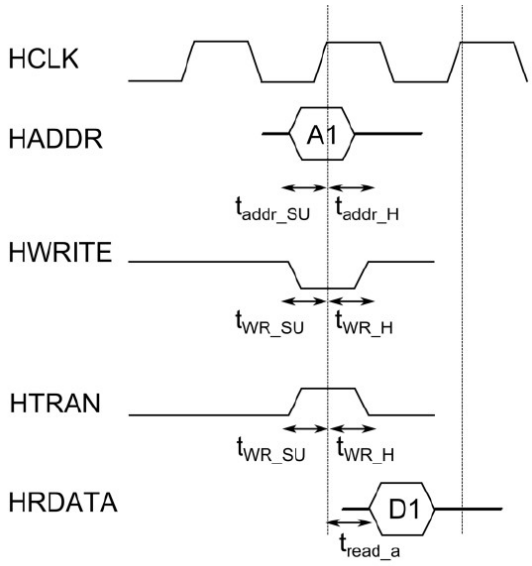


Figure 5.5 Wrapper around ARM M0 Core

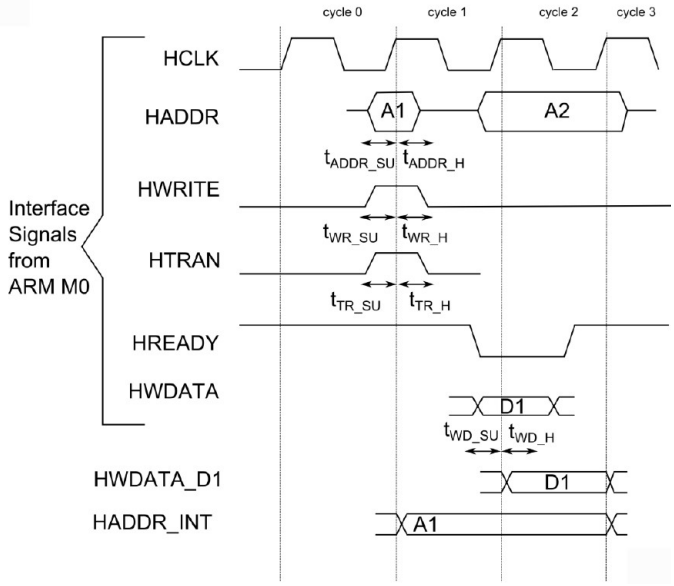


Figure 5.6 SRAM Write Cycle Timing with One Wait State

5.5.1 TMR Memory Wrapper

Three instances of the basic SRAM are combined in a TMR memory wrapper, as shown in Figure 5.7. On the input side, there is a 5:1 mux which selects the control signals from one of the five

processor cores, and which is controlled by the static configuration CONF_CORE_SEL[2:0]. This is followed by a mux that selects between the accesses inserted by the memory controller (EXT_ACCESS_A,B=1) or from the processor cores (EXT_ACESS_A,B=0). For write accesses, there is a small decode (shown as WE) which will only generate the HWRITE for a single RAM when operating in the RAM0, RAM1, RAM2, or which selects the correct RAM based on HADDR[11:10] when in depth expansion mode.

On the output side of the memory, there is a 4:1 mux that either selects the voted read data, or one of the individual read data buses. This mux is controlled by logic that depends on CONF_MEM_MODE as well as the two MSbits of HADDR[11:10].

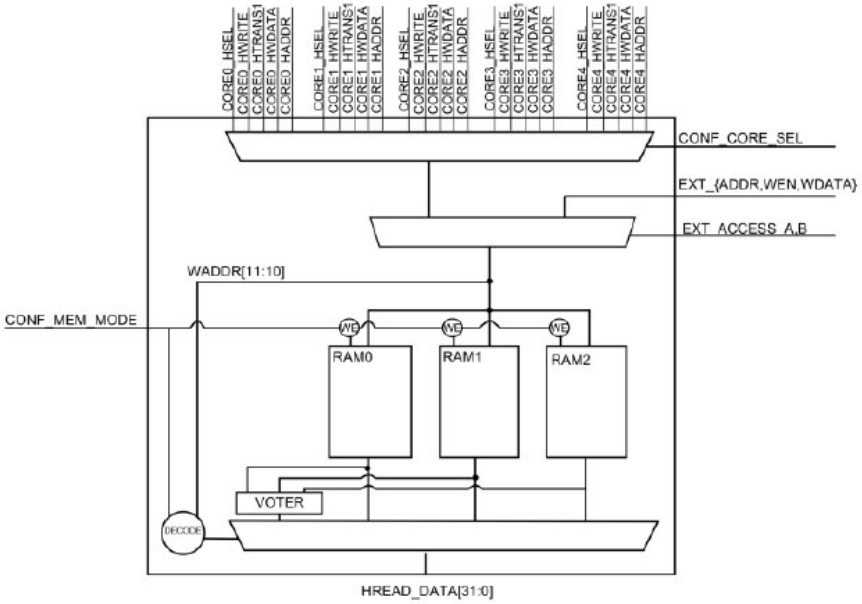


Figure 5.7 TMR Memory Wrapper

5.5.2 External Memory Controller

The on-chip memory is externally accessible using the configuration and status interface. There is a control module called TC_MAIN_CTRL which implements the status and control interfaces, as described in section 5.2.1 and section 5.2.3.

The main state machine for the external memory controller is shown in Figure 5.8. After reset, the controller starts in the IDLE state. On the rising edge of "GO," it executes the command that was shifted in on the configuration interface. The available commands are: READ, WRITE, FILL, CSUM, CPY, SCRUB and RUN. At the end of the command execution, the state machine stays in the DONE state until a falling edge is detected on GO.

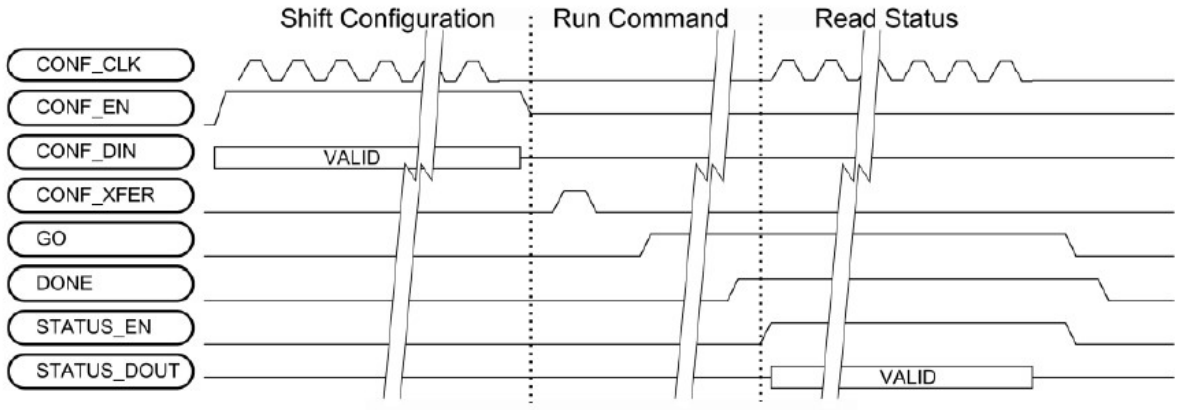


Figure 5.8 Timing Diagram for Configuration Operation

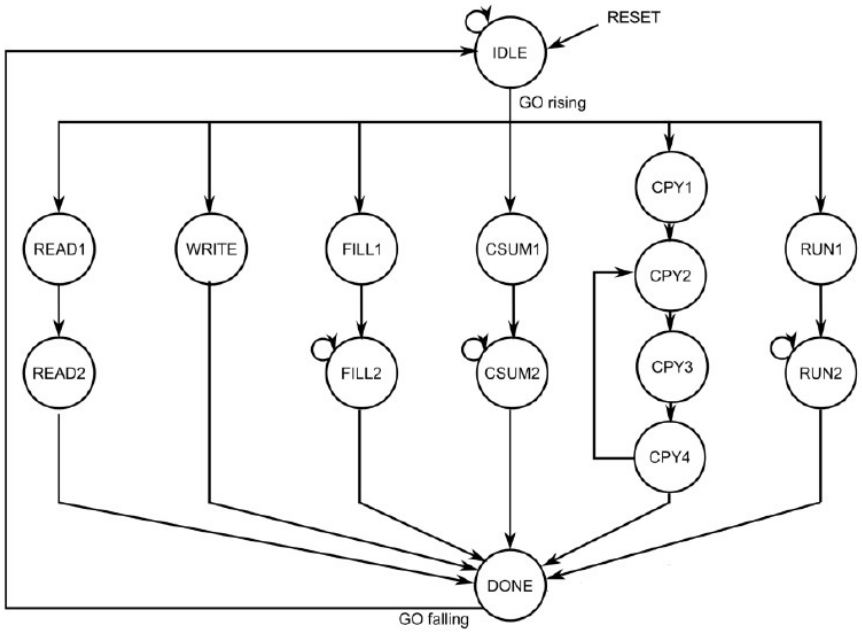


Figure 5.9 Memory Controller State Machine

A timing diagram showing the flow for executing a command on the test chip is shown in Figure 5.9. The first step is that the command is shifted in on the configuration interface. The command

is started by the rising edge of GO. When the command is completed, the chip outputs the "DONE" signal. At this point, the control FPGA will shift out the status. The FPGA can then de-assert the GO signal and the chip is ready for the next operation.

During a typical radiation test experiment, there is an initialization phase which might consist of initially filling the memory with all zeroes and then a series of write operations to store the program, as shown in Figure 5.10. When the program is fully written, its correctness can be verified by

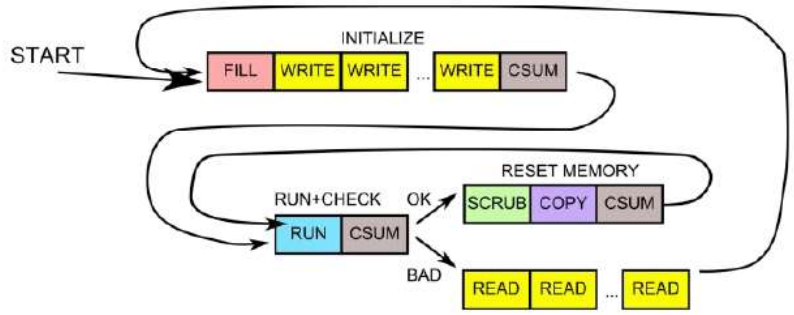


Figure 5.10 Typical Operation Sequence under Radiation Testing

performing a checksum operation (CSUM).

At this point, the device is ready to perform a test, and a RUN command can be issued to execute the program. At the end of the program execution, the contents of the memory can be quickly checked using a CSUM operation. If the checksum is correct, then the program was executed properly (OK). Before starting the next iteration, the memory should be scrubbed to remove any errors that may have occurred in one of the TMR memories. Next, the results of the program need to be cleared. This can be accomplished using either a COPY or a FILL operation. Prior to starting the next test iteration, a CSUM operation may be performed to ensure the memory is in a usable state. Then, the program can be launched again.

In the event of an error after the execution of the program, the memory contents can be read out. This can be done by sequentially reading each word in the memory. A slightly more efficient approach consists of performing a sequence of CSUM operations over smaller memory regions (e.g., 1/8th of the space) and then only reading out those regions whose checksum was not correct.

5.6 Critical Top-Level Timing

We identify three critical timing paths at the top-level:

1. The timing path from HTRAN, generated in the cores, through the top-level interconnect and muxing to the three RAMs – where it is flopped;
2. The timing path from HADDR, HWDATA, HWRITE in the cores, through the top-level interconnect and muxing, to the three RAMs – where it is flopped; and
3. The timing path from reading the RAM, through the VOTER, and then distributing to each core.

Estimates of the actual delays on these paths are given in Tables 5.7, 5.8 and 5.9. Based on the current estimates, the most critical timing is on the read path (Figure 5.11), and this will limit the operating frequency of the entire system to approximately 640MHz.

Table 5.7 Memory Write Path Critical Timing (Path 1)

Description	Delay
CLK -> Q	50 ps
HTRAN Logic (30 layers)	500 ps – Synthesis, P&R from M0
Flight Time (from core to central RAM module)	150 ps
7:1 MUX (5 cores + external memory controller)	~150 ps
Address, Control Flip-Flop Setup	50 ps
Total	~1000 ps

Table 5.8 Memory Write Path (Path 2)

Description	Delay
CLK -> Q	50 ps
HADDR Logic (24 layers)	800 ps – Synthesis, P&R from M0
Flight Time (from core to central RAM module)	~150 ps
7:1 MUX (5 cores + external memory controller)	~150 ps
Address, Control Flip-Flop Setup	50 ps
Total	~1200 ps

Table 5.9 Memory Read Access Path

Description	Delay
PRE -> Pre-charge Stopped	60 ps
Decoder	140 ps
PRE to Read	160 ps
SEA to HRDATA	40 ps
4:1 MUX	~100 ps
TMR Voter	~150 ps
Flight Time (from central RAM to each of 5 cores)	~150 ps
14 layers of logic	770 ps
Internal Flip-Flop Setup	50 ps
Total	~1550 ps

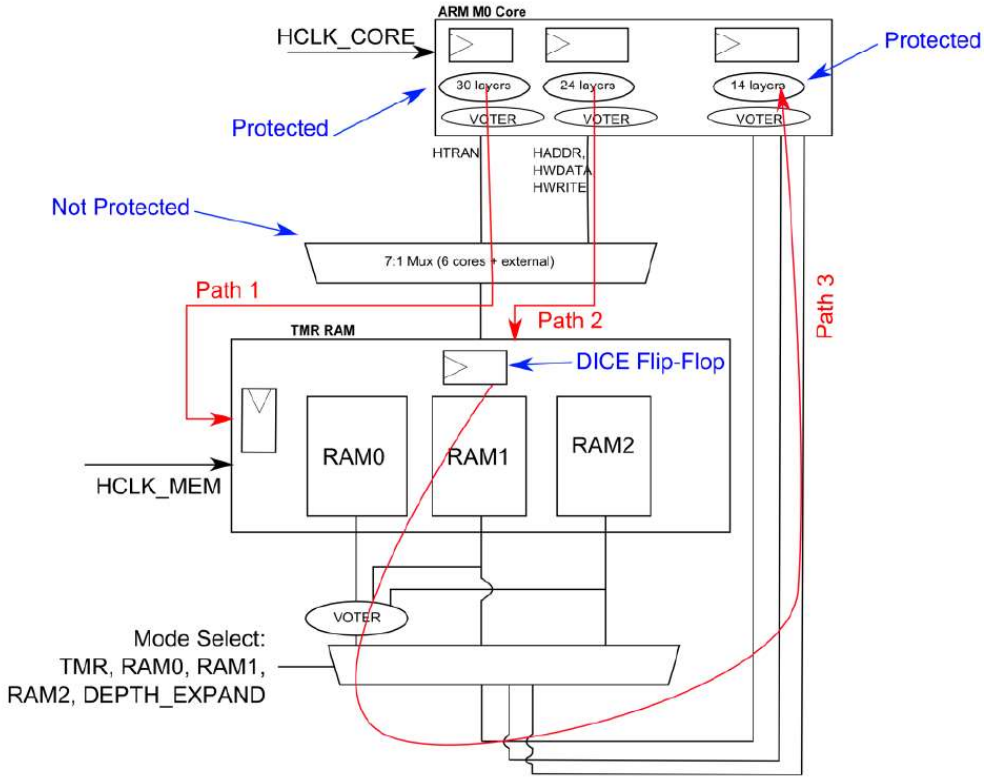


Figure 5.11 Memory Interface and Critical Timing

A clock tree will be created by CTS for each of the five cores and for the control logic. However, care is required to ensure that imbalances in the clock delay at the top-level do not negatively impact the operating infrequency. For this reason, two programmable delays are placed at the top-level on the clock going to the control logic and on the clock going to the memory. These delays

will be programmed to compensate for imbalances in the top-level clock insertion delay. These programmable delays will have 16 settings and will be controlled by four configuration bits. The programmable delay will range from 1 to 16 buffer delays (Figure 5.12). Each of the five processor cores is synthesized separately, and they each have their own clock tree insertion delay ($t_{ins\_c0}..t_{ins\_c5}$). The control logic is synthesized separately, and it has its own clock insertion delay (t_{ins_ctl}). Care, however, is needed to balance the delay between these two clock trees to ensure the signals between the two domains have the same clock reference.

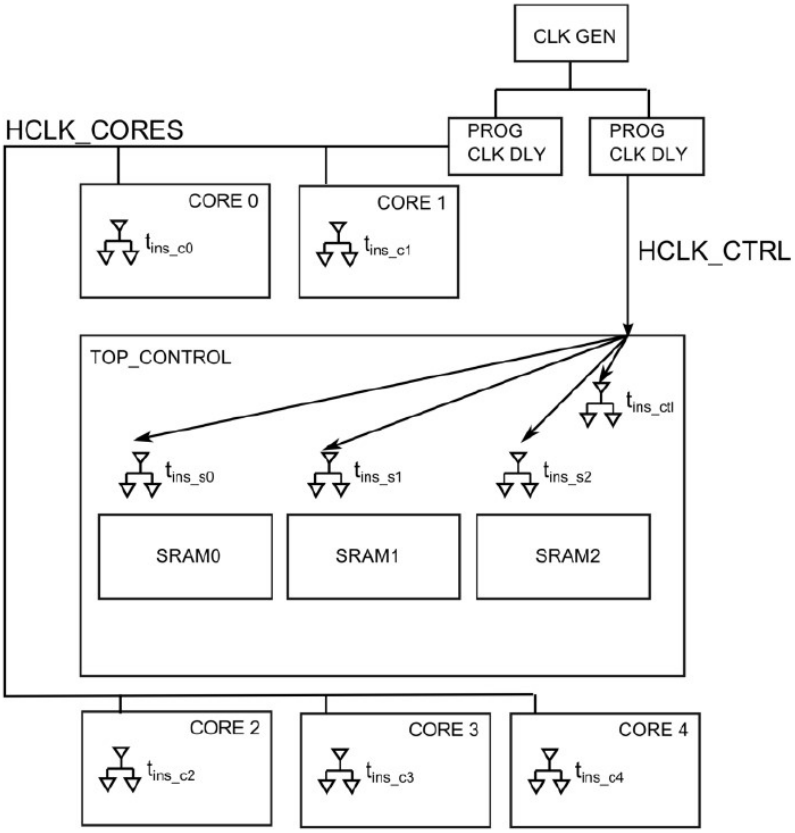


Figure 5.12 Top-level Clock Distribution with Programmable Delay

5.7 Approximate Logic ARM Core Simulation result

To validate the performance of the approximate logic method in protecting the combinational logic, a set of simulations has been performed by the collaboration of our group and the group from Universidad Carlos III de Madrid, Madrid, Spain.

Since software-based simulation, using, for example, Modelsim or VCS, is quite time consuming, AMUSE system [79], [80] was selected to perform the simulation. AMUSE was proposed by our cooperator, Luis Entrena in 2012. It is a multilevel FPGA emulation-based fault injection system which can be used to test the microprocessor sensitivity to soft errors. With this innovative system, the simulation of large digital circuits can be finished within an acceptable time.

Another advantage of AMUSE in testing microprocessor systems is that it can report the invisible errors, also known as latent faults. When a latent fault occurs, the system execution is correct but the circuit state is incorrect. Since latent faults might cause a system failure eventually, we consider them as real errors in our simulation.

In the simulation, three software benchmarks, qsort, string search and crc32 were selected. To fit the RAM size (1k in TMR mode and 3k in Depth mode) in the AR0 test chip, we reduced the program size to around 3k in the simulation. Later, in the laser test, the same program will be used by configuring the RAM in Depth mode.

In the simulation, the pulse width chosen is the worst case, 100% of the clock cycle, which means the SET pulses are extremely wide. However, considering the SET pulse width in the 28nm UTBB-FDSOI technology is small (refer to the test result of the ST1 chip), the error mitigation rate in the real test can be much higher than in the simulation.

Table 5.10 shows the comparison between the error mitigation rate and the overhead obtained from the Design Compiler. The simulation and synthesis results show that the approximate logic method can reduce the soft-error rate dramatically with a reasonable area overhead. Taking the 1% threshold core as an example, three fourths of the soft errors were filtered out while the core size increased by just less than 90%. Although the TMR logic can mitigate all of the errors, the circuit scale is increased by more than 200% (two full circuit copies and the voter).

Table 5.10 Error Mitigation Rate vs. Overhead (The second column is summarized from an unpublished paper)

Approximate logic level	Error masking rate	Area overhead
50%	67.5%	65.7%
20%	71.5%	74.1%
1%	76.5%	87.6%

Chapter 6: Summary and Future work

6.1 Summary

This PhD project focuses mainly on investigating the irradiation effects on the 28nm UTBB-FDSOI technology and the SET hardness method. In this project, two chips, ST1 and AR0, have been designed. The ST1 chip is used for the SEE and TID research on the 28nm UTBB-FDSOI technology, and the AR0 chip for the investigation of the approximate logic protection methodology. Both designs have passed post-silicon validation, which proves their functionality is as we expected.

Various irradiation tests have been performed on the ST1 chip. From the tests results, the following conclusion can be drawn.

1. The heavy-ion test was performed in REDEF. Five kinds of ions (Ne, Ar, Fe, Kr and Xe) were selected and the LET range was from 3 MeV·cm^2/mg to 100 MeV·cm^2/mg. From the cross-section curve, it can be concluded that compared to the bulk competitor, the 28nm UTBB-FDSOI technology is more resilient against SEEs. The saturated cross-section is about two order lower than the bulk technologies;
2. In the heavy-ion test, we observed the SET cross-section is two orders lower than the SEU cross-section. Moreover, the CREST chain sensitivity is quite close to the static SEU sensitivity, which means SEUs are still the dominant error source in both the dynamic flip-flop chains and the static SET detection circuits;
3. The OR2X8 chain contributed most of the SET events in the heavy-ion test. From the post-layout SPICE simulation and the pulsed laser test result, the pulse broadening effect is proven to be the cause. The extreme pulse distortion greatly enlarged the pulse width, and consequently, increase the cross-section of the OR2X8 chain. From further simulation and analysis results, we proposed the transistor size mismatch introduced the pulse distortion effect; and
4. The TID tests were performed in the Co-60 gammacell facilities both at the University of Saskatchewan and the European Space Agency. The test results show that the 28nm UTBB-FDSOI technology also performs well when exposed in an irradiative environment

for a long term. After absorbing 1000 krad(Si) total dose amount, although the chips showed great degradation on their speed, they still functioned properly. Compared to the TID result in the heavy-ion test, the Co-60 source shows much higher efficiency. We also noticed the significance of the on-site dose meter in the long-term TID test. Compared to the TID test performed at the U of S without an on-time dose meter, the test result at ESA/ESTEC is more accurate.

The AR0 chip is designed to estimate the performance of the approximate logic combinational circuits protection method. The chip includes five high-speed ARM Cortex-M0 processors with different protection levels, which can be used to evaluate the SEE rate in the irradiation tests. From the work in the design phase, and the simulation and test results, we can conclude the following:

1. Timing analysis plays a key role in the high-speed design which consumed significant efforts in the tape-out phase. To reach the 600MHz design goal, multiple analysis methods were used to check the circuit timing. Static Timing Analysis (STA) was performed to each core and the top-level control logic. The post-layout SPICE simulation was used to check the timing of the customized on-chip SRAM. Moreover, configurable clock delay adjustors were designed to synchronize the clock phase of each major macro;
2. The Verilog HDL simulation result shows the effect of the approximate logic protection method. With around 75% area overhead, the event rate decreased to about 1/8 of the original, which shows the approximate logic is quite efficient in protecting the combination logic; and
3. A minor bug related to the maximum program running time has been found in the post-silicon validation phase. This bug will limit the testability when the chip runs large loop programs. Because of using directed verification methodology, this bug is extremely hard to find. The bug illustrates the significance of the constraint randomization verification methodology and UVM in large-scale digital system design. Even with a large number of test cases, the functionality directed verification mothed is also hard to cover all the function points.

6.2 Future Work

Although much testing and analysis have been performed to research the irradiation effects on the 28nm UTBB-FDSOI technology, there is still some work needed in the future.

In both the heavy-ion test and the pulsed laser tests, some chains with certain gate types did not capture any event. The reason no pulse generated in these chains is still unclear. Further analysis combining TCAD and pulse injection SPICE simulation will be needed to investigate what prevents the gates from generating pulses.

When performing the laser test at the U of S, we observed the chips were damaged with even low-energy laser pulses. We suspect the damage was caused by the intensive energy that burned the chip. We need to investigate the silicon layer of the chip to find the reason.

The AR0 chip is being tested with the TPA pulsed laser. Other irradiation experiments need to be done in the future. The heavy-ion test should be performed with micro-beam heavy ions, and the cross-section curve of each core should be plotted. The TID test should be done to check the high-performance system speed degradation. Ideally, it would be worthwhile to generate the sensitivity map of each process, using the pulsed laser.

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