Improved Fault Tolerant SRAM Cell Design & Layout in 130nm Technology

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By

Govindakrishnan Radhakrishnan

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Head of the Department of Electrical and Computer Engineering
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University of Saskatchewan
Saskatoon, Saskatchewan, Canada
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ABSTRACT

Technology scaling of CMOS devices has made the integrated circuits vulnerable to single event radiation effects. Scaling of CMOS Static RAM (SRAM) has led to denser packing architectures by reducing the size and spacing of diffusion nodes. However, this trend has led to the increase in charge collection and sharing effects between devices during an ion strike, making the circuit even more vulnerable to a specific single event effect called the single event multiple-node upset (SEMU). In nanometer technologies, SEMU can easily disrupt the data stored in the memory and can be more hazardous than a single event single-node upset.

During the last decade, most of the research efforts were mainly focused on improving the single event single-node upset tolerance of SRAM cells by using novel circuit techniques, but recent studies relating to angular radiation sensitivity has revealed the importance of SEMU and Multi Bit Upset (MBU) tolerance for SRAM cells. The research focuses on improving SEMU tolerance of CMOS SRAM cells by using novel circuit and layout level techniques. A novel SRAM cell circuit & layout technique is proposed to improve the SEMU tolerance of 6T SRAM cells with decreasing feature size, making it an ideal candidate for future technologies. The layout is based on strategically positioning diffusion nodes in such a way as to provide charge cancellation among nodes during SEMU radiation strikes, instead of charge build-up. The new design & layout technique can improve the SEMU tolerance levels by up to 20 times without sacrificing on area overhead and hence is suitable for high density SRAM designs in commercial applications. Finally, laser testing of SRAM based configuration memory of a Xilinx Virtex-5 FPGA is performed to analyze the behavior of SRAM based systems towards radiation strikes.

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ABBREVIATION

ASIC - Application Specific Integrated Circuit

BRAM - Block RAM

CLB - Configurable Logic Block

CMOS - Complementary Metal Oxide Semiconductor

DICE - Dual Interlocked Storage Cell

DRAM - Dynamic Random Access Memory

DRC - Design Rule Check

DSP - Digital Signal Processing

DUT - Device under Test

FPGA - Field Programmable Gate Array

FF - Flip Flop

GDSII - Graphic Database System 2 format

GUI - Graphical User Interface

H_SNM - Hold Noise Margin

IC - Integrated Circuit

IR - Infra Red

ITRS - International Technology Roadmap for Semiconductors

JTAG - Joint Test Access Group

LEAP - Layout Error Aware Position of transistors

LED - Light Emitting Diode

LET - Linear Energy Transfer

LSB - Least Significant Bit

LVS - Layout versus Schematic

MBU - Multi Bit Upset

MeV - Mega Electron Volt

MSB - Most Significant Bit

NMOS - N type Metal Oxide Semiconductor

OPA - Optical Parametric Amplifiers

OTP - One Time Programmable

PBE - Parasitic Bipolar Amplification Effect

PMOS - P type Metal Oxide Semiconductor

RCI - Robust Chip Inc

RHBD - Radiation Hardening By Design

RTL - Register Transfer Level

R_SNM- Read Noise Margin

SBU - Single Bit Upset

SEU - Single Event Upset

SET- Single Event Transient

SEE - Single Event Effect

SEFI - Single Event Functional Interrupt

SEMU - Single Event Multiple-node Upset

SOC - System on Chip

SOI - Silicon on Insulator

SPA - Single Photon Absorption

SPICE - Simulation Program with Integrated Circuit Emphasis

SNM - Signal to Noise Margin

SRAM - Static Random Access Memory

STI - Shallow Trench Isolation

TCAD - Technology Computer Aided Design

TPA - Two Photon Absorption

VHDL - Very High Speed Hardware Description Language

VIO - Virtual Input Output

VLSI - Very Large Scale Integration

W_SNM - Write Noise Margin

CHAPTER 1

INTRODUCTION

1.1 Background

Today's commercial and wireless industries are demanding high performance, ultra-low power Application-Specific Integrated Circuits (ASIC) and System on Chips (SOCs) for implementing their future products. They are driving the integrated circuit (IC) industry to fabricate ICs with denser architectures capable of better performance. IC reliability capable for long-term operations is an important factor that decides the quality of the commercial products, and radiation tolerance plays a big role in it. Before the 1970's, the effects of radiation events on ICs were considered only in mission critical applications for space and military projects, where the reliability of the system was more important than area minimization and speed requirements, that are demanded by commercial applications. During the 1980's, several reports were published showing evidence of radiation strike effects on commercial VLSI circuits in terrestrial environment. The single event effects (SEE) on VLSI circuits in terrestrial environment were initially published by woods et al. in 1979 [35]. In his investigations, the effects of alpha particles in DRAM cells were considered, where the single event phenomenon was treated as a physical problem that corrupted the memory cell, rather than a statistical problem like noise. Hence the suggestion was to incorporate memory design related changes to deal with the problem rather than implementing noise reduction

techniques [35]. Currently, the reliability issues due to radiation effects are considered to be larger than all of the other semiconductor reliability problems such as hot-carrier injection and electromigration [36].

Radiation effects on semiconductors are generally classified into two categories, hard errors and soft errors. Hard errors occur when high energy irradiation particles strike the material to change the chemical lattice configuration of the semiconductor material. This creates a permanent fault in the VLSI circuit which cannot be repaired. Hard errors occur commonly on VLSI chips used in space applications where radiation environments are harsh. Soft errors, on the other hand, are temporary errors which don't change the chemical configuration of the semiconductor material. Typical soft error effects involve ion particle - semiconductor interactions that result in charge deposition in the semiconductor material. Ideally, soft error upsets can be restored by resetting the power. The resetting process leads to draining away of the ion-deposited charge during the disconnection of power. The thesis focuses on soft errors and its mitigation.

Radiation events on digital systems can affect both combinatorial and sequential systems. However, the effect on sequential systems such as memories and flip flops are considered to be more severe since these errors are stored in the memory and hence persist for a longer period of time. Single event transients (SET) generated in the combinational circuits are considered hazardous only if they propagate into the storage circuits, resulting in the storage and propagation of error data.

1.2 <u>Motivation</u>

Static Random Access Memories (SRAM) occupy a large portion of the total chip area in the modern processors and SOCs. According to the ITRS road map, it is predicted that the SRAMs

will occupy up to 80 % of the total area in SOC chips by 2014 [26]. However, SRAMs are often the most sensitive blocks to radiation strikes, where the ions can easily deposit charge on the storage node of these memory cells, corrupting the data stored in them. The errors then will be stored in the memory, unless they are identified and rewritten with the correct data. Hence upsets in memories are considered more critical than the ephemeral single event transients occurring in combinational circuits.

SRAM blocks are commonly used as cache memories in processors because of their high-speed performance compared to Dynamic Random Access Memories (DRAM). SRAMs have a direct impact on the processor performance and therefore its radiation tolerance should be considered with paramount importance. Other common applications of SRAMs are in the Field Programmable Gate Arrays (FPGA). The SRAM based FPGA's have significant performance improvement and re-configurability options compared to the one time programmable (OTP) FPGA's which are based on anti-fuse technology. However, from the reliability perspective, single event upset on SRAMs and their impact on the FPGA operations have to be considered.

The criticality of an SRAM upset is decided based on its effect on the FPGA functionality. A SRAM upset can result in various impacts on the FPGA performance, from negligible output variations, to critical disruption of FPGA functionality. Single Event Functional Interrupt (SEFI) in SRAM-based FPGA is a good example of the detrimental effects of the SRAM single event upset (SEU). SRAM configuration memories are the fundamental blocks that store the configuration and interconnection data of all the functional units within the FPGA. An SEFI configuration bit error has the potential to alter the functionality of the FPGA by corrupting the data stored in the memory, which can lead to the complete disruption of the functional block

associated with that configuration bit. Several studies have been conducted, to observe this phenomenon, by upsetting the FPGA with protons and heavy ion particles [30].

Soft errors on SRAM cells are generally classified into two types. There are single-bit upsets (SBU) and multi-bit upsets (MBU) depending on the number of bits upset due to the single-ion strike. The soft errors are also classified based on the number of nodes the single-ion hits to create an upset in an SRAM cell. There can be a single-ion single-node upset or a single-ion multi-node upset depending on the number of nodes hit in a single cell. Single-ion multi-node upset occurs when ions strike in grazing angles with respect to the IC's plane and is also called as single-event multi-node upset (SEMU).

The multi-bit upset rate in SRAM cells is increasing significantly compared to the single-bit upset rate [6]. Multi-bit upsets in memories depend on several factors such as the energy of the strike, circuit design, layout orientation and density of the cell. They also depend on the direction of the strike, where the number of bits affected by a single ion strike increase with the energy of the ion [29]. The percentage of multi-bit upsets to single-bit upsets was observed to be 1% for 65nm 6T SRAM in SOI technology [27] and 20% for 6T SRAM in 65nm bulk technology [28]. The MBU to SBU ratio has further increased during scaling from 65nm to 45nm [6]. In this study, it was shown that the double bit upsets, which increased during scaling, had a strong dependence on the layout of the cells.

There are 3 main approaches for mitigating soft errors in digital systems. They are

    a) System level approach,

    b) Circuit or layout level approach and,

    c) Device or manufacturing process level approach.

System level approach involves the introduction of error correction coding, bit interleaving [38-40] and triple module redundancy techniques into the SRAM array design. System level approaches can provide efficient mitigation on soft errors with minimum design changes, however the advantage comes at a price of large area overhead. Device and semiconductor level approaches involve mitigation by varying the structures and properties of the semiconductor devices. The cost could be huge since it involves changing the fabrication process. Circuit/ layout level approach uses circuit or layout techniques to mitigate single event effects, which is also called Radiation-Hardening-By-Design (RHBD). This technique involves introducing circuit/layout modifications such as redundancy to improve the SEU tolerance. RHBD techniques have been successful implemented in ASICs to mitigate soft errors [28]. Since RHBD approach does not involve in any process modifications, it has shown huge potential for mitigation of single and multi-bit upsets in SRAM designs without greatly sacrificing on performance or area [12, 28, 43].

1.3 <u>Research Focus & Objectives</u>

The focus of the thesis is to explore the single event characteristics of conventional SRAM cell structures and understand the mechanisms involved in the single event upset. Currently, high-density memory architectures implemented in bulk CMOS technologies have resulted in an increase of MBU upsets [28]. The single-node upset issues have been alleviated to a certain extent by fabricating circuits in SOI process technologies; however, SRAMs fabricated with SOI technologies also exhibit an increase in multi-bit upset rates, with scaling, for grazing angle ion strikes. The primary question to ask here is: how to come up with a RHBD design/layout technique that can reduce the MBU upsets in conventional SRAM designs without severe performance or area penalty.

The central aim of the thesis is to answer this question by introducing a circuit / layout structure that can improve the multi-bit upset tolerance, specifically single-event multiple-node upset tolerance in conventional 6 Transistor (6T) SRAM cells. In order to evaluate the radiation tolerance, the proposed 12T SRAM cell is compared with conventional 6T cell design under several SEMU upset scenarios. A quantitative evaluation of the proposed 12T cell is performed to demonstrate the effectiveness of the achieved multi-bit upset mitigation.

SEU characteristics of SRAMs can be studied by evaluating SRAM based FPGAs, which can give insight into the SEU mechanisms involved during an upset. The radiation tolerance of the FPGA strongly depends on the SRAM blocks used to store the configuration data of the FPGA. Virtex-5 FPGA is an SRAM based FPGA which is used in a wide variety of commercial applications. The FPGA consist of SRAM based configuration memory blocks, which are spread all over the chip area, along with other dedicated functional blocks such as DSP48E, BRAMs etc. Therefore, it is an excellent platform that can help to understand the single event effect (SEE) characteristics of SRAM cells.

The main research objectives of the thesis are

1. Propose a new layout technique that provides better SEMU mitigation

2. Propose a new SRAM design that can utilize this layout technique

3. Understand and evaluate the SEU error cross section of SRAM based configuration memories in Virtex-5 FPGA by using a TPA laser.

1.4 Thesis Overview

The rest of the thesis is organized as follows. In Chapter 2, a background about SEE is provided along with the effects of SEE and SEMU and the techniques used to mitigate them in current CMOS SRAM technologies. The novel layout technique and the 12T SRAM cell are proposed, with the principle of operations explained in Chapter 3. Several SEMU radiation strike scenarios are discussed in details to explain the mechanisms involved in SEMU reduction during grazing angle strikes. Chapter 3 also consists of preliminary schematic level simulation results such as critical charge analysis and signal to noise analysis for evaluation of single event upset characteristics of the proposed cell and 6T cell. Chapter 4 discusses the 3D mixed mode simulation methodology and post processing techniques done using Accuro tools. Chapter 5 discusses the 3D mixed mode simulation results of 6T and the proposed 12T cell using Accuro [12]. The sensitivity map and error cross section curves are plotted to quantitatively compare the effects of radiation strikes in 3 major strike directions (X, Y and Z). Chapter 6 introduces laser testing methodology used for SEE evaluation of Virtex-5 FPGA, followed by the laser testing results of configuration memories in Xilinx Virtex-5 FPGA. Other functional blocks such as CLB blocks, DSP slices and BRAM's in the FPGA are also tested for SEE upsets. Chapter 7 gives the conclusion of the thesis and the future research work that can be done for improvement.

Chapter 2

OVERVIEW

2.1 Radiation Problems in Terrestrial Environment

During the past decades, radiation hardening research was mainly focused on space applications, where various techniques based on redundancy were implemented to mitigate single event effects in electronics [31]. But recently, commercial ICs in the terrestrial environment are also getting affected by radiation events due to low-energy neutrons from space and secondary alpha particle emissions [1]. Nuclear interaction of cosmic rays on boron phosphate silicate glass (BPSG) present in the packaging material demonstrates this effect of secondary emissions on commercial IC reliability. The low-energy neutrons present in the cosmic rays can hit the boron atom to produce secondary alpha particle emission that leads to the upset of SRAM cells [14].

There are 3 major types of radiation sources in the earth's terrestrial environment that can cause single event upsets in SRAM cells. They are a) alpha particles, b) high energy cosmic rays, c) low energy cosmic rays. Alpha particles consist of a helium ion with 2 neutrons and two protons. It is very difficult for an alpha particle to directly strike the silicon from outside the chip because of their rapid loss in energy while propagating through the material [1]. Radiation strike energy is measured in terms of energy lost per unit length in the material called Linear Energy Transfer (LET, MeV-cm^2/mg). A typical 10 MeV-cm^2/mg alpha particle can propagate only 100 μm in

the silicon material before its energy is lost [1]. Therefore, external alpha radiations don't pose a serious threat to ICs. However the secondary alpha emissions from impurities present in packaging material and device material within the chip, pose a serious threat due to its proximity towards the diffusion regions of the SRAM circuit. The most common source of alpha particles is from ^{238}U, ^{235}U, ^{232}Th impurities present inside the chip. In order to mitigate the secondary generation of alpha particle radiations within the chip, manufacturers are using techniques that remove the impurities during the fabrication process. Additionally, design techniques are also incorporated to spatially separate the potential alpha radiation sources from the sensitive nodes of the circuits.

High energy cosmic rays are the second source of irradiation particles in terrestrial environment. These radiation particles react with the earth's atmosphere to create secondary and tertiary radiations. The secondary radiation particles created include muons, protons and neutrons, from which neutrons are the particles with the highest flux and LET energy. Neutrons have more potential to cause MBU and SEMU radiation upset compared to alpha radiation strikes due to its ability to propagate greater distances without energy loss. They are also capable of depositing higher charge per unit length compared to alpha particles [14]. Unlike alpha particle mitigation approaches, neutron radiation effects cannot be mitigated by removing impurities in packaging materials because of its direct charge deposition nature in the silicon [37]. Hence new RHBD based SRAM cells has to be proposed to address this issue.

Finally the 3rd significant source of radiation is the low energy cosmic rays consisting of neutrons ($<$ 1 MeV-cm^2/mg). BPSG material used in packaging of ICs reacts with the cosmic rays to introduce potential single event particles [1]. The nuclear reaction process involves the generation of secondary particles such as alpha and Li recoil that deposit charge on the semiconductor devices creating upsets. This problem is mitigated to a certain extent by using packaging dielectric

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materials without BPSG in it. Introduction of the new packaging material has significantly improved the single event reliability of the ICs fabricated by current advanced manufacturing processes.

2.2 Effects of Scaling on SRAM Radiation Tolerance

The old era CMOS technologies used for commercial IC fabrications were inherently robust to radiations events because of their larger diffusion node sizes. The dimensions of the diffusion nodes were relatively large so that radiation strikes couldn't accumulate enough charge to upset the cells. But with dimension scaling, the charge used by the circuit to hold its data has shrunk to an extent that even a low energy ion strike can induce sufficient charge in the circuit to corrupt the data stored in the SRAM cell. Moore's law trend in VLSI scaling is the main factors for this degradation in radiation tolerance. According to Moore's law, the number of transistors doubles every 18 months. This trend has led to a rapid reduction in circuit dimensions, but at the same time has led to a drastic reduction in single event tolerance of the SRAM cell. The implications of this trend are as follows:

a) The circuit node size is reducing rapidly with each technology generation, leading to a reduction in the diffusion node capacitance of the transistor,

b) The operating voltage of the transistor is decreased to reduce power consumption and maintain constant electric field scaling.

The effect of decrease in node capacitance and operating voltage with scaling has been well documented in the publication by Lloyd et al. [2]. The Figure 2.1 shows the decrease in capacitance and voltage of circuit nodes with technology scaling. The SRAM cell's ability to hold its data, while getting affected by radiation, is evaluated by measuring the critical charge of the affected

node. Critical charge is the minimum amount of charge injected at a circuit node before it triggers an upset [5]. This critical parameter of the node directly depends on the node capacitance and the operating voltage of the SRAM cell. Hence, the reduction in capacitance and operating voltage will reduce the critical charge and thereby decrease the single event tolerance of the CMOS SRAM circuit.
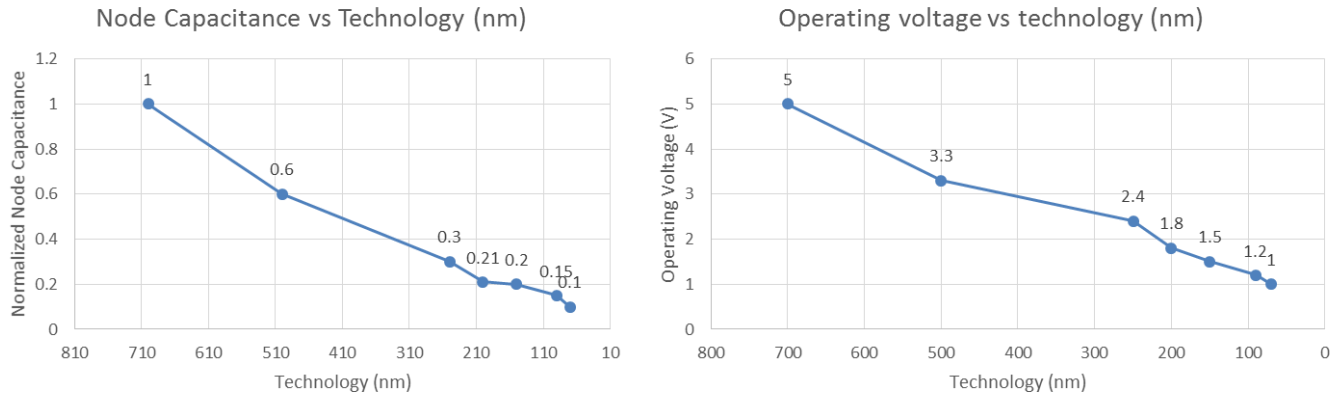
Figure 2.1: Decrease in normalized capacitance and operating voltage with technology scaling [2]

Secondly, scaling has resulted in the fabrication of high density VLSI architectures that has led to the decrease of spatial separation between nodes. This is an advantage for commercial ICs because it can hold more transistors in the same area, but from the radiation tolerance perspective, it has led to several reliability issues. When nodal spacing decreases, the ions have a wider solid angle window for potential single event multiple upset (SEMU) [2]. SEMU is an upset that occurs due to a single ion striking multiple-nodes in the SRAM cell. The effect is more common for ion particle strikes occurring at grazing angles with respect to the layout plane. SEMU phenomenon in SRAMs was demonstrated in a study by Hiedel et al. [6], where the cross sections of the 6T SRAM cell were compared for 2 different data storage patterns such as blanket and checkerboard patterns. In the blanket pattern, the location of the sensitive nodes were so close that a wide solid angle window between the NMOS nodes of the SRAM cell allowed for ions to strike multiple

sensitive nodes of the cell at grazing angles. The effect was significantly low in checker board pattern due to larger spatial separation of sensitive nodes. As the sensitive nodes get closer, the solid angle window for a potential SEMU gets widen. This rapidly increased the probability of an SEMU upset on the SRAM cells. The solid angle widening effect is demonstrated in the Figure 2.2.
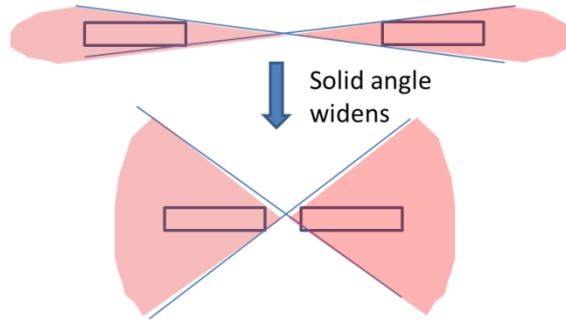
Figure 2.2: Widening of solid angle when nodes get closer during technology scaling

SEMU strikes can upset a cell with less ion energy compared with a single-node strike. This phenomenon can be simulated using a 3D mixed mode simulation that couples the effects of the schematic and the layout of the VLSI circuits. Synopsis TCAD is the most commonly-used tool for mixed mode simulations, however, the computing time is extremely large in order to simulate circuit-level designs. Therefore the application of TCAD tools is often limited to transistor level simulations. Accuro tool by Robust Chip Incorporated [RCI] [12] is capable of simulating circuit level designs using less computational resources. The tool is also suitable for cross section evaluation and LET threshold prediction [4]. All the mixed mode simulation in this project was carried out with Accuro.

A 3D Accuro simulation of a standard 6T cell is performed to compare the effects of normal strike and an SEMU strike. Table 2.1 illustrates the LET threshold energies for different strike situations.

Table 2.1: LET threshold energy needed to induce a single event upset on an SRAM cell for various strike scenarios

Strike Characteristics	LET Threshold MeV-cm^2/mg
Strike on OFF NMOS Drain node	2.75
Strike on OFF PMOS Drain node	4.75
SEMU strike hitting both OFF NMOS and OFF PMOS nodes	0.6875
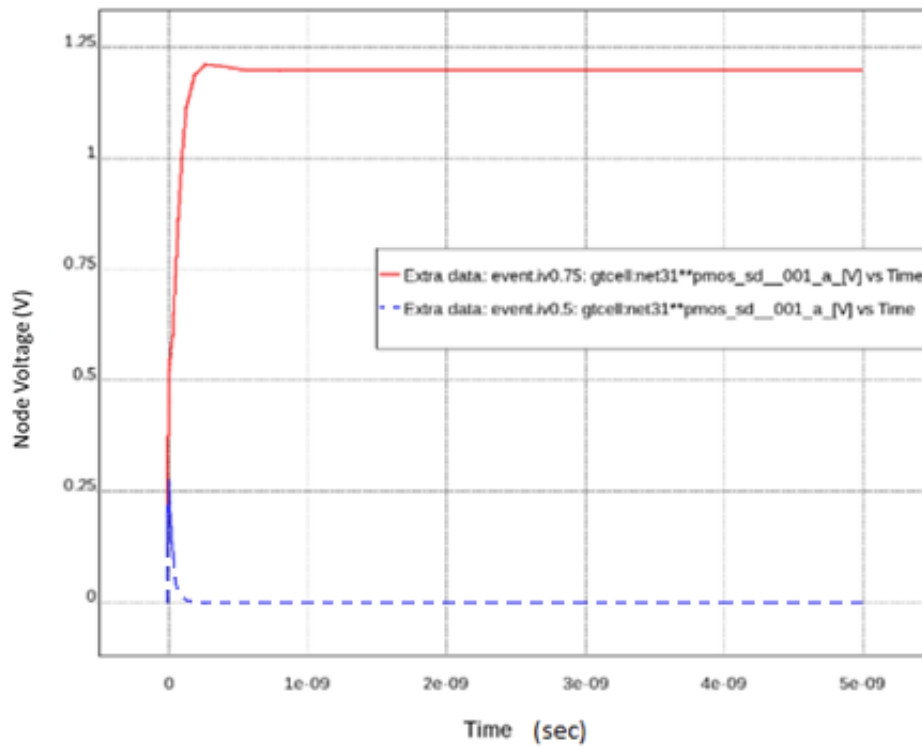
Figure 2.3a: Node voltage at PMOS Drain for SEMU strike for LET = 0.7 (red) and LET = 0.5 (dashed blue)
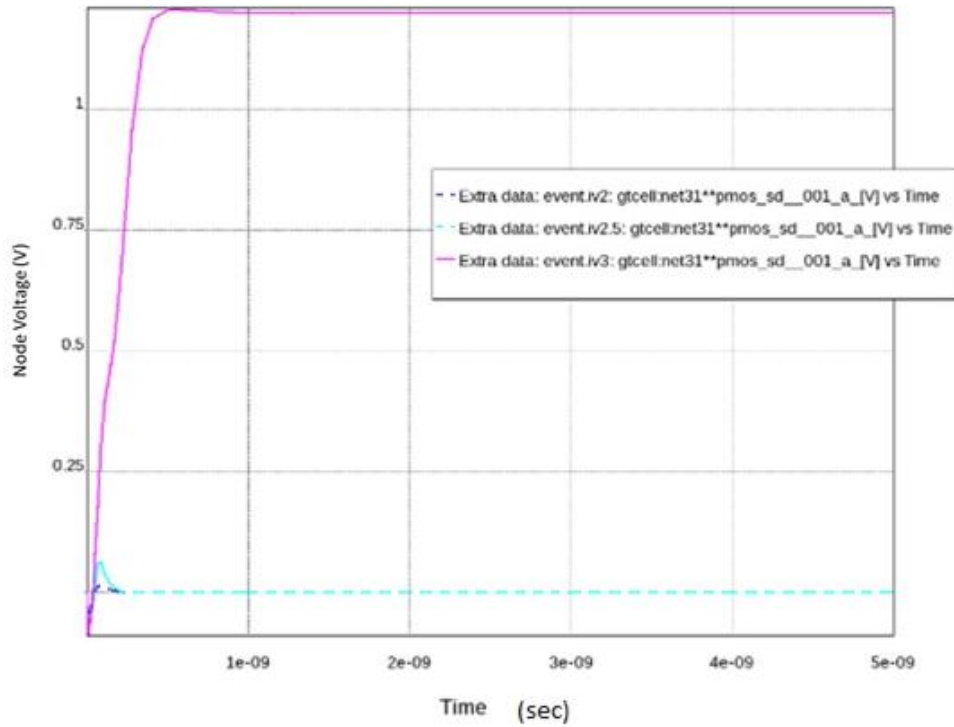
Figure 2.3b: Node voltage for a Normal NMOS strike for LET = 3 (pink) and LET = 2.5 (dashed blue).

From Table 2.1, Figure 2.3a and 2.3b, it is noted that the SEMU strike needs only ¼th the energy of a normal NMOS strike and $1/7^{th}$ the energy of a PMOS strike to corrupt the data stored in the cell. Therefore SEMU's should be considered more problematic than a single event single-node upset. This single event vulnerability towards SEMU strikes will significantly deteriorate the overall radiation tolerance of the circuit. Therefore, novel circuit and layout techniques need to be introduced to improve SEMU radiation tolerance of SRAM cells.

2.3 Physics of Single Event Upsets in SRAM Cells

Charge deposition in semiconductor devices can occur due to direct ionization or ionization by secondary particles. During ionization, the ion passes though the semiconductor particle releasing electrons and holes, decreasing its energy during its travel path. The amount of energy lost per unit length is measured in terms of LET. This energy is normalized with respect to the density of the

material and so the LET energy measured can be considered independent of the semiconductor material. For silicon, LET of 97 MeV-cm^2/mg corresponds to 1pC / μm [2].

Charge collection mechanism in semiconductors can be explained with an example of a radiation strike on the Drain of the OFF transistor. The reverse biased P/N junction formed by the Drain and substrate of the transistors is the location where the circuit is most sensitive to radiation. Under reverse-bias condition, the depletion region gets wider due to a higher electric field across the Drain-substrate junction, enabling the junction to collect more minority charge carriers from the surrounding areas.
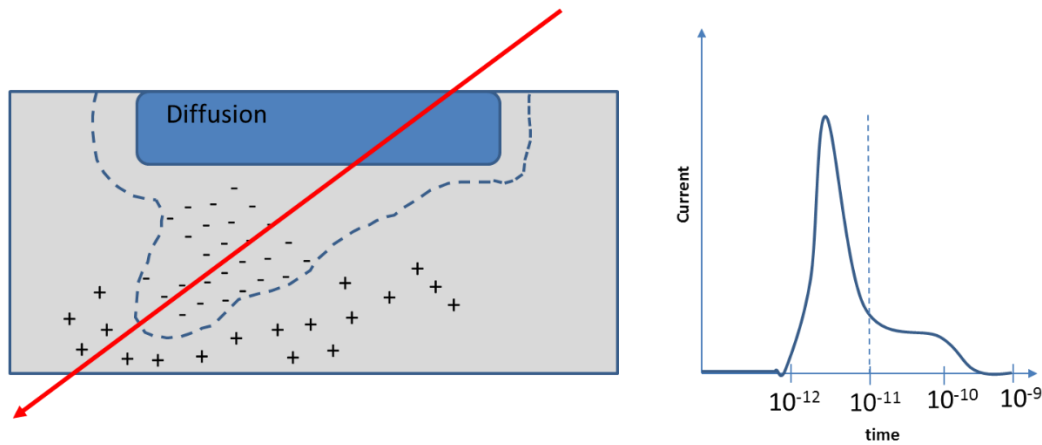
Figure 2.4a: Funneling of depletion region to gather minority carriers. b) (Right) Current at the Drain during a single event strike [1].

During a single event strike at the Drain node, the ion leaves a trail of electrons and holes along its strike path, forcing the depletion region to extend itself along the ion strike path in the shape of a funnel as shown in figure 2.4a (left). The funnel, then collects all of the deposited minority carriers in the substrate through drift mechanism, which results in the sharp increase of charge accumulation in the junction. After all the minority carriers are absorbed, the majority carriers diffuse into the depletion junction. This is a slow diffusion process resulting in the decrease in

charge at the junction as shown in waveform in Figure 2.4 (right). This is the basic physics of single event upsetting in semiconductor circuits. These concepts can be used to explain the single event upset process of 6T SRAM cells.
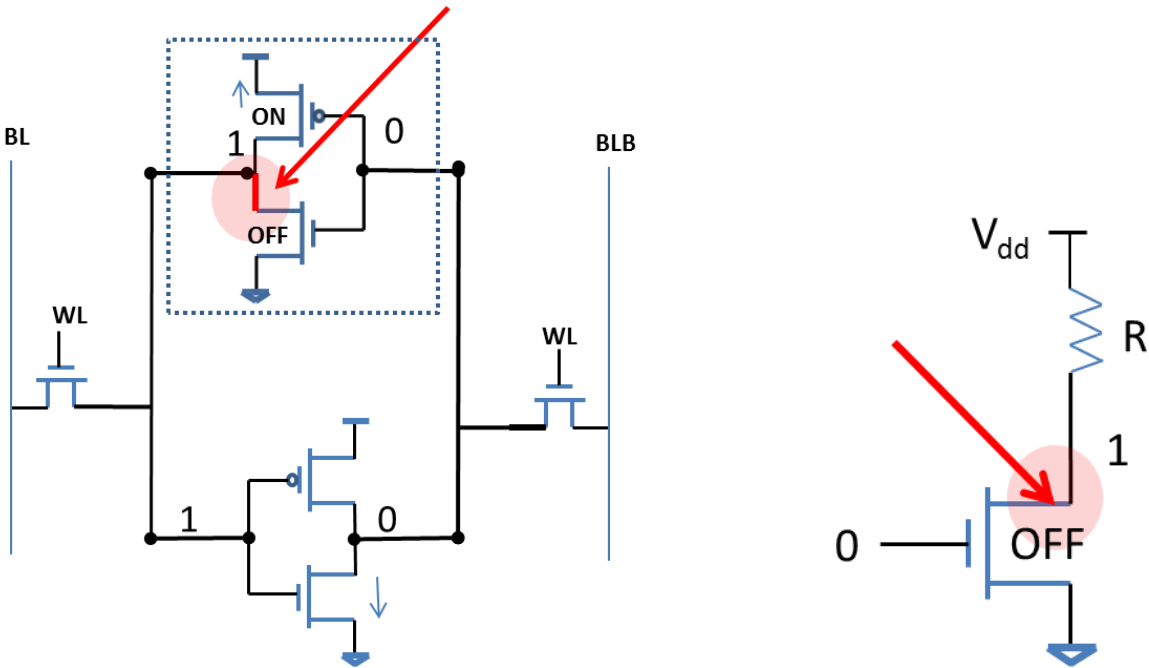
Figure 2.5: a) Radiation strike on a 6T SRAM cell Drain node(red) b) Equivalent inverter circuit with PMOS transistor replace by an equivalent resistance.

Consider the inverter part of a 6T SRAM cell as shown in Figure 2.5a, one of the transistors (NMOS) will be OFF and the complementary transistor (PMOS) will be ON. When the ion strikes the OFF transistor Drain node (NMOS), charge builds up at the depletion junction of the Drain region. This will force the ON complementary transistor (PMOS) to function as a restoring transistor by supplying a transient current to compensate for the charge build up at the Drain junction. The transient current flow results in a voltage drop across the restoring transistor because of its fixed trans-conductance across the source Drain path. The equivalent circuit of the inverter with the PMOS replaced by a fixed trans-conductance is as shown in Figure 2.5b. This voltage drop at the output of the inverter is the source for the single event upset. If the pulse width is long enough, the SET pulse generated propagates to the input of the other inverter and changes its

output. If the SRAM cell is not able to recover itself from this single event upset before the SRAM feedback time, the data gets latched and the SRAM cell gets corrupted.

2.4 <u>Laser Fault Injection Techniques for SEU Tolerance Evaluation</u>

Several methods are available to experimentally evaluate single event tolerance of SRAM cells. The common techniques involves accelerated heavy ions and protons/nuetrons testing using particle irradiation facilities. However, the access to test facilities needed for the SEU tolerance evaluations are expensive and difficult to obtain. Pulsed lasers offer an easy and convenient solution for evaluating SEEs in SRAM cells.

Based on the carrier excitation technique in the semiconductor material, pulsed lasers can be classified into single photon absorption and two photon absorption lasers. The classification is based on the number of photons used by the atoms in the material to reach its excited state. Single photon absorption (SPA) technique uses a single photon to create an electron-hole pair, but it has a major drawback. The laser must have a wavelength above the band gap energy of the semiconductor material (less than 1100nm). This results in a short penetration depth for SPA lasers because of the exponential loss of laser power while propagating through the silicon material. Therefore SPA lasers cannot be used to deposit charge deep in the substrate for single event studies. Two photon absorption (TPA) lasers eliminate this problem by using larger wavelength, at sub band gap energies deep into the material. The technique is based on simultaneous absorption of two photons to generate a single electron-hole pair in the incident region. TPA generates photons at high peak power within a duration of femtoseconds. The individual photons do not incur losses during its propagation through the material because its energy is in the sub band gap region. The collision of these photons results in the electron-hole pair generation at the location where the two

photons are focused. This enables the TPA laser to upset localized regions within the semiconductor material. This can be considered as a huge advantage because it allows to introduce charge through the back side of the IC (silicon side), thereby eliminating metal obstruction problems faced during IC front side testing.

2.5 <u>Existing 6T cell layout designs</u>

Layout for 6T SRAM cells has to be suitable for high density fabrication. The traditional 6T SRAM cells is as shown in Figure 2.6a. The layout is commonly used in fabrication of 6T SRAM designs in 130 and 90 nm technology. The layout design is mirrored and overlapped to create the larger 6T memory array. The main disadvantage of the traditional SRAM layout is that its lithographic unfriendly nature for SRAM fabrication below 90nm [24]. The bends in the diffusion and polysilicon limits the layout fabrication of this design below 90nm.

The thin cell was introduced to combat these disadvantages. As shown in Figure 2.6b, the layout limits the use of polysilicon only in the horizontal direction and the diffusion in the vertical direction without any bends. The layout also removes diffusion bends, which makes them more layout friendly for advanced fabrication technologies below 90nm.
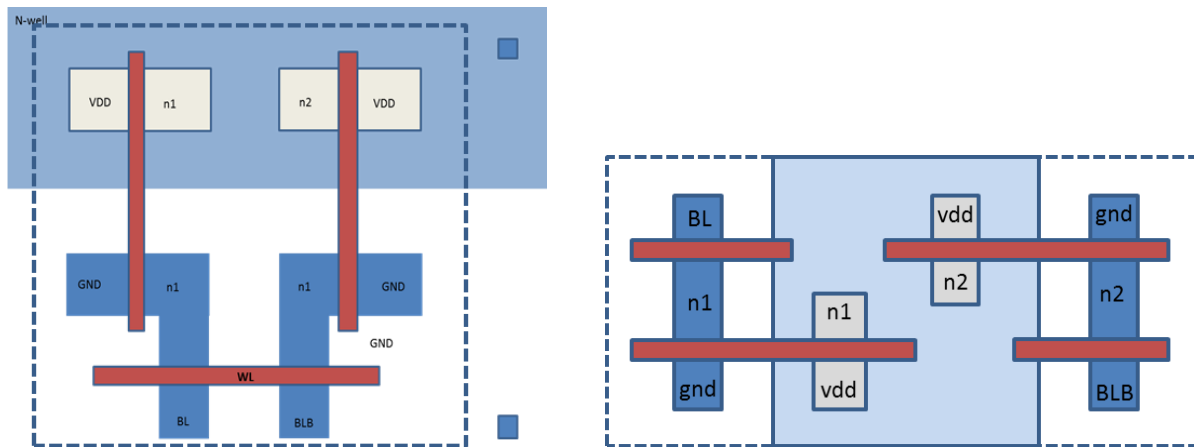
Figure 2.6 a) Traditional 6T SRAM cell b) Thin cell layout of 6T cell

2.6 Current Layout Techniques for SEMU / MBU Mitigation & their Limitation

SEMU events may be triggered by 2 mechanisms. The direct mechanism is a single ion directly hitting multiple sensitive nodes of the SRAM cell. This kind of SEMU upsets depends highly on the angle of the strike and the proximity of the strike to the sensitive node. An indirect mechanism of an SEMU upset involves an ion hitting a sensitive node and depositing enough charge on the substrate so that the sensitive node nearby shares this deposited charge from the strike node or the substrate. Studies regarding the effects of directional radiation strike on charge sharing demonstrate this mechanism for different CMOS technologies [18-20].

Several circuit / layout level techniques have been proposed to mitigate SEMU and MBU effects, such as increasing the separation of critical nodes to 5um [11], introducing redundancy in nodes [12], increasing the number of well contacts to avoids well collapse source injection[15]. This will be further explained in the next section. But all these spatial separation and redundancy techniques are susceptible to failures with device scaling. As per the investigation conducted by Bhuva et.al [16], the Dual Interlocked Storage cell (DICE) flip flop loses its radiation tolerance capabilities drastically with scaling. The DICE design shows 100 times better single event tolerance compared to regular D Flip flops in 65nm. However at 40 nm, this improvement has been reduced to 5X [16]. All the redundancy techniques depend on keeping the affected nodes as far away as possible from the sensitive node, but with device scaling these nodes get closer and charge sharing effect would trigger multi bit upsets [9]. Currently, the following circuit / layout level techniques are used to reduce SEMU effects

2.6.1 Placing Bit-lines between Sensitive Nodes

Bit-lines are used to store and retrieve data from the memory cells. The diffusion nodes of the bit-lines can be strategically placed between sensitive nodes to isolate them, thereby reducing the spreading and collection of charge across nodes. Daniele et al. [10] carried out an investigation on multi bit upset patterns formed in a 150nm SRAM array. It has been seen that the upset pattern signatures on the SRAM chip are more horizontal in nature than vertical (5:1 distribution). The reason provided for this distribution was that the charge collection and sharing between nodes in the horizontal direction was much easier because of the minimum distance between sensitive nodes. However, it was difficult to collect charge and share them vertically across nodes because of the presence of bit-line contacts in between them. Hence the placement of bit-lines between sensitive nodes may aid in reducing the charge sharing effect across sensitive nodes thereby reducing SEMU upsets.

2.6.2 Well / Substrate Tapping Scheme

Well and substrate taps play an important role in multi-bit-upsetting mechanism. For CMOS technologies, an ion strike can deposit charge in the well or substrate to locally collapse the body potential of the transistor [9]. This results in the upsetting of the Drain nodes of the transistors sharing the same substrate. Taps helps maintain the well / substrate potential by giving a good ohmic contact to the power supply and ground. Closer well and substrate tap contacts can help in maintaining the substrate potential by draining away the deposited charge in the well and substrate.

2.6.3 Placing Guard Bands

Placing guard bands between nodes reduce charge collection for low LET strikes, resulting in lowering of multi-bit charge accumulation [16]. Guard bands use the same diffusion material as

their well / substrate taps. Black et al. has investigated the effects of placing guard between PMOS devices and NMOS devices as shown in Figure 2.7 [16].
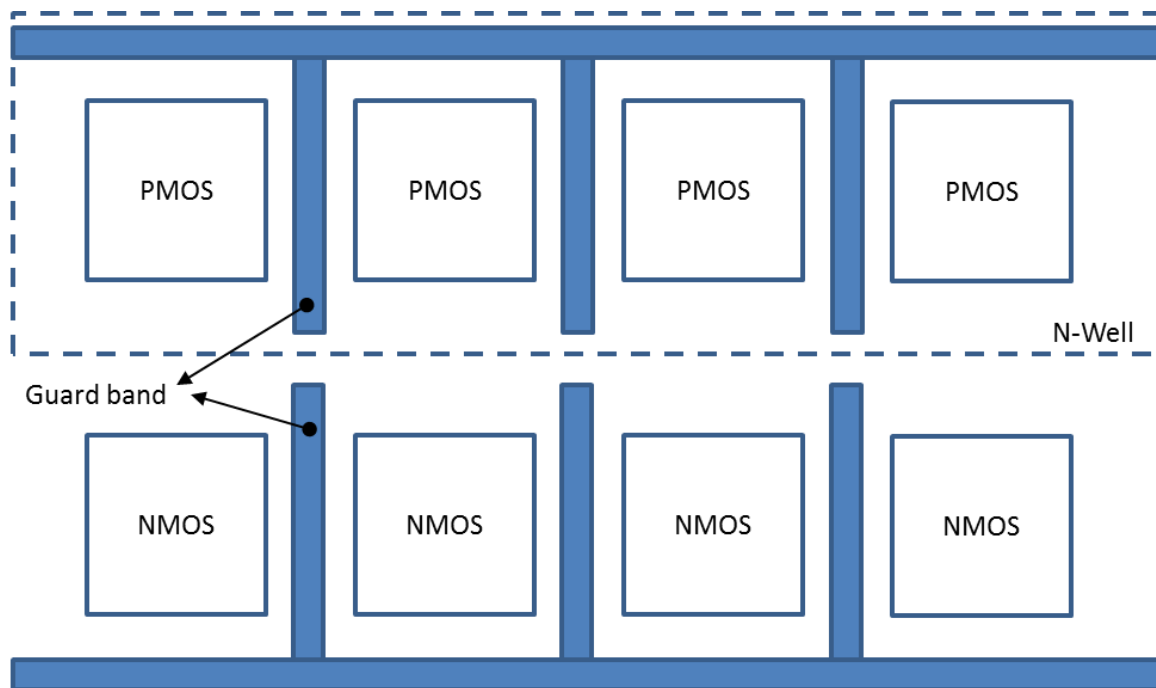
Figure 2.7: PMOS and NMOS devices separated by guard bands [16]

For direct Drain node hits, addition of guard band between PMOS transistors has reduced the charge collected to ½ the value compared to the designs without guard band [16]. For non-direct hits, guard bands offer even better isolation between Drain nodes by preventing spreading of charge through the N-well. However, this technique doesn't offer significant isolation for NMOS devices. This is due to the difference in charge collection mechanism of PMOS and NMOS transistors. Charge collection in PMOS transistors occurs mainly due to parasitic bipolar amplification effect (PBE). In this mechanism, the ion strike deposits charge in the well to drop the local well potential, resulting in switching ON of a parasitic transistor that injects current into the PMOS node [9]. Guard contacts prevent the parasitic transistors of PMOS from turning ON by maintaining the N-well potential. However, charge collection in NMOS transistors is due to charge

diffusion through the substrate and guard bands do not have significant effect on it. Another main drawback of this technique is the area penalty associated with the addition of guard bands between transistor nodes. Also, guard bands do not offer significant reduction of multiple-node charge collection at higher LETs.

2.6.4 Guard Diodes

Guard diodes provide isolation by reducing charge sharing in a way similar to guard bands, but the mechanism involved is different. Guard diodes have the same diffusion material type as the transistors they are guarding. They provide additional reverse biased junctions between nodes, which siphons away the deposited charge so that the amount of charge spread to the adjacent node will be reduced [18]. Guard diodes provide effective reduction in multi node charge sharing for NMOS devices but, the technique also suffers the same area overhead draw back faced by guard bands.

2.6.5 LEAP (Layout Error Aware Positioning of Transistors)

LEAP is by far the most effective technique used for SEMU mitigation. LEAP was proposed by Lee et al. in 2010[4]. The effectiveness of the technique was demonstrated using LEAP based DICE cells which showed an improvement of up to 5X times compared to the regular DICE cells.

The basic principle of the LEAP is to carefully position the NMOS and PMOS transistors in a way as to cancel out the effects of the charge deposition during multi-node strikes. Considering an example of an inverter circuit, during single event strikes at the Drain node of the NMOS transistor, a current is injected into the node, which creates a voltage drop across the PMOS transisitor, resulting in a negative voltage transient. Similarly, a current is generated out of the PMOS transistor Drain during an ion strike, which creates a voltage drop across NMOS transistor,

resulting in a positive transients in Drain node [2]. The OFF transistors Drain nodes are more sensitive to radiation strikes compared to the ON transistor, and hence they create larger transient spikes during upsets.

For an inverter circuit as shown in Figure 2.8, the PMOS and NMOS transistors Drain nodes are electrically connected together. A simultaneous strike on both these nodes will result in generation of a voltage transient of opposing nature. The right sizing of NMOS and PMOS transistor can optimally cancel out the transients generated. The same concept can be extended to a latch design which consists of 2 inverters connected back to back. In the latch layout, the inverters are arranged along a line so that a grazing angle strike hitting all four transistor nodes of the latch will result in cancellation of the charge developed.
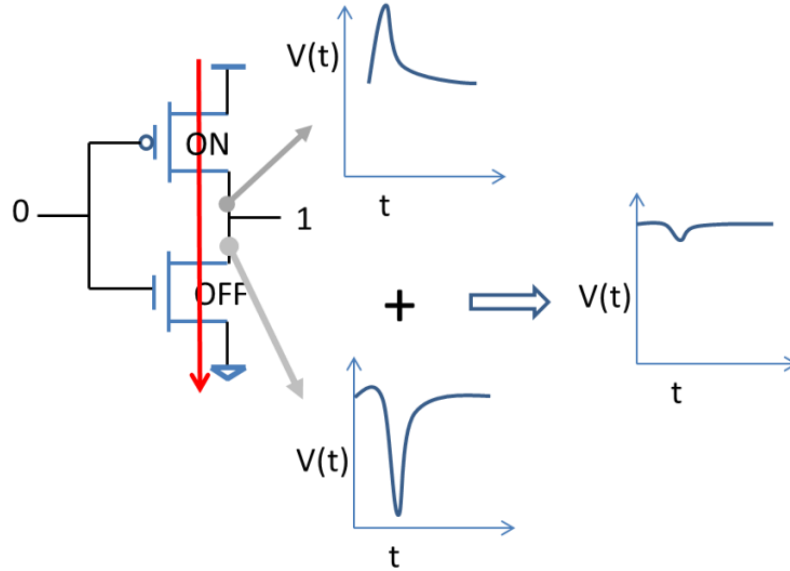
Figure 2.8: Charge cancellation in an inverter based on LEAP technique [4]

For optimum charge cancellation, NMOS and PMOS width should be sized to a particular ratio to achieve optimal effect. This ratio depends on the mobility of the charge carriers in PMOS and

NMOS transistors, which in turn are dependant on the CMOS manufacturing technology and semiconductor doping used.

Despite these advantages, LEAP technique has not been implemented for SRAM designs yet. 6T SRAM cells show high vulnerability to radiation strikes in grazing angles and LEAP technique would be an excellent tool to improve its SEMU Tolerance. The conventional 6T SRAM design is not suitable for implementation with LEAP because of its un-symmetrical layout across the horizontal axis of the layout plane. Hence a new layout of the 6T SRAM cell has to be proposed that can utilize the advantages of the LEAP technique. Additionally, the access transistors has to be considered while applying LEAP technique to SRAM design, since OFF access transistors can inject single event transients into the circuit during SEMU events.

Another factor to consider is the effect of the LEAP technique for CMOS technologies below 180nm. As the technology scales down, the PMOS to NMOS ratio needs to be changed due to the variation in mobility parameters of transistors. The PMOS / NMOS sizing ratio for the 130nm technology has to be investigated to completely utilize the potential of the LEAP technique in advanced CMOS technologies.

The main objective of the thesis is to introduce a novel layout technique that reduces the effects of SEMU in conventional 6T SRAM cells. The layout technique developed in 130nm technology, utilizes the advantages of the LEAP, strategic bit-line placement and guard contact placements to improve SEMU tolerance without introducing additional area penalty to the design. The effectiveness of the layout technique is demonstrated by proposing the 12T SRAM cell and comparing it with its 6T cell counterpart having the same diffusion and total layout area.

CHAPTER 3

PROPOSED LAYOUT TECHNIQUE AND SRAM DESIGN

Radiation tolerance of a 6T SRAM cell for a particular fabrication process depends on both the size of the diffusion area and charge collection efficiency. Generally as the width of the NMOS and PMOS transistors increases, the node capacitance of the transistor also increases, improving the single event transient (SET) tolerances. An alternative approach is to introduce redundancy of storage nodes with isolation in between them. Paralleling 6T cells is an effective technique for mitigating SEMU. The technique provides redundancy, introducing spatially separated transistors driving the same electrical node. Hence during an ion strike, only one of the transistor would likely get upset while the other remains safe, which will improve the single-node upset tolerance of the SRAM cell [1]. Additionally, the Drain nodes of the NMOS and PMOS transistors of the redundant chain can then be arranged on the layout in a particular way so that the charge accumulation at multiple-nodes created during an ion strike can partially or fully cancel out, provided the affected NMOS and PMOS Drain nodes are electrically connected to the same node. Finally, bit-lines can be effectively used for isolation of identical transistor nodes. The layout technique works on reducing the SEMU tolerance of designs that are symmetrical across horizontal and vertical axis of the layout plane. The proposed 12T cell was developed from conventional 6T cell based on this objective in mind. The technique greatly improves the SEMU tolerance of the 6T SRAM cell designs.

3.1 Proposed 12T SRAM Design

The 12T cell was derived from the standard 6T cell by splitting each transistor into 2 and spatially separating them in an interleaved fashion. During the layout translation, the total diffusion area and overall layout area of 12T cell is maintained the same as 6T cell for the purpose of fair comparison. The area overhead introduced by the transistor duplication process is overcome in the layout by sharing the diffusion nodes of identical transistors. The NMOS access transistors of the 6T cell are split into 2 complementary transistors which helps cancel out the transients generated during SEMU at the source. The NMOS and PMOS nodes in the layout are aligned in a particular order so that SEMU strike from vertical and horizontal directions along the layout plane, will lead to charge cancellation at the interconnected node. This greatly improves the SEMU tolerance of the 12T SRAM cell. The proposed 12 T cell is shown in Figure 3.1.

Figure 3.1: The schematic diagram of the proposed 12T cell

Additional layout technique was employed in such a way that bit-line (BL/BLB), power (vdd) and ground (gnd) diffusion nodes are placed in between the storage nodes. Figure 2.2 shows the layout of the 12T SRAM cell design. Here, the bit-line diffusion nodes can act as guard diodes [18] that
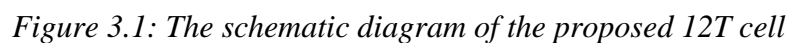
isolates the sensitive nodes from each other by minimizing the charge sharing effect between nodes having the same type of diffusion. Additionally, the interleaving method allows the transistors to be placed closer together.

The main layout based features of the proposed 12T cell is as follows.

a) The diffusion nodes of the same type are spatially separated. This improves the single-node upset tolerance by offering a dual redundancy way of protection, where if an ion passes through one node, it only deposits charge on that node, the other node is kept isolated from the affected area.

b) The NMOS and PMOS transistors are arranged such that SEMU strikes along the horizontal and vertical directions lead to charge cancellation at the nodes where they are electrically connected.

c) Placement of bit-line contacts between diffusion nodes tends to act as an isolation band between adjacent nodes.

The charge accumulation and compensation of Drain nodes depend on the NMOS and PMOS Drain width and angle of incidence of the ion beam. Proper sizing of drain width is needed for equal amount of charge collection and cancellation at NMOS and PMOS Drain nodes.

3.2 Proposed Layout
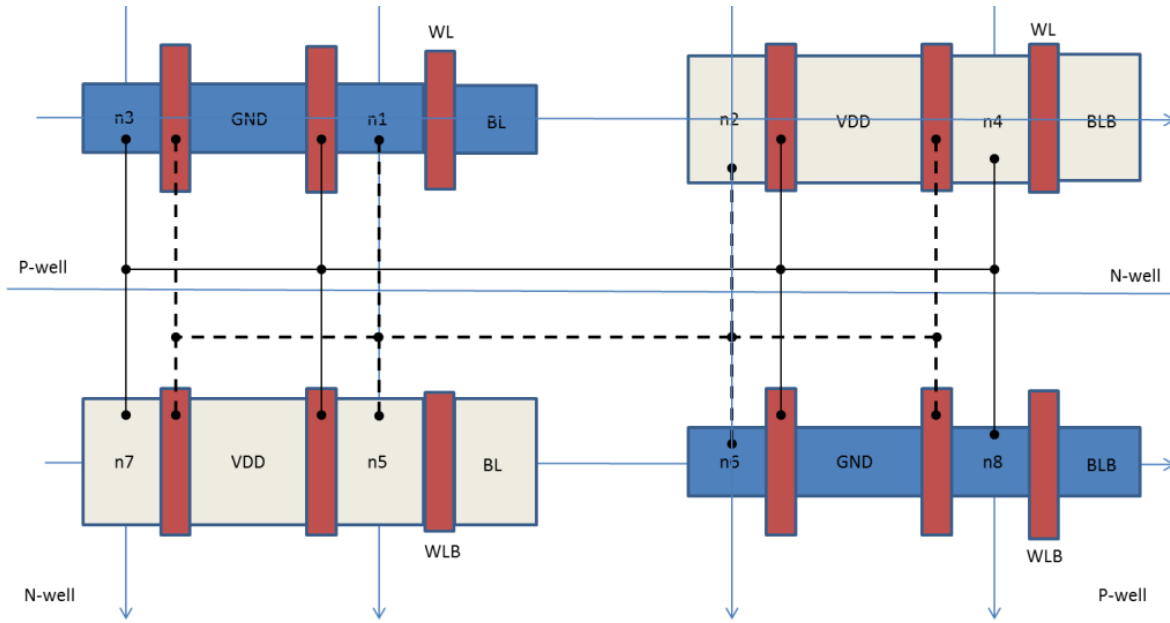
Figure 3.2 Layout of the proposed 12T SRAM cell

In order to explain the effectiveness of the layout in SEMU reduction, 2 major strike scenarios are illustrated as follows. SEMU strikes are considered in both vertical and horizontal direction along the layout plane. The conventions used for directional radiation strikes are as shown in Figure 3.3.
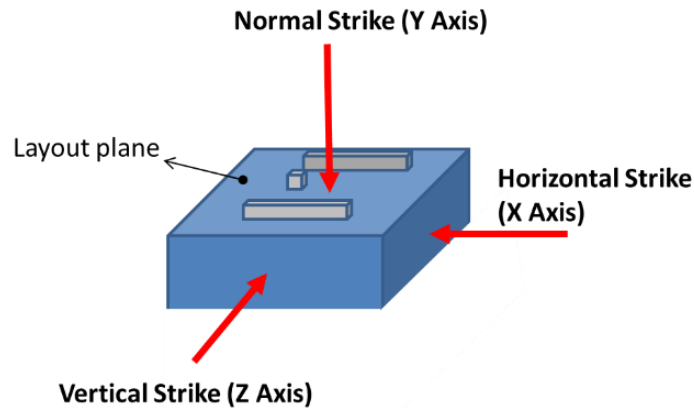
Figure 3.3: Illustration of 3 major radiation strike directions

3.3 <u>Mitigation Mechanism for SEMU Events</u>

a) Horizontal strike (0 deg elevation, 0 deg azimuth): Consider that the 12T SRAM cell is in state 0. This makes the nodes (n1, n2, n5, n6) connected to zero and the nodes (n3, n4, n7, n8) connected to 1. Under this condition, the sensitive nodes are the drain nodes of the OFF transistors which are n2, n6, n3, n7. During horizontal ion strikes along the layout plane, Nodes (n3, n1, n2, n4) or (n7, n6, n5, n8) are mostly affected. Considering top part of the layout in Figure 2.2, nodes n3 and n1 of NMOS, develops a negative voltage transient, which is compensated by the positive voltage built up at n4 and n2 of the PMOS transistors. In addition, striking n3 and n1 NMOS transistors (where n3 is high and n1 is low) will result in a generation of negative voltage transient at both Drain nodes. However, the generation of negative voltage at the non-sensitive Drain node (n1) will provide more negative bias voltage to the gate of the OFF sensitive NMOS transistor (n3 transistor), thereby preventing the sensitive transistor from flipping ON. Another way to induce an SEMU upset in the cell is to simultaneously hit nodes (n3, n2) or (n1, n4), but due to the geometry of the layout, n3 and n2 nodes can't be upset selectively without upsetting n2 and n4. This simultaneous hit of all 4 nodes also result in charge cancellation.

b) Vertical Strike (0 deg elevation, 90 deg azimuth): During vertical strikes, the following pairs of nodes are affected (n3, n7), (n6, n1), (n2, n5), (n4, n8). These are the Drain nodes of PMOS and NMOS transistors in the inverters. When an ion strikes these nodes, the PMOS transistor creates a positive voltage transient and the NMOS transistor creates a negative voltage transient. The charge developed is cancelled out because they are electrically connected to the same node.

3.4 Schematic Design and Simulations

3.4.1 Cadence Simulation & Virtuoso: Brief Description

Cadence simulations were performed in 130nm IBM technology. 2 different schematic simulations are performed, as a preliminary step, in evaluation of radiation tolerance. They are a) critical charge analysis b) signal to noise margins (SNM) analysis. Cadence composer and analog design environment are used for schematic design and testing of the schematic circuit designs. After the functional testing of the SRAM cell, the layouts are done using Virtuoso. Design rule check (DRC) and layout versus schematic (LVS) checks are done to make sure that the schematic and layout are equivalent and they obey all the layout design rules.

3.4.2 SRAM Design

6T cell Transistor sizing

PMOS pull up transistor W/L = 630nm / 130nm
Access transistor W/L = 630nm / 130nm
NMOS pull down transistor W/L = 630nm / 130nm

12 Cell Transistor sizing

PMOS pull up transistor W/L = 630nm / 130nm
NMOS pull down transistor W/L = 390nm / 130nm
Access transistor PMOS (W/L) = 630nm / 130nm
Access transistor NMOS (W/L) = 390nm /130nm

PMOS to NMOS ratio is chosen to be 1.6 for optimum charge cancellation during SEMU strikes. This ratio depends on the fabrication technology used and it can be found through a 3D mixed mode simulation of the 12T cell layout. The ratio (1.6) was obtained from Accuro simulations

done on 12T SRAM cell mesh model (Detailed explanations later). For 12T cell design, the width of the NMOS transistors are found first. The width of NMOS transistor is chosen as half the 6T cell NMOS transistor width. SEMU radiation strikes are then performed for different PMOS widths and the radiation characteristics are studied to find the optimum PMOS width.

3.4.3 Critical Charge Analysis

Critical charge is defined as the minimum amount of charge collected at a sensitive node that can cause the SRAM cell to upset. Critical charge at a node gives us an approximate idea about the radiation tolerance of the SRAM Cell. Upset occurs when the SRAM cells upset recovery time exceeds its feedback time [2]. The significant amount of charge deposited that results in the SRAM upset can be given as

$$Qsig = \int_0^T Id(t).\,dt\ldots\ldots[2]$$

Where Id = drain current

T = Tf, feedback time if cell upsets

Tr recovery time if the cell doesn't upset
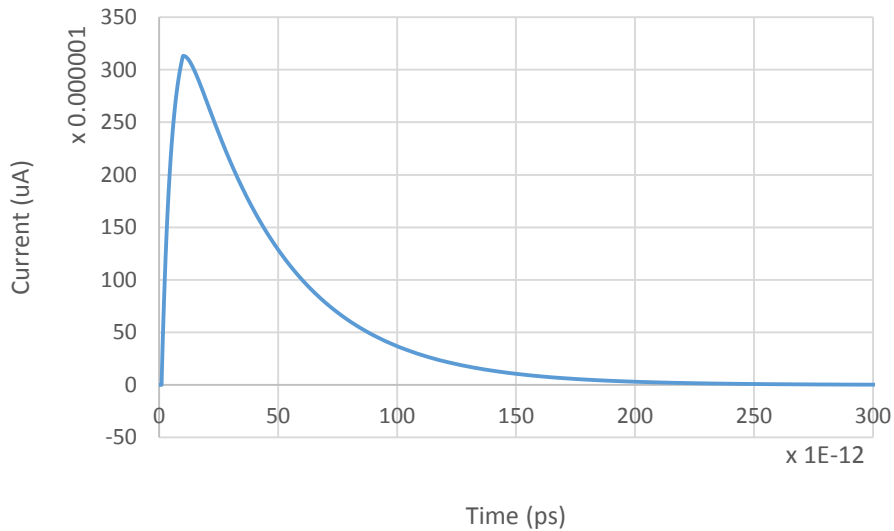
Figure 3.4: The current pulse waveform used for upset

31

Critical charge of a circuit is evaluated by injecting a current pulse into the sensitive node of the SRAM cell design. In the simulations, a current source with the double exponential characteristics, as shown in figure 3.4, is used to simulate a 1 to 0 and a 0 to 1 upset. The critical charge at the sensitive node is evaluated for both 6T and 12T SRAM cell

Pulse Characteristics

Rise time: 10ps

Fall time: 200ps

Pulse shape: double exponential

First, the sensitive node is identified and a current pulse is injected into this node. The magnitude of the pulse is initially set to a low value (10 uA) so that it would not upset the cell. The current magnitude is then gradually increased until the cell flips. The threshold current when the cell flips is identified and the current pulse is integrated to get the critical charge associated with the node. For 1 to 0 upset, the current source is connected between ground and the sensitive Drain node as shown in Figure 4.2. For 0 to 1 upset, the current source is connected between power supply (Vdd) and the sensitive Drain node [8]. After getting the upset transient waveforms for the cell flip, the current pulse is integrated from 0 to T, where T is the time at which the cell output flips (50ps). The time instant when the voltage at the sensitive node cross 50% of the power supply voltage is considered as the cell flip event. This is done to measure the actual charge that resulted in the single event upset rather than integrating the total charge collected at the node.

However, the schematic simulations is only a preliminary analysis, which gives an approximation of the SEU characteristics of the SRAM cell for an ion strikes directly on a single-node. The actual semiconductor effects of an ion strike, like charge sharing and well collapse, play a significant role

in the cell upsetting process. In order to understand these single event effects, A TCAD or Accuro simulation has to be performed.

6t cell Critical charge analysis: Test results

Critical charge (1-> 0) analyses: 6.89fC (225.7uA, 0 to 50ps. The SRAM is in hold condition)

Critical charge (0->1) analysis: 12.7fC (420.3uA, 0 to 50ps. The SRAM is in hold condition)

Proposed 12 T cell Critical Charge analysis: Test results

Critical charge (1-> 0) analyses: 12.3fC (406.7uA, 0 to 50ps. The SRAM is in hold condition)

Critical charge (0 -> 1) analysis: 17fC (563uA, 0 to 50ps. The SRAM is in hold condition)

Summary of critical charge analysis of SRAM cells

Table 3.1: Critical charge comparison of 6T and 12T cell.

Parameter	6T cell	Proposed 12T cell
Single-node upset		
1-> 0 upset	6.89 fC	12.3 fC
0 ->1 upset	12.7 fC	17 fC

From the schematic simulations we can observe that the 12T cell structure has got 5fC more critical node charge compared to 6t cell for both 0->1 and 1->0 upsets, even though the cell areas are the same (area calculations explained in chapter 6). This improvement in critical charge can increase the single-node radiation tolerance of 12T cell design compared to its 6T cell counterpart.

3.4.4 <u>SNM Analysis</u>

SEU sensitivity depends on the size and stability of the SRAM cell. The SRAM cell stability is decided based on signal to noise margins (SNM) of the SRAM cell. Better SNM margins for the cell will improve the stability of the cell during data storing and write/read operations, which will automatically improve the radiation tolerance of the cell.
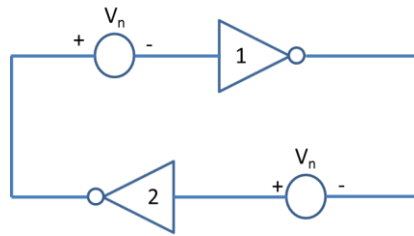
Figure 3.5: Block diagram for test setup for SNM noise margin analysis

As shown in Figure 3.5, an SRAM cell consist of inverter cells connected back to back in a loop to form a latch. For SNM analysis, an additional static noise source is inserted between the inverters. The static noise voltage of the noise source is then varied until the SRAM functionality is disrupted. The maximum noise voltage the cell can withstand without data corruption corresponds to its SNM margin. For SRAM cells, the SNM margin is evaluated for 3 different states of SRAM operation. They are

a) Hold state: The SRAM cell is in hold mode when data is not read / written into it. In this mode, the access transistors are switched OFF. The bit-lines are disconnected from the SRAM cell using the access transistor.

b) Read state: In this mode of operation, both bit-lines (BL and BLB) are pre charged to vdd (1.2V). The access transistors are then turned ON so that the SRAM cell is connected to the bit-lines for read operation.

c) Write state: In this mode, both the bit-lines are pre charged to either [1,0] or [0,1], depending on the data to be written into the SRAM cell. After pre-charging, the access transistors are turned ON to connect the bit-lines to the SRAM cell nodes.

The SNM simulation is done based on the evaluation technique proposed by Severick et.al [13] and Calhoun [21]. Based on this analytical method, additional circuit elements are added to the simulation setup to perform a coordinate transformation of the SNM plot by 45 degrees. This allows us to plot and visualize the SNM curve directly, and measure the actual SNM margin from the graph by looking at the maximum voltage difference of the eye diagram along the vertical axis. The circuit setup proposed by Severick et al. is as shown in Figure 3.6. Here the inverters INV1 and INV2 are connected to additional circuits as per the coordinate transformed equation (shown below the diagram of Figure 3.6). The voltage input u is swept from 0 to supply voltage (vdd) and the output voltages v1 and v2 obtained directly corresponds to the SNM eye diagram.
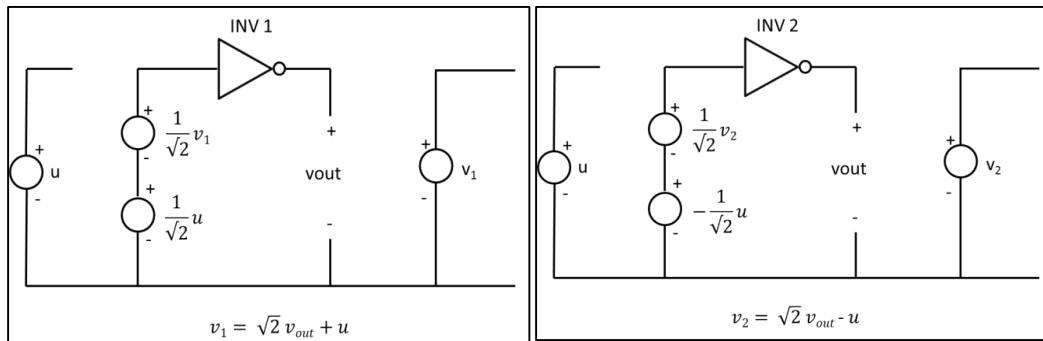
Figure 3.6: Schematic setup for SNM noise margin analysis based on method proposed by Severick [13]

The cadence SNM eye diagram for the 6T and proposed 12T cell are as shown in Figure 3.7 and 3.8 respectively. The SNM margin voltages are obtained from the diagram by measuring the maximum voltage difference within the eye. This maximum voltage is then scaled by $\sqrt{2}$ due to coordinate transformation requirement. The SNM margins for extracted from the Figures 3.7 and 3.8 are listed in Table 3.2.
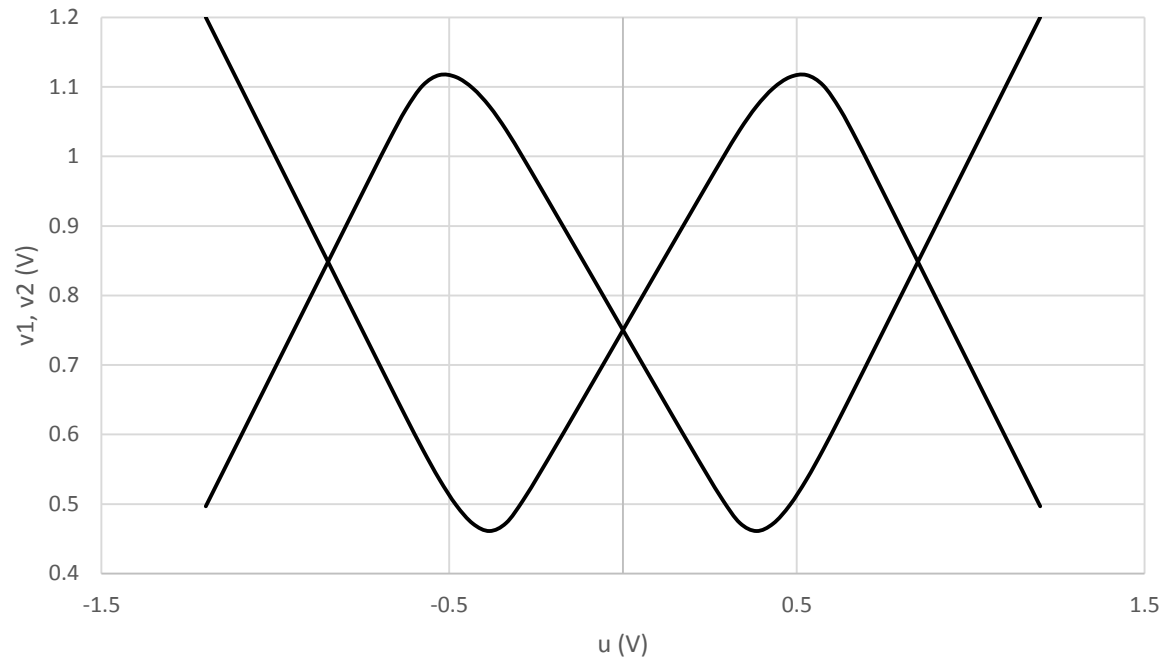
Figure 3.7a: 6T cell hold noise margin
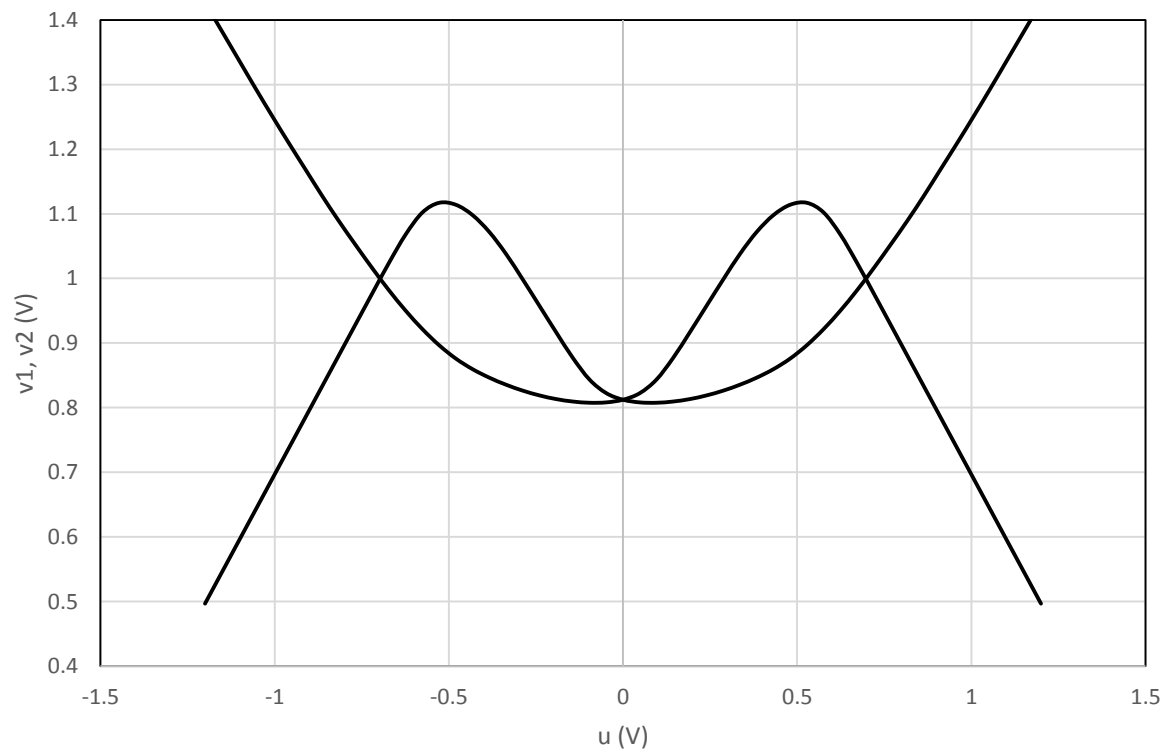
Figure 3.7b: 6T cell read noise margin
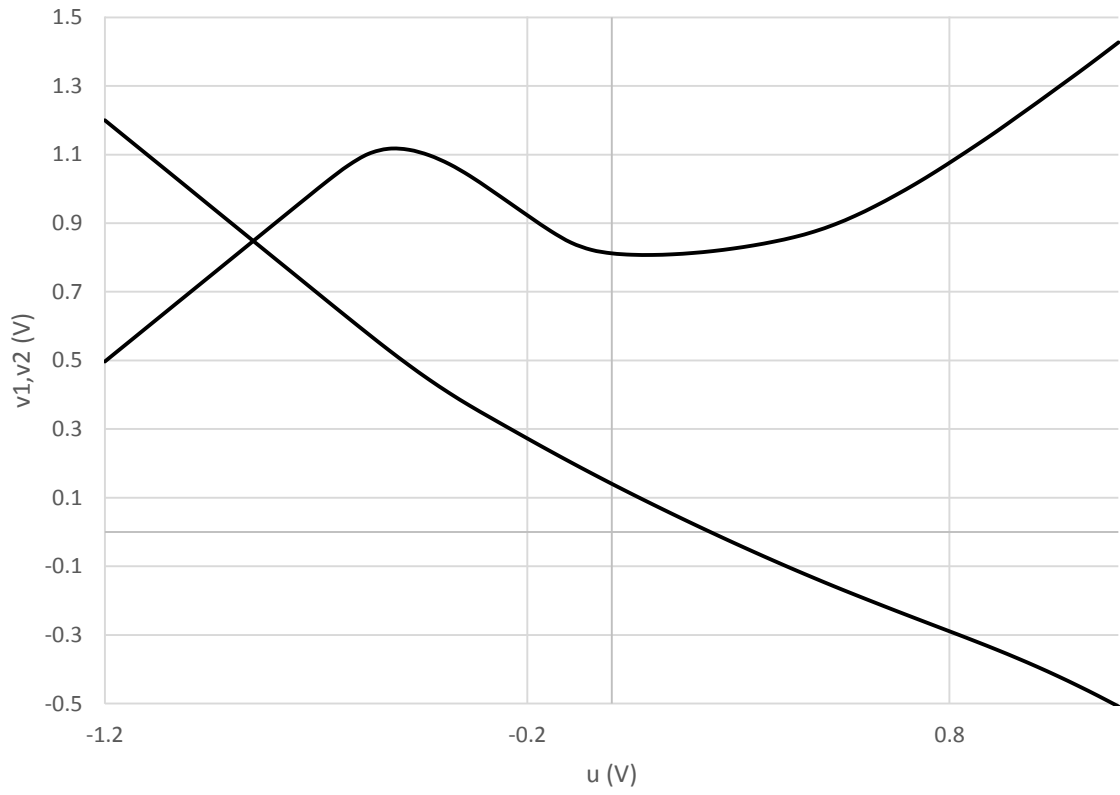
Figure 3.7c: 6T cell write noise margin
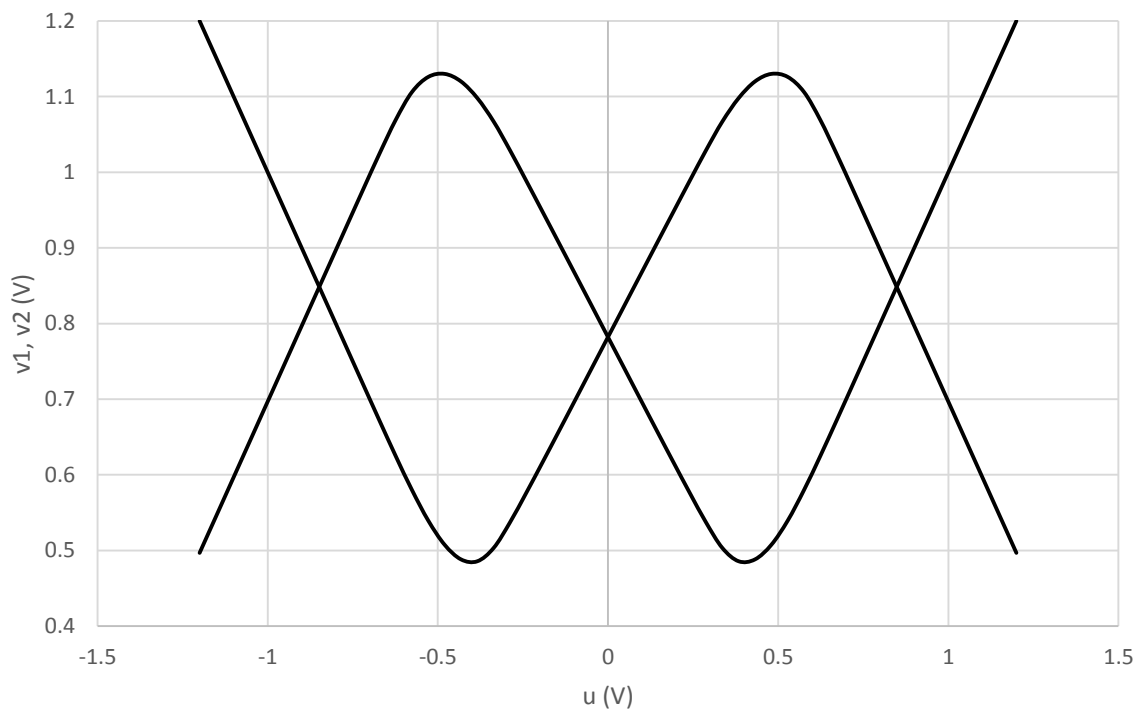
Figure 3.8a: 12T cell hold noise margin
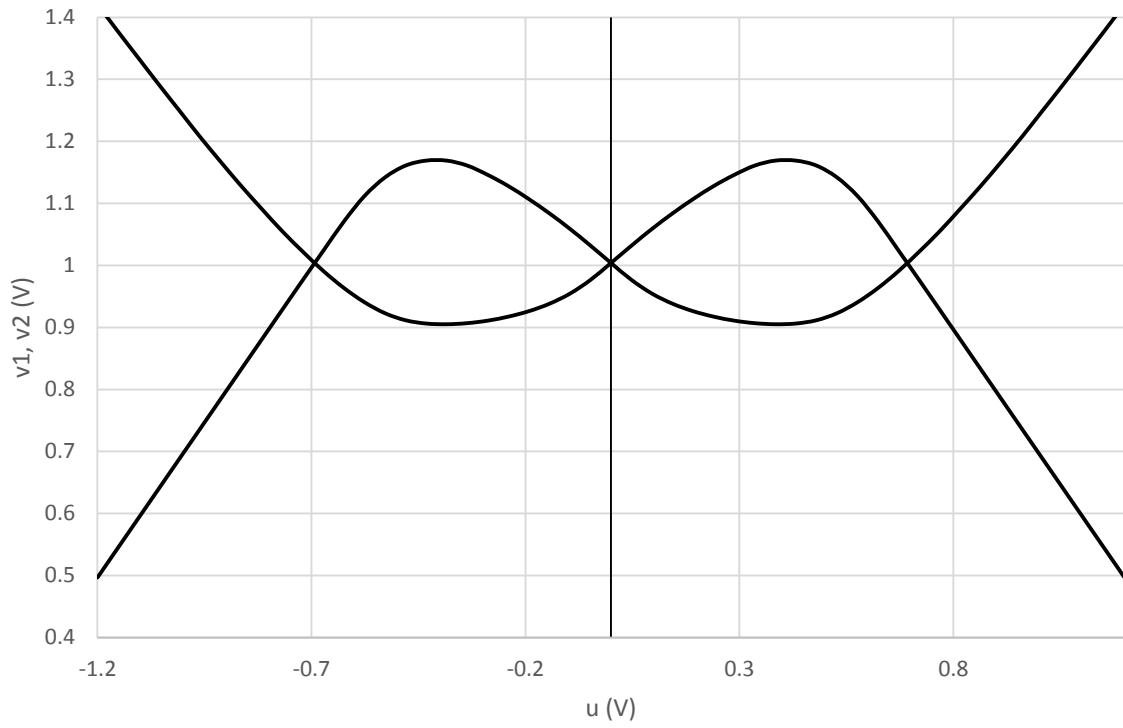
Figure 3.8b: 12T cell read noise margin
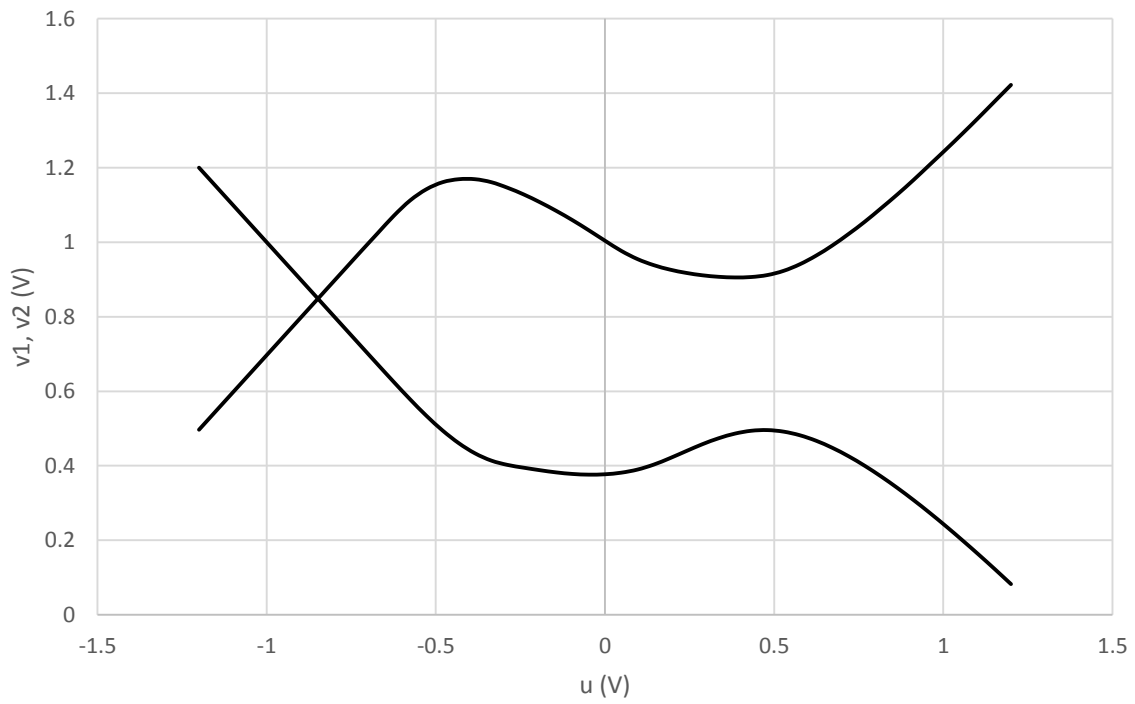
Figure 3.8c: 12T cell read noise margin

Summary

Table 3.2: SNM characteristics of 6T and the proposed 12T cell

Cell	H_SNM	R_SNM	W_SNM
6t_cell	440 mV	168 mV	425 mV
Proposed 12t cell	445 mV	188 mV	340 mV

The SNM noise margin analysis shows that the 12T cell shows an improvement in hold and read noise margins but at the expense of write noise margin degradation. Additionally, the SNM analysis proves the functionality of both SRAM cells.

3.4.5 **Drawbacks**

The main drawback of the proposed design is the increase in power consumption due to introduction of redundant transistors. The conventional 6T cell design consumes a power of 310 pW due to leakage, whereas the 12T cell design consumes a power of 590 pW. Thus the proposed design increases the static power dissipation of the SRAM design by 2X, which is the tradeoff made for the radiation tolerance improvement. The presence of PMOS and NMOS access transistors per bit-line also increases the leakage current via the bit lines, compared to the 6T cell designs that use a single NMOS access transistor per bit-line.

Additionally, the PMOS / NMOS ratio constraint requirement and introduction of transmission gates for access transistors has resulted in the reduction of the write noise margin of the SRAM cell at the expense of improvement in SEMU tolerance.

Chapter 4

4. <u>TESTING METHODOLOGY</u>

4.1 <u>Accuro^{TM} Software Description</u>

Accuro stands for accurate and efficient semiconductor process, device and circuit simulation. It's a highly efficient tool for simulating several single event experiments simultaneously. The tool is suitable for cross section analysis and LET threshold prediction. The GDSII layout and net-list files obtained from Calibre DRC verification tool are the two important input files used for 3D mixed mode single event simulation in Accuro. Apart from that, Accuro also needs supporting library files such as HSPICE models and layout and schematic annotation files.

The HSPICE model files consist of the technology information needed for the SPICE schematic simulation. The model files contain information about SPICE parameters of PMOS and NMOS transistors for the current technology. Additional information provided includes substrate type details, doping information, shallow trench isolation (STI) depth and well depth. These general information, needed for 3D mesh generation of the layout, are obtained from the create definitions script file provided in Accuro directory.

The Accuro tool also needs a layout-schematic annotation file to couple the net list and the 3D mesh model together during simulation. The annotation file helps Accuro to identify contact nodes

in the layout and couple it with the nodes in the net list. The annotation file is generated using a device_match.in script in Accuro. This script also performs a layout (GDSII format) versus net-list (.ckt file) check during its device matching process.

There are 3 main stages in single event simulation in Accuro

a) Creating the 3D Mesh Model: the GDS file and HSPICE information is used to create a 3D mesh model of the SRAM Layout. Accuro simulation tool incorporates 3D transport models to describe the charge collection and transport process [22]. During meshing, higher concentration of mesh points is incorporated at the diffusion and radiation strike regions. This allows for calculation of charge gradient with precision at the location where the ion strike occurs. Also, it reduces the total number of mesh point calculations needed for a complete circuit level simulation. During mesh generation, the cell size is made 2um further from the actual layout boundary occupied by the SRAM cell. This is done to make sure that the charge spreads realistically along the mesh model during single event simulation [22].

b) Circuit Initialization: the initialization process consists of two stages. First, the SPICE simulation of the net list is performed using Accuro. Specific input test vectors are used to drive the circuit into its desired state. Once this is completed, the second stage involves initializing the 3D mesh model to the same circuit state. These processes are to make sure that the circuit reaches its desired state before single event simulation.

c) Event Simulation: single events are simulated at various scan points of the cell and the voltage, current, electric field, and charge density parameters are recorded for each contact node. The extract script used for event simulation captures the voltage at each contact node and records in a .circuit file. The extract command is then used to extract

the voltage and current on the contact node for a particular LET energy condition. These data are then used for post processing analysis for LET threshold prediction and error cross section.

rExplore is the GUI interface of the RCI tool suite, and Accuro is the engine that does the single event simulation. The whole simulation is split into several thousands of experiments, where each experiment corresponds to a particular ion strike scenario. Several parameters such as theta, phi, pivot, LET limit, x, y, z are specified for each experiment. These parameters define the direction and location of the ion strike. Initially a course-grid simulation is done all over the cell area to roughly identify the sensitive areas of the cell. After that, a scan-grid refinement script is executed which will automatically generate more scan points near the identified sensitive location. This refinement technique allows for striking ions at locations where it is sensitive, hence converging into the sensitive areas faster.

4.2 <u>LET Threshold Calculation</u>

For each experiment, the LET energy is varied from a minimum value of 0.0625 MeV-cm^2/mg to the threshold LET value for which the cell flips. The output of the SRAM cell is monitored for each LET strike during scan. The LET threshold value is the energy of the ion strike for which the output node voltage of the SRAM cell crosses Vdd/2 voltage. The highest LET energy used for simulation is 128 MeV-cm^2/mg. The LET threshold value is found for each strike location in the SRAM cell and it is recorded in a tabular format in the rExplore GUI. These LET threshold values are then used to calculate the cross section & sensitivity map of the SRAM cell

As shown in Figure 4.1 (left), radiations strike through all three planes Z-plane (vertical strike), Y plane (normal to the SRAM cell layout plan), and X plane (horizontal plane) to obtain the LET

threshold values at various locations and direction in the SRAM cell. The 3D mesh model of the 6T cell is as shown in Figure 4.1 (right).
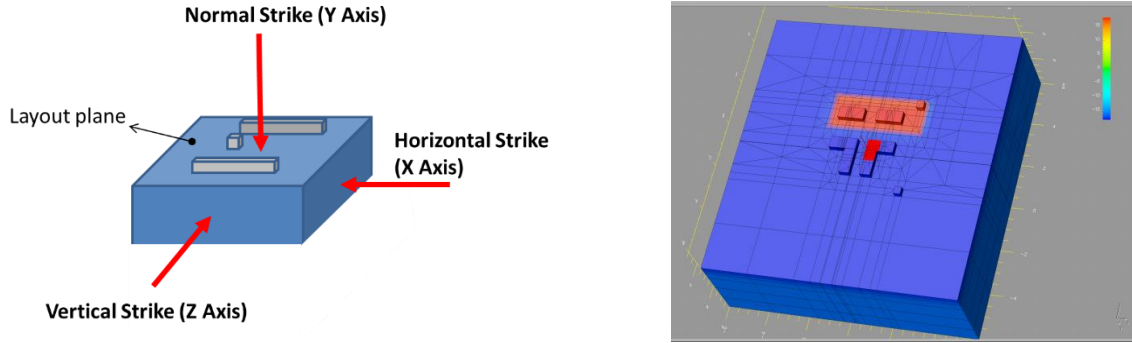
Figure 4.1 : 3D mesh model of the 6T cell used for radiation simulation in Accuro.

4.3 <u>Post Processing</u>

Post processing involves calculation of the cross section area and plotting of the sensitivity map of the SRAM cell. Error cross section of SRAM cells is very useful for analytical evaluation of a cell's radiation performance. A cross section curve considers the impact of both the circuit and layout of the SRAM circuit and hence it gives a realistic picture of a cell's radiation tolerance performance compared to a schematic level simulation. In Accuro, the script xsect_calc is used to calculate the cross section of the chip. The script extracts LET threshold values obtained from individual radiation event experiments done at different ion strike locations and directions. The LET threshold data and the affected unit area are then added up to get the final error cross section curve. Cross section curves for 6T cell and 12T cell are plotted for radiation strikes in 3 different planes (X, Y and Z Axis).

Sensitivity maps are used for estimating the sensitivity of the cell after layout implementation. The map is useful for identifying sensitive areas that are vulnerable to radiation strike events. The script xsect_disp is used to plot the sensitivity map of the SRAM cell, which allows to overlay the

sensitive map of the cell over the layout of the SRAM cell for a particular LET profile. This allows users to quickly identify the weak areas of the cell. Sensitivity maps for a vertical strike (X axis) and a horizontal strike (Z axis) is generated and projected onto the layout plane for display. In this thesis, the sensitivity maps will be projected and shown below the layout for a horizontal strike direction and right side of the layout for a vertical strike direction.

Chapter 5

SINGLE EVENT SIMULATION RESULTS

5.1 6T SRAM Cell Simulation Results

The layout of the 6T SRAM cell was implemented in IBM 130 nm technology. The cadence layout foot print of the 6T SRAM cell is as shown in Figure 5.1. The 6T cell design occupies an area of 27.36 μm^2 with the diffusion area of 5.35μm^2.
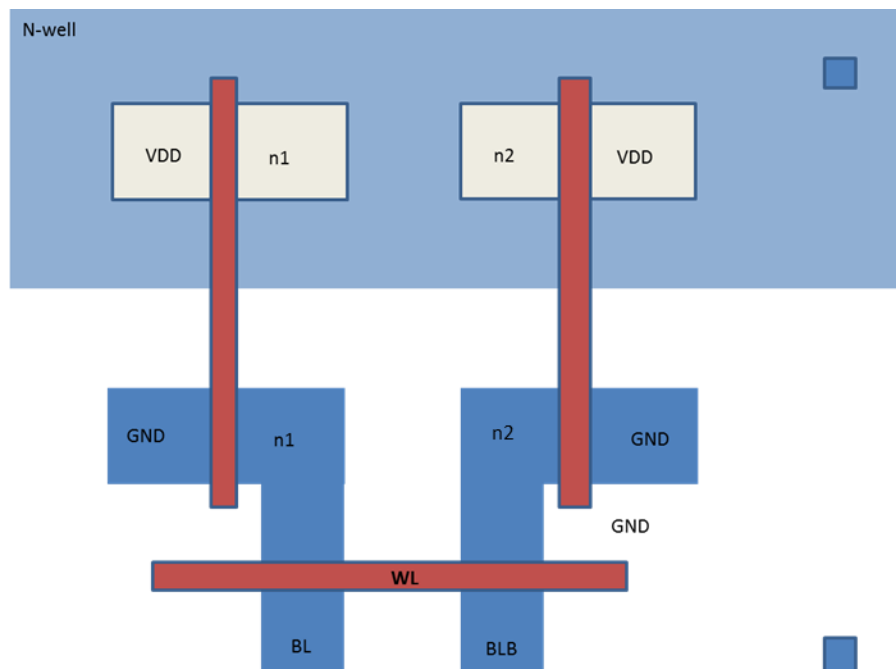
Figure 5.1: Layout of the 6T SRAM cell.

Total diffusion area

PMOS diffusion Area + NMOS diffusion area $= 1.4 * 0.63 * 4 + 1.44 * 0.63 * 2$

$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad = 3.528 + 1.8144$

$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad = 5.3434 \ \mu m^2$

Total layout area

$6.0 * 4.56 = 27.36 \ \mu m^2$

The meshed 3D model of the 6T SRAM cell is as shown in Figure 5.2.
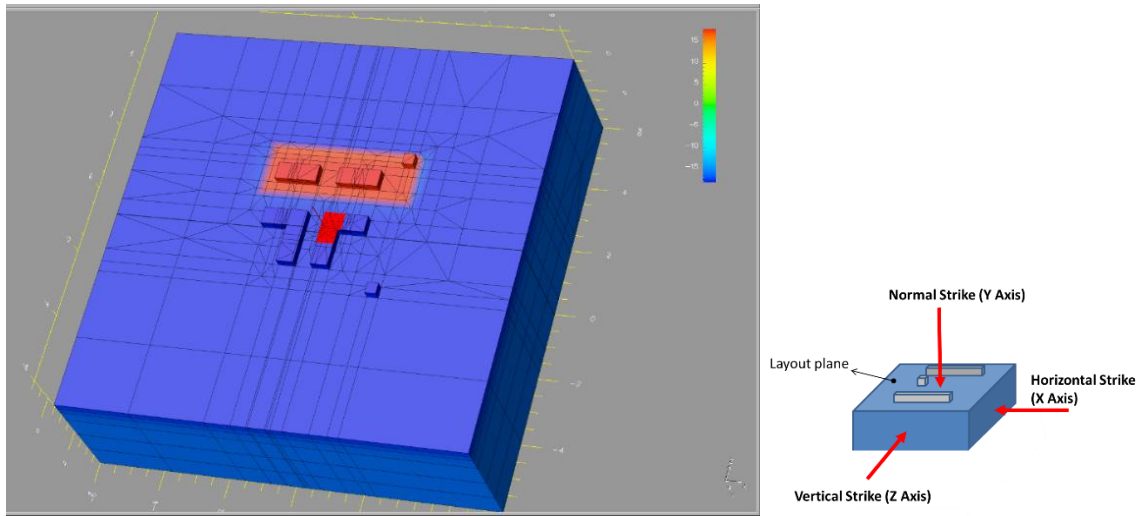
Figure 5.2: 3D mesh model of 6T SRAM cell

Single event strike experiments were performed on the cell with a scan pitch of 0.1μm. Each of the experiments gives the LET threshold value of the single event strike for a particular location of the cell. The 6T SRAM cell was initialized to state 0, and experiments were conducted under this circuit condition. The sensitivity map of the 6T SRAM cell for normal strikes is as shown in Figure 5.3. For sensitivity maps, the unit of distance is in micrometers (10e-6 meters).
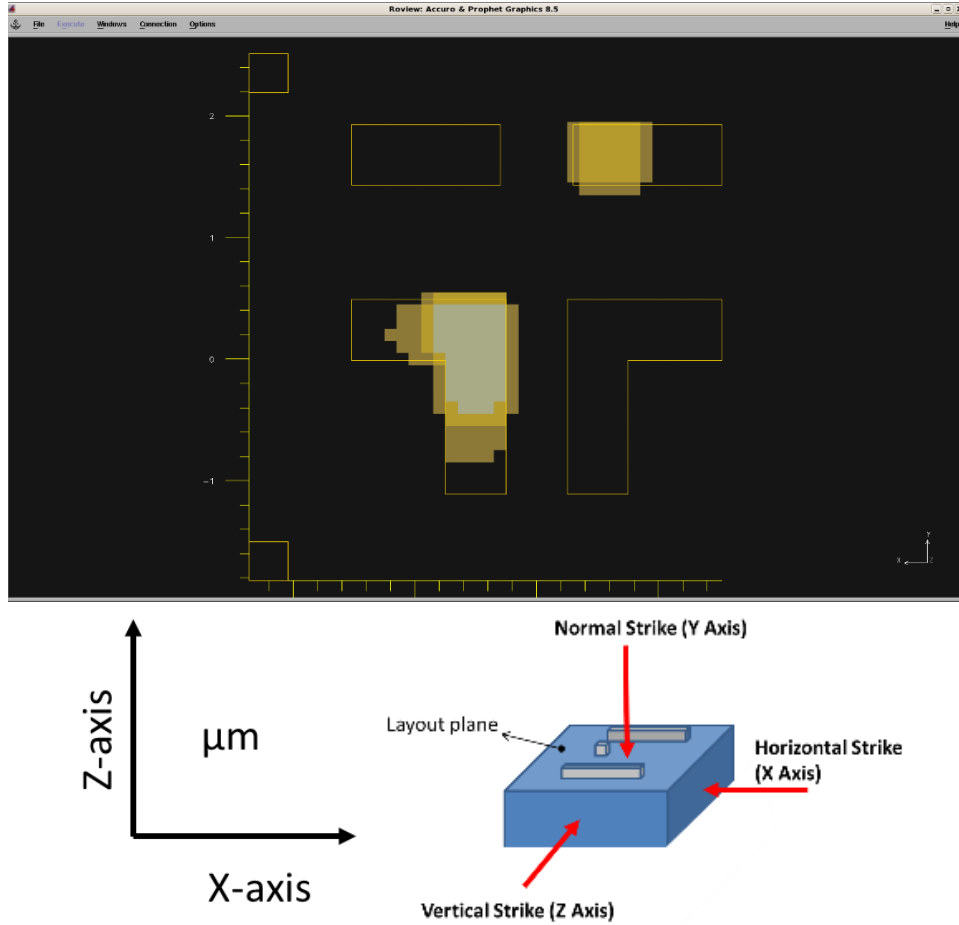
Figure 5.3: Normal strike cross section map of 6T cell for LET= 4 (grey), LET = 5 (yellow) and LET = 10 (light yellow)

From the sensitivity map in the Figure 5.3, we can see that the NMOS node (on the bottom left of figure) has got sensitive regions starting at LET = 3. However, the PMOS node starts showing sensitive regions only at LET = 5. This implies that the OFF Drain node of the NMOS transistor to be more sensitive than the OFF Drain node of the PMOS. This could be because of the fact that the PMOS resides within the N-well, and the well-substrate junction provides a barrier for collection of charge deposited deep in the substrate. Due to this barrier, the charge deposited deep in the substrate cannot re-enter back into the N-well and affect the PMOS node, resulting in fewer charge collection at the PMOS node. The sensitivity map for different LET profiles are plotted as shown in Figure 5.4.
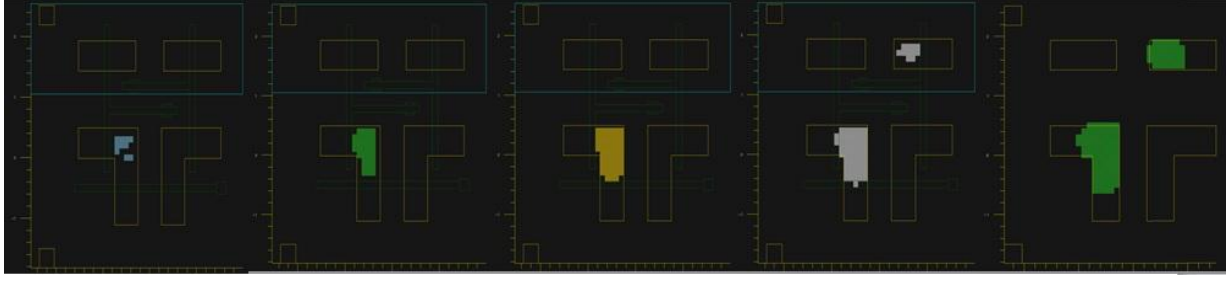
Figure 5.4: LET profile, from left a) LET = 3, b) LET = 3.6, c) LET = 4, d) LET = 5, e) LET = 10

In order to evaluate the sensitive regions during an SEMU strike, we need to plot the sensitive maps for grazing angle ion strike directions. The sensitivity map for horizontal strike direction (X axis) is as shown in Figure 5.5.
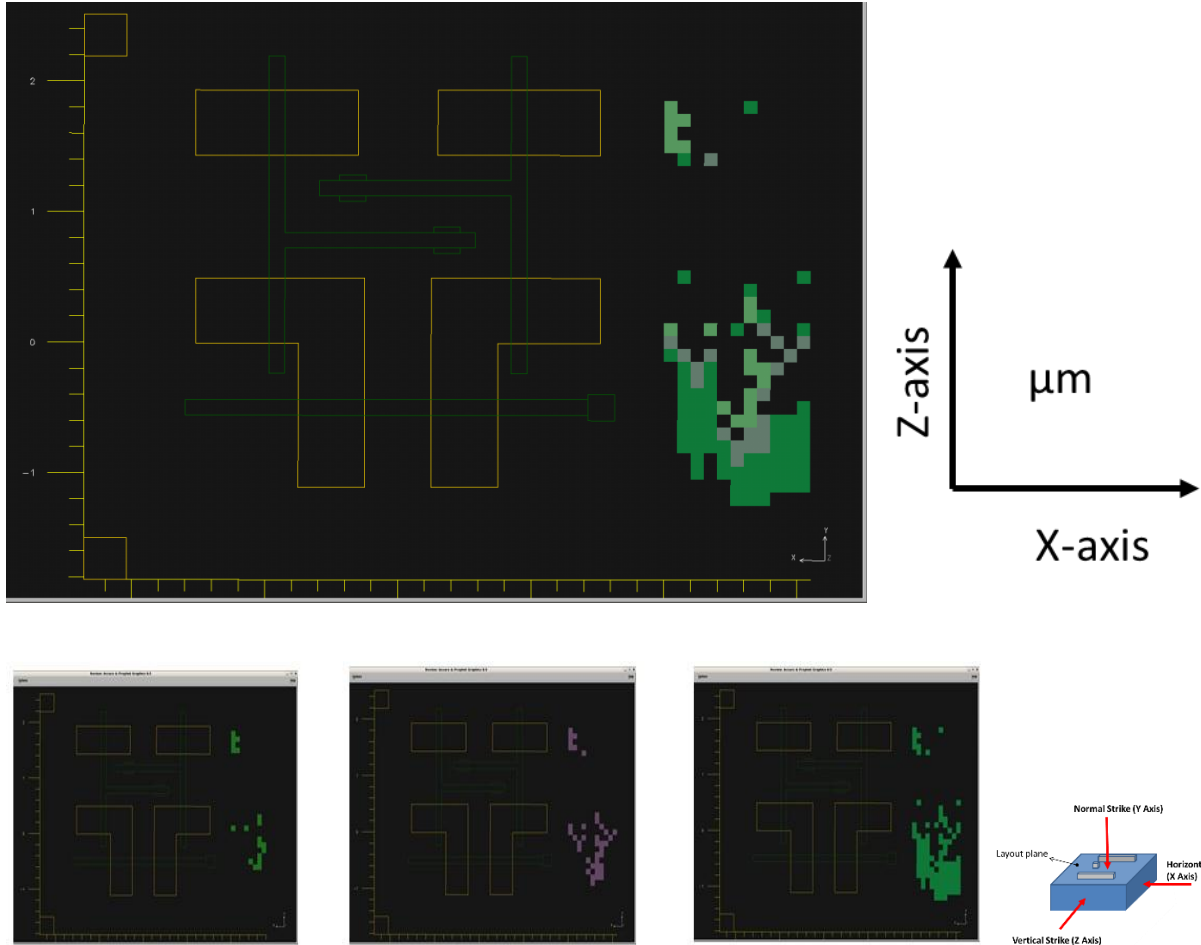
Figure 5.5: Sensitivity map for horizontal strike on 6T SRAM cell for LET = 24, LET = 32, LET = 64.

For grazing angle strikes along the X axis, the map shows that the sensitive area is more towards the bottom of the layout (NMOS region) than to the top region (PMOS). This further reveals the fact that NMOS node is more sensitive than PMOS nodes for the current 6T configuration. However, the threshold LET energy needed for the upset has been significantly raised, since it shows sensitivity only at LET = 24. This is due to the simultaneous upsetting of NMOS or PMOS transistors, which was explained in horizontal strike SEMU mitigation mechanism in chapter 2. Additionally, the effect of access transistors (bottom end of the the 6T layout diffusion region in Figure 5.5) on SRAM upsetting is also shown. For low energy strikes (LET < 24), the access transistors doesn't affect the SRAM cell. However for higher LET energies, the OFF access transistors do cause single event upsets.
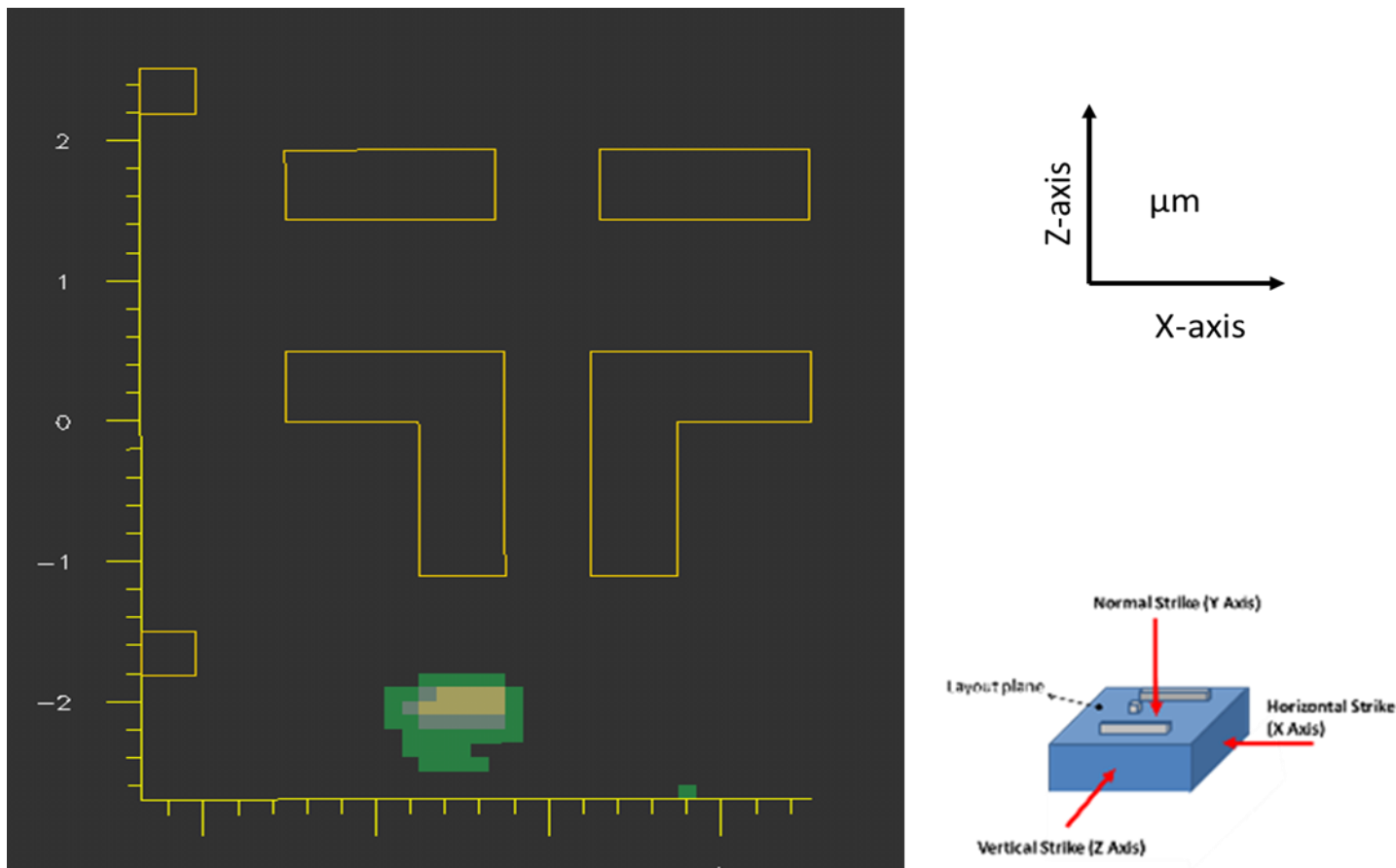
Figure 5.6: (Top) Vertical sensitivity map for LET=2 (yellow), LET = 4 (grey), LET = 16 (green); (Bottom) shows the vertical sensitivity map for LET = 2, 4, 8, 16, 32.
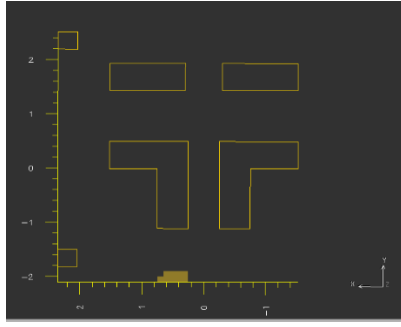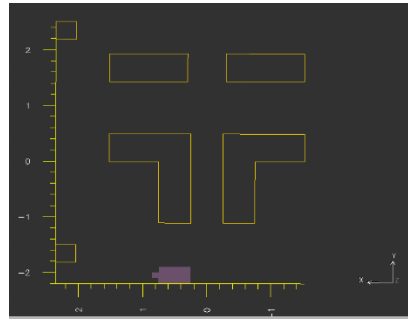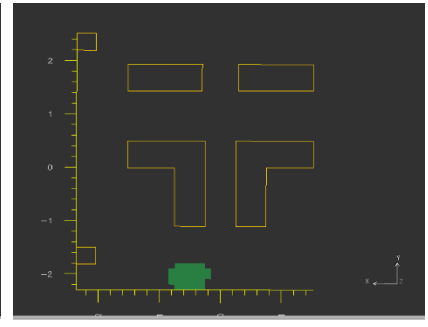
LET = 2   LET = 4   LET = 8
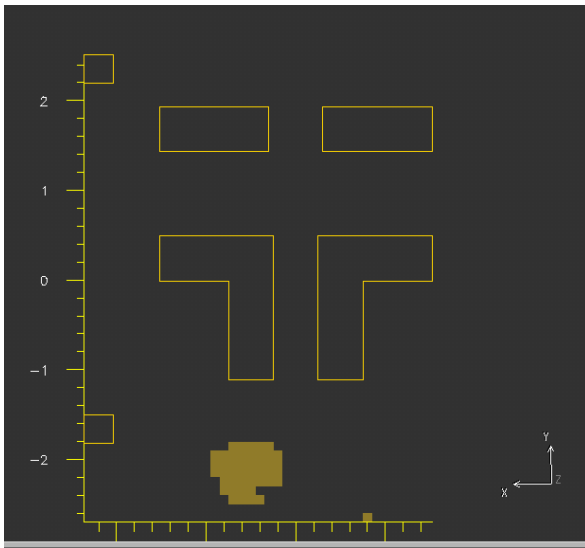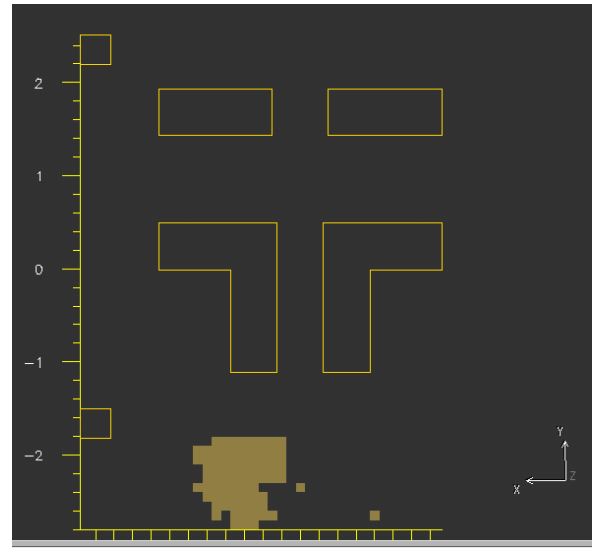
LET = 16   LET = 32

The vertical (Z axis) sensitivity map is as shown in figure 5.6. Here the sensitive region of the SRAM cell is towards the left portion of the SRAM cell layout. For state 0, the left region of the SRAM cell consists of ON PMOS at the top and an OFF NMOS at the bottom. From the sensitivity map, we can see that the cell has sensitive areas for LET energies as low as 2 MeV-cm^2/mg. This makes the 6T SRAM cell highly vulnerable to grazing angle SEMU strikes. The OFF transistors are responsible for the SET generation because they are more sensitive to radiation strikes [2]. In this scenario, NMOS transistor is in OFF condition and therefore we can conclude that the OFF

NMOS node is creating a SET which overpowers the PMOS node that tries to compensate for the transient created.

5.2 12T SRAM Cell Simulation Results

The layout of the 12T SRAM cell is as shown in Figure 5.7. The 12T cell was initialized to state 0, like the 6T cell configuration test setup in the previous experiment. The 12T cell occupies an area of 23.12 µm2 and a diffusion area of 4.9µm2.
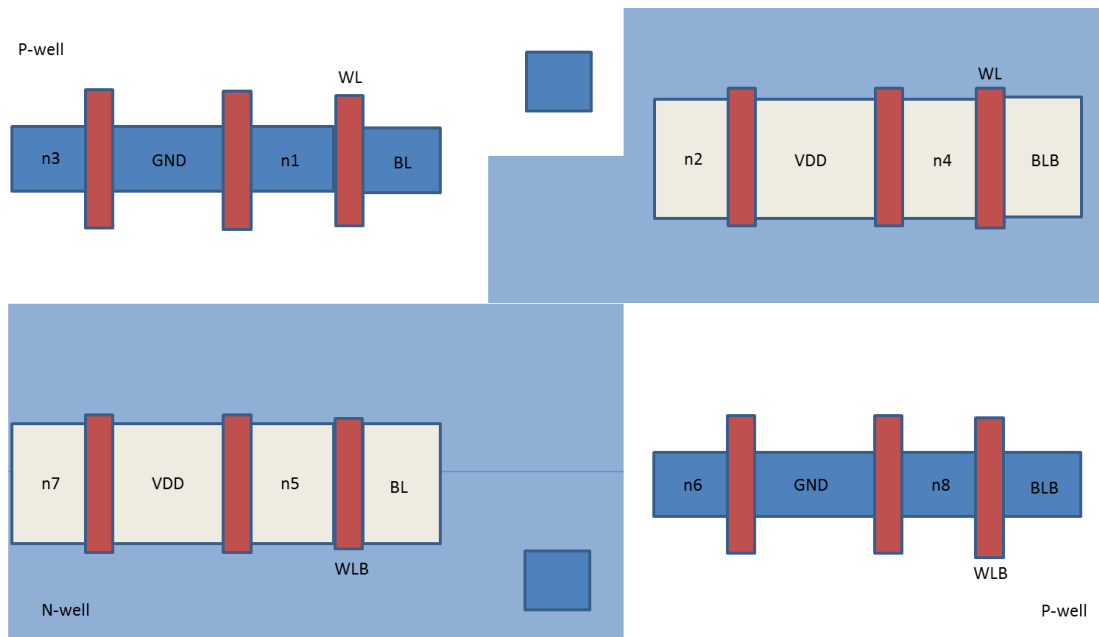
Figure 5.7: Layout footprint of the 12T SRAM cell design

Area calculation of the 12T cell

During the design of the layout for 12T cell, maximum effort has been done to maintain the area of the 12T cell to be same with respect to the 6t cell layout. For fair comparison between both 12T cell and 6T, the total Diffusion and layout area is made equal. The area calculations for the 12T cell are as shown below.

Total diffusion area

PMOS Diffusion Area + NMOS Diffusion area   = 2.41 * 0.39 * 2 + 2.41 * 0.63 * 2

                                              = 1.8798 + 3.024

                                              = 4.9038 um2

Total layout area

6.8 * 3.4 = 23.12 µm2

The mesh diagram of the 12T cell is as shown in figure 2.
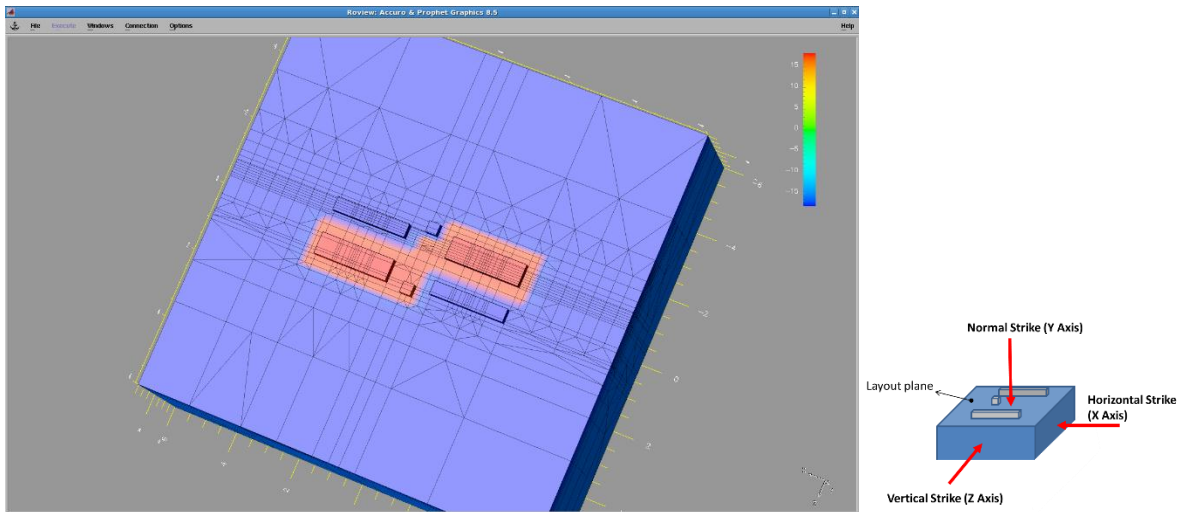
Figure 5.8: 3D mesh model of the 12T SRAM cell

Single event simulations are done on the 12t cell, where the ion strike is simulated throughout the cell with a scan pitch of 0.1µm. The same simulation setup as the 6T cell was used. The cross section map of the 12T cell for normal ion strike along the Y axis (perpendicular to the layout plane) is shown in Figure 5.9.
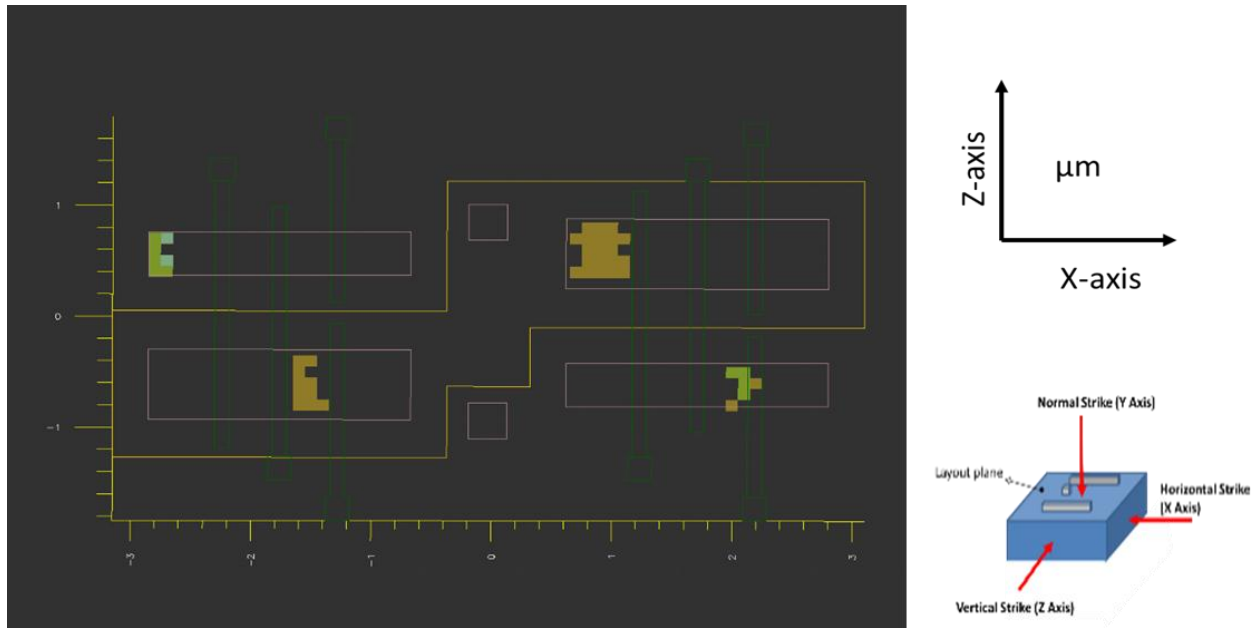
Figure 5.9: Sensitivity map of 12T SRAM cell for normal strike

Comparing this to the previous 6T cell sensitivity map (figure 5.3), we can observe that the total sensitive region has reduced. This reduction in sensitivity area will improve the single-node upset tolerance of 12T cell. Figure 5.10 shows the cross section map of 12T cell for LET=3 (light blue), LET = 4 (light green), LET = 5 (yellow).
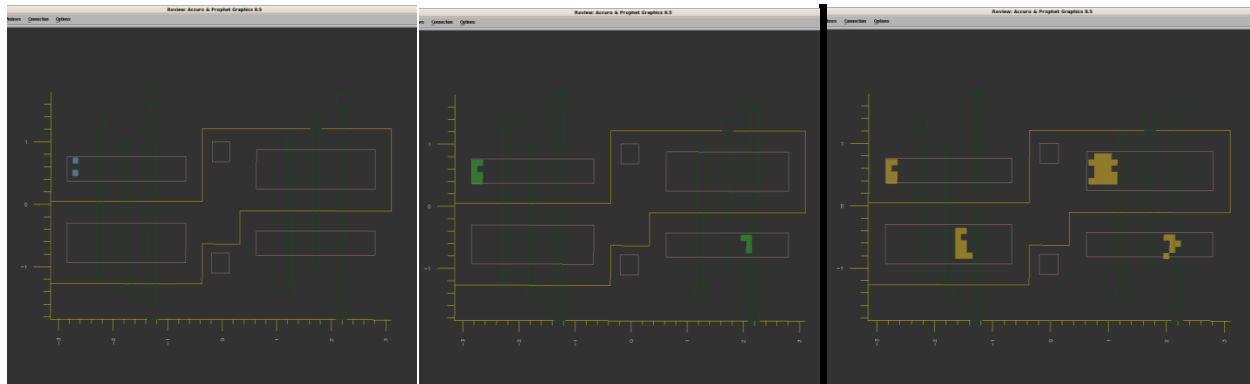
Figure 5.10: Sensitivity map for normal strike, from left a) LET = 3, b) LET = 4, c) LET = 5

Comparing sensitivity maps in Figure 5.10 for 12T cell with Figure 5.4 for 6T cell, gives an idea about the sensitive area reduction (for the same LET) during the layout translation from 6T to 12T cell. An error cross section curve is plotted to quantitatively compare the 6T and 12T SRAM cells.

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5.3 Error cross section analysis and comparison
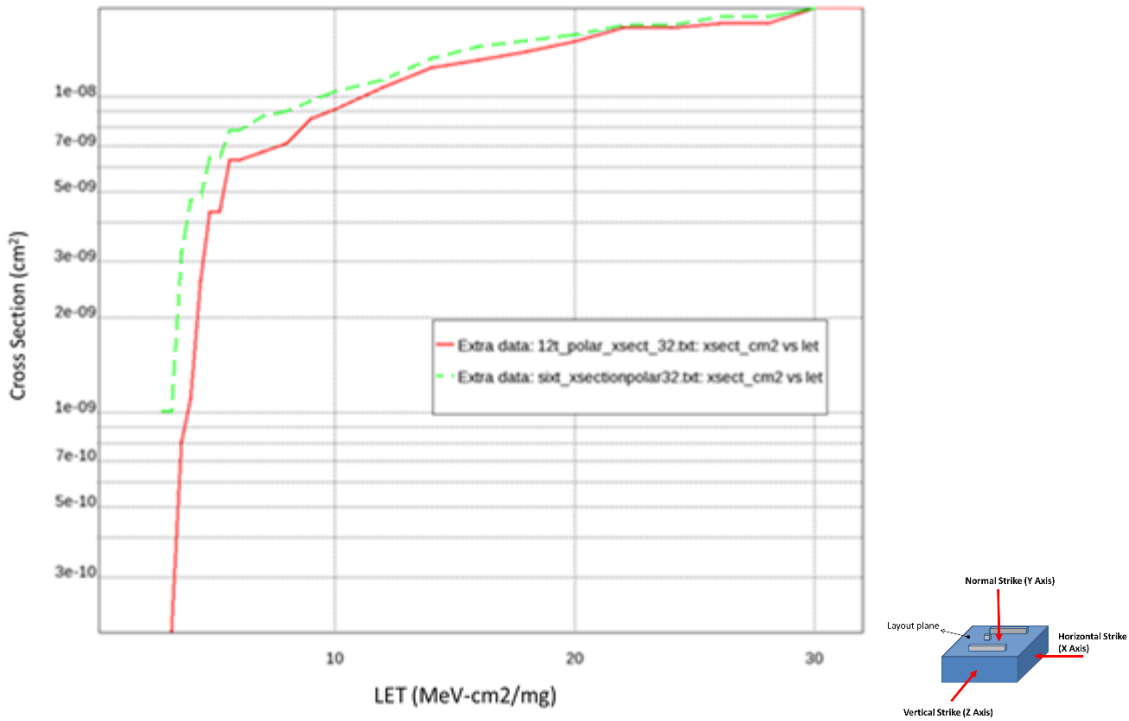
Figure 5.11: Cross section map of 6T (green) Vs 12T cell (red) for normal strikes

Figure 5.11 shows the cross section plot for normal strikes along the y axis. The plot corresponds to the tolerance of the SRAM circuit against single-node upsets striking normal to the layout. From the normal cross section plot, we see an overall lowering of error cross section curve for the 12T cell, which agrees with single-node upset improvement results obtained from the critical charge analysis in chapter 3. We can see that the 12T offers significant radiation tolerance performance for low LET (LET < 10) values.

For SEMU tolerance evaluation, the cross section curve is plotted for ion strikes in grazing angles to the layout plane. For this, ion strikes are simulated in vertical (along Z axis) and horizontal (along X axis) directions.

Initially during the design process, the ratio of width of PMOS to NMOS was chosen to be 2.4.
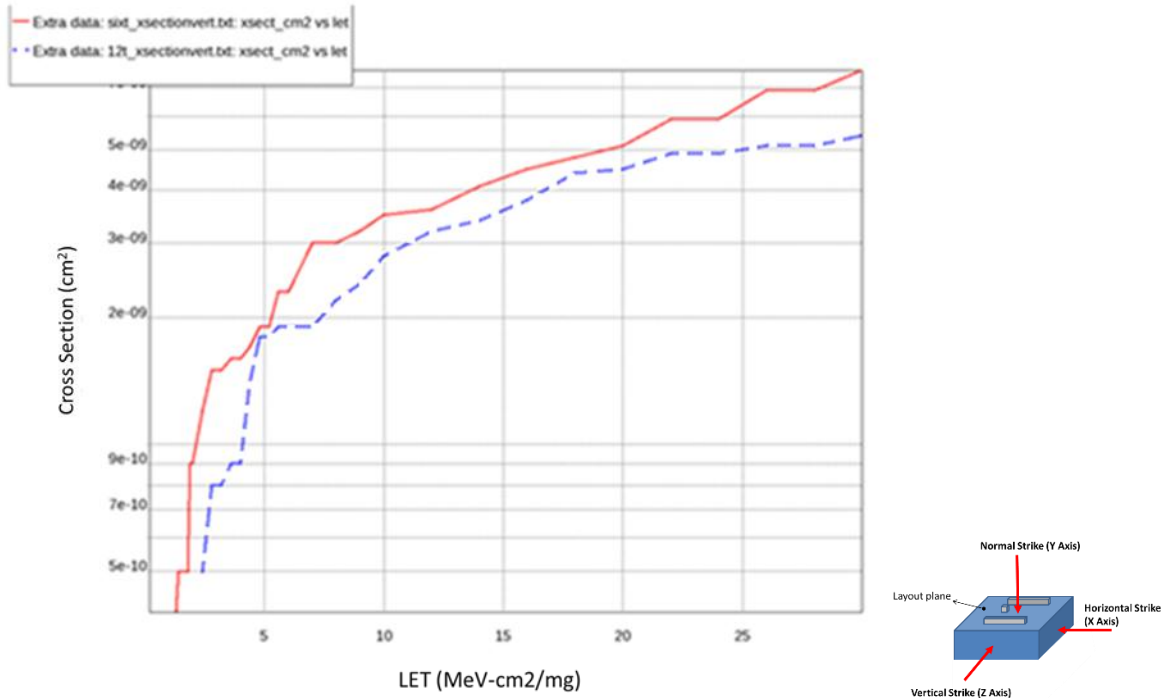
Figure 5.12: Initial vertical strike cross section map for 6T (red) and 12T cell (dashed blue) without PMOS/NMOS matching

The ratio is based on the design given in the LEAP flip-flop (FF) inverter cell design [4]. The Leap FF design was implemented in 180nm technology. However, the current 12T SRAM cell has been implemented in 130nm technology. Hence the optimum PMOS to NMOS ratio for charge cancellation will be different because of the difference in charge carrier mobility associated with different technologies. Also, the SRAM cell implemented consist of access transistors, and they have to be taken into account during the transistor width matching process. Therefore, a new optimum P/N Ratio has to be found using Accuro simulation for maximum charge cancellation in the vertical and horizontal direction. Several 12T cell layouts with different PMOS/NMOS ratios are simulated to find the optimum P/N ratio.
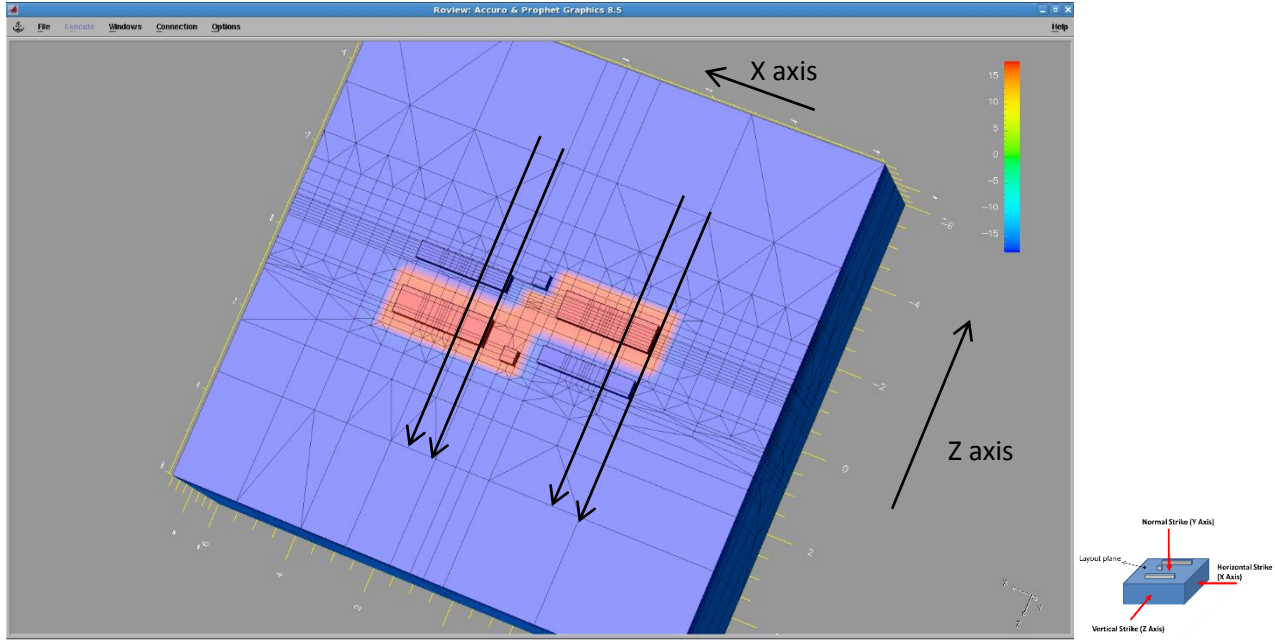
Figure 5.13: 3D mesh model of the 12T SRAM cell, the 2 regions scanned are within black arrows.

Two criteria are considered during the PMOS/NMOS matching process. During the operation of the 12T SRAM cell, inverter can be in two different states. When inverter output is zero, PMOS transistor is OFF and the NMOS transistor is ON. Similarly when inverter output is High (one), the NMOS is OFF and PMOS is ON. For efficient SEMU mitigation, an ion strike on both these inverter configurations should result in efficient charge cancellation.

In 12T cell, two locations with these inverter configuration are identified, and they are subjected to grazing angle ion strikes. These locations corresponds to the 2 different states the inverter can reside during its operation. Ion strike region 1 is from x = 0.6um to x = 1.1µm, as shown in Figure 5.13. This region corresponds to an inverter state, where PMOS is OFF (sensitive node) and NMOS is ON. The second location is from x = -2.8µm to -2.2µm, which corresponds to the inverter cell where NMOS is OFF (sensitive node) and PMOS is ON. The optimum PMOS to NMOS ratio matching occurs when both these strike scenarios result in good charge cancellation. During simulation,

lowering of the LET threshold values indicates the charge overpowering due to OFF PMOS or OFF NMOS transistor, implying a mismatch of PMOS to NMOS ratio. From the experiment results provided in table 5.1, it can be seen that for PMOS/NMOS ratio < 1.6, LET threshold values are decreasing, which can be due to the PMOS off node contributing to the upsetting of the cell. On the other hand, for ratio > 1.6, NMOS OFF node is upsetting the cell. Hence an optimum ratio of 1.6 is chosen. With this optimum ratio, the vertical cross section of the 12T SRAM cell is evaluated.

Table 5.1: LET threshold for radiation strikes at different locations for various PMOS / NMOS ratio.

node	location(μm)	P/N device matching for maximum charge compensation in 12t cell						
	PMOS/NMOS	1	1.5	1.6	1.7	1.8	2.2	2.4
PMOS OFF & NMOS ON (y=2)	-2.8	-	-	128	128	128	128	128
	-2.7	2.75	52	88	128	128	128	128
	-2.6	2.75	44	76	128	128	128	128
	-2.5	2.375	38	60	128	128	128	128
	-2.4	2.375	34	52	128	128	128	128
	-2.3	2.75	22	30	52	-	128	128
	-2.2	5	26	30	38	-	104	88
NMOS OFF & PMOS ON (y=2)	0.6	128	128	128	17	13	9.5	7.5
	0.7	128	128	128	7.5	4.75	3.75	2.75
	0.8	128	128	128	6.5	4.25	3.75	2.75
	0.9	128	128	128	128	4.25	3.25	2.375
	1	128	128	128	128	4.75	3.25	2.375
	1.1	128	128	128	7.5	4.25	3.25	2.375
	1.2	128	128	128	128	-	9.5	4.75
	1.3	128	128	128	128	-	128	38

The cross section plot of figure 5.14 shows the vertical strike cross section curve after matching the PMOS and NMOS transistor widths. From Figure 5.14, it can be seen that the Minimum LET threshold for 12T cell is 26, whereas the 6t cell threshold is only 1.1875. This corresponds to a 22X times improvement in SEMU tolerance in vertical strike direction. These LET threshold values are obtained from the rExplore LET threshold table, which was used to plot the cross section curve in Figure 5.14. The sensitivity map in the vertical direction after matching is as shown in Figure 5.15.
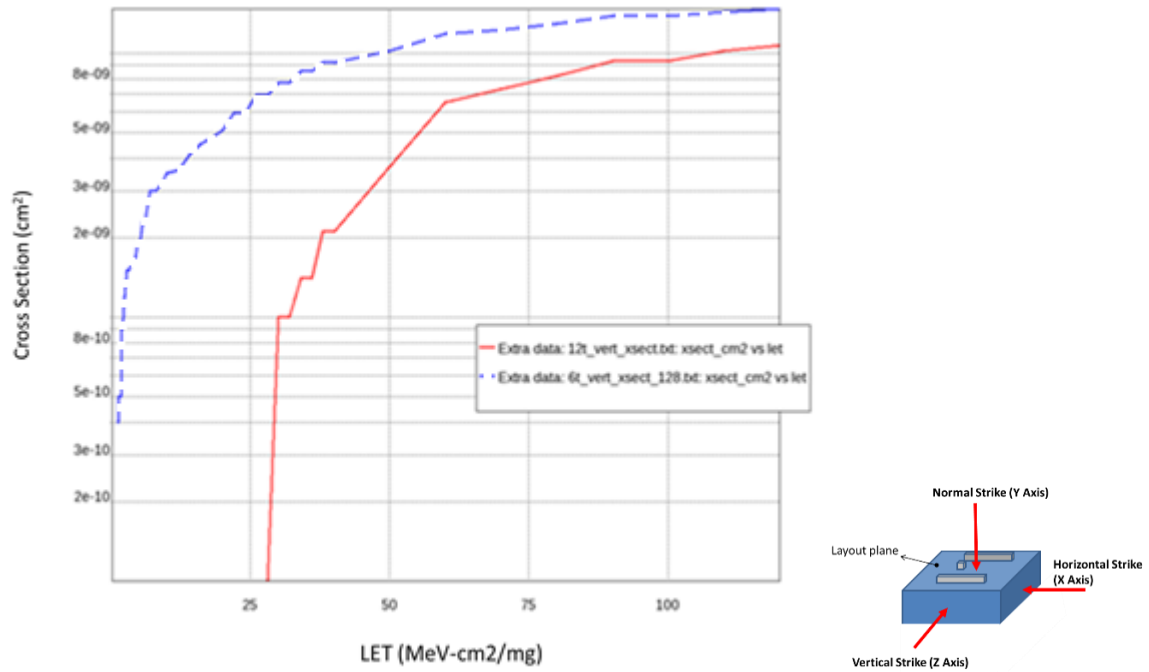
Figure 5.14: Vertical cross section plot for 6T (dashed blue) and 12T (red) after PMOS / NMOS matching
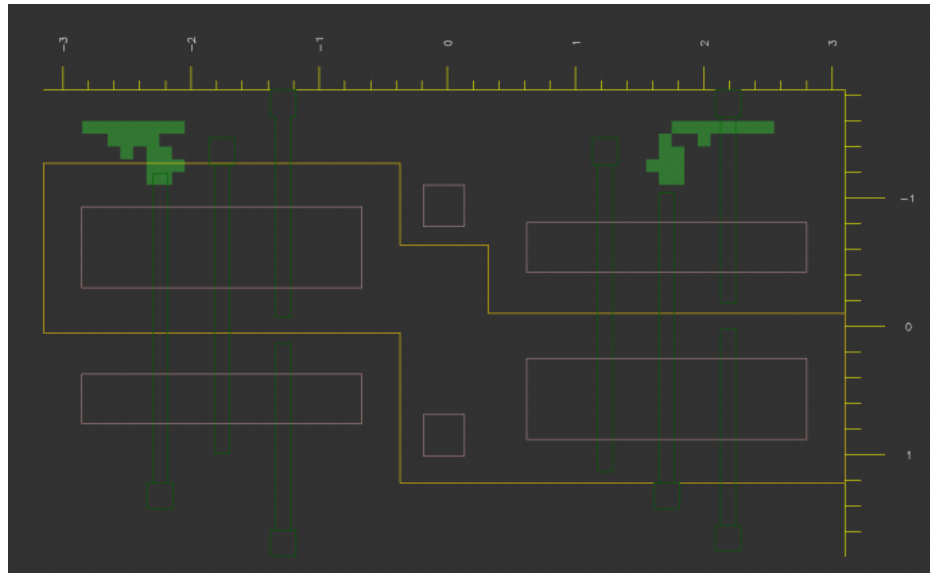
(a)
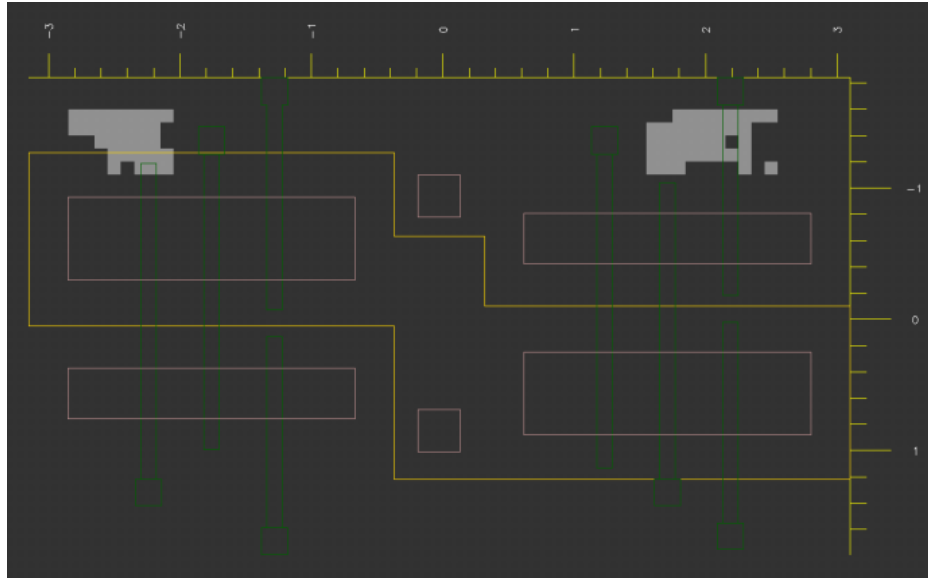
(b)
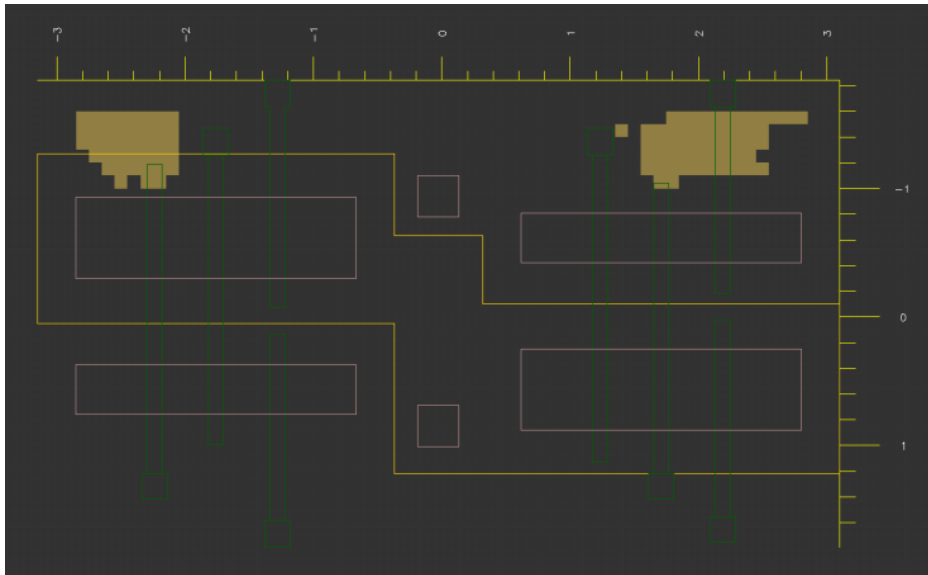
(c)

Figure 5:15: Sensitivity map for 12T cell when a) LET = 48 b) LET = 64 c) LET = 96
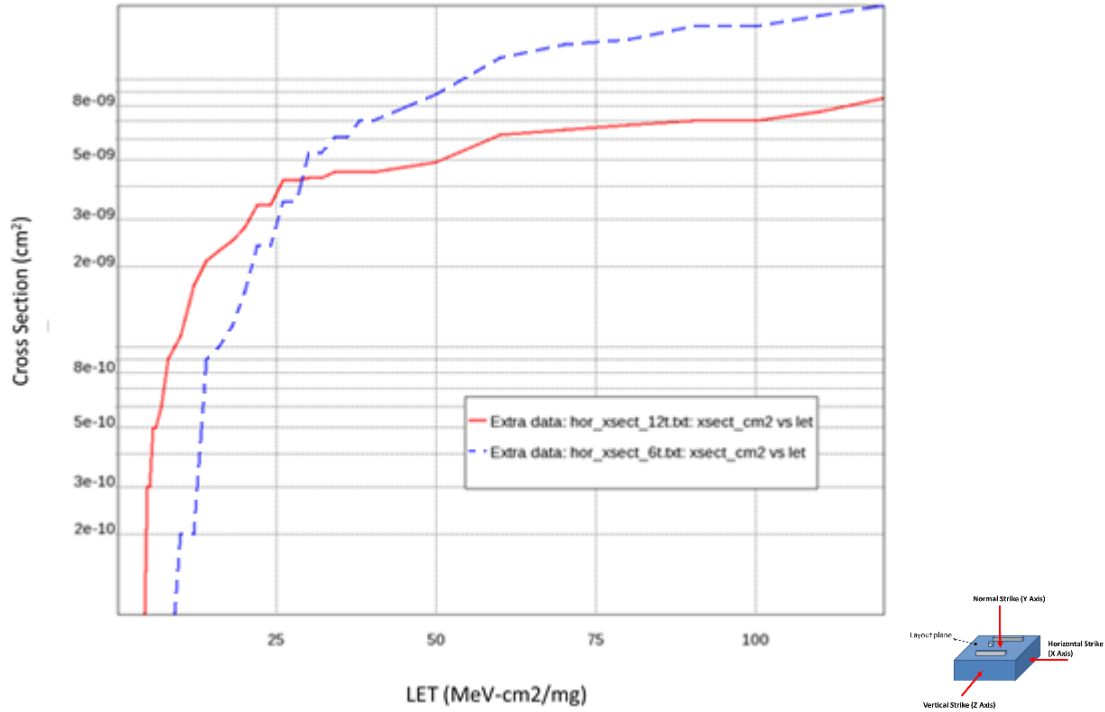
Figure 5.16: Horizontal cross section plot for 6T cell (dashed blue) and 12T cell (red)

Figure 5.16 shows the cross section curve for 6T and 12T cell for radiation strikes along the X axis (horizontal strike parallel to the layout plane). It can be seen that the radiation tolerance level improves in the horizontal direction for LET values greater than 28 MeV-cm^2/mg and for LET < 28 MeV-cm^2/mg, the 6T cell has slightly lower cross section than 12T. However, Also note that the error difference between 12T and 6T for LET < 20 MeV-cm^2/mg is in the order of 1^-9) compared to cross section error difference in higher LETs > 20 MeV-cm^2/mg (10^-9). Hence this advantage of 6T cell in low LETs doesn't give a significant radiation tolerance improvement for the 6T cell compared to 12T. This anomaly can be due to the access transistors of PMOS and NMOS nature along the horizontal strike direction. In case of 6T cells, both the access transistors are of NMOS type. Hence during a radiation strike, they generate the same negative voltage transient which only flip the cell for higher strike energies (LET > 32 MeV-cm^2/mg) as shown in

Figure 5.5. However for 12T cell the access transistors on both sides generate positive and negative voltage transient respectively, which creates a different upset mechanism to the 12T cell compared to the 6T.

5.4 <u>Summary</u>

Cross section and sensitivity map analysis of 6T and 12T cell, done in 3 major axis (X, Y, Z axis), reveals a significant improvement for single-node and SEMU tolerance for the proposed 12T cell design. The SEU simulations in the normal strike direction were done to compare the single-node upset tolerance of the cells. Based on the simulation results, the improvement in cross section of the 12T cell does correlate with the 5fC improvement obtained during the critical charge analysis. Furthermore, the 12T cell showed decrease in the sensitive area compared to the 6T cell for the same LET energy profiles.

SEMU tolerance analysis of both the 6T and 12T cell are done for vertical and horizontal strike directions. The cross section plot for vertical strike showed a significant improvement in LET threshold by a factor of 22x for the 12T SRAM cell. This would greatly improve the overall SEMU tolerance of the cell, since this is the direction where the cell is most vulnerable to SEMU strikes. A slight anomaly was observed for the horizontal radiation strikes. For lower LET values (LET < 25 MeV-cm^2/mg), cross section of the 6T cell was slightly better than proposed design. But for higher LET values (LET > 25 MeV-cm^2/mg), 12T cell has better cross section results.

Chapter 6

LASER TESTING OF VIRTEX-5 FPGA

Lasers provide an easy and convenient solution for SEU tolerance testing of SRAM's. They provide flexibility to precisely vary the energy of the laser pulse strike, enabling us to evaluate the SEE characteristics of SRAMs. Additionally, lasers can be used to make targeted strikes on narrow scan areas, allowing us to map the sensitive areas of the chip. The invention of two photon absorption laser technique has further accelerated the use of lasers on radiation tolerance testing. The technique has enables targeted charge deposition in the semiconductor material with low loss compared to the conventional single photon lasers.

6.1 Objectives

An infra-red laser based on two photon absorption (TPA) is used for SEU tolerance evaluation of Xilinx Virtex-5 LX50T FPGA. The DUT FPGA is part of the Genesys Virtex-5, XC5VLX50T-FFG1136 (1C) development board**.**

The main objective of the laser experiment is to evaluate the SEU tolerance of SRAM based configuration memories in Virtex-5 FPGA. Upset threshold estimation and cross section analysis of configuration memories are performed for a 386 x 386 μm scan area to evaluate the error cross section. Additionally, the SEU characteristics of other major functional blocks such as CLB's,

DSP48E, and Block RAM's are also studied. The testing procedure for these blocks involves location identification and upset threshold analysis of various functional blocks of the FPGA.

Four types of RTL codes are used for testing 4 major functional blocks in the FPGA.

The tests conducted by using pulsed laser are as follows

1. Config_memory Test: To assess the SEU tolerance of SRAM based configuration memory

2. Counter Test: Test the SEU tolerance of CLB blocks in the FPGA.

3. XDSP48 Test: Test the SEU tolerance of Xilinx XDSP48 Macro blocks in FPGA.

4. Block RAM code: Test the SEU tolerance of Xilinx RAM blocks in FPGA

Each Verilog hardware description language (VHDL) codes activates various functional block inside the FPGA. Initially, scan windows are chosen to selectively scan the areas in the FPGA chip where the functional blocks might most likely be present. During the laser scan, any disruption in their functionality is read back in real time through the JTAG or FPGA debug output lines to detect the single event upset. All the RTL codes used for the TPA laser testing have been obtained from MDA Corporation. However, the codes have been modified to make it suitable for Virtex-5 LX50T based laser testing.

6.2 <u>Test Setup</u>

Laser Type: Pulsed two photon absorption infrared laser
Wavelength: 1210 nm
Pulse Repetition Rate: 1 KHz
Pulsed Laser Power: Variable from 100 pJ to 1 nJ
The Virtex-5 FPGA board was tested in the TPA pulsed laser laboratory at Saskatchewan Structural Sciences Centre (SSSC), University of Saskatchewan. The photograph of the test facility is as shown in Figure 6.1a. Two photon absorption (TPA) is the mechanism in which 2 photons of

the same nature or different wavelength is simultaneously absorbed by the material to excite its state. The laser source uses a sapphire crystal to generate the IR beam, which passes through a tunable optical parametric amplifiers (OPA) to generate the 1210 nm IR laser at 1 KHz repetition rate. The laser is then passed through a beam splitter that passes a fraction of the power (10%) to the IR power meter for measuring the laser power in real time. The main power of the laser goes to the confocal microscope and is focused on to the device in the test sample.

A 10X optical lens is used for imaging / scanning the laser, with 4x, 16x and 32x digital zooming capability. Each of these zoom setting correspond to 386 x 386 μm, 96 x 96 μm and 48 x 48 μm respectively. The scanning was done with a dwell time of 3.2us / pixel.
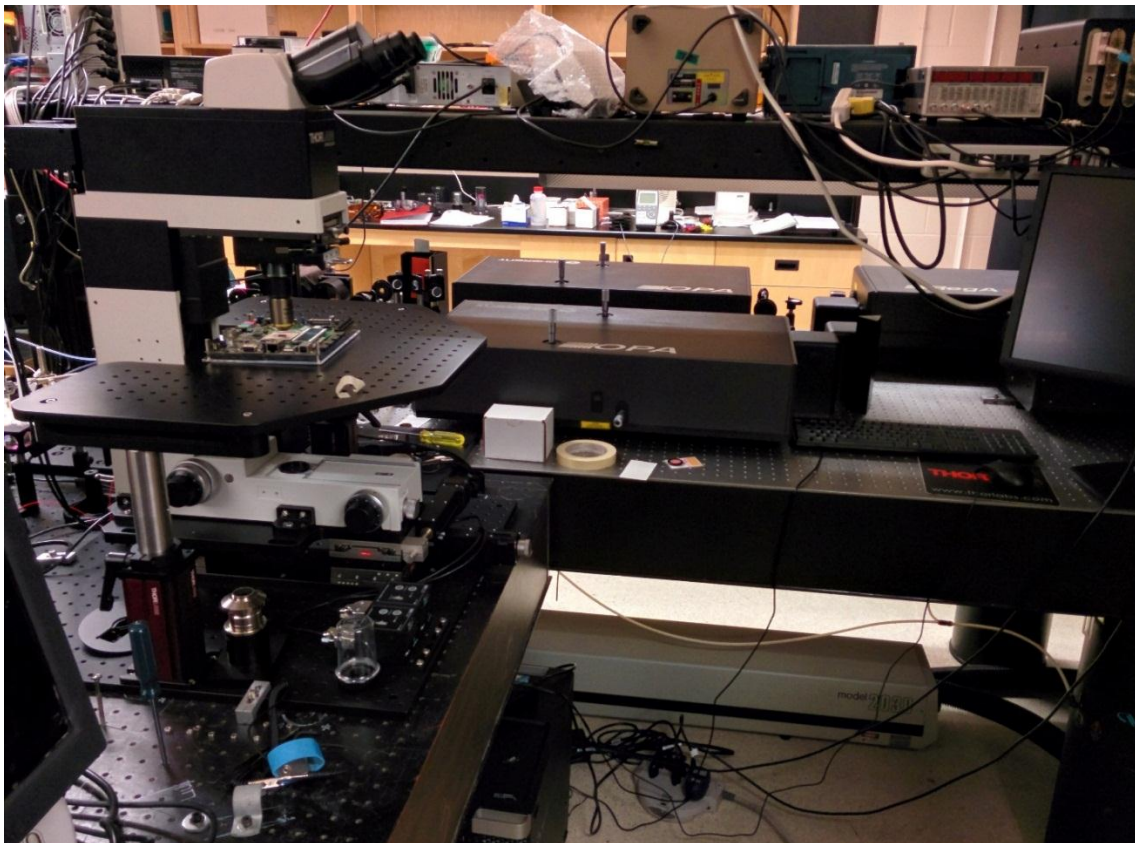
Figure 6.1a: TPA laser facility at SSSC, University of Saskatchewan

The Virtex-5 FPGA is fabricated in a 65nm process, with the internal core logic operating at 1V supply voltage [33]. The chip cover is removed in order to expose the FPGA from the chip back side, which will allow the TPA laser to easily penetrate through the silicon substrate side of the chip. This allows the laser to upset the diffusion regions of the FPGA without metal layer obstruction. The Virtex-5 board with the silicon side of the chip exposed is as shown in figure 6.1b.
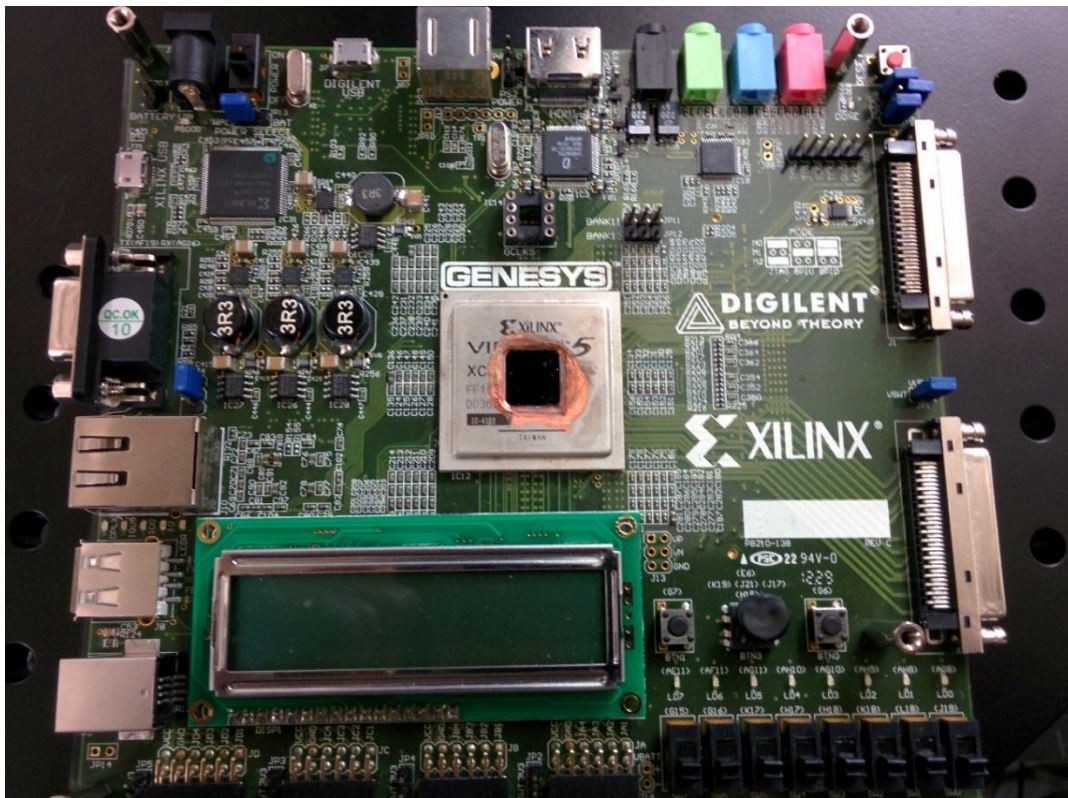
Figure 6.1b: Virtex 5 LX50T board used for laser testing

6.3 <u>Testing Methodology</u>

Initial tests involve scanning of selected areas in the chip to identify the location of various functional blocks within the Virtex-5 FPGA. The Xilinx floor planner tool offers a virtual map regarding the relative location of functional blocks with respect to the chip boundary, but it doesn't give the actual geometric locations of these blocks. Different VHDL codes are used to activate

different functional blocks within the FPGA and additional debug test points and error counters are used along with the main code to detect errors occurring due to laser induced upsets. JTAG interface and Xilinx Chip Scope Pro software are used to monitor the internal signals of the FPGA. While scanning, the debug data obtained from the chip scope software and JTAG are continuously monitored to pin point the location of functional blocks within the FPGA.

After identifying the location of blocks, the next step is to identify the upset threshold energy for each functional blocks. For this test, the TPA laser scan is focused on a particular scan area around the functional block. The laser energy is then varied from a low value of 100 pJ to 1 nJ and the error outputs are observed. The energy at which the functional blocks exhibits data corruption is considered as its threshold upset energy.

Some of the functional blocks are huge in number and is distributed throughout the FPGA, e.g. the configuration memory. For these blocks, an error cross section analysis has to be performed in order to quantitatively assess the radiation tolerance. In cross section analysis, 3 different scan areas sizes are chosen, where the laser is used to the scan each of the area for a fixed period of time with a certain laser energy. This gives us a general idea of the bit error rate with time of exposure and laser pulse energy. The number of bit errors versus time is then recorded for different laser pulse energies. The data is used to plot the error cross section of the configuration memory.

6.4 <u>Configuration Memory Test</u>

Configuration memory is the fundamental SRAM unit used for storing the configuration data within the FPGA. Configuration data determines the function and interconnections of different blocks, hence they can be considered as the most critical units within the FPGA. A single event

upset in the configuration block can result in a non-upset condition, or a functionality upset disrupting a critical functionality of the FPGA (e.g. upset on a power reset logic).

The 6T SRAM cells used in the configuration memory of the FPGA are different from those in the general purpose SRAMs. In general, the 6T SRAM cell used in FPGA's have resistive feedback between the two back-to-back inverters for improving its radiation tolerance [34]. The schematic of the resistive feedback 6T SRAM cell is shown in Figure 6.2. The addition of resistors will increase the feedback time of the cell, resulting in improvement of its SEU tolerance [2], but it comes at a price. Resistive feedback will increase write time and hence is not commonly used for general-purpose memory applications.
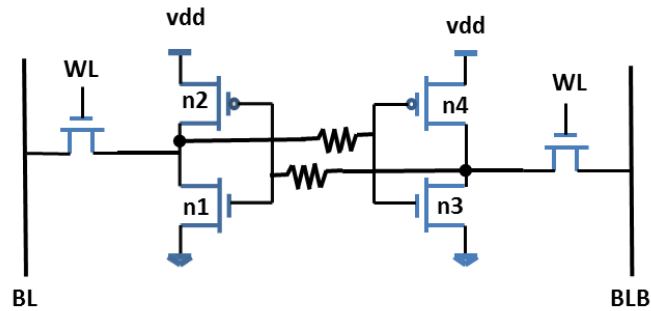
Figure 6.2: Resistive feedback based SRAM cell used in FPGA's

In this test, a simple bit file is loaded into the internal configuration memory of the FPGA. It's a simple piece of code to turn ON the LED's in the DUT board and maintains them. After loading the bit file, the laser is used to scan the selected area of the FPGA. In the experiment, the scan area chosen is in the CLB array, (Refer Figure 6.3) located between the Block RAM column and DSP48 column of the Virtex-5 FPGA. During the laser scan, the configuration memory data are repeatedly read back at defined time intervals via the JTAG interface. The read back data are compared with the original bit file data to identify the number of bit upsets.

Initially a threshold analysis is performed on a 386 x 386 μm scan area within the CLB array area of the FPGA as shown in Figure 6.3. The configuration memory bit errors versus laser pulse energy is as shown in Table 6.1.

Table 6.1: Number of configuration bit errors vs laser pulse energy (pJ)

Energy per pulse (pJ)	Errors in configuration bits
200	0 errors
250	0 errors
295	1-2 bit errors
300	5 bit errors
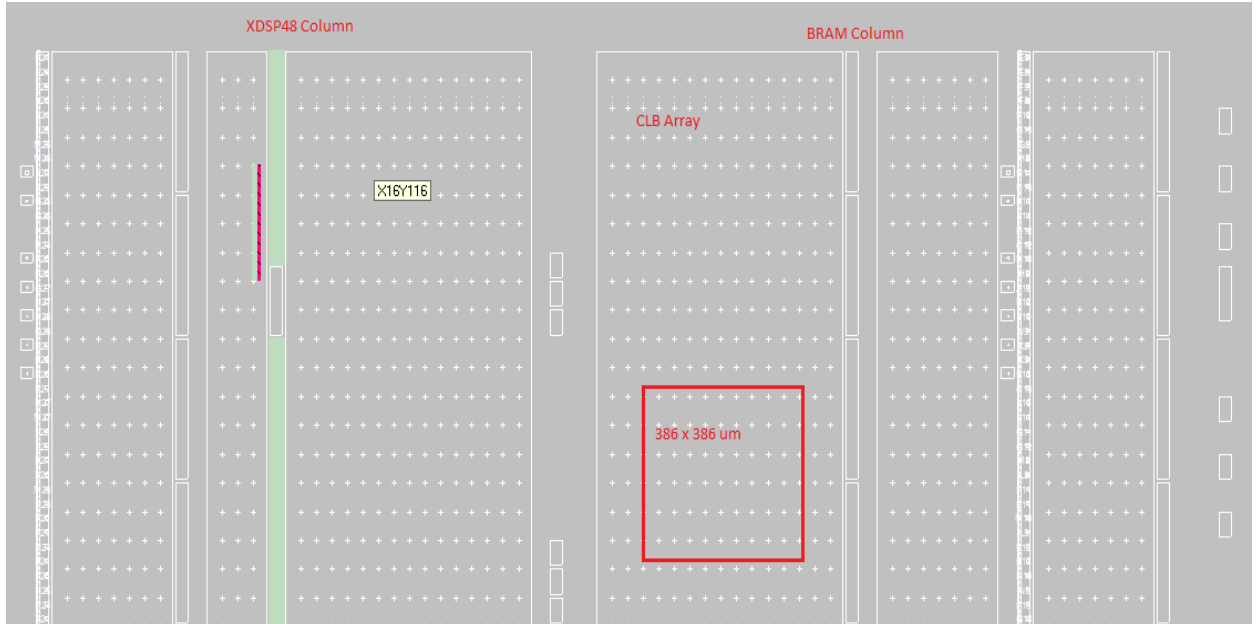
Figure 6.3: The 386 x 386 μm scan area chosen for configuration memory testing in Virtex-5 (Courtesy: Xilinx floor planner)

From Table 6.1, we can see that the threshold upset energy for configuration memory is around 300 pJ. Beyond the threshold energy, the configuration memory bit errors increase rapidly. In order to better understand the rate of increase of bit errors with laser energy and laser exposure time, 3 different scan areas are chosen in the CLB array with areas of a) 384 x 384 μm, b) 96 x 96 μm,

and c) 48 x 48 µm. The micrograph of the scan region and the bit error data corresponding to different energies are provided in following figures and tables. The laser scan parameters are as follows

Laser repetition rate = 1 KHz; Scan area = 386.4 x 386.4 µm

Pixel size = 1.502 µm/pixel; Therefore, pixel area = 257 x 257 = 66049 pixels

Pixel dwell time = 3.2us / pixel; Time taken for a single scan = 66049 * 3.2e-6 = 0.2s

Figure 6.4: Configuration memory micrograph for laser scan area of 384 x 384 µm

Table 6.2: Configuration bit errors with laser exposure time for different laser pulse energies

Energy (pJ)	10s	30s	60s	2min	4min
100	0	0	0	0	0
200	0	0	0	0	0
300	0	2	2	6	13
350	6	21	48	94	166

400	51	136	188	348	559
500	154	352	599	1029	1429
600	224	479	732	1169	1616
700	766	1514	2322	3571	5387
800	2111	4401	6497	8821	11604
900	3307	6726	8992	11546	12741
1000	3830	7689	10286	12657	12977

Based on the results for 386 x 386 μm scan (Table 6.2), the bit error count increases rapidly after the threshold energy of 300pJ. The bit error count increases 3 – 4x times from 500 pJ to 800 pJ. After 800pJ, the error count follows a saturation trend and the bit error count saturates to 13000 errors.
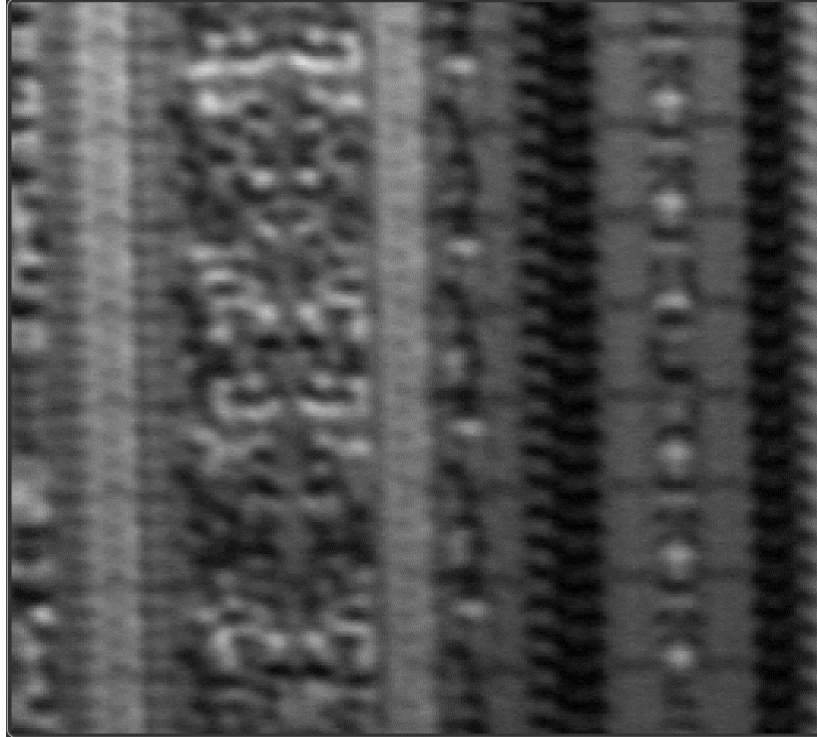
Figure 6.5: Configuration memory micrograph for laser scan area of 96 x 96 μm.
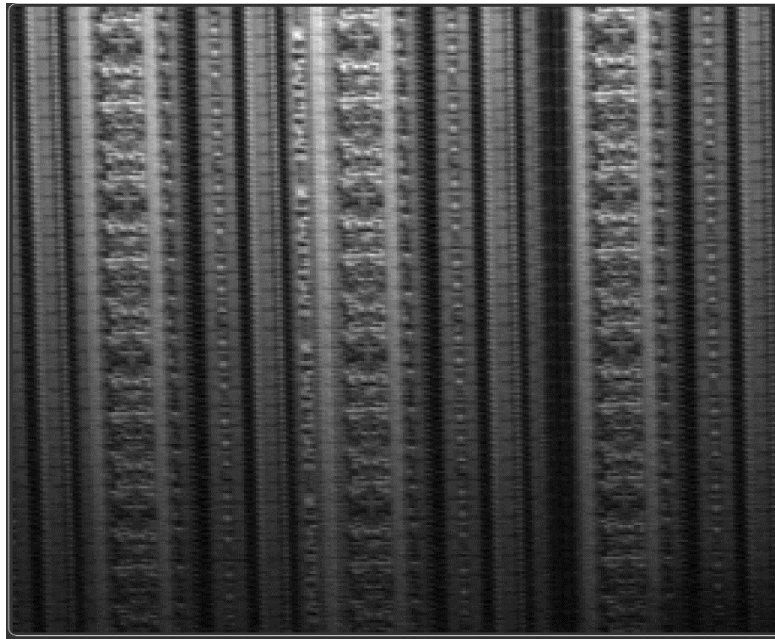
Table 6.3: Configuration bit errors with laser exposure time for different laser pulse energies at 96 x 96 μm scan area

Energy (pJ)	10s	30s	60s	2min	4min
100	0	0	0	0	0
200	0	0	0	0	0
300	0	0	1	2	8
350	5	17	29	49	65
400	22	51	72	105	129
500	128	187	198	222	225
600	115	135	168	202	232
700	627	778	836	880	888
800	965	1006	1003	1076	1098
900	1004	1069	1056	1048	1014
1000	1108	1111	1137	1125	1123

The configuration bit error data pattern obtained from the 96 x 96μm (table 6.3) is consistent with the 386 x 386 μm scan results, with the number of bit errors saturating at 900-1000pJ. Also from data, we can see that the bit error count value fluctuates with time near the saturation region (900 – 1000 pJ). This can be due to the same configuration memory bit getting upset more than once (even number of times) so that they are corrected back to their original stored bit values.

Table 6.4 show the configuration bit errors for 48 x 48 μm scan area. Based on the results, the bit error pattern was found to be different for the 48x48 μm scan compared to previous scan results.

Table 6.4: Configuration bit errors with laser exposure time for different laser pulse energies at 48 x 48 μm scan area

Energy (pJ)	10s	30s	60s	2min	4min
100	0	0	0	0	0
200	0	0	0	0	0
300	0	0	0	0	0
400	9	17	21	25	25
500	58	66	67	68	70
600	83	81	84	89	88
700	85	85	75	81	81
800	95	94	97	95	96
900	116	124	133	137	129
1000	260	251	251	258	240
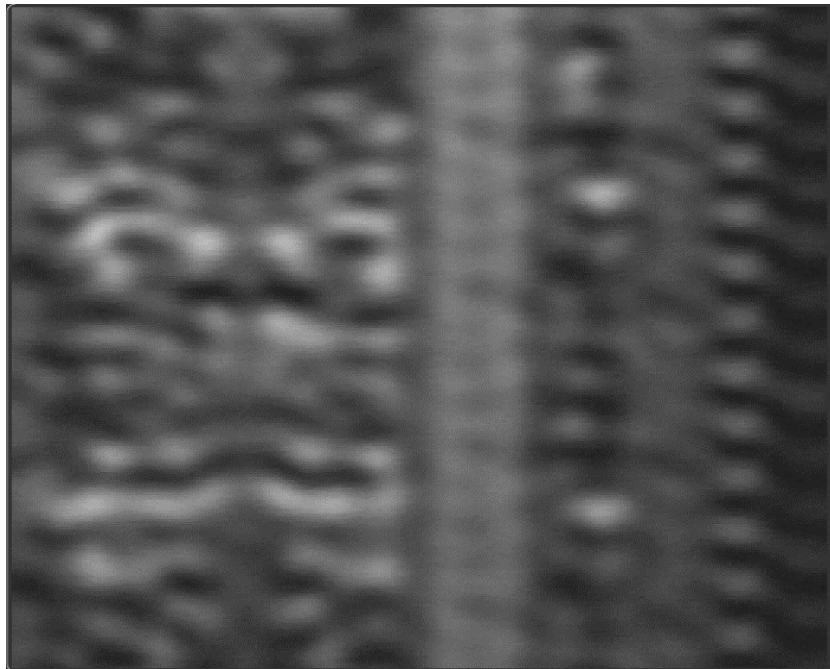
Figure 6.6: Configuration memory micrograph for laser scan area of 48 x 48 μm.

For the 48 x 48μm scan area, the bit errors quickly converged to a saturation value within 10 - 30 seconds of laser exposure. This can be due to reduced scan area such that the pulsed laser strikes the sensitive spot more frequently, compared to previous scans.

6.5 Cross Section Analysis

The cross section curve calculation for pulsed laser testing is similar to calculations done for heavy ion and proton radiation testing. Each laser pulse strike is in the order of femtoseconds, which can be considered as a single particle strike on the FPGA surface [41]. The total radiation fluence is calculated by [30].

Fluence = Number of pulses per second (pulse repetition rate) * Time of exposure / Area

Cross section = Number of bit errors observed / Fluence

Based on these parameters, the fluence was calculated to be 0.203 x 10^{12} p/cm^2.

The error cross section versus laser pulse energy of configuration memory is as shown in Figure 6.7. The cross section curve is calculated based on laser testing of the chosen scan area of 386 x 386 μm which was exposed to laser for 30 sec.

The cross section curve follow the same trend as the cross section curves from normal strike in 6T and 12T cell, shown in Figure 5.11.
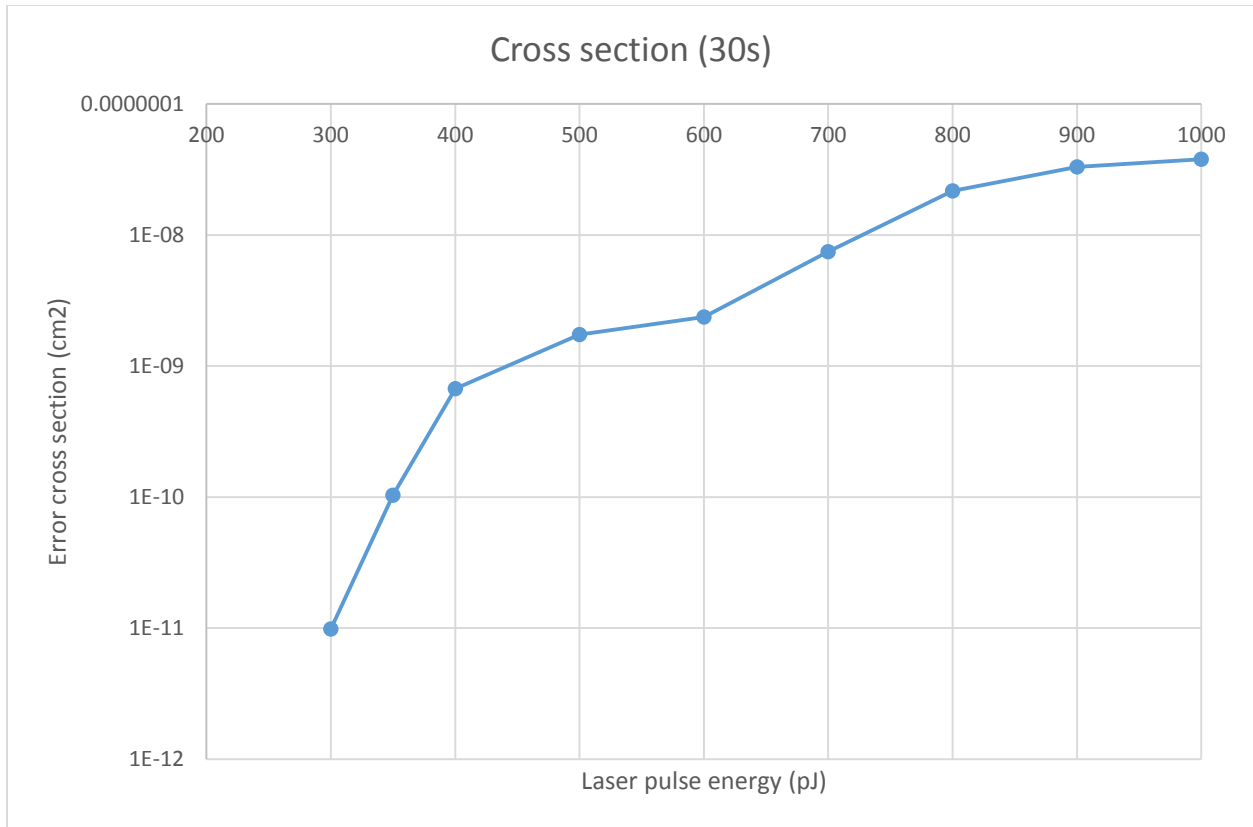
Figure 6.7a: Error cross section vs laser pulse energy of configuration memory

<u>Proton and heavy ion data correlation with laser</u>

The cross section curve corresponding to area per bit is also calculated as shown in Figure 6.8. The data is obtained by dividing the cross section curve in Figure 6.7a by the estimated number of configuration bits present in the scan area. Based on the scan results, the total number of memory elements were estimated to be 13000. The cross section per bit data helped us correlate the laser testing data with the proton test results conducted by Dave et al. [42] for Virtex-5 FPGA.
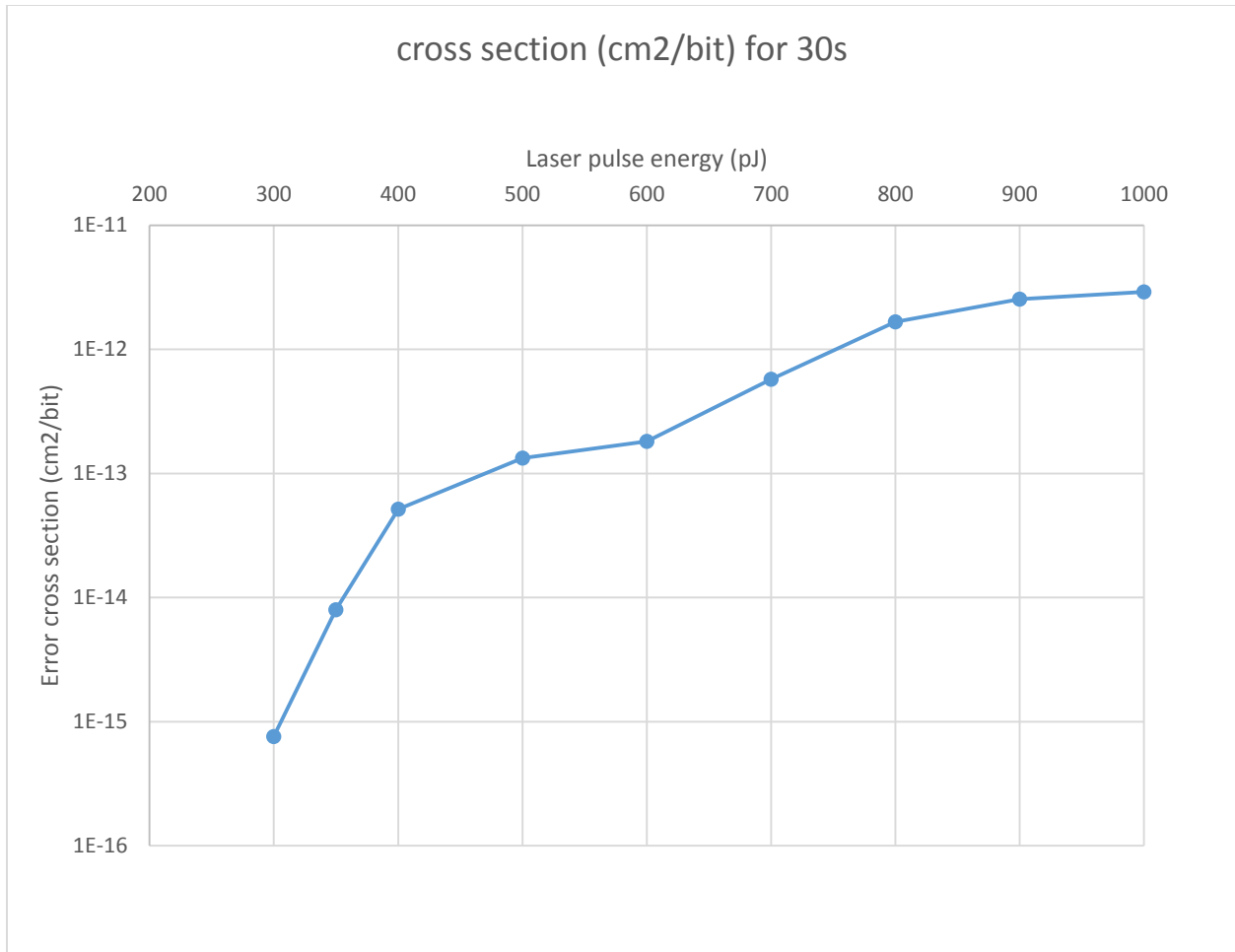
Figure 6.7b: Cross section per bit vs laser pulse energy of the configuration memory

In this investigations, the proton energies used for Virtex-5 testing corresponds to equivalent laser pulse energies around 350 pJ. Based on the proton testing, the SEU cross section was observed to be 1.95×10^{-14} cm^2/bit for configuration memories [42]. This correlates with the cross section curve data shown in Figure 6.7b where the error is in the order of 10^{-14}.

6.6 Test Results of Other Functional Blocks in the FPGA

6.6.1 Configurable logic blocks

Configurable logic blocks (CLB) are the main functional logic blocks used for building combinational and sequential logic in the FPGA. A CLB is split into smaller modules called slices. In Virtex-5 FPGA, each slice consists of a 6 input look up tables (LUT), flip flops and multiplexers. Slices also have dual-port RAM blocks that can be used as a distributed RAM memory.
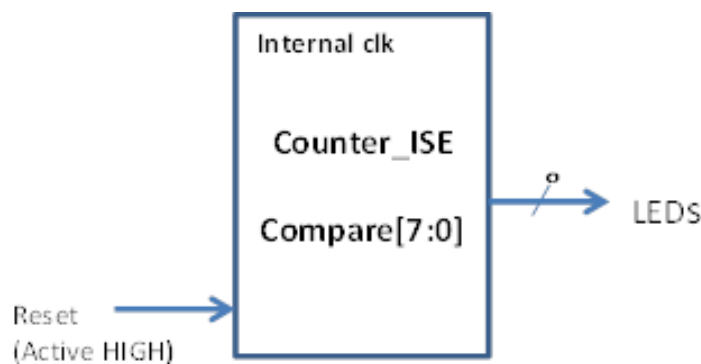
Figure 6.8: Functional block diagram of the counter code

There are 456-bit counters implemented in order to utilize the CLB blocks available in the FPGA. Each counter occupies one CLB column in the FPGA which makes the laser scanning process easier. Implementing counters using CLB is a standard technique for evaluating CLB SEU sensitivity, since it utilizes most of the functional units within the CLB.

The block diagram of the counter VHDL code is as shown in Figure 6.8. The counter code is divided into 8 sections where each section consists of three, 456 bit counters. The counters are controlled by an internal clock, making them count concurrently after power on. Only 8 bits of the counter (7 LSB bits and one MSB bit of the 456 bit counter) is taken as output for verification. This allows us to reduce the size of the comparator needed. The 8-bit outputs of the counters, within a section, are compared and a compare bit is generated which indicates the error in the

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counter. Figure 6.9 shows the detail functional diagram of a section. Provision for synchronous reset is also provided to reset all the counters to zero during operation.

Separate area constraints are given in the code to constrain counters into separate columns. Figure 6.10 shows the floor plan for the counter VHDL code in Virtex-5 FPGA. Additionally, each counter column is interleaved so that no two counters of the same section are adjacent to each other. This makes sure that the single event strike would not affect the counters in the same section simultaneously.

During the laser scanning process, the scan window is chosen so that only one counter chain is affected by the pulsed laser strike. This erroneous output of the counters can be detected using the comparator output bits (LED indication). The laser micrograph for the counter 1a, 2a and 3a are as shown in Figure 6.11. The position of IOB's and Block RAMs are also marked in the micrograph (red) as a landmark in the chip.
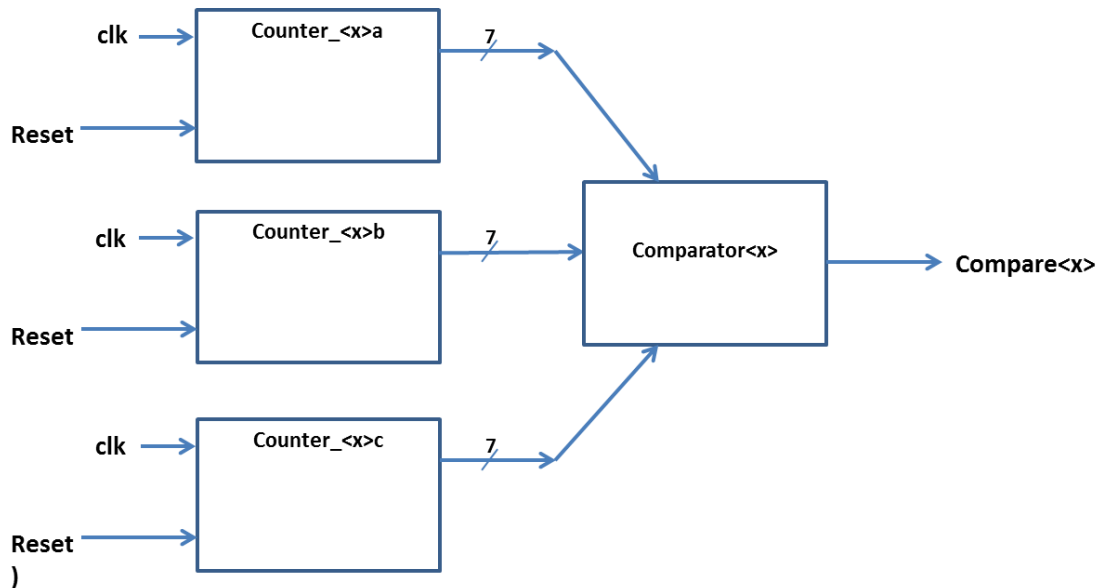
Figure 6.9: Functional diagram of counters and the comparator within a section
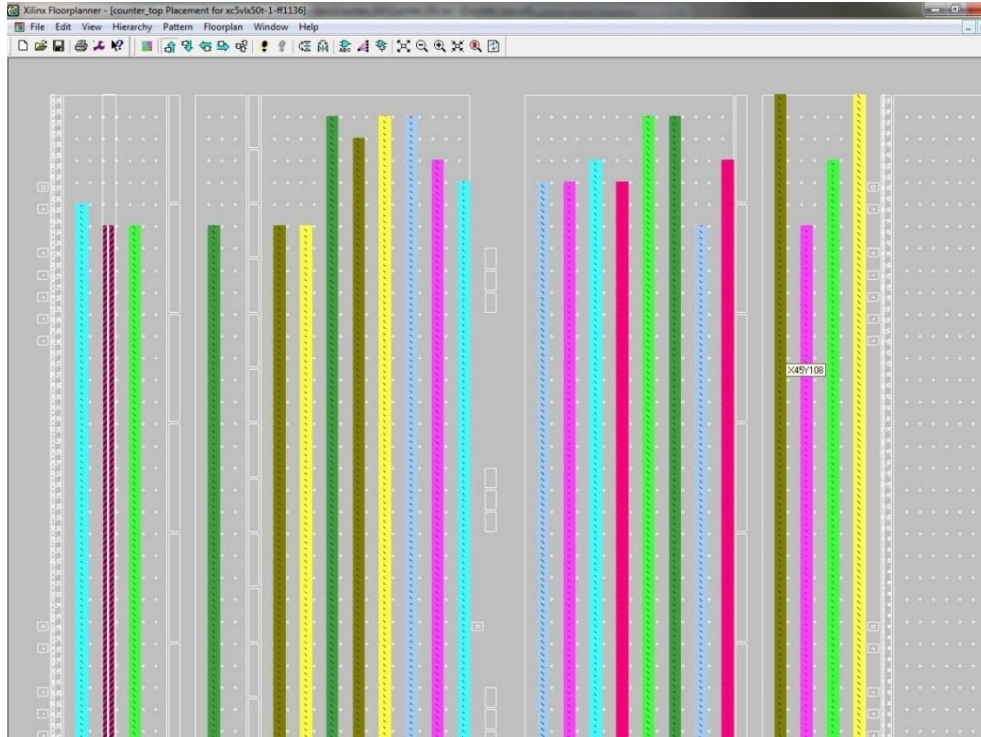
Figure 6.10: Xilinx floor planner layout of 456 bit counter modules arranged in columns
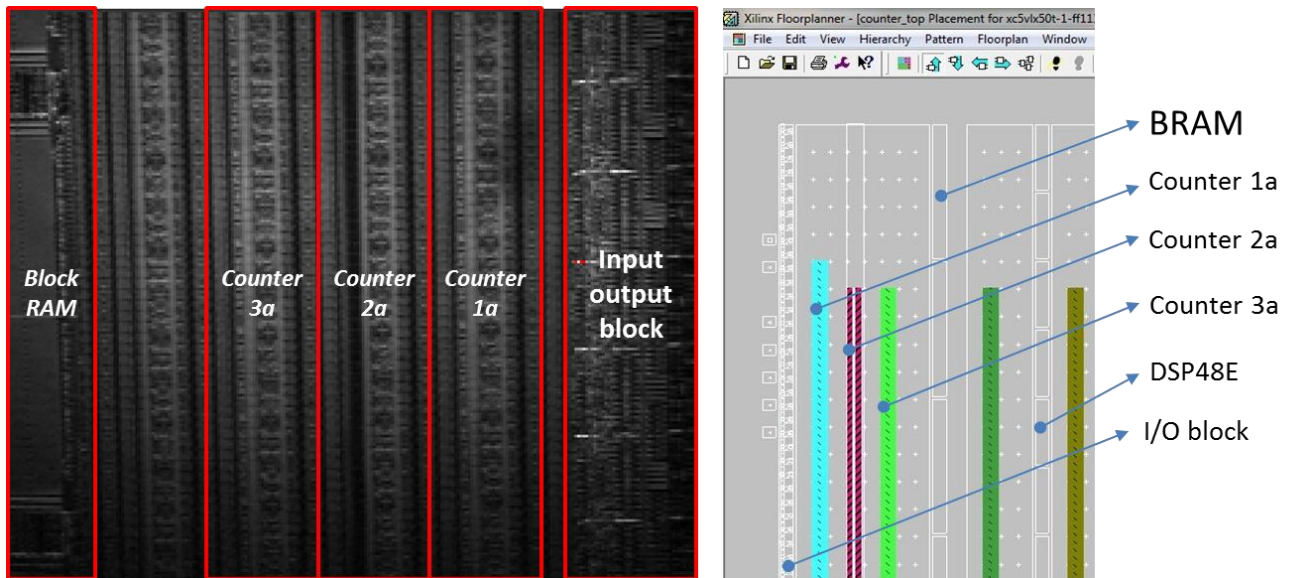
Figure 6.11: Laser micrograph showing counter 1a, 2a & 3a located in between the I/O logic and BRAM (768 x 768 μm) (right) shows the corresponding blocks in the Xilinx floor planner

Several configuration bits are affected during the scanning of counter columns, however all the

configuration bit errors do not lead to errors at counter output. For low pulse energies (300 to

500pJ), there are only few configuration bit errors, so that the errors accumulated rarely leads to upsetting of the counter. Hence the counter upsetting process for low energies can be considered as a long time process which again depends on the strike location and energy of the laser pulse. The long duration of laser exposure may gradually corrupt enough number of configuration bits so as to affect the counter. In this testing, the upsetting process is accelerated by applying higher pulse laser energies above 600pJ. This has led to rapid accumulation of configuration bit errors leading to the upsetting of the counter. The time taken to upset the counter for higher energies is given in Table 6.5.

Table 6.5: Counter error output for different laser pulse energies

Energy per Pulse (pJ)	Results for scan at 192 x 192 μm
600	Tested for 10 min, No LED output
700	LED lights up after 2min (1m53s to 2m30s)
800	LED lights up after 5-8 sec
900	LED lights up 2-6 sec

Compared to the configuration memory, the counters exhibited better tolerance to laser strikes. This can imply a higher SEU hardness for flip flops used in the CLB's. However, counters can be get corrupted from various mechanisms such as

1. Upsetting of a critical configuration bit that leads to corruption of counter output (SEFI).

2. Error introduced due to a Flip flop upset in the CLB.

3. Generation of SET at the output of combinational logic that gets latching at the Flip flop input.

Further investigations has to be done to determine the contribution of each individual blocks to the counter upset.

6.6.2 DSP48E blocks

Virtex-5 has dedicated DSP48E macro blocks for DSP functions. The DSP module consists of multiply and accumulate blocks, multipliers, barrel shifters and multiplexers. The DSP48E offers a dedicated block for implementing math functions and complex arithmetic needed for implementing various DSP operations. Figure 6.12 shows the DUT functional diagram of a DSP 48E VHDL code implemented.
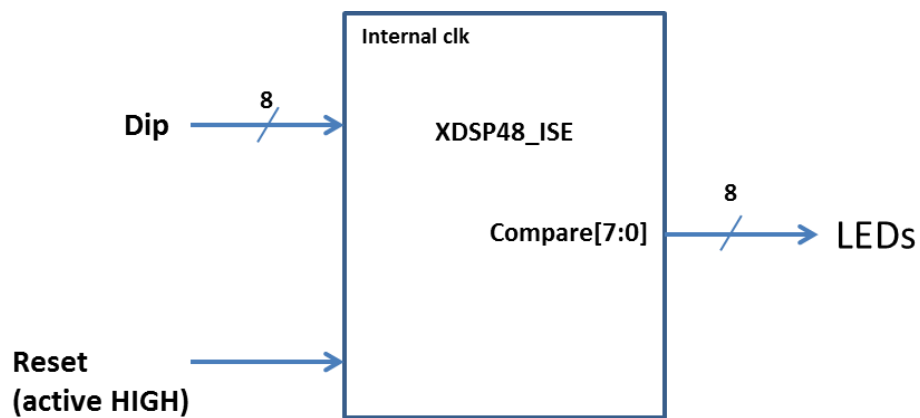
Figure 6.12: Functional block diagram of DSP48E Macro

Virtex-5 FPGA has got a single column dedicated for DSP blocks at the left side of the FPGA chip area as shown in Figure 6.13. The VHDL code uses 6 pairs of DSP48E blocks in this column. The DIP inputs are fed to all of the DSP blocks to make sure every DSP block is operating with the same input test conditions. The DSP block outputs are then compared within each pair and the compare bit is given out as an LED indication.

Laser testing was performed in 3 different scan areas as shown in figure 6.14 and 6.15. The testing results are given in Table 6.6.

Figure 6.13: DSP48 VHDL code floor plan, showing the DSP column (colored blocks) in the Virtex-5 FPGA.
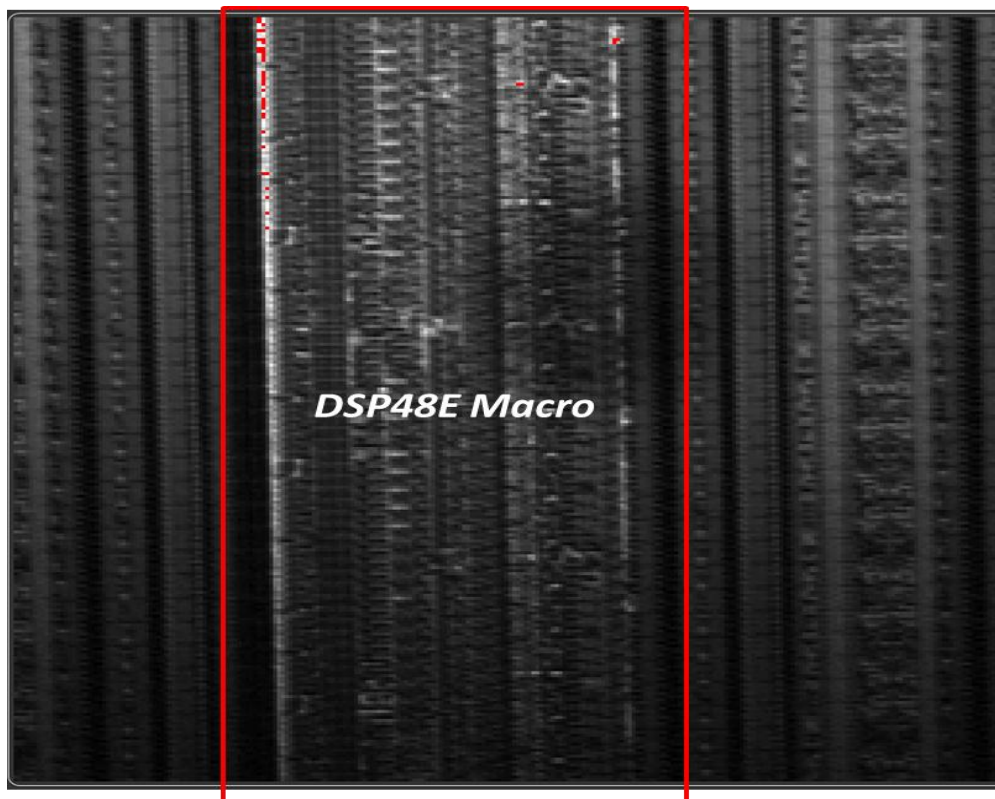
Figure 6.14: DSP 48E block 384 x 384 μm (marked in red) besides a CLB column on right
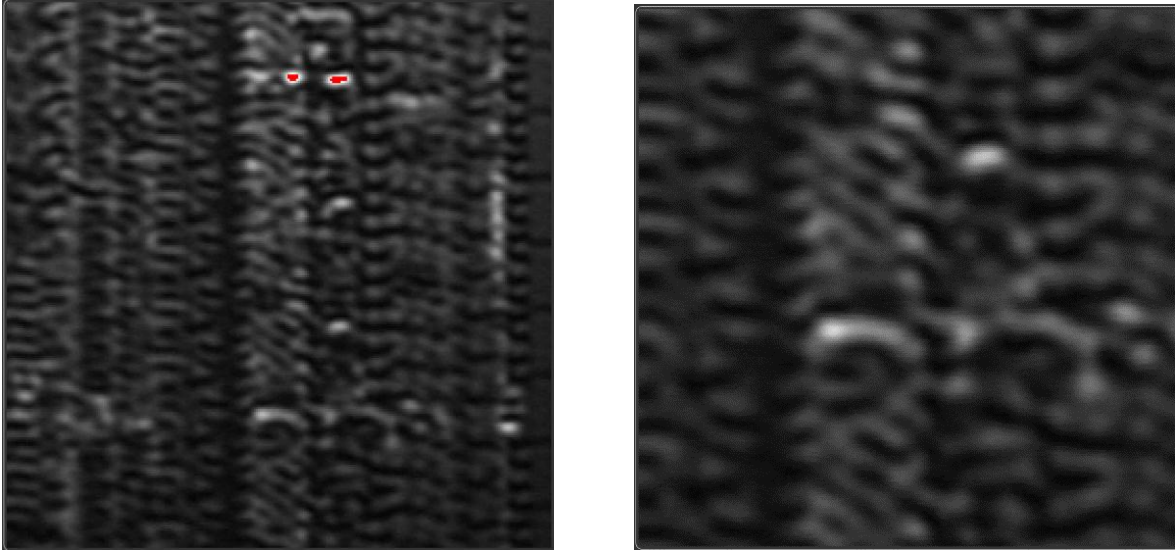
Figure 6.15. Laser micrograph of DSP48 (96 x 96 μm) (left) and 48 x 48 μm (right) scan area

Table 6.6: DSP48E upset vs laser exposure time for different scan areas and laser energies

Energy per Pulse (pJ)	Time after program when LED lights		
	386 x 386 μm	96 x 96 μm	48 x 48 μm
250	No upset	No upset	No upset
320	No upset	No upset	No upset
360	2-3 min	16-18 s	8 s
400	10 – 18 s	1 – 2 s	1-2 s
500	immediate	immediate	immediate

Based on the test results shown in Table 6.6, the DSP48E Macro block upsets at an energy level around 320 - 360pJ. This threshold is slightly higher than the upset threshold of the configuration memory (300 pJ).

6.6.3 <u>Block RAM</u>

Block RAM's (BRAM) provide high density storage apart from the distributed memory present in the CLB's of the FPGA. Virtex-5 consist of dedicated 36KB BRAMs, which can be used as a single 36KB block or 2 independent 18KB BRAM blocks [33]. In Virtex-5 LX50T, block RAM's are distributed as two columns along both sides of the FPGA chip.

The VHDL testing code uses 16 BRAMs (16 bit data, 10 bit address), located along a column of the FPGA, to work concurrently. The floor plan of the BRAM code is as shown in 6.18. The code employs data and address generators that generate data to be stored in a particular location of the BRAM memory. The data stored is same as the address location where it is stored. This makes it easy to verify the corruption of data when retrieving it.

The functional block diagram of the BRAM VHDL code is as shown in figure 6.16. The BRAM VHDL code works in 2 modes. In write mode, the binary values generated by the data generator are stored in the BRAM memory in sequential order. During laser scanning, the BRAM is set to read mode and the data is retrieved from memory locations. Additional error detection and counter circuits are used to count the number of bit errors encountered during the read back of each memory location. Finally, the errors are summed up together to get the total number of bit errors during the read back. Chip scope software is used to read the number of bit errors from the internal error counters of the FPGA. The error data read is then used to evaluate the single event tolerance of BRAM memory. Figure 6.17 shows the micrograph of BRAM, besides the CLB array.
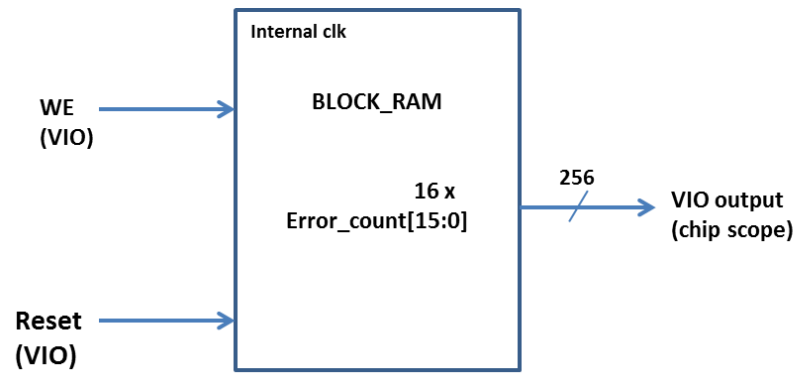
Figure 6.16: Functional block diagram of BRAM
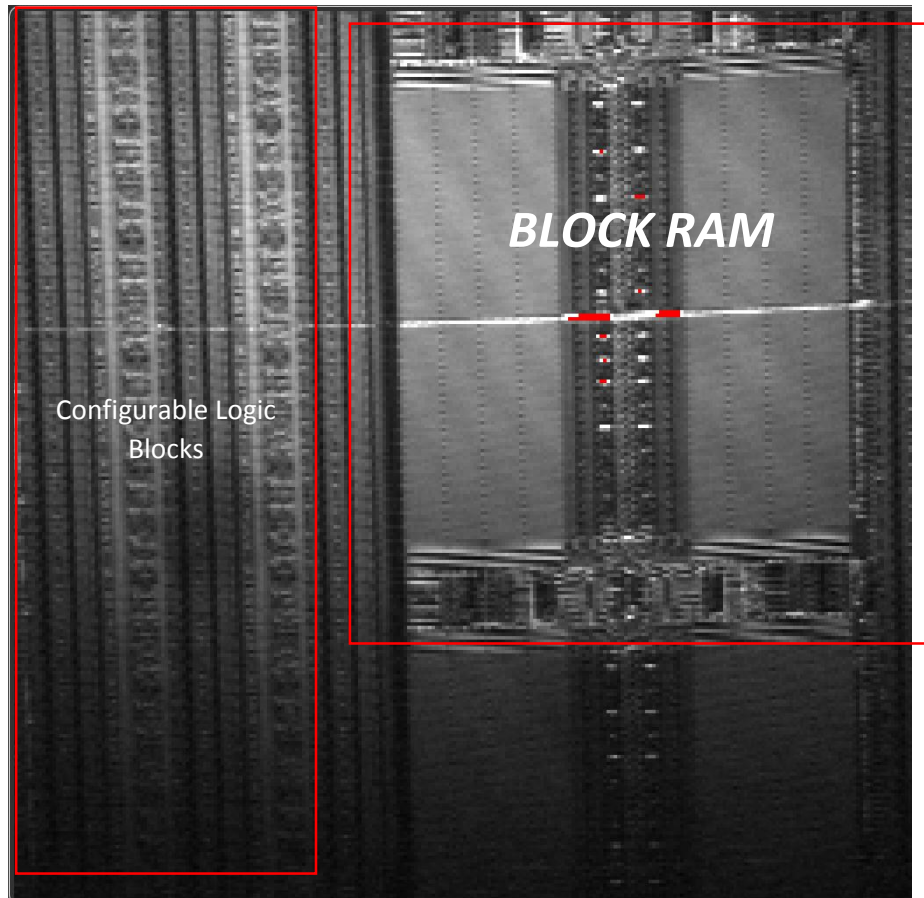
Figure 6.17: Laser micrograph of BRAM (768 x 768 µm)
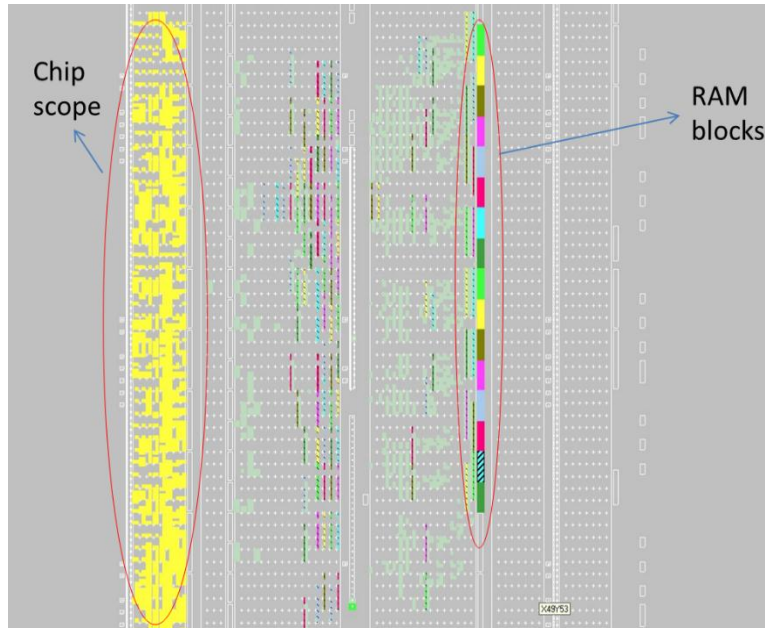
Figure 6.18: Floor plan of BRAM test code in Virtex-5 FPGA
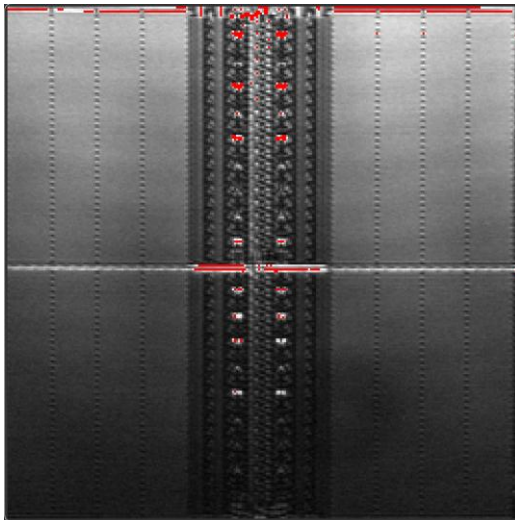
Energy (pJ)	Bit errors
250	0
325	6
400	15
475	33
550	97

Figure 6.19: Laser testing on 384 x 384 μm BRAM cell. Table 6.7 (right) BRAM bit errors vs energy of the pulse

Figure 6.19 shows the laser micrograph of the BRAM scan area where the laser test is performed.

From the table 6.7, the BRAMs have a threshold upset at around 300 - 325 pJ, which is almost

same as the upset threshold for configuration memories used in the FPGA. The bit errors for a read

operation at various laser energies are shown in table 6.7. The BRAMs tend to exhibit unstable

error outputs for longer exposure times and higher energies which can only be removed by reprogramming the FPGA. This phenomenon may be due to a functional interrupt that disrupts the normal function of the BRAM blocks.

6.6.4 Summary

TPA laser testing was done on Virtex-5 FPGA to evaluate the SEU tolerance. The summary of upset threshold energy for various functional blocks in the FPGA is shown in Table 6.8.

Table 6.8: Threshold upset energy for various functional blocks of the FPGA.

Functional blocks	Threshold energy
Configuration memory	295 pJ
DSP48E Block	360 pJ
BRAM	325 pJ
Counters	700 pJ

From the laser investigations, it shows that the SRAM-based configuration memories are the most vulnerable functional blocks in the FPGA. Error cross section analysis is performed for SRAM based configuration memories to evaluate and understand the single event error characteristics. For the configuration memory, the laser scan parameters were chosen so that the laser would take 60 seconds to strike all the pixels within the scan window. As expected, the bit errors reach their saturation values at 60 seconds for 386 x 386 μm and 96 x 96 μm scans. For 48 x 48um scan, the bit errors converged to their saturation values before 60 seconds, because of the laser scan window being focused on to the sensitive area of the configuration memory cell. Additionally, for the smaller scan areas, the bit errors were found to decrease after reaching their saturation values. This can be due to the laser pulse striking the memory cells twice (even number of times) so as to flip the cell back to their original values. The results are comparable to the simulation results obtained for 6T and 12T SRAM designs using Accuro.

Chapter 7

7. <u>Conclusion</u>

The 12T SRAM cell based on novel layout technique is proposed to improve the SEMU radiation tolerance of the 6T SRAM cell. The layout technique introduces interleaving of diffusion nodes, which has proved effective in improving SEMU tolerance of the 6T SRAM cell design. During horizontal and vertical SEMU strike, the charge deposited at the diffusion nodes are cancelled out due to the arrangement of NMOS and PMOS nodes in the layout. As per the Accuro 3D simulations, the proposed new cell improves the SEMU tolerance level of the cell by up to 22X. The dual redundancy layout technique employed in the design improves the critical node capacitance of the cell compared to its 6T cell counterpart by 5fC without any area overhead. This has improved the single-node tolerance of the cell. The comparison of sensitivity map of 6T and 12T cell in 3 major axis (X, Y, Z axis) reveals a significant reduction in vulnerable areas in the proposed 12T cell design. The 12T cell has lower error cross section area for normal strikes (Y plane) and vertical strikes (X axis) compared to the 6T cell. However, a slight anomaly was observed in the horizontal radiation strikes. For lower LET values (LET < 25 MeV-cm^2/mg), cross section of the 6T cell was slightly better than proposed design. But for higher LET values (LET > 25 MeV-cm^2/mg), 12T cell has got better cross section results.

A novel approach for testing Virtex-5 FPGA using two photon laser is introduced. The TPA laser testing of FPGA helped understand the SEU tolerance of SRAM based configuration memory cells and various other functional block used in the FPGA. The cross section curve for configuration memories reveals a similar trend as the 6T and 12T SRAM cross section curves that were obtained from Accuro simulations. The laser scan parameters was chosen so that the laser would take 60 seconds to strike all the pixels within the scan window. As expected, the bit errors reach their saturation values at 60 seconds for 386 x 386 μm and 96 x 96 μm scans. For 48 x 48um scan, the bit errors converged to their saturation values before 60 seconds, because of the laser scan window being focused on to the sensitive area of the configuration memory cell. Additionally, for smaller scan areas, the bit errors were found to decrease after reaching their saturation values. This can be due to the laser pulse striking the memory cell twice (even number of times) so as to flip the cell back to its original value. The cross section per bit results obtained from TPA laser testing of the configuration memory correlates with the proton test results performed by Dave et al. [42].

The upset threshold energy analysis of all the functional blocks in the FPGA show that the configuration memories in the FPGA are the most vulnerable blocks towards ion strikes. Hence techniques like configuration memory scrubbing and redundancy schemes has to be employed to improve the configuration memory SEU tolerance.

7.1 <u>Future work</u>

In future, the proposed 12T cell will be implemented in 28nm nanometer technology which will give an idea about the radiation tolerance characteristics of the proposed design in an advanced CMOS technology. In the new technology, the PMOS / NMOS optimum ratio has to be investigated because of variation in mobility of PMOS and NMOS diffusion regions. Radiation tolerance of the 12T cell can then be simulated for angular strikes at various grazing angles. Finally, a 32KB SRAM based on the proposed cell will be fabricated in 28nm, and radiation testing will be performed to verify the SEU performance of the design. Heavy ion, proton and TPA based laser testing can performed to verify and correlate the SEU characteristics of the proposed 12T cell design.

Currently, the configuration memory tests in Virtex-5 FPGA reveal the total number of configuration bits upset which include both SBU's and MBU's. The configuration bit values can be read back to identify the pattern of upsets formed in the scanned area. The data can then be grouped based on localization of upset bits to identify the SBU and MBU upset patterns in them. This can help identify the dominant mechanism that results in the SEU bit error rate. Furthermore, studies can be done to identify the upset threshold of flip flops and look up tables (LUT) present within the CLB of the FPGA. This can help understand the LET threshold of individual units and their contribution to SEU tolerance of the CLB block.

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