A Q-ENHANCED 3.6 GHZ TUNABLE CMOS BANDPASS FILTER FOR WIDEBAND WIRELESS APPLICATIONS

A Thesis Submitted to the College of

Graduate Studies and Research

In Partial Fulfillment of the Requirements

For the Degree of Master of Science

In the Department of Electrical Engineering

University of Saskatchewan

Saskatoon

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March 2004

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ABSTRACT

With the rapid development of information technology, more and more bandwidth is required to transmit multimedia data. Since local communication networks are moving to wireless domain, it brings up great challenges for making integrated wideband wireless front-ends suitable for these applications. RF filtering is a fundamental need in all wireless front-ends and is one of the most difficult parts to be integrated. This has been a major obstacle to the implementation of low power and low cost integrated wireless terminals.

Lots of previous work has been done to make integrated RF filters applicable to these applications. However, some of these filters are not designed with standard CMOS technology. Some of them are not designed in desired frequency bands and others do not have sufficient frequency bandwidth. This research demonstrates the design of a tunable wideband RF filter that operates at 3.6 GHz and can be easily changed to a higher frequency range up to 5 GHz. This filter is superior to the previous designs in the following aspects: a) wider bandwidth, b) easier to tune, c) balancing in noise and linearity, and d) using standard CMOS technology.

The design employs the state-of-the-art inductor degenerated LNA, acting as a transconductor to minimize the overall noise figure. A Q-enhancement circuit is employed to compensate the loss from lossy on-chip spiral inductors. Center frequency

and bandwidth tuning circuits are also embedded to make the filter suitable for multi band operations.

At first, a second order bandpass filter prototype was designed in the standard 0.18 μm CMOS process. Simulation results showed that at 3.6 GHz center frequency and with a 60-MHz bandwidth, the input third-order intermodulation product (IIP3) and input-referred 1 dB compression point (P1dB) was -22.5 dBm and -30.5 dBm respectively. The image rejection at 500 MHz away from the center frequency was 32 dB (250 MHz intermediate frequency). The Q of the filter was tunable over 3000 and the center frequency tuning range was about 150 MHz.

By cascading three stages of second order filters, a sixth order filter was designed to enhance the image rejection ability and to extend the filter bandwidth. The sixth order filter had been fabricated in the standard 0.18 μm CMOS process using 1.8-V supply. The chip occupies only 0.9 mm × 0.9 mm silicon area and has a power consumption of 130-mW.

The measured center frequency was tunable from 3.54 GHz to 3.88 GHz, bandwidth was tunable from 35 MHz to 80 MHz. With a 65 MHz bandwidth, the filter had a gain of 13 dB, an IIP3 of -29 dBm and a P1dB of -46 dBm.

ACKNOWLEDGMENTS

This is the moment, I believe, for me to express my gratitude to those who helped me and supported me through out my Master's study and research.

I would like to express my gratitude to my supervisor, Professor Anh Dinh, for his constant support and guidance during the research work. His suggestion and encouragement helped me to overcome the difficulties and obstacles encountered in the research. Without his help, I could not have completed this research.

I would also like to thank CMC who provided the design environment and technical support. They funded the chip fabrication and made the design meaningful.

I wish to thank TRlabs for providing the test equipment. I would also wish to thank the laboratory technician Vic Meyer for his technical support in making the PCB board and Garth Wells (TRLabs) for his assistance in setting up the test environment and for making the suitable balun for testing.

Finally, I wish to thank my parents and my wife Dongmei Fang for their endless support in my life and for helping me get through my postgraduate studies. Special thanks are given to my lovely daughter Emily.

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LIST OF ABBREVIATIONS

Abbreviation	
A/D	analog to digital
ADS	advanced design system (simulation software from Agilent)
A_{IP3}	amplitude of input referred 3rd order intermodulation point
BiCMOS	bipolar complementary metal-oxide semiconductor
BPF	bandpass filter
BW_{3dB}	3 dB bandwidth
C_{gs}	gate-source capacitance
C_{gsx}	extra gate-source capacitance
C_j	junction capacitance
C_{ox}	oxide intrinsic capacitance
CMC	Canadian Microelectronics Corporation
CMOS	complementary metal oxide semiconductor
CTM	cap_top_metal
DR	dynamic range
DRC	design rule check
DSP	digital signal processor
EPI (epi)	epitaxy process (used on an “EPI substrate”)
f	frequency

F	noise factor
f_0	center frequency, resonance frequency
F_{sys}	system noise factor
f_T	transit frequency (unit gain frequency)
G	gain
GaAs	gallium arsenide
g_{d0}	zero bias drain-source conductance
G_m (g_m)	transconductance
HBT	hetero junction bipolar transistor
Hz	hertz
IC	integrated circuit
IF	intermediate frequency
IP_3	third-order intermodulation product
IIP3	input referred 3^{rd} order intermodulation point
ISM	industrial scientific medicine
k	Boltzmann's constant
L	transistor length
L_g	inductor connected to the gate of an LNA input transistor
L_s	inductor connected to the source of an LNA input transistor
LC	passive network made out of inductors and capacitors
LNA	low noise amplifier
LO	local oscillator
MOS	metal oxide semiconductor

MOSFET	metal oxide semiconductor field effect transistor
MDS	minimum detectable signal
MESFET	metal extrinsic semiconductor field effect transistor
MIM	metal-insulator-metal (capacitor)
N_f	noise floor
NF	noise figure
PA	power amplifier
PCB	printed circuit board
PWB	printed wire board
Op amp	operational amplifier
PGS	patterned ground shield
pHEMT	pseudomorphic high-electron-mobility transistor
Q	quality factor
R_{eq}	equivalent parallel resistance of the resonant tank
RF	radio frequency
RLC	passive network made out of resistor, inductors and capacitors
R_P	resistance loss of the LC tank
R_{poly}	sheet resistance of the polysilicon material
R_s	source resistance
R_g	parasitic transistor gate resistance
S	signal power, power spectral density
SAW	surface acoustic wave
SiGe	silicon germanium

SNR	signal-to-noise ratio
SOI	silicon on insulator
t_{ox}	thickness of the oxide layer
V_{eff}	effective gate to source voltage
V_{GS}	transistor gate to source voltage
V_R	reverse voltage
V_T	threshold voltage
W	transistor width, metal width
Y	admittance
Z	impedance
Z_{Tank}	tank impedance

LIST OF SYMBOLS

Symbols

α	MOS transconductance degradation factor
ε_0	electrical permittivity in free space
ε_r	relative permittivity
δ	MOS gate noise constant, skin depth
σ	permeability of free space
θ	MOS mobility degradation fitting parameter
Δf	frequency bandwidth, noise bandwidth, frequency spacing
γ	MOS drain noise constant
μ_n	effective surface mobility of an NMOS device
ω	frequency in radians
ω_0	center frequency, resonance frequency in radians

CHAPTER 1 INTRODUCTION

This chapter serves as an introduction to integrated RF circuits and integrated RF filtering in wireless communication front-ends. The first section explains why integrated RF filters are required, current progress in integrated RF filter design and the problems that remain. Section 2 illustrates some of the technical challenges in implementing wideband CMOS RF filters. Section 3 highlights the contributions of this research work. Section 4 gives the thesis outline.

1.1 Motivation

Traditional radio transceiver front-ends include analogue components such as RF filters, low-noise amplifiers, mixers, IF filters and power amplifiers. Each circuit component is implemented with specialized analogue process technologies such as GaAs pHEMT, GaAs MESFET, hetero junction bipolar transistor (HBT) and SiGe BiCMOS [1]. Most transceivers today are implemented with two chips, one is the integrated RF front-end using one of the above analogue technologies, and the other is the baseband back-end which is implemented using CMOS technology. CMOS is now the most popular technology in digital design. It is used for band processors and memory in wireless communication terminals [2]. Three important advantages of CMOS are its high integration level, low cost, and low power consumption. If the RF front-end needs to be integrated into a single chip with the baseband, CMOS would be the best

choice. However active devices in CMOS technology exhibit lower unity-gain frequencies and lower transconductance than the analogue technologies mentioned above. In addition, due to the lossy substrate of CMOS, the noise performance is much worse than other technologies and the high quality passive components are not available. These factors make it very difficult to integrate RF front-ends using CMOS technology. The rapid advancement in deep sub-micron CMOS technology and the continuous downscaling in CMOS device size have made low-cost and small-size implementation of CMOS RF integrated circuits more and more feasible [3], [4]. More recently, many analogue circuits have been integrated using low power, cost effective CMOS technology to meet the fundamental needs for radio reception [5]-[7]. In order to reduce cost and power consumption of the wireless communication systems, a single chip transceiver in which the integrated RF filtering is an essential part is the ultimate solution.

RF filtering is a fundamental need in wireless communications. The RF filter is usually the first block in the transceiver after the antenna and it is used to filter out the out-of-band blocking signals and to improve the selectivity of the receiver. Unfortunately the RF filter is one of the most difficult parts of the RF transceiver to be integrated due to the lack of high quality passive components in CMOS technology. Much work has been done in the area of integrated filters. Most of these filters are narrow band second order filters, some high order filters either do not have enough bandwidth or do not work at frequency in the gigahertz range. With the development of the wireless personal communication systems, there is an increasing demand for RF front-ends working at wider bandwidths and higher center frequencies. For example,

Bluetooth needs 100 MHz bandwidth at a 2.4 GHz center frequency [8]. The lack of integrated wideband RF front-end filter becomes a big obstacle for the single chip solution of the transceiver. There are some technology challenges that need to be overcome before wideband RF filters can be integrated using CMOS technology. These challenges are described in the next section.

1.2 Technical Challenges

Usually passive filters can not be integrated using CMOS technology because the on-chip inductors have very low quality factor (typically 2-4 in the standard CMOS technology) and thus the use of on-chip passive filter inhibits a huge insertion loss. On the other hand, active filters are not linear and usually can not operate in the GHz range.

In recent years, the CMOS technology has improved tremendously in analogue (RF) circuit design. By shrinking the length to less than one-tenth of a micrometer, unity gain frequencies (f_T) of the transistor have exceeded 100 GHz [9]. The poly resistors, MIM capacitors and thick top layer metal inductors also provide relatively high quality passive components [4], [9].

On-chip spiral inductors have emerged in the CMOS substrate for more than a decade, but their quality factor is still in the low end. These low Q inductors dominate the loss in the LC resonator and greatly contribute into the loss of the on-chip LC filters [10]. In order to improve frequency selectivity and to reduce noise, it is required to keep the resonator loss as low as possible. In order to improve the quality factor of the on-chip inductor, a loss compensation technique must be employed. By using loss compensation techniques, the Q of on-chip inductors can be tuned very high and thus brings the possibility of implementing on-chip LC filters [11], [12]. These loss

compensation circuits usually consist of active devices and thus degrade the overall filter linearity and noise performance. In other words, research in loss compensation with high linearity and low noise is extremely important.

In order to fit into the multi-band RF systems, wide frequency tuning range of the RF filters is also required. At the same time, because of the lack of the precise models of the on-chip inductors and varactors, extra frequency tuning range for the design margin is required. The design of a wide tuning range and high quality varactor in the CMOS technology is also a great challenge [13].

The wideband wireless communication systems require wideband RF filters. The wideband filter with good selectivity can be implemented with higher order filters, the simplest way is to cascade several stages of the second order filters together (i.e., ladder filter) [14]. However, in order to acquire designed frequency response, the values of the inductors and capacitors must be very accurate; this is not possible in CMOS technology. As the result, new filter architecture must be found to implement the wideband solution without using precise passive components. Another drawback of the traditional high order LC filters is that it is very difficult to tune; the new filter architecture also needs to simplify the tuning scheme.

In summary, the research work is to achieve a low noise, high linearity CMOS wideband RF filter with a wide tuning range and a simple tuning scheme.

1.3 Contributions

This research work makes some contributions to the field of RF filtering in CMOS transceivers. The contributions are the design of a high Q inductor in the standard CMOS on low resistive substrates, research on improving the linearity of the

filter, and the exploration of the new architecture to implement wideband RF filter. The new architecture does not require the precise value of capacitors and makes the filter performance more predictable and reliable. This research work also finds a tuning scheme that greatly simplifies the tuning of the high order filter and makes the filter more applicable to commercial products.

1.4 Thesis Outline

Some background knowledge in RF circuit design is presented in Chapter 2. The chapter includes some basic RF fundamentals: noise figure, linearity, sensitivity and dynamic range and quality factor of the RF filters. The chapter also discusses radio receiver architectures, general filter requirements and common filtering solutions.

Chapter 3 covers the second order differential filter design, which include input LNA design, second order resonator design, noise analysis and linearity considerations. The chapter also includes the sixth order bandpass filter design based on the second order filters.

Chapter 4 presents the layout of the circuit components which includes the layout of a LNA, an inductor, capacitors and a Q-enhancement circuit. The chapter also discusses the floor planning of the layout.

Chapter 5 demonstrates the simulation and measurement results. This chapter also compares the results from simulation and measurement; with the difference being explained.

Chapter 6 presents the conclusion of the thesis.

CHAPTER 2 BACKGROUND

This chapter provides background information to the field of RF and RF filtering. The first section describes some basic RF fundamentals. The second section presents some different radio receiver architectures and explains how these architectures affect the RF filter requirements. Section 3 describes some general filter requirements. An example of the Bluetooth RF filter requirements is included in this section. The requirements for the proposed RF filter are also set in this section. In Section 4, some common filtering solutions are presented. This section also discusses the proposed filter architecture.

2.1 Basic RF Fundamentals

In this section, some of the useful parameters for measuring RF circuit performances, such as noise figure, third-order intermodulation distortion, 1 dB compression point and quality factor are introduced.

2.1.1 Noise figure (NF)

The signals received at the antenna are very weak and have to be amplified in order to drive the mixer. In order not to further deteriorate the signal to noise ratio (SNR) of the received signal, the following circuits should be designed to add as little noise as

possible especially at the front end of the receiver. Noise factor is a measure of the amount of noise added after the signal goes through a circuit. The noise factor is defined as the input signal to noise ratio divided by output signal to noise ratio (shown in Eq. 2.1). Another expression of noise factor can be found in Eq. 2.2 [15].

$$F = \frac{S_i / N_i}{S_o / N_o} = \frac{SNR_{in}}{SNR_{out}} \tag{2.1}$$

$$F = \frac{S_i}{N_i}\frac{(N_i G + N_{c,o})}{S_i G} = 1 + \frac{N_{c,o}}{N_i G} = 1 + \frac{N_{c,i}}{N_i} \tag{2.2}$$

where $N_{c,o}$ is noise generated by the circuit's components. $N_{c,i}$ is the input-referred noise of $N_{c,o}$ and equals to $N_{c,o}/G$. G is the circuit gain and N_i is the source noise power. Noise figure (NF) is usually expressed in log scale (dB) and the noise factor (F) is its corresponding value in linear scale. In this dissertation, the noise performance is evaluated in terms of noise figure. The relationship between the noise figure and the noise factor is as follow:

$$NF = 10\log(F) \tag{2.3}$$

2.1.2 Linearity

Ideally, when the input is a sinusoid signal, the input-output relationship of a linear, time-invariant system can be modeled as:

$$y(t) = a_1 x(t) \tag{2.4}$$

where x(t) and y(t) are the input and output of the linear system. But, due to non-linearity of the active devices, the input-output relationship is changed to be:

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \ldots \tag{2.5}$$

The coefficients a_2, $a_{3\ldots}$ provide information on the non-linearity of a device

or of a circuit. When a sinusoidal signal x(t)=Acos(ωt) is applied to the system in Eq. 2.5, the output y(t) is:

$$y(t) = \frac{a_2 A^2}{2} + \left(a_1 + \frac{3a_3 A^2}{4} \right) A\cos(\omega t) + \frac{a_2 A^2}{2}\cos(2\omega t) + \frac{a_3 A^3}{4}\cos(3\omega t) + \ldots \quad (2.6)$$

From Eq. 2.6, the output contains not only the fundamental frequency term, but also many higher order harmonics caused by $x^2(t)$ and $x^3(t)$ and so on. Typically, high-order terms are negligible when the input signal level is small. However as the input amplitude becomes large, the high-order terms increase rapidly and significantly affect the output. If the circuit is implemented in a fully differential architecture, the even-order harmonics will be mostly canceled out and can be neglected (shown in Fig. 2.1 and Eq. 2.7).

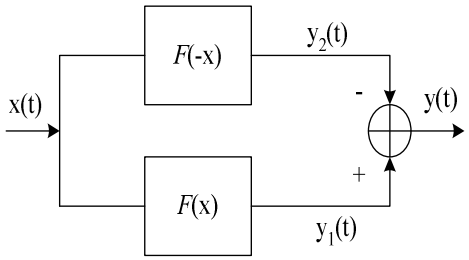

Fig. 2.1 Signal through a differential mode system

$$\begin{aligned} y_1(t) &= a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \ldots \\ y_2(t) &= -a_1 x(t) + a_2 (-x(t))^2 - a_3 x^3(t) + \ldots \\ y(t) &= y_1(t) - y_2(t) = 2a_1 x(t) + 2a_3 x^3(t) + \ldots \end{aligned} \quad (2.7)$$

When a sinusoidal signal x(t)=Acos(ωt) is applied to the system of Fig. 2.1, the output y(t) is:

$$y(t) = \left(2a_1 + \frac{3a_3 A^2}{2} \right) A\cos(\omega t) + \frac{a_3 A^3}{2}\cos(3\omega t) + \ldots \quad (2.8)$$

As seen from Eq. 2.8, there is no second order frequencies terms remained at

the output.

There are two important parameters used to measure the performance of linearity, that is the 1 dB compression point (P1dB) and the third-order intermodulation distortion (IP3).

2.1.2.1 1 dB compression point

The 1 dB compression point is defined as the input signal amplitude at which the output deviates from the ideal response by 1 dB. Fig. 2.2 illustrates the concept of this parameter. In Eq. (2.6), the first-order coefficient includes two terms, the desired gain a_1, and the undesired term $3a_3A^3/4$. For a small input amplitude A, the first term dominates and the output is linearly dependent on the input. However, due to non-linearity, when the input signal amplitude is large, the third order term increases rapidly and the gain of the fundamental frequency will drop off.

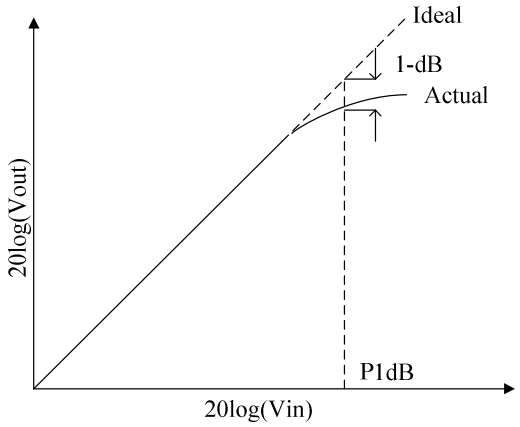

Fig. 2.2 1 dB compression point

2.1.2.2 Third-order intermodulation distortion

Another key parameter to evaluate the linearity of a circuit is the intermodulation distortion. When two closely spaced signals $x_1(t) = A_1 \cos(\omega_1 t)$ and

$x_2(t) = A_2\cos(\omega_2 t)$ mix with each other, they produce a signal with frequencies other than the high-order harmonics of the two signals.

$$
\begin{aligned}
y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \ldots &= a_2 \frac{A_1^2}{2} + a_2 \frac{A_2^2}{2} \\
&+ \left[a_1 A_1 + \frac{3}{4} a_3 A_1 (A_1^2 + 2A_2^2) \right] \cos(\omega_1 t) \\
&+ \left[a_1 A_2 + \frac{3}{4} a_3 A_2 (2A_1^2 + A_2^2) \right] \cos(\omega_2 t) \\
&+ a_2 \frac{A_1^2}{2} \cos(2\omega_1 t) + a_2 \frac{A_2^2}{2} \cos(2\omega_2 t) \\
&+ a_2 A_1 A_2 \cos\left[(\omega_1 + \omega_2)t\right] + a_2 A_1 A_2 \cos\left[(\omega_1 - \omega_2)t\right] \\
&+ \frac{3}{4} a_3 A_1^2 A_2 \cos\left[(2\omega_1 - \omega_2)t\right] + \frac{3}{4} a_3 A_1^2 A_2 \cos\left[(2\omega_1 + \omega_2)t\right] \\
&+ \frac{3}{4} a_3 A_1 A_2^2 \cos\left[(\omega_1 + 2\omega_2)t\right] + \frac{3}{4} a_3 A_1 A_2^2 \cos\left[(\omega_1 - 2\omega_2)t\right] \\
&+ \frac{1}{4} a_3 A_1^3 \cos(3\omega_1 t) + \frac{3}{4} a_3 A_1 (A_1^2 + 2A_2^2) \cos(\omega_1 t) \\
&+ \frac{1}{4} a_3 A_2^3 \cos(3\omega_2 t) + \frac{3}{4} a_3 A_2 (2A_1^2 + A_2^2) \cos(\omega_2 t)
\end{aligned}
\tag{2.9}
$$

The most severe distortion is called the third-order intermodulation due to the non-linear x^3 term. As seen from Eq. 2.9, the output will consist of fundamental frequency terms $\cos\omega_1 t$, $\cos\omega_2 t$ and the third order intermodulation frequency terms $\cos(2\omega_1+\omega_2)t$, $\cos(2\omega_2+\omega_1)t$, $\cos(2\omega_1-\omega_2)t$ and $\cos(2\omega_2-\omega_1)t$. Two strong interferers $A_1\cos(\omega_1 t)$ and $A_2\cos(\omega_2 t)$ can generate in-band distortion components $\frac{3}{4} a_3 A_1^2 A_2 \cos\left[(2\omega_1 - \omega_2)t\right]$ and $\frac{3}{4} a_3 A_1 A_2^2 \cos\left[(2\omega_2 - \omega_1)t\right]$ (shown in Fig. 2.3).

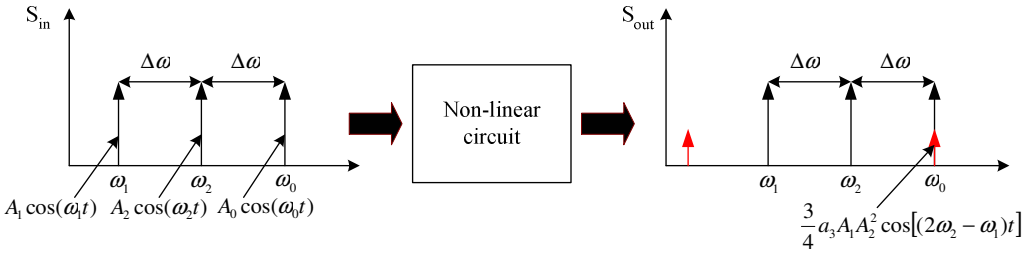

Fig. 2.3 Signal propagation through a non-linear circuit

The third order intermodulation can be measured by applying two tones Acos(ω_1t) and Acos(ω_2t) at the input of the circuit, the amplitude of the intermodulation product is measured at the output of the circuit. A plot of the output signal versus the input signal of both fundamental and intermodulation product frequency in logarithmic scale is shown in Fig. 2.4.

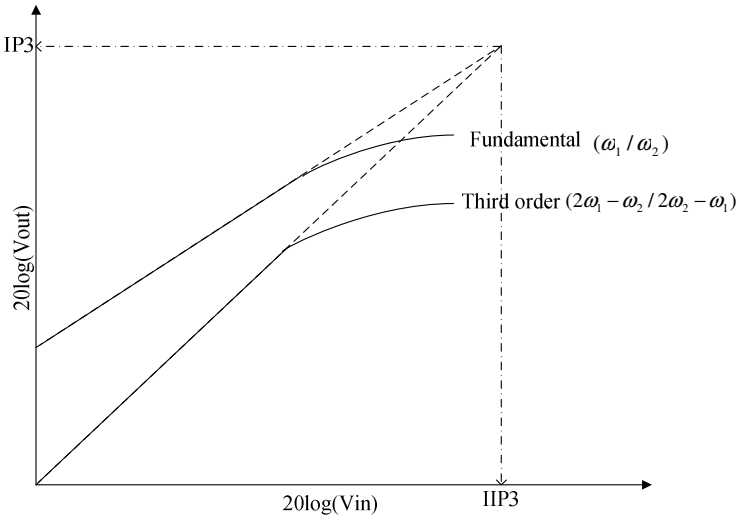

Fig. 2.4 Third-order intermodulation distortion

The third-order intermodulation interception point (IP3) is used to measure the distortion, which occurs when the third-order intermodulation products equals the fundamental signal amplitude. However this never happens in the real case due to the compressive nature of the circuit. The IP3 is calculated by extrapolating both components until they finally intercept. The input-referred IP3 is called IIP3. Assuming

the input power of two tones are the same (A_1=A_2), the amplitude of IIP3 (A_{IP3}) can be calculated as follow:

$$\begin{aligned} a_1 A_{IP3} + \frac{9}{4} a_3 A_{IP3}^3 &= \frac{3}{4} a_3 A_{IP3}^3 \\ \Rightarrow a_1 A_{IP3} &= -\frac{3}{2} a_3 A_{IP3}^3 \\ \Rightarrow A_{IP3} &= \sqrt{\frac{2}{3}\left|\frac{a_1}{a_3}\right|} \end{aligned} \tag{2.10}$$

2.1.3 Sensitivity and dynamic range (DR)

The sensitivity of a receiver is usually defined by the minimum detectable signal (MDS) of that receiver. A minimum detectable signal must have the power higher than the noise floor of the receiver. A definition of MDS is given by Eq. 2.11 [15]. Where N_f is the noise floor, NF is the noise figure of the receiver, B is the receiver 3dB bandwidth and SNR is the required signal to noise ratio at the output. The N_f can be defined by Eq. 2.12. Where k is the Boltzmann constant (1.38×10^{-23} J/K); T_0 is the room temperature in Kelvin (290 K).

$$P_{MDS} = N_f\,(dBm/Hz) + NF\,(dB) + 10\log_{10} B(dBm) + SNR \tag{2.11}$$

$$N_f = 10\log(kT_0) = -174(dBm/Hz) \tag{2.12}$$

The dynamic range of a receiver is the ratio of the maximum to the minimum input signal power levels over which the receiver can operate within some specified range of performance. The minimum level is usually determined by the sensitivity of the receiver, while the maximum level is usually set by the maximum tolerable nonlinear effects. This maximum tolerable nonlinearity is usually defined by the input 1 dB compression point P1dB (shown in Fig. 2.5). Then the dynamic range of the receiver can

be expressed as [15]:

$$DR(dB) = P1\text{dB} - P_{MDS} \tag{2.13}$$

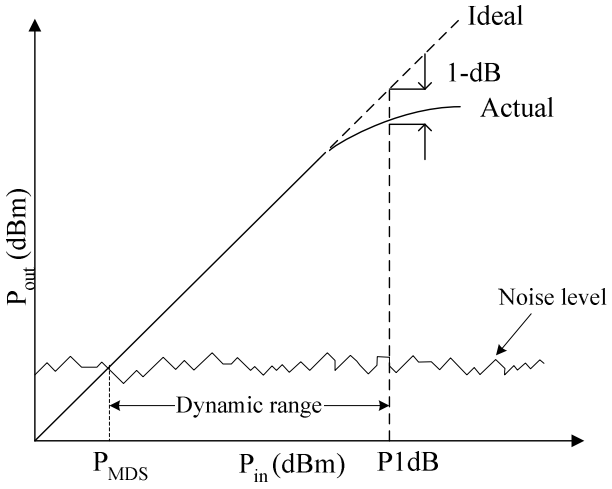

Fig. 2.5 Dynamic range

2.1.4 Quality factor (Q)

The figure of merit for assessing the performance or quality of a resonator, the quality factor, is a measure of energy loss or dissipation per cycle as compared to the energy stored in the fields inside the resonator. The Q is defined by:

$$Q = 2\pi \frac{\text{maximum energy stored}}{\text{energy dissipated per cycle}} \tag{2.14}$$

Fig. 2.6 shows a simple parallel RLC resonator driven by a current source. The impedance Z(s) of the resonator is:

$$Z(s) = \frac{s/C}{s^2 + s/RC + 1/LC} = \frac{sk}{s^2 + sBW_{3dB} + \omega_0^2} = \frac{sk}{s^2 + s\dfrac{\omega_0}{Q} + \omega_0^2} \tag{2.15}$$

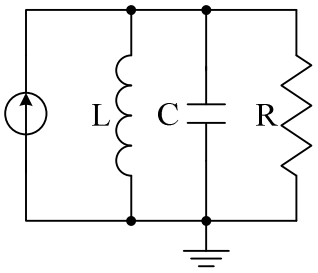

Fig. 2.6 Second order parallel resonator

where k is a constant, $\omega_0 = 1/\sqrt{LC}$ and BW_{3dB}=1/RC. ω_0 is the resonant frequency and the BW_{3dB} is the 3 dB bandwidth of the transfer function. The frequency response of this system is given in Fig. 2.7. The quality factor of this second order resonator can be expressed as [16]:

$$Q = \frac{\omega_0}{BW_{3dB}} = R\sqrt{\frac{C}{L}} \tag{2.16}$$

Therefore is equal Q, to the ratio of the resonant frequency to the 3 dB bandwidth. The higher the quality factor, the smaller the 3 dB bandwidth and the better the selectivity. From the equations above, if the center frequency of the filter is tuned by decreasing the value of capacitor, the Q of the filter decreases accordingly. So when the filter center frequency is tuned by changing the value of the capacitor, the Q of the filter, at the same time is inevitably changed.

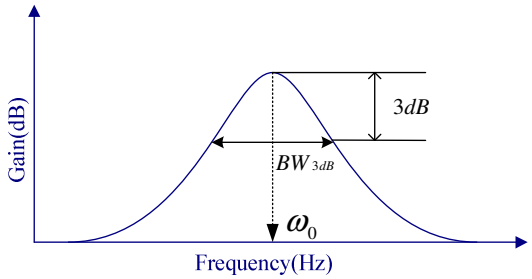

Fig. 2.7 Frequency response of a second order resonator

2.2 Radio Receiver Architectures

The three most important attributes of a good receiver design are: (a) high sensitivity, (b) good selectivity and (c) low power consumption. Receiver architectures have been developed over the last century to accommodate the increasing demand of selectivity, sensitivity and low power in wireless communication systems. The super-heterodyne receiver was introduced in 1918 which successfully overcame the problem of selectivity, and until today, almost all commercial receivers are built using this architecture. A special case of the super-heterodyne receiver is the direct conversion receiver where the LO coincides with the incoming carrier frequency and converts the RF directly to the baseband.

Super-heterodyne receiver

Heterodyning in this context simply refers to the inclusion of a mixer in the chain to convert the incoming high frequency RF signal to a lower frequency (usually a fixed intermediate frequency (IF)). Fig. 2.8 shows a typical modern super-heterodyne receiver [17]. To achieve this mixing function, a local oscillator (LO) running near the incoming carrier frequency is needed. The difference between the LO and input signal frequency results in the desired intermediate frequency (IF).

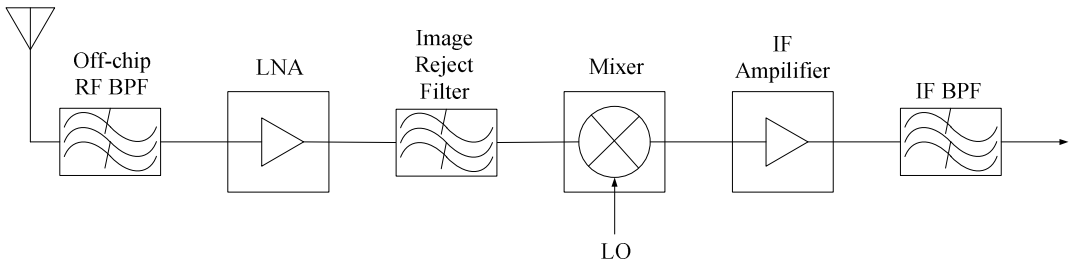

Fig. 2.8 A typical super-heterodyne receiver front-end

The first stage of the receiver is a Radio Frequency (RF) Filter. The filter

provides attenuation of the strong out-of-band interferers. The Intermediate Frequency (IF) filter rejects the slightly smaller in-band blockers soon after. The main function of the Low Noise Amplifier (LNA) is to provide enough gain to drive the mixer and to overcome the noise of the subsequent stages.

One drawback of this architecture is the image frequency problem. For a given LO, there are two distinct frequencies which will generate the same lower frequency difference. In the super-heterodyne receiver, this results in an image channel where interferers can potentially be mixed into the desired channel (shown in Fig. 2.3). The image reject filter is added to attenuate signals at this image frequency in order to remedy this problem. Another method to alleviate the image problem is to employ multiple frequency conversion stages, with a high IF chosen as the first stage to make image rejection easy, and a low IF chosen for the second (and third) stages to make channel selection more precise.

Direct conversion receiver

The direct conversion or homodyne receiver is shown in Fig. 2.9 [17]. The direct conversion receiver, sometimes called the Zero-IF receiver, converts the modulated signal directly to the baseband. The benefit of this architecture is that there is only one conversion stage and there is no image frequency to be dealt with. There are unfortunately two design challenges with the direct conversion receiver solution. The first is the problem of local oscillator re-radiation from the antenna [17]. Very careful design is needed to ensure that the LO, which is now at the frequency of the incoming signal, does not leak back through the front end mixer/amplifier/filter chain and violate spurious emission regulations. The second design challenge is the problem of dc-offset

within the two baseband signals which can corrupt wanted information that has been mixed down around zero Hz [17]. Causes of the dc offset are either drift in the baseband components (e.g. op amps, filters, A/D converters), or dc from the mixer output caused by the LO mixing with itself or with the mixers acting as square law detectors for strong input signals.

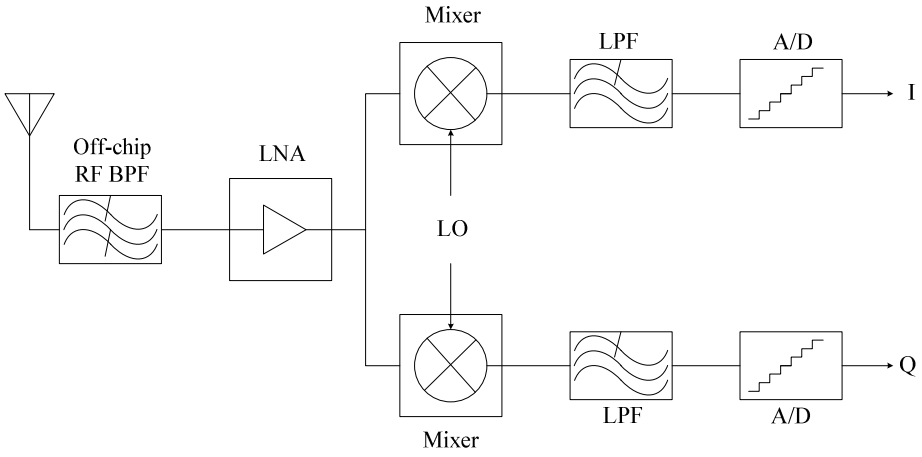

Fig. 2.9 Direct conversion receiver architecture

Proposed Receiver Architecture

As mentioned earlier, both the RF filter and image rejection filter in the super-heterodyne receiver are implemented using off-chip discrete components (ceramic and/or SAW filters). By implementing an on-chip BPF with LNA, one can replace the LNA, the off-chip RF bandpass filter and the image rejecting filter in the receiver front-end as shown in Fig. 2.10 thus reducing the system cost and power consumption. The most important is that the integration of the RF and image rejection filter makes single-chip transceiver implementation feasible. The proposed RF filter is a broadband filter which has a tunable bandwidth range from 80 MHz to 120 MHz.

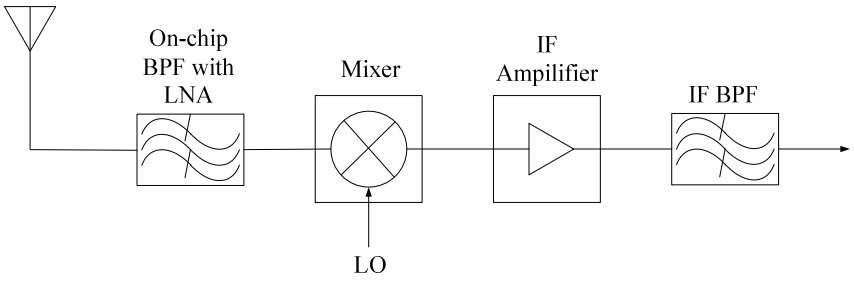

Fig. 2.10 Proposed receiver architecture

2.3 General Filter Requirements

This section will describe some common RF filtering requirements which need to be met for the transceivers used in wireless applications.

2.3.1 Out-of-band blocker rejection

The antenna usually picks up all the RF signals present in the air. There are some very strong unwanted signals located far away from the desired signal in spectrum. The RF filter must be implemented to attenuate these strong out-of-band blocking signals (Fig. 2.11.) in order not to saturate the LNA and thereby desensitize the receiver. Out-of-band blocking signals also create intermodulation products that may corrupt the desired signal.

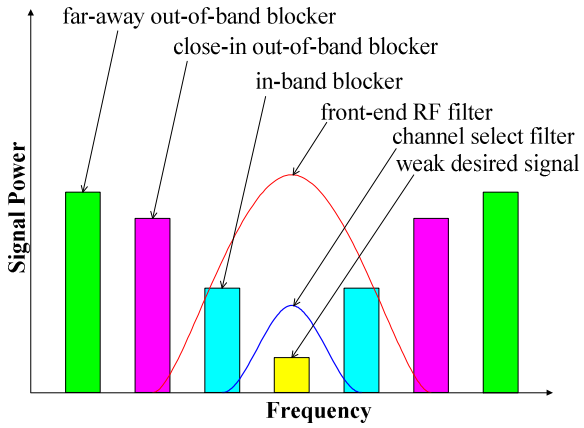

Fig. 2.11 In-band and out-of-band rejection

2.3.2 In-band blocker rejection

The strong unwanted signals found in the allocated frequency band of a wireless system are called the in-band blocking signals (Fig. 2.11). These blockers are not as strong as the out-of-band blockers. They are located close to the desired signals. Therefore it would be necessary to have an RF filter with extremely sharp edges to filter out these in-band blocking signals. The filtering at these frequencies is called channel selection filtering.

2.3.3 Image rejection

When the super-heterodyne receiver architecture is used, the image frequency superimposes on the desired signal after the first frequency conversion (shown in Fig. 2.3). Once that happens, it is not possible to recover the desired signal if the image is stronger than the desired signal. Therefore it is important to ensure that the image is rejected by a sufficient amount before or during the first conversion.

2.3.4 Noise filtering

In some situations it is necessary to filter wideband RF noise. One of the common examples is the transmitter noise in the receive band. When a strong signal is transmitted in the upper end of the transmit band it may have wideband noise with sufficient energy to corrupt a weak wanted signal in the lower end of the receive band (Fig. 2.12.)

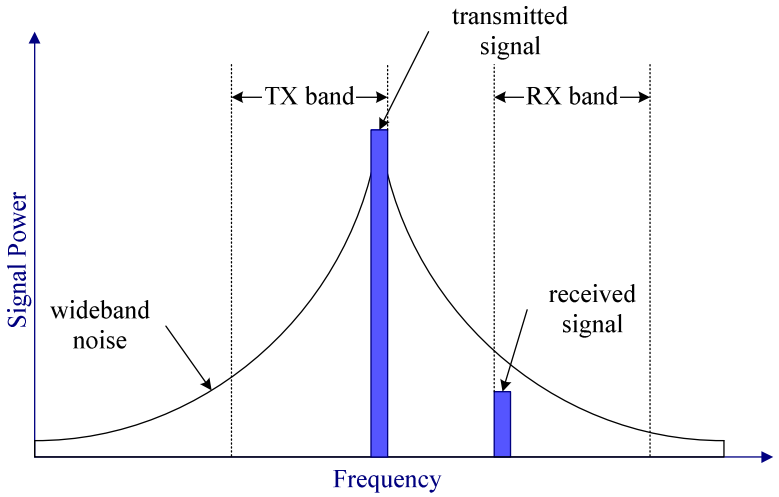

Fig. 2.12 Transmitter wideband noise in the receiver band

2.3.5 An example of filtering requirements (the Bluetooth receiver)

The Bluetooth system operates in the 2.4 GHz ISM (Industrial Scientific Medicine) band. The system frequency allocation is shown in Fig. 2.13 [8].

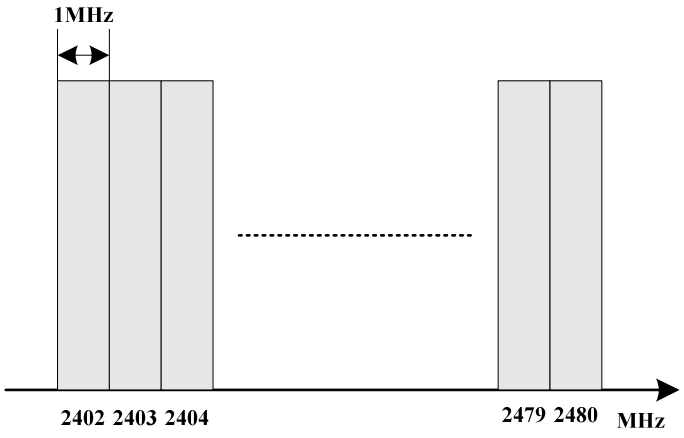

Fig. 2.13 Frequency allocation of the Bluetooth system

The in-band and out-of-band blocking specifications of the Bluetooth system are shown in Fig. 2.14 [8]. Other receiver requirements are shown in Table 2.1 [8].

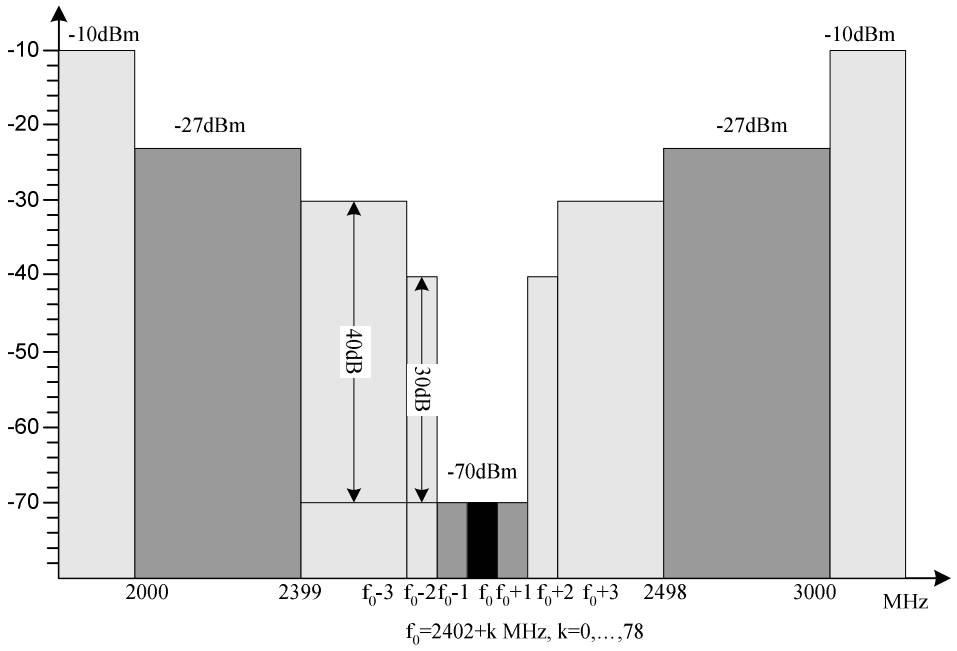

Fig. 2.14 Bluetooth blocking requirements

Table 2.1
Bluetooth receiver requirements

Bluetooth receiver requirements	Values
Actual sensitivity level	-70 dBm
Maximum usable receiver input level (BER<0.001)	-20 dBm
Dynamic range	>50 dB

2.3.6 Proposed filter requirements

The proposed filter presents in this thesis is not designed for a certain wireless system. The filter should be able to fit into various broadband short range wireless systems such as Bluetooth, 802.11a, 802.11b, 802.11g, etc. Because all of these systems operate at different frequency range and have different filtering requirements, a prototype RF filter is designed here with the requirements listed in Table 2.2. The frequency range in this design is set from 3.55 GHz to 3.65 GHz; this range can be

easily changed to other frequency ranges by changing the values of the varactors.

Table 2.2
Proposed filter requirements

Proposed RF filter requirements	Values
Actual sensitivity level	-85 dBm
Maximum usable receiver input level (P1dB)	-45 dBm
Dynamic range	>45 dB
IIP3	-30 dBm
Image rejection (500 MHz away)	50 dB
Bandwidth	100 MHz
Noise figure	15 dB
Q tuning ability (bandwidth)	80 MHz-120 MHz
Center frequency tuning ability	3.55 GHz- 3.65 GHz

2.4 Common Filter Types

There are two common types of filter, one is passive filters and the other is active filters. Each type of filter operates at a certain frequency range and has both advantages and disadvantages. This section describes the filtering solutions which are commonly used today.

2.4.1 Passive filters

Passive filters are the most common components used in wireless transceivers for RF filtering. Some common passive filters are listed as following:

LC type filters

LC type filters are the most basic passive filter. These filters are built with inductors and capacitors. They have relatively high insertion loss due to the moderate

Q-value of the passive devices.

PWB filters

Edge coupled filters made by printed wire board (PWB) are cost efficient and the out-of-band attenuation is acceptable for some less demanding standards. But the structure of the PWB is very bulky in the lower GHz range and can not fit in most wireless applications.

SAW filters

Surface acoustic wave filters are commonly used in RF filtering. They offer low insertion loss, sharp cut-off edges, small size and moderate power handling capabilities at a reasonable cost [18]. The drawback is that these filters are not tunable and they are not compatible with standard IC technology.

2.4.2 Active filters

Active filters are usually used in lower frequency range (< 1 GHz). They can be integrated in standard IC technology and easily tuned to fit different frequency bands. Some different types of active filters are discussed below:

Gm-C filters

Gm-C filters are continuous time filters which are common in lower frequency applications. In the GHz range, these filters have serious limitations in terms of linearity and noise performance. Usually they are not being employed in RF filtering.

Switched capacitor filters

Switched capacitor filters are also very common in lower frequency applications. These structures provide better dynamic range than Gm-C filters. These filters are discrete time filters; they rely on sampling in the time domain, thus aliasing

becomes a major problem.

Q-enhanced LC filters

Filters which use loss compensation for the LC resonators are called Q-enhanced LC filters. This type of filter has shown to have the best RF performance among all the active filter topologies [11]. Noise and linearity problems still exist in these filters; in addition the Q-enhancement circuit uses a large portion of the filter power consumption.

DSP filters

This type of filter uses an A/D converter to convert the analog signal to digital signal, and then use a digital processor to implement the filtering, a D/A converter is applied to convert the output digital results back to an analog signal. In the GHz range, a DSP filter requires about 20 bits of resolution and the computation time (delay) is quite long.

2.4.3 Proposed RF filter

As discussed above, the proposed filter will fulfill the requirements to filter out the out-of-band RF blocks and also provide sufficient image rejection in order to eliminate the image rejection filter. The solution to the proposed RF filter is an actively coupled Q-enhanced LC filter (shown in Fig. 2.15). By coupling stages of the Q-enhanced LC filters, the out-of-band blocker filtering and image rejection are greatly improved. The integrating of RF filtering using CMOS technology makes the low cost, low power and highly-sophisticated wireless personal communication devices possible. This proposed filter has tunable bandwidth and tunable center frequency and thus can fit into a wide range of wireless applications.

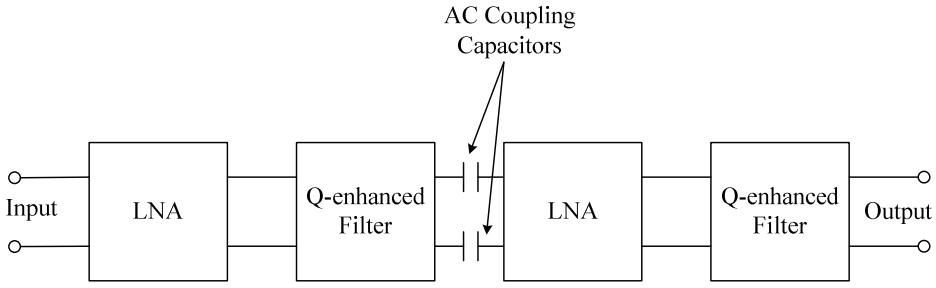

Fig. 2.15 Proposed RF filter solution

CHAPTER 3 BANDPASS FILTER DESIGN

This chapter describes the implementation of the proposed bandpass filter in CMOS. The first section illustrates a second order differential filter prototype and presents the simulation results of this filter. Section 2 describes a sixth order filter architecture using the second order prototype as a building block. The simulation results of the sixth order filter are also included in this chapter.

3.1 Design of a Second Order Differential Bandpass Filter

In this design, a second order Q-enhanced LC differential filter is used as the basic building block for the proposed sixth order bandpasss filter. As shown in Fig. 3.1, the second order filter has three parts. The input LNA serves as a tranconductance which converts the input voltage to current output; the parallel LC resonate circuit (LC tank) forms a second order filter and the Q-enhancement circuit compensates for the loss of the LC tank.

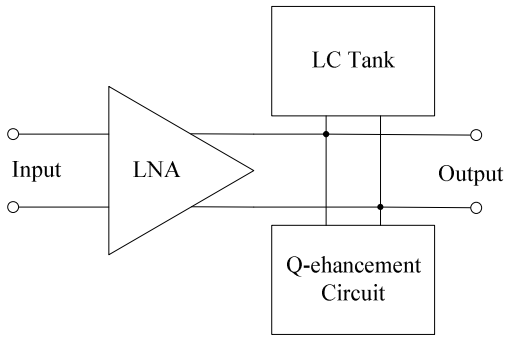

Fig. 3.1 Second order Q-enhanced LC differential filter

3.1.1 Input LNA design

When constructing the LC tank in parallel mode, a current source is needed to drive the tank. Inputs to the filter are usually voltage signals; an input transconductance is required to transfer the voltage signal to a current signal. This input transcondutance provides current gain and acts as a low noise amplifier (LNA).

3.1.1.1 LNA topologies considerations

A CMOS LNA usually has some basic requirements: a high voltage gain, a low noise figure (NF), a good input matching and a high linearity. Two groups of LNAs will be discussed here, one is the common gate LNA and the other is the common source LNA.

A typical common gate LNA is shown in Fig. 3.2. The inductor L_s is the RF-Choke inductor for the DC-path to ground. From the small signal model of the circuit (shown in Fig. 3.3), the input admittance Y_{in} is equal to:

$$Y_{in}(s) = \frac{1}{sL_s} + sC_{gs} + g_m \tag{3.1}$$

When input impedance matches, $L_s = \frac{1}{\omega^2 C_{gs}}$ and $Y_{in} = g_m = \frac{1}{R_s}$, where C_{gs} is the gate-to-source capacitance of the input MOS transistor.

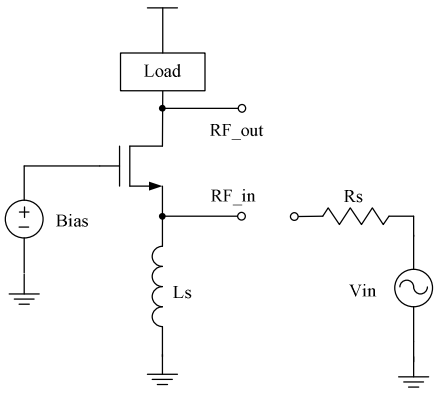

Fig. 3.2 Common gate LNA

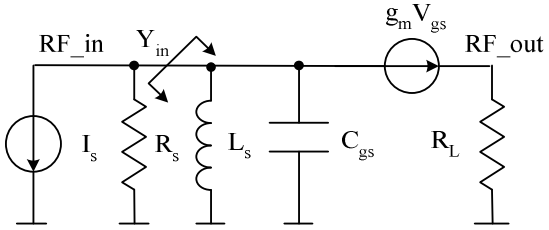

Fig. 3.3 Small signal model of the common gate LNA

Assuming the thermal noise from the transistor is the most significant noise. The noise figure of this LNA is shown in Eq. 3.2.

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{I_n^2 r_{in}^2 + 4kTR_s}{4kTR_s} = 1 + \frac{I_n^2}{4kTR_s g_m^2} = 1 + \frac{4\gamma kTg_m}{4kTR_s g_m^2} = 1 + \frac{\gamma}{R_s g_m} \quad (3.2)$$

where I_n the source noise current and r_{in} is the input impedance. γ is the drain noise constant. For the long channel transistor in saturation, γ=2/3, and γ=2-3 for short channels [19]. When input matching, Eq.3.2 simplifies to:

$$F = 1 + \gamma \quad (3.3)$$

In the equation, The NF of this LNA topology is in the order of 3dB.

Fig. 3.4 is a typical common source LNA. In order to match the input impedance, there are 3 possible choices listed in Fig. 3.5. The first one is to use a 50Ω resistor across the input terminal, the second one is a shunt-series feedback and the third

one is on inductive source degeneration. Both the first one and the second one use noisy resistor to provide input matching and this degrade the noise figure of the LNA. The noise figure of the first one is in the order of 3dB. Shunt-series feedback also has a high power consumption problem. These drawbacks make the above topology less attractive for LNA portable applications.

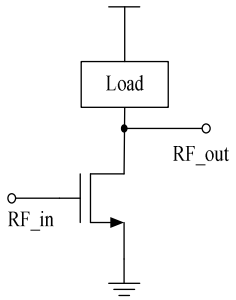

Fig. 3.4 A typical common source LNA

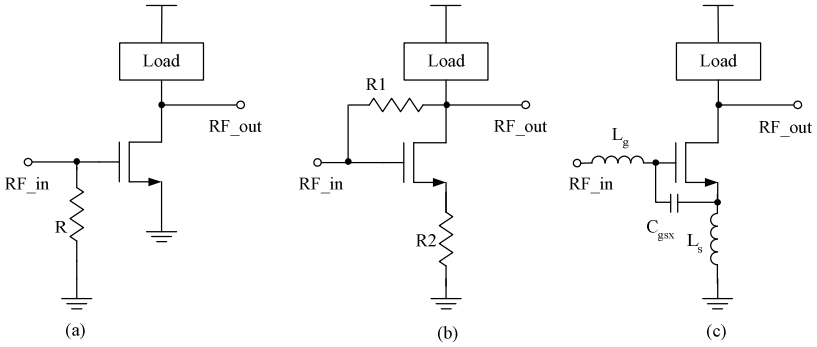

Fig. 3.5 (a) Resistive termination, (b) shunt-series feedback and (c) inductive source degeneration

The last one is the inductive source degeneration LNA in which the input signal is fed to the gate terminal and to the source terminal through the parasitic gate-to-source capacitance. This topology uses a combination of phase shift and capacitive coupling to provide a real LNA input impedance. This topology has 2 main advantages: (1) it enables a good power match; (2) it allows high gain while adding a minimum of noise. Sub-1dB noise figures have been reported for inductively source

degenerated CMOS LNA operating in the lower GHz range [20]. These features have made this the most commonly used topology for CMOS LNA and it is also the one that is pursued in this work.

3.1.1.2 Input matching for the inductively degenerated LNA

A good power match at the input of LNA is very important in this case because this LNA will connect directly to the antenna. As shown in Fig. 3.6, C_{gs} is the parasitic gate-source capacitance of the input MOS transistor. C_g is the input capacitance. L_s is an inductance that lowers the gain through negative feedback. This improves linearity and helps creates the desired input impedance. L_g represents the inductance of the off-chip PCB traces and the bondwire inductance. The parasitic resistance of the inductors L_s and L_g are represented as R_l and R_g. The input impedance of this circuit is derived as:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{g_m L_s}{C_{gs}} + R_g + R_l + j\left(\omega(L_g + L_s) - \frac{1}{\omega C_g} - \frac{1}{\omega C_{gs}}\right) \tag{3.4}$$

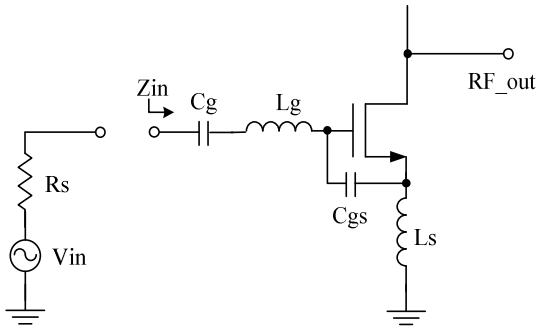

Fig. 3.6 Input matching of the inductively degenerated LNA

As shown in the equation, the real part of the input impedance is independent of frequency and the imaginary part only equals zero at a single frequency

where $\omega = \sqrt{\frac{C_{gs} + C_g}{C_g C_{gs}(L_g + L_s)}}$. This implies that the input impedance can only provide a good power match over a certain bandwidth.

When the impedance matches the source resistor R_s, the input impedance of the LNA becomes:

$$\mathrm{Re}(Z_{in}) = \frac{g_m L_s}{C_{gs}} + R_g + R_l = R_s \tag{3.5}$$

$$\mathrm{Im}(Z_{in}) = \omega(L_g + L_s) - \frac{1}{\omega C_g} - \frac{1}{\omega C_{gs}} = 0 \tag{3.6}$$

3.1.1.3 Noise analysis of the inductively degenerated LNA

Noise figure (NF) is the most important parameter of the LNA. In this section, the noise model of MOSFET will be presented and the NF of the inductively degenerated LNA will be calculated and optimized.

Thermal noise of a resistor

A resistor is a common noise source in analog circuits. The mean square noise voltage spectral density of a physical resistor R due to thermal noise (shown in Fig. 3.7) is [22]:

$$\overline{v_{n,R}^2} = 4kTR\Delta f \text{ or } \overline{i_R^2} = \frac{4kT\Delta f}{R} \tag{3.7}$$

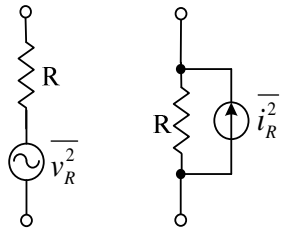

Fig. 3.7 Resistor thermal noise model

High frequency noise model of a deep submicron MOSFET

A noise model of a deep submicron MOSFET is depicted in Fig. 3.8. The mean square drain noise current due to thermal noise is [21]:

$$\overline{i_{n,d}^2} = 4kT\gamma g_{d0}\Delta f \tag{3.8}$$

In this equation, γ is the drain noise constant and g_{d0} is the zero bias drain-source conductance. γ equals to 2/3 for long channel and 2-3 for sub micron short channel devices [19].

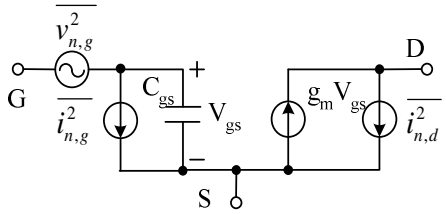

Fig. 3.8 MOSFET transistor noise model

Noise figure calculation

Fig. 3.9 shows a small signal diagram which is used to calculate the LNA noise figure. The first noise generator in the circuit is $v_{n,Rs}$ which models the thermal noise of the source resistor R_s. The next noise generator is the drain noise current of the input transistor.

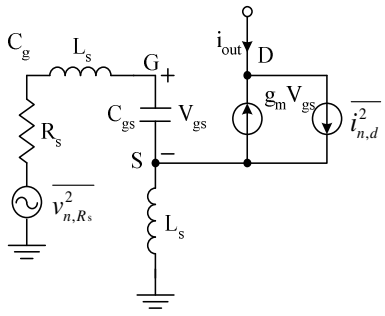

Fig. 3.9 Small signal diagram with noise source for the LNA

The output noise current which is caused by thermal noise of the source resistor $i_{out,Rs}$ can be calculated as shown in (3.9) where it is assumed that the input is power matched. The output noise current which is caused by thermal noise in the channel of the input transistor can be calculated as shown in (3.11).

$$i_{out,R_s} = g_m \frac{1}{sC_{gs}} i_{g,R_s} = g_m \frac{1}{sC_{gs}} \frac{v_{n,R_s}}{2R_s} = -j \frac{g_m}{\omega 2R_s C_{gs}} v_{n,R_s} \tag{3.9}$$

$$i_{out,R_g+R_l} = g_m \frac{1}{sC_{gs}} i_{g,R_g+R_l} = g_m \frac{1}{sC_{gs}} \frac{v_{n,R_g+R_l}}{2R_s} = -j \frac{g_m}{\omega 2R_s C_{gs}} v_{n,R_g+R_l} \tag{3.10}$$

$$i_{out,d} = \frac{i_{n,d}}{2} \tag{3.11}$$

The output noise power spectral density which arises due to the noise from the source is calculated as shown in Eq. 3.12. The output noise power spectral density caused by the parasitic resistance of bond wire inductor and source inductor is shown in Eq. 3.13. The output noise power spectral density which is caused by the channel noise in the input transistor is calculated as shown in Eq. 3.14 where g_{d0} is replaced by g_m/α due to mobility degradation in short channel MOS transistors [22].

$$S_{out,R_s}(\omega_0) = \frac{\left|i_{out,R_s}\right|^2}{\Delta f} = \frac{g_m^2}{\omega^2 4R_s^2 C_{gs}^2} \frac{\overline{v_{n,R_s}^2}}{\Delta f} = \frac{g_m^2}{\omega^2 4R_s^2 C_{gs}^2} 4kTR_s = \frac{g_m^2 kT}{\omega^2 R_s C_{gs}^2} \tag{3.12}$$

$$S_{out,R_g+R_l}(\omega_0) = \frac{\left|i_{out,R_g+R_l}\right|^2}{\Delta f} = \frac{g_m^2}{\omega^2 4R_s^2 C_{gs}^2} \frac{\overline{v_{n,R_g+R_l}^2}}{\Delta f} = \frac{g_m^2}{\omega^2 4R_s^2 C_{gs}^2} 4kT(R_g + R_l) \tag{3.13}$$

$$S_{out,d}(\omega_0) = \frac{\left|i_{out,d}\right|^2}{\Delta f} = \frac{1}{4} \frac{\overline{i_{n,d}^2}}{\Delta f} = \frac{1}{4} 4kT\gamma g_m = kT\gamma g_m \tag{3.14}$$

As defined in Eq. 2.2, noise factor can also be expressed as [15]:

$$F = 1 + \frac{N_{c,o}}{N_i G} = 1 + \frac{S_{out,circuit}(\omega)}{S_{out,source}(\omega)} \tag{3.15}$$

$S_{out,circuit}(\omega)$ is the output noise power spectral density caused by the circuit and $S_{out,source}(\omega)$ is the output noise power spectral density caused by the source. Applied to the source degenerated LNA, the noise factor is derived as follow:

$$F = 1 + \frac{S_{out,d}(\omega_0) + S_{out,R_g+R_l}(\omega_0)}{S_{out,R_s}(\omega_0)} = 1 + \frac{R_g + R_l}{R_s} + \frac{kT\gamma g_m}{\frac{g_m^2 kT}{\omega_0^2 R_s C_{gs}^2}} = 1 + \frac{R_g + R_l}{R_s} + \frac{\gamma \omega_0^2 R_s C_{gs}^2}{g_m} \tag{3.16}$$

3.1.1.4 Other considerations

Gate Resistance: The polysilicon material which forms the gate of MOS transistors usually has a relatively high resistance. The gate resistance can be expressed as [23]:

$$R_g = \frac{R_{poly} W}{3n^2 L} \tag{3.17}$$

In this equation, R_{poly} is the sheet resistance of the polysilicon material, n is the number of transistor fingers, L is the length of the transistor and W is the width of the transistor. As can be seen from this equation, the gate resistance can be reduced by increasing the number of transistor fingers. This R_g can be made negligible if $R_g = 0.01 \times R_s$ or less. An expression for the number of transistor fingers can be found as follow when $R_g = 0.01 \times R_s$.

$$n = 10\sqrt{\frac{R_{poly} W}{3R_s L}} \tag{3.18}$$

Power Gain, Load Impedance: This LNA topology is actually an input transconductance (g_m) which transfers the input voltage to output current. g_m of this LNA can be expressed as:

$$g_m = \frac{\mu\varepsilon_r\varepsilon_0}{t_{ox}}\left(\frac{W}{L}\right)(V_{GS} - V_T) \tag{3.19}$$

In this equation, μ is the carrier mobility, ε_r is the relative permittivity, equal to 3.9 for SiO_2, ε_0 is the permittivity of free space $\varepsilon_0=8.85\times10^{-12}$ F/m, V_{GS} is the gate to source voltage, V_T is the threshold voltage, and t_{ox} is the thickness of the oxide layer.

The power gain or voltage gain of this LNA depends on the impedance load. In the design, the impedance load is a tunable LC tank. As a result, the power gain of this LNA is also tunable in a certain range.

Differential Operation: The LNA designed in this section is in a single ended form, because it is easier to analyze the LNA in this form. However a differential LNA exhibits some merits and is often used in RF front-ends. If a differential LNA is used, R_s needs to be substituted with $R_s/2$ in the analysis.

3.1.1.5 Design example

An example is given here to illustrate the design methodology of the inductively degenerated LNA. The LNA is designed in differential mode, but here only half of the circuit is considered. The LNA works at f_0=3.6 GHz, has a source resistance of 25 ohms (R_s) and uses the 0.18 micron CMOS process. The input transistor is biased at $V_{GS}=V_{DS}$=0.95V. R_l=4.3 ohm, R_g=5.7 ohm, L_s=1.021 nH, L_g=1.35 nH. The sample design is shown in Fig. 3.10. C_{gs} and g_m can be calculated as follow:

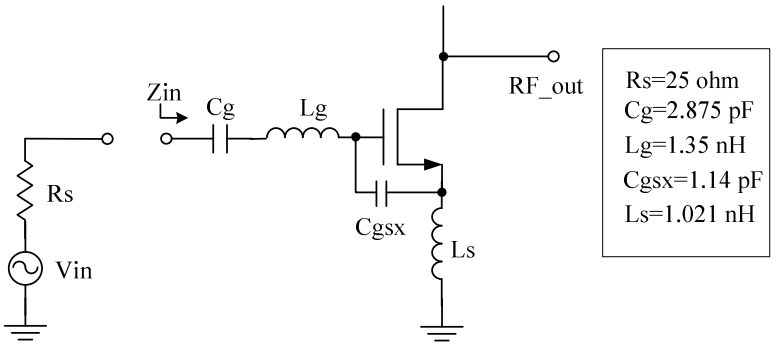

Fig. 3.10 A LNA design example

$$C_{gs} = \frac{2}{3}\left(\frac{\varepsilon_0 \varepsilon_{sio_2}}{t_{ox}}\right) A = 15.7\, fF \tag{3.20}$$

$$g_m = 0.017 A \cdot V^{-1} \tag{3.21}$$

$$I_D = \mu \frac{\varepsilon_0 \varepsilon_{sio_2}}{2t_{ox}} \frac{W}{L} (V_{GS} - V_T)^2 = 4.25\, mA \tag{3.22}$$

An extra gate to source capacitance C_{gsx} is added to match the input. The value of C_{gsx} can be found as:

$$C_{gsx} = \frac{g_m L_s}{R_s - (R_g + R_l)} - C_{gs} = \frac{0.017 \times 1.021 \times 10^{-9}}{25 - (4.3 + 5.7)} - 15.7 \times 10^{-15} = 1.14\ pF \tag{3.23}$$

The NF can be calculated as:

$$NF = 10 \log(1 + \frac{4.3 + 5.7}{25} + \frac{0.4 \times (2\pi \times 3.6 \times 10^9)^2 \times 25 \times ((15.7 + 1140) \times 10^{-15})^2}{0.017}) = 2.56\, dB \tag{3.24}$$

From Eq. 3.6, the C_g can be calculated as:

$$C_g = \frac{1}{\omega^2 (L_g + L_s) - \frac{1}{(C_{gs} + C_{gsx})}}$$

$$= \frac{1}{(2\times\pi\times 3.6\times 10^9)^2 (1.021+1.35)\times 10^{-9} - \frac{1}{(15.7+1140)\times 10^{-15}}} \qquad (3.25)$$

$$= 2.875\,\text{pF}$$

3.1.1.6 A differential cascoded LNA

The source degenerated common source LNA provides good linearity, high gain and low noise figure. But it also has some drawbacks, the common source LNA is narrow band and has high output impedance. By cascoding a common gate stage, one can lower the output impedance and also improve the LNA bandwidth. Once the LNA circuit topology is complete, it is necessary to make the circuit differential. Differential circuits are an important part of the integrated circuit design because they offer many important advantages over single-ended circuits. One important advantage offered by the differential LNA is the stable reference point. With any type of circuit, the measured values are always taken with respect to a reference. In the case of a non-differential LNA in the RF front end, this reference would be the on-chip ground. However, the on-chip ground may not be very reliable due to the presence of the parasitic resistance and capacitance, leading to unpredictable results. By contrast, with a differential LNA, the measured results of the half-circuit are always taken with respect to the other half-circuit. This minimizes the chances of getting unexpected results.

Another significant and relevant benefit of using a differential circuit is the linearity improvement. By using differential structure, the even order harmonics are

mostly cancelled out thus greatly improves the linearity performance of the LNA (which is demonstrated in the Section 1.3.2). The complete differential LNA is demonstrated in Fig. 3.11, where two source degeneration inductors are combined together as a center tapped differential inductor L_s.

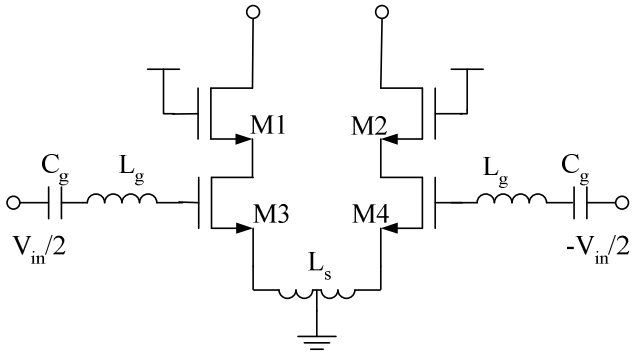

Fig. 3.11 A differential source degeneration LNA

A differential LNA based on Section 3.1.1.5 design example with tuned load (shown in Fig. 3.12) was designed for testing. Where L_d and C_d are the load impedance. The input impedance is 50 ohms. The parameters for the circuit elements are shown in Table 3.1

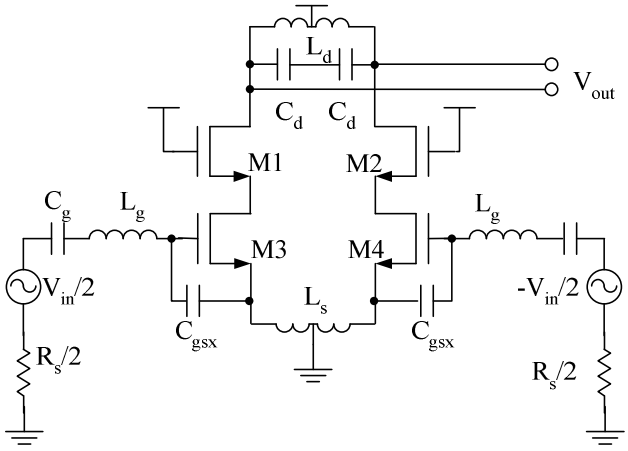

Fig. 3.12 A differential LNA with tuned load

Table 3.1
Circuit parameters for the differential LNA

Symbol	Component	Value
L_g	input inductor	1.35 nH
L_s	source inductor	4.042 nH
L_d	load inductor	4.042 nH
C_d	load capacitance	1.0 pF
Cg	input capacitance	2.875 pF
M1 & M2	cascode MOSFET	15 μm / 0.18 μm
M3 & M4	input MOSFET	15 μm / 0.18 μm
C_{gsx}	extra gate-to-source capacitance	1.14 pF

The differential LNA was simulated under the ADS dynamic-link using standard 0.18 μm CMOS technology file. In the simulation, the LNA is defined as a two port network. Scattering parameters are used to evaluate the gain and input matching of the LNA. By defining the input port as port 1 and the output port as port 2, the forward transmission coefficient S21 represents the gain of the LNA, the reflection coefficient S11 represents the ratio of reflected signal at the input, and the reflection coefficient S22 represents the ratio of reflected signal at the output. The simulation results are shown in the following:

1) Input matching:

The input matching is evaluated by the reflection coefficient S11. A smaller S11 represents a better match; a perfect match appears at S11 equals zero. As can be seen from the simulation result in Fig. 3.13, a maximum input match appears at 3.58 GHz where S11 equals -52 dB. S11 is less than -20 dB over the designed frequency

range.

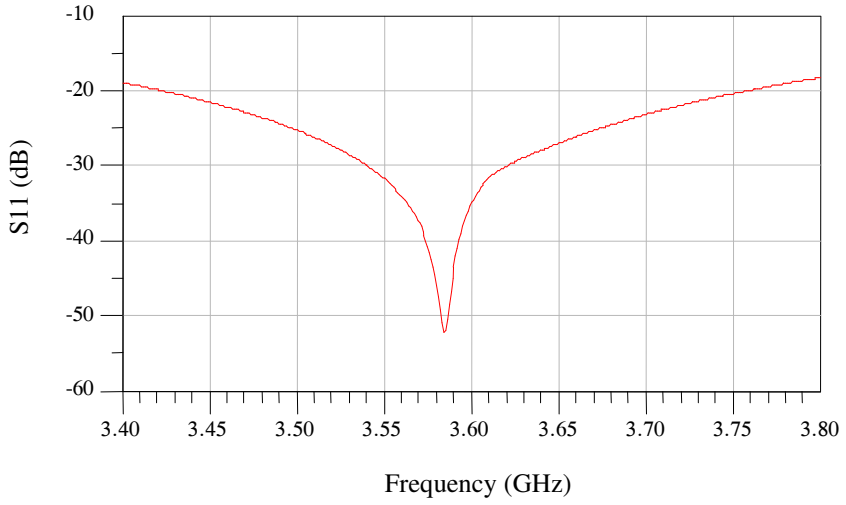

Fig. 3.13 Input matching of the differential LNA

2) Gain:

The forward transmission coefficient S21 of the two port network is the gain of the LNA. The simulated S21 is shown in Fig. 3.14. The maximum gain of 11.5 dB appears at 3.58 GHz.

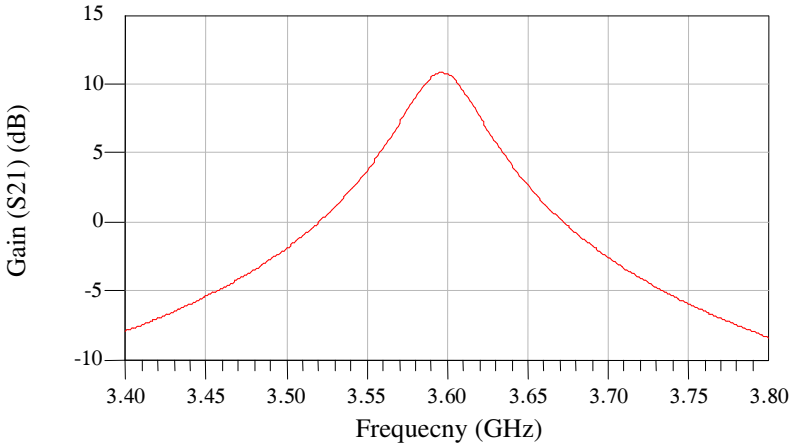

Fig. 3.14 Gain of the differential LNA

4) Noise performance:

The noise performance of the LNA is evaluated by the noise figure. Seen from

the simulated result in Fig. 3.15, a minimum NF of 2.75 dB appears at 3.58 GHz which is very close to the calculated value of 2.56 dB.

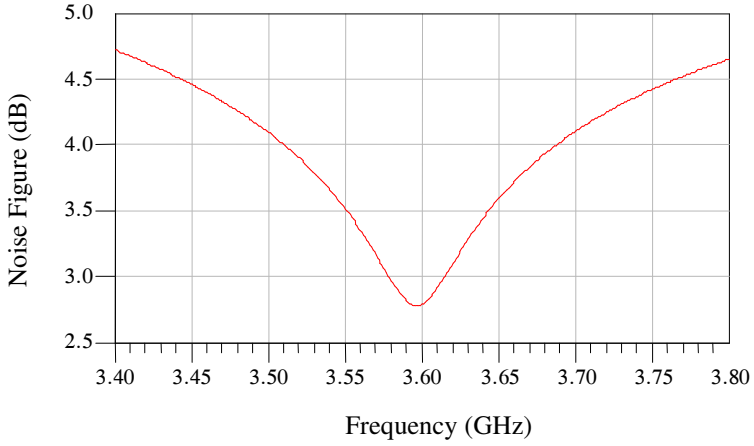

Fig. 3.15 Noise performance of the differential LNA

5) Linearity performance:

The linearity performances are evaluated by IIP3 and 1 dB compression point. The simulated result is shown in Fig. 3.16, where P1dB equals to 3.8 dBm and IIP3 equals to 18 dBm.

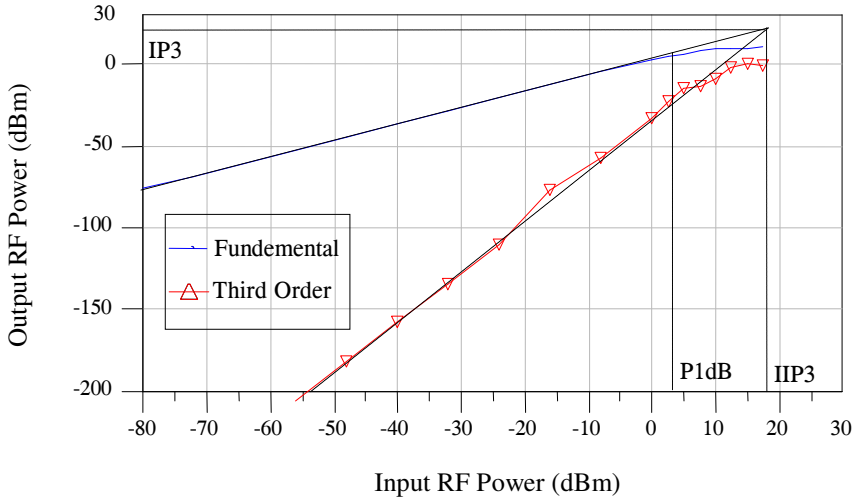

Fig. 3.16 Linearity of the differential LNA

The performances of the differential LNA are summarized in Table 3.2.

Table 3.2
Differential LNA performance

Symbol	Comment	Value
Vdd	power supply	1.8 V
Iss	current dissipation	8 mA
G	Gain	11.5 dB
NF	noise figure	2.8 dB
IIP3	input third order intercept point	18 dBm
IP3	output third order intercept point	26 dBm
P1dB	input 1 dB compression point	3.8 dBm

3.1.2 Parallel RLC resonant circuit

In this section, the most important properties of resonators used for filtering in RFIC filters will be discussed. A LC tank is simply an inductor and a capacitor coupled in parallel. A model for the parallel LC resonator is given in Fig 3.17, where R_p represents the resistance loss of the LC tank which mainly comes from the series parasitic resistance R_s of the inductor L_s. The relationship between R_p, R_s, C_p, C_s, L_p, L_s can be found in the following equations [16]:

$$R_P = \frac{\omega^2 L_s^2}{R_s} + R_s \tag{3.26}$$

$$L_P = \frac{R_s^2}{\omega^2 L_s} + L_s \tag{3.27}$$

$$C_p = C_s \tag{3.28}$$

The resonance frequency of the resonator is:

$$\omega_0 = \frac{1}{\sqrt{L_P C_P}} \tag{3.29}$$

And the quality factor is in the form of [16]:

$$Q = \frac{R_P}{\omega_0 L_P} = \omega_0 R_P C_P = \frac{R_P}{\sqrt{L_P C_P}} = \frac{\omega_0}{BW_{3dB}} \tag{3.30}$$

where $f_0 = \frac{\omega_0}{2\pi}$ and BW_{3dB} is the 3dB bandwidth in Hz.

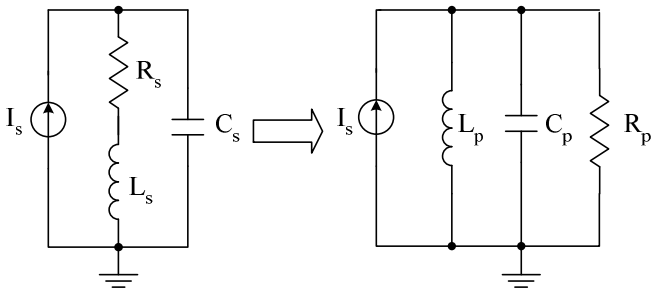

Fig. 3.17 Parallel LC resonator model

3.1.3 CMOS inductor design

One of the key factors that determine the performance of the RF integrated circuits (RF IC's) is the availability of good quality integrated inductors. Unfortunately, parasitic effects, such as coupling capacitance and losses related to the integration substrate degrade their performance. These unwanted effects are particularly important for silicon substrates.

The on-chip CMOS inductor design is critical important in the RF filter design because the Q value of the inductor dominates the losses in the LC tank thus directly affects the filter selectivity.

3.1.3.1 CMOS spiral inductor parasitics and modeling

On-chip inductors in CMOS processed with EPI substrates are affected by the lossy substrate. The resistivity of the bulk CMOS substrate is much lower than which for bipolar, BiCMOS and SOI CMOS processes [24]. There are three dominating loss mechanisms in on-chip inductors in CMOS processes. The first is the series parasitic resistance of the inductor. The second is the eddy currents loss due to the lossy substrate. The third is the capacitive coupling to the conducting substrate [25].

Fig 3.18 is a layout of an on-chip spiral inductor and Fig 3.19 is the model of this inductor.

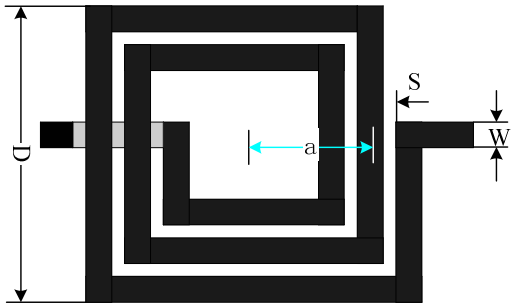

Fig. 3.18 A layout of an on-chip spiral inductor

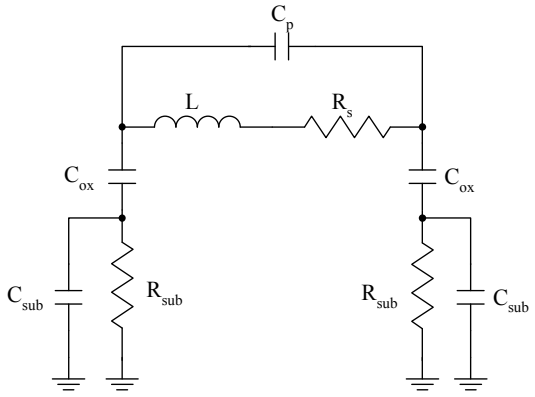

Fig. 3.19 A model of the on-chip spiral inductor

The parameters of the model are listed below [25]:

$$L = \frac{37.5\mu_0 N^2 a^2}{11D - 14a} \tag{3.31}$$

$$R_s = \frac{l}{W\sigma\delta(1 - e^{-t/\sigma})} \tag{3.32}$$

$$C_P = NW^2 \frac{\varepsilon_{ox}}{t_{ox}} \tag{3.33}$$

$$C_{ox} = WL \frac{\varepsilon_{ox}}{t_{ox}} \tag{3.34}$$

$$R_{sub} = \frac{2}{WLG_{si}} \tag{3.35}$$

$$C_{sub} = \frac{WLC_{si}}{2} \tag{3.36}$$

where $\mu_0=4\pi\times10^{-7}$, σ is the conductivity of the material, D is the diameter of the inductor, a is the distance from the center of the inductor to the middle of the windings, L is the total length of the spiral, t is the thickness of the metal and δ is the skin depth given by $\delta = \sqrt{\frac{2}{W\mu_0\sigma}}$ [26], G_{si} (C_{si}) is process-dependent parameters.

3.1.3.2 Design guidelines for CMOS spiral inductors

1) Layer topology: Use the upper most metal layer for inductor turns. The upper most metal layer in CMOS technology usually is the thickest metal layer and it is located far away from the lossy substrate.

2) Inductor shape: An inductor with circular turns gives the highest inductance value and hence the highest Q-value [27].

3) Outer radius (R): The quality factor of the inductor increases with the radius of the spiral for small R, but self-resonant frequency also increases with R, as

parasitic capacitance between the substrate and the spiral increases. A good design usually has R<100 micron [27], [28].

4) Metal width (W): Metal width should be as wide as possible. The series parasitic resistance (R_s) decreases when the metal width increases and hence the quality factor of the inductor also increases. However, as the metal width increasing, the skin effects appear in the metal traces, this tends to increase R_s. The chip areas also increase with the metal width. A good design uses $10\mu m < W < 20\mu m$ [27].

5) Spacing between turns: Spacing should be as small as possible. The mutual inductance decreases as the spacing increases.

3.1.3.3 Layout consideration for CMOS spiral inductors

CMOS inductors suffer from the substrate loss and hence have very low Q. With patterned ground shields (PGS) in the first metal layer under the inductor, the substrate loss is greatly reduced and further more, the noise from the substrate is also isolated [29]. Fig. 3.20 shows an optimized PGS which can reduce substrate resistance loss and eddy currents (shown in Fig. 3.21).

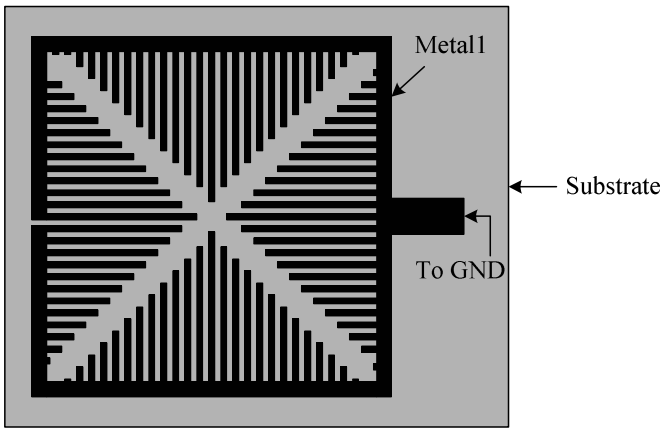

Fig. 3.20 Patterned Ground Shield (PGS)

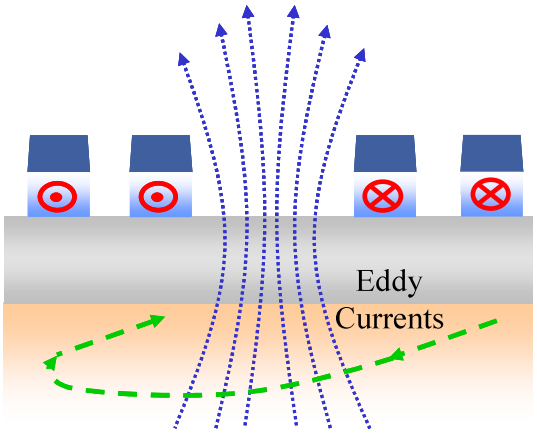

Fig. 3.21 Eddy currents

3.1.3.4 Design example of a CMOS spiral inductor

Designing a high Q CMOS spiral inductor with an accurate model requires tremendous work. Fortunately, there are a few commercial and free software programs that provide some degrees of assistant. This software includes ASITIC [30], Spiral Inductor Simulation Program (SSIP), Agilent ADS Momentum circuit designer and other 3D electromagnetic simulation programs. ASITIC is used here to design the inductor because the software contains a 0.18 μ m technology file and it calculates the eddy current effect. Fig 3.22 is the layout of the CMOS spiral inductor in differential mode designed with ASITIC software. Fig 3.23 illustrates the inductor model. Table 3.3 lists the geometries of this inductor. Table 3.4 lists the parameters of the model.

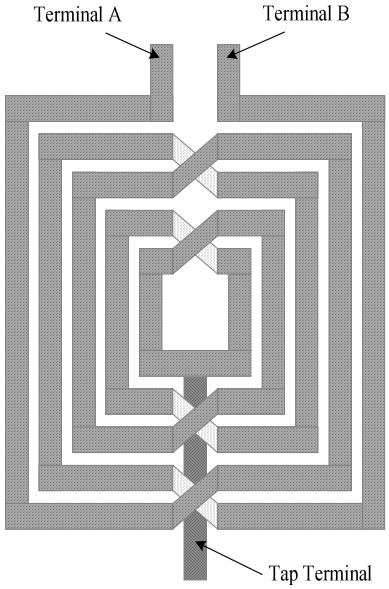

Fig. 3.22 Differential mode spiral inductor

Table 3.3
Geometries of the inductor

Symbol	Comment	Value
W	wire width	8 μ m
S	spacing between turns	1 μ m
N	number of turns	5
R_1	inner radius	16 μ m
R_2	outer radius	60 μ m

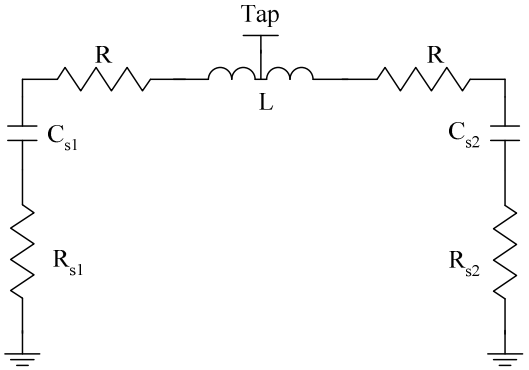

Fig. 3.23 Model of the differential spiral inductor

Table 3.4
Parameters of the model

Symbol	Comment	Value
L	inductor	2.042 nH
R	serial parasitic resistor	4.3 ohms
C_{s1}	inductor to substrate capacitor	45.81 fF
C_{s2}	inductor to substrate capacitor	44.92 fF
R_{s1}	substrate loss	3.314 ohms
R_{s2}	substrate loss	4.376 ohms
Q	quality factor	4.9
f_0	resonance frequency	16.45 GHz

The parallel equivalent resistance R_P of this inductor can be calculated using Eq. 3.26. The calculated R_P equals 256.7 ohms at the center frequency of 3.6 GHz.

3.1.4 Variable capacitors (Varactors) design

Because of the inaccuracy of passive models of CMOS technology and the process variation, the resonate frequency of the LC tank can not be precisely made. So a frequency tuning mechanism must be employed. There are two types of variable capacitors (varactors) can be employed in the design; one is a MOS varactor based on NMOS FET and the other is a junction varactor based on a pn junction [13]. The C_{max}/C_{min} ratio and the Q value are the two main considerations of the capacitor varactors. C_{max} is the maximum capacitance value of the varactor and C_{min} is the minimum capacitance value of the varactor. Junction varactors have larger Q than MOS varactors and have similar tuning C_{max}/C_{min} ratio to MOS varactor but occupy larger silicon area [31]. The junction varactors are chosen in this design because the tank loss

is the main concern. Fig 3.24 is the illustration of a p^+-to-n-well junction. The depletion region between the p^+-implantation and the n-well results the junction capacitance varactor (C_j). The capacitance is a function of the width of the depletion region, which is controlled by the reverse voltage (V_R). The inherent losses are represented by the series resistor, R_{sj} and the parallel resistor R_{pj}. The series resistor is expected to represent the major loss contribution, and hence dominates the Q.

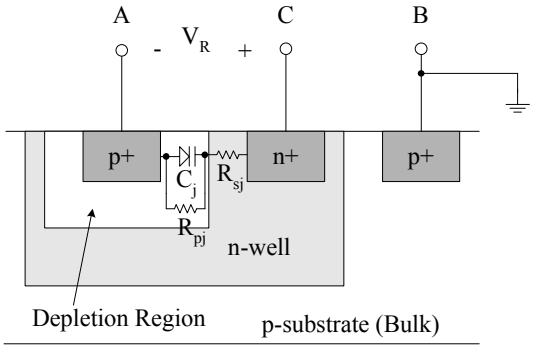

Fig. 3.24 p+ to n-well junction

3.1.4.1 Junction varactor model

A simplified model of a p+ to n-well junction is shown in Fig. 3.25.

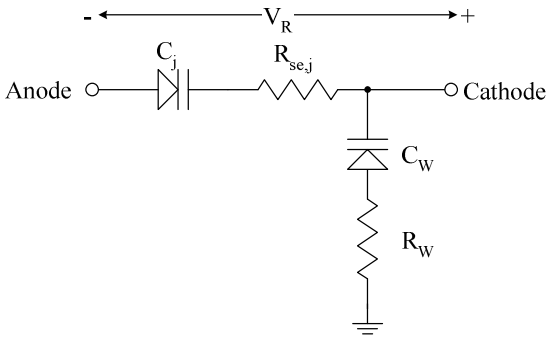

Fig. 3.25 Junction varactor model

where C_j is the junction capacitance and can be expressed as a function of the reverse voltage (V_R) [32]:

$$C_j(V_R) = \frac{C'_{j0} A_j}{\left(1 + \frac{V_R}{V_j}\right)^{m_j}} \tag{3.37}$$

C'_{j0} is the junction capacitance per unit area at zero voltage, A_j is the junction area, V_j is the built-in junction potential and m_j is a fitted process constant dependent on the doping profiles for the p^- and n^- implantations.

For an abrupt junction, C'_{j0} is given by [32]:

$$C'_{j0} = \sqrt{\frac{q\varepsilon_r\varepsilon_0}{2V_j}\frac{N_A N_D}{N_A + N_D}} \tag{3.38}$$

where $q=1.602\times10^{-19}$ C is the elemental charge, $\varepsilon_0=8.85\times10^{-12}$ F/m is the permittivity of free space, $\varepsilon_r=11.8$ is the relative permittivity of silicon, N_A is the concentration of the acceptor dopants [holes/m^3] in the p-region and N_D is the concentration of the donor dopants [electrons/m^3] in the n-region.

The series resistor $R_{se,j}$ represents the losses associated with the junction. R_W represents the lossy signal path through the p-substrate. C_W is n-well to p-substrate junction capacitance.

3.1.4.2 C_{max}/C_{min} ratio

From Eq. 3.37, the C_{max}/C_{min} ratio can be derived as:

$$\frac{C_{\max}}{C_{\min}} = \frac{C_j(V_{R,\max})}{C_j(V_{R,\max})} = \left(\frac{V_j + V_{R,\max}}{V_j + V_{R,\min}}\right)^{m_j} \tag{3.39}$$

The exact value of V_j depends on doping levels and temperature. Typical values of V_j at room temperature are 0.8 V- 0.9 V and m_j has a typical value of 0.4 [31]. In order to avoid forward biasing, the $V_{R,min}$ should not lower than the swinging voltage

in the LC tank, by choosing the reverse voltage from 0.6 V to 2.4 V, the C_{max}/C_{min}=1.37. However, this ratio is a theoretical value which can not be realized in practice. Due to the fixed parasitic capacitances, the overall C_{max}/C_{min} ratio for a pn-junction could be much smaller than 1.37.

3.1.4.3 Layout consideration

Eq. 3.37 is a simplified expression for C_j which does not take the parasitics into account. As shown in Fig 3.26, there two important parasitic capacitances, one is the side wall parasitic capacitance ($C_{j,SW}$) which is also tunable by the reverse voltage [33], the other is the fixed interconnection parasitic capacitance which decreases the C_{max}/C_{min} ratio. In order to occupy as small chip area as possible, an array of small junctions are used in the layout instead of a large junction (shown in Fig. 3.27) as the side wall capacitance increases the variable capacitance per unit area. But at the same time, an array of small junctions needs more interconnections and degrades the C_{max}/C_{min} ratio [34], [35].

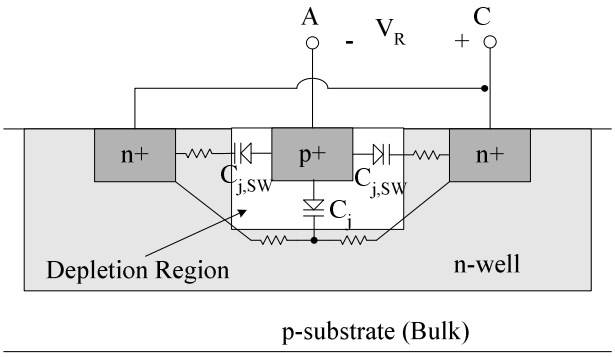

Fig. 3.26 Side wall parasitic capacitance of a p+-to-n-well junction

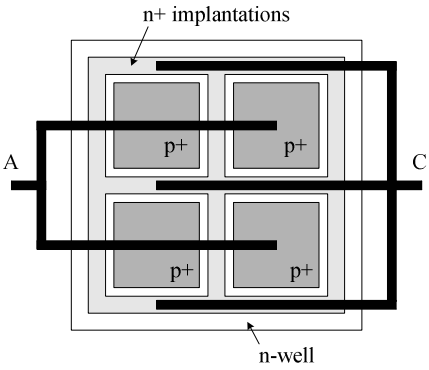

Fig. 3.27 Junctions array

3.1.4.4 Varactor design example

A well designed junction varactor array is shown in Fig. 3.28, which consists of two varactor arrays working in parallel mode. Table 3.5 shows the geometries of the designed junction varactor array.

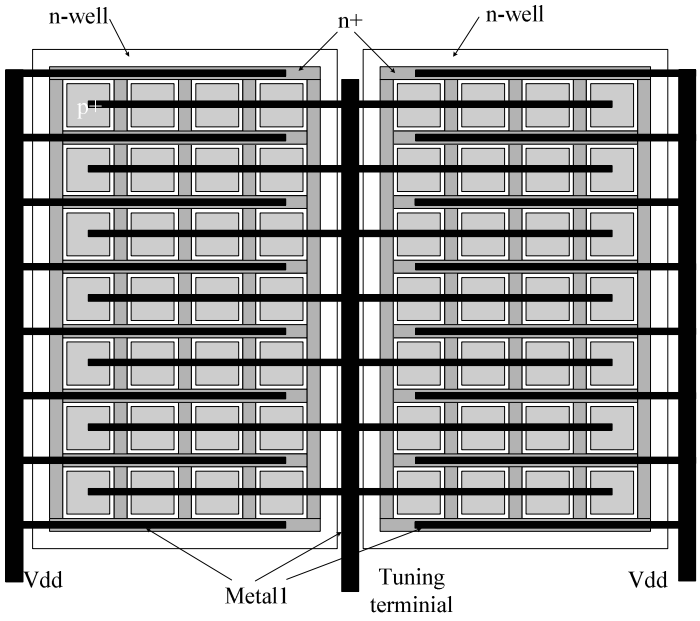

Fig. 3.28 A p+-to-n-well junction varactor array example

Table 3.5
The geometries of the designed junction varactor array

Symbol	Comment	Value
L	length of the junction cell	5.8 μ m
W	width of the junction cell	5.8 μ m
Column	junction array columns	8
Row	junction array rows	7

The simulation result of the junction varactors is shown in Fig.3.29. As seen from the figure, C_{max}=2.825 pF and C_{min}=2.550 pF. The C_{max}/C_{min} ratio is 1.11, which is less than the theoretical value of 1.37. As will be seen later, this ratio determines tuning frequency range of the filter.

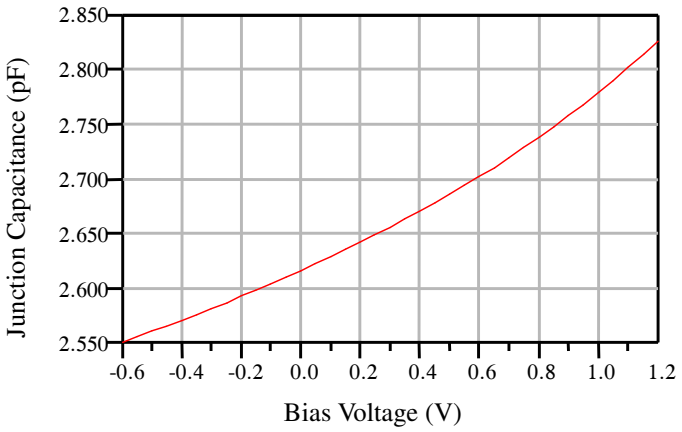

Fig.3.29 Junction capacitance versus bias voltage

3.1.5 Q compensation technique

As discussed in previous sections, the series resistance loss of the on-chip inductor dominates the losses in the LC tank, which must be compensated in order to get the desired selection requirements of the filter. This section explains how loss compensation or equivalently negative resistance circuits can be designed for

Q-enhancement of the LC resonators.

As shown in Fig. 3.30, a negative conductance G_n is introduced in parallel to the resonant tank, where R_{eq} is the equivalent parallel resistance of the resonant tank after compensation. R_{eq} can be expressed as:

$$R_{eq} = \frac{R_p}{1 - G_n R_p} \tag{3.40}$$

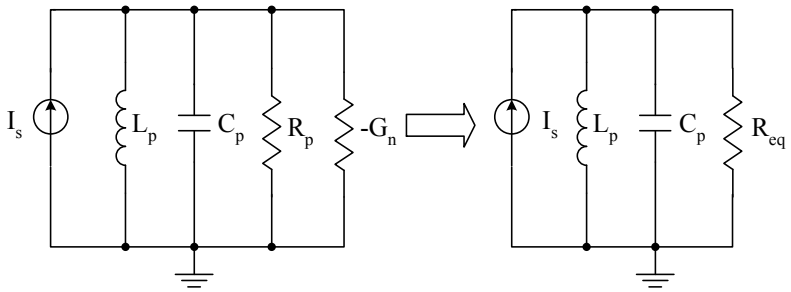

Fig. 3.30 A parallel LC resonant tank compensated with negative conductance

The quality factor Q_c of the Q-enhanced LC resonator is:

$$Q_c = R_{eq}\sqrt{\frac{C_p}{L_p}} \tag{3.41}$$

The impedance of the LC tank is:

$$Z(s) = \frac{1}{\frac{1}{sL_p} + sC_p + \frac{1}{R_{eq}}} = \frac{sL_p R_{eq}}{s^2 L_p R_{eq} C_p + sL_p + R_{eq}} \tag{3.42}$$

The quality factor of the Q-enhanced resonator Q_c can be set arbitrary large by tuning the G_n approaching $1/R_p$. As discussed in Section 3.1.1.4, the power gain of the input LNA depends on the load impedance which is the impedance of the LC tank in this case.

A cross-coupled differential pair given in Fig. 3.31 is a simple way to achieve a negative conductance [36]. Fig. 3.32 gives the equivalent small signal representation

of the circuit. As seen from Fig. 3.32, the negative conductance provided by the cross-coupled differential pair can be found as:

$$Z_{eq} = \frac{V_{in}^{+}}{g_m V_{in}^{-}} = \frac{\frac{V_{in}}{2}}{g_m \frac{-V_{in}}{2}} = -\frac{1}{g_m} \tag{3.43}$$

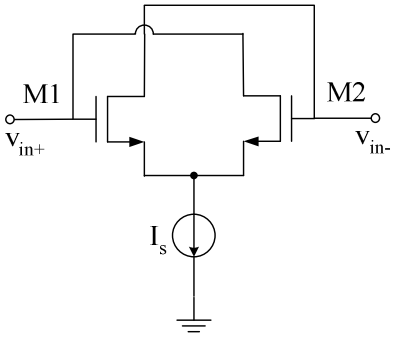

Fig. 3.31 A cross-coupled differential pair

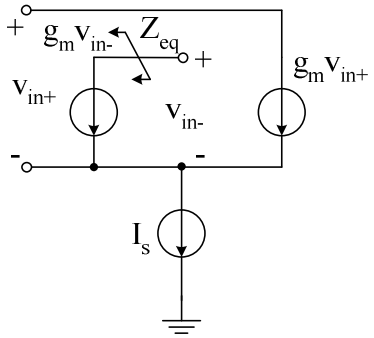

Fig. 3.32 The small signal equivalent of a cross-coupled differential pair

3.1.6 Noise analysis of the Q-enhanced LC resonator

A simplified schematic with noise sources of the Q-enhanced LC resonator is shown in Fig 3.33. As seen from Fig 3.33, there are three noise sources in the Q-enhanced LC resonator: the thermal noises of transistor M1 & M2 and the thermal noise of the parallel equivalent resistor R_P. The contributions from these noises can be computed by calculating the different noise voltages resulting from each noise source.

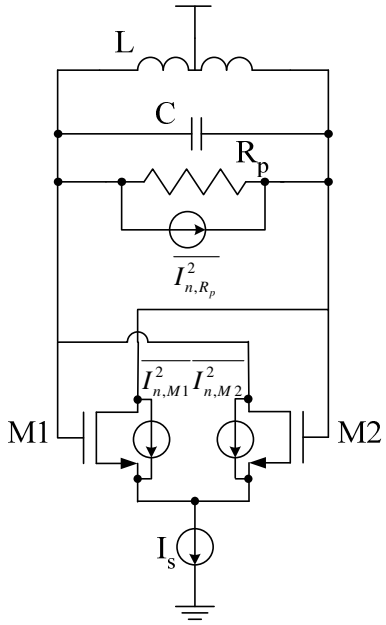

Fig. 3.33 Q-enhanced LC resonator with noise sources

$$\overline{v_{n,out}^2}\Big|_{M1,M2} = \left(\frac{Z_{\text{tank}}}{2}\right)^2 \overline{I_{n,M1,M2}^2} \tag{3.45}$$

$$\overline{v_{n,out}^2}\Big|_{R_p} = Z_{\text{tank}}^2 \overline{I_{R_p}^2} \tag{3.46}$$

$$\overline{v_{n,out}^2} = \overline{v_{n,out}^2}\Big|_{M1} + \overline{v_{n,out}^2}\Big|_{M2} + \overline{v_{n,out}^2}\Big|_{R_p} = Z_{\text{tank}}^2\left(\frac{1}{2}\overline{I_{n,M1,M2}^2} + \overline{I_{R_p}^2}\right) \tag{3.47}$$

From Eq. 3.47, noise model of the Q-enhanced LC resonator can be simplified as shown in Fig 3.34. The equivalent noise current is:

$$\overline{I_{n,\text{tank}}^2} = \frac{\overline{v_{n,out}^2}}{Z_{\text{tan}\,k}^2} = 2kT\gamma g_{do}\Delta f + 4kT\gamma\Delta f / R_p \tag{3.48}$$

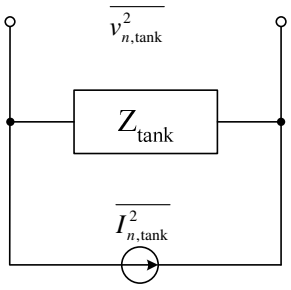

Fig. 3.34 Equivalent noise model of the Q-enhanced noise LC resonator

3.1.7 Linearity Consideration of the Second Order Filter

In RF circuit design, trade-offs exist between noise, linearity and power gain. Noise performance can be improved by increasing the gain of the circuit, but at the same time, high gain causes linearity degradation. In this design, the non-linearity is contributed mainly from the Q-enhancement circuit. In this section, a couple of methods will be provided to improve the filter linearity.

3.1.7.1 Non-linear characteristic of the MOS device

The drain current I_d of a MOS device is modeled as [37]:

$$I_{ds} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 \tag{3.49}$$

where μ is the mobility of the majority carrier, C_{ox} is the gate oxide thickness, W/L is the width to length ratio, V_{GS} is the gate to source bias voltage, V_{DS} is the drain to source bias voltage, and V_T is the threshold voltage. For a simple differential pair shown in Fig 3.35, the drain current I_{ds1}, I_{ds2} can be expressed as:

$$I_{ds1} = \frac{1}{2}\beta\left(\frac{v_{in}}{2} + V_{GS} - V_T\right)^2 \tag{3.50}$$

$$I_{ds2} = \frac{1}{2}\beta\left(-\frac{v_{in}}{2} + V_{GS} - V_T\right)^2 \tag{3.51}$$

where
$$\beta = \mu C_{ox}\frac{W}{L} \tag{3.52}$$

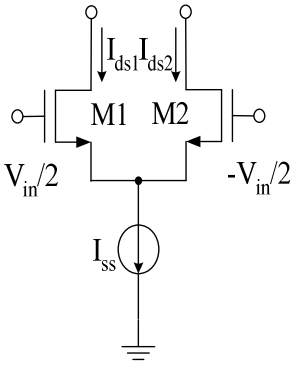

Fig. 3.35 A simple differential pair

From Eq. 3.50 and 3.51:

$$v_{in} = \left(\frac{v_{in}}{2} + V_{GS} - V_T\right) - \left(-\frac{v_{in}}{2} + V_{GS} - V_T\right) = \left(\frac{2I_{ds1}}{\beta}\right)^{1/2} - \left(\frac{2I_{ds2}}{\beta}\right)^{1/2} \tag{3.53}$$

And
$$I_{ds1} + I_{ds2} = I_{ss} \tag{3.54}$$

By substituting Eq. 3.54 into Eq. 3.53 and forming a quadratic, the solution for I_{ds1} and I_{ds2} can be obtained as:

$$I_{ds1} = \frac{I_{ss}}{2} + \frac{I_{ss}}{2}\left[\frac{\beta \cdot v_{in}^2}{I_{ss}} - \frac{\beta^2 v_{in}^4}{4I_{ss}^2}\right]^{1/2} \tag{3.55}$$

$$I_{ds2} = \frac{I_{ss}}{2} - \frac{I_{ss}}{2}\left[\frac{\beta \cdot v_{in}^2}{I_{ss}} - \frac{\beta^2 v_{in}^4}{4I_{ss}^2}\right]^{1/2} \tag{3.56}$$

Assuming the two MOS transistors are working in the saturation region, the output current I_o of the differential-pair is:

$$I_o = I_{ds1} - I_{ds2} = I_{ss}\left[\frac{\beta \cdot v_{in}^2}{I_{ss}} - \frac{\beta^2 v_{in}^4}{4I_{ss}^2}\right]^{1/2} \tag{3.57}$$

The G_m of the differential-pair is then:

$$G_m = \frac{\partial I_o}{\partial v_{in}} = \left[\beta I_{ss} - \frac{\beta^2}{4} v_{in}^2 \right]^{1/2} - \frac{\beta^2}{2I_{ss}} \left[\frac{1}{4\beta \cdot I_{ss} - \beta^2 \cdot v_{in}^2} \right]^{1/2} \cdot v_{in}^2 \tag{3.58}$$

$$G_m(\max) = \left. \frac{\partial I_o}{\partial v_{in}} \right|_{v_{in}=0} = \left(\beta \cdot I_{ss} \right)^{1/2} \tag{3.59}$$

From Eq. 3.58, for small input signals, the G_m is constant. However, for large input signals, G_m drops and becomes non-linear. As a result, linearization techniques for G_m-cells are required.

3.1.7.2 Different types of linearization techniques

1) Source-degeneration with resistor

One of the commonly used techniques for improving the linearity of a G_m-cell is the source degeneration shown in Fig. 3.36 [38].

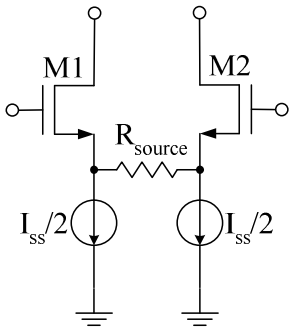

Fig. 3.36 Source degeneration with resistor

The effective G_m of this G_m-cell is:

$$G_m = \frac{g_m}{1 + g_m R_{source}} \tag{3.60}$$

In the equation, g_m is the tranconductance of the differential pair before degeneration. The linearity depends on the choice of R_{source}. If a large source resistor is

employed, the linearity can be improved at the expense of a reduction in G_m. The drawback of this method is that the source resistor consumes power and the resistor also degrades the noise performance.

2) Source-degeneration by using varying bias triode transistors

Another choice in source-degeneration is to use varying bias triode transistors. Transistors M_3 and M_4 shown in Fig. 3.37 are biased in their triode regions and act as resistors [38]. The small-signal source resistance of a MOS transistor can be expressed as:

$$r_{ds} = \frac{1}{g_m} = \frac{1}{\mu C_{ox} \frac{W}{L} V_{eff}} \tag{3.61}$$

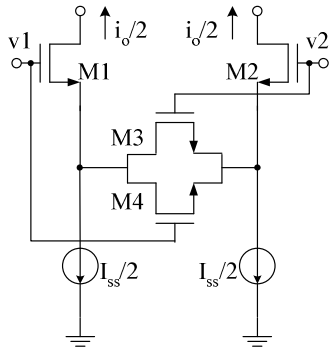

Fig. 3.37 Source-degeneration by using varying bias triode transistors

The small-signal output current of the circuit can be calculated by:

$$i_o = \frac{v_1 - v_2}{r_{ds1} + r_{ds2} + (r_{ds3} \| r_{ds4})} \tag{3.62}$$

By defining G_m as $i_o/(v_1-v_2)$:

$$G_m = \frac{1}{r_{ds1} + r_{ds2} + (r_{ds3} \parallel r_{ds4})} = \frac{4k_1 k_3 V_{eff1}}{k_1 + 4k_3} = \frac{4k_1 k_3 \sqrt{I_1}}{(k_1 + 4k_3)\sqrt{k_1}} \tag{3.63}$$

where

$$k = \frac{\mu C_{ox}}{2}\frac{W}{L} \tag{3.64}$$

G_m can be tuned by changing the bias current I_{ss}. Other two types of circuits using triode transistors degeneration are shown in Fig 3.38. The comparison of three types of linearization techniques using triode transistors is listed in Table 3.6.

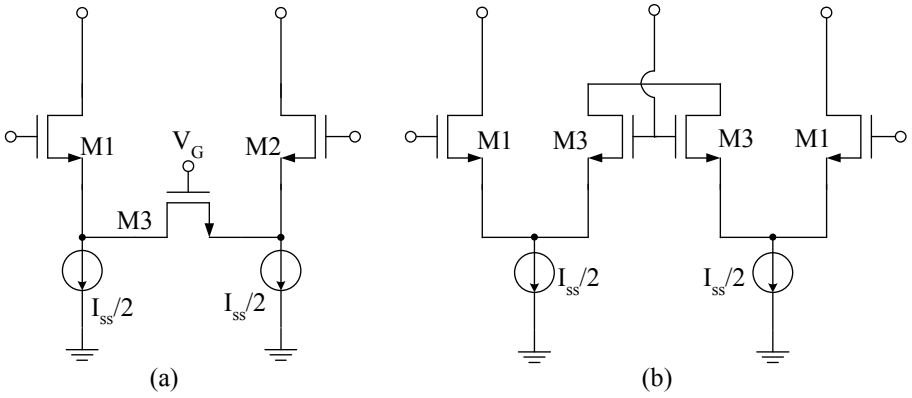

Fig. 3.38 (a) Source degeneration with transistor biased at triode region and (b) with saturated transistors

Table 3.6
Comparison of three types of linearization techniques

Figure	Transconductance	Properties
3.37	$G_m = \frac{4k_1k_3\sqrt{I_1}}{(k_1+4k_3)\sqrt{k_1}}$	Low sensitive to common-mode input signals. The linear ranges is limited to $V_{in}<V_{DSAT}$
3.38(a)	$G_m = \frac{g_{m1}}{1+g_{m1}R}$ $R = 1/\mu C_{ox}(V_{GS}-V_T)$	Highly sensitive to common-mode input signals. For better linearity large V_{GS3} voltages are required. Large tuning range if V_G is used.
3.38(b)	$G_m = \frac{g_{m1}}{1+g_{m1}/g_{m3}}$ [39]	Low sensitive to common-mode input signals. Limited linearity improvement. More silicon area is required.

3.1.8 Second order differential filter implementation

The fully integrated second order differential filter for personal wireless communication applications is implemented in this section. This second order filter is also the building block for the proposed sixth order bandpass filter which provides much more out-of-band attenuation and image rejection ability.

This section combines all the results of the previous sections to design a fully integrated front-end filter for wireless communications.

3.1.8.1 Filter topology

The block diagram and the schematic diagram of the designed second order filter are shown in Fig. 3.39 and Fig. 3.40 respectively. The input stage uses a source degenerated LNA (implemented in differential mode) which is designed in Section 3.1.2. The LC tank consists of an inductor and a varactor. The inductor is the differential on-chip spiral inductor designed in Section 3.1.3 and the varactor is an array of small junctions designed in Section 3.1.4. The Q-enhancement circuit is the cross-coupled different pair discussed in Section 3.1.5. Linearization techniques discussed in Section 3.1.7 are employed to improve the linearity. The bias and output buffer circuits are not shown in the schematic.

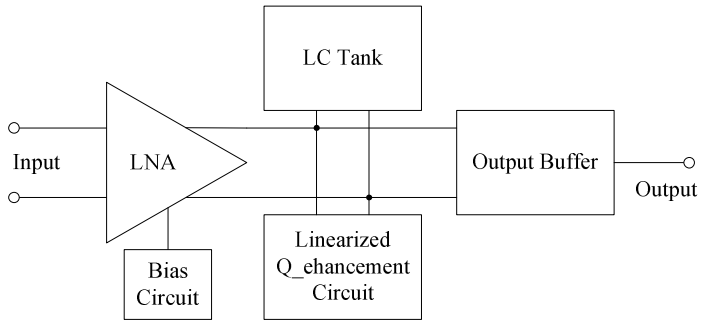

Fig. 3.39 Block diagram of the designed second order bandpass filter

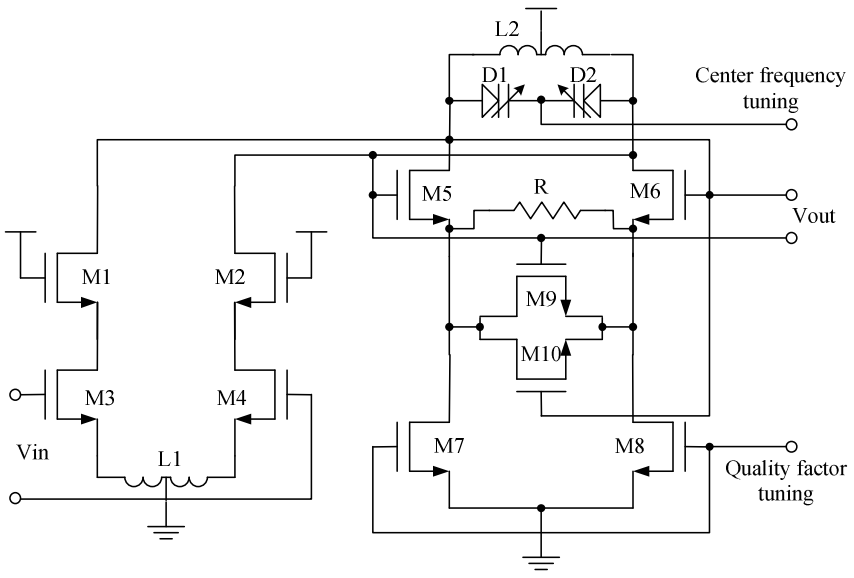

Fig 3.40 Schematic diagram of the second order differential filter

3.1.8.2 Filter simulation results

The second order differential filter was designed under the Cadence environment and the schematic was simulated under ADS dynamic link for Cadence.

1) Tuning ability:

Using the equations in Table 3.6, the G_m of the designed Q compensation circuit can be expressed as:

$$G_m = \frac{4k_5k_9\sqrt{I_1}}{(k_5+4k_9)\sqrt{k_5}+4Rk_5k_9\sqrt{I_1}} \tag{3.65}$$

where I_1 is the current flow through M5 and M7, R is the source degeneration resistor and k_5, k_9 are the process parameters of M5 and M9 defined by Eq. 3.64 respectively. At resonate frequency, the overall tank impedance is $R_P \parallel (-1/G_m)$, where R_P is the parallel equivalent of the tank loss. The tank impedance can be expressed as:

$$Z_{\text{tank}} = \frac{R_P(k_5+4k_9)\sqrt{k_5}+4RR_Pk_5k_9\sqrt{I_1}}{(k_5+4k_9)\sqrt{k_5}+4(R+R_P)k_5k_9\sqrt{I_1}} \tag{3.66}$$

From Section 3.1.3.4, the parallel equivalent resistance of the designed inductor is equal to 256.7 ohms which can be considered to be the tank loss R_P. The tank impedance is a function of the current I_1 which is illustrated in Fig. 3.41.

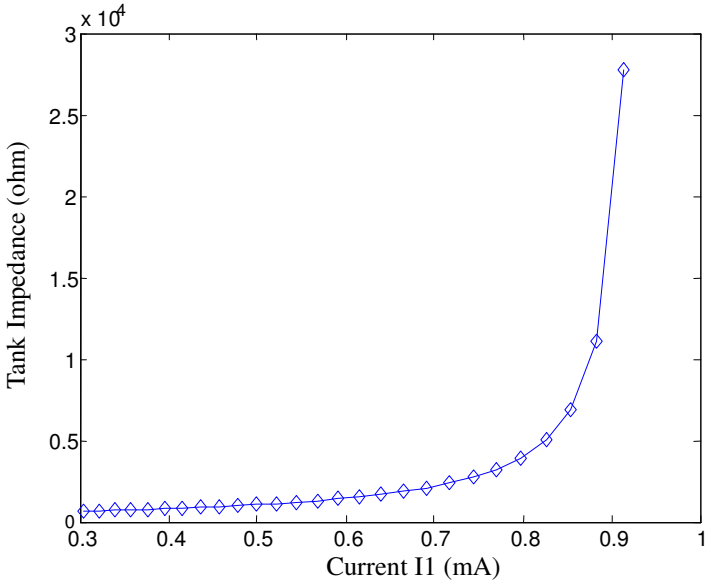

Fig. 3.41 Tank impedance versus current I_1

From Eq. 3.49 and 3.64, I_1 can be expressed as:

$$I_1 = k_7 (V_{GS7} - V_T)^2 \tag{3.67}$$

And from Eq. 2.17, quality factor of a second order tank can be expressed as:

$$Q = \frac{Z_{\text{tank}}}{\omega_0 L} \tag{3.68}$$

As can be seen from Eq. 3.66, 3.67 and 3.68, the Q tuning voltage changes the current I_1, thus changes the tank impedance and the quality factor of the filter [40].

k_7 is the process parameters of M7 defined by Eq. 3.64, V_{GS7} is the gate to source voltage of M7 and M8 in Fig. 3.40 which equals to the quality factor tuning voltage V_q. The calculated Q tuning versus V_q is shown in Fig. 3.42.

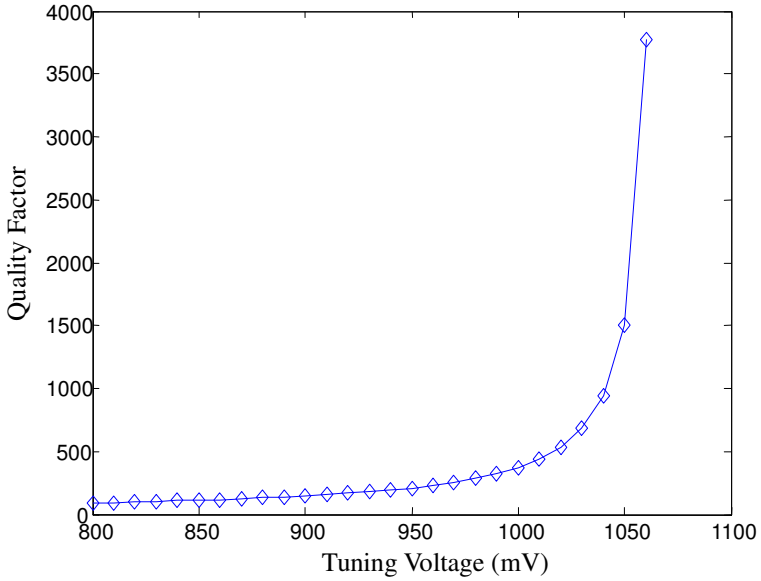

Fig. 3.42 Calculated quality factor tuning

The simulated Q-tuning ability of the filter is demonstrated in Fig. 3.43. In this second order filter, the Q value can be tuned very high when the source degenerated G_m value of the cross-coupled differential pair M5, M6 is tuned approaching to the parallel equivalent conductance of the LC tank loss. As shown in Fig. 3.44 the Q value can exceed 3000 in the simulation. According to Eq. 2.17, the bandwidth of the filter will decrease when Q increases. At the same time, the image rejection will increase as Q increases (shown in Fig. 3.45).

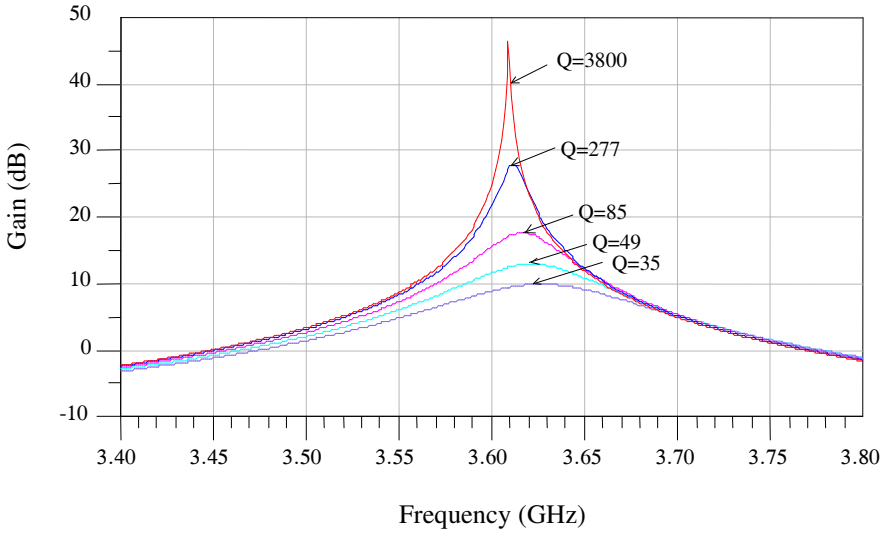

Fig. 3.43 Q tuning ability of the second order filter

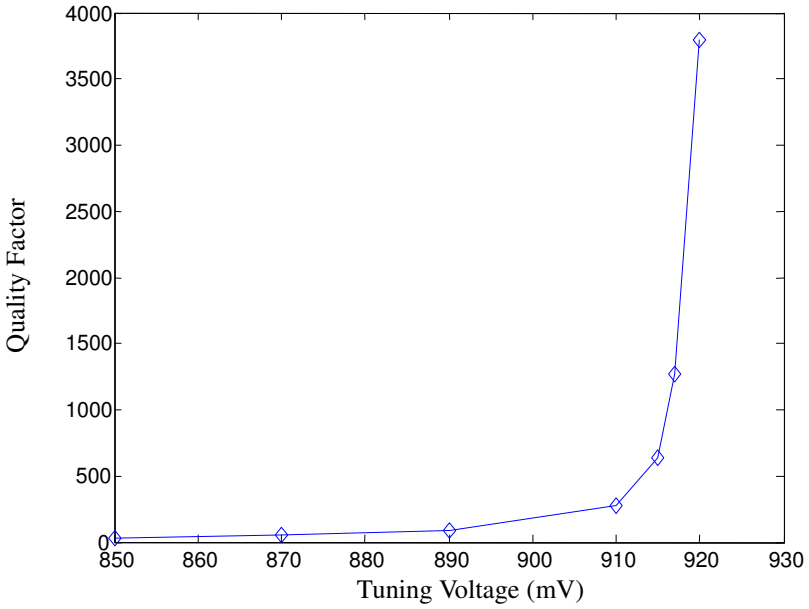

Fig. 3.44 Quality factor of the second order filter versus tuning voltage

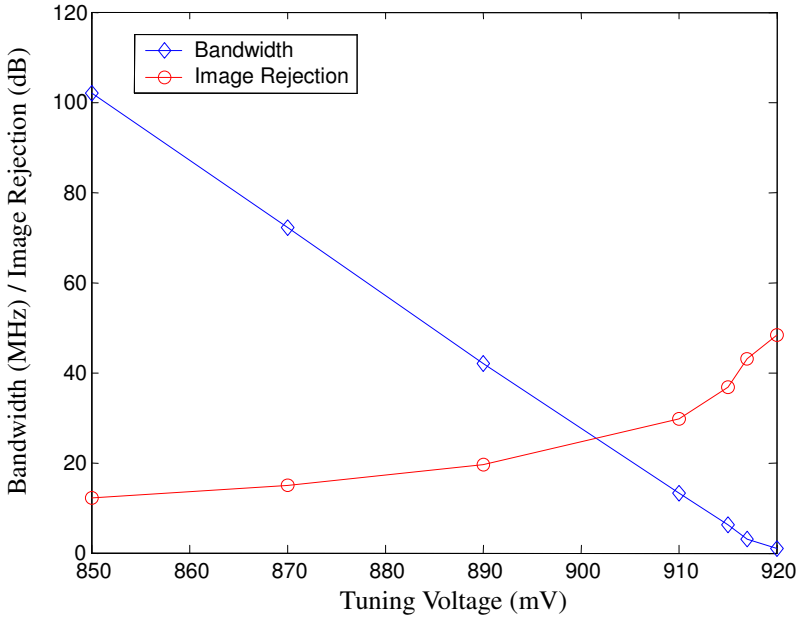

Fig. 3.45 Bandwidth and image rejection of the second order filter versus tuning voltage

The simulated center frequency tuning ability is shown in Fig. 3.46. When the tuning voltage sweeps from -0.6 V to 1.2 V, the center frequency shifts from 3.69 GHz to 3.54 GHz. The tuning range is about 150 MHz.

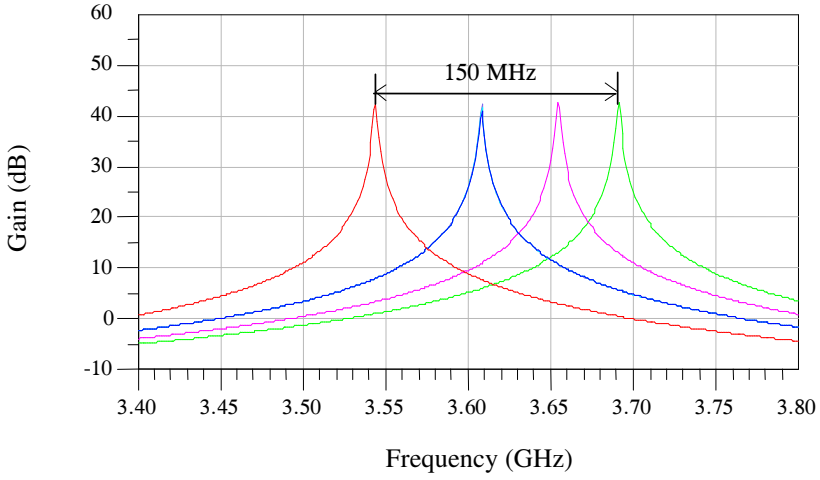

Fig. 3.46 Frequency tuning ability of the second order filter

2) Linearity performance:

Another consideration is the linearity of the filter. The input referenced third order distortion (IIP3) and 1 dB compression point are two important parameters to measure the linearity. In the linearity simulation, the Q of the filter is set at 150 and the center frequency is set at 3.60 GHz. Two tones at 3.595 GHz and 3.605 GHz are used as the fundamental frequencies at the input. The third order products are at 3.615 GHz and 3.585 GHz, both are in the pass band of the filter. Fig. 3.47 shows the fundamental product and third order product at the output of the second order filter. The image rejection at this operation point is 32 dB, IIP3 is -21.5 dBm, 1 dB compression point is -30.5 dBm.

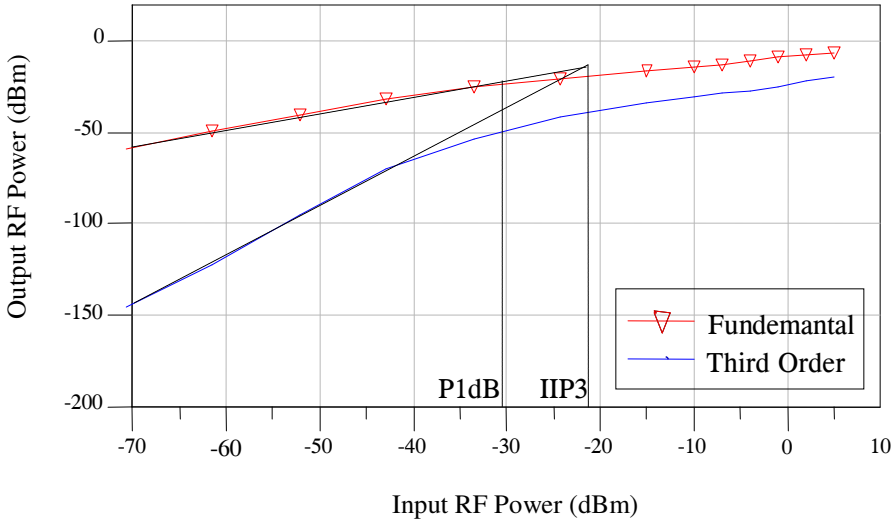

Fig. 3.47 Linearity performance of the second order filter at Q=150, center frequency=3.6 GHz

Fig. 3.48 shows the IIP3 and 1 dB compression point of the filter versus tuning voltage. As can be seen from the figure, tuning up the quality factor of the filter degrades the linearity performance of the filter.

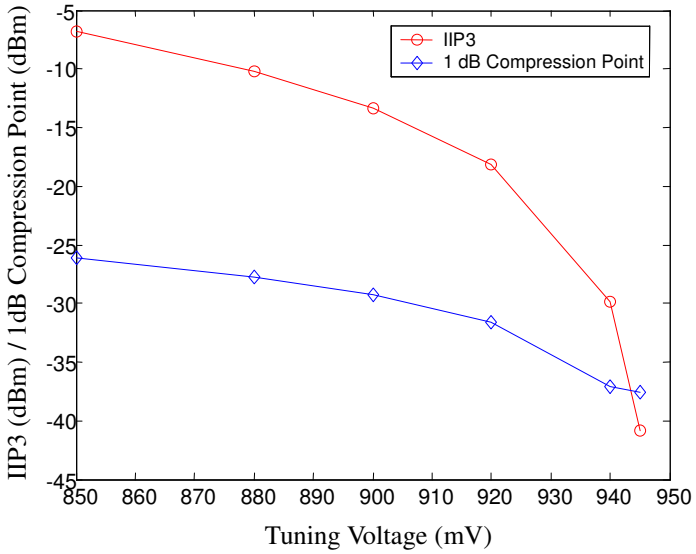

Fig. 3.48 IIP3 and 1 dB compression point of the second order filter versus tuning voltage

From the simulation results shown in Fig. 3.44 and Fig. 3.45, if an image rejection of 50 dB is required, the Q of the filter needs to be tuned to over 4000. At this situation, the bandwidth of the filter is merely 1.2 MHz, which is not suitable for the RF front end of wideband systems. At the same time, as seen from Fig. 3.48 the IIP3 of the filter is less than -42 dBm which indicates that the linearity is unacceptable. In order to fit this second order filter into wideband systems, the Q of the filter needs to be tuned around 50. At this Q, the bandwidth is about 80 MHz and the IIP3 is around -11.5 dBm. However, the image rejection is reduced to 22 dB. An image rejection filter is required to filter out the image signals.

3) Noise performance:

The simulated noise figure of the filter is shown in Fig. 3.49. As seen from the figure, the minimum noise figure appears around center frequency of the filter, 3.6 GHz in this case. The minimum noise figure is 8.65 dB, in which the LNA contributes 2.8 dB

and the Q-enhancement circuit and LC tank contributes 5.85 dB.

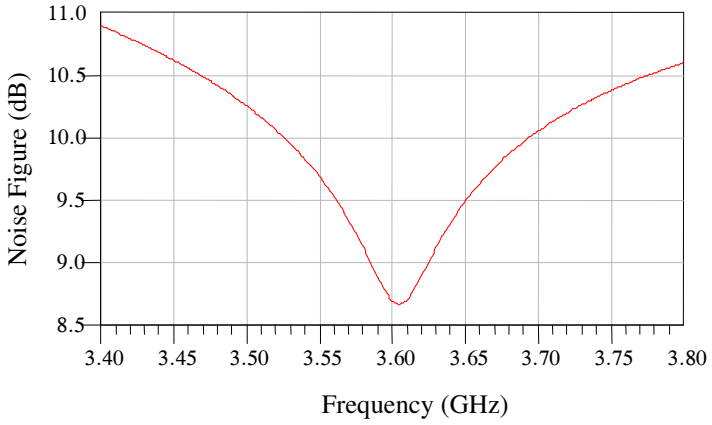

Fig. 3.49 Noise figure of the second order filter

4) Input matching:

In the design, the input matching is calculated to be a perfect match to 50 ohm. The simulated result is shown in Fig. 3.50. At the center frequency point, the input reflection coefficient S11 is -54 dB which can be considered a very good match.

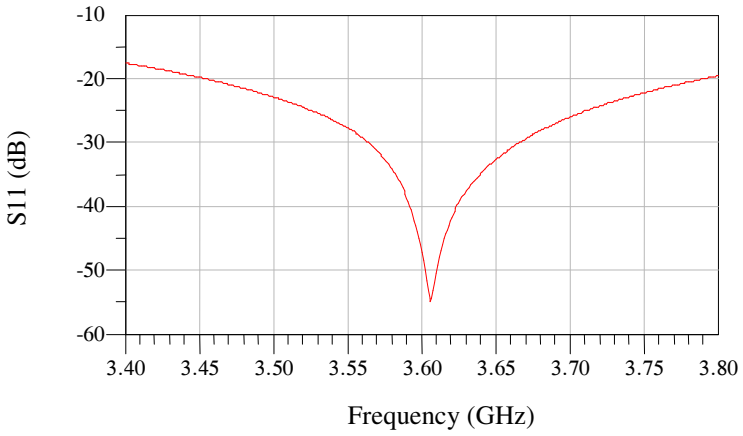

Fig. 3.50 Input matching of the second order filter

3.2 Sixth order Bandpass Filter Design

Section 3.1.8 shows a second order bandpass filter which may be used in the front end for RF filtering. The image rejection in Fig. 3.45 for the second order filter

with 100 MHz bandwidth is about 25 dB, which can not satisfy the specification, an off-chip image rejection filter is needed between the second order filter and a mixer in the receiver to filter out image signals. One of the design goals is to eliminate the off-chip image rejection filter and implement a fully integrated RF front end. To provide enough image rejection on-chip, the second order filter that designed in the pervious section will be used as part of the proposed sixth order filter design. In this section, the design methodology will be discussed and the circuit schematic will be presented. The simulation results of the designed sixth order bandpass filter will be shown to demonstrate its performance.

3.2.1 Topology of the sixth order filter

As shown in Fig. 3.51, the sixth order filter is realized by cascading three stages of the second order filters. They are coupled together using ac-coupling capacitors. There is a LNA in front of each stage of the resonator. This topology is referred as active resonator coupling which shows that the resonators can be coupled without affecting each others impedances [41]. In this case, the individual resonator's frequency selectivity is not affected by other resonators.

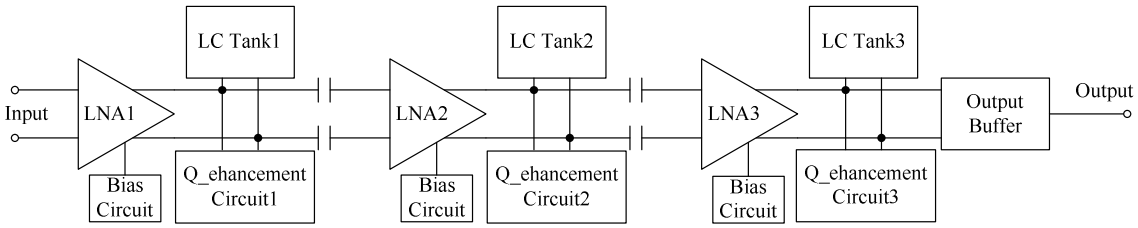

Fig. 3.51 Sixth order filter topology

3.2.2 Gain and quality factor distribution

In order to operate with a supply voltage as low as 1.8 V, the gain distribution of the three stages is very important in order not to saturate the following stages. At the same time, the distribution of the gain will affect the noise performance and linearity of the sixth order filter. The Friis's equation on system noise factor (F_{sys}) (3.69) is presented here for reference [42], where noise factor of each stage is calculated with respect to the source impedance of the next stage. F_i and G_i are the noise factor and the available gain of the i^{th} stage.

$$F_{sys} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_1} + ... + \frac{F_n - 1}{G_1 ... G_{n-1}} \tag{3.69}$$

For a three-stage system, Eq. 3.69 can be simplified to Eq. 3.70.

$$F_{sys} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} \tag{3.70}$$

As illustrated in Eq. 3.70, noises of the second and third stages are attenuated by their gains. Noise performance of the system is optimized by maximizing the gain of the first stage.

Distribution of the gain in each stage also affects linearity performance of the whole circuit. Fig 3.52 shows the signal pass two cascaded nonlinear systems.

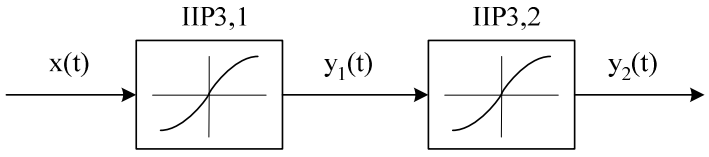

Fig. 3.51 Linearity of a cascaded system

Assume that the input signal is x(t), output of the first stage is given in Eq. 3.71 and, output of the second stage is given in Eq. 3.72:

$$y_1(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \tag{3.71}$$

$$\begin{aligned} y_2(t) &= b_1 y_1(t) + b_2 {y_1}^2(t) + b_3 {y_1}^3(t) \\ &= b_1[a_1 x(t) + a_2 x^2(t) + a_3 x^3(t)] \\ &+ b_2[a_1 x(t) + a_2 x^2(t) + a_3 x^3(t)]^2 \\ &+ b_3[a_1 x(t) + a_2 x^2(t) + a_3 x^3(t)]^3 \end{aligned} \tag{3.72}$$

If only the first order term and the third order term are considered, then:

$$y_2(t) = a_1 b_1 x(t) + (a_3 b_1 + 2a_1 a_2 b_3 + a_1^3 b_3) x^3(t) + \ldots \tag{3.73}$$

By using Eq. 2.10, the input amplitude at the IIP3 point A_{IP3} is:

$$A_{IP3} = \sqrt{\frac{2}{3}\left|\frac{a_1 b_1}{a_3 b_1 + 2a_1 a_2 b_2 + a_1^3 b_3}\right|} \tag{3.74}$$

A worst case estimate is:

$$\begin{aligned} \frac{1}{A_{IP3}^2} &= \frac{3}{2}\frac{\left|a_3 b_1\right| + \left|2a_1 a_2 b_2\right| + \left|a_1^3 b_3\right|}{\left|a_1 b_1\right|} \\ &= \frac{1}{A_{IP3,1}^2} + \frac{3a_2 b_2}{b_1} + \frac{a_1^2}{A_{IP3,2}^2} \end{aligned} \tag{3.75}$$

As a_1 increase, the overall IIP3 decreases. With higher gain in the first stage, the second stage has larger input levels; producing much greater third order intermodulation products thus decreases the overall IIP3. In differential mode, a2, b2≈0, the A_{IP3} of the overall circuit can be simplified to:

$$\frac{1}{A_{IP3}^2} \approx \frac{1}{A_{IP3,1}^2} + \frac{a_1^2}{A_{IP3,2}^2} \tag{3.76}$$

For more stages:

$$\frac{1}{A_{IP3}^2} \approx \frac{1}{A_{IP3,1}^2} + \frac{a_1^2}{A_{IP3,2}^2} + \frac{a_1^2 b_1^2}{A_{IP3,3}^2} + \ldots \tag{3.77}$$

a_1 and b_1 in the above equations are the circuit gains of the fundamental

frequencies which can be considered approximately equal to the gain of the circuits G_1 and G_2.

It is easy to see the trade off here; when the gain of the first stage increases, noise performance will improve, but the linearity performance will degrade. In this design, the gains of each stage are set to be G_1, G_2 and G_3. In order to get a compromise between the noise performance and the linearity performance, the ratio among G_1, G_2 and G_3 must be carefully selected. From the simulation results of the second order filter, the noise figure is chosen to be 8.6 dB (the noise factor is 7.24) and IIP3 is chosen to be -15 dBm (A_{IP3} is 0.04 V). The overall gain (G_1+G_2+G_3) is 20 dB. By choosing different values of G_3, a set of curves shown in Fig. 3.53 which demonstrates the relationship between the gain of first stage (G_1) and the overall noise figure of the sixth order filter.

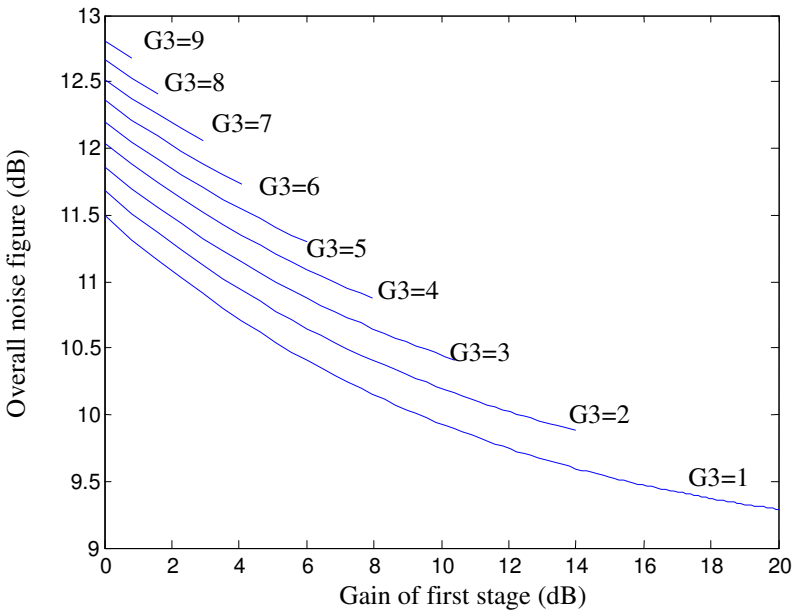

Fig. 3.53 Overall noise figure versus gain of the first stage

Fig. 3.54 demonstrates the relationship between the gain of first stage (G_1) and the overall IIP3 performance.

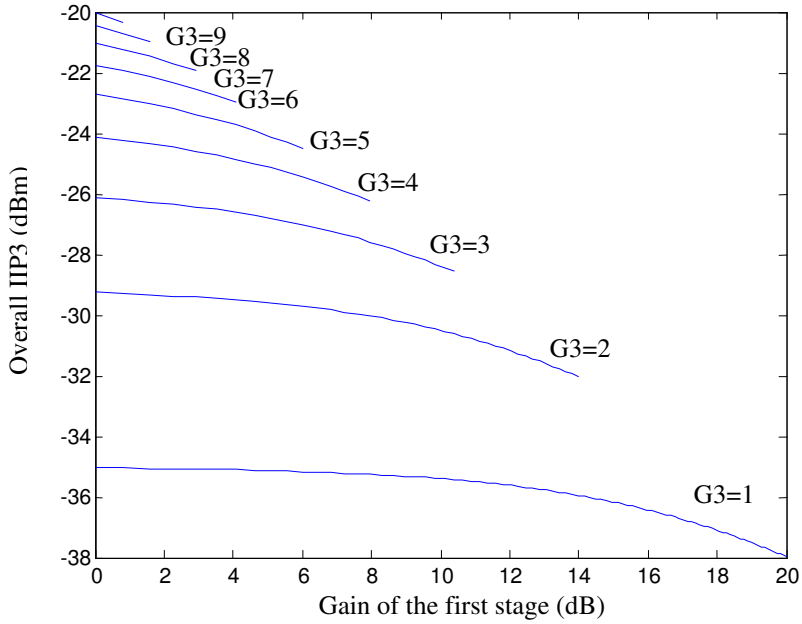

Fig.3.54 Overall IIP3 versus gain of the first stage

The proposed filter requires an IIP3 greater than -30 dBm. When G_3 is chosen to be 6 dB, the IIP3 ranges from -29 dBm to -32 dBm that satisfies the requirement. The noise figure is also limited to 11.7 dB. In this design, the gain of each stage is chosen to be 6 dB, 8 dB and 6 dB. Under this configuration, the IIP3 is -29.7 dBm, the noise factor is 10.6 dB and a compromise between the noise performance and the linearity performance is obtained.

3.2.3 Quality factor and gain tuning

In the design, the gain of the filter is not only determined by the current output of the LNA but also by the impedance of the resonate tank. The gain of each stage can be expressed as:

$$G = \frac{V_{out}}{V_{in}} = g_m Z_{Tank} \tag{3.78}$$

As seen from Eq. 3.68, the quality factor is proportional to the tank impedance

Z_{Tank} thus proportional to the circuit gain.

In this design, the input tranconductance (g_m) of each stage are all set to be equal. The gain and quality factor of the stages can be tuned by changing the impedance of the tank (Z_{Tank}). In order to keep a reasonable gain and quality factor relationship among stages while tuning the quality factor of the circuit, each stage must be tuned accordingly. This makes the filter more difficult to tune and limits its applications. To simplify the Q tuning scheme, only one tuning terminal is used in the design. From Eq. 3.78, 3.66 and 3.67, the gain relationship among stages can be expressed as:

$$G_1 : G_2 : G_3 = Z_{Tank1} : Z_{Tank2} : Z_{Tank3} = \frac{R_P(k_5+4k_9)\sqrt{k_5}+4RR_Pk_5k_9\sqrt{k_{71}}(V_q-V_T)}{(k_5+4k_9)\sqrt{k_5}+4(R+R_P)k_5k_9\sqrt{k_{71}}(V_q-V_T)} :$$
$$\frac{R_P(k_5+4k_9)\sqrt{k_5}+4RR_Pk_5k_9\sqrt{k_{72}}(V_q-V_T)}{(k_5+4k_9)\sqrt{k_5}+4(R+R_P)k_5k_9\sqrt{k_{72}}(V_q-V_T)} : \frac{R_P(k_5+4k_9)\sqrt{k_5}+4RR_Pk_5k_9\sqrt{k_{73}}(V_q-V_T)}{(k_5+4k_9)\sqrt{k_5}+4(R+R_P)k_5k_9\sqrt{k_{73}}(V_q-V_T)} \quad (3.79)$$

In this design, k_5, k_9, R and R_P of each stage are all set to be the same. By changing the width to length ratio of current source MOSFET, k_7 of each stage can be changed to different values. Try using k_{71}:k_{72}:k_{73}=1:1.1:1, the gain distribution is illustrated in Fig. 3.55.

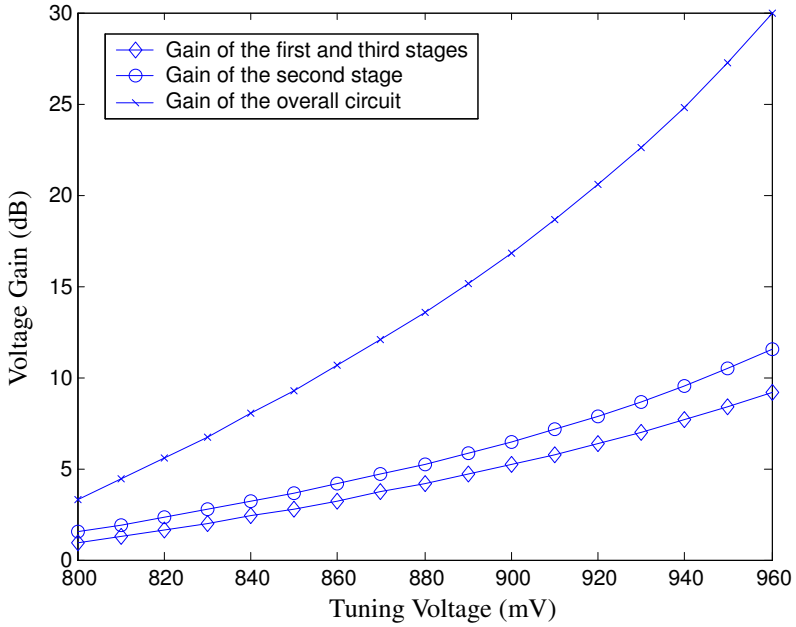

Fig. 3.55 Calculated gain distribution versus Q tuning voltage

The ratio between G_2 and $G_1(G_3)$ is demonstrated in Fig. 3.56.

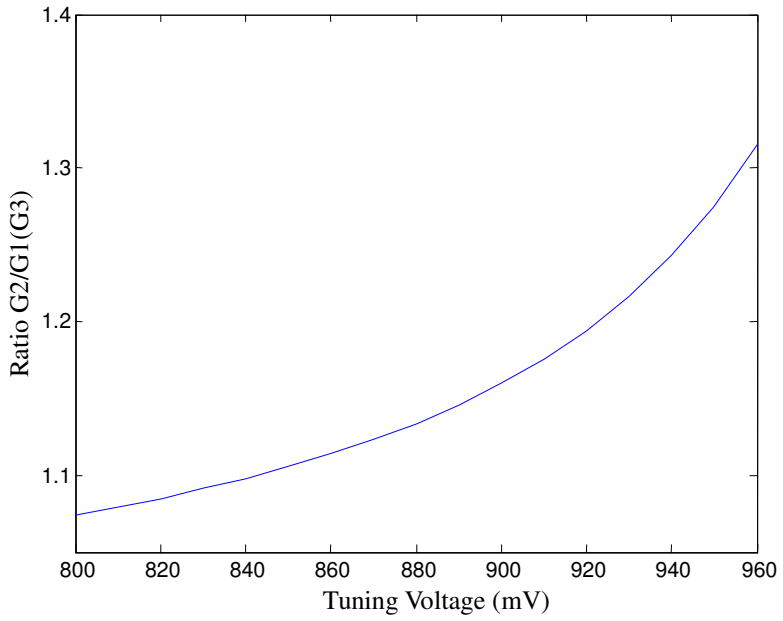

Fig. 3.56 Calculated $G_2/G_1(G_3)$ ratio

As can be seen from Fig. 3.55 and Fig. 3.56, when the overall voltage gain equals to 20 dB, the ratio between G_2 and $G_1(G_3)$ is about 1.25 which fits into the

designed gain relationship G_1:G_2:G_3=1:1.25:1.

3.2.4 Center frequencies distribution

In order to acquire a larger bandwidth, center frequencies of each stage are to be set slightly different. By choosing the center frequencies of each stage, the bandwidth of the overall response can be effectively controlled. Unfortunately the overall gain will be smaller than the combined gain of the three stages because frequency response of the first stage is attenuated by the second stage and so on. The attenuation from the second stage and third stage largely depends on the center frequency spacing of each stage. The attenuation becomes less with a smaller spacing. However, at the same time, the bandwidth of the overall filter also becomes smaller. At the extreme case, when three stages work at exactly the same center frequency, there will be no attenuation, thus maximize the overall gain of the filter. But on the other hand, this configuration minimizes the filter bandwidth. In case the filter is used in wideband applications, some gain must be traded for bandwidth by increasing the spacing among the center frequencies.

Fig.3.57, 3.58, and 3.59 show simulation results of the bandwidth associated with different center frequency spacings.

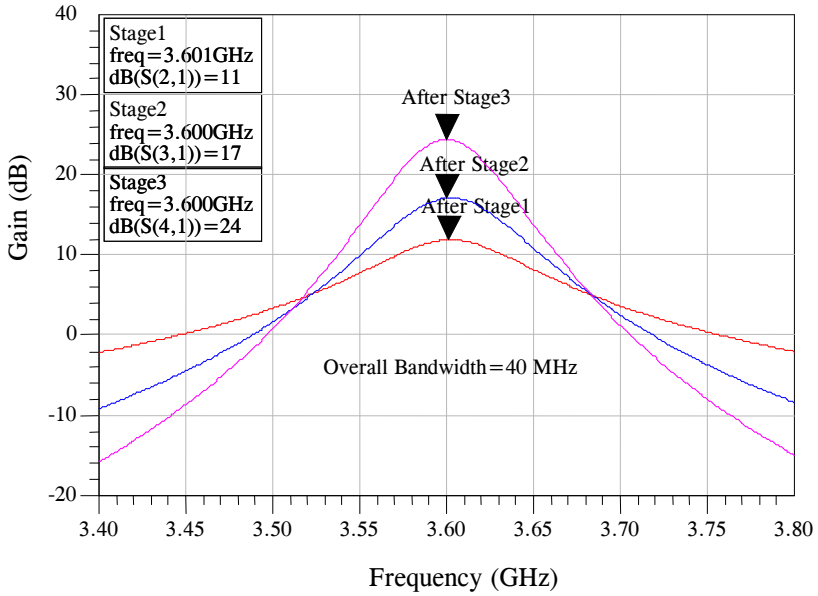

Fig. 3.57 Three stages with the same center frequencies

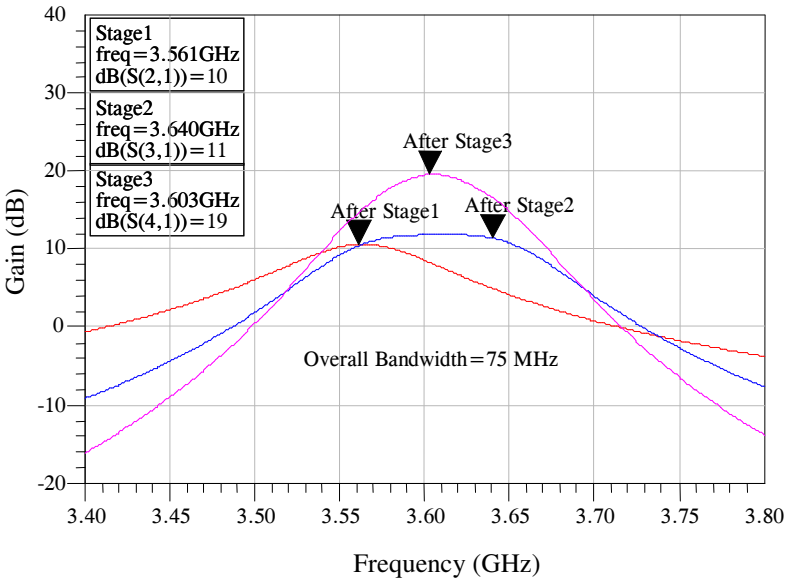

Fig.3.58 Three stages with 40 MHz spacing between center frequencies

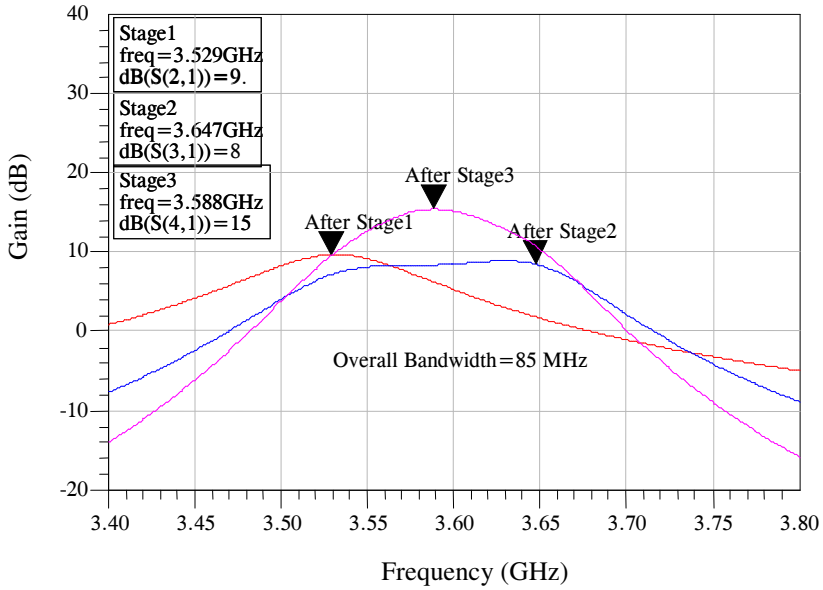

Fig. 3.59 Three stages with 60 MHz spacing between center frequencies

As shown in the simulation results, when three stages are at the same center frequency, the gain of the overall response is the largest, which is 24.4 dB for a bandwidth of 40 MHz (Fig. 3.57). When the spacing between stages is 40 MHz and the bandwidth is 75 MHz, the gain of the overall response is 19.5 dB (Fig. 3.58). When the spacing increasing to 60 MHz, the gain is 15.4 dB and bandwidth is about 85 MHz (Fig. 3.59).

3.2.5 Center frequency tuning

Frequency tuning of the second order filter is implemented by tuning the reverse voltage of the junction diode varactors. In the sixth order filter, there are three resonate tanks; each must be tuned to different center frequency to provide a certain overall bandwidth. This can be done by tuning each stage separately. To simplify the frequency tuning scheme, an innovation method is applied in this design so that only one tuning terminal is used to tune the center frequencies.

In order to set the center frequencies apart, extra capacitances are inserted into the first stage and the third stage. From Eq. 3.29 and 3.37:

$$\omega_n = \sqrt{\frac{LC'_{j0}A_j + LC_{xn}(1+\frac{V_R}{V_j})^{mj}}{(1+\frac{V_R}{V_j})^{mj}}} \tag{3.80}$$

where C_{xn} are the extra capacitances added to each stage. Using C_{x1}=80 fF, C_{x2}=0 and C_{x3}=40 fF, center frequency of each stage is shown in Fig. 3.60. The spacing between stages is shown in Fig. 3.61. As can be seen from this figure, frequency spacing changes with the frequency tuning voltage. The spacing range from 70 MHz to 77.8 MHz, these spacings are in the acceptable range and provide an overall bandwidth between 100 MHz and 150 MHz.

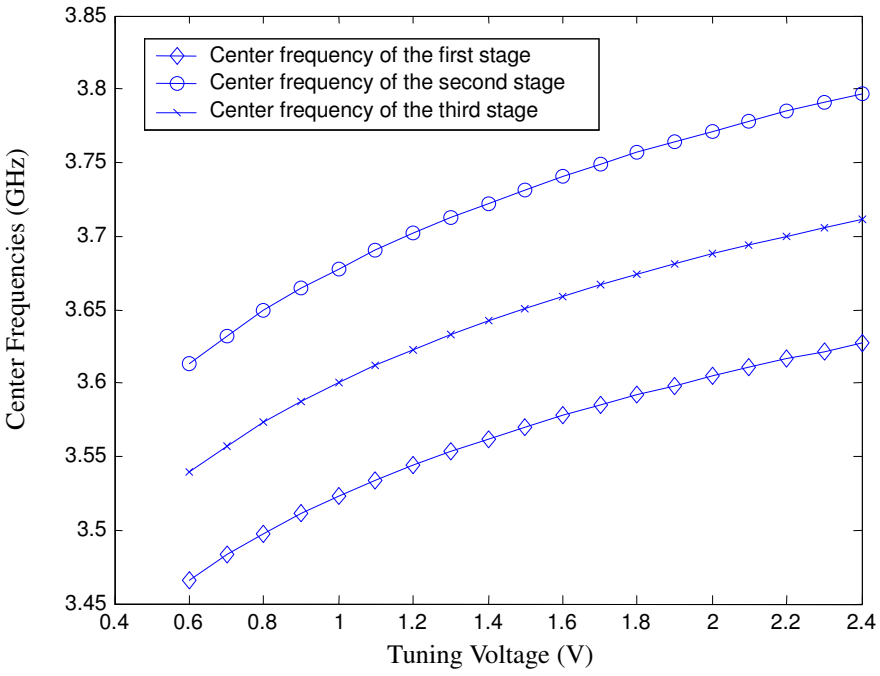

Fig. 3.60 Calculated center frequency of each stage

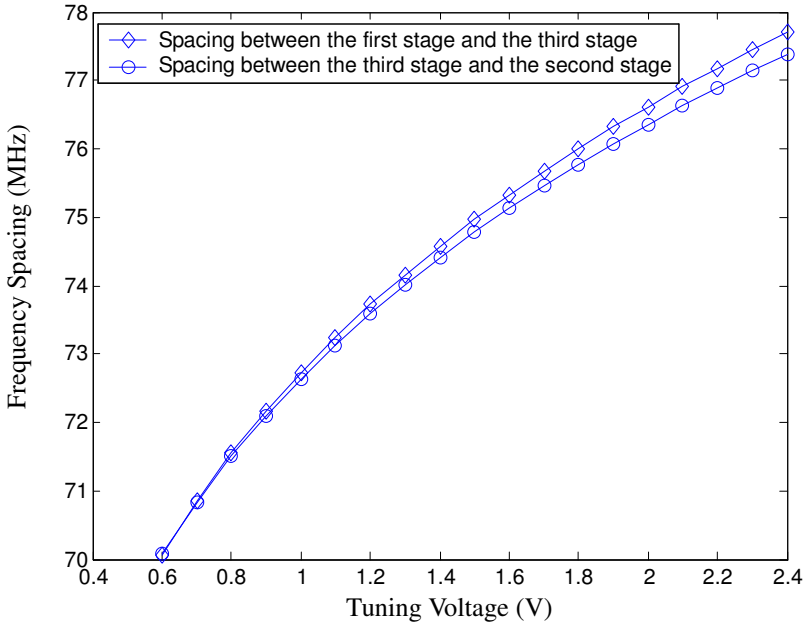

Fig. 3.61 Calculated frequency spacing between stages

3.2.6 Circuit design of the sixth order filter

As shown in Fig. 3.62, the sixth order filter was implemented by cascading three stages of the second order filter. These stages are coupled with ac capacitors. The LNA in each stage is the same, in order to control the gain distribution, the width to length ratios of the current source transistors in each stage are scaled to 1:1.1:1 to satisfy the equation k_{71}:k_{72}:k_{73}=1:1.1:1. Extra capacitances C_{x1} and C_{x2} are added to the first and the third stages to set the center frequencies apart.

All the parameters of the elements in Fig. 3.62 are shown in Table 3.7.

Table 3.7
Parameters of the sixth order bandpass filter

Symbol	Comment	Value
M1, M2, M11, M12, M21, M22	common gate cascade MOSFETs	L=0.18 μm, W=15 μm
M3, M4, M13, M14, M23, M24	input common source MOSFETs	L=0.18 μm, W=15 μm
M5, M6, M15, M16, M25, M26	cross couple differential pairs	L=0.22 μm, W=80 μm
M7, M8, M27, M28	current sources	L=2 μm, W=21.84 μm
M17, M18	current source for second stage	L=2 μm, W=24 μm
M9, M10, M19, M20, M29, M30	triode biased MOSFETs	L=0.22 μm, W=24 μm
L1, L3, L5	source degeneration inductors	2.042 nH
L2, L4, L6	tank inductors	2.042 nH
D1, D2, D3, D4, D5, D6	varactors	5.8 μm×5.8 μm ×4×7
C1, C2, C3, C4	coupling capacitors	0.3 pF
Cx1	extra capacitor for the first stage	35 fF
Cx2	extra capacitor for the third stage	25 fF
R1, R2, R3	source degeneration resistors	35 ohms

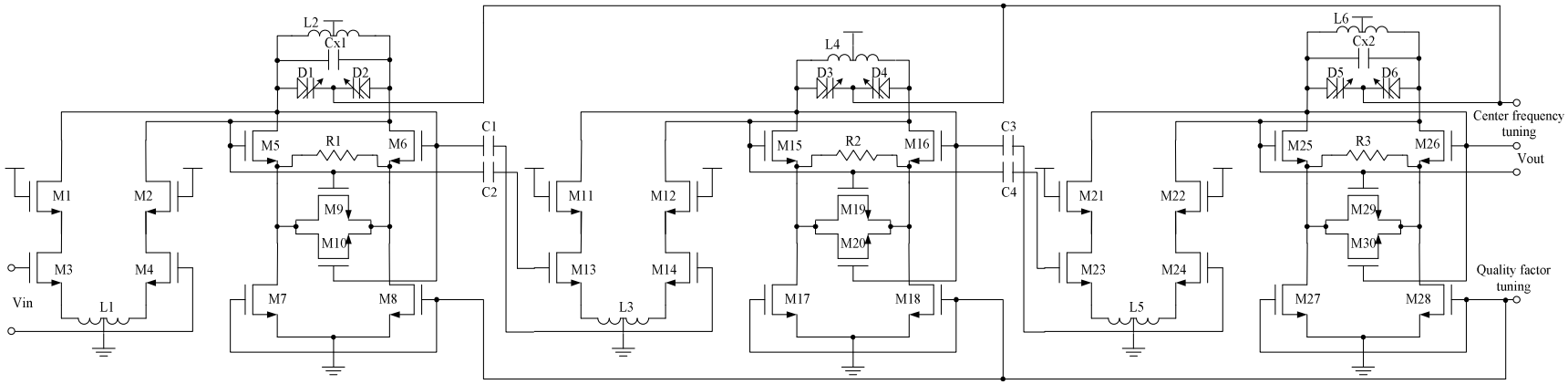

Fig. 3.62 Schematic diagram of the sixth order bandpass filter

3.2.7 Simulation results of the sixth order filter

Q tuning ability

Tuning of the filter gain has effects in changing the bandwidth and image rejection of the filter. Fig. 3.63 shows the bandwidth and gain tuning ability of the sixth order filter.

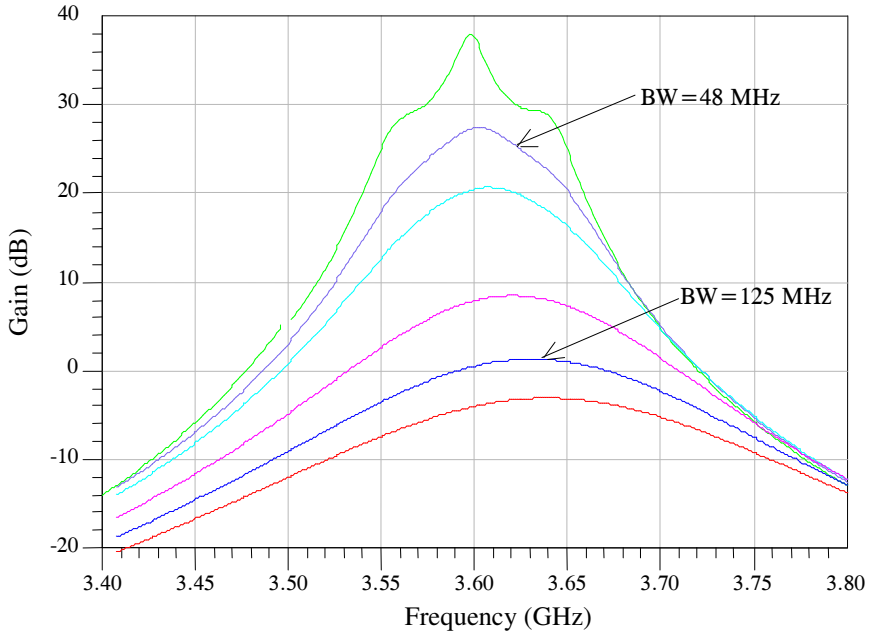

Fig. 3.63 Bandwidth and gain tuning ability of the sixth order filter

As shown in Fig. 3.63, when the gain is tuned to a certain level, ripple appears and at the same time the linearity of the filter degrades. In the design, the maximum gain of the filter is set by the ripple less than 1 dB and the minimum gain of the filter is set to 0 dB. The bandwidth tuning range seen from Fig. 3.63 is 48 MHz to 125 MHz. Fig. 3.64 shows the filter response of each stage under the maximum gain operation. The overall gain of the filter is about 29 dB, and image rejection after each stage is 26 dB, 42 dB and 69 dB.

The frequency spacing of each stage can be also identified from Fig. 3.64, which is about 40 MHz.

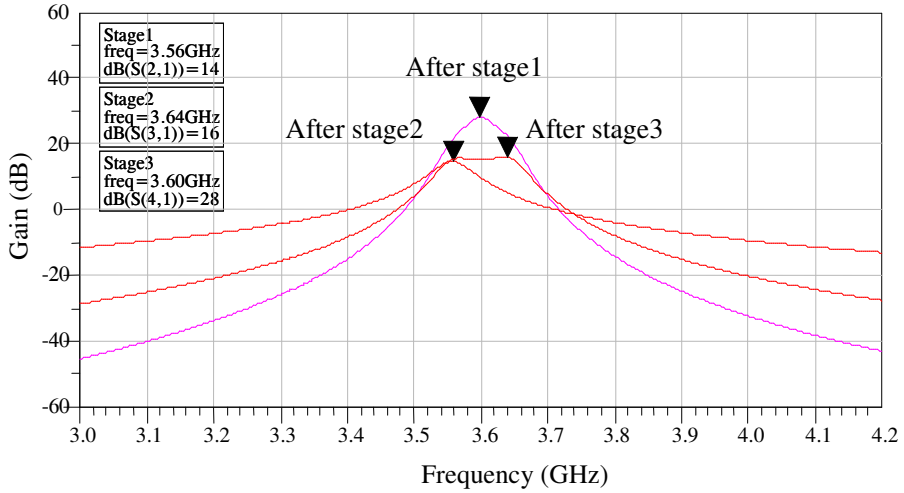

Fig. 3.64 Frequency responses of three stages with maximum gain

By increasing the Q of each stage, the gain of the sixth order filter and the image rejection increase. But at the same time, the bandwidth decreases. Fig. 3.65 shows the tradeoff between the bandwidth and image rejection. As seen from this figure, if a 100 MHz bandwidth is needed, a 50 dB image rejection can be achieved by this sixth order filter.

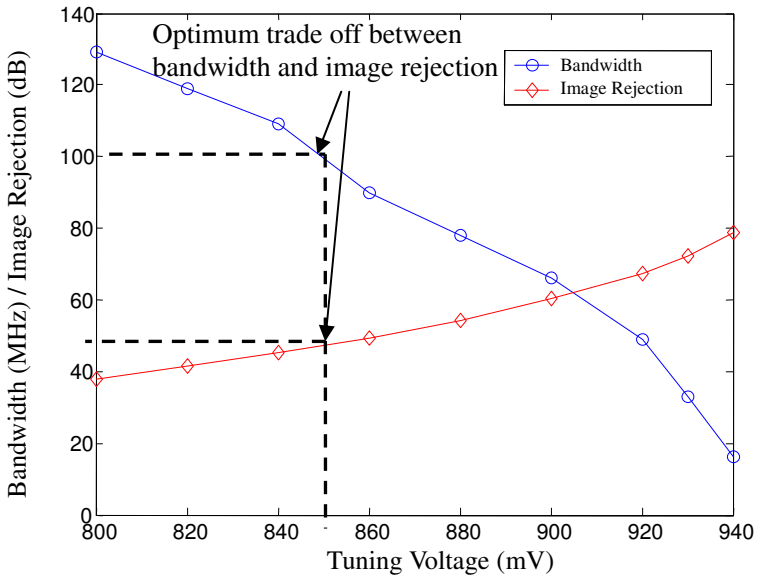

Fig. 3.65 Bandwidth and image rejection versus tuning voltage of the sixth order filter

Frequency tuning ability

As illustrated in Chapter 2, tuning of the center frequency inevitably changes quality factor of the filter. Fig. 3.66 shows a frequency tuning combined with the Q tuning results.

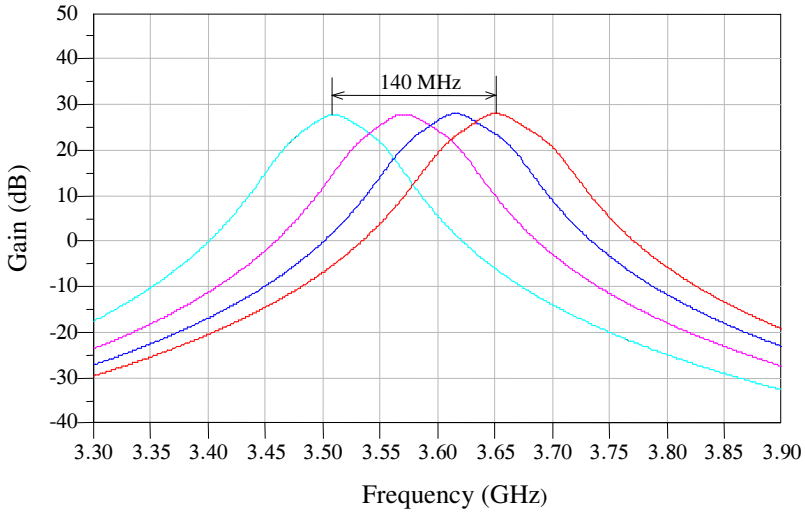

Fig. 3.66 Center frequency tuning ability of the sixth order filter

As shown in Fig. 3.66, the frequency tuning range is from 3.51 GHz to 3.65 GHz.

Input and output matching

The input and output ports in the design are both set at 50 ohm. The simulation result of input matching of the sixth order filter is the same as the input matching of the second order filter (shown in Fig. 3.50). The output matching (reflection coefficients) after each stage is shown in Fig. 3.67. As can be seen from this figure, all the reflection coefficients at the output are less than -40 dB in the frequency range of interest.

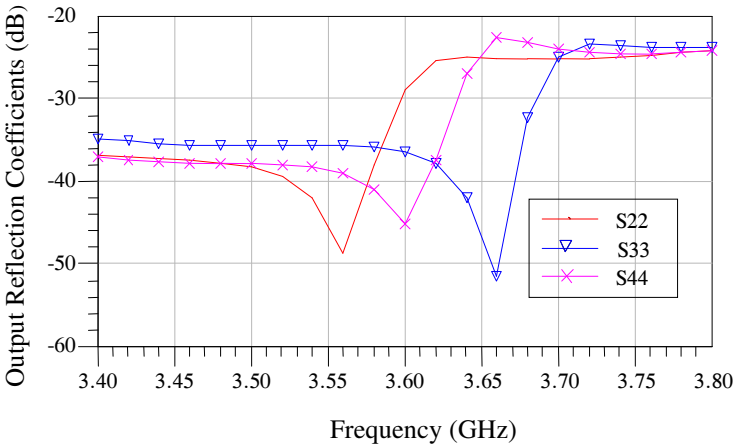

Fig. 3.67 The output matching of three stages in the sixth order filter

Linearity performance

The linearity performance highly depends on the Q value of the filters; high Q is accompanied with the high gain, the large image rejection and the degradation in overall linearity. Fig. 3.68 shows the linearity performance versus the tuning voltage. From Fig. 3.65 and Fig. 3.68, when quality factor tuning voltage is 855 mV, the sixth order filter provides a 100 MHz bandwidth, a 50 dB image rejection, a -44 dBm 1 dB compression point and a -29 dBm IIP3.

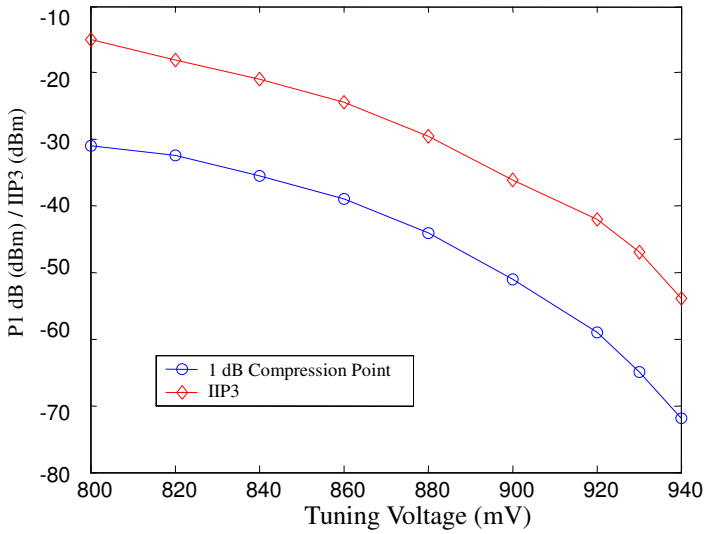

Fig.3.68 1 dB compression gain and IIP3 versus tuning voltage of the sixth order filter

Noise performance

The noise performances after each stage are shown in Fig. 3.69. From the figure, the minimum noise figure of the sixth order filter (third stage) is about 13.9 dB.

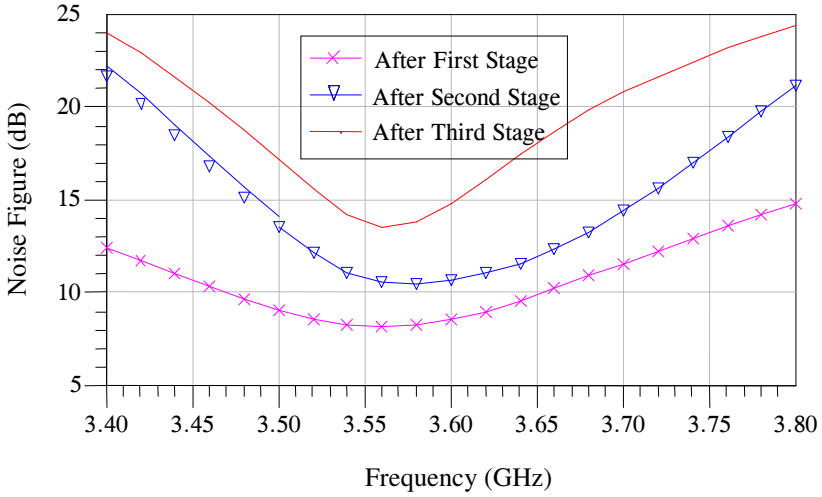

Fig. 3.69 Noise performance of three stages

Dynamic range

By using Eq. 2.12 and Eq. 2.14, the dynamic range can be expressed

as $DR = P_{1dB} - (-174\,\text{dBm/Hz} + \text{NF} + 10\log\text{B} + \text{SNR})$. Using the simulation results, P1dB=-44 dBm, NF=13.9 dB, bandwidth of the filter=100 MHz, and the minimum required SNR=10 dB, the calculated dynamic range is 45.1 dB.

CHAPTER 4 CIRCUIT LAYOUT

A layout is the equivalent of an engineering blueprint of the circuit. In digital design, the layout of the circuit is automatically generated by the software but this is not the case in analog design, the layout has to be manually created. Layout is critical to an analog circuit design, especially for RF circuits in the GHz range. Careful floor plan and layout considerations are important. A poor layout generates unexpected parasitics and leads to performance degradation or circuit failures. This chapter describes the layout techniques of some basic elements used in the design and layout considerations for the filter circuits.

4.1 Layout design flow

After optimizing the schematic to meet the design requirements, each circuit block is implemented to layout using Cadence Virtuoso. There are two guidelines to implement the layout, one is to optimize the layout to reduce parasitics (R, L and C), and the other is to improve device matching (transistors, capacitors, resistors and inductors). When the layout of each block is finished, they need to be arranged together, this is called floor planning. Some guidelines to floor planning are: optimizing area efficiency, isolating noisy devices (resistors) and reducing parasitics. Extraction from the layout finds expected and unexpected parasitics. Post-layout simulation indicates if these parasitics have significant effects to the circuit performance. If so, one may need to redo

the floor plan and even the individual block layout. After successful post layout simulation, the design can be streamed out for fabrication.

4.2 Inductor layout

The guidelines of design for a CMOS inductor were discussed in detail in Section 2.1.3. An actual layout of design example in Section 2.1.3 using Cadence Virtuoso is shown in Fig. 4.1.

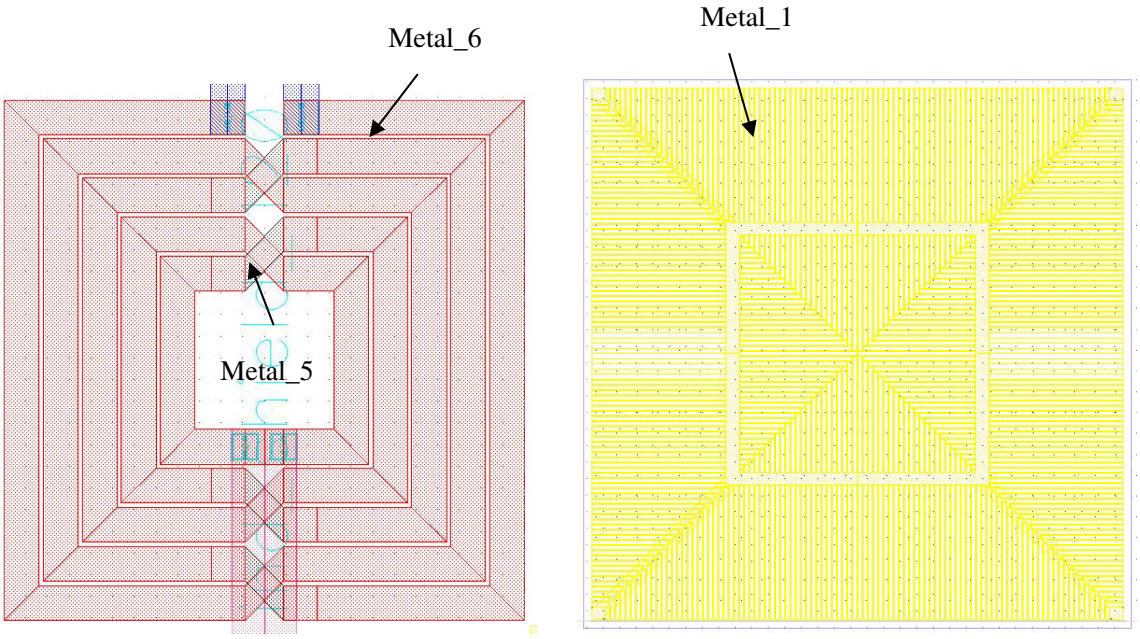

Fig. 4.1 Inductor layout (left) and patterned ground shield (PGS) layout (right)

As stated in Section 2.1.3, the most top layer of metals (metal_6) is used to layout the inductor because this is the thickest metal layer with the smallest sheet resistance. In addition, this layer is located far away from the lossy silicon substrate, which reduces the substrate loss and provides better noise isolation. A wide metal width helps to reduce the series resistance of the metal inductor. However at high frequencies, current only flows through the surface of the metal due to skin effect. The skin depth of a conductor, δ can be calculated as:

$$\delta = \sqrt{\frac{1}{\pi f \mu_0 \sigma}} \tag{4.1}$$

where f is the frequency of the signal, μ_0 is the permeability in free space and σ is the conductivity of the metal. For pure aluminum, the skin depth can be estimated to be around 1.35 μm at 3.6 GHz. An 8 μm metal width is chosen in the design which can be considered a good conductor at 3.6 GHz. At the same time, increasing the metal width increases the silicon area dramatically. With the increasing of inductor size, the parasitic capacitance from inductor to the substrate increases proportionally and thus lowers the self-resonant frequency of the inductor.

By removing some of the inner turns of the inductor, hollow inductors usually have better Q value than the solid ones. The reason for that is the innermost turns of the inductor do not provide much of the inductance while they suffer from series resistance loss due to eddy current in the substrate. The inner radius in the design is set to be 16 μm, compared to the outer radius of 60 μm, which can be considered a hollow inductor. To improve the magnetic coupling between segments of an inductor, the spacing between metal segments is often kept to a minimum size. In this design, the spacing is set to be 1 μm.

As shown in Fig. 4.1 (right) a patterned ground shield (PGS) is used under the inductor to reduce eddy currents in substrate, and at the same time, it reduces the noise generated from the substrate.

4.3 Capacitor layout

Two different capacitors have been utilized in the design, one is the metal-to-metal capacitor and the other is metal-insulator-metal (MIM) capacitor (shown

in Fig. 4.2). MIM capacitor uses an extra metal layer CTM, which is much closer to the next metal layer and thus provides much more capacitance per unit area than the usual metal-to-metal capacitors.

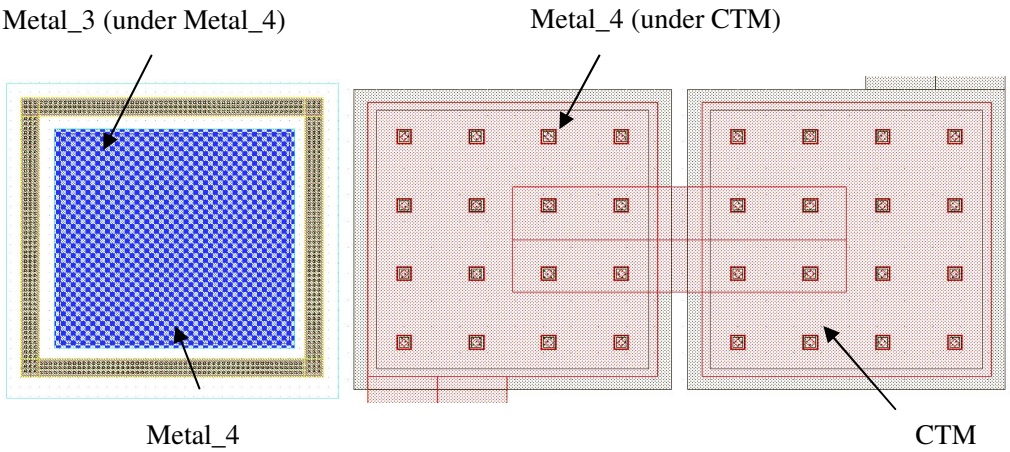

Fig. 4.2 Layout of a metal-to-metal capacitor (left) and a MIM capacitor (right)

4.4 Resistor layout

All the resistors in the design are unsilicide polysilicon resistors. These resistors have relatively large resistances, low temperature coefficient and relatively low parasitic capacitances. Fig. 4.3 shows a layout of the degeneration resistor using polysilicon.

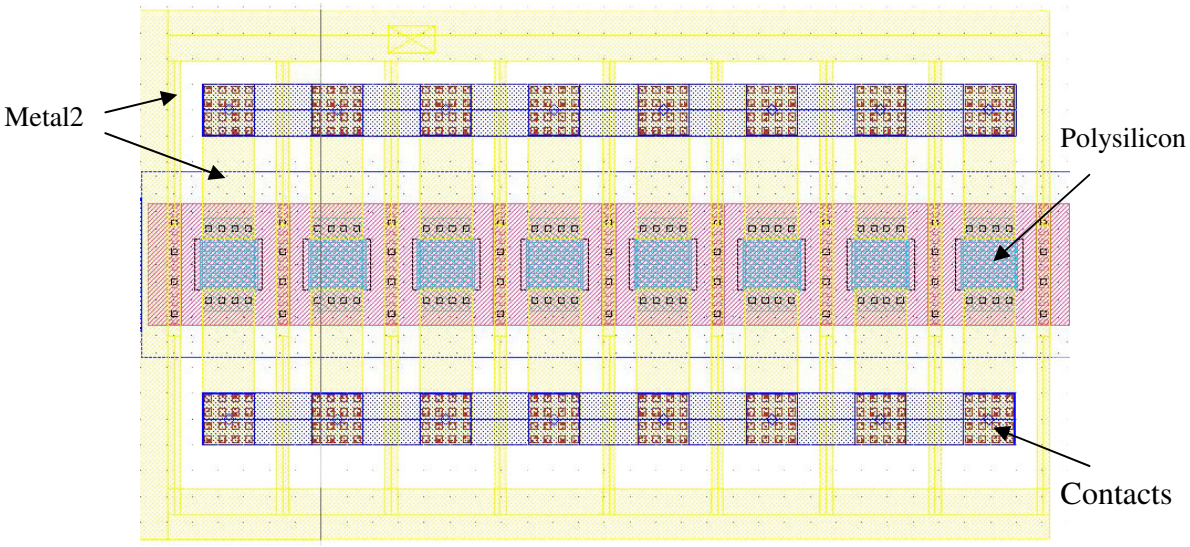

Fig. 4.3 Layout of the polysilicon resistor

4.5 Transistor layout

The layout of a transistor has a great influence on the overall performance of the design including symmetry, noise, parasitic capacitance and gate resistance issues, especially for low noise circuit design. The transistor with a large width is usually divided into a number of small width transistors placed in parallel to reduce parasitic capacitance as well as gate resistance. To isolate the noise, a guard ring with many substrate contacts is also employed.

Symmetry needs to be carefully planned if differential topology is used in the design. Dummy transistors and common-centroid are two common methods used to overcome process variances. Transistors in a half layout of the differential LNA using above techniques are shown in Fig 4.4.

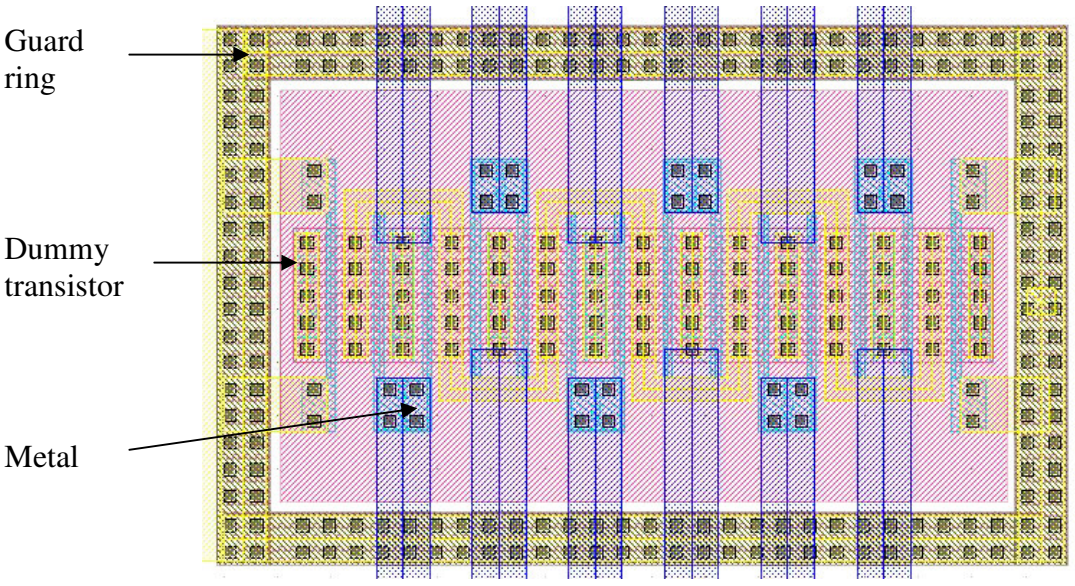

Fig. 4.4 Layout of transistors in the LNA

4.6 Sixth order filter layout

As the filter operates in differential mode, the layout needs to be symmetrical

to keep the passing signal balanced. The floor plan and the layout of the filter are shown in Fig. 4.5 and Fig. 4.6.

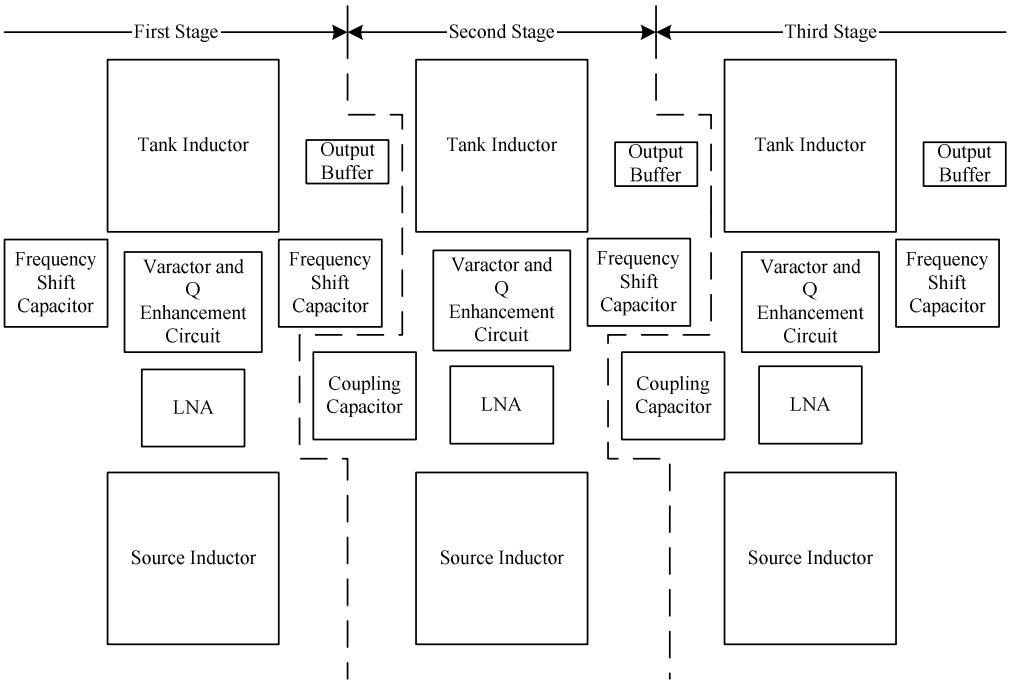

Fig. 4.5 Floor plan of the sixth order filter

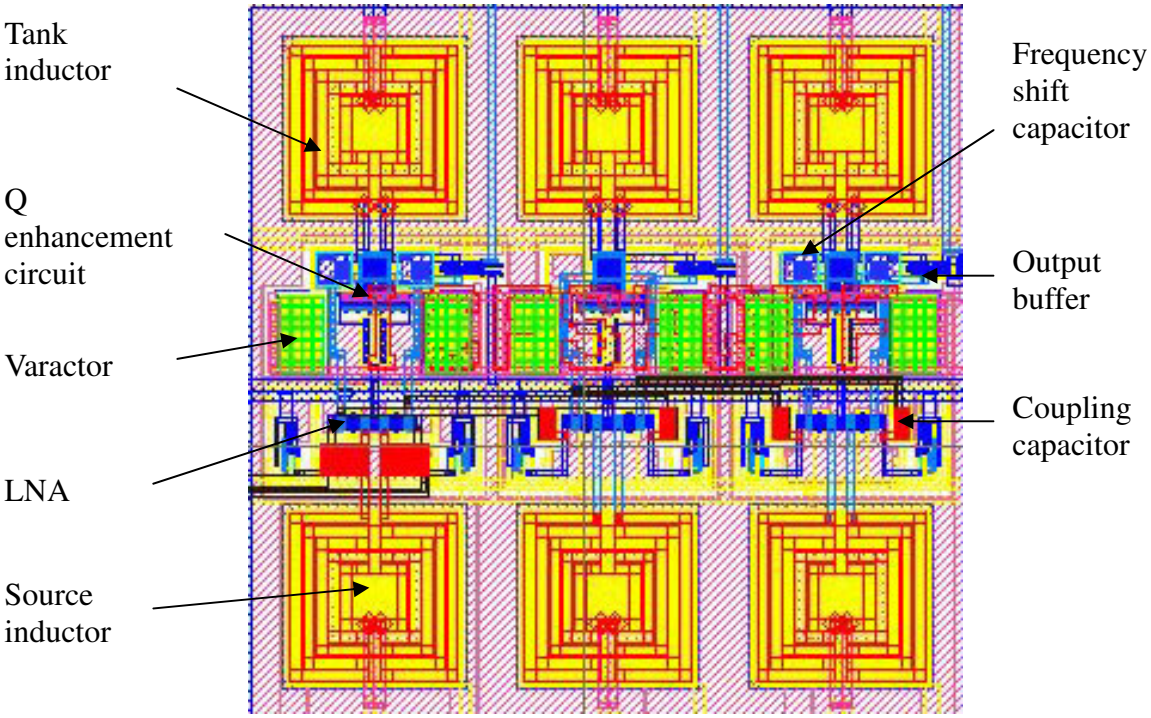

Fig. 4.6 Layout of the sixth order filter

The varactor is designed in Section 2.1.4. The actual layout of one side is shown in Fig. 4.7.

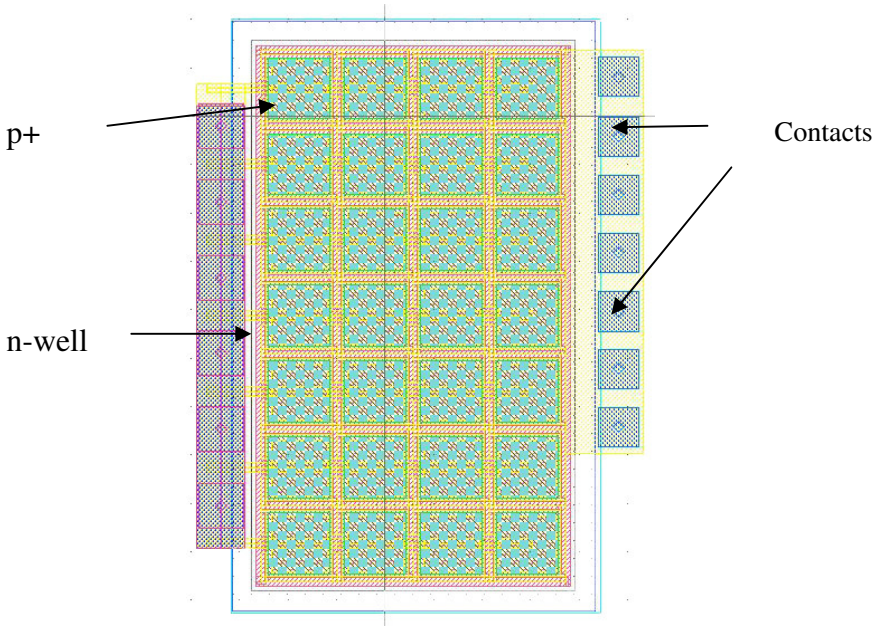

Fig. 4.7 Layout of the varactor array

The layout of the Q-enhancement circuit is shown in Fig. 4.8.

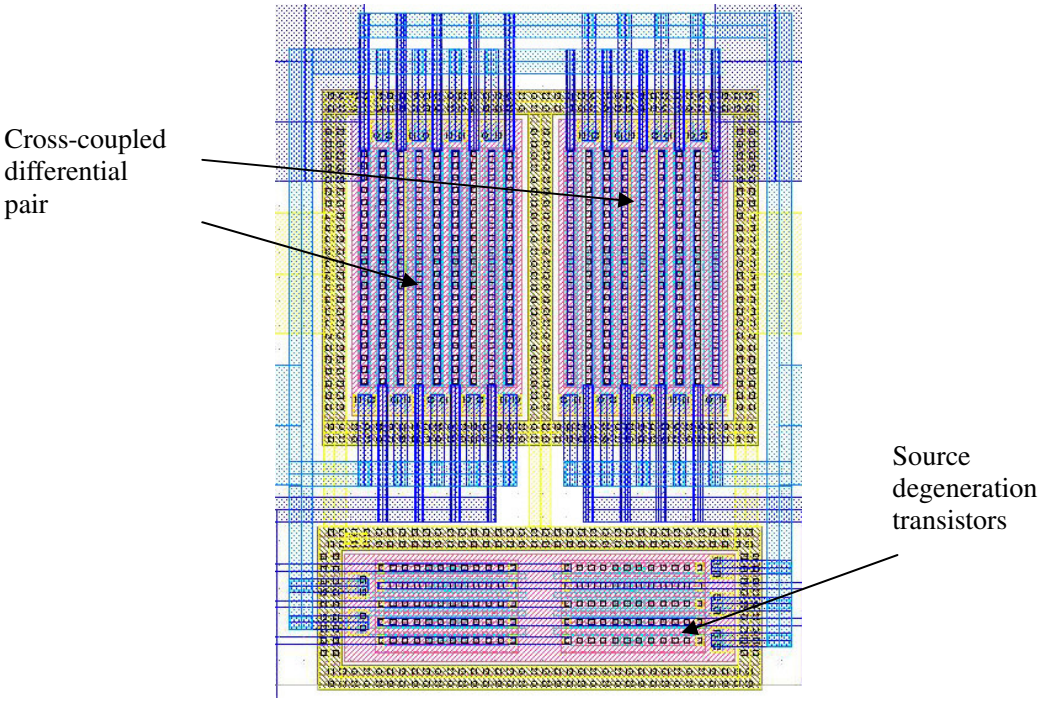

Fig. 4.8 Layout of the Q-enhancement circuit

The layout of the current source of the Q-enhancement circuit is shown in Fig. 4.9.

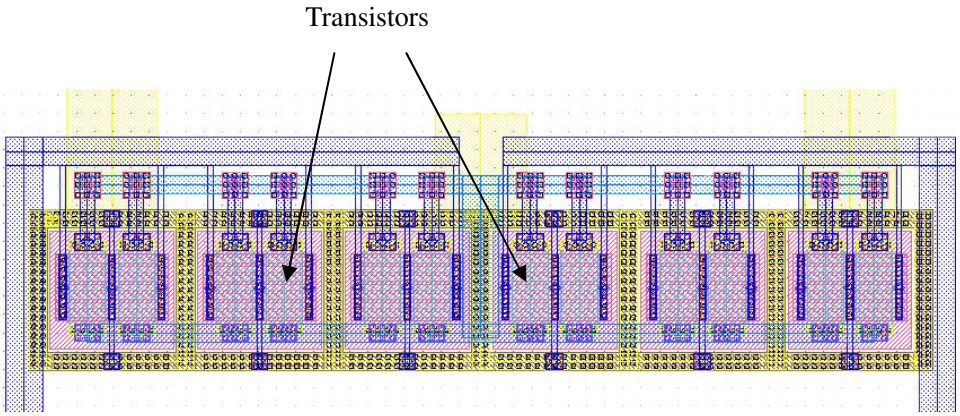

Fig. 4.9 Layout of the current source of the Q-enhancement circuit

The layout of the entire sixth order filter circuit including power ring and bonding pads is shown in Fig. 4.10.

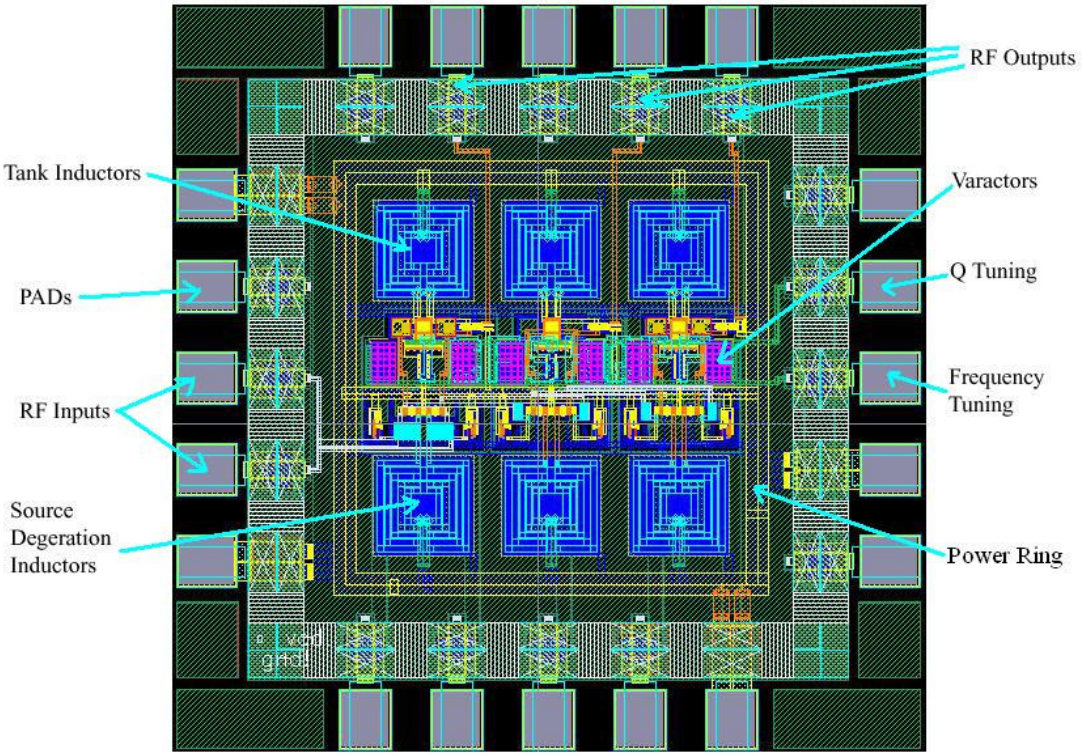

Fig. 4.10 Final layout of the sixth order filter

CHAPTER 5 MEASUREMENT RESULTS

The proposed sixth order filter was fabricated using standard 0.18 μm CMOS technology. A micrograph of the fabricated chip is shown in Fig. 5.1.

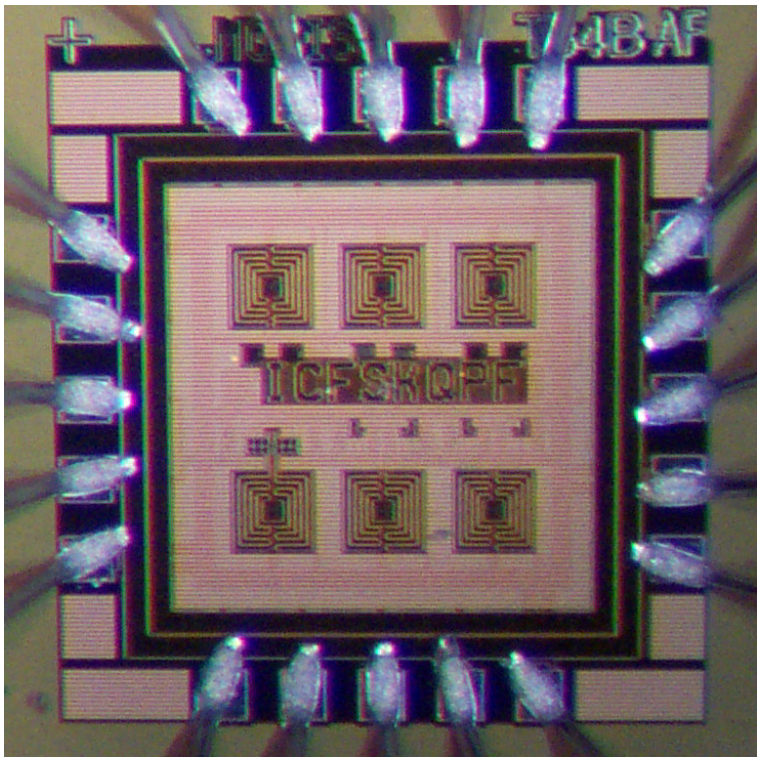

Fig. 5.1 Micrograph of the fabricated chip

In this chapter, testing setup and measurement results of the sixth order bandpass filter will be presented. Testings include the following:

1) Input matching,

2) Frequency response and filter gain,

3) Image rejection,

4) Q tuning ability,

5) Frequency tuning ability,

6) Input 1 dB compression point,

7) Input third-order intermodulation intercept point (IIP3),

8) Noise figure,

9) Power consumption.

5.1 Center frequency, gain and image rejection

In order to carry out the measurement, a testing board was made as shown in Fig. 5.2. The balun on the testing board acts as a 2-way 180^0 power splitter to split the single sided signal (RF_in) from the network analyzer to a pair of differential signals (RF_in+ and RF_in-). The testing board includes the following ports: RF input (RF_in), first stage RF output (RF_out_1), second stage RF output (RF_out_2), third stage RF output (RF_out_3), power supply terminal (power), frequency tuning terminal (Freq_tuning), and quality factor tuning terminal (Q_tuning). The measurement setup shown in Fig. 5.3 was used to evaluate the circuit parameters including center frequency, maximum gain, Q tuning and frequency tuning abilities and image rejection. In the setup, a HP 8722 vector analyzer was used to test the S parameters of the circuit. The power board provided power supply, Q tuning and frequency tuning voltages. The tuning voltages are generated by adjusting the variable resistors on the power board. To prevent the filter gain from being compressed, the test signal power of the network analyzer was set at -50 dBm.

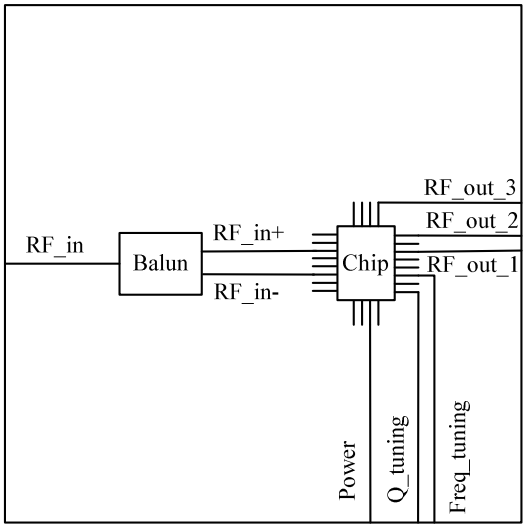

Fig. 5.2 Layout of the testing board

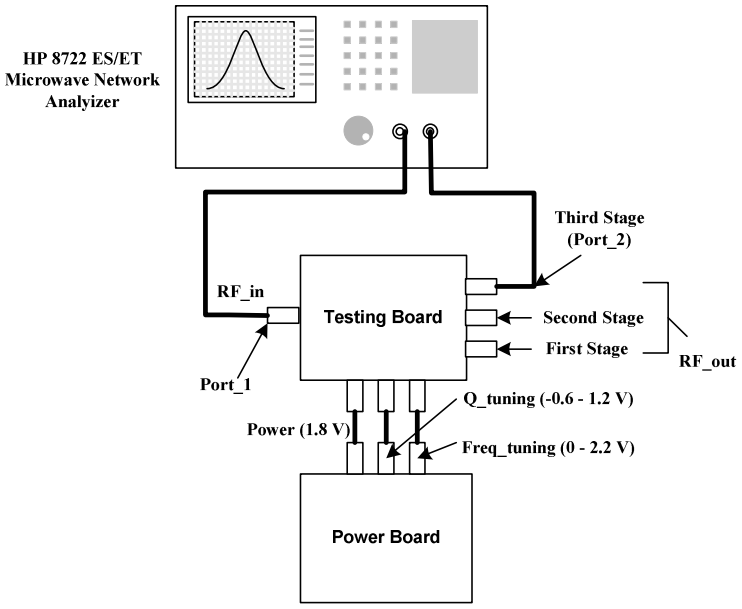

Fig. 5.3 Frequency response measurement setup

The filter under test can be seen as a two port network, the parameter S21 is the gain of the filter. By setting the network analyzer center frequency to 3.6 GHz and the bandwidth to 600 MHz, the tested result of S21 is plotted in Fig. 5.4.

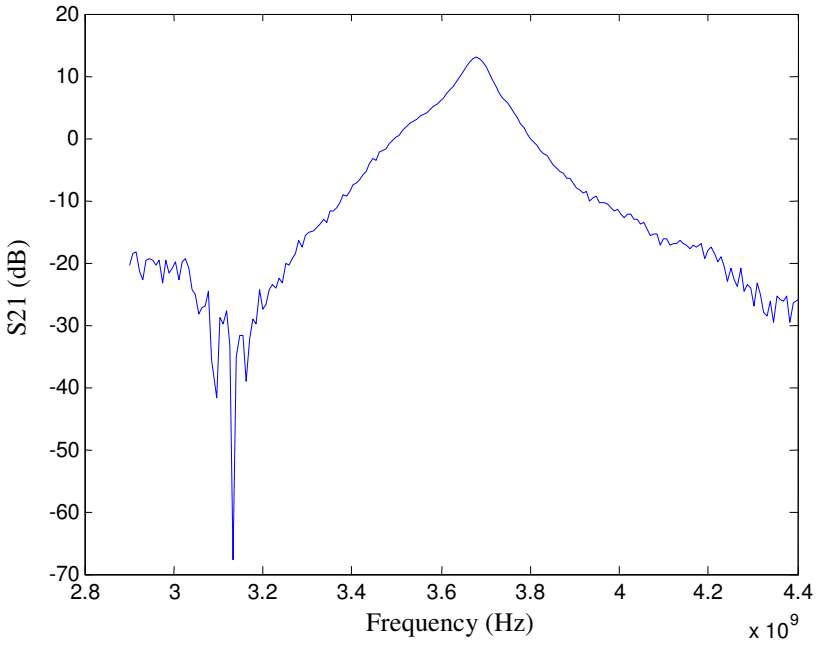

Fig. 5.4 Measurement of frequency response of the sixth order filter

As shown in Fig. 5.4, the center frequency of the filter is at 3.67 GHz, the bandwidth is 72 MHz, and the gain of the filter is 13 dB. With an intermediate frequency (IF) of 250 MHz, the image signal attenuation at 500 MHz away from the desired frequency is 50 dB.

The frequency responses under different Q tuning voltages to determine tuning bandwidth are plotted in Fig. 5.5. As seen from the figure, if the insertion gain great than 0 dB is required; the bandwidth of the filter can be tuned from 35 MHz to 95 MHz. The tuning bandwidth is less than the simulated value of 48 MHz to 125 MHz; this may be caused by the losses introduced by the off-chip balun (the power splitter) and the unexpected resistance parasitics from the PCB trace, the on-chip gate resistance and the interconnections. These losses lower the gain of the filter and reduce the available bandwidth.

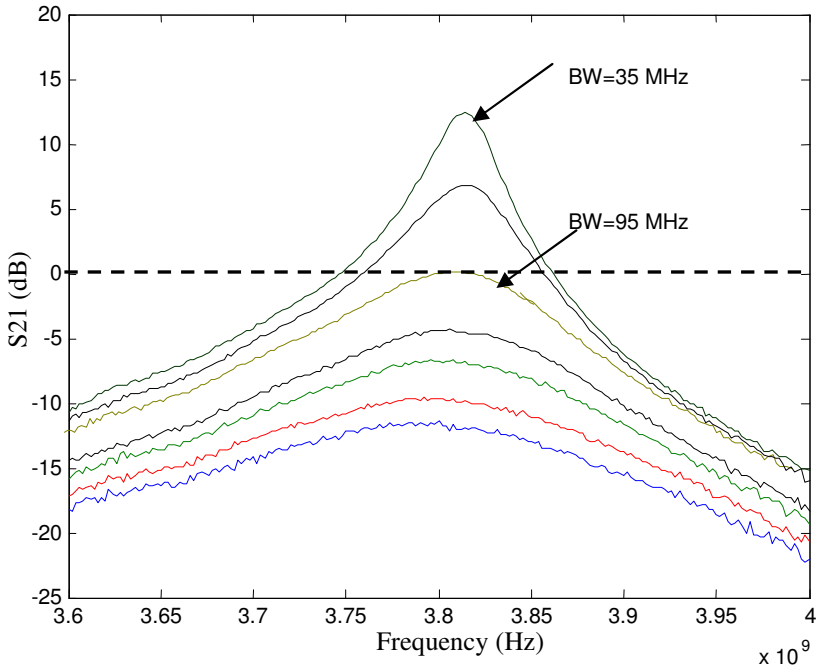

Fig. 5.5 Measurement of bandwidth tuning ability of the sixth order filter

To determine frequency tuning range, the frequency tuning voltage was varied from -0.6 V to 1.2 V. The frequency responses are shown in Fig. 5.6. As shown in this figure, the frequency tuning range is from 3.54 GHz to 3.88 GHz. The frequency tuning range is about 340 MHz which is much larger than the simulated value of 140 MHz. The reason for this may be the inaccuracy of the varactor model and the over estimation of the fixed parasitic capacitance of the varactors. As discussed in Chapter 2, the tuning of center frequency inevitably changes the Q of the filter. A frequency tuning combined with the Q tuning to achieve the same bandwidth at different center frequencies is shown in Fig. 5.7. The combinations of the frequency tuning voltages and Q tuning voltages to achieve the same bandwidth are shown in Fig. 5.8.

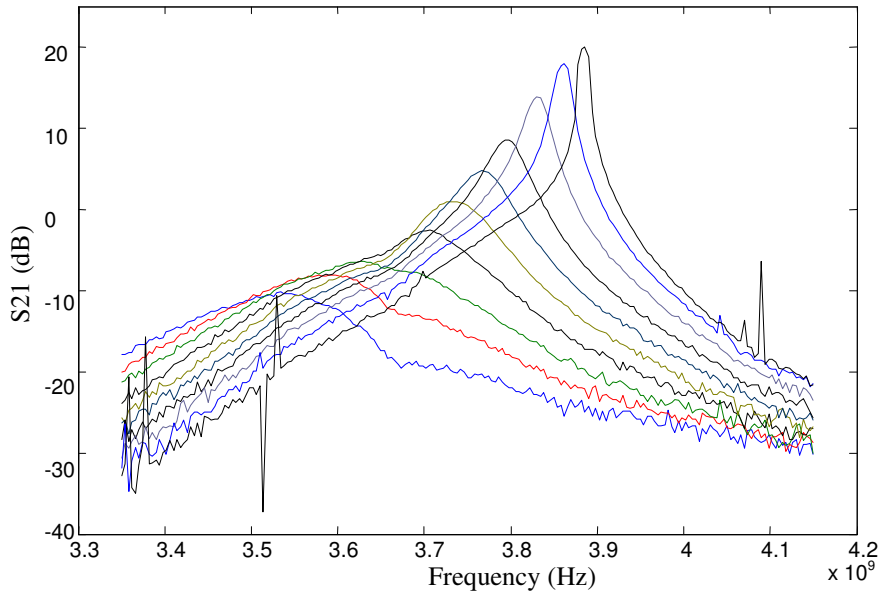

Fig. 5.6 Measurement of center frequency tuning ability of the sixth order filter

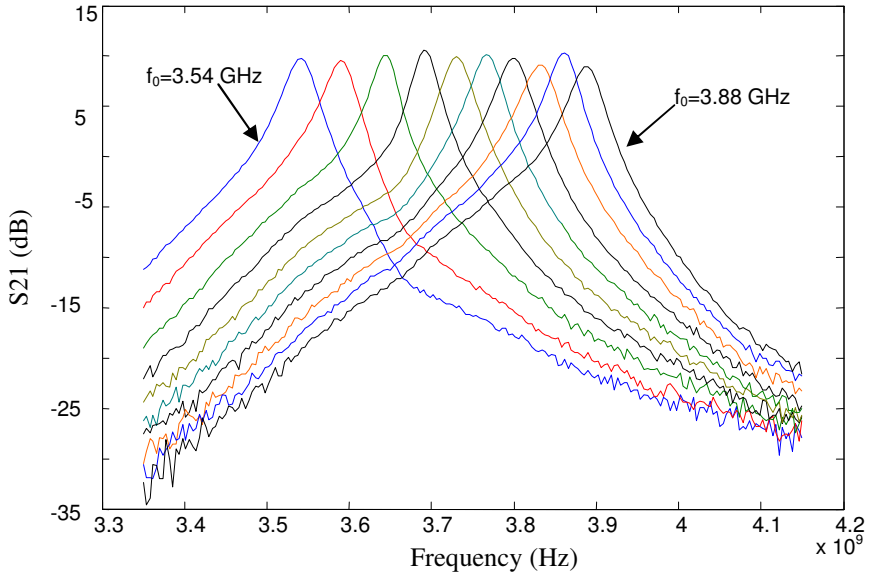

Fig. 5.7 Measurements of the center frequency tuning combined with bandwidth tuning

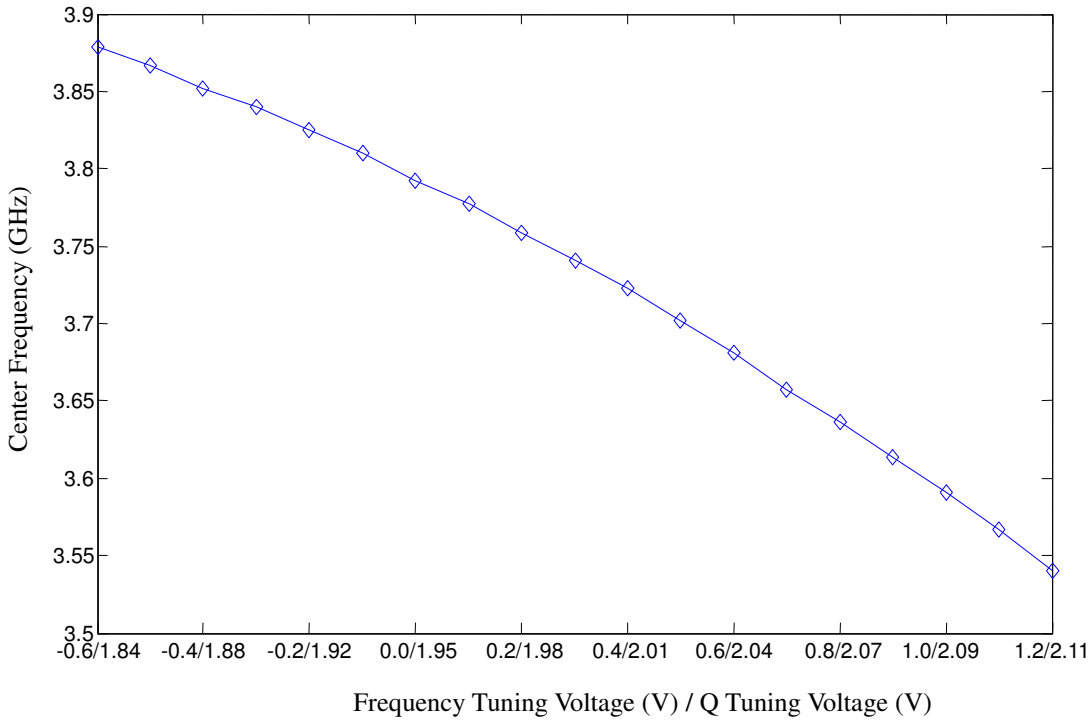

Fig. 5.8 Combination of bandwidth tuning and frequency tuning

5.2 Input matching

In order to measure the input matching, the balun on the testing board is bypassed and the differential input ports are connected to the terminals. Since there is no differential calibration kit available, only single-ended input matching is measured. The source impedance of the network analyzer is 50 ohm; the ideal value of the single-end of the differential input is actually 25 ohm. Another 25 ohm resistor was added to the input. The other input port was terminated with a 25 ohm terminal and the output ports were all terminated by 50 ohm resistors. Fig. 5.9 shows the measurement setup.

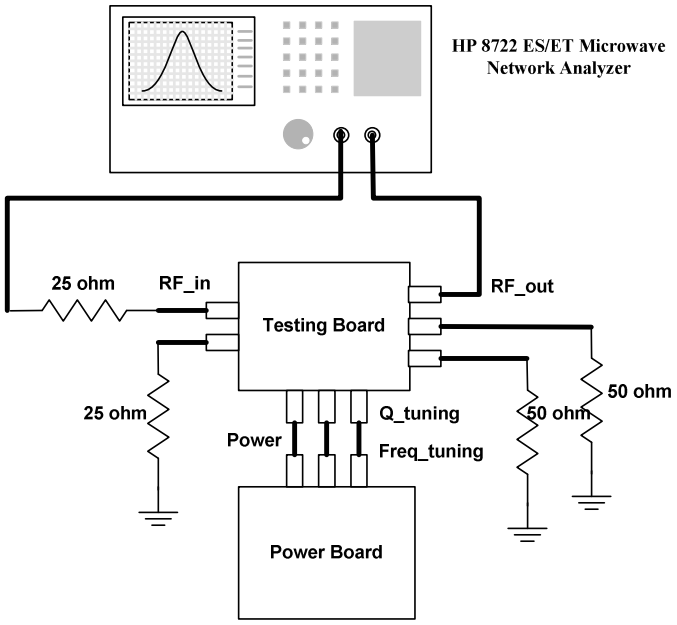

Fig. 5.9 Input matching measurement setup

The measured input reflection coefficient S11 is shown in Fig. 5.10. The S11 minimum is about -34 dB and appears at 3.818 GHz. The measured input match is not as good as the simulated result. The matched frequency range shifted from 3.6 GHz to 3.82 GHz. This may be caused by the off-chip parasitics on the testing board.

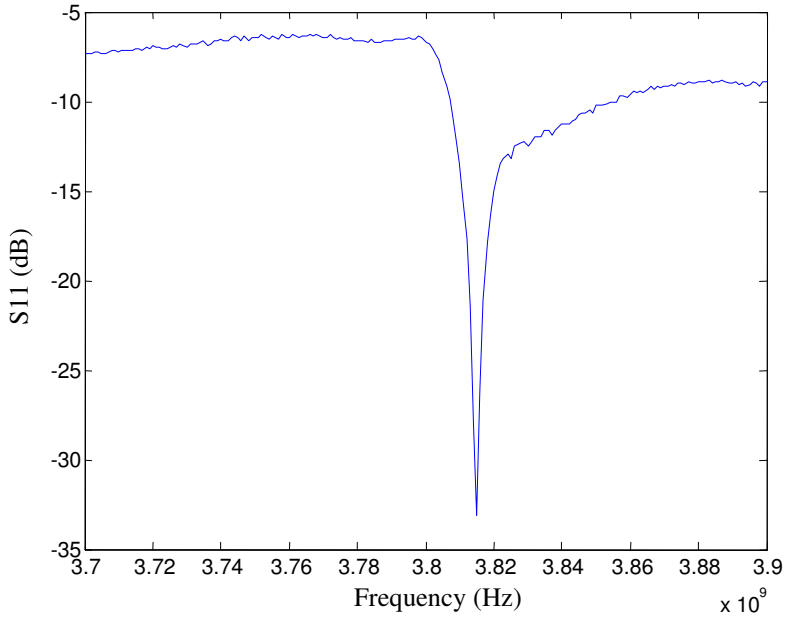

Fig. 5.10 Measurement of the input matching

5.3 Linearity measurement

1 dB compression gain measurement is realized by increasing the input signal power and measuring the output power of the filter. Testing was carried out by setting the center frequency at 3.67 GHz and a bandwidth of 65 MHz. A 3.67 GHz RF signal with sweeping power was fed into the circuit. The output was displayed in the spectrum analyzer. This measurement setup is shown in Fig. 5.11.

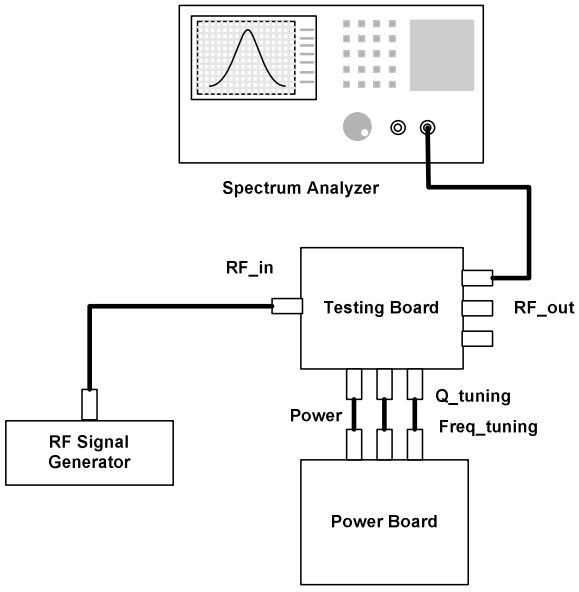

Fig. 5.11 Linearity measurement setup

The output power versus input power of the filter is shown in Fig. 5.12. As shown in the figure, the output of the filter deviates from the straight line with the increasing of the input power. The input 1 dB compression point is -46 dBm and the output 1 dB compression point is about -33.5 dBm.

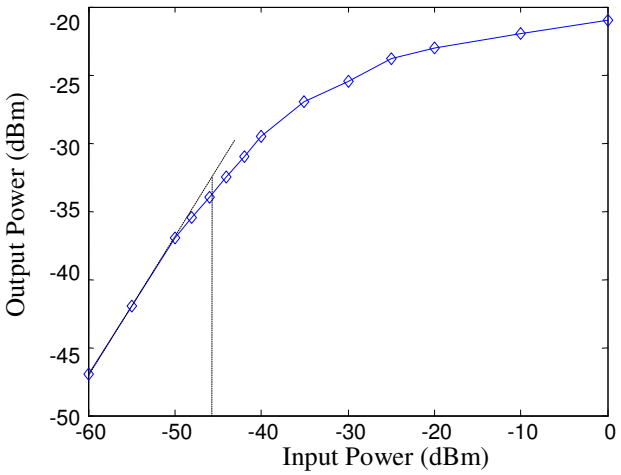

Fig. 5.12 Measurement of 1 dB compression point of the sixth order filter

The IIP3 is measured by a two-tone test and its basic principle is already discussed in Chapter 2. Fig. 5.13 shows the test setup. Two closely spaced signals (3.77 GHz+5 MHz and 3.77 GHz-5 MHz) with equal power were first combined by a 2-way 0^0 power combiner before being split by the on board balun (2-way 180^0 power splitter). Then, the signals were fed into the circuit, the output response at the fundamental frequencies and third-order intermodulation frequencies were measured from the spectrum analyzer. Fig. 5.14 shows the fundamental and third-order products of the filter captured by the spectrum analyzer.

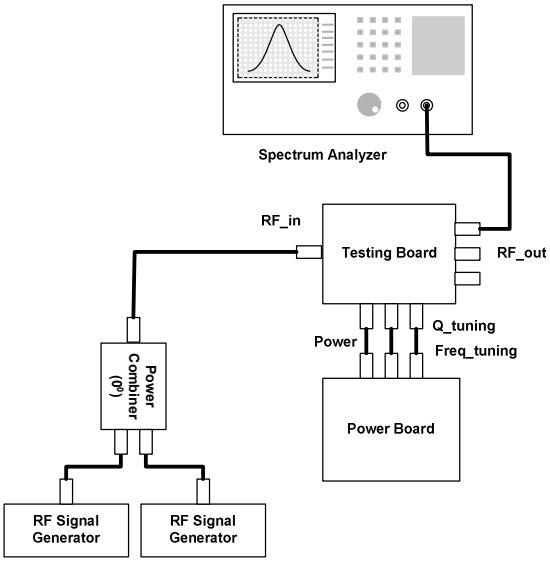

Fig. 5.13 Two tone test measurement setup

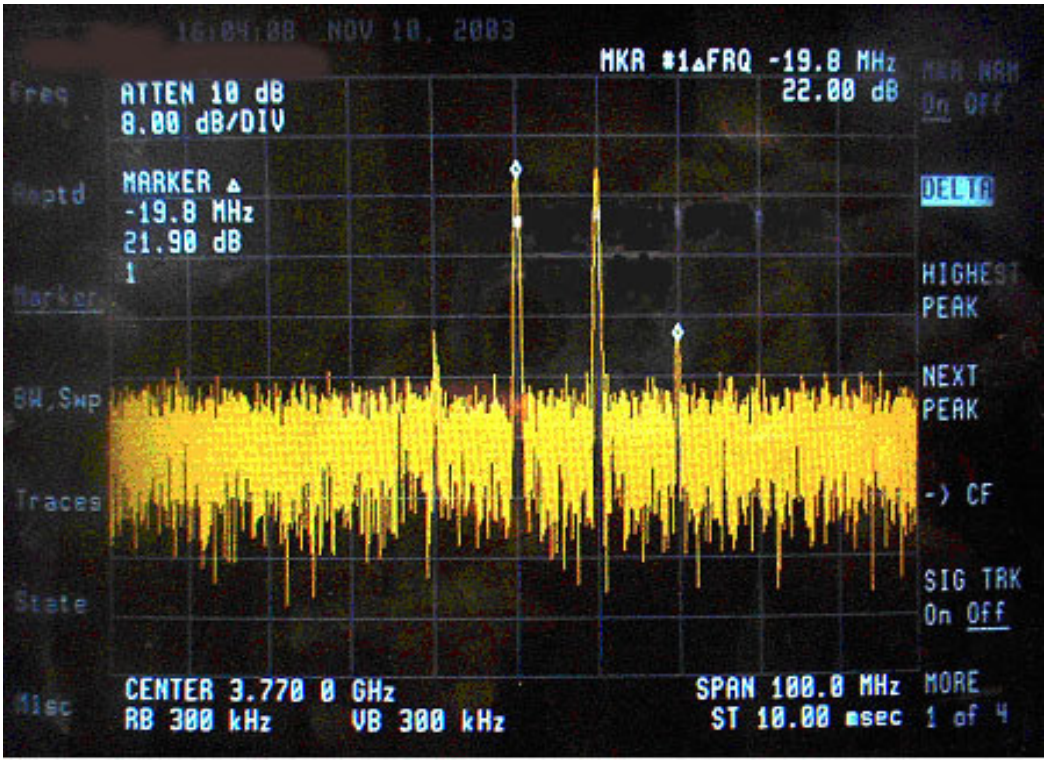

Fig. 5.14 Two tone test results

The plot of the relationship between the input and output powers are depicted in Fig. 5.15. The measured IIP3 is about -29 dBm.

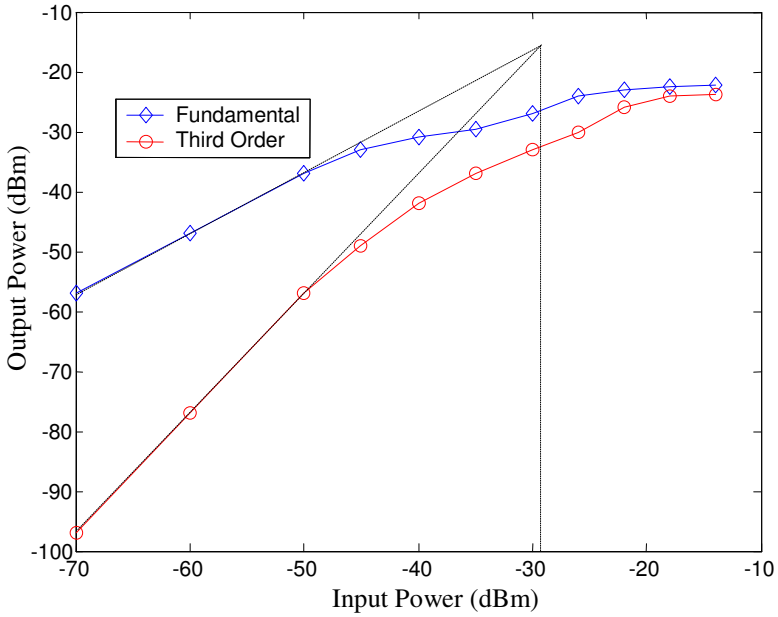

Fig. 5.15 Measurement of fundamental and third order products of the sixth order filter

5.4 Noise figure and dynamic range

Because of the lack of the noise source at the desired frequency range, the noise figure measurement could not be performed. Since the input dynamic range depends on the noise figure of the system, this could not be measured either. However, as seen from the spectrum analyzer in Fig. 5.14, the noise floor is about -90 dBm. The output dynamic range can be calculated by using DR_{out} = P1dB (output) – Nf (output) – SNR. The output 1 dB compression point is -33.5 dBm, if the minimum SNR required is 10 dB, the calculated output DR is around 46.5 dB.

5.5 Power consumption

The measured DC current of the filter is 72 mA, for a 1.8 V voltage supply, the DC power consumption of the filter is about 130 mW.

5.6 Summary

To sum up, the measured and the simulated results of the sixth order filter are shown in Table 5.1. As seen from this table, most simulated and tested parameters of the sixth order filter are very well matched. However, there are two main differences from the simulation and measurement results. The measured center frequency is shifted 3.5% higher and the tuning range is about 2.4 times of the simulated result. The center frequency shifting may be caused by the inaccuracy of the varactor and inductor models. The wider tuning range could come from the over estimation of the fixed parasitic capacitance of the varactors during simulation. The other difference is the gain of the filter; this also affects the usable bandwidth of the filter. The measured gain is 12 dB lower than the simulated result and the maximum usable bandwidth is 45 MHz less. The lower of the gain may be caused by the off-chip balun (power splitter) and some unexpected on-chip parasitic resistances. Since the maximum usable bandwidth is defined by the 0 dB gain of the filter, the lower of the gain inevitably shrinks the bandwidth. As seen from Table 5.1, most filter requirements are met by the measurement results. The measured maximum usable bandwidth is about 80 MHz, which is close to the requirement of 100 MHz bandwidth. The measured 1 dB compression point is -46 dBm, which meets the required value of -45 dBm.

Table 5.1
The measured and simulated results of the sixth order filter

Parameters	Specifications	Simulation	Measurement
Voltage Supply	1.8 V	1.8 V	1.8 V
Center frequency	3.6 GHz	3.6 GHz	3.67 GHz
Gain	-	0-30 dB	0-18 dB
Frequency tuning range	-	3.51 GHz-3.65 GHz	3.54 GHz-3.88 GHz
Bandwidth (Q tuning)	100 MHz	48 MHz-125 MHz	35 MHz-80 MHz
IIP3	> -30 dBm	-29.5 dBm	-29 dBm
P1dB	> -45dBm	-44 dBm	-46 dBm
Dynamic range	> 45 dB	45.1 dB	46.5 dB
Image rejection (500 MHz away)	>50 dB	50 dB	50 dB
Noise figure	15 dB	14.9 dB	-
Power consumption	-	65 mA	72 mA

CHAPTER 6 CONCLUSIONS

A 3.6 GHz bandpass filter designed using the 0.18 μm CMOS technology was presented. This filter is suitable for variety implementations of the wideband RF transceivers. The design employed state-of-the-art inductive degeneration techniques to minimize the noise of the input stage. A Q-enhancement circuit was designed to overcome the lossy inductors on the CMOS epi substrate. A center frequency tuning circuit was also included to compensate frequency deviation due to process variations and the inaccuracy of the models. The causes of the poor circuit linearity were investigated and a couple of linearization techniques were employed to improve the device linearity.

In the first prototype, a second order bandpass filter is designed and simulated. With a 1.8 V supply, the design achieves a voltage gain of 30 dB with a 15 MHz bandwidth for a Q of 240. The reflection coefficient S11 is -55 dB, the input 1 dB compression point and input third-order intermodulation product (IIP3) are -20 dBm and -16 dBm respectively. The noise figure of the filter is around 10 dB. The filter has a 150 MHz (3.54 GHz to 3.69 GHz) tuning range.

In order to enhance the image rejection ability of the filter, a three-stage, sixth order bandpass filter was designed and fabricated. The design cascades three stages of the second order filters to achieve wider bandwidth and higher image rejection.

Simulation results show that an image rejection as high as 59 dB can be achieved and the bandwidth can be extended to 125 MHz.

By research into the relationship between tuning voltage and the center frequency, an innovation method is employed to set apart the center frequency of each stage in the 3-stage cascading filter. With the need of only one tuning terminal, this method greatly simplifies the center frequency tuning scheme and makes the filter response much more predictable and reliable. Gain distribution affects the linearity and noise performance of the overall filter. The research provides an optimized configuration of each stage gain. The research on the relationship between the tuning voltage, and the gain and the quality factor innovates a new tuning scheme. This bandwidth tuning scheme needs only one tuning terminal and greatly simplifies the tuning method thus makes the filter more applicable to commercial applications.

The design was fabricated using 0.18 μm CMOS technology, and the area of the circuit including 25 bonding pads is 0.9mm×0.9mm. The total current consumption including the bias circuits and the output buffers is 72 mA using 1.8 V supply. In the testing, for the three stage design, the voltage gain is 13 dB at a bandwidth of 75 MHz. The bandwidth is tunable from 35 MHz to 80 MHz by tuning the Q of each stage. The center frequency is tunable from 3.54 GHz to 3.88 GHz. In addition, the input third order intermodulation product (IIP3) and the input-referred 1 dB compression point are -29 dBm and -46 dBm respectively (when the bandwidth is tuned to 75 MHz). Frequency deviation and inaccuracy of the tuning range in the fabricated chip are mainly due to the imprecise modeling of the inductors and varactors. The parasitic capacitance and inductance also affect center frequency of the filter. The shrink in the filter gain is

mainly caused by the off-chip balun in the testing and the parasitic resistance has not been extracted in the simulation. In summary, this RF filter meets most of the preset requirements.

Table 6.1
A comparison of this design to previously reported works

Parameters	[11]	[43]	[44]	[45]	This work
Year	1998	2001	2002	2003	2003
Filter order	4	4	6	4	6
Center frequency (GHz)	0.85	1.9	2.1	1.8	3.54-3.88
Passband Gain (dB)	0	0	0	9	0-18
Ripple in passband (dB)	< 2	1.6	0.7	< 0.5	< 1
Bandwidth (MHz)	18	150	60	80	35-80
Q of inductor	< 3	N/A	N/A	2.7	4.9
Dynamic range (dB)	61	63	63	42	46.5
Current drain/pole (mA)	19.25	4.5	1.17	4	24
Supply voltage (V)	2.7	2.7	2.5	2.7	1.8
Technology	0.8 μ m	0.25 μ m	0.25 μ m	0.5 μ m	0.18 μ m

A comparison of this design to previously reported work of on-chip high order bandpass filters is given in Table 6.1. As seen from the table, the filter designed in this research work using the most advanced CMOS technology and the on-chip inductor has the highest Q. Most importantly is that the designed filter works at a higher frequency range which makes this filter more applicable for wideband wireless applications. A drawback of this filter is its power consumption much higher than the others. Works in [11], [43], [44] and [45] are not using Q-enhancement circuit and there is no LNA involved, thus the power consumption of these filters can be controlled at a very low level. However, without a LNA in the design, high gain cannot be achieved; the LNA is

required in the system in order to amplify the weak incoming signal.

With small modification, the filter can be used in a wide range of wideband wireless applications. However, there are still problems that need to be solved. For a low power design, the power dissipation needs to be further reduced; this can be achieved by removing the linearization resistor and improving the quality factor of the inductor. High order passive filters have lower power dispassion but they are usually not tunable and can not provide voltage gain. The research on tunable high order passive filter architecture is a promising direction. In order to fit in the future ultra wideband and multi channel applications, a digital tuning method is needed to switch the filter passband to different frequency ranges. Switch capacitors may be used for digital tuning and extending the bandwidth.

The varactor model is extremely important in the design; the model assists to determine the accuracy of the center frequency and the available tuning range. There is much research work that needs to be done in device physics to achieve better varactor model. With the rapid development of CMOS technology, there are more and more research opportunities available in CMOS RF filter design. The new 90 nm CMOS technology provides a f_T over 100 GHz and uses copper instead of aluminum in metal layers. With these new features, RF filters working at a center frequency over 20 GHz are expected in the near future.

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