Study of Layout Techniques in Dynamic Logic Circuitry for Single Event Effect Mitigation

A Thesis Submitted to the College of
Graduate Studies and Research
In Partial Fulfillment of the Requirements
For the Degree of Master of Science
In the Department of Electrical and Computer Engineering
University of Saskatchewan
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ABSTRACT

Dynamic logic circuits are highly suitable for high-speed applications, considering the fact that they have a smaller area and faster transition. However, their application in space or other radiation-rich environments has been significantly inhibited by their susceptibility to radiation effects. This work begins with the basic operations of dynamic logic circuits, elaborates upon the physics underlying their radiation vulnerability, and evaluates three techniques that harden dynamic logic from the layout: drain extension, pulse quenching, and a proposed method. The drain extension method adds an extra drain to the sensitive node in order to improve charge sharing, the pulse quenching scheme utilizes charge sharing by duplicating a component that offsets the transient pulse, and the proposed technique takes advantage of both. Domino buffers designed using these three techniques, along with a conventional design as reference, were modeled and simulated using a 3D TCAD tool. Simulation results confirm a significant reduction of soft error rate in the proposed technique and suggest a greater reduction with angled incidence. A 130 nm chip containing designed buffer and register chains was fabricated and tested with heavy ion irradiation. According to the experiment results, the proposed design achieved 30% soft error rate reduction, with 19%, 20%, and 10% overhead in speed, power, and area, respectively.

ACKNOWLEDGEMENTS

This thesis would not have been possible without the support of many. First, I would like to express my heartfelt gratitude to my supervisor Dr. Li Chen for his continuous support and valuable mentorship over the years. I am also grateful for the great opportunities he provided me to explore the ASIC world and gain valuable experience.

A sincere thank you goes to my colleagues, Haibin Wang and Rui Liu, for their wonderful work during the chip design and testing, and all the fun we had in the research.

I am also appreciative of the financial and technical support from CMC Microsystems during the chip design and fabrication.

I would also like to thank all my fellow labmates in the U of S VLSI group: Hao Xie, Qiong Wu, Zhichao Zhang, Yi Ren, Li Fan, Lixiang Li, and Govindakrishnan Radhakrishnan for the great time we spent together.

Special thank you to Kuande Wang and Nihaar Mahatme for their helpful advices in my research projects.

I would like to express my gratitude to Qingqing, Kevin, and all my friends as well for being so caring and supportive towards me.

Last but not least, I am forever indebted to my parents and my girlfriend Jen for their love, encouragement and support throughout my studies.

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LIST OF ABBREVIATIONS

3D	Three-Dimension
a.u.	Arbitrary Unit
BJT	Bipolar Junction Transistor
BPSG	BoroPhosphoSilicate Glass
CMOS	Complementary Metal-Oxide Semiconductor
DCB	Dual Clock Buffer
DCM	Digital Clock Manager
decap	Decoupling Capacitor
DHC	Double Height Cell
DICE	Dual-Interlocked storage CEll
DIMM	Dual In-line Memory Module
DRAM	Dynamic Random-Access Memory
DRC	Design Rule Checking
DUT	Device Under Testing
EDA	Electric Design Automation
EDAC	Error Detection And Correction
ESD	ElectroStatic Discharge
FPGA	Field Programmable Gate Array
GCR	Galactic Cosmic Ray
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
JEDEC	Joint Electron Device Engineering Council
LDD	Lightly Doped Drain
LEAP	Layout design through Error-Aware transistor Positioning
LET	Linear Energy Transfer
LVS	Layout Versus Schematic
MBU	Multiple-Bit Upset
PC	Personal Computer
PCB	Printed Circuit Board

PDK	Process Design Kit
PDN	Pull-Down Network
OCQFN	Open Cavity Plastic Quad Flat No-lead
RHBD	Radiation Hardening By Design
SEB	Single-Event Burnout
SEE	Single-Event Effect
SEFI	Single-Event Functional Interrupt
SEGR	Single-Event Gate Rupture
SEILA	Soft-Error Immune LAtch
SEL	Single Event Latch-up
SER	Soft Error Rate
SET	Single-Event Transient
SEU	Single-Event Upset
SI	Signal Integrity
SOI	Silicon-On-Inductor
SPE	Solar Particle Event
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random-Access Memory
STA	Static Timing Analysis
STI	Shallow Trench Isolation
TAMU	Texas A&M University
TCAD	Technology Computer Aided Design
TMR	Triple Modular Redundancy
VLSI	Very-Large-Scale Integration

CHAPTER 1 INTRODUCTION

The preponderance of information in this day and age is ciphered by electronic circuits in the form of charge or current flow. With the development of modern complementary metal-oxide semiconductor (CMOS) technology, the feature size has been scaling down and has currently reached 14 nm and below. In April 2012, Intel Core i7 and i5 processors based on its 22 nm technology hit the market worldwide. While the transistor dimension shrunk, the supply voltage needed to scale down to around 1.0 V in order to prevent material wear or breakdown due to high electric fields. As a result, node charge decreased at a rate that was at least linear with the channel width. In 1962, Wallmark and Marcus already discerned that a single cosmic ray particle strike would start upsetting microelectronic devices if the channel length scales below 1 μm [1]. Ever since this was made aware, the effect of radiation on microelectronics has gained a tremendous amount of attention and increasingly more researchers began studying the underlying mechanisms. In 1978, May and Woods from Intel Corporation reported that these upsets were triggered by alpha particles emitted during the radioactive decay of thorium and uranium from radioactive impurities in the device materials. The term “soft error” was first used in their paper to denote “random, nonrecurring, single-bit errors in memory devices” [2]. Guenzer and Wolicki [3] later discovered that the particles that triggered soft errors came not only from thorium and uranium, but also from highly energetic neutrons, protons and heavy ions originating from cosmic rays in the natural environment. Moreover, they introduced the term “single event upset” to refer to a soft error that occurs in dynamic random-access memories (DRAMs). In 1995, Baumann et al. [4] discovered that boron fission induced by thermal neutrons in the borophosphosilicate glass (BPSG) layer acts as another source of radiation-induced errors in high density DRAMs.

1.1 Radiation Sources

1.1.1 Alpha Particles

An alpha particle is comprised of two protons and two neutrons bound together, which is identical to a helium nucleus. It is generally created during the process of alpha decay. In the 1970's, alpha particles emitted from radioactive impurities in package resin were found to be the major source of terrestrial soft errors. An alpha particle loses energy when it travels through materials by means of interacting with the electrons of that material. The distance it travels before being stopped by material is a function of both its energy and material density. The range of an alpha particle is fairly short: a few tens of micron in packaging materials and even less in metals and oxides. Therefore, the semiconductor industry has focused on purifying the packaging materials near the die surface in order to eliminate the major source of contamination. As a result, the alpha particle emissivity on integrated circuits (ICs) and packaging materials has decreased from 2.3 α/khr-cm^2 to 0.9 α/khr-cm^2 for 40 nm technology [5]. However, with ever-decreasing node capacitance and low supply voltages, alpha particles originating from the package, on-chip interconnects and wafers will remain a significant source of soft errors.

1.1.2 Space Radiation

Radiation in space predominantly consists of ionizing radiation that exists in the form of high-energy, charged particles. There are three sources of natural space radiation: galactic cosmic rays (GCR), solar particle events (SPEs), and trapped radiation.

Galactic cosmic rays originate outside the solar system and may generate showers of secondary particles that penetrate and impact the earth's atmosphere. Primary cosmic rays, originally produced in various astrophysical processes, are composed largely of protons and alpha

particles. When the primary cosmic rays impact the atmosphere, secondary cosmic rays are generated, which include mainly electrons, photons and muons [6].

SPEs occur when electrons, protons, and alpha or heavier particles emitted by the sun accelerate to extremely high energies in interplanetary space. These particles temporarily increase the radiation in interplanetary space around the magnetosphere, with the potential to penetrate to lower altitudes in the polar regions [7].

Trapped radiation is the result of particles from solar wind and cosmic rays becoming trapped in two magnetic rings surrounding the earth, which are referred to as Van Allen belts. These belts are comprised of an outer and inner component; the outer belt is formed by high energy electrons with an energy value as high as 10 MeV, while the inner belt is formed by a combination of protons with an energy value as high as 400 MeV and electrons with an energy value range that spans hundreds of keV [7].

High-energy cosmic rays do not directly generate electron-hole pairs in silicon, but rather cause soft errors mainly by neutron-induced silicon recoils. Neutrons colliding with Si nuclei transfer enough energy to displace Si nuclei from the lattice, which then break into lighter fragments that generate charge and cause soft errors.

The energy of silicon reaction products is significantly higher than that of alpha particles, thus rendering high-energy cosmic rays more likely to upset semiconductor devices than alpha particles. In addition, the charge density of neutron-generated silicon recoils ranges from 25 to 150 $fC/\mu m$, while alpha particles generate around 16 $fC/\mu m$. Therefore, soft error effects such as multiple-bit upset (MBU) and single event latch-up (SEL) are generally triggered by high-energy neutrons instead of alpha particles, considering the fact that their linear energy transfer (LET) threshold is typically above 16 $fC/\mu m$ [8].

1.1.3 Thermal Neutron-Induced Boron Fission

Boron is widely used as a p-type silicon doping implant and is also extensively used in the formation of BPSG dielectric layers. It naturally occurs with two isotopes, ^{11}B (80.1%) and ^{10}B (19.9%). When a ^{10}B nucleus captures a low-energy neutron, or thermal neutron, a fission reaction occurs and produces a 0.84 MeV ^{7}Li recoil nucleus, a 1.47 MeV alpha particle, and a 478 keV gamma particle. While both Li recoil and alpha particle are capable of causing soft errors, the Li recoil hitting a sensitive node has a higher possibility of inducing a soft error, considering the fact that it generates more charge per unit length of travel. For the traditional BPSG-based semiconductor process, this is sometimes the primary cause of soft errors. Several methods have been developed to mitigate the soft error rate (SER) due to the activation of ^{10}B in BPSG, the most simple and direct of which is to abandon the use of BPSG from the process flow. Since BPSG was eliminated at the technology node beyond 0.25 μm, the SER has experienced a dramatic drop. 180 nm static random-access memory (SRAM) devices with the BPSG dielectric layer eliminated were reported to exhibit an SER drop by a factor of 600 [9].

1.2 Single-Event Effect

The naturally occurring space radiation environment, along with semiconductor fabrication materials and process, produce transient and permanent changes in the electrical properties of integrated circuits and solid-state devices. These changes may cause malfunctions, not only in avionics, space, and military electronics, but also in commercial semiconductor devices in the terrestrial environment. Therefore, a considerable amount of research focusing on the mechanisms of various radiation effects has been conducted.

The Joint Electron Device Engineering Council (JEDEC) standard JESD89A defines a single event effect (SEE) as “any measurable or observable change in state or performance of a

microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike" [10]. SEEs are induced by the interaction between an ionizing particle and electronic components. As previously discussed, these ionizing particles can be either primary (including heavy ions originating from space environment or alpha particles emitted by radioactive impurities in the die and packaging materials), or secondary particles (recoils produced by the nuclear interaction between a particle, such as a thermal or high-energy neutron or a proton, and atoms in the die, such as silicon and oxygen). SEEs can be generally categorized into 2 types: non-destructive and destructive effects.

Outlined below are the nondestructive functional errors, also referred to as soft errors:

- Single-event upset (SEU): A change of state in electronic devices caused by energetic particles striking a sensitive node.
- Multiple-bit upset (MBU): Upsets of two or more bits in the same word triggered by a single particle event.
- Single-event functional interrupt (SEFI): A soft error that causes a detectable malfunction of devices, and is commonly associated with a change in control bit or register.
- Single-event transient (SET): A transient voltage spike at a certain node in an IC that may not cause an upset unless latched by a storage element.

Other SEEs can cause non-recoverable errors or even destruction of devices [11]. These so-called "hard errors" include:

- Single-event latch-up (SEL): Single particle strike induced parasitic bipolar formation in CMOS wells that results in a low-impedance path between power and ground, resulting in a high current condition.

- Single-event burnout (SEB): Simultaneous high currents and high voltages initiated by a high-energy particle strike can induce second breakdown of the parasitic bipolar transistor in a power metal-oxide semiconductor field-effect transistor (MOSFET) which may subsequently cause a meltdown of the device [12].
- Single-event gate rupture (SEGR): A condition in which a single particle strike results in a breakdown and ensuing increase in gate leakage current of a MOSFET. SEGR is typically observed at the same time as SEB in power MOSFETs.

This thesis examines the mechanisms and mitigation techniques of soft errors, with particular attention devoted to SET and SEU.

1.3 Motivations

Since the discovery of soft error in electronic devices, many techniques have been proposed aiming to mitigate SET and SEU. These mitigation techniques can be roughly divided into three categories: device level, system level and circuit level.

Technology- or device-level hardening requires fundamental changes of fabrication process to limit charge collection in ICs. One popular and promising technique is the silicon-on-inductor (SOI) structure [13], in which the active device is on a thin silicon layer that is dielectrically insulated from the substrate.

System- or architecture-level techniques detect and correct soft errors by adding extra information to the data. One of the most popular approaches is the use of error detection and correction (EDAC) codes, which use redundant bits to detect bit flip in the data [14].

Other approaches deal with SET and SEU at the circuit level. Among them, triple modular redundancy (TMR) is an easily applicable method that can be implemented, not only at the circuit level, but additionally at the system board or module level. Although TMR has proven efficient in

masking soft errors, it also typically implies a considerable hardware overhead. In this day and age, most researchers have turned to radiation hardening by design (RHBD) approaches. This entails that the circuit structure is designed in such a fashion that, rather than relying on specialized devices or process features, the special circuit topologies and/or layout can provide sufficient radiation hardening.

Numerous RHBD techniques have been proposed to improve the tolerance of the CMOS device against radiation. Some of the techniques provide hardening on the gate level by introducing extra transistors into the circuit, such as the dual-interlocked storage cell (DICE) [15] and soft-error immune latch (SEILA) [16]. Contrastingly, other techniques rely on a delicately designed layout, such as guard bands/rings, guard drains [17], and layout design through error-aware transistor positioning (LEAP) DICE [18]. Most of the RHBD techniques primarily apply to latch and flip flop structures, with the exception of guard rings and guard drains, which can be utilized for any cell at the sensitive node). However, with the technology trends of smaller feature size, lower supply voltage and higher operating frequency, a resulting increase in combinational logic soft errors has been observed. It is reported that, normalized to the number of cells, SER for combinational dynamic logic and SRAMs in 0.25 μm test circuits are essentially synonymous [19]. Furthermore, the need for RHBD techniques in combinational logic is of equal (if not of more) importance to that in memory elements.

Despite the urge for combinational logic rad-hardening, minimal research has been conducted to study SER in dynamic logic circuits, which are considerably faster than static CMOS and are often used in the performance-critical blocks of microprocessors, digital signal processors and memories. Operating by periodically charging circuit nodes, dynamic logic is usually considered more vulnerable to radiation than its static counterpart. Along with the decreasing node capacitance, charge stored on the nodes is becoming so small that even a minimal perturbation or any single

particle strike may discharge the nodes and alter their states. A few rad-hardening methods for dynamic logic were reported in last two decades, most of which took the gate-level approaches that either doubled the circuit size or introduced a considerable delay that slowed down the dynamic logic circuits. On the other hand, recent research on layout techniques has achieved significant hardening by simply repositioning transistors or adding a small component in the layout. Furthermore, layout techniques appear to be more promising in dynamic logic application. Therefore, thorough research directed towards cost-effective and easy-to-apply approaches for dynamic logic rad-hardening is essential.

1.4 Research Objectives

Based on the discussion above, the overall objectives of this thesis work are to study dynamic logic circuits with several RHBD approaches, reduce the SER through layout adjustment, and compare and verify the improvement through the use of simulation and radiation experiments. In order to achieve the objectives, the steps below are adhered to:

1. Study different SET/SEU mechanisms and effects during dynamic logic operations.
2. Propose a layout-level RHBD technique that introduces relatively small area overhead and delay.
3. Build three-dimension (3D) technology computer aided design (TCAD) device models for the proposed approach and some previous rad-hardening methods.
4. Perform mixed-mode heavy ion simulation under various conditions, comparing the effect of particle strike incidence, energy and frequency on SEU probability.
5. Design and fabricate a 130 nm testing chip that contains different layout-level RHBD dynamic logic circuits.

6. Build up a testing system with printed circuit boards (PCBs) and carry out heavy ion experiments using different particles, incident angles, operating frequencies, and power supply voltages.

1.5 Thesis Outline

The remainder of the thesis is organized as follows: Chapter 2 provides an introduction outlining how a domino logic circuit operates, along with a comparison to static CMOS logic, and analyzes how SET/SEU affects dynamic logic circuits. Chapter 3 provides a review of previous RHBD methodologies for logic circuit and memories. Chapter 4 proposes a layout-level RHBD method for domino logics, and discusses the design implementation and simulation of 3D device models using Synopsys Sentaurus TCAD. The simulation results, along with a comparison to other layout techniques, is subsequently listed and analyzed. Chapter 5 describes the testing chip layout design in IBM 130 nm CMOS technology. In Chapter 6, the radiation testing methodology and results are discussed, following a description of the testing system architecture. Chapter 7 concludes the thesis and presents suggestions for future works.

CHAPTER 2 DYNAMIC LOGIC

Static CMOS logic with a fan-in of *N* requires 2*N* devices and is relatively slow as a result of both the NMOS and PMOS gate capacitance at each input. This chapter investigates the dynamic logic family, which is an alternative logic family that has been shown to substantially reduce the number of transistors to *N+2*, while avoiding static power dissipation.

2.1 Basic Principles of Dynamic Logic

The basic structure of an n-type dynamic logic gate is displayed in **Figure 2.1**. The pull-down network (PDN) is constructed the same manner as in static CMOS logic. With the addition of a clock input, dynamic logic operates in a periodical sequence of precharge and evaluation phases. The output logic value is represented by the presence or absence of charge at the *Out* node.

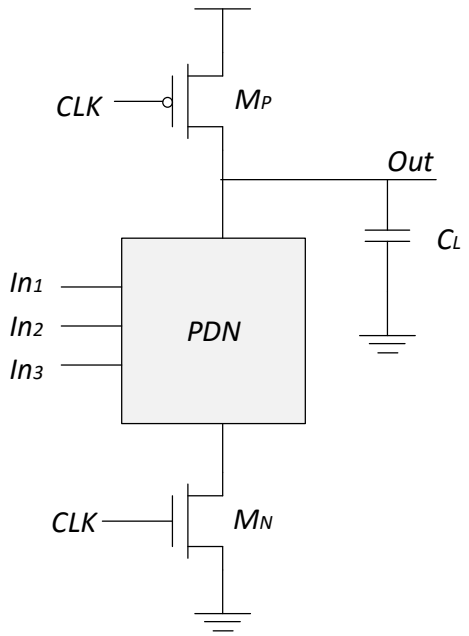


Figure 2.1 Structure of an n-type dynamic logic

2.1.1 Precharge Phase

When $CLK = 0$, the PMOS transistor M_P turns on and the output node *Out* is charged to *VDD*. Due to the fact that the NMOS transistor M_N is "off", the pull-down path is disabled. Therefore, no static power is consumed during this period. This stage is referred to as precharge, in which the output is precharged to logic 1 and prepared for evaluation in the next stage.

2.1.2 Evaluation Phase

When $CLK = 1$, the PMOS transistor M_P is shut off and the NMOS transistor M_N is turned"on". Depending upon the PDN topology and the input values, the output will be conditionally discharged. During this phase, if the PDN conducts, a resulting low resistance path from Out to GND transpires that discharges the output node. In the case where the PDN is "off", the precharged value on the output node remains stored on C_L, a combination of junction capacitance, wiring capacitance, and input capacitance of the fan-out gates. Note that, during the evaluation stage, the only possible path between the output node and supply rail is from output to *GND*. Therefore, once the output node is discharged, it will not go up to *VDD* until the next precharge phase. In other words, the output can make a maximum of one monotonic falling transition during each evaluation phase.

2.1.3 Dynamic Inverter

Take the simplest dynamic logic gate, a dynamic inverter, for example, as displayed in **Figure 2.2**. In precharge phase, the low *CLK* signal cuts off the pull-down path and turns the PMOS on, and thus *Out* is pulled up to *VDD*. During this period, regardless of the value applied to the input, the output will not be affected. When *CLK* goes to high, the gate enters the evaluation phase where the pull-up path is turned off. In this case, two possible situations exist. If *In* remains low for the

whole evaluation phase, considering the fact that both pull-up and pull-down path are "off", *Out* will be floating and retain its value as long as the leakage is negligible. For this reason, the clock frequency cannot be too low, as otherwise the evaluation phase will be so long that the output will gradually lose all of its charge through the leakage current. On the other side, if *In* goes up anytime during evaluation, *Out* will be quickly discharged due to the low-impedance path to *GND*. At this point, there is no way for *Out* to be recharged regardless of the input value, and it will remain low until the next precharge stage.

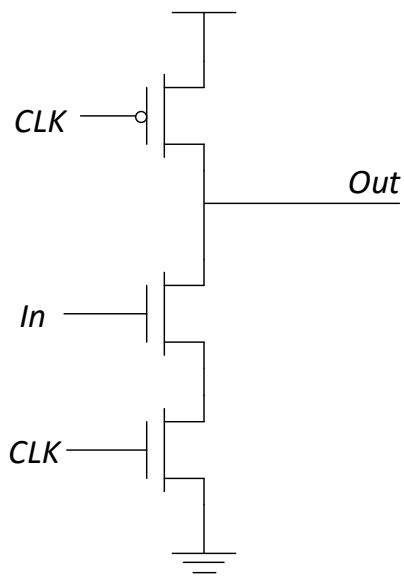


Figure 2.2 Dynamic inverter

For this dynamic inverter, the following function is thus realized:

$$Out = \overline{CLK} + \overline{A} \cdot CLK \tag{2.1}$$

2.2 Domino Logic

2.2.1 Domino Logic Basics

As discussed above, the only effective transition at the output during evaluation is from 1 to 0, which means the output for dynamic logic is always monotonically falling. On the contrary, dynamic logic always expects a monotonically rising signal at its input; this is the only possible

way to create a conducting pull-down path during evaluation that discharges the output node. The case in which two dynamic inverters are directly connected is depicted in **Figure 2.3**. In precharge phase, both nodes *X* and *Y* are charged to *VDD*. At the beginning of evaluation phase, *CLK* shifts from 0 to 1, and turns on M_{n2} and M_{n4} simultaneously. Because of the fact that $X = 1$, M_{n3} is already turned on, node *Y* is discharged through M_{n3} and M_{n4} to *GND*. Once the output drops, it stays low until the next precharge phase. In other words, output *Y* will not change with input *A*. Consequently, directly cascaded dynamic gates will not perform the expected function correctly.

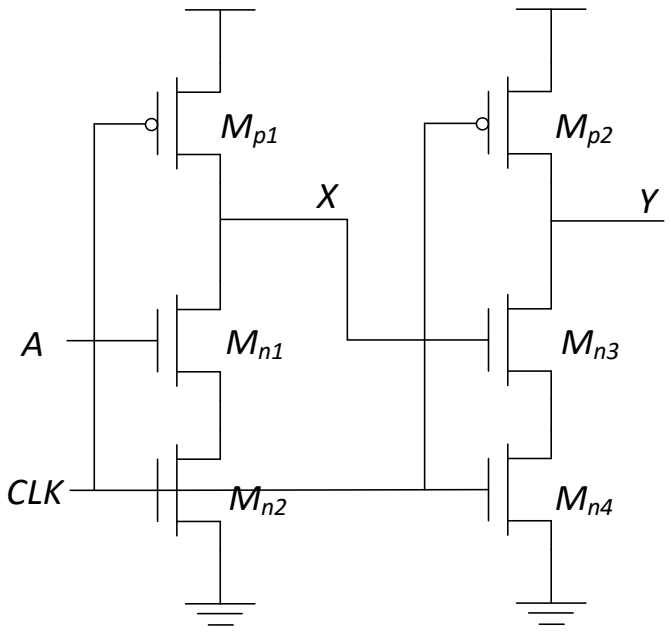
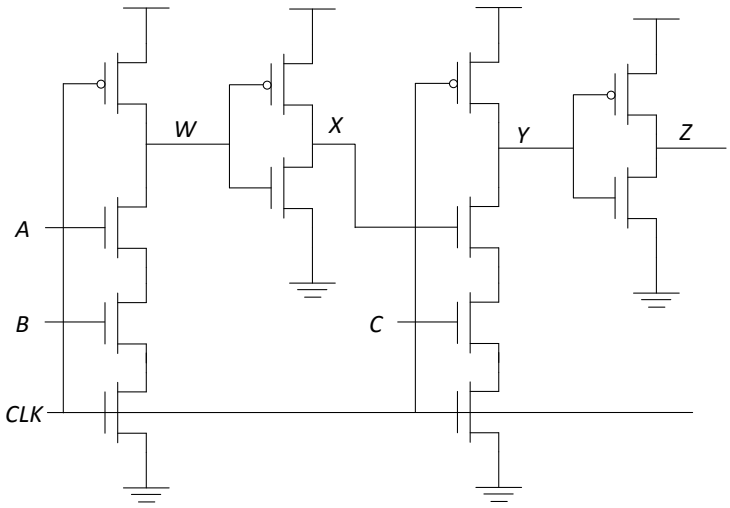


Figure 2.3 Directly connected dynamic inverters

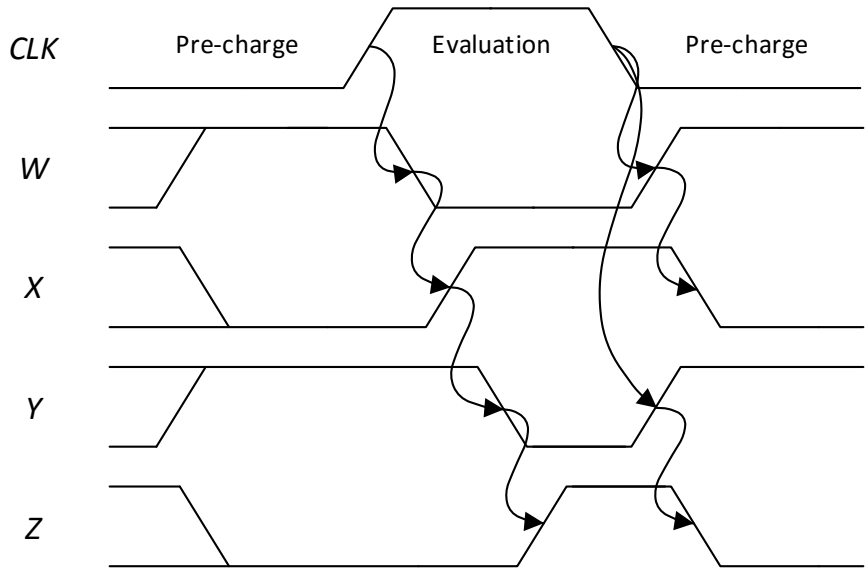
To solve the monotonicity problem, a structure called domino logic is often exerted, which inserts a static CMOS inverter between dynamic stages. While this may appear to conflict with the point of dynamic logic at first glance, the ability to avoid PMOS transistors in order to increase speed renders the domino logic structure very functional, as it is able to convert a monotonically falling output into a monotonically rising input suitable for dynamic gates. The overall speed is not degraded, as the static inverter connects primarily to the NMOSs in dynamic logic gates.

Subsequently, the P/N ratio in the inverter is often sized larger than usual to favor rising output, which is the transition of primary concern to us.

The structure of two cascaded domino AND gates is depicted in **Figure 2.4**(a). The timing diagram of each signals is depicted in **Figure 2.4**(b), assuming inputs A, B and C are high. As can be observed, a falling output at *W* is converted by the HI-skew inverter into a fast rising signal *X* that is also an effective input for the next domino AND gate. Such a dynamic-static pair together is referred to as a domino gate, as the evaluation process of each precharged gate triggering the next precisely resembles a chain of dominos tipping over.



(a)



(b)

Figure 2.4 Cascaded domino AND gates

2.2.2 Keepers

Owing to the fact that inputs to dynamic logic primarily connect to NMOSs, dynamic circuits have poor input noise margins. If, due to noise, the input rises above V_t during evaluation, the input transistors would be weakly turned on and irreversibly discharge the output. Furthermore, dynamic circuits, as mentioned before, are susceptible to charge leakage on the output node. Voltage on a dynamic node will drop over time through subthreshold, gate and junction leakage, provided it is precharged and left floating in evaluation. Depending on process, voltage and temperature, the time constants are usually in the range of nanosecond to millisecond.

Both noise margins and leakage problems, however, can be addressed by the use of a keeper circuit. The keeper circuit operates by stabilizing the output at the supply voltage when it would otherwise float or incorrectly degrade. A conventional keeper added to a domino buffer is illustrated in **Figure 2.5**. During evaluation, if the dynamic node $X = 1$, then the inverted output $Y = 0$, and the keeper is turned on to prevent X from floating. Considering the input signal, if it rises slightly above V_t and weakly turns on the pull-down path, the fact that Y is not immediately

affected and remains at 0 will trigger the keeper to attempt to fight against the weak conducting current, while subsequently holding *X* at the correct voltage level. However, this contention also exists when *X* falls and opposes the transition even if it is supposed to. For this reason, the keeper must be designed much weaker than the transistors in the PDN, allowing *Y* to eventually rise and turn off the keeper in order to avoid further static power dissipation. For a dynamic gate with small transistor sizes, the keeper should be weaker than a minimum-sized transistor, which can be achieved by increasing the keeper gate length. A number of keeper designs have been proposed to further address issues such as area [20], noise margin [21][22][23], and power dissipation [24][25]; while in this work, we will stick to the conventional keeper design so as to easily make comparisons between different layout level approaches.

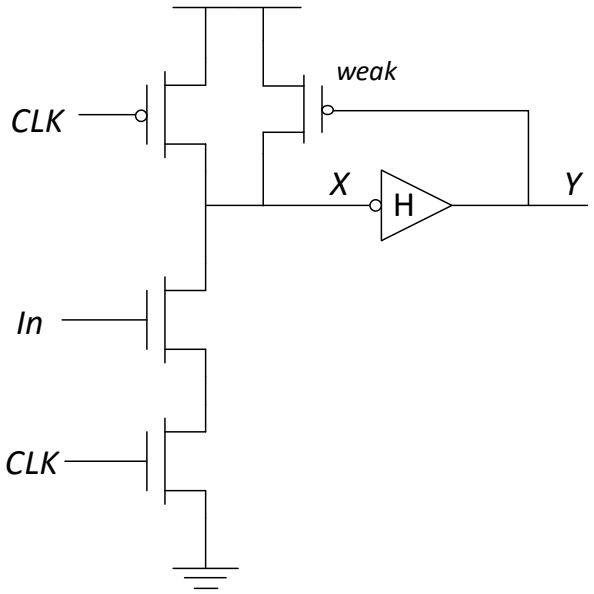


Figure 2.5 Domino buffer with a conventional keeper

2.3 SEU in Dynamic Circuits

2.3.1 Ion Strike

When charged particles strike a semiconductor device, charge is generated along the track. If the charge generation occurs in the bulk, it will simply recombine or diffuse out through supply

rails. If the ion strike occurs at or near the diffusion regions, the electrons and holes generated will be affected by the electric fields at the junctions, thus potentially creating a current that will disturb the correct circuit operation. The direction and magnitude of such a current largely depends on the structure of the hit device and the bias at its terminals. As depicted in **Figure 2.6**, an ion strike on the drain of an NMOS, or N-hit, may cause the drain voltage to drop by generating a transient current that flows towards the P-well and substrate. Contrarily, a hit on the PMOS drain, or P-hit, usually results in a current flowing towards the drain and leads to a voltage spike. When a device is "on", an ion strike will essentially fortify the logic level at the hit drain. SET occurs primarily when an ion hits a device that is "off", and potentially turns it on.

In Simulation Program with Integrated Circuit Emphasis (SPICE), the SET current can thus be modeled by injecting a double-exponential current source at the site of particle strike [26]:

$$I_{in}(t) = \frac{Q}{\tau_\alpha - \tau_\beta}\left(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}\right) \tag{2.2}$$

In the equation above, Q represents the positive or negative charge deposited due to particle strike, τ_α is the collection time constant, and τ_β is the ion-track establishment time constant. The values of constants τ_α and τ_β are influenced by several process-related factors.

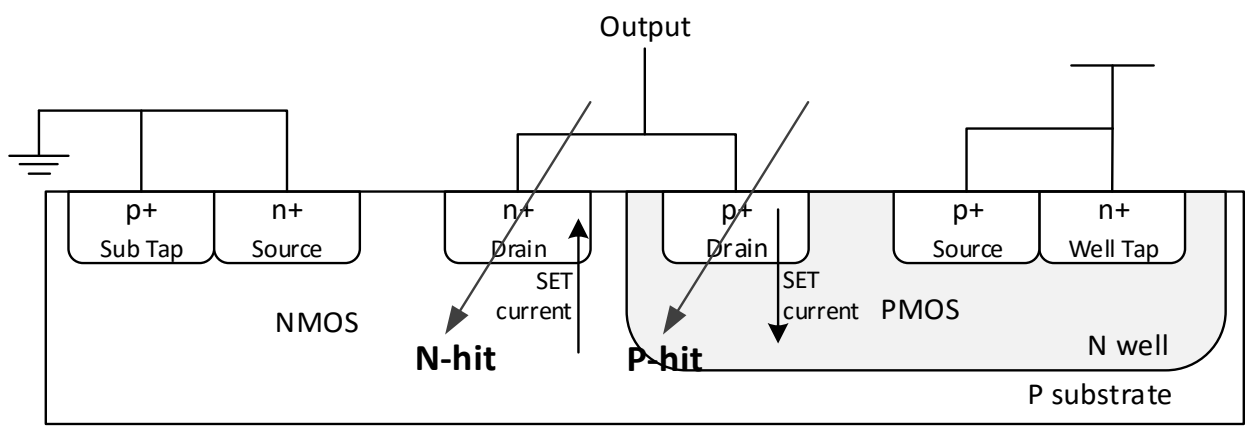


Figure 2.6 SET current generated by N-hit and P-hit on drains

2.3.2 SEU in Precharge

Due to its two-phase operation, dynamic logic has a fairly different response to ion strike from static logic. When the circuit is in precharge, an ion hit on the drain of an NMOS can create an SET current that discharges the output node. Because of the fact that the precharge PMOS transistor is "on", the output voltage will eventually recover. If, however, the next evaluation phase begins before the output voltage fully recovers, an upset may consequently occur. Such soft errors in dynamic logic are referred to here as SEUs instead of SETs because, unlike in static logic where transient current can recuperate over time, SETs that occur in the described conditions always result in a bit flip due to lack of pull-up path.

This SEU mechanism is simulated using a 130 nm domino buffer circuit. **Figure 2.7** depicts an N-hit on the drain of the sensitive NMOS transistor. The transient current deposits a total charge of 5.6 fC, with $\tau_\alpha = 100\ ps$ and $\tau_\beta = 5\ ps$. These numbers are used as an approximation of pulse shapes observed in 130 nm technology TCAD simulations [27]. As demonstrated in **Figure 2.8**, because of the fact that the output node *Out_inv* of the dynamic inverter is not fully charged when evaluation starts, an upset occurs at the buffer output *Out_Buf*.

The dynamic circuit is only vulnerable to such an SEU mechanism at the end of a precharge phase. This window of vulnerability is actually the time required for the circuit to be charged up to a logic high level, with the worst case existing when all the NMOS devices in the PDN are "on".

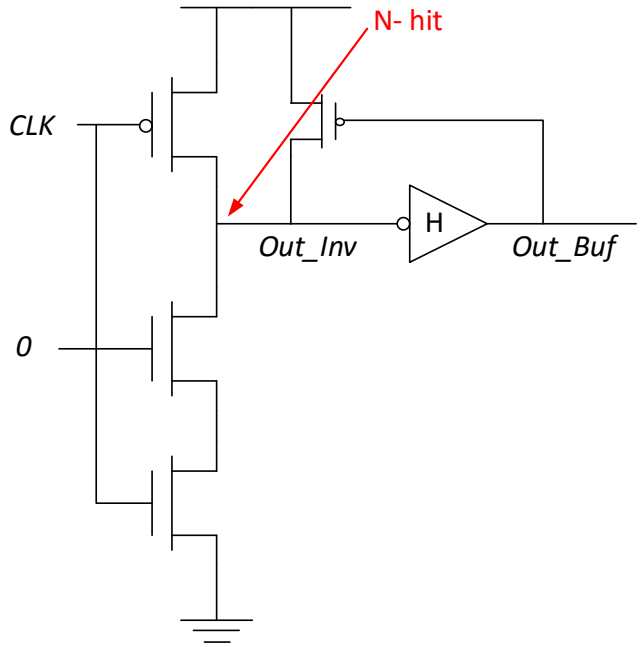


Figure 2.7 N-hit on a domino buffer during precharge

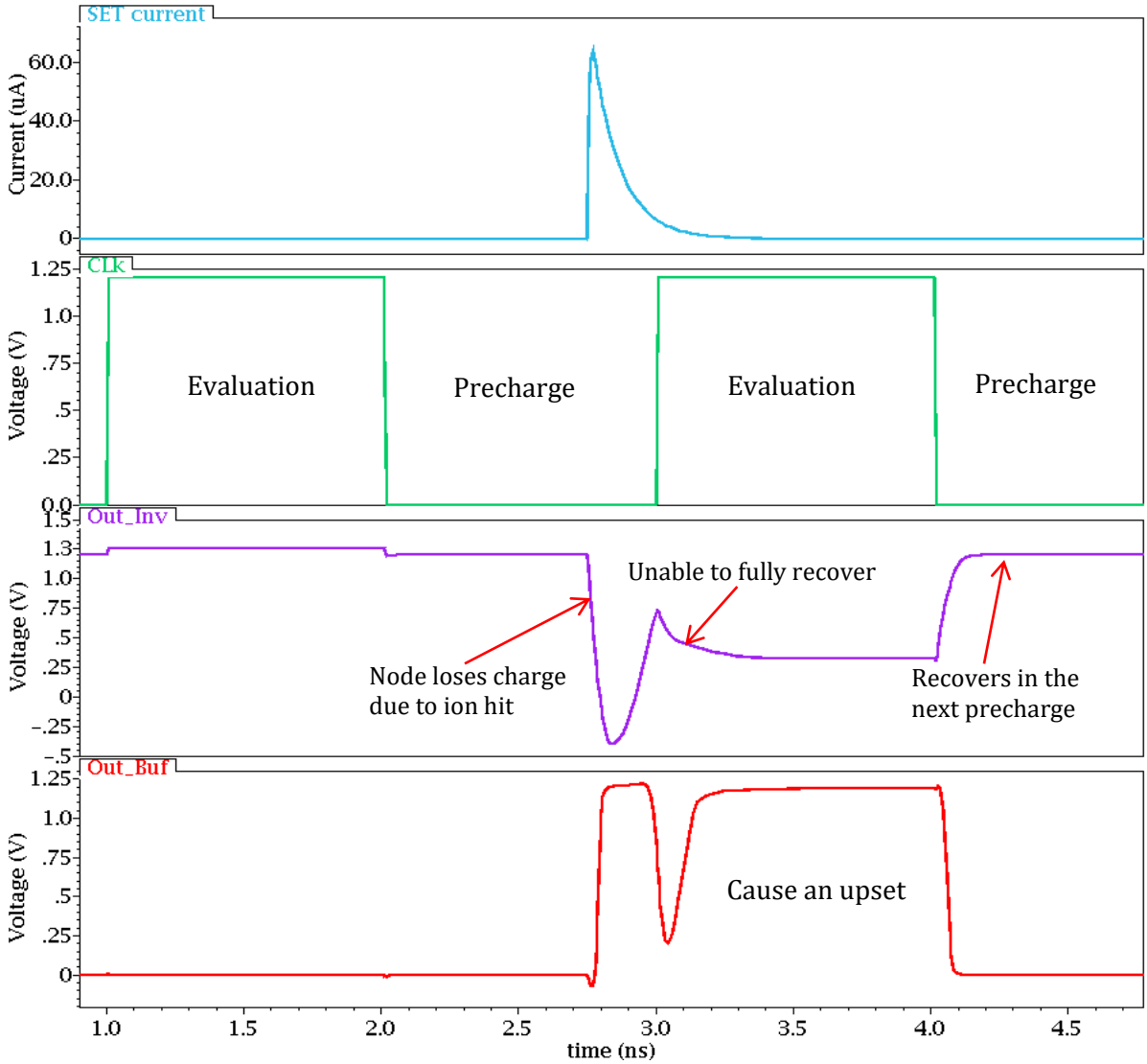


Figure 2.8 N-hit that occurs at the end of precharge

2.3.3 SEU in Evaluation

The dynamic circuit is susceptible to ion strike during the evaluation phase as well. The most distinct difference that separates dynamic logic from its static counterpart is the use of charge stored on a node to represent a high logic level. It is these nodes, however, that are sensitive to radiation and inclined to lose charge if hit by particles. Considering the fact that a floating node has no active path to *VDD*, it is impossible to recover from charge loss until the next precharge phase.

The same domino circuit as in **Figure 2.7** is simulated for ion hit during evaluation, with the results depicted in **Figure 2.9**. As can be observed from the waveforms, dynamic inverter output node *Out_Inv* decreases to approximately 0.7 V below *GND* and then remains low until fully charged to *VDD* in the precharge phase. The consequent pulse width at node *Out_Buf* is determined by the propagation delay in the circuit and the time between ion hit and the falling precharge clock edge. Furthermore, an upset will not happen if the pulse is not able to reach a latch before the precharge phase.

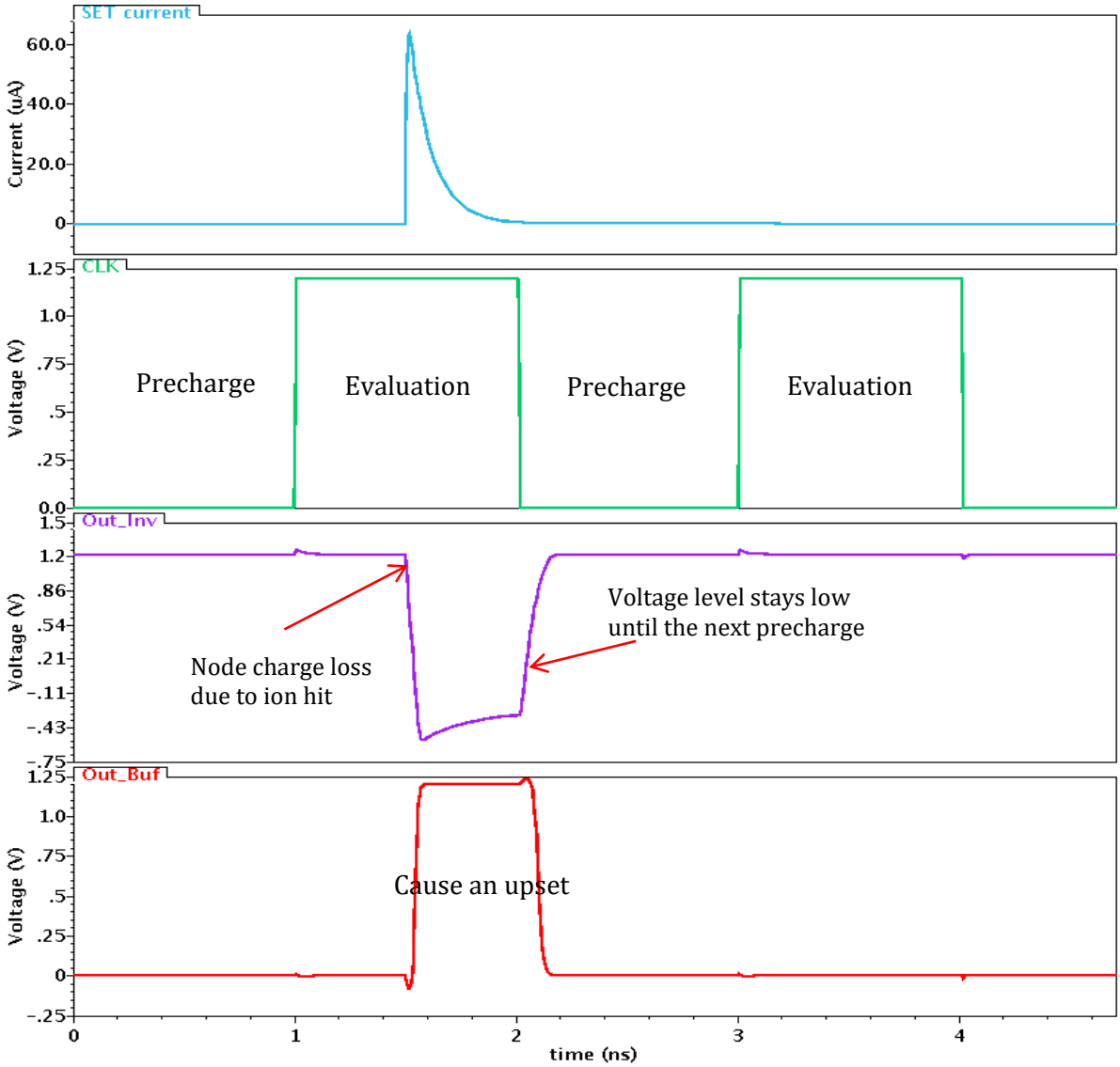


Figure 2.9 N-hit that occurs during evaluation

2.4 Dynamic Logic versus Static Logic

As mentioned in the beginning of this chapter, dynamic logic has numerous advantages over static logic. A series of simulations are performed in order to quantitatively compare these two logic families in terms of area, power dissipation, delay and critical charge. Critical charge Q_{crit} refers to the minimum amount of charge collected on a sensitive node due to a particle hit that is able to cause an upset. To determine Q_{crit}, the deposited charge is gradually increased until an SET appears at the end of a logic chain which causes a bit flip in the storage element that follows, as depicted in **Figure 2.10**. The transistor sizing of the unit domino buffer is demonstrated in **Figure 2.11**. Considering the fact that precharge occurs while the gate is idle, the PMOS transistor width is chosen to deliver half driving current of the pull-down network. This, at the cost of greater rising delays, minimizes the parasitic capacitance and the capacitive load on the clock. To be comparable, all of the other circuits are sized to carry out an effective rise and fall resistance equal to that of the unit domino buffer. The comparison in **Table 2.1** is made based on the premise that all of the circuits have the same switching activity, and that only the rising propagation delay is considered for FO4 delay estimation.

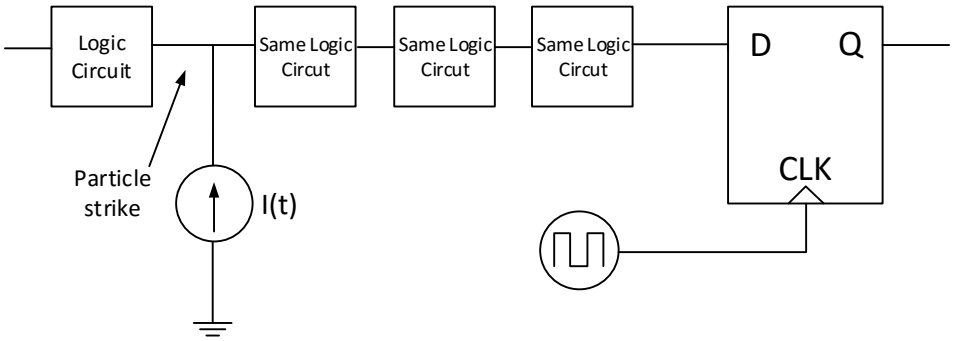


Figure 2.10 Logic chain used for SEE simulation

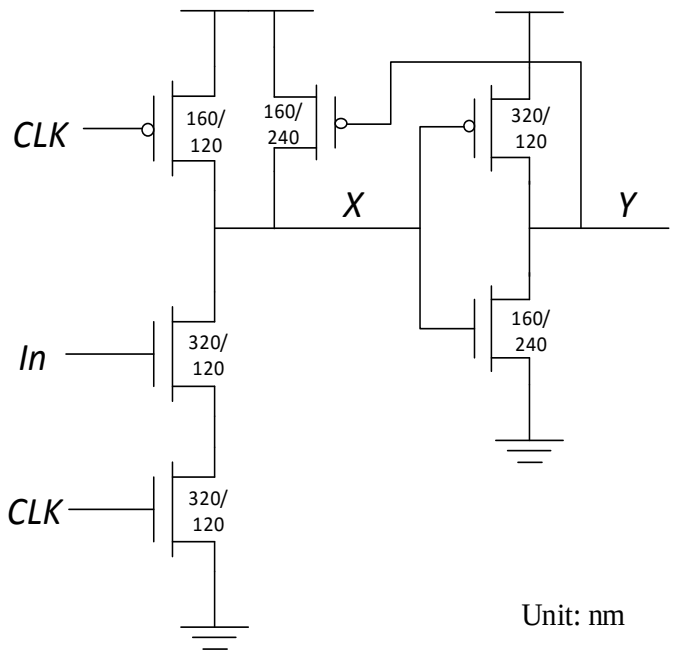


Figure 2.11 Domino buffer sizing

Table 2.1 Comparisons between dynamic and static logic circuits

Logic	Area (a.u.)	Power (a.u.)	FO4 Delay (ps)	Q_{crit} (fC)
Domino buffer	1	1	62.31	3.55
Static buffer	0.64	1.38	64.25	8.96
Domino AND2	1.45	1.83	69.90	3.73
Static AND2	1.09	0.73	75.55	9.68
Domino OR2	1.18	1.20	67.17	3.94
Static OR2	1.27	1.50	93.74	11.39
Domino AND3	1.93	2.59	77.85	3.93
Static AND3	1.73	1.10	86.95	10.47
Domino OR3	1.36	1.61	71.97	4.28
Static OR3	2.27	3.23	122.41	13.96

Comparing each domino logic circuit to its static counterpart from the table above, the following conclusions can be reached:

1. Dynamic gates are particularly suitable for wide NOR/OR functions, as they are smaller, much faster, and have less power dissipation.
2. For logic with a large number of inputs, the dynamic circuit normally requires less area.
3. The power dissipation of dynamic logic varies depending on the circuit structure and system specifications. It would seem that dynamic logic presents an advantage over static logic in terms of power due to its lower physical capacitance and zero (or little) static-power dissipation. Such benefits, however, would be offset when the clock power and higher switching activity as a result of periodic precharge and evaluation operations are considered [28].
4. Due to the reduced number of PMOS transistors that are innately slow, dynamic circuits are always faster than static circuits.
5. Despite its increased speed and reduced implementation area that are well suited to today's high-speed very-large-scale integration (VLSI) systems, dynamic logic is at least twice as vulnerable to radiation effect as static CMOS logic circuits. This further emphasizes the motivation and importance of this work: an effective method to harden dynamic logic against radiation is needed.

CHAPTER 3 LITERATURE REVIEW

Owing to its high speed performance and the ability to implement complex logic functions with fewer transistors, dynamic logic plays a critical role in applications such as processors [29][30][31] that are targeted towards high frequency operation and low pipeline latency. However, as the feature size shrinks, the increasing susceptibility to soft errors has become an obstacle to its wider application in modern designs. Some traditional circuit-level RHBD techniques can still be applied. However, due to the nature of dynamic logic, these improvements are often very limited. In the meantime, a few other rad-hardening designs that utilize the characteristics of dynamic logic have proven to work quite efficiently. Some of these circuit-level approaches will be introduced in this chapter. In terms of physical level, on the other hand, little research has been conducted in studying an RHBD approach specific to dynamic logic. Several layout-level rad-hardening techniques for static logic and memory elements will be reviewed and discussed as well.

3.1 Circuit-level RHBD

The circuit-level RHBD approaches focus on blocking the propagation of SEUs from hit node to adjacent devices by either properly sizing the gates or introducing a certain redundancy to the circuit.

3.1.1 Triple-Modular Redundancy

The TMR technique was first introduced in 1962 [32]. The basic concept can be illustrated in **Figure 3.1**, where the three blocks labeled *M* are identical modules, each with a single output. The three outputs are sent to the majority voting circuit. In contrast to the relatively complex functions computed in the triplicated modules, the majority voter is a very simple circuit; thus it is considered

much more reliable than the other TMR components. Assuming the voter does not fail, if only one of the three modules fails, the other two can correct and mask the fault. TMR techniques are often applied to SRAM-based Field Programmable Gate Arrays (FPGAs) in order to protect the configuration memory against soft errors [33][34]. Although TMR strategies are easy to implement and offer tremendous improvements in reliability, they are extremely expensive in terms of area and power consumption.

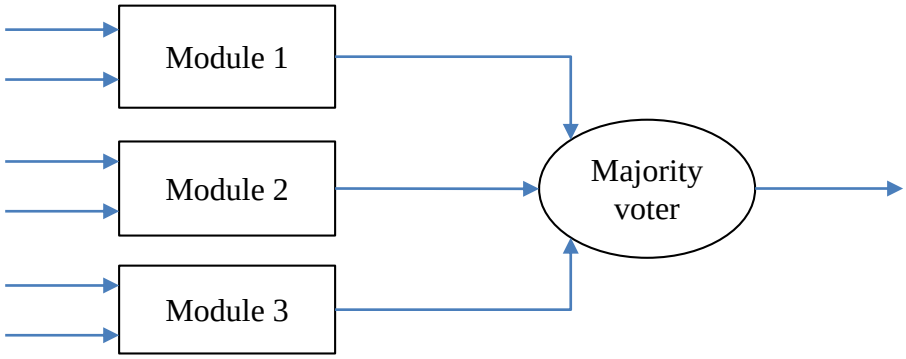


Figure 3.1 TMR block

3.1.2 Gate Sizing

The following three factors determine whether a particle strike causes an SEU at the hit node: the total charge deposited at the node, the node capacitance, and the drive strength of the gate driving that node [35]. When the size of a transistor increases, both its drive strength and node capacitance increase, resulting in a rapid decrease in the magnitude and duration of the SET. However, larger transistor sizes will also lead to more area overhead. In [35], a gate sizing technique is used to harden combinational logic circuits with some overhead costs. The optimal transistor sizes are obtained by choosing the minimum W/L required to limit the worst case transient pulse to 0.5 *VDD*. In order to achieve cost-effective tradeoffs between SER reduction and overhead,

an algorithm is proposed to determine the gates with lowest logical masking probability, which are the critical ones that need to be hardened.

According to the paper, this gate sizing technique achieves a 90% coverage for SER reduction across four processes ranging from 180 nm to 70 nm, with an average overhead of 38.3%, 27.1%, and 3.8% in area, power, and delay.

3.1.3 Dual Interlocked Storage Cell

Proposed by T. Calin et al. in 1996 [15], DICE-based latches, flip-flops and memory cells have been widely used for SEU immunity. A basic DICE storage element, as illustrated in **Figure 3.2Figure 3.2**, consists of four interlocked inverters, using two nodes to store each logic state. This dual redundancy strategy has rendered DICE-type latch cells immune to SEUs at technology nodes 180 nm and above [36].

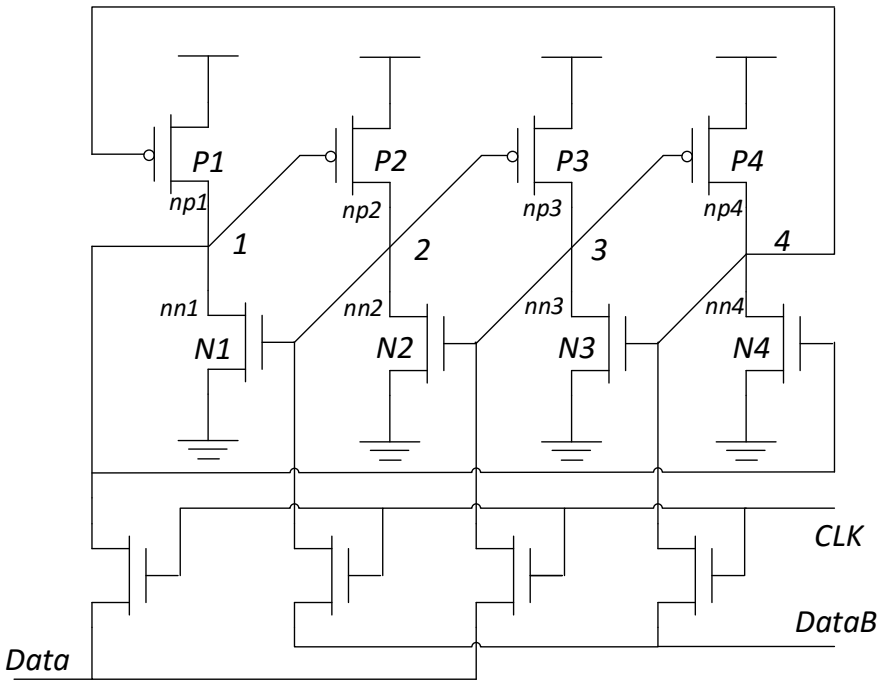


Figure 3.2 DICE structure

The redundancy and self-recover mechanism operate as follows:

Assume that the initial condition for the circuit is as follows: nodes 1 and 3 have logic value 1, while nodes 2 and 4 have value 0. Thus, transistors *N2*, *N4*, *P1* and *P3* are "on", whereas *N1*, *N3*, *P2* and *P4* are "off". Without loss of generality, assume the drain contact of transistor *N1* is hit by a particle. As a result, node 1 temporarily changes its logic state, and turns on *P2* which was previously "off", while turning off *N4* which was previously "on". The fact that both *P2* and *N2* are now "on" causes voltage contention on node 2, whose voltage now depends on the sizes of these two transistors. This voltage shift on node 2 changes the state of *P3* from "on" to partially "on"; in other words, node 3 is weakly driven by *P3*. As for node 4, because both *P4* and *N4* are "off", it is left floating. Therefore, any transient current on node 1 will not affect the original state of node 3 or node 4, and node 1 will eventually recover to its previous state if no other node is affected by the particle strike.

However, as feature size scales below 100 nm, the assumption that a single particle strike merely influences one node is no longer valid. Heavy ion experiment results in [37] indicate an order-of-magnitude increase of cross-section in the traditional DICE structure at an incident angle of 60˚ when compared to normal incidence. With smaller distance between devices, a tilted particle strike is very likely to hit multiple circuit nodes simultaneously, and charge sharing between adjacent devices becomes much easier as well. As a result, conventional DICE topology that relies on spatial separation of sensitive devices is no longer SEU-immune.

3.1.4 C-pass Isolation Dynamic Logic

The authors of [38] argue that, by suppressing the magnitude of an SEU glitch to 60%, the glitch will be unable to propagate to the next logic due to logical masking. In order to achieve such a suppression, single or dual c-pass transistors are added to isolate the hit node from the next stage. An additional keeper can also be added in this methodology to further suppress SEU. An example

of dual c-pass isolation and dual keeper implementation is depicted in **Figure 3.3**. Combinations of different numbers and sizes of the c-pass transistor and keeper undergo experimentation to evaluate tradeoffs between soft error suppression, speed and area. The simulation results show that, with 13.6% and 2.6% overhead in delay and area, respectively, 49% suppression of SEU can be achieved.

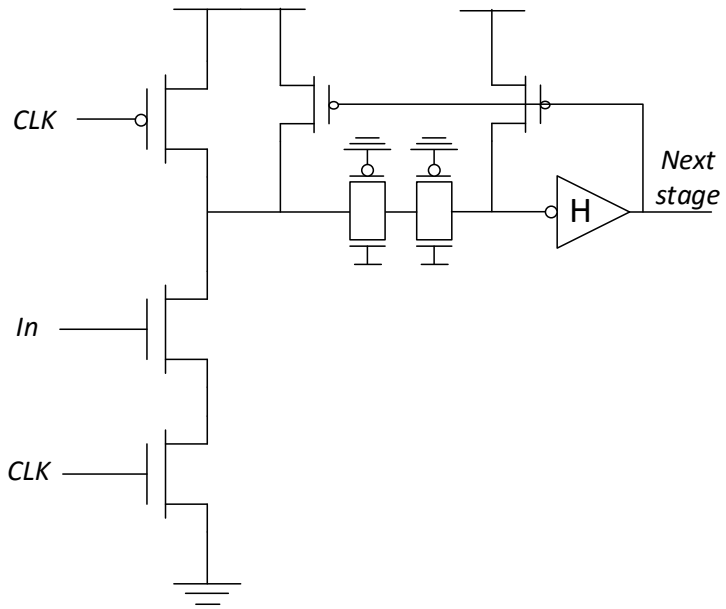


Figure 3.3 Dual c-pass isolation with dual keeper [38]

3.1.5 Dual Redundancy Dynamic Logic

Another SET-tolerant dynamic logic design approach is discussed in [39]. In this design approach, the pull-down network is duplicated to provide dual redundancy, and an OR gate is implemented near the output to correct the value if one of the paths is corrupted. To further improve SET tolerance, two feedback inverters and PMOS keepers can be added. Three design schemes are proposed, and the one with the best trade-off between speed and threshold LET is illustrated in **Figure 3.4**.

The two PDN components *R1* and *R2* are identical. If one of them, *R1* for example, is struck by a particle during a precharge or evaluation phase, *Out1* will be pulled low. However, because

R2 is not affected, *Out2* remains unchanged, and consequently *K1* will be "on" and will try to recover *Out1*. Therefore, as long as no SET occurs on *R2* before *Out1* recovers, Output will not be affected.

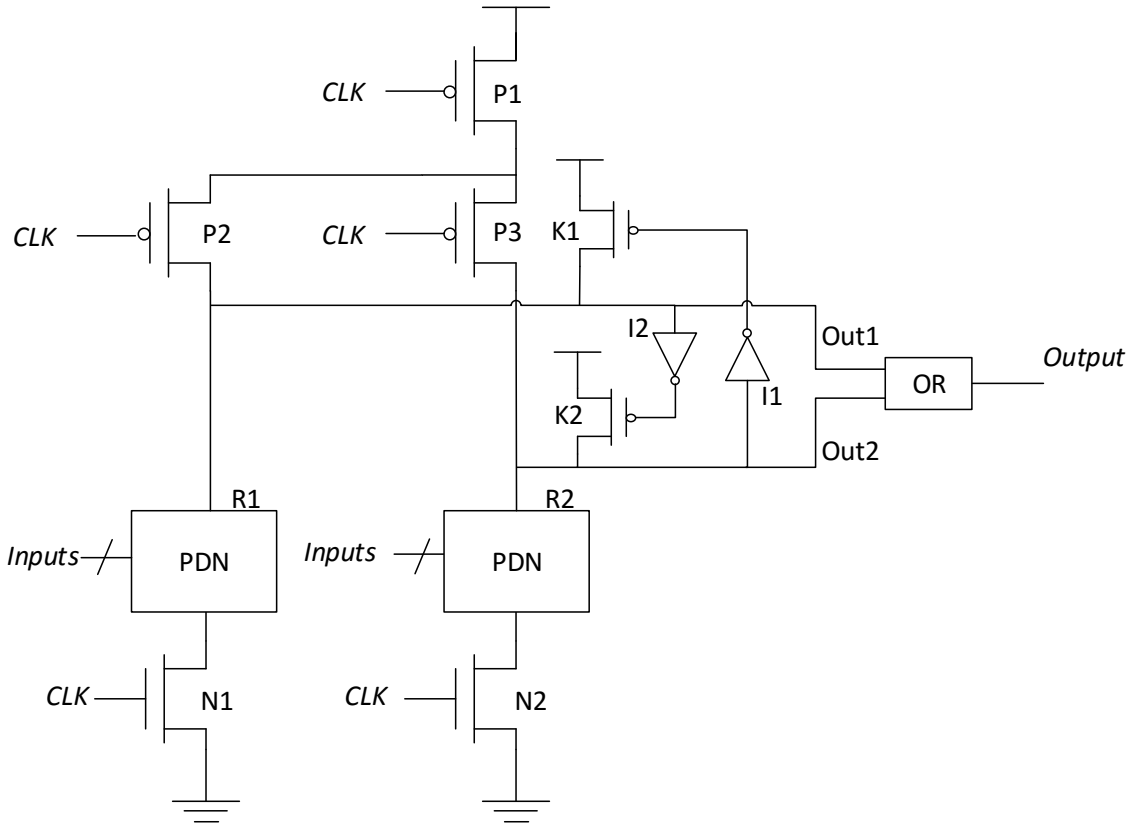


Figure 3.4 Dual-redundant SET-tolerant dynamic logic [39]

As compared to keeper based dynamic logic, this SET-tolerant design has an overhead of 168% in area and 182% in power consumption, as introduced by the duplicate PMOS keeper and inverter when *Output* switches from logic 1 to logic 0. Experiments on test chips designed in a 130 nm process demonstrate the following SER improvements on this proposed design technique, as compared to the traditional keeper based design: the threshold LET increases from 8.2 to 11.8 MeV*cm^2/mg, and at any LET ranging from 12.7 to 99 MeV*cm^2/mg, the cross-section has been reduced by 4.5X to 6X.

3.2 Layout-level RHBD

Due to the proximity of adjacent nodes and reduced node charge in advanced technologies, charge collection at a single node or between multiple nodes has greatly increased. Such increased charge collection has rendered many rad-hardening techniques that target at the circuit-level ineffective. Layout techniques address charge collection in a more straightforward approach. By making adjustments to the device structure, these techniques improve radiation tolerance by either isolating neighboring devices to reduce charge collection or rearranging the devices in a specific pattern, enabling shared charge between certain nodes to be cancelled out and thus mitigating SEU.

3.2.1 Guard Rings and Guard Drains

One way to alleviate charge sharing in adjacent nodes is to surround the critical node with guard rings. This technique was first discussed in [40] as "N-well full isolation". For an NMOS device, a guard ring is formed by isolating it with P+ diffusion regions in the P-substrate. In order to guard a PMOS device, the transistor is surrounded by N+ diffusion regions in the N-well. The top and cross-section views of an NMOS with a guard ring is depicted in **Figure 3.5**.

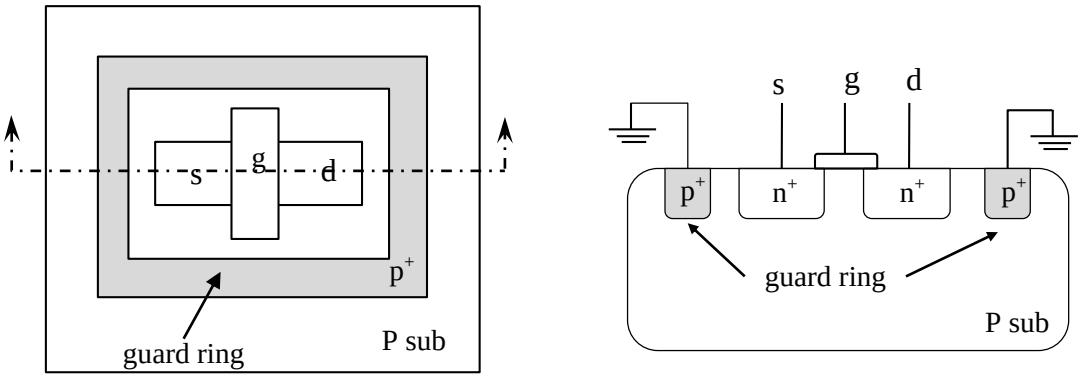


Figure 3.5 Top and cross-section views of an NMOS with a guard ring

As substantiated by simulation and experimental results in previous works, guard rings are more effective for PMOS devices than NMOS [17]. This is due to the different charge collection

mechanisms of the two devices. The total amount of charge collected depends on three processes: drift, diffusion, and bipolar amplification. The electrical field present in a reverse-biased PN junction can collect charge through drift process. Diffusion collection is caused by carriers outside the depletion region diffusing back toward the junction due to concentration gradients. In comparison to drift collection, diffusion collection is a much slower process. Excessive carriers trapped in the well cause well potential collapse, forming a parasitic bipolar junction transistor (BJT) and thus enhancing charge collection. BJT amplification is usually observed in dual-well PMOS transistors due to the higher resistivity of the N-well than that of the P-well. After a particle strike occurs in a PMOS device, electrons in the N-well lower the well potential along the track. The collapsed N-well potential results in a forward-biased PN junction between the source and the N-well surrounding it, which turns on the NPN BJT with the source acting as the emitter, the drain as the collector, and the N-well as the base, as illustrated in **Figure 3.6** [41]. With the BJT turned on, positive charge flows from source to drain, amplifying the SET current. In a dual-well CMOS process, drift is the main form of charge collection in NMOS, while bipolar amplification dominates the charge collection process in PMOS.

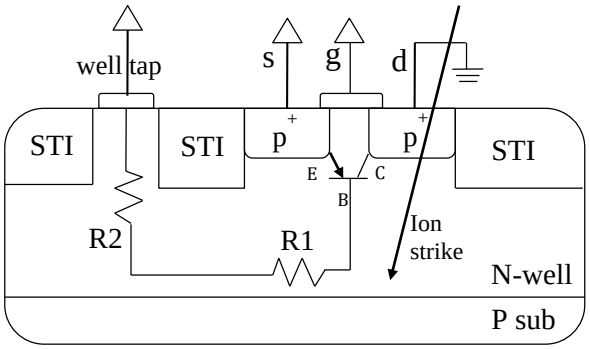


Figure 3.6 Bipolar junction transistor formed in a PMOS device [41]

Therefore, the guard ring surrounding a PMOS transistor helps to maintain the N-well potential, while subsequently mitigating parasitic charge collection.

Another famous isolation technique is referred to as guard drains. This technique was first reported in open literature in 2008 [17], although it had been applied in design projects before that. Guard drains are highly doped diffusion regions implanted close to drains. As the name implies, they are of the same doping type as the drains, forming reverse biased diodes to act as alternative charge collection regions, as illustrated in **Figure 3.7**.

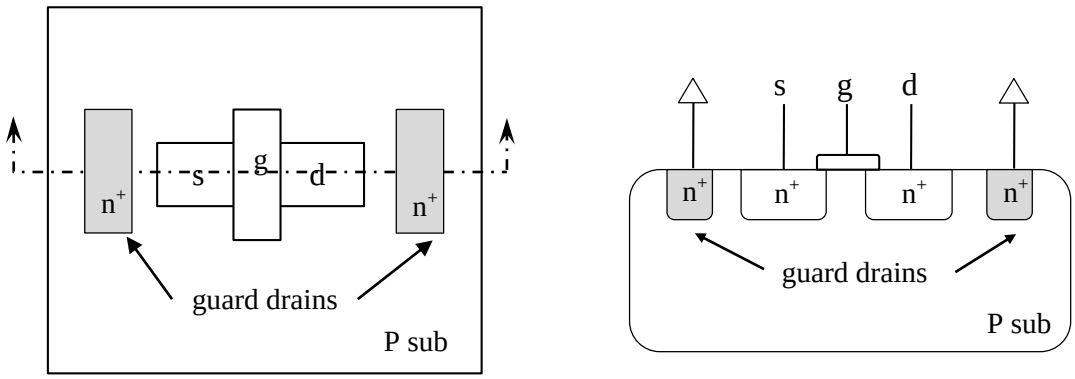


Figure 3.7 Top and cross-section views of an NMOS with guard drains

Guard drains compete with the hit drains by collecting some of the charge that would otherwise be collected by the drains. Therefore, this technique is designed at reduce drift and diffusion charge collection. In other words, guard drains work better for NMOS devices.

The areas of guard ring and guard drain layouts are found to be similar for different cells, with approximately15% more area than the conventional layout. According to experiment results, the maximum SET pulse width, which is proportional to the maximum collected charge, is reduced by 20% in the guard ring circuit as compared to conventional layout circuit. In addition, the guard ring circuit demonstrates a 42% reduction in SET cross-section compared to the conventional one. On the other hand, the cross-section of the guard drain circuit is 30% to 40% lower than that of the guard ring circuit.

3.2.2 Soft Error Immune Latch

A rad-hardened latch design scheme was proposed in 2010 by researchers in [16]. The design is based on an interlocked storage structure, as depicted in **Figure 3.8**. Two major techniques are applied to further reduce SER: dual clock buffer (DCB) and double height cell (DHC).

Local clock buffers in a latch are usually small in size, and thus sensitive to SEUs. In the design, the clock buffers are duplicated and placed apart from each other. By doing so, a particle strike on one clock buffer will only cause a single node change in the interlocked structure Similar to DICE, an SEU will only propagate to the output if two of the four nodes are changed at the same time. Therefore, the DCB technique decreases the possibility of soft errors on a local clock buffer.

Apart from hardening the internal clock, the latch is also designed in a double height manner, ensuring that, if two critical nodes are to be hit simultaneously, the "cancelling area" will be hit as well, which can offset the upset. If a particle strike hits at the same time as the drains of a PMOS and an NMOS, which are connected to the same node, the resulting upset will be suppressed. Such drain areas are referred to as cancelling areas. As illustrated in **Figure 3.9**, if a multiple node upset occurs on critical area 1 and 2, deposited charge will be collected by the cancelling area as well. Considering the fact that the cancelling area and critical area collect the opposite charge, the SET current is neutralized, given that these two areas are connected to the same node.

A transforming example from conventional layout to DHC layout is depicted in **Figure 3.10**. Assume *P1* and *P3* are two critical nodes and that *N1* is the cancelling area of *P3*. In the DHC layout, *P1* and *P3* are separated into different rows, with *N1* placed in between. Because of the well separation between critical nodes, this design style subsequently reduces the possibility of MBU triggered by well potential collapse.

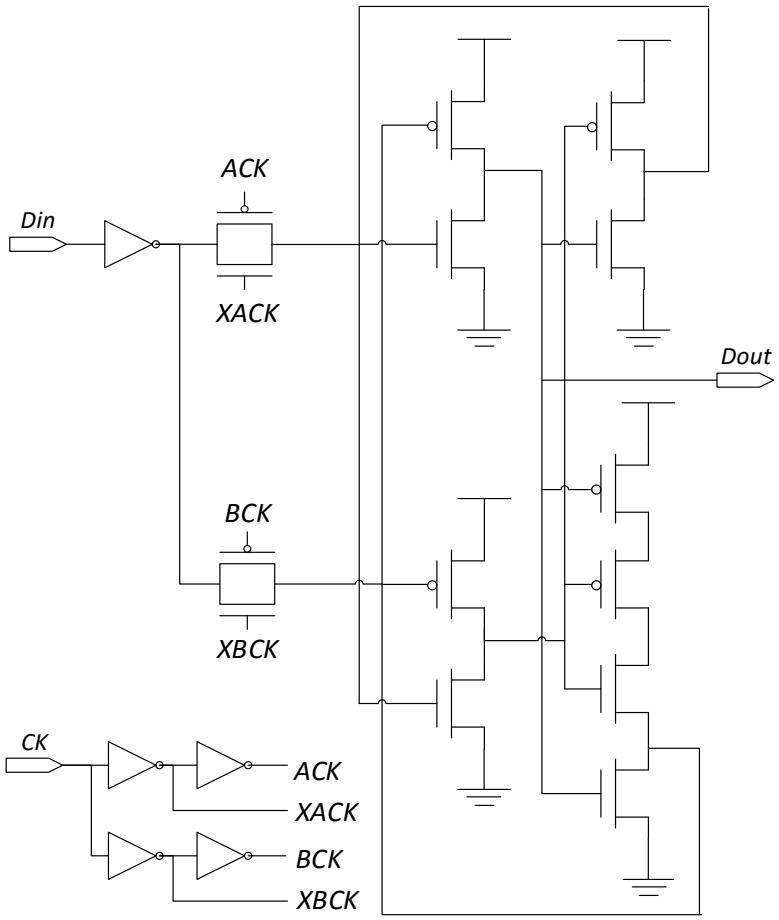


Figure 3.8 SEILA schematic [16]

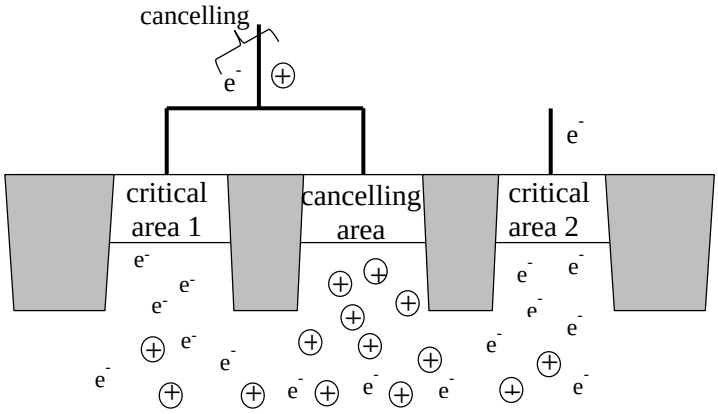


Figure 3.9 Cancelling area between two critical areas [16]

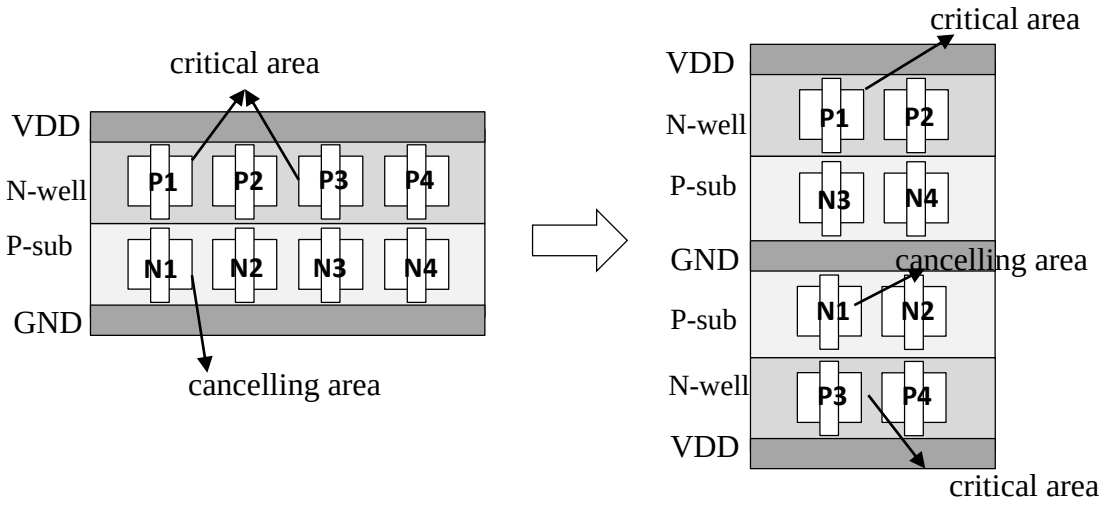


Figure 3.10 A conventional layout transformed to DHC layout

Two SEILA structures are implemented in this research, either with or without DHC. Compared to the conventional latch, the latch without DHC achieves 90% SEU reduction, while the full SEILA latch with DHC protects 99.3% of SEU.

3.2.3 Layout Design through Error-aware Transistor Positioning

Another soft-error-resilient layout design referred to as LEAP-DICE was reported in [18]. LEAP-DICE is based on the DICE circuit structure, utilizing special transistor positioning techniques to reinforce its resilience to MBUs.

As previously discussed, a particle strike on a node that is connected to drains of both a PMOS and an NMOS can result in partially (if not fully) cancelled SET current at the node. This principle is exerted in LEAP-DICE as well, in which PMOS and NMOS transistors are horizontally aligned to reduce charge collection at the output node, as displayed in **Figure 3.11**. To maximize the charge cancellation, LEAP applies this technique to multiple nodes in DICE through positioning transistors by the following rule: for any two transistors *T1* and *T2* that are simultaneously "off", the drain contact node of an "on" transistor *T3* is placed between their drain contacts. In this respect,

the three of them are in a horizontal line and the drain of either *T1* or *T2* is directly connected to that of *T3* [18].

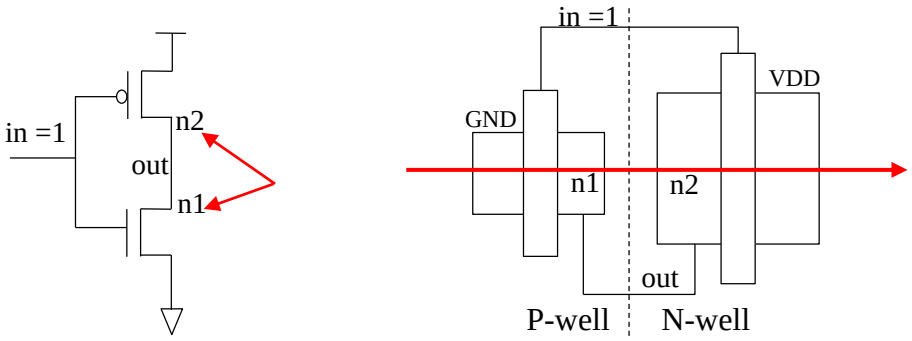


Figure 3.11 LEAP principle illustrated with an inverter [18]

The LEAP-DICE layout of the DICE structure in **Figure 3.2** is depicted in **Figure 3.12**. As can be observed from the figure, any three adjacent drain contacts follow the above-mentioned positioning rule. In each cell there are six such triples in total: {*nn3, nn4, np4*}, {*nn4, np4, np1*}, {*np4, np1, nn1*}, {*np1, nn1, nn2*}, {*nn1, nn2, np2*}, {*nn2, np2, np3*}. For any of the triples, the second drain contact is directly connected to either the first or the third. Moreover, when the first and third drains are “off”, the second one is always “on”. In order to trigger an MBU, the first and third drains must be hit simultaneously, in which case the second drain in-between is inevitably hit as well. Thus, the charge collection is notably reduced.

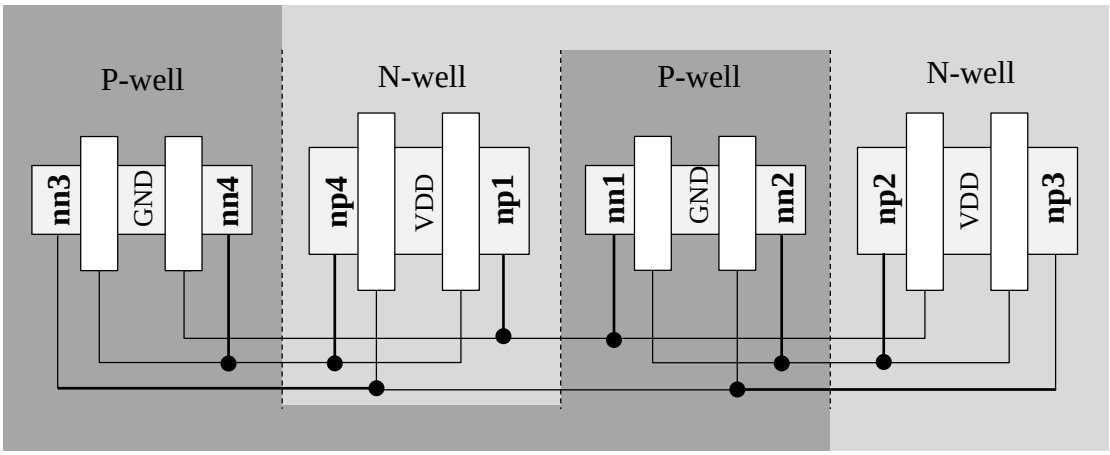


Figure 3.12 LEAP-DICE cell layout [18]

The LEAP-DICE in [18] is fabricated in an 180 nm process. Radiation experiment results indicate 5X fewer errors on average, as compared to the conventional DICE layout, and around 2,000X fewer errors compared to the conventional D flip-flop. Because of the lateral positioning, however, LEAP-DICE costs 1.4X the area of the reference DICE layout.

Recent research outlined in [42] examines LEAP performance in 28 nm bulk technology. Three different LEAP-DICE layouts are analyzed in the study, all of which have a similar, or even smaller, area than the baseline DICE. According to the experiment results, LEAP design achieves dramatic SER reduction in ultra-deep submicron technology. Compared to the conventional DICE, SER reduction of LEAP-DICE rises by two orders of magnitude.

3.2.4 Pulse Quenching

The concept of pulse quenching was first introduced in [43] to describe the single-event mechanism that limits pulse width at high LET. The schematic of two invers in a chain in **Figure 3.13** explains the finding. Assume a HIGH input at the first inverter, and an ion strike hits the drain of the "off" transistor *P1*. The charge collected by *P1* drives *OUT1* HIGH, resulting in a consequential SET pulse at *OUT1*. The positive SET pulse propagates through the second transistor

and generates a negative pulse at *OUT2*. On the other hand, the SET pulse at *OUT1* temporarily turns off *P2*, rendering it susceptible to charge collection. Charge from the strike can easily diffuse to *P2* when it is in close proximity to *P1*. The charge collected by *P2* triggers a LOW-to-HIGH transition at *OUT2*, which in turn resets the voltage of *OUT2* to its original HIGH state. In consequence, the pulse at *OUT2* is effectively truncated, or quenched.

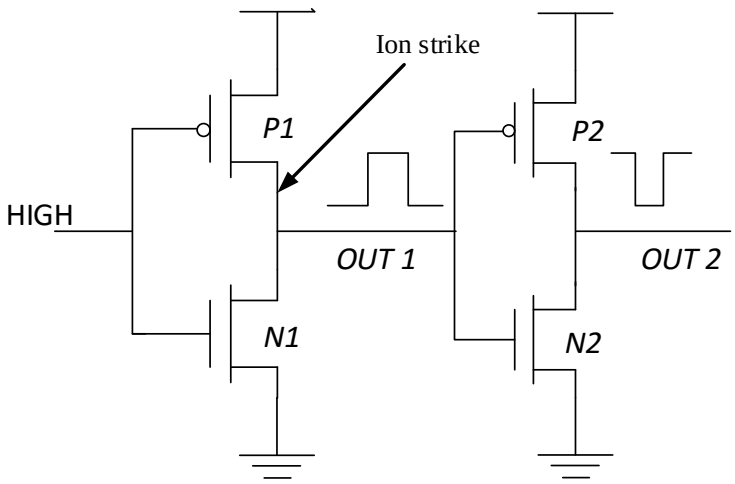


Figure 3.13 SET pulse propagating through two inverters

The reduction in pulse width depends on the time differential between the arrival of propagated SET pulse and the collection of shared charge that occurs after. Experiments demonstrate that pulse quenching is more effective in advanced technologies and with angled single event strike [43].

The study in [44] further investigates the pulse quenching effect, presenting an SET mitigation technique in layout by promoting pulse quenching in combinational logic. This study exploits pulse quenching between transistors inside a logic cell, such as an OR gate or more complex compound gates, in order to improve SET tolerance.

To illustrate the technique used in [44] , the schematic of a two-input OR gate is demonstrated in **Figure 3.14**. The N-well portion of its layout is shown in **Figure 3.15**, where *W*, *X* and *Y* represent the corresponding nodes in the schematic. In a conventional layout (a), the distance

between *X* and *Y* renders it difficult for charge sharing to occur. The pulse quenching effect is influenced strongly by the strike location and incident angle, considering the fact that node *Y* must collect enough charge from *X* to restore its initial state and prune the SET pulse. According to the study, in 90 nm technology, a 10 MeV*cm^2/mg normal-incidence strike at node *X* can result in an SET pulse that propagates to the next gate.

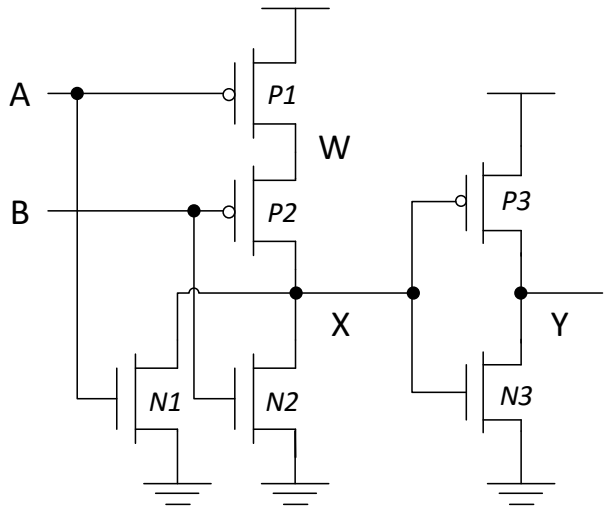
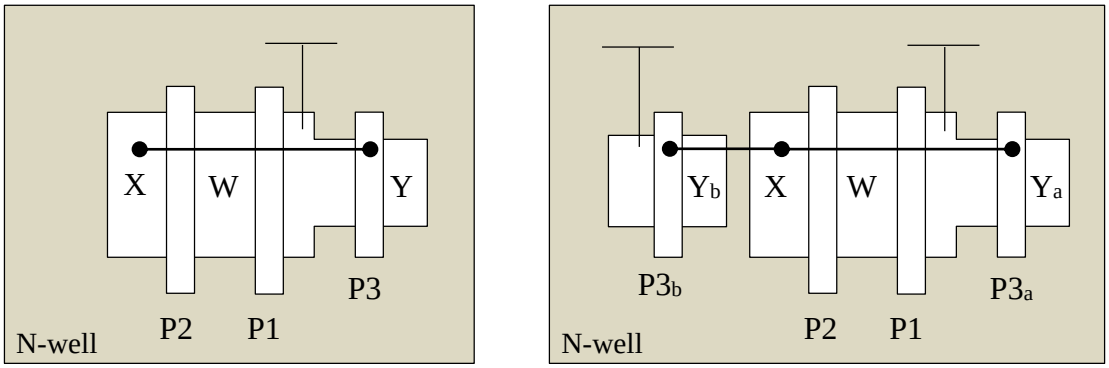


Figure 3.14 Schematic of a two-input OR gate



(a) Conventional layout (b) Layout via pulse quenching

Figure 3.15 Layouts of N-well portion of a two-input OR gate [44]

Figure 3.15 (b) illustrates the OR gate layout using the technique proposed in [44]. The only difference between the OR gate layout and the conventional layout is transistor $P3_b$, which is a duplicate of transistor $P3_a$, and is placed to the left of *P2*. The gate of $P3_b$ is connected to that of

$P3_a$, making the two transistors connected in parallel. Such placement benefits pulse quenching by enhancing charge sharing between nodes *X* and *Y* from both directions. TCAD simulation concludes that this layout renders the gate immune to ion strike with LET of 10 MeV*cm^2/mg at any strike location in or near the gate (i.e., the SET pulse is completely quenched). The distance from $P3_b$ to node *X* plays a crucial part in the pulse quenching effect. To achieve full quenching, transistor $P3_b$ is positioned with minimal spacing (140 nm in a 90 nm process) from node Y_b to node *X*.

The tradeoffs in this design scheme are area and power dissipation. The additional PMOS in the example OR gate increases the N-well area by nearly 40%. In devices whose total area is much larger than the additional part, the area penalty will be somewhat reduced. The additional transistor also introduces extra capacitance on node *X*, which in turn increases power dissipation.

3.2.5 Drain/Source Extension

As we know, the parasitic bipolar effect is the main cause of SET in PMOS devices. Because the bipolar transistor is formed by forward-biased PN junction between P+ source and N-well, source diffusion plays a detrimental role in PMOS SET mitigation. In NMOS devices, on the other hand, SET-induced electrons and holes can easily disperse from the P-well into the substrate due to the absence of PN junction between the P-sub and N-well as in a PMOS. According to TCAD simulation findings in [45], source plays a beneficial role in NMOS SET mitigation by absorbing electrons that will otherwise be collected at the drain. The mechanism is described as follows:

After an ion strike at the drain, electrons and holes are generated along the ion track. Some electrons are collected by the drain, creating an SET pulse at the node. The collapse of drain potential temporarily forward-biases the PN junction between P-well and N+ drain. Considering the fact that holes in the P-well can easily diffuse into P-substrate, even though P-well potential

slightly increases, the PN junction between P-well and N+ source remains reversed-biased. TCAD simulation confirms that, following ion strike, an electron current is injected from P-well into source, while no hole current flows from P-well to source. The electrostatic potential indicates that the parasitic BJT is in the forward-active region, where the drain acts as the emitter, the P-well as the base, and the source as the collector, as depicted in **Figure 3.16**. Therefore, on the contrary to PMOS, an NMOS source helps reduce the amount of electrons collected by the drain during particle strike.

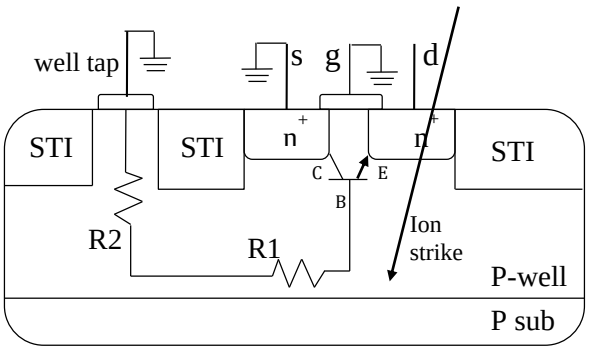


Figure 3.16 Forward-active parasitic BJT in an NMOS

Based on the above mentioned mechanism, [45] proposes a layout technique to mitigate SET in NMOS devices by adding an extended source region beside the sensitive drain. The implementation of source extension technique can be divided into three different categories, according to the original layout. If only one gate is between drain and source, a double-finger structure can be used instead, as demonstrated in **Figure 3.17** (a). In a double-finger structure, the drain is surrounded by source regions on both sides, which reduces the drain's area by half, lowering the possibility of particle hit. In cases where the drain width cannot be further cut by half due to process restrictions, an additional source region can be placed on the other side of the drain. The source region is separated from the drain by an additional gate that is tied to ground. This structure can also be used when there is more than one gate between the source and the target drain,

as in **Figure 3.17** (b). When the drain is in the centre of the layout, a combination of the above mentioned techniques can be used, as in **Figure 3.17** (c).

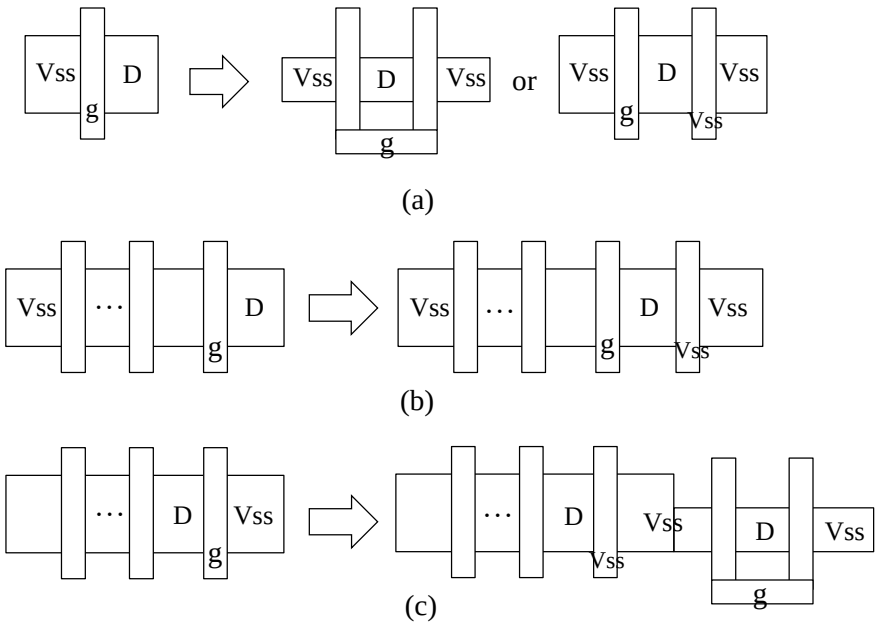


Figure 3.17 Different source extension applications in NMOS layout [45]

The additional source does not have to connect to ground. It can be connected to *VDD* as well, and is referred to in the paper as "drain extension". Using the three guidelines, drain/source extension techniques can be applied to almost any combinational logic cells. For common standard library cells, such as INV, NAND2, and AOI21, the area penalty is about 30% - 40%. Simulation with 65nm 3D TCAD models indicated that inverters using drain/source extension layout have less SET pulse width compared with those using a guard drain. A reduction of 12.60% or 18.57% in SET pulse width was achieved when the additional source was connected to ground or *VDD*, respectively.

3.3 Review Summary

Many rad-hardening approaches have been developed over the past several decades. Techniques on the circuit level often have higher area penalty due to the redundant components,

whereas techniques on the layout level can sometimes be more difficult to implement depending on the physical design limitations of the technology process. In the following chapter, the application of pulse quenching and drain extension techniques on domino logic will be explored, and a new layout-level hardening technique will be proposed and discussed as well.

CHAPTER 4 SEU MITIGATION BY LAYOUT

This chapter will focus on the physical implementation of layout-level hardening techniques. A new layout technique will be proposed and, for comparison purpose, a few previous techniques will be discussed.

4.1 Implementation of Layout Techniques

4.1.1 Conventional Layout of Domino Logic

The operation mechanisms and schematics of domino logics have previously been described in Chapter 2. **Figure 4.1** illustrates a conventional way of sketching a domino buffer layout. Diffusion regions are shared between transistors wherever possible to minimize the total area.

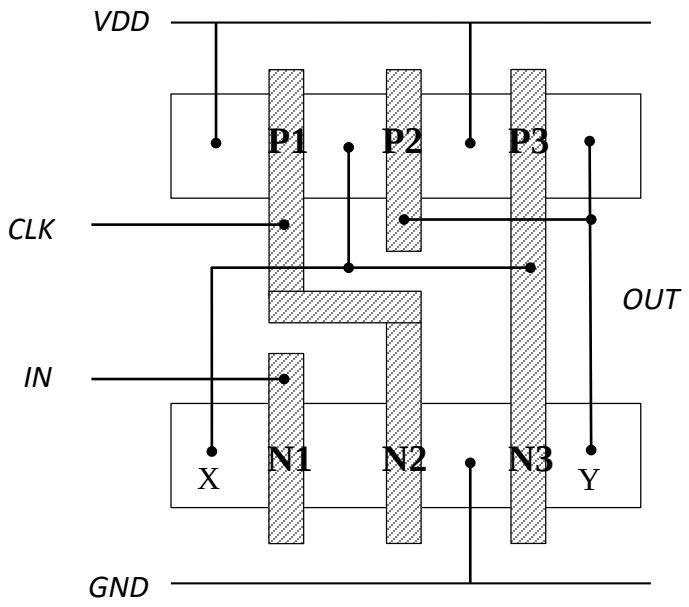


Figure 4.1 Conventional domino buffer layout

As discussed in Chapter 2, due to the periodical precharge-evaluation-precharge operation, dynamic logic is especially vulnerable to N-hit during both precharge and evaluation stages.

Therefore, the predominant objective of this thesis is to harden the critical nodes in NMOS devices, i.e. *X* and *Y* in **Figure 4.1**.

4.1.2 Previous Layout Techniques on Domino Logic

In order to evaluate of the effectiveness of layout RHBD techniques, drain extension and pulse quenching techniques described in [45] and [44] are applied in domino logic as well.

The layout of a domino buffer using drain extension technique is depicted in **Figure 4.2**. As indicated in the picture, an additional diffusion *Z* is added to the left of drain *X* through gate *N0*, which is tied to *GND*, effectively turning off the gate. Diffusion *Z* is connected to *VDD* to promote charge sharing with node *X*. An effective schematic of the circuit is displayed in **Figure 4.3**.

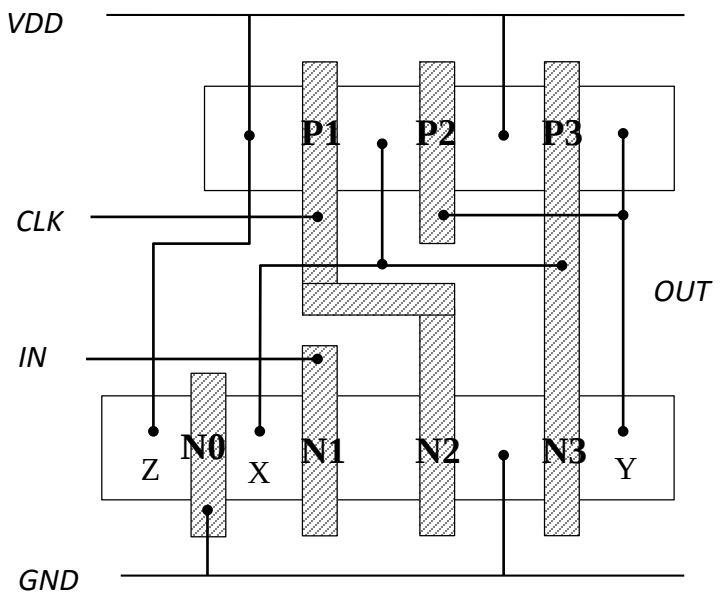


Figure 4.2 Domino buffer layout using drain extension

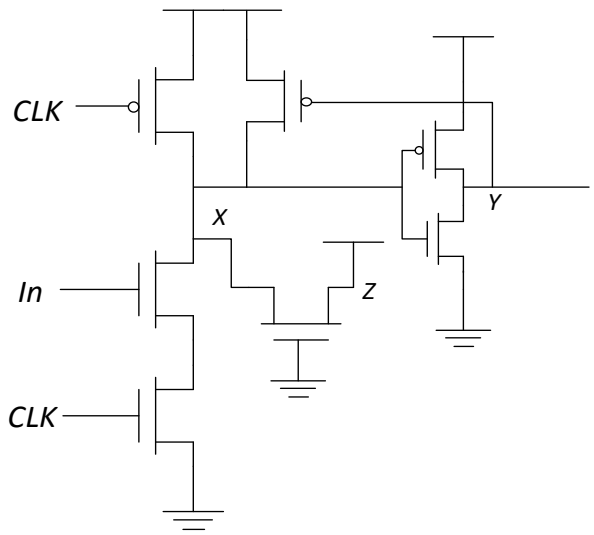


Figure 4.3 Domino buffer effective schematic using drain extension

The layout of a domino buffer with pulse quenching is illustrated in **Figure 4.4**. The non-inverting nature of domino logic (inverting dynamic logic followed by a static inverter) makes it suitable for the pulse quenching technique. Nodes *X* and *Y* always have opposite logic values, rendering charge sharing between them beneficial to SET pulse quenching. Such charge sharing is promoted in the layout by the addition of *N3*'s duplicate *N0* to the left of node *X*. An effective schematic of this implementation is presented in **Figure 4.5**.

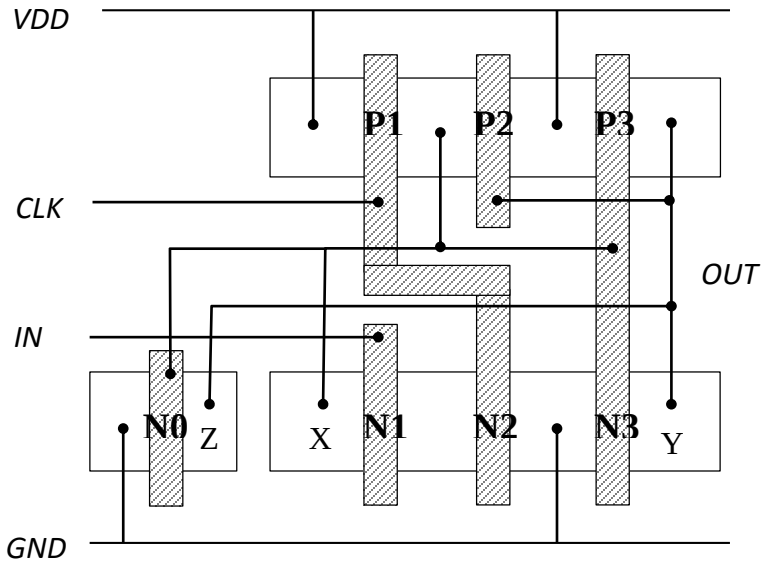


Figure 4.4 Domino buffer layout using pulse quenching

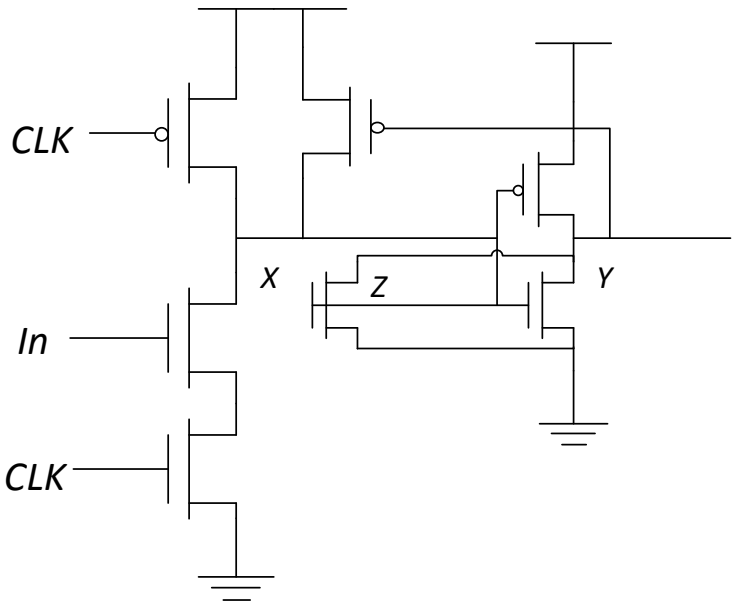


Figure 4.5 Domino buffer effective schematic using pulse quenching

4.1.3 Proposed Layout Technique on Domino Logic

Inspired by the above-mentioned drain extension and pulse quenching techniques, a new layout RHBD technique is proposed in this work. As exhibited in **Figure 4.6**, an additional diffusion region *Z* is added to the left of the drain *X*, similar to that in drain extension implementation. To promote charge sharing between *X* and *Y*, the additional diffusion is connected to *Y*, resembling the duplicated NMOS in the pulse quenching technique. As compared to the pulse quenching technique, however, in which a whole extra transistor is used, in the proposed method, only a diffusion region is added. The extra diffusion region is subsequently separated from the critical node by merely a gate rather than the shallow trench isolation (STI) implemented in the silicon. In this way, not only is the distance between two diffusions largely reduced (gate length vs. minimum active-to-active distance allowed by fabrication process), but the free carriers can subsequently diffuse more easily to the added diffusion without the blockage of STI, which is nominally 0.35 μm deep into the silicon in the IBM CMRF8SF process. The effective schematic of this technique is exhibited in Figure 4.7.

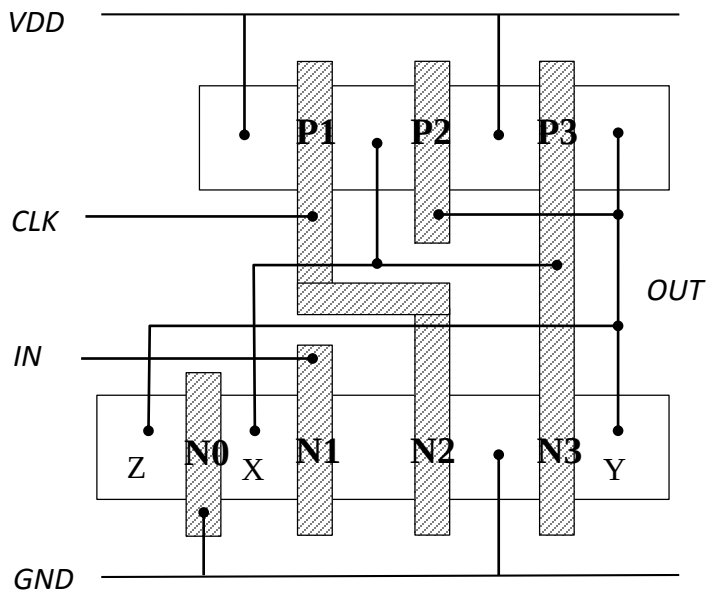


Figure 4.6 Domino buffer layout using proposed method

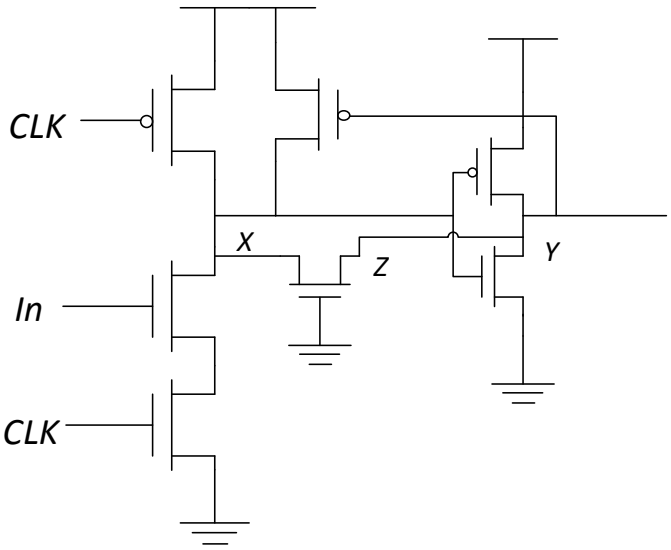


Figure 4.7 Domino buffer effective schematic using proposed method

4.2 3D TCAD modeling and simulation

4.2.1 TCAD models design

Traditional SPICE is not sufficient for single event simulation when considering layout-based techniques. For accurate heavy ion simulation, TCAD models must be used. TCAD tools are able

to perform simulation on semiconductor devices based on customized device structure and doping profiles. To analyze radiation effect on different layout implementations, 3D device models of the 4 layouts (conventional, drain extension, pulse quenching, and proposed method) were built using the Synopsys Sentaurus TCAD tool. Considering the fact that the 4 layouts solely differ in NMOS devices, only the critical NMOS devices were modelled in 3D TCAD. Other devices were instantiated using SPICE models and electrically connected to TCAD models.

All NMOS devices are implemented in cubes with an edge length of 10 μm. The cubes are constructed with silicon and doped with boron based on the doping profile used in previous studies [46] [47]. The doping profiles have been edited to better match the SPICE model in the IBM CMRF8SF 130 nm design kit.

The 3D TCAD structures and 2D cross-section views (cut along X-Z plane at Y=0) of each design are illustrated in the following pictures (drain extension technique uses the same TCAD model as the proposed design, but is electrically connected differently and is, therefore, not listed in the 3D and cross-section views).

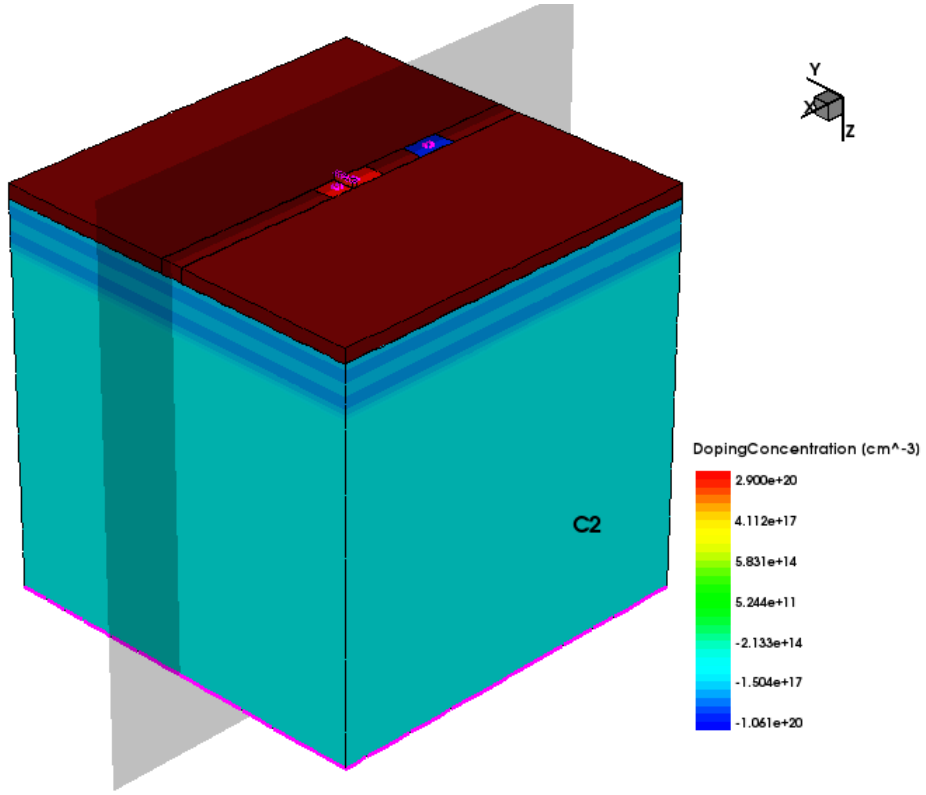


Figure 4.8 3D view of conventional layout

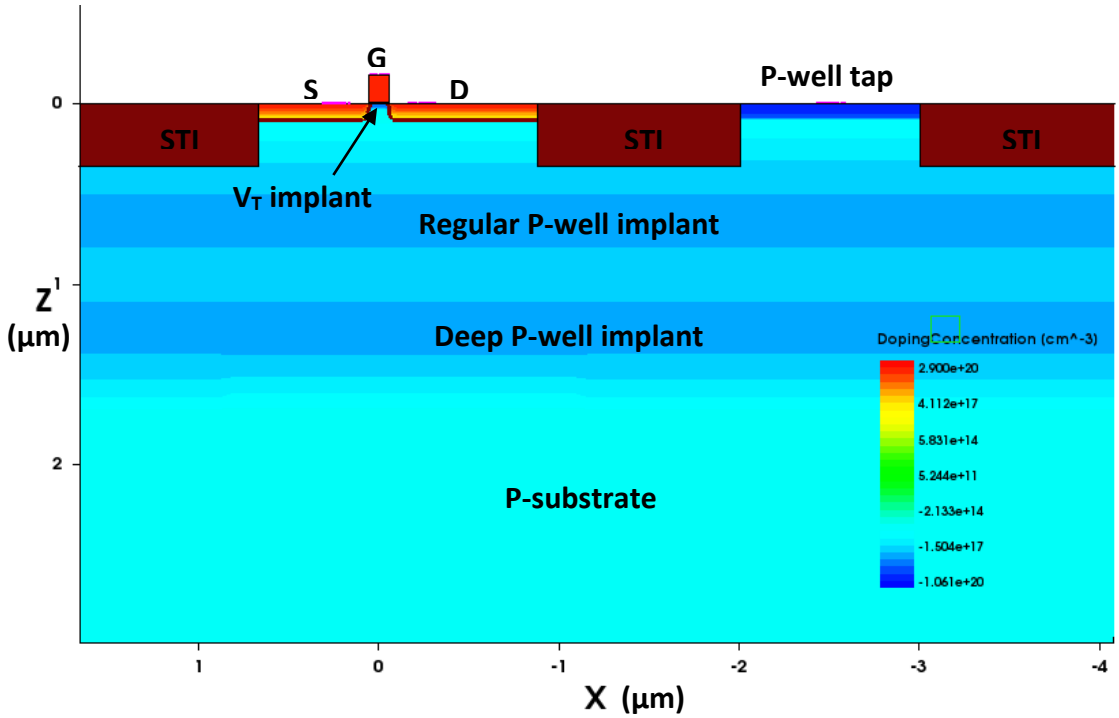


Figure 4.9 Cross-section view of conventional layout

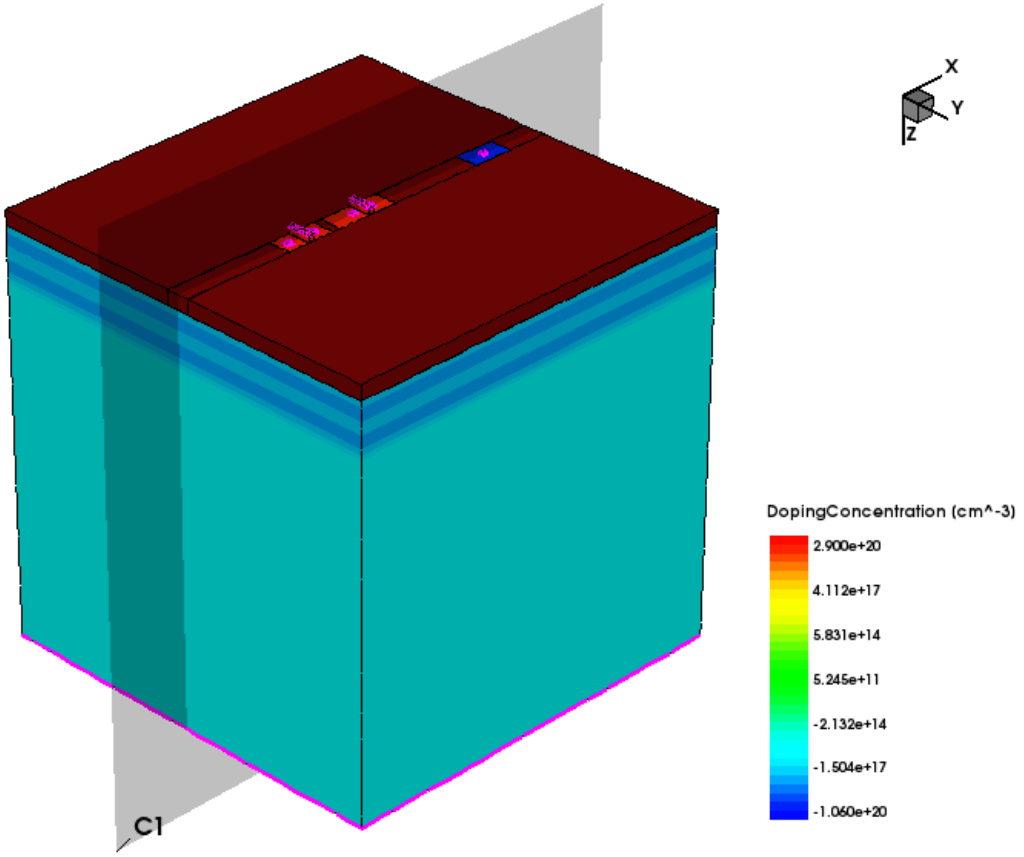


Figure 4.10 3D view of pulse quenching technique

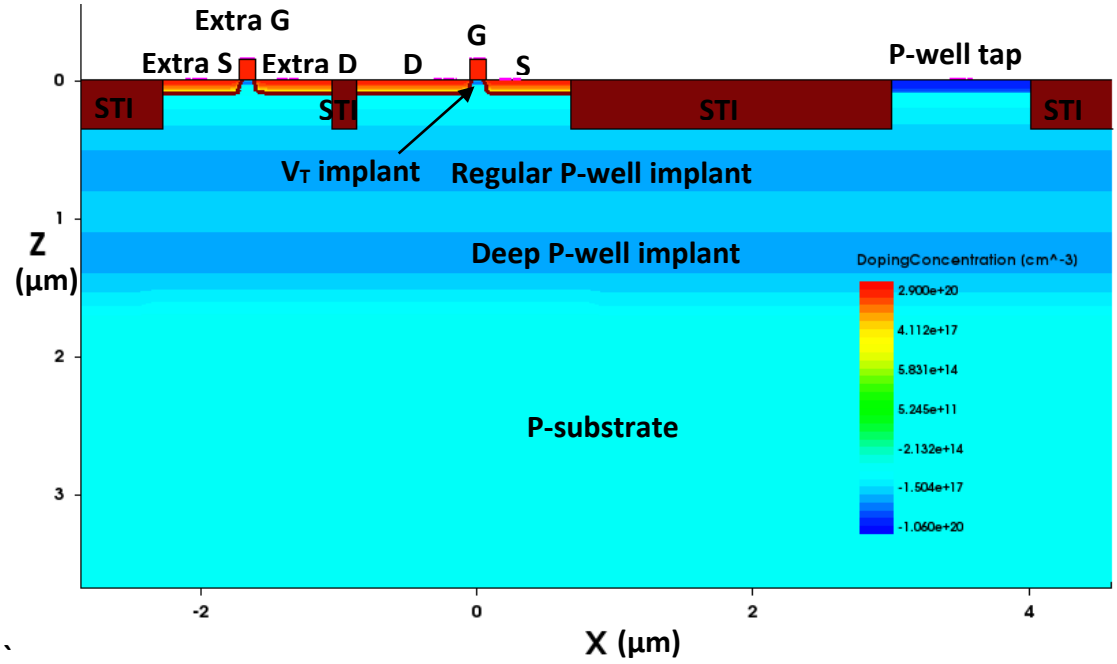


Figure 4.11 Cross-section view of pulse quenching technique

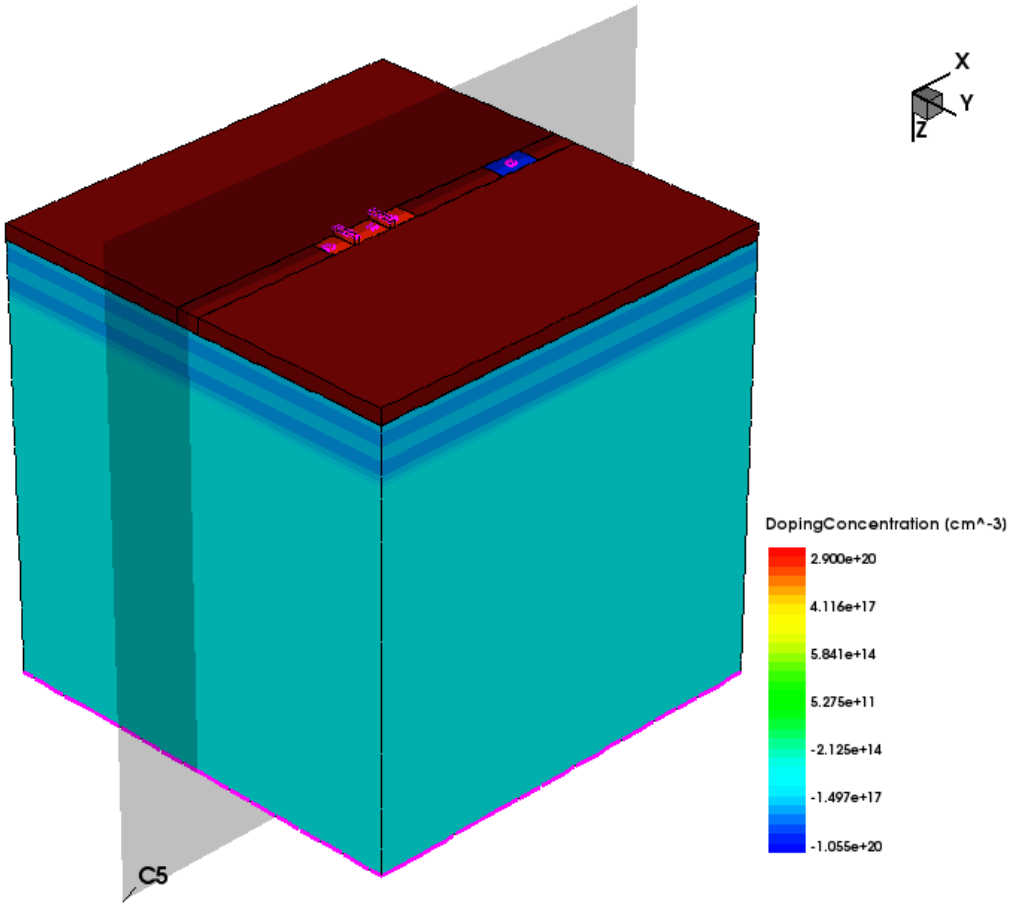


Figure 4.12 3D view of proposed method

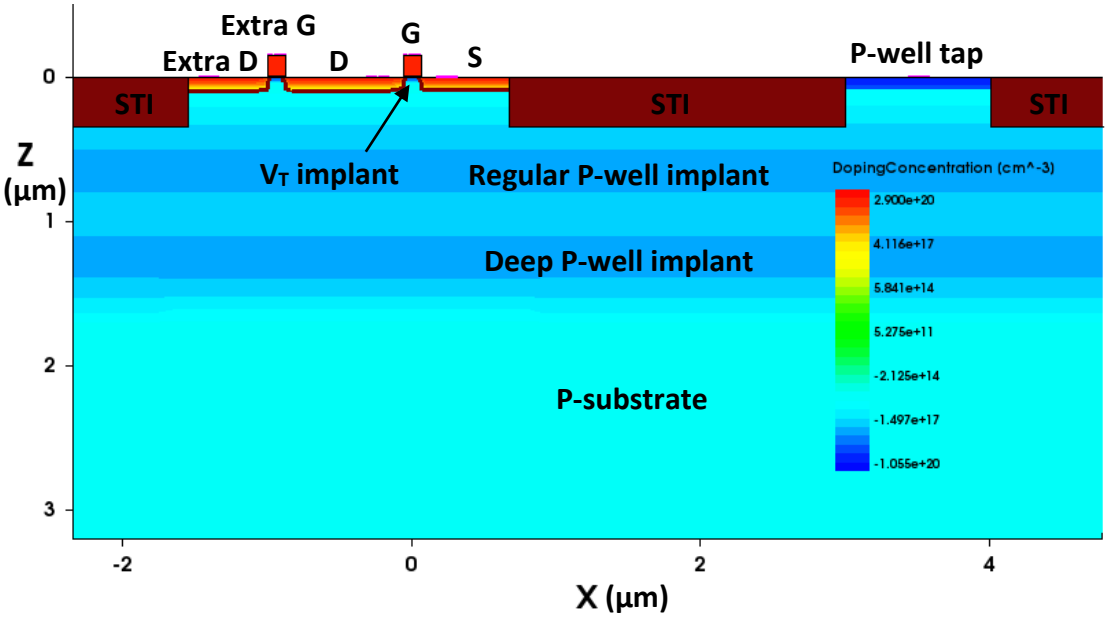


Figure 4.13 Cross-section view of proposed method

4.2.2 TCAD Model Calibration

The NMOS models have been calibrated to match the electrical characteristics of IBM CMRF8SF 130 nm SPICE models. By adjusting the lightly doped drain (LDD) depth, threshold voltage (V_T) implant, and diffusion doping depth of the TCAD NMOS device, reasonable agreement on I_d-V_g and I_d-V_d curves has been obtained between our TCAD model and the IBM process design kit (PDK). The correspondences between the curves are displayed in **Figure 4.14** and **Figure 4.15.** The NMOS devices of both TCAD and IBM PDK have the same size (W/L) of 540 nm/120 nm. The calibrated TCAD model enhances the credibility of the mix-mode simulation results.

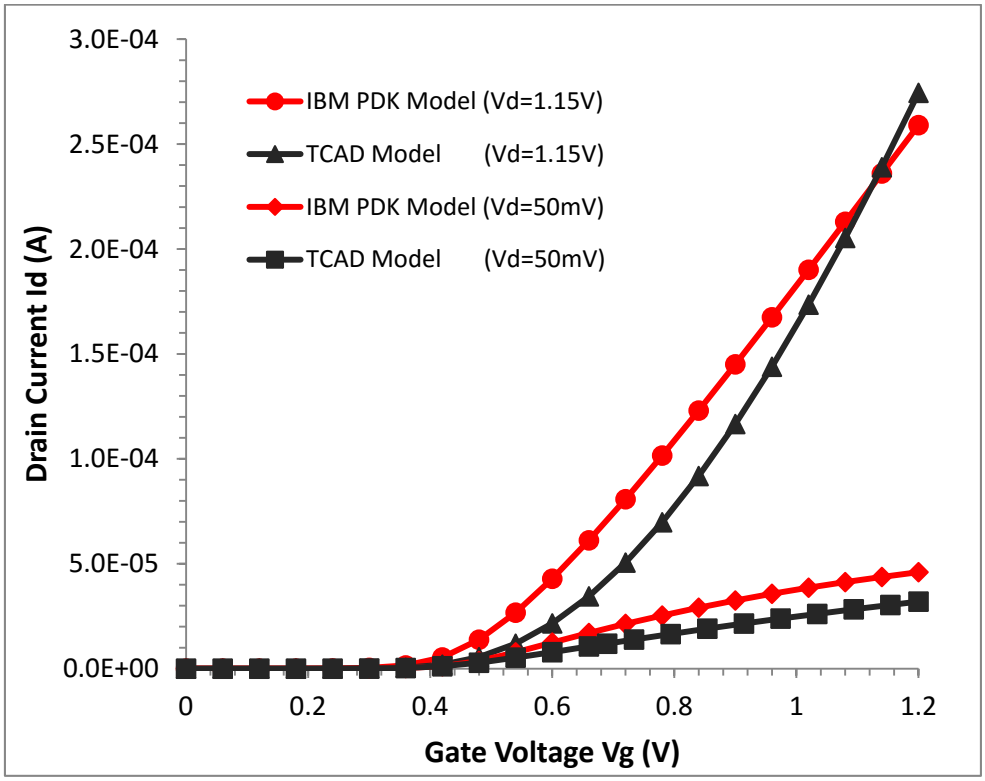


Figure 4.14 NMOS I_d-V_g curve of 3D TCAD model vs. IBM 130 nm PDK model

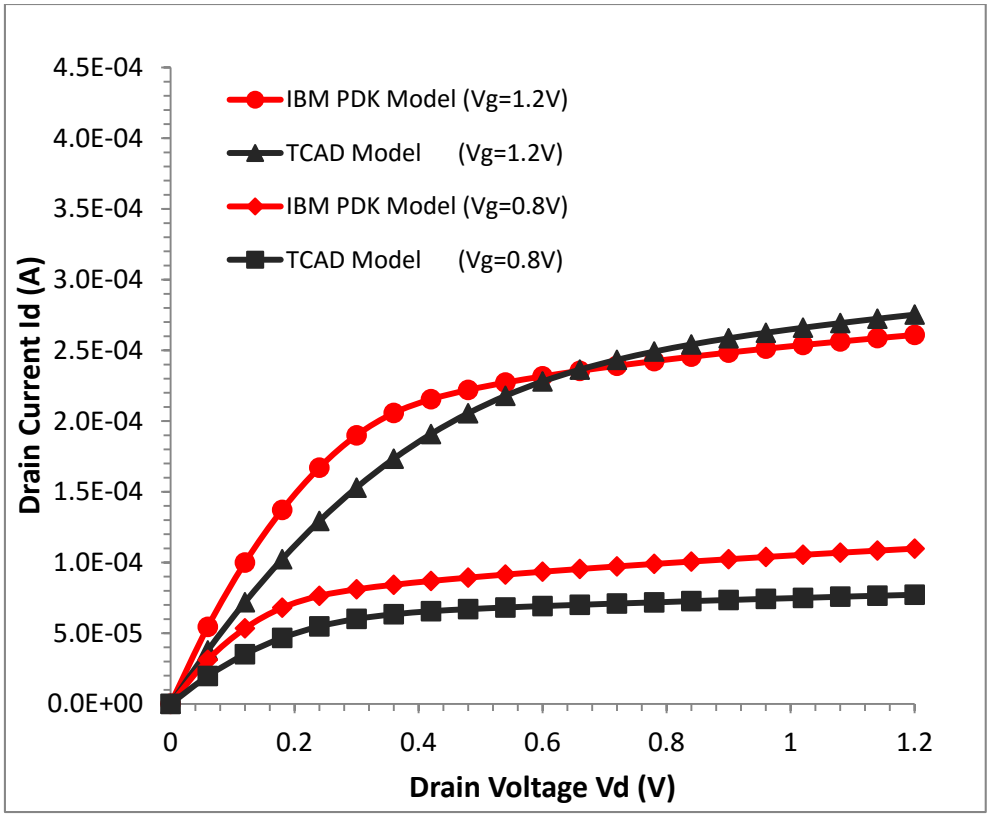


Figure 4.15 NMOS I_d-V_d curve of 3D TCAD model vs. IBM 130 nm PDK model

4.2.3 Mixed-mode Simulation setup

Heavy ion simulations were performed to analyze the single event effect on the devices. The circuit structure depicted in **Figure 4.16** was used: four domino buffers are connected in a chain, with the output of the last one connected to the data input of a D-latch. The latch shares the same clock signal with the buffers. Thus, when *CLK* is low, all buffers are in precharge state and the last state from the buffer chain output is locked up in the latch. When *CLK* is high, the *IN* signal is evaluated by the dynamic logics and transparently passed to the output of the latch. The critical NMOS devices in the first domino buffer uses a 3D TCAD model, while the rest of the circuit use SPICE models from the PDK. Simulations using testbenches that combine TCAD and SPICE models are referred to as a mixed-mode simulation. With most devices in the circuit using SPICE

models, mixed-mode simulation is not only time efficient, but subsequently maintains reasonable accuracy through complete process simulation on the critical components.

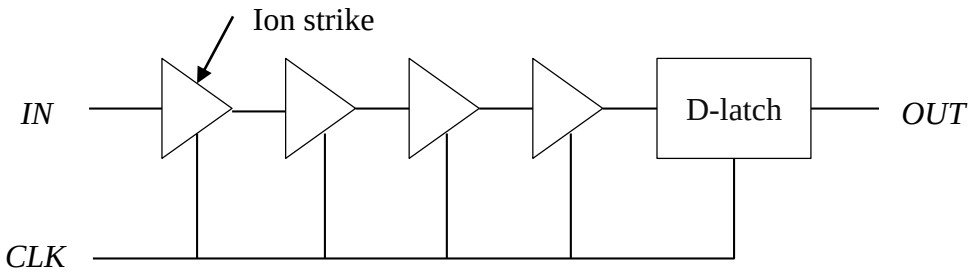


Figure 4.16 Buffer chain circuit used in simulation

In the simulations, heavy ions hit the same location on the sensitive drain contact with different incident angles. Some properties of the simulation and heavy ion settings are listed in **Table 4.1**. Heavy ion simulations were performed during both precharge and evaluation phases. Input to the buffer chain was tied to *GND* and therefore, the pull-down network was not partially charged during precharge. A clock frequency of 100 MHz was used during simulation to allow enough time for SET to settle before the next stage.

Table 4.1 Mixed-mode simulation settings

Parameter	**Value**
Temperature	298 K
VDD voltage	1.2 V
Device size (W/L)	540 nm / 120 nm
Incident angle	Normal or 30 °/75 °towards charge-sharing components
Ion track length	7 μm
Ion track radius	50 nm
Ion LET	1 – 50 MeV*cm^2/mg

As discussed in Chapter 2, ion hit that occurs near the end of a precharge phase has the potential to cause an upset in the next evaluation phase. The precharge SET pulse width determines the probability of such an upset; the wider the SET pulse, the higher the probability of a single event setup. Therefore, during the simulation, ion strike occurs at the beginning of a precharge phase to allow the SET to fully recover during precharge, allowing the complete pulse width to be measured.

For the simulation during evaluation stage, the ion strike occurs at the beginning of the evaluation as well. A particle strike that deposits enough charge to lower the drain voltage below 50% *VDD* will inevitably cause an upset in dynamic logics, as described in Chapter 2. The presence of the charge sharing components may collect some of the deposited charge, and may suppress the upset for a certain period of time through the pulse quenching mechanism.

4.2.4 Simulation Results

1. Precharge phase

Figure 4.17 and **Figure 4.18** illustrate the SET pulse width during a precharge N-hit of different incident angles. As expected, higher LET results in wider pulse width. Under normal incidence, the SET pulse width increases almost linearly with LET for all designs. Drain extension and the proposed design demonstrate approximately 33% pulse width reduction at 28 MeV*cm^2/mg. With a tilted incidence of 30°, approximately 45% reduction is achieved due to increased charge sharing.

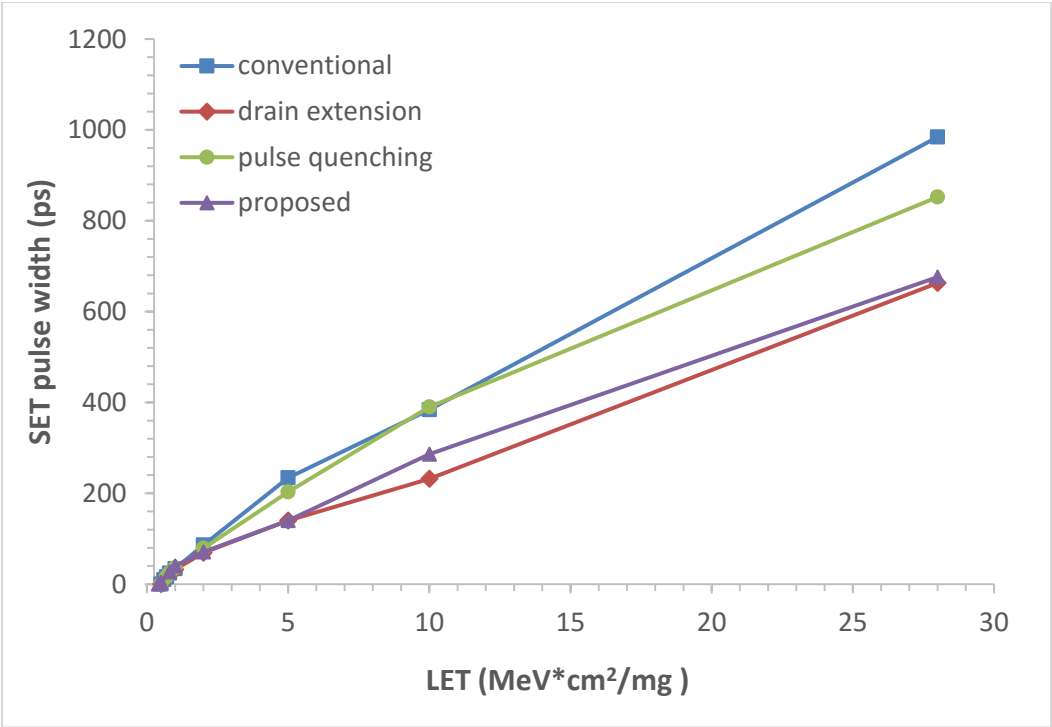


Figure 4.17 Precharge N-hit with normal incidence

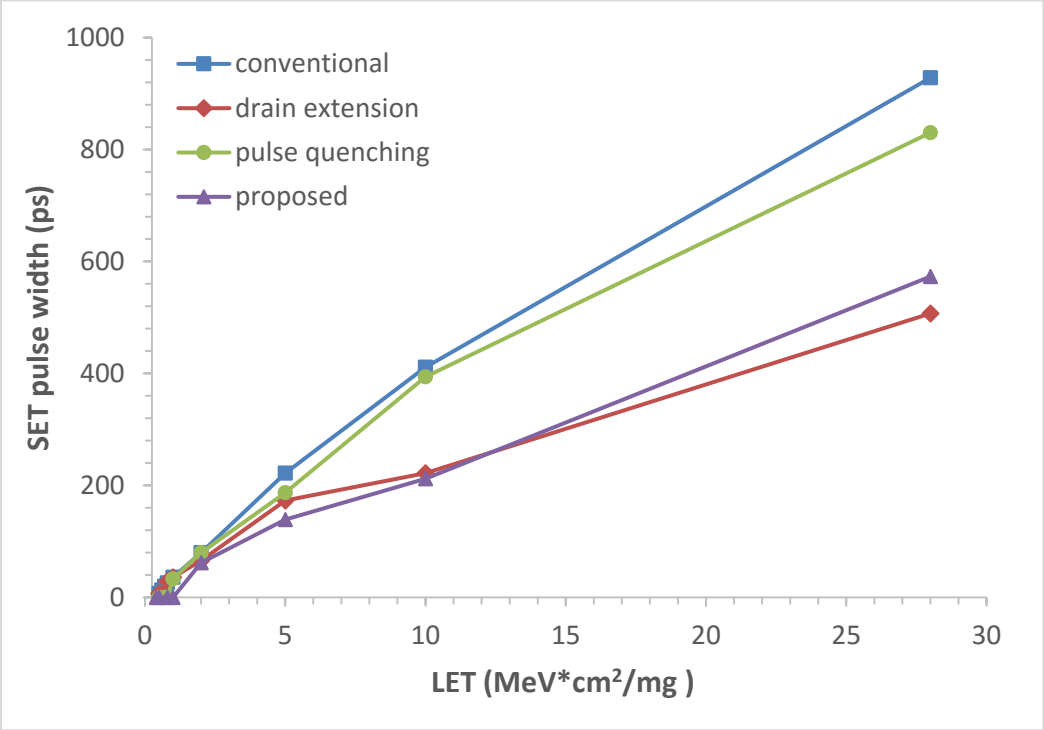


Figure 4.18 Precharge N-hit with 30 °incident angle

2. Evaluation

Figure 4.19 to **Figure 4.21** depict the SET pulse propagation delay (through the logic chain) during an evaluation N-hit. As indicated in the figures, for conventional and drain extension designs, the propagation delay is irrelevant to the particle LET under any incidence angle. However, for the proposed designs, a positive correlation between propagation delay and LET is observed when the incident angle is tilted to 30°. This is due to the pulse quenching effect suppressing the SET pulse from propagating through. Pulse quenching design demonstrates the same correlation starting from a 75° incident angle. The correlation is nearly linear at higher LETs (5 MeV*cm^2/mg and above).

The following definition is used for evaluating the efficacy of SEU mitigation:

$$Upset\ probability = \frac{t_{vulnerable}}{t_{evaluation}} = 1 - \frac{t_{propagation}}{t_{evaulation}} \tag{4.1}$$

The upset probability defined above evaluates how likely it is that, during one clock cycle, an SEU will be captured by the latch when a particle hits the first domino buffer in the buffer chain. Assuming an ideal clock, if an upset occurs within $t_{propagation}$ prior to the end of the evaluation phase, the SET pulse is unable to pass to the latch due to propagation delay. The upset probability for a 30° incident angle at different frequencies is depicted in **Figure 4.22**. As can be observed, the proposed design can substantially reduce the evaluation upset probability under high frequency, high LET, and tilted incidence conditions. Note this conclusion is based on the assumption in the simulation that the input data is constant and that the N-hit only occurs on the first dynamic inverter in the chain.

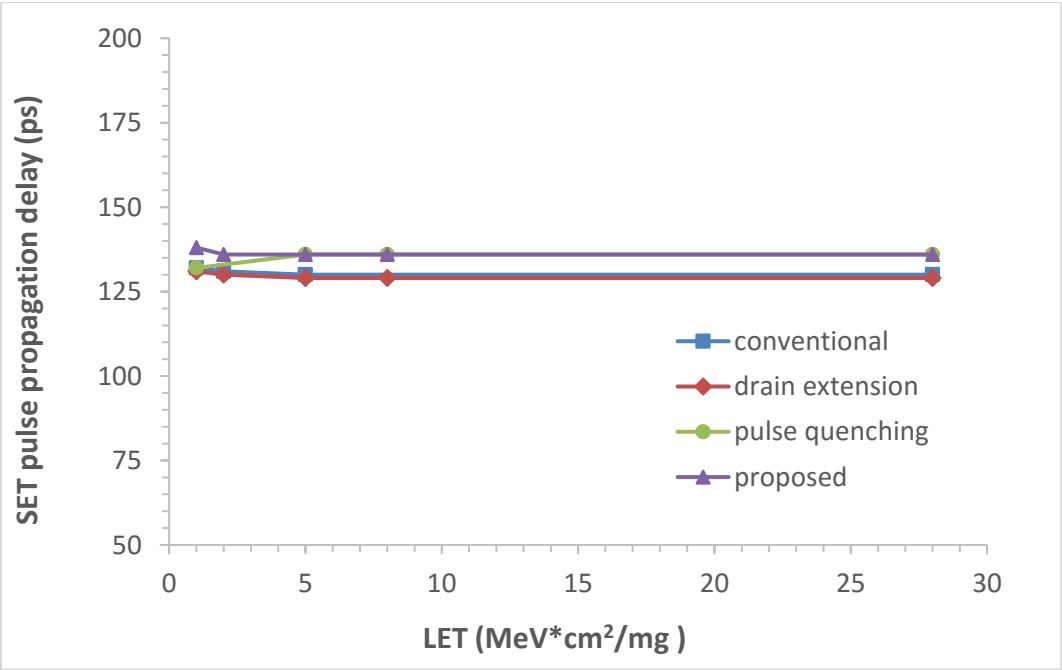


Figure 4.19 Evaluation N-hit with normal incidence

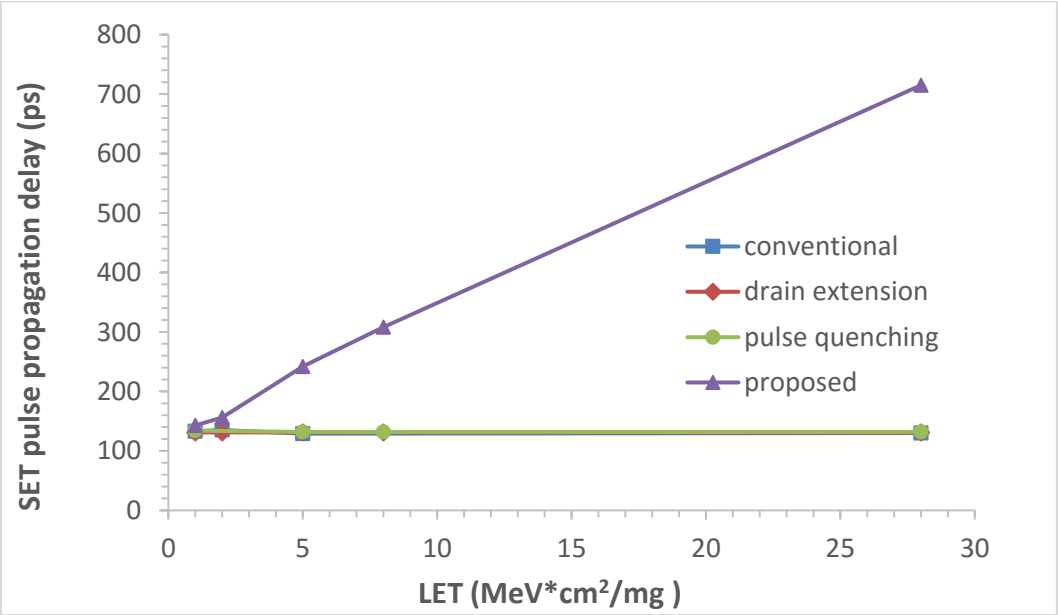


Figure 4.20 Evaluation N-hit with 30 °incident angle

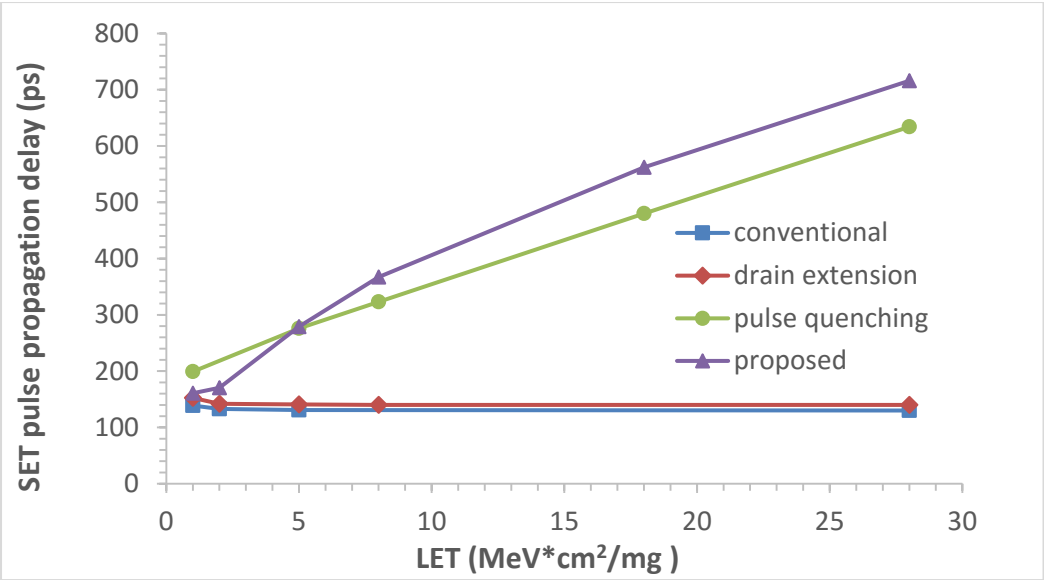


Figure 4.21 Evaluation N-hit with 75 °incident angle

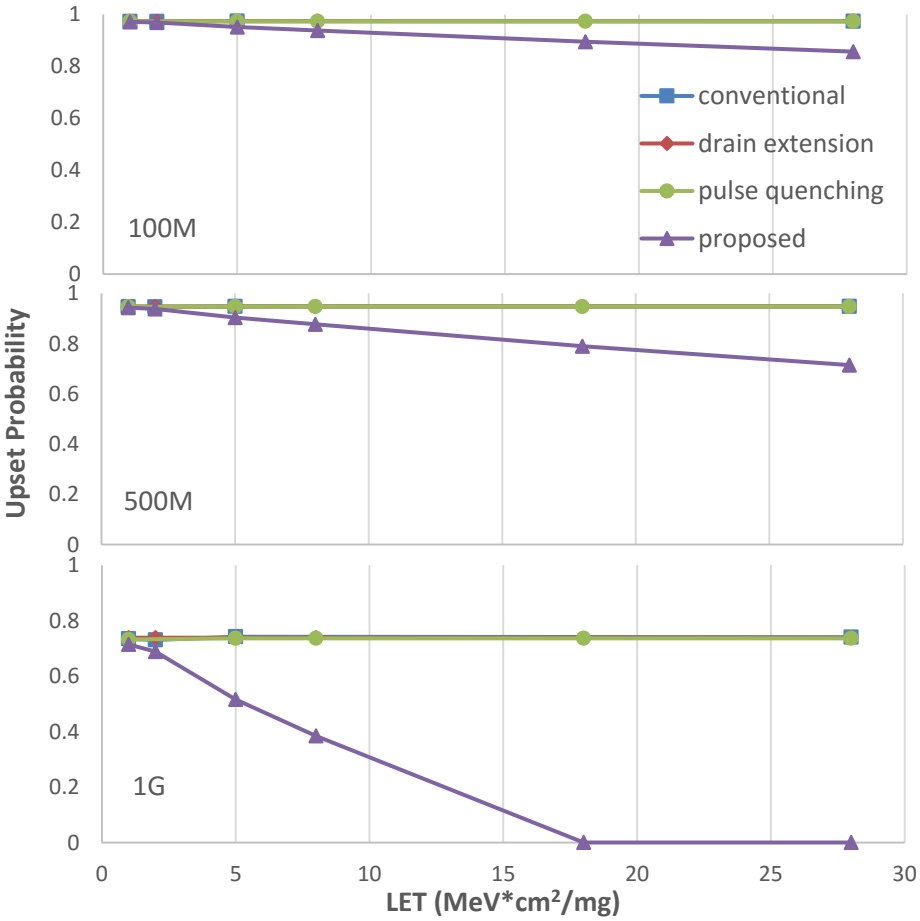


Figure 4.22 Evaluation upset probability at 30 °incident angle

Charge sharing between the hit drain and the pulse-quenching element can be confirmed by **Figure 4.23**. As demonstrated in the picture, immediately after the particle hit at 0.1 ns, the additional (pulse-quenching) drain collects almost ¼ of the total charge collected by the hit drain. After the peak drain current, a large number of ionized electrons flow through the additional drain.

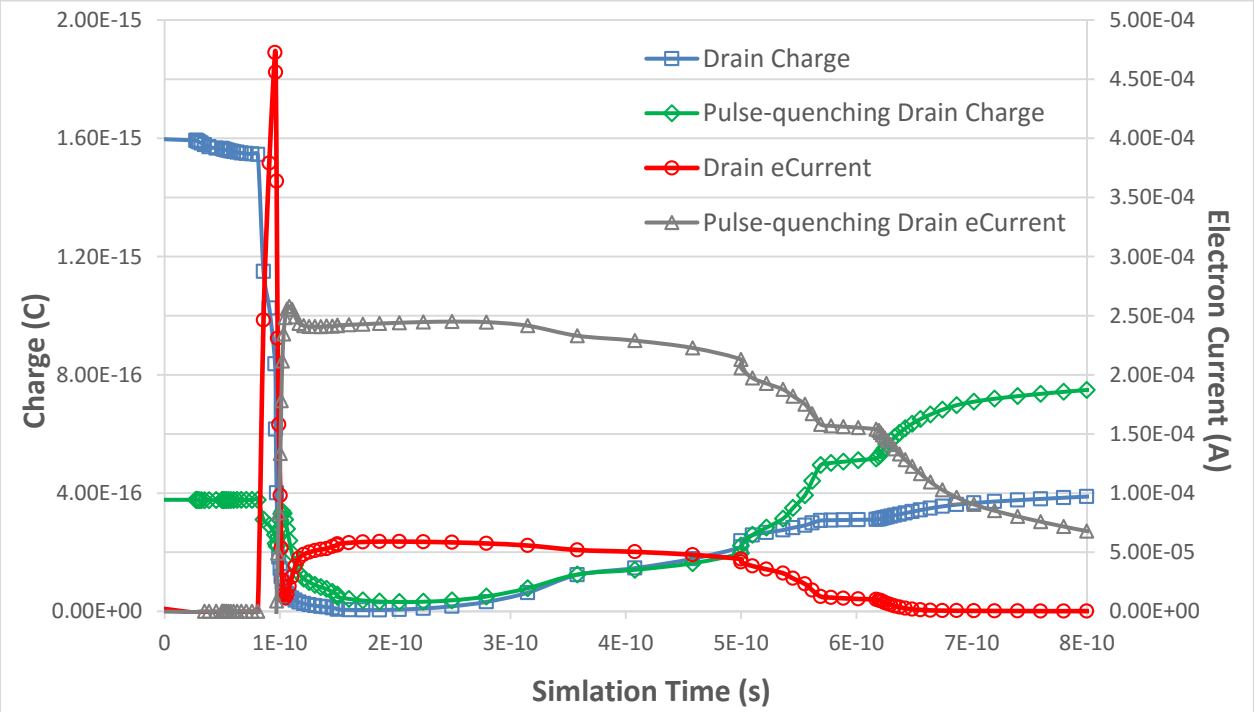


Figure 4.23 Proposed design charge and electron current at 30 °incidence of 28 MeV*cm^2/mg particle LET

CHAPTER 5 TEST CHIP DESIGN

A test chip using IBM CMRF8SF 130 nm process has been designed and fabricated for the purpose of radiation experiments. Due to limited electric design automation (EDA) tool resources, physical placement and routing of all core and IO cells, clock distribution network and power grid were performed manually. This chapter will describe the details inherent to the test chip design.

5.1 Inverter and Flip-flop Chains

Four domino buffer chains using different layout schemes were implemented in the chip: proposed technique, drain extension, pulse quenching, and the conventional layout as the baseline. Akin to the mixed-mode simulation setup, the block structure of 4 domino buffers followed by a DICE flip-flop was used in each chain. DICE flip-flops were used to minimize possible soft errors on the registers. Each buffer chain contained a total of 432 (6 rows by 72 columns) domino buffers, with 4 μm between any two to ensure that inter-cell charge sharing was eliminated. Transistors within each cell were placed with minimum space in-between, as allowed by PDK. The areas of the sensitive drain were kept constant across all designs for equal chance of particle hit. All cells in the chip had the same height of 12-track (4.8 μm). The detailed schematics, along with the transistor sizes of the domino buffer and DICE flip-flop, are displayed in **Figure 5.1** and **Figure 5.2**.

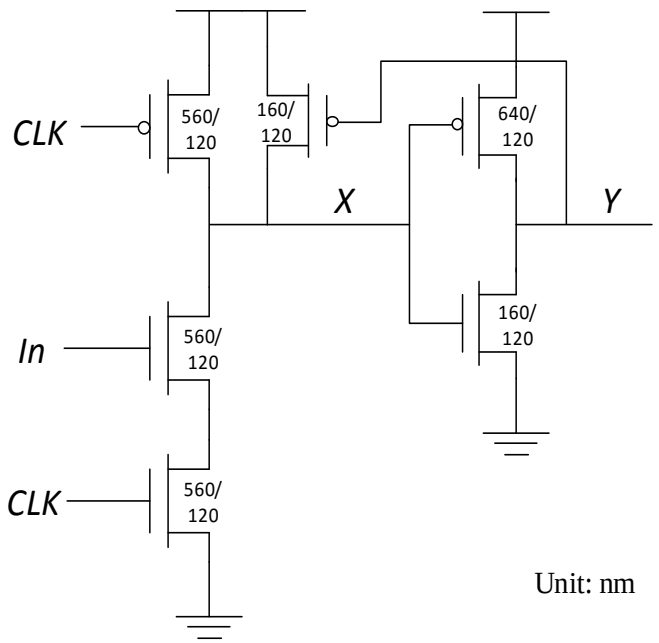


Figure 5.1 Schematic of domino buffer with transistor sizing

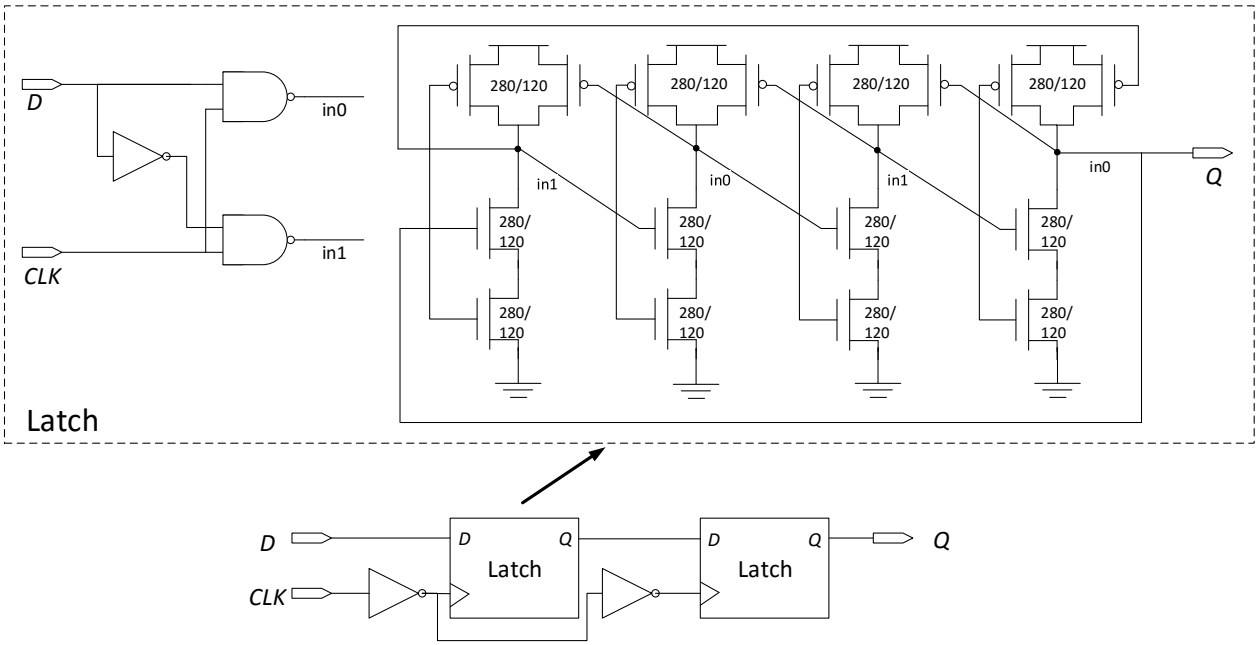


Figure 5.2 Schematic of DICE flip-flop with transistor sizing

5.2 Clock Distribution Network

A reverse clock distribution network was employed in the test chip. In the reverse clocking technique, clock signal is applied in the reverse direction with respect to data flow, ensuing that the risk for hold time violation is reduced.

As depicted in **Figure 5.3**, the positive clock edge of capturing flop *FF2* arrives earlier than that of launching flop *FF1*. Assuming clock-to-Q delay t_{c2q} in *FF1*, hold time t_{hold} in *FF2*, local clock skew of t_{skew}, and contamination (best-case) logic delay of t_{cd}, in order to avoid hold time violation, the following needs to be met:

$$t_{c2q} + t_{cd} + t_{skew} \geq t_{hold} \tag{5.1}$$

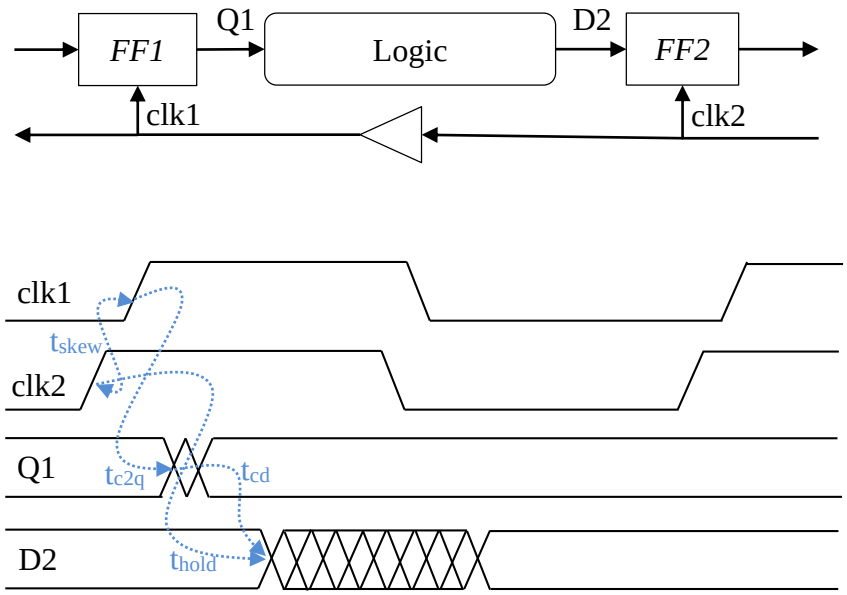


Figure 5.3 Flip-flop hold time constraint

Unlike setup time failures that can be bypassed by lowering frequency, if hold time failures are found after fabrication, the chip must be re-designed and re-fabricated. In our designs, the short logic delay between flops poses a potential risk for hold time violations. The presence of useful clock skew from reverse clocking helps to bring down the risk of hold time failures, with the price

of a less balanced clock than an H-type. Moreover, reverse clocking consumes less area than traditional H-type clock tree. This, furthermore, leaves more room for logic cells, given the fact that our chip size is very limited. To reduce the risk of particle hit on clock buffers, large multi-fingered buffers of 40X to 50X were used in the clock network.

5.3 Well Taps, Decoupling Capacitors, and Power Grid

N-well and P-sub taps were used in the chip to maintain well and substrate potentials and prevent latchup. The tap cells are built within each clock buffer as so to meet the design rule for maximum distance between taps.

On-chip decoupling capacitors (decaps) were also added to address power integrity issues. Decaps are capacitors that are placed between power rails to overcome dynamic IR drop due to simultaneous core logic switching. Dynamic IR drop occurs at the active clock edge when sequential elements and dynamic logics are simultaneously switching and the power supply cannot respond instantaneously to the current draw. Decaps act as local energy storage, providing a boost to the power grid when the current demand is high.

Each decap was made from both NMOS and PMOS devices, with its gate connected to *VDD* (for NMOS type) or ground (for PMOS type) and both source and drain connected to ground (for NMOS) or *VDD* (for PMOS), as in **Figure 5.4**. A rule of thumb for decap placement is to place as many as possible (ideally filling up all empty spaces in chip) and to place them in close proximity to switching elements. In this work, decap cells with an effective capacitance of 60 fF each were added into every clock buffer. There were a total of 5,472 decap cells evenly distributed in the chip, contributing an overall capacitance of 0.33 nF.

Estimations for decap allocation requirement were based on available published data and literature. According to [48], for high performance circuits running at 200 MHz frequency and

above, a decap area allocation of as much as 10% of the core area should be sufficient to achieve a power grid voltage drop of less than 10% *VDD*. In this work, decap cells take up a total area of 0.14 mm^2, which is approximately 11% of the core area. In another paper [49], a decap density of 16.2 to 54.0 nF/cm^2 for 130 nm process node is recommended, based on calculated data from International Technology Roadmap for Semiconductors (ITRS) 2001 studies. Our design has a decap density of 26.2 nF/cm^2, which is within the recommended range as well. Therefore, the amount of decap cells in this chip is considered be sufficient to ensure a less than 10% IR drop.

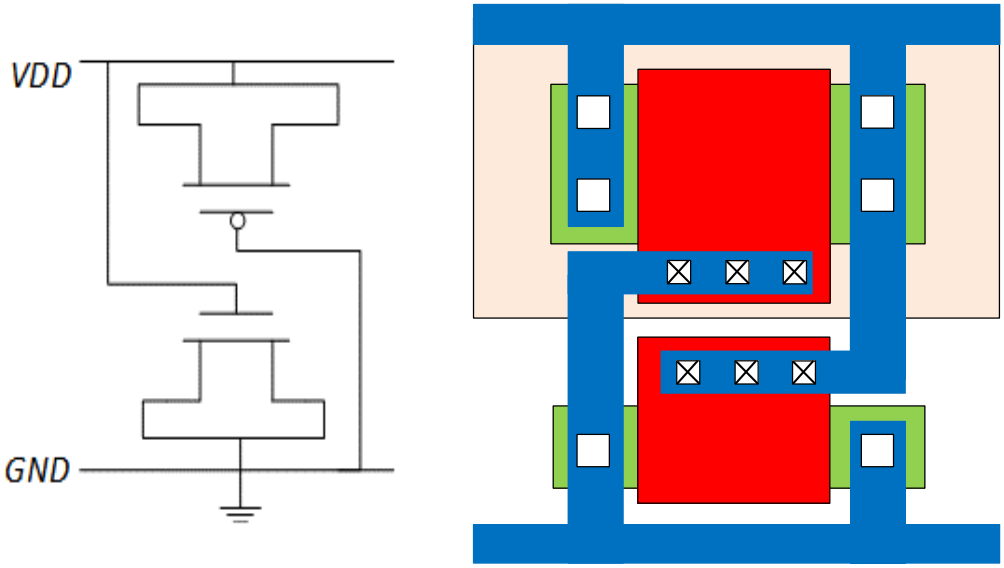


Figure 5.4 Decap cell schematic and layout

A power grid following the pattern presented in **Figure 5.5** was constructed to provide a robust power supply to the core. Metal layers 5 to 8 were used solely for the power grid. A width of at least 2X was applied for both horizontal and vertical power straps to reduce the total resistance on the grid.

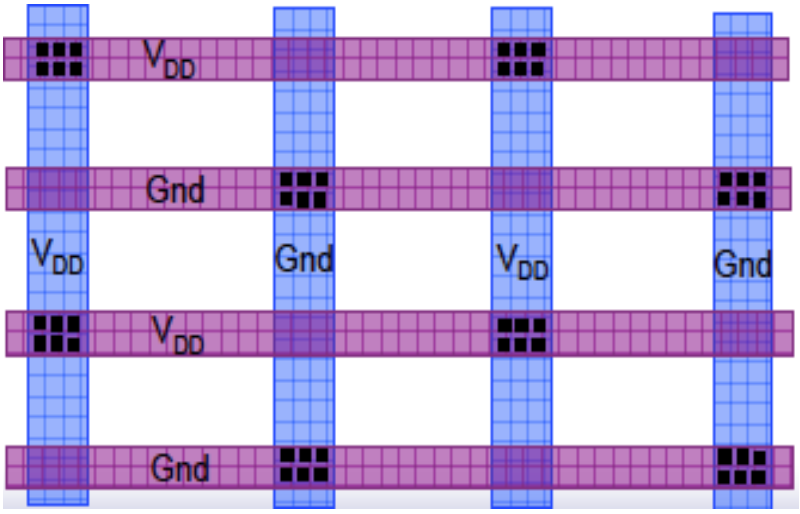


Figure 5.5 Power grid pattern used in chip

5.4 Top-level Floorplan and IOs

The top-level chip floorplan is illustrated in Figure 5.6. The die size is 1.5 mm by 2 mm. With 58 IO pads in total, that leaves an effective core area of about 0.9 mm by 1.4 mm. The logic chains are located at the top and bottom, with designs of other projects sitting in the middle. Each logic chain has a separate output pad, while all chains share the same input data and clock signal.

3 pairs of core and 2 pairs of IO p/g pads were placed each side on the west and east, while 2 pairs of core and 1 pair of IO p/g pads were placed each side on the north and south. All of the IO pads were equipped with electrostatic discharge (ESD) protection. **Table 5.1** presents a summary of implemented IO pads from IBM 130nm CMRF8SF-RVT General Purpose In-Line I/O library.

Table 5.1 IO pads used in the chip

Pad Name	Function
PBCOD8A	Bidirectional buffer with CMOS input and 8 mA p-channel open drain output
PVDD/PVSS	Core power and ground
PDVDD/PDVSS	IO cell power and ground
PCORNER	Allows continuation power, ground and guard rings at each chip corner

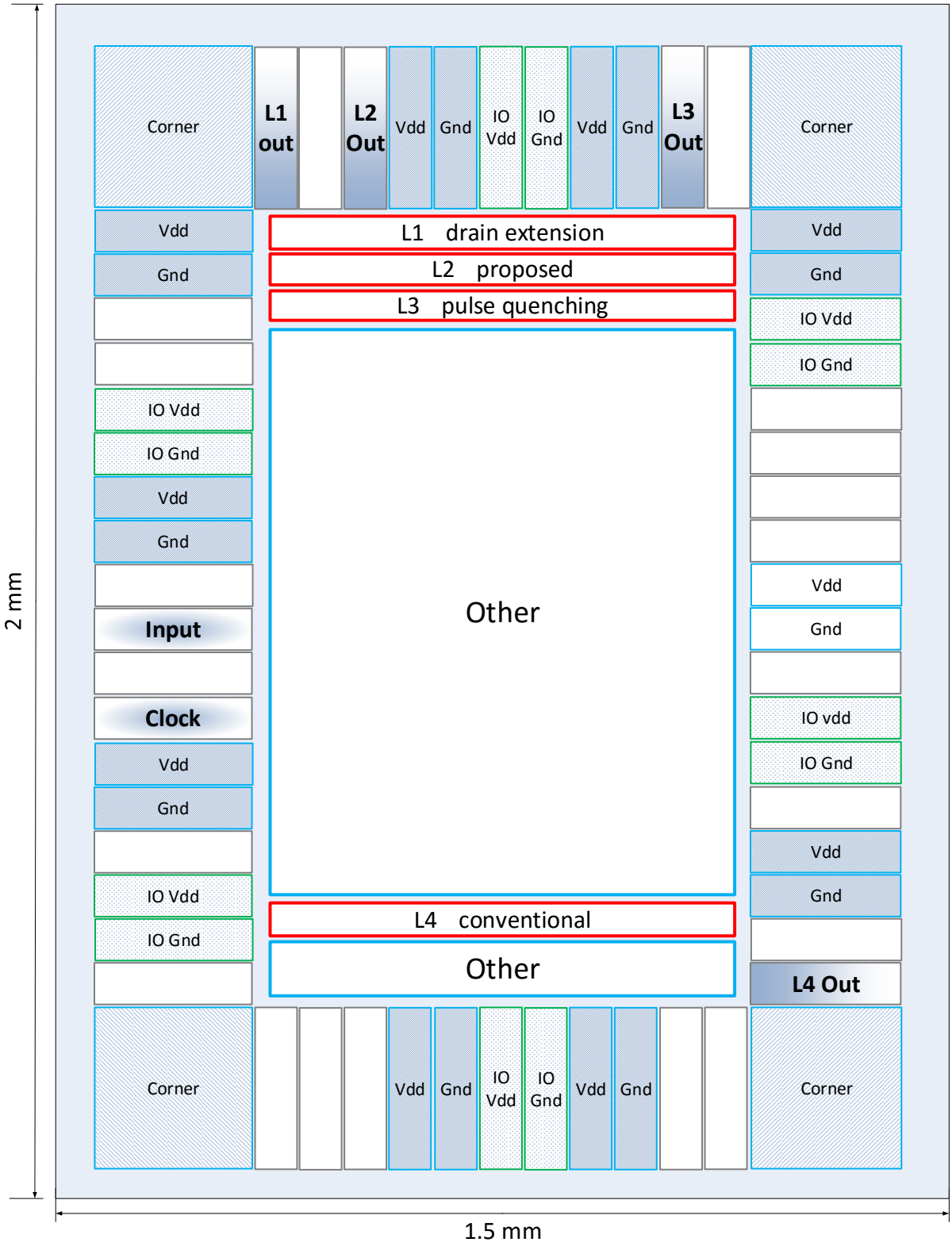


Figure 5.6 Chip floorplan

The layout of the full chip is depicted in **Figure 5.7**. Dummy metal fillings were subsequently added to the outside of the IO ring to increase local metal density and mark chip corner. Several windows were opened on the chip for future laser experiments. No wiring metal was present in those windows and dummy metal filing by foundry was disabled. Each window covered at least one critical device accessible for the high-resolution laser beam.

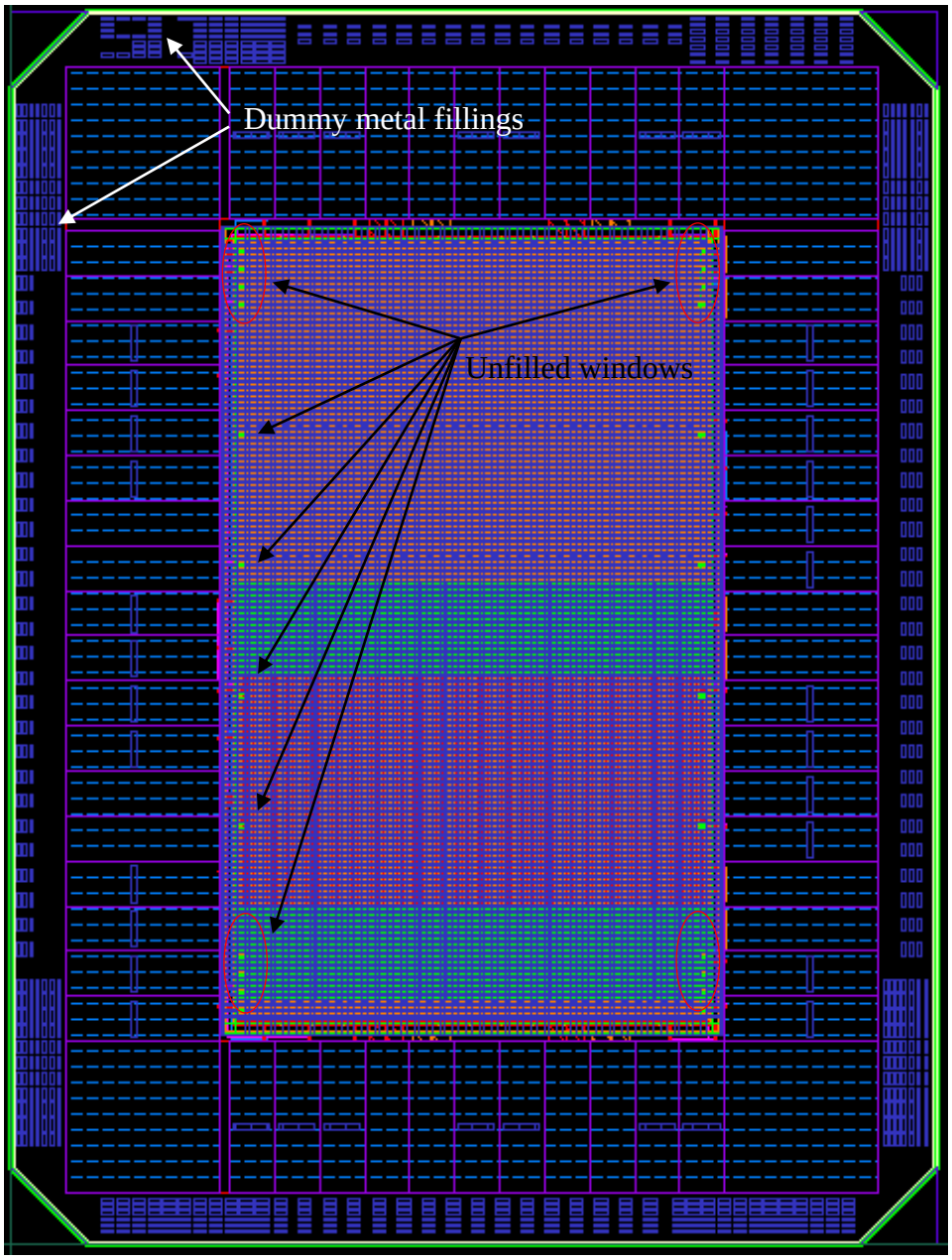


Figure 5.7 Top level chip layout

5.5 Sign-off Verification

Design rule checking (DRC), layout versus schematic (LVS), and SPICE simulation have been performed for chip sign-off verification.

Physical DRC, along with global and local density check, was verified with both Calibre and Assura tools provided in the PDK. Considering the fact that the whole chip was manually placed and routed, the LVS check was considered crucial in this work for successful tape-out. The LVS was performed using Calibre for only the core area, as layouts for the IO cells were not accessible to designers.

Whole chip simulation was not possible, due to large cell number and limited computing resources. SPICE simulation was conducted for each logic chain for functionality verification. Data patterns of all “1”, all “0” and checkerboard was sent to each chain input, and signals at the chain output were observed to check data consistency. Logic chains were verified to work correctly at up to 1 GHz in SPICE simulation.

CHAPTER 6 RADIATION EXPERIMENT

The test chip was fabricated through MOSIS in IBM 130nm CMOS technology. 20 packaged dies were shipped back using a 64-pin open cavity plastic quad flat no-lead (OCPQFN64A) package. Test chips were mounted on PCBs and placed under particle beams for radiation effects testing. An FPGA-based motherboard was used to provide input signals to test chips and send calculated error numbers to a personal computer (PC) in real time. Software on the PC end collects the error data and, subsequently, logs the error number per second and in total for each chain.

6.1 Experiment Setup

6.1.1 PCB Design

Each test chip was mounted onto a PCB with a 244-pin mini dual in-line memory module (DIMM). The PCBs were then plugged into an FPGA-based motherboard through its mini-DIMM socket.

The main function of the PCB is to connect chip inputs and outputs to the correct mini-DIMM pins for control and data signal transceiving by the motherboard. Four-layer PCBs were designed, with power and ground planes in the middle for optimal power distribution and heat dissipation. An additional 21 μF decoupling capacitance was added for IO and core power to maintain power integrity. The PCB layout is illustrated in **Figure 6.1**.

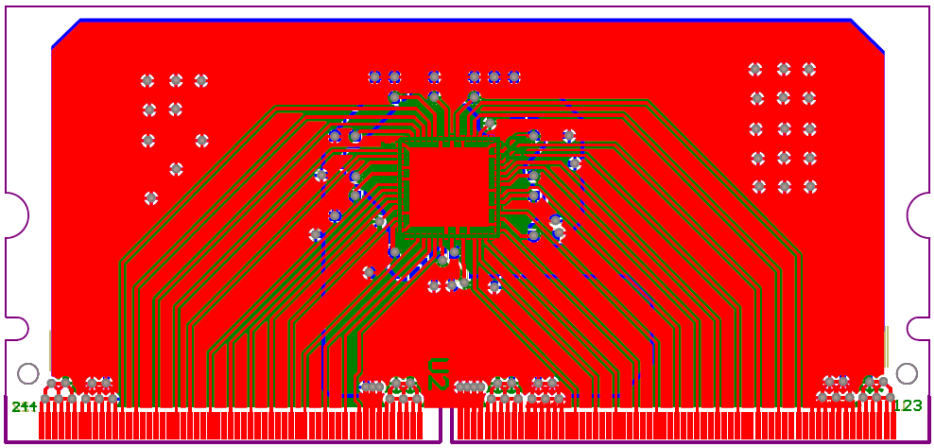


Figure 6.1 Daughter card PCB design

6.1.2 Testing System Configuration

The testing system for the radiation experiment is depicted in **Figure 6.2**. For heavy ions experiments, the motherboard, with device under testing (DUT) mounted, is placed in the vacuum chamber, and a particle beam of various energies is directly applied to the DUT. A power board provides 1.2 V and 2.5 V voltages to the DUT for its chip core and IO, and 5V for the motherboard. The motherboard communicates with a PC through an Ethernet cable. Clock frequency is controlled by a PC program through the FPGA digital clock manager (DCM).

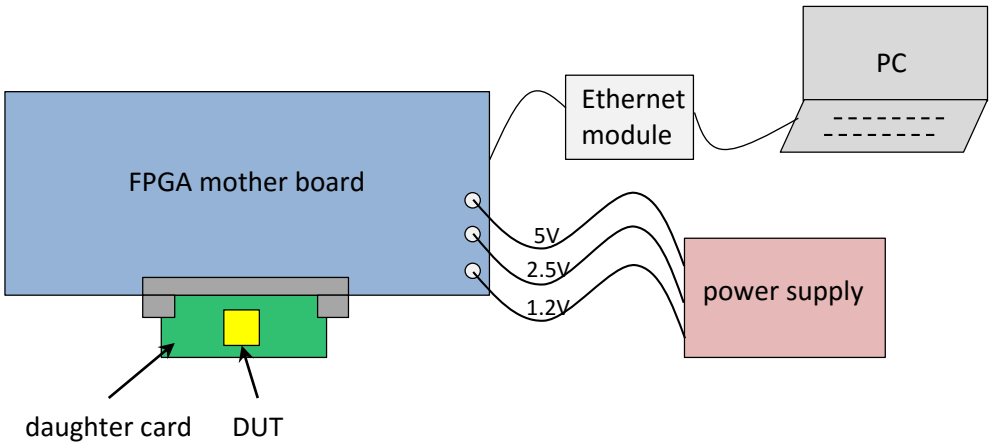


Figure 6.2 Radiation testing system

Considering the fact that the designs are hardened against SEE-induced HIGH-to-LOW transitions at the inverter outputs, a fixed logic LOW was fed into the chip as the logic chain data input. Checkerboard input pattern was not applied so as to limit burst errors triggered by clock buffers being hit. The clock signal for both dynamic logic and flops was running at either 10 kHz or 1 MHz. At a clock frequency of 100 MHz or higher, the test chip ceased to work properly, which was likely a result of by setup violations or signal integrity issues at high speed. Possible causes and explanations will be discussed later in this chapter.

The heavy ion experiments were carried out at the Cyclotron Institute of Texas A&M University (TAMU), which provides a diverse range of particle beams for radiation effect tests. Ions of LETs ranging from 1.3 to 28.3 MeV*cm^2/mg were used during the experiments. These ion profiles are presented in **Table 6.1**. The fluence of particle radiation is defined as the number of radiant-energy particles emitted from or incident on a surface in a given period of time, divided by the area of the surface.

Table 6.1 Heavy ions used during radiation experiments [50]

LET (MeV*cm^2/mg)	**Ion**	**Fluence**	**Energy (MeV/μ)**	**Range (μm)**
1.3	N	1.50×10^8	14.1	385.6
2.7	Ne	1.00×10^8	13.7	273.5
8.4	Ar	5.00×10^8	13	186.1
28.3	Kr	1.00×10^8	11.8	128

The ion beam was applied onto the DUT only. The test system ran for 5 minutes for each ion type and incident angle to generate enough errors. The run time and clock frequency was set from PC, and the number of errors was recorded at the end of each run. **Figure 6.3** shows the radiation test facility at TAMU.

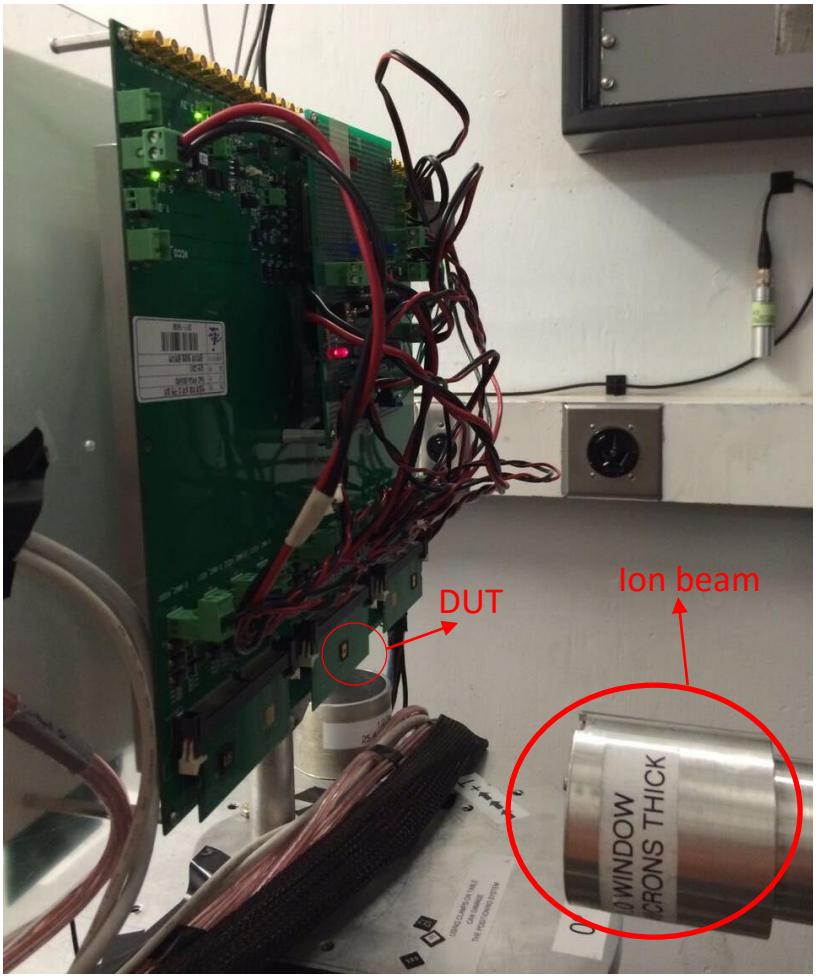


Figure 6.3 Heavy ion test facility at TAMU

6.2 Experiment Results

The DUT was first tested with 50 °angled incident heavy ions at a 10 kHz operating frequency. The SEU cross-section is defined as number of single events per unit fluence (logic gate SEU cross-section is expressed in area per gate), and is calculated by

$$SEU\ Cross\ section = \frac{number\ of\ errors}{fluence \times number\ of\ gates} \tag{6.1}$$

The cross-sections are demonstrated in **Figure 6.4**. As indicated by the picture, the proposed design demonstrated a lower soft error rate as compared to all other 3 designs: approximately 42% less than that of drain extension and 30% less than the other two at 28.3 MeV*cm^2/mg.

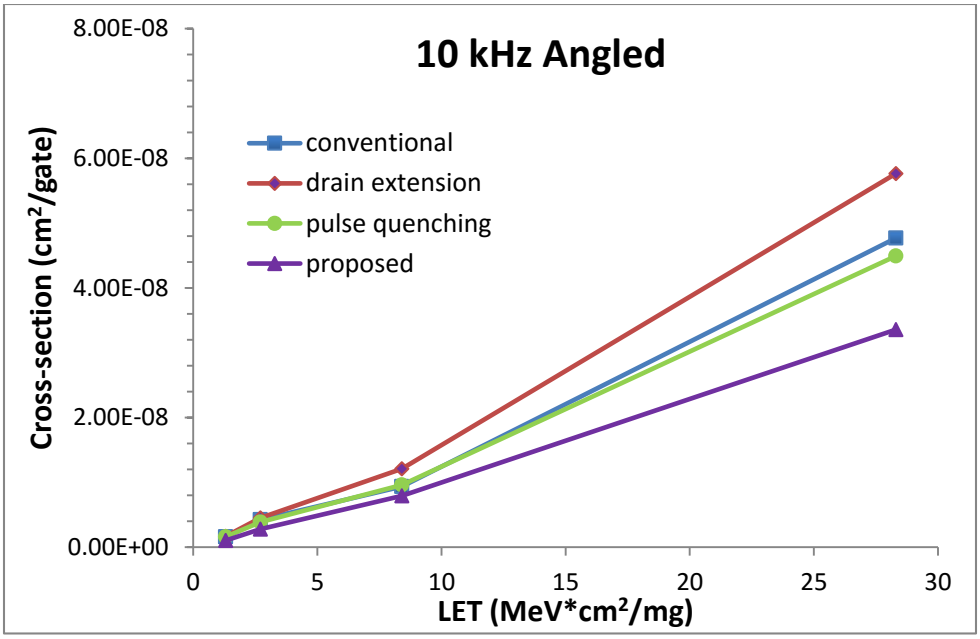


Figure 6.4 Cross-sections at 10 kHz with angled incidence

The DUT was then irradiated with normal incidence running at 1 MHz. **Figure 6.5** indicates that all of the cross-sections increased by approximately 4X, as expected. These results are in accordance with the precharge simulation results, in which the drain extension and proposed designed demonstrated a 28% pulse width reduction as compared to the conventional method.

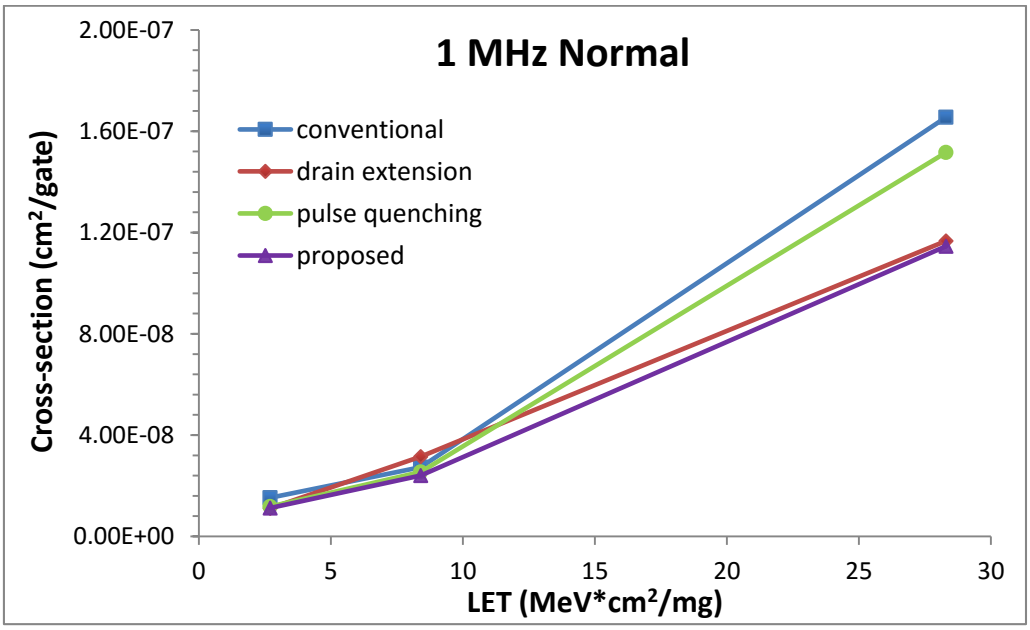


Figure 6.5 Cross-sections at 1 MHz with normal incidence

The incident angle was subsequently tilted to 50° to increase charge sharing between components. SEU cross-sections were observed to go up by another 2X, due to increased MBUs. The proposed design still demonstrated the lowest soft error rate among the four: as much as 30% less than the conventional design.

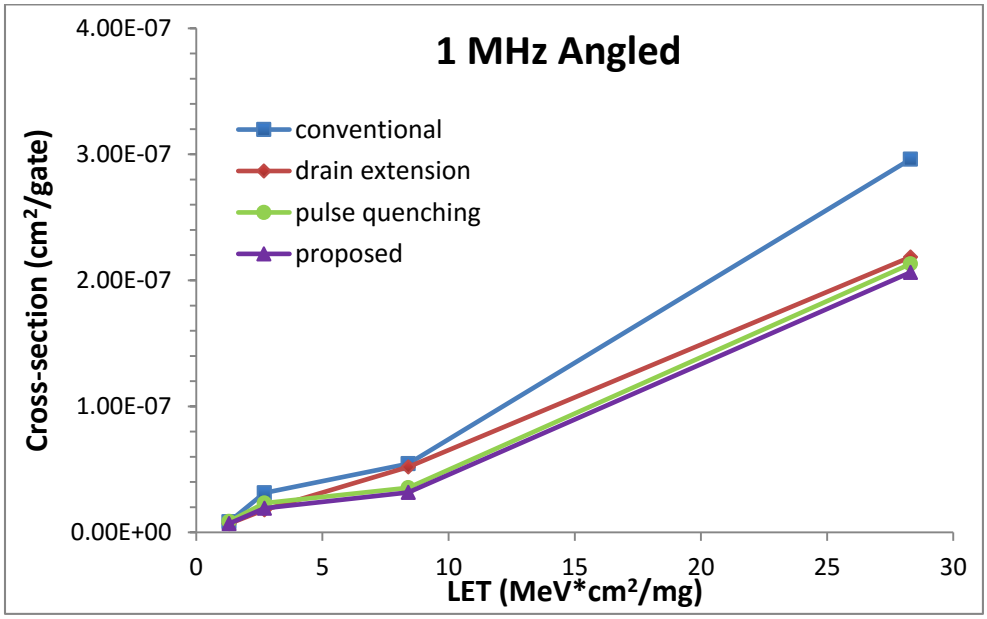


Figure 6.6 Cross-sections at 1 MHz with angled incidence

The DUT was also tested under a 1 MHz 28 MeV*cm^2/mg normal incident condition with a lowered 0.8 V power supply. The results are displayed in **Figure 6.7**. Most designs presented slightly fewer soft errors in lower voltage conditions, while the proposed design achieved a reduction of 42%.

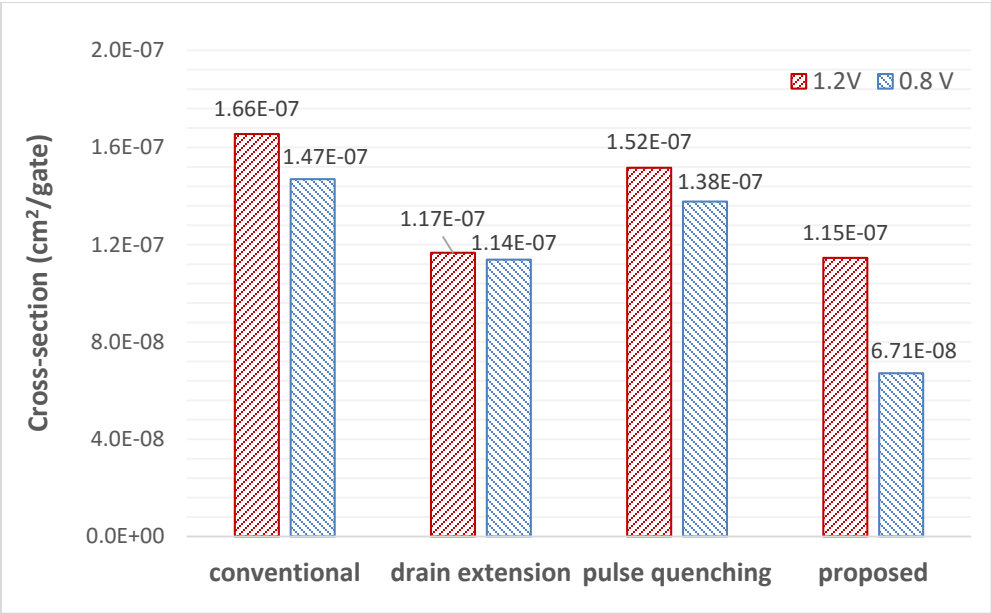


Figure 6.7 Cross-sections of different supply voltages at 1 MHz clock with 28 MeV*cm^2/mg normal incident ion

6.3 Results Analysis

1. LET threshold

Improved upset LET threshold is often associated with increased capacitance at the critical node, which in turn leads to area cost and speed degradation. Considering the fact that the dynamic logic family is extremely sensitive to SEE, it is extremely difficult to harden it by raising the threshold LET without introducing significant area cost. Furthermore, when taking into consideration that dynamic logics depend on the fast charge and discharge of the critical for high-speed operation, it is be impractical to prioritize rad-hardening over speed. Therefore, of the three unconventional designs presented in this work, none of them are targeted to increase the threshold LET of the SEU. As a result, the designs did not demonstrate significant improvements in regards to the upset LET threshold.

2. Simulations vs. experiments

Although the proposed design did outperform all other designs in this work from experiments, its improvement was not as optimal as indicated in the simulations. There are two possible factors: first, in the simulations, the definition of upset probability was introduced as an indicator to help evaluate the hardening performance; the circuit is considered more likely to suffer from an SEU when the SET pulse is wider during precharge, or when the propagation delay is larger during evaluation. This indicator gives a more optimistic prediction than the experimental results. Second, from the simulation results, the proposed design showed a prominent improvement in high-speed operations from at least 100 MHz. However, the highest frequency achievable in the actual experiments was less than 100 MHz due to system failures.

3. High speed

Several reasons may have caused the system failures at high speed.

While the reverse clocking eliminated risks of hold time violations, it may have triggered setup time violations at a high clock frequency.

Signal integrity (SI) issues could also lead to such failures. On-chip crosstalk between data and clock signals and an IR drop has the potential to cause SI problems on the DUT. Crosstalk can also originate from the PCB due to improper trace width and distance.

4. Low voltage

It is well known that higher SER in latch/flop is expected when supply voltage decreases, as it is easier to cause an upset at a lower voltage. In addition, according to a recent study that analyzed 28 nm circuit [51], the SER on static combinational logic presents a weaker negative correlation to supply voltage. In this work, however, a very weak positive correlation was found between the dynamic logic SER and supply voltage for the majority of the designs, while a stronger positive correlation was discovered for the proposed design.

For a flip-flop, the critical charge decreases when the supply voltage is reduced, and the cross-section is exponentially dependent on critical charge [52]. However, for a dynamic logic, critical charge plays a less important role, as the output node can easily be discharged when floating. On one hand, a lower supply voltage makes it faster to recover to *VDD* from a precharge SET. On the other, the fact that the trailing static inverter has a lower supply voltage renders the pulse quenching effect more efficient.

5. Performance comparison

Table 6.2 compares the performance of different logic designs. The data of TMR-based logic and static logic are obtained from [53]. As indicated from the table, the layout-based techniques have smaller delays than static logic, which is attributed to the removal of PMOS pull-up transistors. In terms of power consumption, all of the dynamic designs use a somewhat larger amount of power than static logic, due to the clocking activity. The proposed design costs only a slightly larger area than the conventional design, as does the drain extension design. With regard to soft error suppression, the proposed design exhibits comparable performance to TMR-based logic, which also has the most delay, power, and area costs.

Table 6.2 Performance comparison

	Conventional	**Drain extension**	**Pulse quenching**	**Proposed**	**TMR-based**	**Static**
Delay	1	1.12	1.10	1.19	1.98	1.27
Power	1	1.06	1.09	1.20	3.64	0.82
Area	1	1.10	1.34	1.10	3.60	2.40
Cross-section	1	0.70-1.20	0.72-0.94	0.69-0.70	0.64-0.79	N/A

CHAPTER 7 CONCLUSIONS AND FUTURE WORK

7.1 Summary

The dynamic combinational logic, or domino logic, families are a great fit for high-speed applications, especially in present day when the demand for high-speed performance has been ever-increasing. However, as a result of their fast transition, dynamic logics are also much more sensitive to radiation effects than their static counterpart. The working mechanism of domino logics and what renders them vulnerable to radiation effects were discussed comprehensively in this work. Previous works on hardening techniques, and dynamic logics in particular, were reviewed. A new layout-level hardening technique was proposed and implemented, along with two other hardening concepts. Designs have been simulated using 3D TCAD models to compare their SEE hardness. A 130 nm test chip containing different dynamic logic designs was designed, fabricated, and irradiated by heavy ion particles. Radiation experiment results confirmed the efficacy of the proposed hardening technique. Although only inverter/buffer designs were studied in this work, the proposed hardening technique can be applied to any dynamic logic circuit.

7.2 Conclusions

The following conclusions can be drawn from this study:

1. Radiation can affect dynamic logics at different operation stages. Ion strikes usually lead to SEUs other than SETs in domino logic circuits.
2. Layout techniques applied in a dynamic logic circuit can effectively improve its tolerance against radiation by introducing little overhead in speed and area.

3. 3D TCAD models for different hardening approaches were designed and calibrated to match the device characteristics of the design kit models.
4. Mixed-mode simulations were performed on different design approaches. The proposed design demonstrated substantial improvement over the other two design techniques in high-speed simulations.
5. The different designs were implemented on a 130 nm testing chip. The chip was designed to lower the risk of hold time violation and reduce IR drop.
6. A FPGA-based testing system was used to perform radiation experiments on the DUT test chip. According to the experiment results, the proposed design achieved as much as a 30% reduction in SEU cross-section under various incident angle and frequency conditions. The improvement is expected to be more prominent in higher frequencies. The proposed design also demonstrated improved hardening performance by 42% SEU cross-section reduction when the supply voltage was lowered by 400 mV. This improvement indicates that dynamic logic is promising for low-power applications.

7.3 Future Work

Considering the fact that the test chip is unable to function correctly at high speed, the chip can be redesigned to better fit high-speed applications. A more balanced clock distribution network can be designed to eliminate both setup and hold time violations. The placement and routing procedures can be automated by utilizing advanced CAD tools so as to save design effort and increase reliability. A static timing analysis (STA) can also be performed in signoff to further verify the chip's functionality.

More experiments on the chip can be carried out using the local laser facility at the VLSI lab. Using a high-resolution laser to induce soft errors directly on the sensitive node, experiment errors from particle hit on register or clock buffer components can be eliminated.

The chip can also be fabricated using more advanced technologies such as 65 nm and 28 nm, in which charge sharing is more abundant.

More factors should be taken in consideration during the PCB design as well. The optimal trace widths and lengths are required to control the characteristic impedance of the traces. Parallel running traces should be avoided during design too. SPICE simulations can be performed to check for SI issues on the PCB.

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