

# **Investigation on LIGA-MEMS and On-Chip CMOS Capacitors for a VCO Application**

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## ABSTRACT

Modern communication systems require high performance radio frequency (RF) and microwave circuits and devices. This is becoming increasingly challenging to realize in the context of cost/size constraints. Integrated circuits (ICs) satisfy the cost/size requirement, but performance is often sacrificed. For instance, high quality factor ( $Q$  factor) passive components are difficult to achieve in standard silicon-based IC processes.

In recent years, microelectromechanical systems (MEMS) devices have been receiving increasing attention as a possible replacement for various on-chip passive elements, offering potential improvement in performance while maintaining high levels of integration. Variable capacitors (varactor) are common elements used in various applications. One of the MEMS variable capacitors that has been recently developed is built using deep X-ray lithography (as part of the LIGA process). This type of capacitor exhibits high quality factor at microwave frequencies.

The complementary metal oxide semiconductor (CMOS) technology dominates the silicon IC process. CMOS becomes increasingly popular for RF applications due to its advantages in level of integration, cost and power consumption. This research demonstrates a CMOS voltage-controlled oscillator (VCO) design which is used to investigate methods, advantages and problems in integrating LIGA-MEMS devices to CMOS RF circuits, and to evaluate the performance of the LIGA-MEMS variable capacitor in comparison with the conventional on-chip CMOS varactor. The VCO was designed and fabricated using TSMC 0.18  $\mu\text{m}$  CMOS technology. The core of the VCO, including transistors, resistors, and on-chip inductors was designed to connect to either an on-chip CMOS varactor or an off-chip LIGA-MEMS capacitor to oscillate between 2.6 GHz and 2.7 GHz. Oscillator phase noise analysis is used to compare the performance between the two capacitors. The fabricated VCO occupied an area of 1  $\text{mm}^2$ .

This initial attempt at VCO fabrication did not produce a functional VCO, so the performance of the capacitors with the fabricated VCO could not be tested. However, the simulation results show that with this LIGA-MEMS capacitor, a 6.4 dB of phase noise improvement at 300 kHz offset from the carrier is possible in a CMOS-based VCO design.

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## LIST OF ABBREVIATIONS

ADS	Advanced Design System
ASITIC	Analysis and Simulation of Spiral Inductors and Transformers for ICs
BJT	Bipolar Junction Transistor
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CPW	Coplanar Waveguide
CTM	Capacitor Top Metal
DXRL	Deep X-ray Lithography
EDM	Electro Discharge Machining
FET	Field Effect Transistor
FOM	Figure Of Merit
FZK	Forschungszentrum Karlsruhe (Research Centre Karlsruhe)
GaAs	Gallium Arsenide
HB	Harmonic Balance
HFSS	High Frequency Structure Simulator
IC	Integrated Circuit
IF	Intermediate Frequency
IMT	Institute of Microstructure Technology
LC	Inductor Capacitor (Passive Network)
LO	Local Oscillator
ISF	Impulse Sensitivity Function
LIGA	German acronym for Lithography, Electroforming, and Moulding (Lithographie, Galvanoformung, Abformung)
LTI	Linear Time-Invariant
LTV	Linear Time-Varying
MEMS	Microelectromechanical Systems

MIM	Metal-Insulator-Metal (Capacitor)
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MUMPS	Multi-user MEMS Process
NMOS	N-type Metal Oxide Semiconductor
PGS	Patterned Ground Shield
PLL	Phase-Locked-Loop
PMMA	Polymethyl Methacrylate
PMOS	P-type Metal Oxide Semiconductor
RC	Resistor Capacitor (Passive Network)
RF	Radio Frequency
RLC	Resistor, Inductor and Capacitor (Passive Network)
SEM	Scanning Electron Microscope
SOC	System-On-Chip
TSMC	Taiwan Semiconductor Manufacturing Company
UJT	Unijunction Transistor
VCO	Voltage-Controlled Oscillator
YIG	Yttrium Iron Garnet

## 1. Introduction

### 1.1 CMOS Radio Frequency Integrated Circuits

The explosive growth in wireless telecommunications has brought the field of radio frequency (RF) circuit design to a renaissance. It is advantageous from cost and size perspectives to integrate RF transceiver front-end components into a single chip with the back-end baseband components. Thus, radio transceiver design is merging with integrated circuit (IC) design, particularly in CMOS (complementary metal oxide semiconductor). CMOS technology has become the most popular technology in digital design. It has three major advantages: high integration level, low cost, and low power consumption. The rapid advancement in CMOS technology and the continuous down-scaling the size of CMOS device has made low cost, small size RF integrated circuits feasible.

However, difficulties exist in synthesizing RF integrated circuits on CMOS. Due to the lossy silicon substrate, performance of CMOS circuits at microwave frequencies (i.e.,  $> 1$  GHz) is an issue. High quality ( $Q$ ) passive components are difficult to achieve in CMOS due to the nature of materials and fabrication process. These factors make CMOS RF integrated circuit design an interesting and challenging area to study.

RF circuits are typically made up of many passive components. Since integrated circuit processes were mainly developed to satisfy the demands of digital circuits, passive components are limited and often unsatisfying to the RF IC designers. For example, CMOS inductors occupy large chip area and have poor  $Q$ -factor (typically less than 10) and low self-resonant frequency (a few GHz). CMOS capacitors also exhibit low  $Q$ -factor. New techniques, such as metal-insulator-metal (MIM) capacitors

and thick top layer metal inductors, have been introduced to CMOS, which provide relatively higher quality [1]. However, traditional CMOS passive components are still inadequate for high performance applications with increasing operating frequencies, and alternative technologies for realizing high performance passive components are the subject of recent research.

## 1.2 Introduction to MEMS

In recent years, microelectromechanical systems (MEMS) have been receiving increasing attention. As the name suggested, MEMS are devices in the micrometer scale. They typically range in size from the sub-micron to 100's of microns.

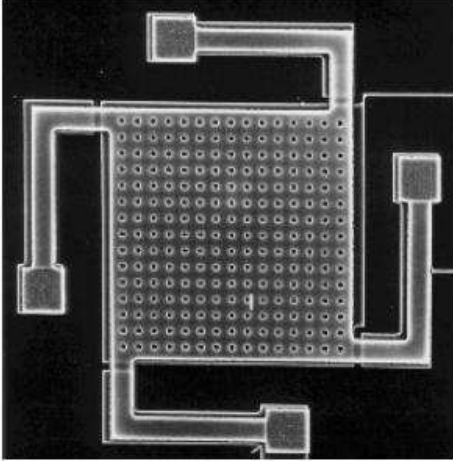
MEMS technology promises high integration abilities between structural mechanical devices and electronics. But by not being strictly tied to CMOS electronics, MEMS offers the potential for improved performance. Also, MEMS processes, which are similar to integrated circuit fabrication and suitable for high volume production, make MEMS devices potentially inexpensive.

There are numerous possible applications for MEMS. MEMS products are found in medical devices, optical devices, sensors, actuators and many different areas. In RF circuits such as voltage-controlled oscillators (VCOs), phase shifters, MEMS devices are used as switches, filters, inductors, and variable capacitors (also known as varactors).

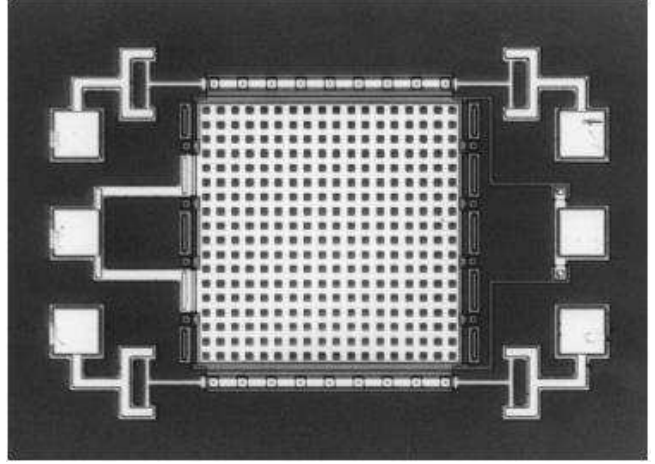
There are a number of MEMS microfabrication technologies. Silicon surface micromachining makes completely assembled mechanical systems. Silicon bulk micromachining uses either etches that stop on the crystallographic planes of a silicon wafer or etches that act isotropically to generate mechanical parts. These techniques combined with wafer bonding and boron diffusion allow complex micro-mechanical devices to be fabricated. Another technique in MEMS fabrication is called LIGA, which will be introduced in the next section.

Most of the existing MEMS capacitors are fabricated using silicon-based thin film processes, such as the multi-user MEMS process (MUMPS). Typically they fall into three categories. The first type is the parallel plate designs in which planar

geometries and the plates are parallel to the substrate. The capacitance is varied by changing the gap between the plates. These capacitors typically have capacitance values between 1 - 4 pF, and are targeted for applications in lower end of the microwave frequency range (1 - 3 GHz) [2,3]. Figure 1.1 shows some examples of this type of capacitors.



(a) Young et al. [2]



(b) Dec et al. [3]

Figure 1.1: Parallel Plate Capacitor Designs

A second type are the lateral comb designs. They have comb-shaped fingers overlapping each other and the capacitance is varied by adjusting the overlap. Figure 1.2 shows an example of these capacitors [4].

A third type is shunt mounted designs. These are a variation of the parallel plate design and intended to operate at higher frequency. A bridge shunt mounted over a coplanar waveguide (CPW) transmission line forms the capacitor instead of two plates. Figure 1.3 shows an example of this type of capacitor, which can operate above 10 GHz [5].

### 1.3 LIGA Process

LIGA is the German acronym for lithografie, galvanoformung, and abformung, which means lithography, electrodeposition, and moulding. The LIGA technology

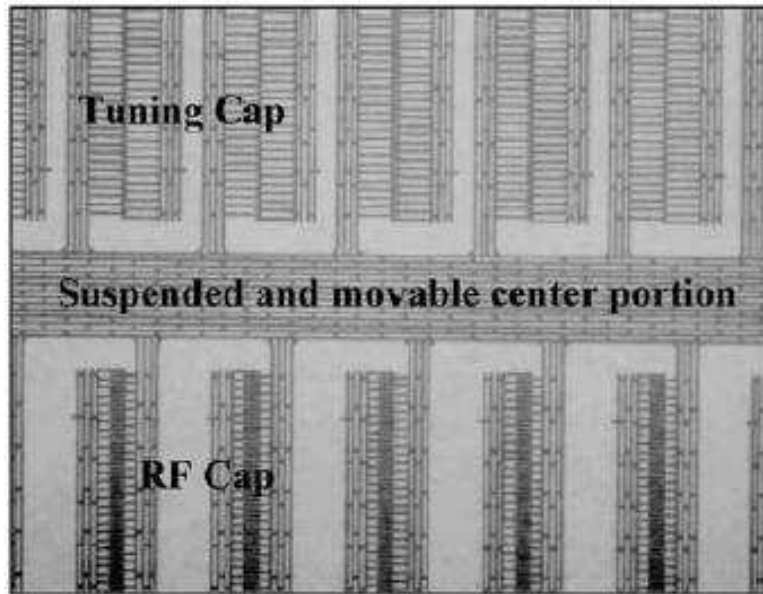


Figure 1.2: Lateral Comb Capacitor Design [4]

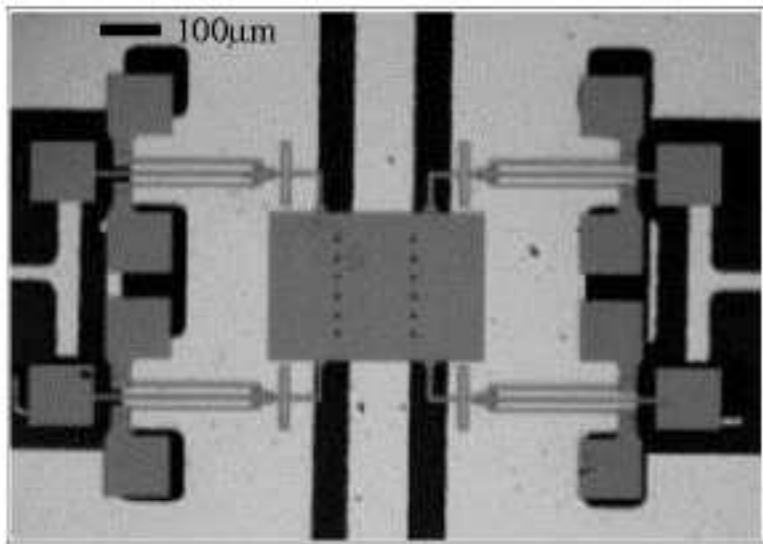
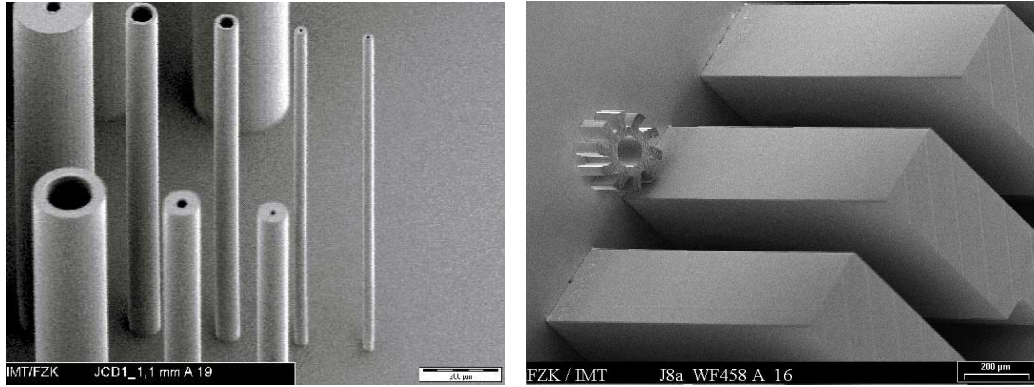


Figure 1.3: Shunt Mounted Capacitor Design [5]

makes miniature parts with spectacular accuracy and structural quality. Electro discharge machining (EDM) extends conventional machine shop technology to make sub-millimeter sized parts [6].

The complete LIGA process involves deep X-ray lithography (DXRL) using syn-

chrotron radiation, electroplating of metals, and replication using moulding techniques. The LIGA process was developed during the 1980's in Germany at the Research Centre Karlsruhe (Forschungszentrum Karlsruhe) as a method to produce tiny and precise separation nozzles for uranium isotopes [7,8]. The unique advantage of the LIGA process, due to the strong penetration ability of high energy X-rays, is that it can produce structures with extremely high vertical aspect ratios (greater than 100). Also, the structures can have greater than  $89.9^\circ$  and optically smooth sidewalls, and can be very tall (hundreds of microns or even millimetres), while the lateral feature sizes can be smaller than one micron. No other fabrication technique so far can provide comparable structure quality. Figure 1.4 shows two examples of structures fabricated using LIGA, which demonstrate the tiny but precise features of LIGA devices [9, 10].



(a) 1100  $\mu\text{m}$  Posts in SU-8 with Minimum 7  $\mu\text{m}$  internal diameter holes [9] (b) 1100  $\mu\text{m}$  PMMA Frames & 125  $\mu\text{m}$  Nickel Turbine [10]

Figure 1.4: LIGA Structure Examples

The unique properties of the LIGA process have led to an interest in developing high performance RF/microwave LIGA devices. Researches on microwave LIGA devices include transmission lines, filters, and couplers have been reported [11–13].

## 1.4 LIGA-MEMS Variable Capacitor

As described in Section 1.2, most of the traditional MEMS variable capacitors operate either at the lower end of the microwave frequency range below 3 GHz (planar parallel plate designs and lateral comb structure designs), or in the 10 - 40 GHz range (shunt mounted designs). In the 3 - 10 GHz frequency range, current techniques have difficulty realizing high  $Q$ -factor variable capacitors. The LIGA technology could potentially fill the gap.

LIGA-MEMS variable capacitors have demonstrated promising performance [14]. The capacitor designs feature parallel plates and the capacitance is varied by changing the gap between the plates. But unlike traditional planar parallel plate capacitors, in the LIGA-MEMS capacitor designs, the parallel plates are perpendicular to the substrate. This vertical structure is suitable to realize with the LIGA technology because of the high aspect ratio possibilities of the vertical plates. The use of thick metal structure reduces the resistance, while use of the vertical dimension results in an electrically compact structure and also separates the fields from the substrate, both of which result in devices with high  $Q$ -factors and high self-resonance frequencies. The use of alumina and other low-loss substrates, avoiding the lossy silicon substrates, also leads to improved performance. The LIGA-MEMS variable capacitors exhibit excellent properties for microwave frequency applications.

## 1.5 Introduction to VCO

Most electronic signal processing systems require frequency or time reference signals. For the lower end of the spectrum, the stable quartz crystals can be used as resonators to build high accuracy fixed frequency reference signals. For higher frequencies, the quality of crystal resonators degrades due to physical limitations and material properties. Many communications applications require programmable carrier frequencies. For these applications, multiple crystal resonators usually would not be used due to the limitations in cost and size. In such cases, RF oscillators, whose frequency can be controlled with a control signal are used.

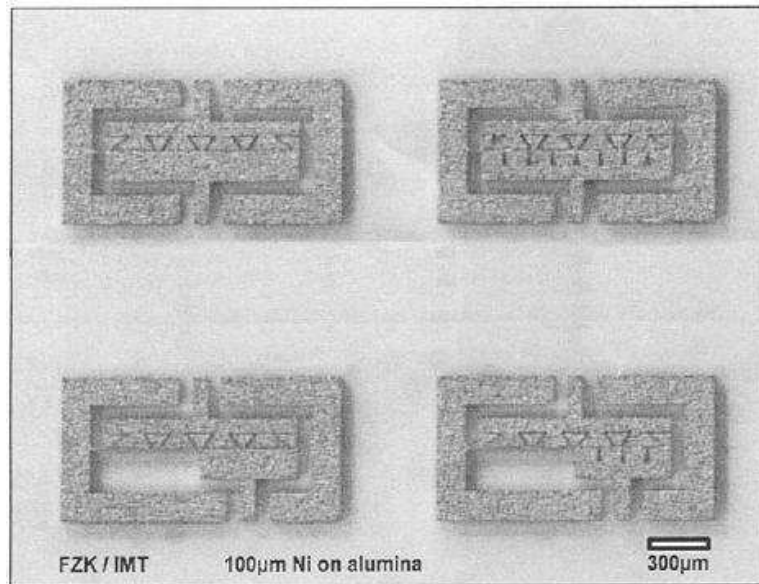


Figure 1.5: LIGA MEMS Variable Capacitors [14]

Oscillators are one-port devices that consume DC power and generate periodic signals at certain frequencies without any input signal. Often, the oscillation frequency can be controlled by a voltage (or, in some cases, current). This kind of device is called a voltage-controlled oscillator.

The VCO is a very important component in a phase-locked-loop (PLL). PLLs are widely used in analog and digital systems. For example, PLLs are used in clock recovery in communication and digital systems, in frequency synthesizers used in wireless communication systems to select different channels, and in modulation and demodulation of frequency or angle modulated carriers.

Technology evolutions have pushed realization of VCOs into the GHz range. The better propagation characteristics and the larger available bandwidth in the 1 GHz to 2 GHz range have allowed the standardization and exploitation of digital cellular phone systems worldwide. At higher frequencies around 2.5 GHz to 5 GHz, new wireless data applications have spurred a lot of interest and large markets, such as short range automation applications, and cable replacement wireless links. These new applications set a large demand for high performance GHz VCOs. Internet growth and the convergence of data and voice communications, which deploys Gbit/sec data channels and relies on clock recovery architectures, also increases the

demand for GHz VCOs [15].

Recent research on RF VCOs is generally focused on IC technologies [16–20]. The choice of IC technology is mainly driven by the requirements of the majority of the circuits, which are usually digital. Price, package, performance and power are four “*P words*” that govern high volume markets. For the VCO itself, integration has advantages in terms of cost, package and power consumption. ICs reduce production cost by allowing mass production. Integrating VCOs in ICs allows easy integration between VCOs and other RF components. ICs allow low voltage operation which results an advantage in power consumption. Using ICs for RF typically results in a lower performance, such as noise.

## 1.6 Motivation

The LIGA technology provides a new method of fabricating high quality passive components. The LIGA-MEMS variable capacitors mentioned in the previous section have shown performance advantages over conventional CMOS varactors, and promising potential in RF circuits. However, capitalizing on these advantages in RF circuits and still maintaining high levels of integration likely require effectively integrating such devices with RF ICs.

CMOS has become a mainstream of RF IC design, while the CMOS on chip passive components are not satisfying the increasingly demanding performance requirements of the fast advancing telecommunication systems. There is a good potential for the high quality LIGA-MEMS passive components as a replacement for CMOS passive components in performance-oriented RF circuits.

As for replacing the CMOS passive components with LIGA-MEMS devices, many issues must be considered. How can the LIGA-MEMS devices be integrated into the CMOS chip? How much improvement can the MEMS device achieve in the RF circuit performance? Which passive components should have the priority of being replaced? Will the CMOS and LIGA fabrication processes conflict?

## 1.7 Objectives

This thesis focuses on developing a CMOS VCO circuit based on existing LIGA-MEMS capacitor designs [14], as the first attempt to integrate CMOS RF integrated circuits with LIGA-MEMS devices, and to exemplify the performance advantages of LIGA-MEMS devices over conventional CMOS passive components in RF circuits. To the author's knowledge, no LIGA passive component has been integrated with CMOS circuitries for RF applications. The specific objectives of the research are summarized as follows:

1. Develop a CMOS VCO circuit in the 2.6 - 2.7 GHz range which can use either an on-chip CMOS varactor or a LIGA-MEMS variable capacitor as the tuning component.
2. Investigate possible methods for integrating the LIGA-MEMS variable capacitor to the CMOS circuitry.
3. Simulate and compare the performance of the VCO using the on-chip CMOS varactor and LIGA-MEMS variable capacitor.
4. Fabricate the VCO chip and integrate it with the fabricated LIGA-MEMS variable capacitor and the on-chip varactor.
5. Test the VCO circuit and determine the performance against the simulation results.

## 1.8 Thesis Organization

This thesis is organized into six chapters. Chapter 2 presents background theories related to CMOS RF integrated circuit design. Chapter 3 describes the VCO design procedure, including design issues to be considered and schematic design. Chapter 4 describes the VCO layout in CMOS. Chapter 5 presents simulation results and performance comparison, and test procedure and results of the fabricated VCO chip. The difficulties encountered in integration and possible solutions are also discussed. Chapter 6 presents conclusions of this research, and future work is suggested.

## 2. VCO Background

In this chapter, introduction to the voltage controlled oscillator (VCO) and background theories on various VCO concepts, such as quality factor and phase noise will be presented.

### 2.1 Voltage-Controlled Oscillator

In this section, different ways of realizing a VCO and important criteria and principles are presented.

#### 2.1.1 Types of Oscillators

There are many different types of oscillators. Two major classifications are those that create sinusoidal outputs and those that create square or triangular wave outputs. Sinusoidal-output oscillators are more typical of analog or RF circuits and normally contain frequency-selective circuits. Square-wave-output oscillators are more typical of digital circuits and can be realized using feedback circuits such as relaxation oscillators or ring counters.

The ring oscillator is one of the most popular forms of digital output oscillators. A ring oscillator is realized by placing an odd number of inverters in a feedback loop. A rising edge at any node propagates through the inverters in the loop, and returns as a falling edge after the delays through the inverters. This falling edge then propagates and returns inverted as a rising edge. This repeats and generates a square wave oscillation. The oscillation frequency is determined by the delay and the number of the inverters. Assuming all the inverters have a delay of  $t_p$ , a ring oscillator with  $N$  inverters will oscillate at frequency  $1/2Nt_p$ .

Another popular method for realizing digital output VCOs is a relaxation oscilla-

tor. A relaxation oscillator is a circuit that repeatedly charges a capacitor gradually and discharges it rapidly. It is usually implemented with devices with threshold, such as a neon lamp, unijunction transistor (UJT), or Gunn diode. A relaxation oscillator often produces a square wave or sawtooth wave.

Sinusoidal-output oscillator design usually involves placing a frequency-selective circuit into a positive feedback loop in which, at the selected frequency, the loss in the tuned circuit is compensated by the feedback circuit and the loop gain becomes unity. Sinusoidal oscillators, based on different frequency-selective components, can be classified into RC oscillators, LC oscillators, switched-capacitor oscillators, and crystal oscillators. Early integrated oscillators based on tuned circuits were largely realized using switched-capacitor circuits or off-chip crystals [21]. Integrated LC filters at GHz frequencies were used in oscillators with the development of semiconductor processes in the early 1990's [22].

For low frequency applications (DC to 100 kHz), the frequency-selective circuits seldom use inductors because the required inductors are large and technically impossible to fabricate in monolithic form. Thus, inductorless filters, such as RC and switched capacitor filters are usually used. RC filters are fabricated using discrete, hybrid thick-film, or hybrid thin-film technology. However, these technologies are not as cost efficient as monolithic fabrications for large volume production. At the present time, the switched capacitor technique is the most viable approach [21]. Switched capacitor circuits use combination of switches and capacitors to simulate the effect of resistors, thus allow filters to be realized without using resistors since resistors are more difficult to implement in ICs than capacitors and switches.

For RF and microwave frequencies, crystals and LC-tuned circuits are often used. They exhibit higher  $Q$  than RC-tuned circuits. LC-tuned oscillators utilize parallel LC tank circuits as frequency selective components. These oscillators are known as self-limiting because the effective gain of the transistors reduces as the oscillation amplitude grows and eventually the loop gain becomes unity.

A piezoelectric crystal, such as quartz, has its reactance inductive over a very narrow frequency band. Replacing the inductor in the LC-tuned circuits with a

crystal results a very well defined resonance frequency. When used as a high  $Q$  frequency selective component, a crystal exhibits extremely stable resonance characteristics and very accurate operation frequency. Unfortunately, being mechanical resonators, crystal oscillators are fixed-frequency circuits and cannot be easily tuned.

### 2.1.2 Barkhausen Criteria

In an amplifier circuit with feedback, if the feedback signal is in phase with the input and the magnitude of the feedback is large enough, the circuit becomes unstable. If any input, including noise, is applied to such a feedback circuit, the input grows. After a period of time, the growing transients are sufficiently large, the circuit elements produce nonlinear response and eventually the signals stop growing. In the steady-state, the circuit becomes an oscillator.

However, to obtain a useful oscillator requires more than stability. At the oscillation frequency  $\omega_0$ , the phase of the loop gain should be zero and the magnitude of the loop gain should be unity. This is known as the Barkhausen criterion. For the circuit to oscillate at one frequency, the oscillation criterion should be satisfied only at one frequency,  $\omega_0$ ; otherwise the resulting waveform will not be pure sinusoidal.

Consider a system as shown in Figure 2.1, which contains an amplifier with frequency-dependent forward loop gain  $G(j\omega)$  and a frequency-dependent feedback network  $H(j\omega)$ .

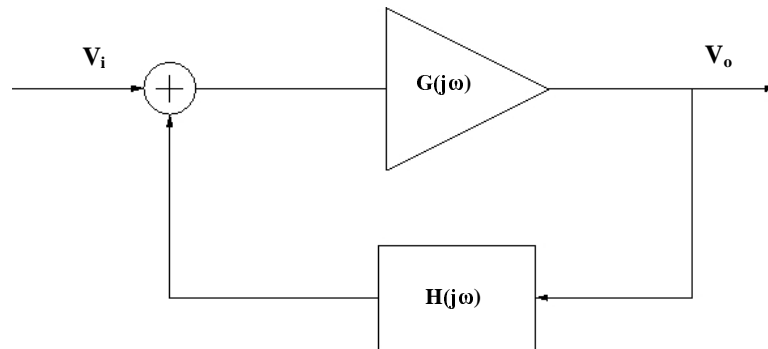


Figure 2.1: Block Diagram of Feedback Circuit

The closed-loop transfer function can be written as

$$T(j\omega) \equiv \frac{v_o(j\omega)}{v_i(j\omega)} = \frac{G(j\omega)}{1 - G(j\omega)H(j\omega)} \quad (2.1)$$

The loop gain  $G(j\omega)H(j\omega)$  is a complex number that can be represented by:

$$L(j\omega) \equiv G(j\omega)H(j\omega) = |G(j\omega)H(j\omega)|e^{j\phi(\omega)} \quad (2.2)$$

where  $L(j\omega)$  is the loop gain composed of magnitude and phase. If at a specific frequency  $\omega_0$ ,  $L(j\omega_0) = 1$ ,  $T(j\omega_0)$  will be infinite. This indicates that at this particular frequency, the circuits will have a finite output signal even with zero input. Hence, oscillation occurs when  $L(j\omega_0) = 1$ , or

$$|G(j\omega_0)H(j\omega_0)| = 1 \quad (2.3)$$

and

$$\phi(\omega_0) = \arg(G(j\omega_0)H(j\omega_0)) = 2n\pi \quad \text{for } n = 0, 1, 2, \dots \quad (2.4)$$

Since the amplitude of oscillation is associated with the nonlinear gain of the active device, Equation 2.3, known as the open-loop gain, sets the oscillation amplitude (the amplitude at which Equation 2.3 is satisfied), and Equation 2.4, known as the loop phase, sets the oscillation frequency.

### 2.1.3 Negative Resistance Oscillator Principles

A frequency-selective oscillator is mainly composed of a resonator, represented by  $H(j\omega_0)$ , and an active circuit, represented by  $G(j\omega_0)$ . There are numerous frequency-selective components available for oscillators, including lumped elements, dielectric puck, distributed transmission line (microstrip or coaxial line), waveguide or cavity, and YIG (Yttrium Iron Garnet) sphere resonators. Most of the RF and microwave resonators can be represented by series/parallel lumped equivalent circuits, i.e., capacitors and inductors. As with all lumped components, losses exist due to finite conductivity, hysteresis, eddy currents, leakage and many other reasons. As a result, the equivalent circuits always need resistors to represent the losses in the circuits. To satisfy the Barkhausen Criteria, the active circuits must provide gains to compensate the losses. As these active devices are to counteract the positive resistance

in the resonators, they can be seen as negative resistance. If the negative resistance is able to exactly cancel out the resonator losses, steady-state oscillations are obtained. For convenient and intuitive design and analysis, active circuits in RF and microwave oscillators are often treated as negative resistance.

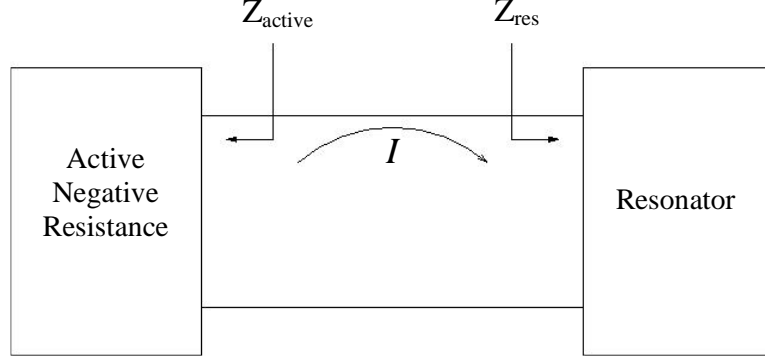


Figure 2.2: One-port Negative Resistance Oscillator Model

The basic principles of a negative resistance oscillator can be shown by the one-port model in Figure 2.2. The resonator has impedance of  $Z_{res} = R_{res} + jX_{res}$ , and the active device has impedance of  $Z_{active} = R_{active} + jX_{active}$ . This impedance is usually current (or voltage) and frequency dependent. Kirchhoff's voltage law gives

$$(Z_{res} + Z_{active})I = 0 \quad (2.5)$$

When oscillating, current  $I$  is nonzero, then the following condition must be satisfied:

$$R_{res} + R_{active} = 0 \quad (2.6)$$

and

$$X_{res} + X_{active} = 0 \quad (2.7)$$

Since the resonator is a passive load,  $R_{res}$  is always positive. This indicates that  $R_{active}$  must be negative, which implies an energy source.

The process of oscillation depends on the nonlinear behavior of  $Z_{active}$ . Initially, the circuit must be unstable at a certain frequency, with  $R_{res} + R_{active} < 0$ . Any transient excitation or noise will cause an oscillation to build up. As  $I$  increases,  $R_{active}$  becomes less negative until the current reaches  $I_0$  such that  $R_{res} + R_{active}(I_0, j\omega_0) = 0$ , and  $X_{res}(j\omega_0) + X_{active}(I_0, j\omega_0) = 0$ . Then the oscillation is in steady-state. The final frequency  $\omega_0$  is generally different from the startup frequency, because  $X_{active}$  is current (or voltage) dependent.

#### 2.1.4 Resonator Principles

A typical resonant tank is a parallel LC circuit. Both the inductor and the capacitor have resistance associated with them, which for illustration can be modeled as a parallel RLC equivalent circuit.  $R_p$  represents the combined resistive loss of the inductor and capacitor.  $L_p$  and  $C_p$  represent the parallel equivalent inductance and capacitance, and both are purely reactive.

A parallel RLC circuit resonates when the susceptance of the inductor and capacitor cancels each other, or

$$\frac{1}{2\pi f_0 L_p} = 2\pi f_0 C_p \quad (2.8)$$

If the susceptance of the active circuit is ignored, the oscillation frequency  $f_0$  is given by the above resonant condition:

$$f_0 = \frac{1}{2\pi \sqrt{L_p C_p}} \quad (2.9)$$

For VCOs whose frequencies can be tuned, variable capacitors are usually implemented instead of fixed capacitors. The tuning ability of a VCO is determined by the ratio of maximum and minimum capacitance achievable from the variable capacitor. Replacing  $C$  in Equation 2.9 with the maximum capacitance  $C_{max}$  and the minimum capacitance  $C_{min}$ , the tuning range of the VCO can be found to be:

$$f_{ratio} = \frac{f_{max}}{f_{min}} = \sqrt{\frac{C_{min}}{C_{max}}} \quad (2.10)$$

## 2.2 Quality Factor ( $Q$ )

The quality factor ( $Q$ ) is one of the most important descriptive parameter used in resonant systems. The fundamental definition of  $Q$  is as follows:

$$Q \equiv \omega \frac{\text{energy stored}}{\text{average power dissipated}} \quad (2.11)$$

This definition applies to both resonant and non-resonant systems, and both to electrical and mechanical systems.

Consider a parallel RLC circuit driven by a current source as shown in Figure 2.3. At resonant frequency  $\omega_0$ , the energy stored in the resonant circuit,  $E$ , which is equal to the peak energy stored in the capacitor, is given by

$$E = \frac{1}{2}C(I_{pk}R)^2. \quad (2.12)$$

and average power dissipated in the resistor  $P_{avg}$  is given by

$$P_{avg} = \frac{1}{2}I_{pk}^2R. \quad (2.13)$$

The  $Q$ -factor of the network at resonance is then

$$Q = \omega_0 \frac{E}{P_{avg}} = \frac{1}{\sqrt{LC}} \frac{\frac{1}{2}C(I_{pk}R)^2}{\frac{1}{2}I_{pk}^2R} = \frac{R}{\sqrt{L/C}}. \quad (2.14)$$

Since in the frequency response, the centre frequency  $\omega_0 = 1/\sqrt{LC}$  and the 3 dB power bandwidth  $BW_{3dB} = 1/RC$ ,  $Q$  can also be expressed as

$$Q = \frac{\omega_0}{BW_{3dB}}. \quad (2.15)$$

$Q$  equals the ratio of the resonant frequency to the 3 dB bandwidth. The greater the  $Q$  is, the sharper and more frequency selective the frequency response is. Therefore,  $Q$ -factor represents the quality of the resonance circuit.

For a series RLC network,  $Q$ -factor at  $\omega_0$  can be derived as

$$Q = \frac{\sqrt{L/C}}{R} \quad (2.16)$$

For a single inductor or capacitor, the  $Q$ -factor is frequency dependent. By the definition shown in Equation 2.11,  $Q$  for inductor or capacitor is the ratio of

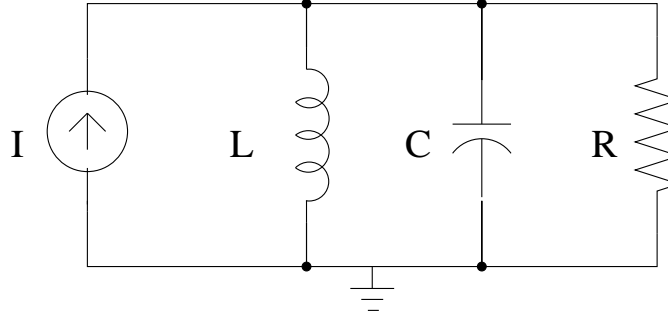


Figure 2.3: Second Order Parallel Resonator

the reactance to the equivalent parasitic series resistance at a particular frequency. Thus, for inductors and capacitors, reducing the equivalent parasitic resistance will improve their  $Q$ -factors.

### 2.3 Phase Noise

Phase noise is an important parameter in oscillators. It describes the short term random frequency fluctuations of a signal. Frequency stability is a measure of the degree to which an oscillator maintains the same value of frequency over a given time. Phase noise reduces this stability. The phase noise in the radio receiver local oscillator limits immunity against nearby interference signals and accurate timing recovery. Phase noise in the transmitter may even overwhelm nearby weak channels. In the receiver, phase noise may downconvert nearby channels onto the desired intermediate frequency (IF).

Consider the situation for a receiver, as shown by the power spectral densities in Figure 2.4. The local oscillator (LO) used for downconverting the RF signal has a noisy spectrum (shaded area). The received RF signal has an interfering signal with large power beside the desired signal with small power at adjacent frequency. After mixing with the LO, the noise from the LO will appear both around the desired signal and interfering signal in the downconverted spectrum, and form overlapping spectra. The wanted signal suffers from significant noise due to the interferer, and the signal-to noise ratio is degraded [23, 24]. In order to detect the desired signals

with large interferers presented, stringent phase noise specifications must be met in wireless communication systems.

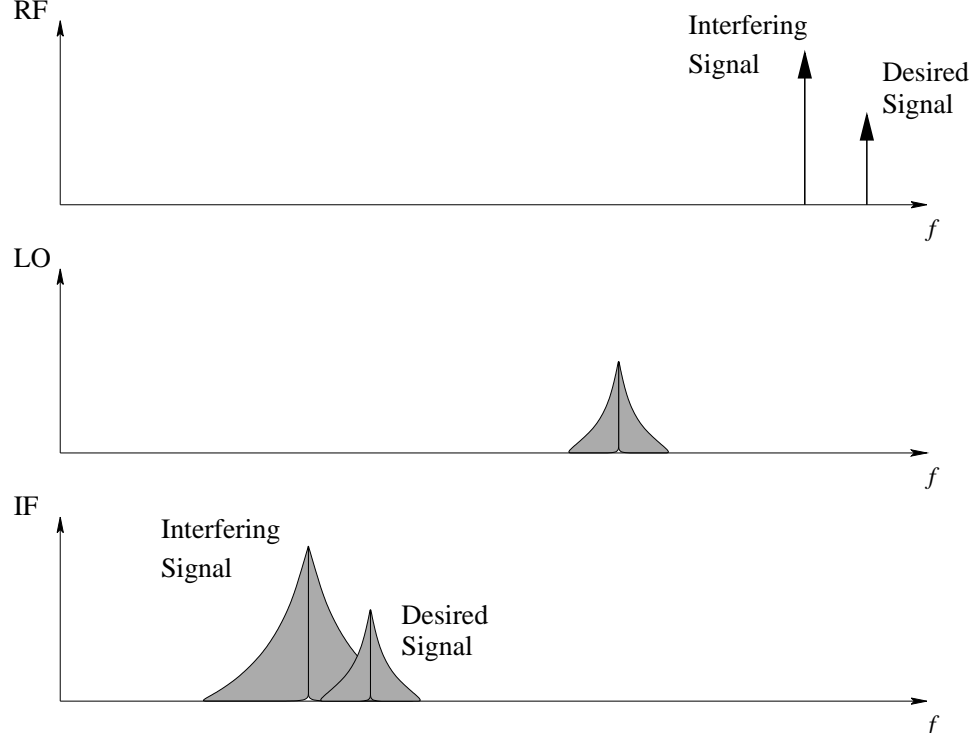


Figure 2.4: Effect of Oscillator Phase Noise

### 2.3.1 Definition

A sinusoidal signal with random phase fluctuation can be represented by

$$v(t) = v_s \sin[2\pi f_0 t + \Delta\phi(t)] \quad (2.17)$$

where  $\Delta\phi(t)$  represents the phase fluctuations. In the time domain, this can be observed as fluctuations of the zero crossings of the original signal, as shown in Figure 2.5.

Since frequency and phase are related by:

$$f(t) = f_0 + \frac{1}{2\pi} \frac{d\phi(t)}{dt} \quad (2.18)$$

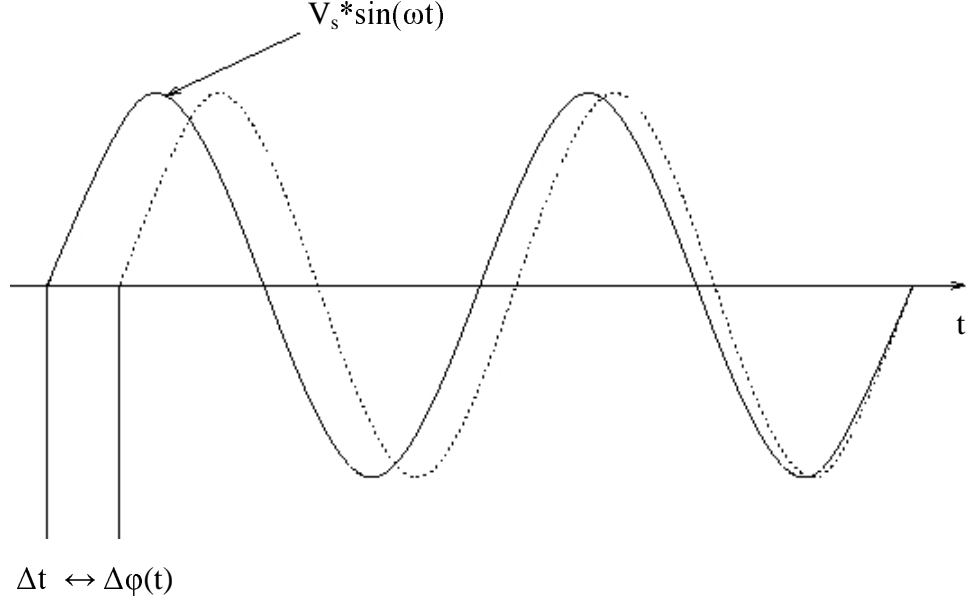


Figure 2.5: Sine Wave with Phase Fluctuation

phase fluctuations, with respect to time, are also an indication of frequency fluctuations with respect to time.

One of the most common fundamental descriptions of phase noise is the one sided spectral density of phase fluctuations per unit bandwidth. The term spectral density describes the power distributions as a continuous function, expressed in units of power per unit bandwidth. The phase noise of an oscillator is described in the frequency domain where the spectral density is characterized by measuring the noise sidebands on either side of the output signal centre frequency. Single sideband phase noise is specified in dBc/Hz at a given frequency offset from the carrier.

The National Bureau of Standards defines single sideband phase noise  $L(\Delta f)$  as the ratio of power in one phase modulation sideband per Hertz bandwidth, at an offset  $\Delta f$  Hz away from the carrier, to the total signal power, as shown in Figure 2.6, in which  $P_S$  is the carrier power and  $P_{SSB}$  is the sideband power in 1 Hz bandwidth at an offset frequency of  $\Delta f$  from the centre.

$$L(\Delta f) = 10 \log \left( \frac{P_{SSB}}{P_S} \right) \text{ dBc/Hz @ } \Delta f \text{ Hz} \quad (2.19)$$

The phase noise generated by a VCO is determined by the  $Q$ -factor of the res-

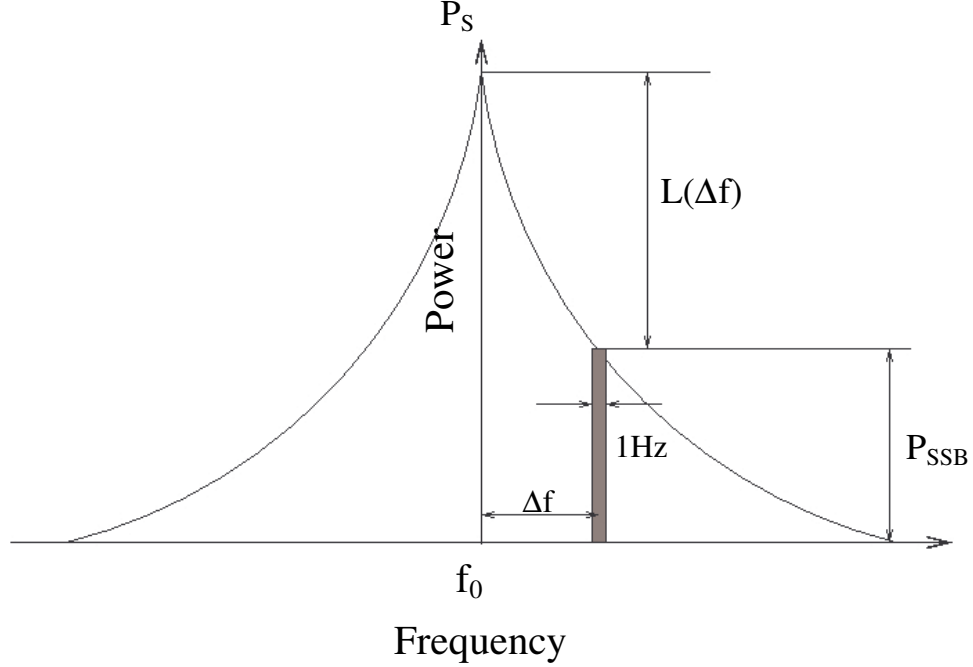


Figure 2.6: Single Sideband Phase Noise to Carrier Ratio

onator, the active transistor device used for the oscillator, the power supply noise, and the external tuning voltage supply noise. The later two noise sources can be minimized by careful choice of the power supplies. Therefore, designing a low phase noise VCO primarily involves implementing a high  $Q$  resonator and carefully operating the oscillator active devices at low phase noise bias points.

Leeson was the first to propose a simple intuitive model [25] relating to the level of phase noise in a widely used class of resonator-based oscillators in 1966. Later, different quantitative models have been established to explain the cause of phase noise, each of which focuses on different noise sources [26].

### 2.3.2 Leeson's Phase Noise Model

Consider an ideal oscillator, whose only noise source is the white thermal noise of the RLC resonant tank resistance. The current noise mean-square spectral density is

$$\frac{\overline{i_n^2}}{B} = 4kTG \quad (2.20)$$

where  $B$  is the bandwidth,  $k$  is the Boltzmann's constant,  $T$  is the temperature in degrees Kelvin, and  $G$  is the tank conductance.

This current noise can be converted to voltage noise when multiplied by the effective impedance, which is simply a perfectly lossless LC network as the energy restoration elements contribute a negative conductance that precisely cancels the positive conductance ( $G$ ) of the tank.

For small displacements  $\Delta f$  from the resonant frequency  $f_0$ , the impedance of the oscillating tank can be calculated as followed:

$$\begin{aligned} Z(f_0 + \Delta f) &= [j(\omega_0 + \Delta\omega)C + \frac{1}{j(\omega_0 + \Delta\omega)L}]^{-1} \\ &= \frac{j(\omega_0 + \Delta\omega)L}{1 - (\omega_0^2 + 2\omega_0\Delta\omega + \Delta\omega^2)LC} \end{aligned} \quad (2.21)$$

Since  $LC = 1/\omega_0^2$  and  $\omega_0 \gg \Delta\omega$ , the impedance can be further approximated by

$$Z(f_0 + \Delta f) = -\frac{j(\omega_0 + \Delta\omega)L}{2\frac{\Delta\omega}{\omega_0} + (\frac{\Delta\omega}{\omega_0})^2} \approx -j\frac{\omega_0 L}{2(\Delta\omega/\omega_0)} = -j\frac{\pi f_0 L}{\Delta f/f_0} \quad (2.22)$$

By introducing the expression of the unloaded tank  $Q$ , where

$$Q = \frac{R}{2\pi f_0 L} = \frac{1}{2\pi f_0 L G} \quad (2.23)$$

$L$  can be substituted and the magnitude of the tank impedance can be written as

$$|Z(f_0 + \Delta f)| \approx \frac{1}{G} \frac{f_0}{2Q\Delta f}. \quad (2.24)$$

Thus, for a small offset frequency, the spectral density of the mean-square noise voltage can be written as

$$\frac{\overline{v_n^2}}{B} = \frac{\overline{i_n^2}}{B} \cdot |Z|^2 = 4kTR \left( \frac{f_0}{2Q\Delta f} \right)^2 \quad (2.25)$$

The noise power in a 1 Hz bandwidth is

$$P_n = \frac{\overline{v_n^2}}{BR} = 4kT \left( \frac{f_0}{2Q\Delta f} \right)^2. \quad (2.26)$$

The above expression includes the noise effects in both amplitude and phase. The equipartition theorem of thermodynamics states that, in equilibrium, the noise

power distributes evenly among each of the quadratic degrees of freedom [27], in this case, amplitude and phase. Therefore, in the absence of amplitude limiting, the noise affecting phase is half of Equation 2.25.

Normalizing the noise voltage density to the mean-square carrier voltage  $v_s$ , where

$$P_S = \frac{\overline{v_s^2}}{R}, \quad (2.27)$$

the phase noise is obtained as

$$L(\Delta f) = 10 \log \left[ \frac{2kT}{P_S} \cdot \left( \frac{f_0}{2Q\Delta f} \right)^2 \right] \quad (2.28)$$

This shows that the phase noise is inversely proportional to the square of the resonator  $Q$ . That is why improving resonator  $Q$  is critical in VCO design.

The phase noise predicted using Equation 2.28 considers only the thermal noise from the resonator. There are other important noise sources, which cause the measured phase noise to be greater. The predicted noise continues to drop quadratically, while in real cases, phase noise spectra always exhibits a noise floor (noise does not drop with increasing of frequency offset) at large frequency offsets. Such a noise floor may be due to the noise associated with active elements and impossible to eliminate. Also, there is a  $1/f^3$  region at small offset frequencies. Thus, Leeson developed a more involved equation which considers some of these factors:

$$L(\Delta f) = 10 \log \left\{ \frac{2FkT}{P_S} \cdot \left[ 1 + \left( \frac{f_0}{2Q\Delta f} \right)^2 \right] \cdot \left( 1 + \frac{f_{1/f^3}}{\Delta f} \right) \right\} \quad (2.29)$$

This equation, known as Leeson's Equation, consists of three modifications to Equation 2.28. A factor  $F$  (often called the "device excess noise number") is introduced to account for the noise in addition to thermal noise in the  $1/f^2$  region. An additive unity factor (inside the square brackets) accounts for the noise floor. A multiplicative factor (the last part of the equation) provides a  $1/f^3$  behavior at small offset frequencies. Figure 2.7 shows a typical phase noise Bode plot described by Leeson's Equation.

There are a few problems limiting the predictive power of Leeson's model. The factor  $F$  is an empirical fitting parameter, which must be determined from mea-

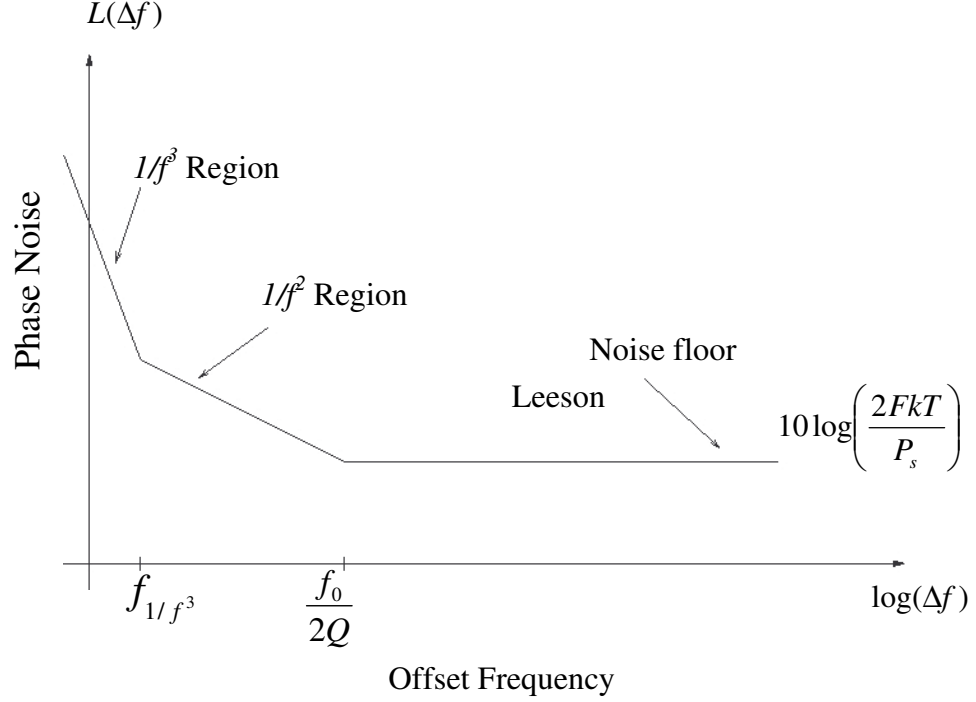


Figure 2.7: Phase Noise in Leeson's Model

surements. Although  $f_1/f^3$ , the boundary between the  $1/f^2$  and  $1/f^3$  regions, is asserted to equal to the  $1/f$  corner frequency of the device (the frequency below which flicker noise dominates and above which thermal noise dominates), measurements often disagree, and thus has to be treated as an empirical fitting parameter as well. Finally, the frequency at which the noise becomes constant is not always equal to  $f_0/2Q$ .

### 2.3.3 LTV Phase Noise Model

Leeson's phase noise model treats the oscillator as a linear, time-invariant (LTI) system. However, this assumption does not always hold true, and is addressed by Hajimiri and Lee's LTV phase noise model.

Oscillators are fundamentally nonlinear, as amplitude limiting is necessary. However, amplitude-control nonlinearity affects phase noise only incidentally, by controlling the detailed shape of the output waveform. Disturbances are always much smaller in magnitude than the carrier in oscillators. Thus, linearity would be a

reasonable assumption if the noise-to-phase transfer function is concerned.

The assumption of time-invariance fails to hold for oscillator phase noise analysis. This can be shown by considering how an impulse affects the waveform of an oscillator. As shown in Figure 2.8, the oscillator system responds differently to the impulses injected into the system at different times. If the impulse occurs at a voltage maximum of the sinewave, the amplitude increases but the timing of the zero crossings does not change. On the other hand, if the impulse is injected in at some other time, both amplitude and zero crossing timing of the oscillation are affected. Since zero crossing timing is a measure of phase, one may conclude that the phase disturbance of an injected impulse depends on when the injection occurs. Thus, an oscillator is a periodically time-varying system. Hajimiri and Lee modeled phase noise theory in a linear, time-varying (LTV) system [28].

To study the time-varying nature of the oscillator, first the impulse response at time  $\tau$  for excess phase is defined.

$$h_\phi(t, \tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t - \tau) \quad (2.30)$$

where  $u(t)$  is the unit step function, and  $q_{max}$  is the maximum charge displacement across the capacitor on the node, which makes the function  $\Gamma(x)$  independent of signal amplitude.  $\Gamma(x)$  is called the impulse sensitivity function (ISF) periodic in  $2\pi$ . It describes how much phase shift results from the impulse.  $\Gamma(x)$  is a function of the waveform. In general, it is practical to determine  $\Gamma(x)$  through simulation. But there are also analytical methods for special cases [23, 29].

Consider the excess phase  $\phi(t)$  as the superposition of impulse response for all  $\tau$  values, one can compute the excess phase by superposition integral as

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t, \tau) i(\tau) d\tau = \frac{1}{q_{max}} \int_{-\infty}^t \Gamma(\omega_0\tau) i(\tau) d\tau \quad (2.31)$$

Since the ISF is periodic, it can be expressed as a Fourier series

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau + \theta_n) \quad (2.32)$$

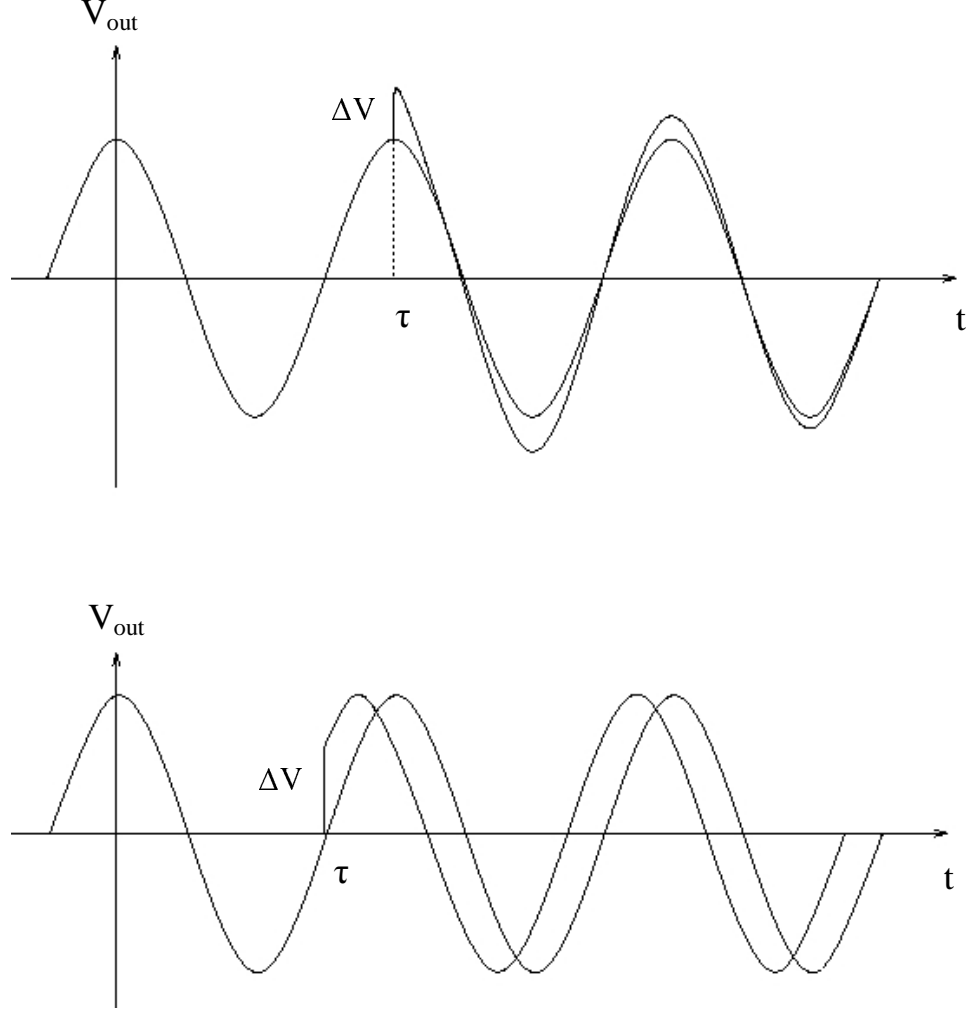


Figure 2.8: Impulse Responses of Oscillator

where the coefficients  $c_n$  are real, and  $\theta_n$  is the phase of the  $n$ th harmonic of the ISF.  $\theta_n$  can be ignored assuming that noise components are uncorrelated and thus, their relative phase is irrelevant.

Substituting the Fourier expansion into the superposition integral gives:

$$\phi(t) = \frac{1}{q_{max}} \left[ \frac{c_0}{2} \int_{-\infty}^t i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^t i(\tau) \cos(n\omega_0\tau) d\tau \right] \quad (2.33)$$

Equation 2.33 allows computation of excess phase caused by an arbitrary noise current injected into the system, once the Fourier coefficients of the ISF have been found.

The fact that the system is not LTI implies that noise injected into the system

at some frequency may produce spectrum at different frequencies. This property is demonstrated below.

Consider injecting a current whose frequency is close to an integer multiple  $m$  of the oscillation frequency,

$$i(t) = I_m \cos[(m\omega_0 + \Delta\omega)t] \quad (2.34)$$

where  $\Delta\omega \ll \omega_0$ . Substituting into Equation 2.33 gives:

$$\begin{aligned} \phi(t) = \frac{c_0}{2q_{max}} \int_{-\infty}^t I_m \cos[(m\omega_0 + \Delta\omega)t] d\tau \\ + \frac{1}{q_{max}} \sum_{n=1}^{\infty} c_n \int_{-\infty}^t I_m \cos[(m\omega_0 + \Delta\omega)\tau] \cos(n\omega_0\tau) d\tau \end{aligned} \quad (2.35)$$

Equation 2.35 can be considerably simplified. Since  $\Delta\omega \ll \omega_0$ , and each integral in the equation has the following form:

$$\begin{aligned} c_n \int_{-\infty}^t I_m \cos[(m\omega_0 + \Delta\omega)\tau] \cos(n\omega_0\tau) d\tau \\ = \frac{I_m c_n}{2} \left[ \frac{\sin(m\omega_0 + n\omega_0 + \Delta\omega)\tau}{m\omega_0 + n\omega_0 + \Delta\omega} + \frac{\sin(m\omega_0 - n\omega_0 + \Delta\omega)\tau}{m\omega_0 - n\omega_0 + \Delta\omega} \right], \end{aligned} \quad (2.36)$$

the contribution by terms other than when  $n = m$  are negligible. Equation 2.35 thus collapses to the following approximation:

$$\phi(t) \approx \frac{I_m c_m \sin(\Delta\omega t)}{2q_{max} \Delta\omega} \quad (2.37)$$

This shows that the injection occurs near an integer multiple of  $\omega_0$  will be converted into excess phase at  $\pm\Delta\omega$ .

Equation 2.37 shows how much phase error results from a given current  $i(t)$ . To find the spectrum of the output voltage, the phase error must be converted to voltage. To obtain the sideband power around the fundamental frequency, the output may be approximated as a sinusoid, so that  $v_{out} = \cos[\omega_0 t + \phi(t)]$ . This equation may be considered as a phase-to-voltage converter. This conversion is nonlinear [28].

Performing this phase-to-voltage conversion, one can see that a current injected at frequency  $m\omega_0 + \Delta\omega$  results in a pair of equal sidebands at  $\omega_0 \pm \Delta\omega$  with a sideband power with respect to the carrier given by

$$P_{SBC}(\Delta\omega) = 10 \log \left( \frac{I_m c_m}{4q_{max} \Delta\omega} \right)^2 \quad (2.38)$$

Equation 2.38 implies both upward and downward frequency translations of noise, as shown in Figure 2.9. Noise near DC is up-converted, so  $1/f$  device noise becomes  $1/f^3$  noise near the carrier. Noise near the carrier remains the same frequency. White noise near higher integer multiplies of the carrier down-converts and turns into noise in the  $1/f^2$  region.

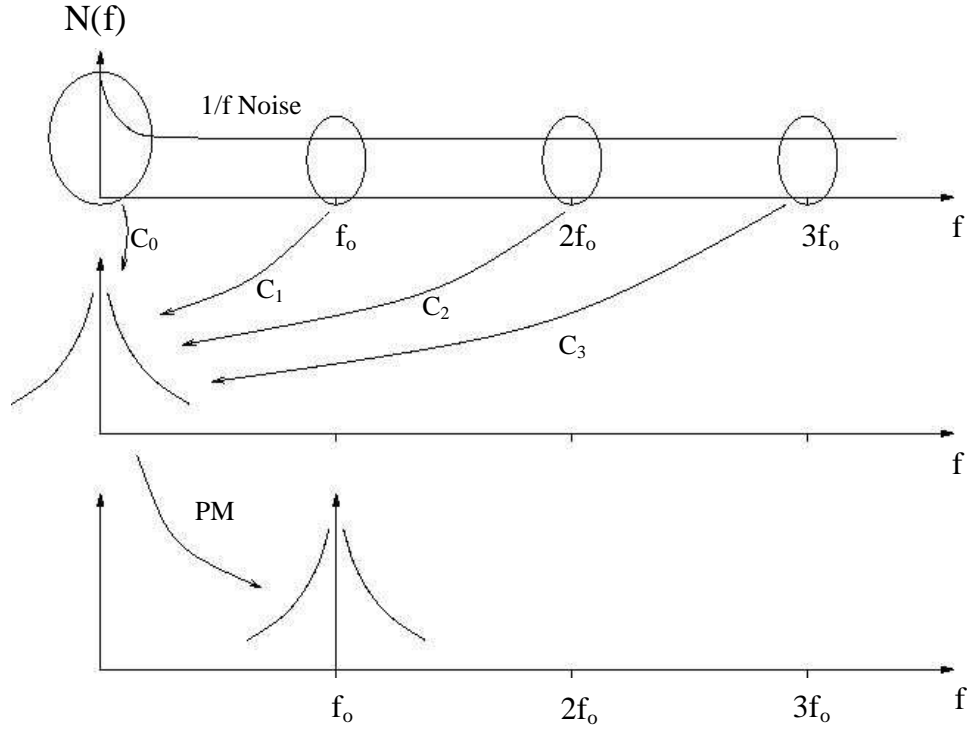


Figure 2.9: Evolution of Circuit Noise into Phase Noise

Consider in particular the phase noise contribution by the white thermal noise, whose spectral density is  $\overline{i_n^2}/\Delta f$ .  $I_m$  in Equation 2.38 represents the peak amplitude,  $\overline{i_n^2}/\Delta f = I_m^2/2$  for  $\Delta f = 1$  Hz. Thus, the phase noise at an offset frequency of  $\Delta\omega$

is given by

$$L(\Delta\omega) = 10 \log \left( \frac{\frac{\overline{i_n^2}}{\Delta f} \sum_{m=0}^{\infty} c_m^2}{4q_{max}^2 \Delta\omega^2} \right) \quad (2.39)$$

According to Parseval's theorem,

$$\sum_{m=0}^{\infty} c_m^2 = \frac{1}{\pi} \int_0^{2\pi} |\Gamma(x)|^2 dx = 2\Gamma_{rms}^2, \quad (2.40)$$

which gives a result

$$L(\Delta\omega) = 10 \log \left( \frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{2\Delta\omega^2} \right) \quad (2.41)$$

This is the rigorous equation for the  $1/f^2$  region, similar to Leeson's model, but with no empirical curve-fitting parameters.

### 2.3.4 Figure of Merit

To compare the performance of different VCOs implemented with different technologies, the phase noise is normalized into a figure of merit (FOM) [15,18], defined as:

$$FOM = 10 \log \left[ L(\Delta f) \left( \frac{\Delta f}{f_0} \right)^2 P_{VCO} \right] \quad (2.42)$$

where  $L(\Delta f)$  is the single sideband noise (linear) at offset frequency  $\Delta f$  from the centre frequency  $f_0$ .  $P_{VCO}$  denotes the total power consumption of the VCO in mW. FOM generates a comparable value system from which different oscillators can be evaluated. The performance of a VCO is regarded to be better with higher absolute value of FOM. This quantity is biased towards monolithic CMOS designs, whose power consumption is minimized. For other device comparison, such as GaAs (Gallium Arsenide), the expression can be modified to concern more on power consumption.

### **3. VCO Design**

The goal of this research is developing a CMOS VCO circuit as a platform to integrate LIGA-MEMS capacitor to CMOS circuit and to evaluate its performance. The VCO design should provide a reasonably fair performance comparison environment for the LIGA-MEMS capacitor and the conventional CMOS varactor. Thus, the VCO design should be able to either use an on-chip CMOS varactor, or integrate with an off-chip LIGA-MEMS capacitor as a resonator component. Any effects in the VCO performance, which would be introduced by the integration, should be considered in the design so that the difference in the VCO performance merely reflects the advantage (or disadvantage) of the LIGA-MEMS capacitor over the on-chip varactor.

#### **3.1 Design Issues**

In this section, various design issues, including choice of fabrication technologies, design topologies and approaches are discussed.

##### **3.1.1 CMOS Fabrication Technologies**

CMOS technology has become the most popular technology in IC designs, especially for digital circuits. CMOS is the ideal technology to realize system-on-chip (SOC) solutions for complex circuits and systems. Thus, research in analog, mixed-signal, and RF circuits focuses on CMOS technology as well, so that the circuits benefit from better compatibility with other circuits and systems.

CMOS technology is continuously advancing by shrinking the size of the transistors. This leads to smaller circuit size, faster response, higher operating frequencies, and in the case of digital circuits, greater calculation capability. Many

different CMOS fabrication standards are available, from 0.8 micron to the newest 65 nanometre. Among the different CMOS fabrication standards available, TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 micron is a good choice in terms of performance and technology maturity. TSMC 0.18 micron is not the newest technology in fabrication, but it is an advanced mainstream technology. It features a high degree of process stability and runs on the foundry industry's largest available capacity that provides consistent support. TSMC 0.18 micron process technology provides a good combination of density, speed and power to serve a broad range of computing, communications and consumer electronics applications. This technology supports features such as deep N-well, multiple threshold voltage devices, and MIM (metal-insulator-metal) capacitor. Also, models, design kit, cell libraries, verification technology files, and technical support are well provided. It has been proven to be a mature technology for RFIC designs [20, 30, 31].

### 3.1.2 Oscillator Design Approaches

There are various approaches to design an oscillator. Traditionally, these approaches are classified either as small-signal (linear) with emphasis on start-up conditions, or large-signal (nonlinear) with emphasis on steady-state conditions.

Small-signal design approaches focus on obtaining active device scattering parameters (S-parameters) to satisfy oscillation conditions. This type of design approaches is relatively simple since device S-parameters are usually readily available. However, small-signal design approaches often suffer from inaccuracy in estimating oscillation performance, such as oscillation frequency, output power, and phase noise [32–34].

Large-signal design approaches, on the other hand, focus on predicting the correct steady-state oscillation frequency and power levels. Different methods have been presented. Some characterize the active devices as an amplifier and derive the oscillator power from input and output power of the amplifier [35]. Some estimate the saturation gain or large signal behavior based on small signal S-parameters [36, 37]. Some use a “Device Line” technique, which measures the impedance when

the device saturates and therefore utilize the large signal behaviors [38]. Large-signal design approaches usually have difficulties deriving nonlinear models for devices, and sometimes experience problems in oscillation start-up.

With the advancement of computer aided design (CAD) tools, oscillator design is taking a new approach. CAD tools are able to simulate a variety of results, such as oscillation frequency, power, phase noise, stability, and harmonic distortion. CAD tools can use different simulation technologies, such as DC simulation, AC and S-parameter simulations, transient time-domain simulation, and Harmonic Balance (HB) simulation, to ensure oscillation conditions in different aspects. The CAD approach makes oscillator design more systematic and focused. However, it is worth noting that CAD tools can only be as accurate as the models used in the simulation.

### 3.1.3 Oscillator Topologies

LC-tuned oscillators can be realized with different topologies. Figure 3.1 shows the AC model of two classic configurations common at lower frequencies, the Colpitts oscillator and Hartley oscillator (bias details are not shown). Both configurations utilize a parallel LC circuit between the collector and the base of a BJT (bipolar junction transistor), or between the drain and the gate of a FET (field effect transistor). These configurations can be realized with only one transistor and thus exhibit great simplicity.

To analyze the Colpitts oscillator, the passive components can be simplified and re-modeled in a negative resistance configuration, as shown in Figure 3.2, with the assumption that impedances of the capacitors are less than the load resistance at resonant frequency.

Figure 3.2 (a) is an AC model of the Colpitts oscillator shown in Figure 3.1 (a). The resistance  $R_L$  represents the load, the transistor output resistance, and the loss in the tank. The transistor can be modeled by a large-signal gate-source resistance  $1/G_m$ , and a current source  $G_m V_1$ , where  $G_m$  is the large-signal transconductance of the transistor, as shown in Figure 3.2 (b). The capacitive voltage divider  $C_1$  and  $C_2$  can be modeled as an ideal transformer, as shown in Figure 3.2 (c). The equivalent

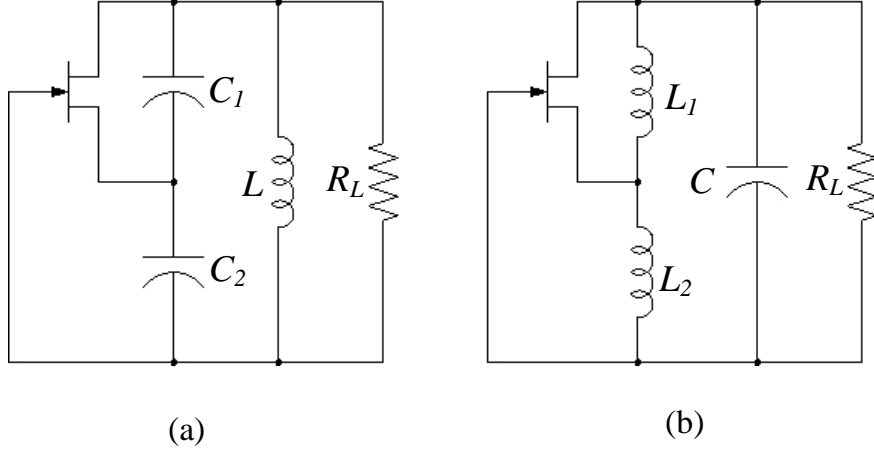


Figure 3.1: Two Common Oscillator Configurations: (a) Colpitts and (b) Hartley

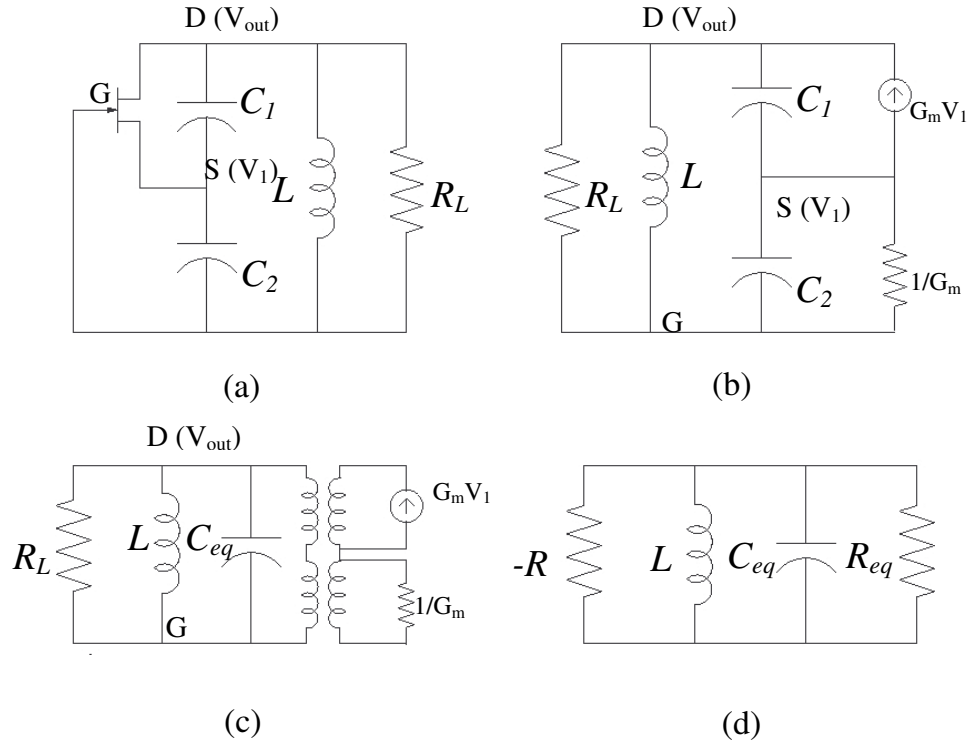


Figure 3.2: Modeling Colpitts Oscillator: (a) Oscillator Circuit AC Model. (b) Modeling Transistor. (c) Modeling Transformer. (d) Simplified Model.

turns ratio is determined by the voltage-divider:

$$N = \frac{C_1}{C_1 + C_2}. \quad (3.1)$$

The relationship between  $V_{out}$  and  $V_1$  is also determined by the capacitor divider:

$$V_1 = NV_{out}. \quad (3.2)$$

Using the turns ratio to convert the resistance looking through the transformer, the Colpitts oscillator can be simplified into an  $RLC$  tank with the transistor modeled as a negative resistor, as shown in Figure 3.2 (d). In this simplified model, the equivalent capacitance is the series combination of the two capacitors:

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}. \quad (3.3)$$

The equivalent resistance is the parallel combination of the load resistance  $R_L$  and large-signal gate-source resistance looking through the capacitive transformer:

$$R_{eq} = R_L \parallel \frac{1}{N^2 G_m}. \quad (3.4)$$

The negative resistance is determined by the voltage-current relationship of the current source in the transistor model, looking through the transformer:

$$-R = \frac{V_{out} - V_1}{-G_m V_1} \frac{1}{(1 - N)^2} = -\frac{1}{N(1 - N)G_m}. \quad (3.5)$$

Thus, neglecting the transistor parasitics, the oscillation frequency of the Colpitts oscillator can be expressed as followed:

$$\omega_o = \frac{1}{\sqrt{LC_{eq}}} = \frac{1}{\sqrt{L \left( \frac{C_1 C_2}{C_1 + C_2} \right)}}. \quad (3.6)$$

Similar analysis can be applied to the Hartley oscillator, and its oscillation frequency is:

$$\omega_o = \frac{1}{\sqrt{(L_1 + L_2)C}}. \quad (3.7)$$

Colpitts and Hartley oscillators have good noise properties and thus potentially lower phase noise. They also achieve high voltage swing for a given bias current and resonator  $Q$  [23]. However, these configurations are rarely used in CMOS integrated circuits. This is because of the high gain required for a reliable start-up condition

and the single-ended nature, which makes them sensitive to common-mode noise sources, such as substrate and power supply noise. Recent research shows that a differential Colpitts VCO topology can overcome these shortcomings [19].

Another popular topology is the cross-coupled oscillator. Cross-coupled oscillators are easy to implement due to their relaxed start-up condition. They also provide fully differential output which reduces common-mode noise.

Cross-coupled oscillators can be realized with NMOS (N-type metal oxide semiconductor) transistors only, as shown in Figure 3.3(a), or PMOS (P-type metal oxide semiconductor) only, or with both NMOS and PMOS transistors (complementary), as shown in Figure 3.3(b). The NMOS-only configuration is easy to implement, while the complementary version provides larger amplitude swing.

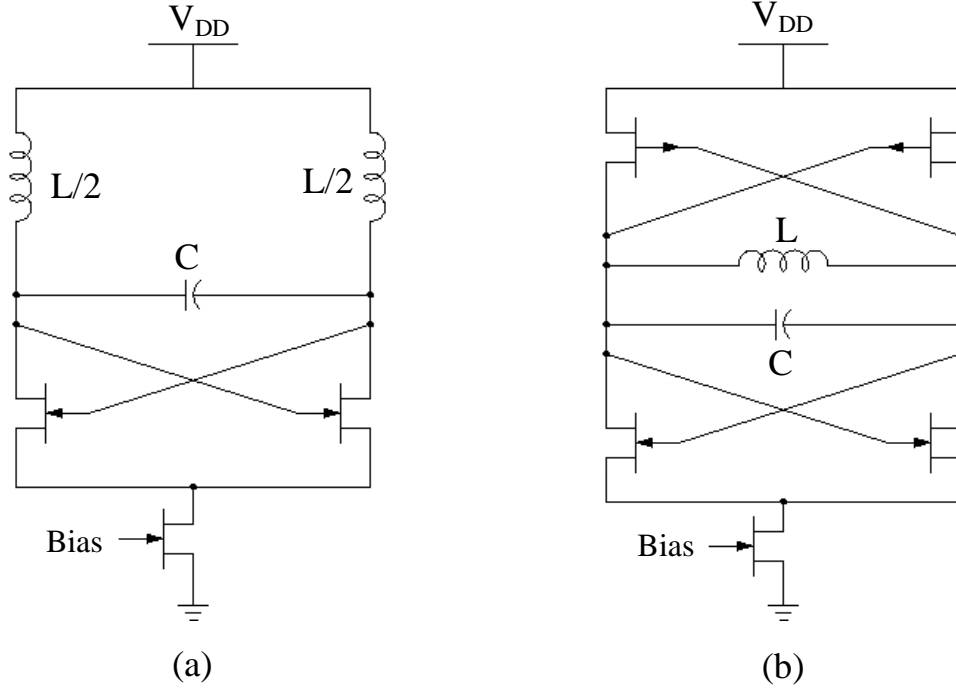


Figure 3.3: (a) NMOS-Only Cross-Coupled Oscillator (b) Complementary Cross-Coupled Oscillator

The cross-coupled transistor pair effectively works as a negative resistance that cancels out the resistance in the non-ideal resonant tank. This can be explained

using the simplified AC large-signal model as shown in Figure 3.4, providing that the two transistors are perfectly matched.

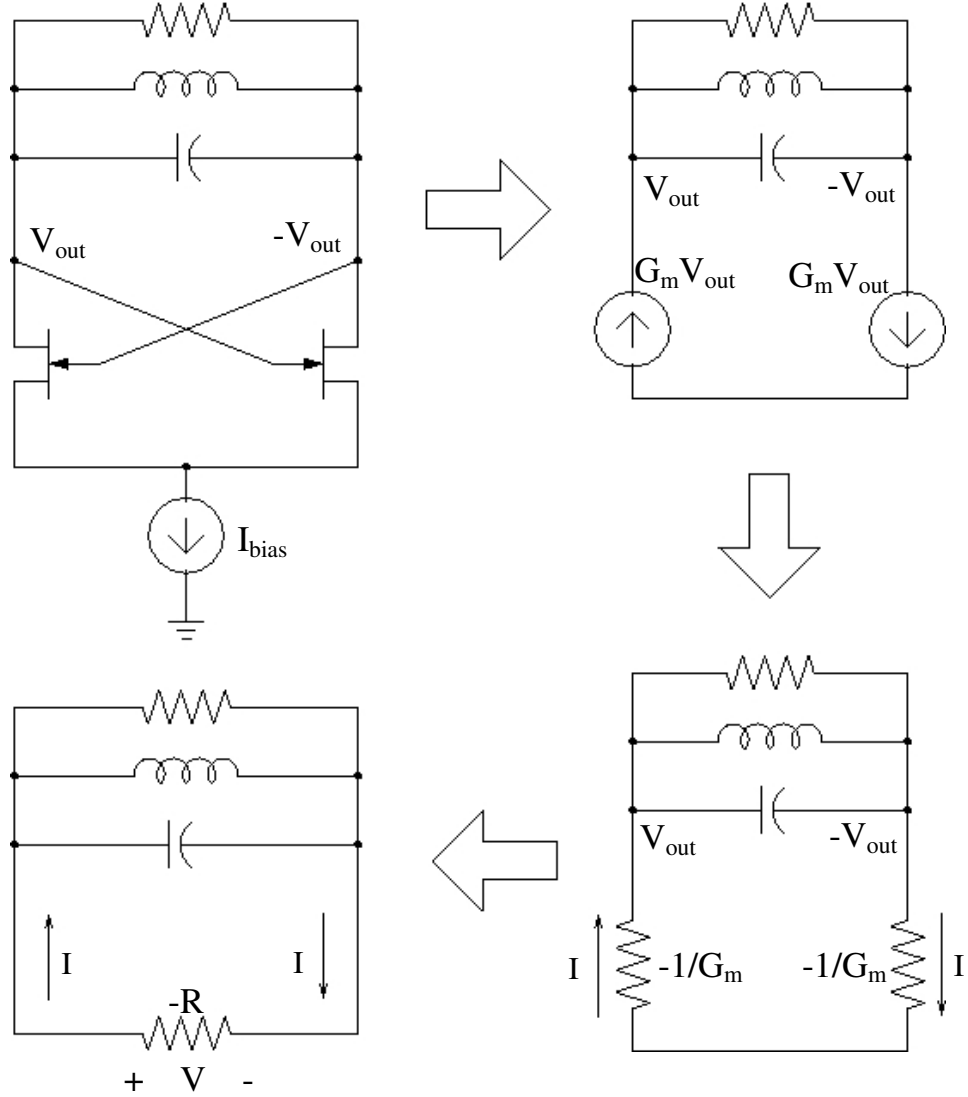


Figure 3.4: Cross-Coupled Negative Resistance

Consider half of the cross-coupled transistor pair. Due to the inverting nature of the transistor stages, the AC voltage at the drains is the negative of that at the gates, while the drain current flows from  $-V_{\text{out}}$  to  $+V_{\text{out}}$  in the differential pair, indicating a negative resistance. By modeling the transistor as a current source  $G_m V_{\text{out}}$ , where  $G_m$  is the large-signal transconductance, the transistor can be calculated to have a

negative resistance of  $-1/G_m$ . Assuming that two transistors are identical, the total negative resistance can be described by

$$R = \frac{-2}{G_m} \quad (3.8)$$

This negative resistance technique is also used in  $Q$ -enhanced LC filters.

### 3.1.4 Resonator Components

A resonator is the frequency selective part of a VCO. An LC resonator is simply an inductor and a capacitor coupled in parallel. For CMOS RFICs, both inductor and capacitor are traditionally realized on-chip. In the CMOS process, a top layer metal trace in spiral shape forms an on-chip spiral inductor. An On-chip capacitor can be realized in various ways. Some use the capacitance between two metal plates, such as the MIM capacitor. Some use the capacitance between different regions of active devices, such as the diode varactor and the MOS varactor. Other types of inductors and capacitors can be used in RFIC, including MEMS passive components. The following section will discuss various inductive and capacitive resonator components.

#### 3.1.4.1 Spiral Inductor

The inductor is one of the most critical components in CMOS RF circuit design as the inductor  $Q$  value can dominate the loss in the resonant tank. CMOS on-chip inductors typically range around a few nanohenries. This makes it normally impractical to implement on-chip inductors at sub-gigahertz frequencies. For gigahertz range frequencies, on-chip inductors have sufficient inductance to allow utilization of these components in CMOS circuits, however, loss becomes an increasing problem with increasing frequency due to parasitics.

##### 3.1.4.1.1 CMOS Spiral Inductor Modeling

A spiral inductor can be built on a silicon substrate using today's mainstream silicon fabrication processes. A minimum of two metal layers is needed to build a basic spiral coil and connect its inner terminal to the outside. The structure of a spiral inductor

can be defined by the number of turns ( $n$ ), the conductor width ( $w$ ) and spacing ( $s$ ), and the area it covers ( $d \times d$ ), as shown in Figure 3.5.

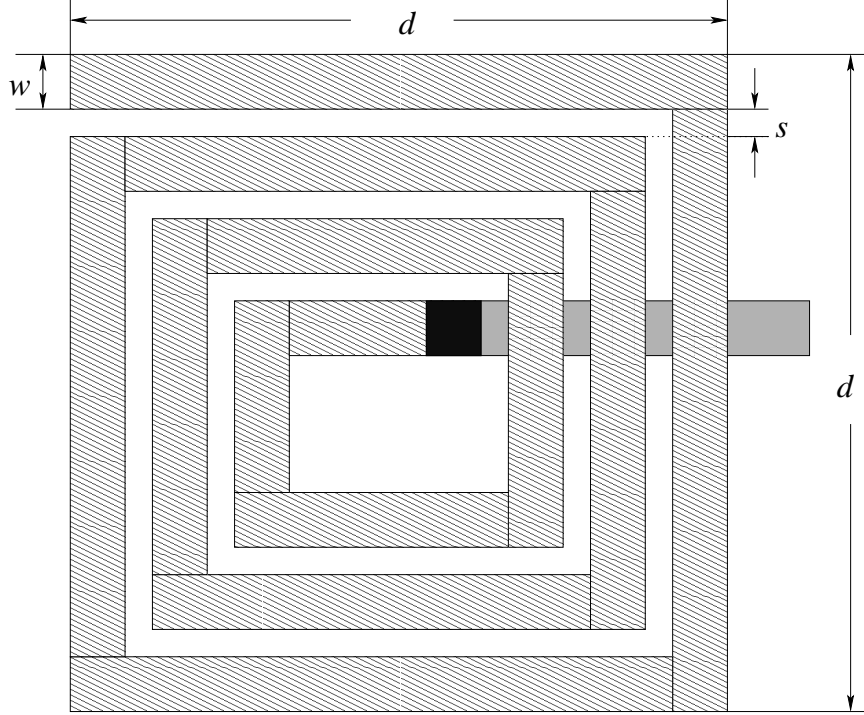


Figure 3.5: A Typical Spiral Inductor Layout

There are three dominating loss mechanisms in on-chip inductors in CMOS processes: the series parasitic resistance of the inductor, the eddy current loss due to the low resistivity lossy silicon substrate, and the capacitive coupling to the conducting substrate [39]. The Ohmic loss of the series parasitic resistance is the most important loss among the three at low frequencies. Thus, a typical CMOS spiral inductor at low frequencies can be modeled as a series combination of an ideal inductance  $L$  and a series resistance  $R_s$ , as shown in Figure 3.6(a). At high frequencies, the other two loss mechanisms become obvious, and the inductor can be modeled as shown in Figure 3.6(b). A capacitance in parallel with the coil ( $C_p$ ) represents the capacitive coupling between the two terminals of the inductor. The oxide capacitors ( $C_{ox}$ ) represent the capacitance between the spiral and the substrate. And finally

there are resistances and capacitances of the silicon substrate ( $R_{sub}$  and  $C_{sub}$ ).

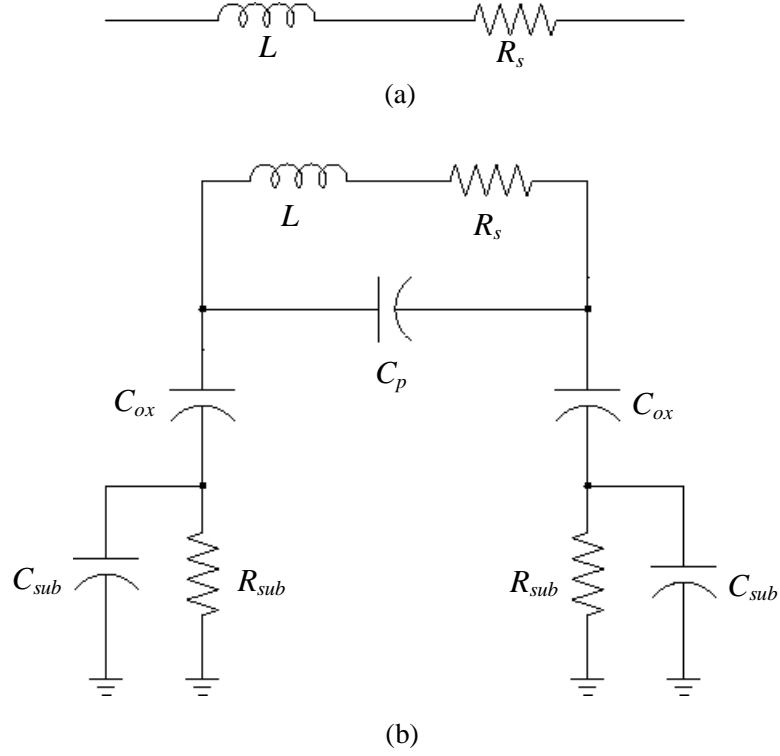


Figure 3.6: Lumped-Element Model of an On-Chip Spiral Inductor: (a) Low Frequency Model and (b) High Frequency Model

The overall inductance of a square spiral  $L$  can be computed accurately by summing the self inductance of each wire segment and the mutual inductance between all possible wire segment pairs, using Grover's formula [40] and Greenhouse's method [41]. The equations for this calculation are complicated and not presented here. The other parameters in the model can be described as followed [42]:

$$R_s = \frac{l}{w\sigma\delta(1 - e^{-t/\sigma})} \quad (3.9)$$

$$C_p = nw^2 \frac{\epsilon_{ox}}{t_{ox}} \quad (3.10)$$

$$C_{ox} = wl \frac{\epsilon_{ox}}{t_{ox}} \quad (3.11)$$

$$R_{sub} = \frac{2}{wlG_{si}} \quad (3.12)$$

$$C_{sub} = \frac{wlC_{si}}{2} \quad (3.13)$$

where  $l$ ,  $w$ ,  $t$  and  $\sigma$  are the total length, width, thickness, and the conductivity of the coil metal respectively,  $\delta$  is the skin depth, which can be calculated as  $\delta = \sqrt{1/\pi f \mu_o \sigma}$  with  $\mu_o$  is the permeability,  $n$  is the number of turns of the coil,  $\epsilon_{ox}$  is the dielectric permittivity of the oxide,  $t_{ox}$  is the oxide thickness between the spiral and the underpass,  $G_{si}$  and  $C_{si}$  are the conductance and capacitance per unit area of the substrate.

The quality factor of the inductor can be approximated using the low frequency model before substrate loss effects contribute.

$$Q = \frac{\omega L}{R_s} \quad (3.14)$$

At higher frequencies, the Q-factor is normally significantly lower [43].

Simulation programs are available to greatly reduce calculation and parameter extraction work for designers. ASITIC (Analysis and Simulation of Spiral Inductors and Transformers for ICs) is a well-established simulation tool [44]. It provides lumped-element models for inductors and other types of passive components and interconnect metal structures. It takes into account skin effects, crowding effects, eddy current losses, and the models are accurate to different fabrication technologies by adapting a mini technology file that describes the substrate and metal layers of the process.

#### 3.1.4.1.2 Design Guidelines for CMOS Spiral Inductors

There are a few guidelines to be considered in design and layout for CMOS spiral inductors.

The top layer of metal is normally used for inductor coils. In CMOS technology, the top metal layer is usually the thickest metal layer, which increases conductance, and is farthest away from the lossy substrate, which reduces parasitics. Small coil width decreases the inductance, which requires longer coil or more turns to compensate. Small width also increases the series resistance, as shown in Equation 3.9. However, large metal width increases the physical size of the inductor, which consumes a large portion of the circuit area. So the width of the coil should only be large enough to reduce the ohmic losses in balance with other losses in the inductor structure. The spacing between turns can be kept reasonably small to greatly save circuit area without sacrificing the self-resonant frequency [45].

CMOS inductors suffer loss due to energy dissipation in the substrate. Isolating the inductor from the substrate can enhance the performance of the inductor. Therefore, patterned ground shield (PGS), as shown in Figure 3.7, using the first layer metal under the inductor can be used, which greatly reduces substrate loss and isolates from substrate noise [42].

#### **3.1.4.2 CMOS Variable Capacitors**

The variable capacitor is an important frequency tuning component in RF IC's. The frequency of the resonator is defined by the value of the inductance and capacitance. Since the inductance value is usually difficult to tune once the physical structure of the inductor is determined, changing the resonator capacitance is the usual way of tuning frequencies. Two types of varactors are usually employed in CMOS technology. One is called junction (or diode) varactor, which uses PN junctions, and the other is called MOS (metal oxide semiconductor) varactor, which uses MOSFETs (metal oxide semiconductor FETs) [46].

Reverse-biased diodes have been the traditional way to realize varactors. They traditionally perform better than MOS varactors in terms of  $Q$ -factor. The varactor capacitance is results from the junction depletion region, as shown in Figure 3.8.

More recent work shows that, with the shrink of transistor size available in advanced fabrication processes, MOS varactor performance can be superior to diode

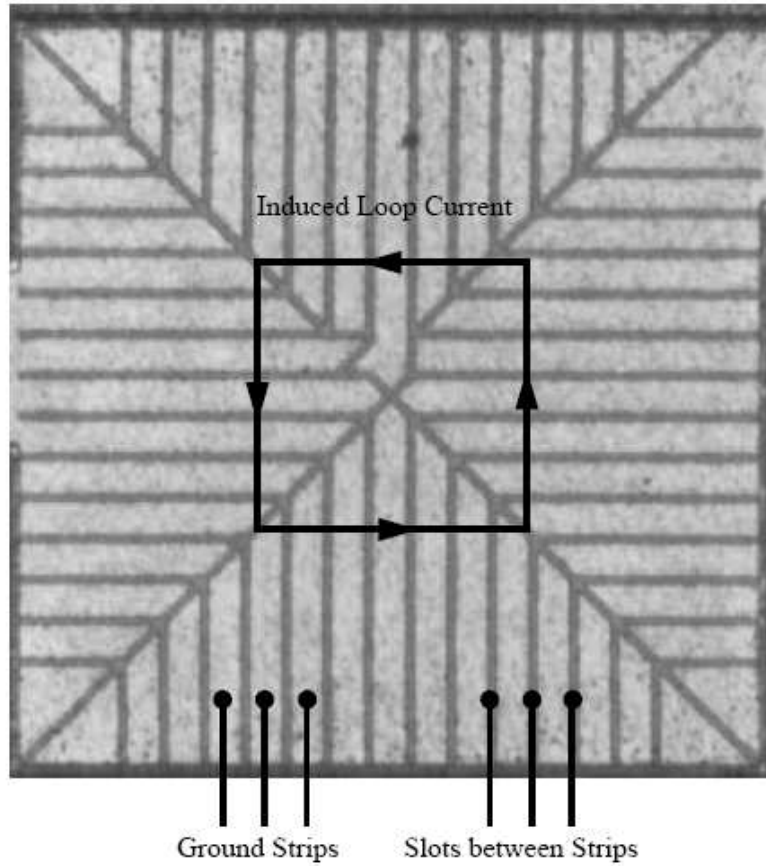


Figure 3.7: Patterned Ground Shield [42]

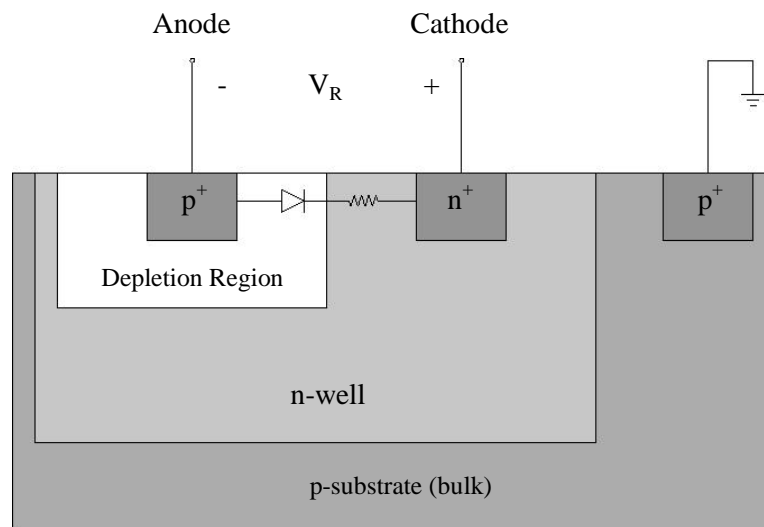


Figure 3.8: PN Junction Varactor

varactors, especially in terms of physical size and power consumption [47].

A MOS transistor with drain, source and bulk (D, S, B) connected together forms a MOS capacitor whose capacitance depends on the voltage between the gate (G) and the bulk. Thus, it can be used as a MOS varactor. Figure 3.9 shows the cross section of a NMOS varactor.

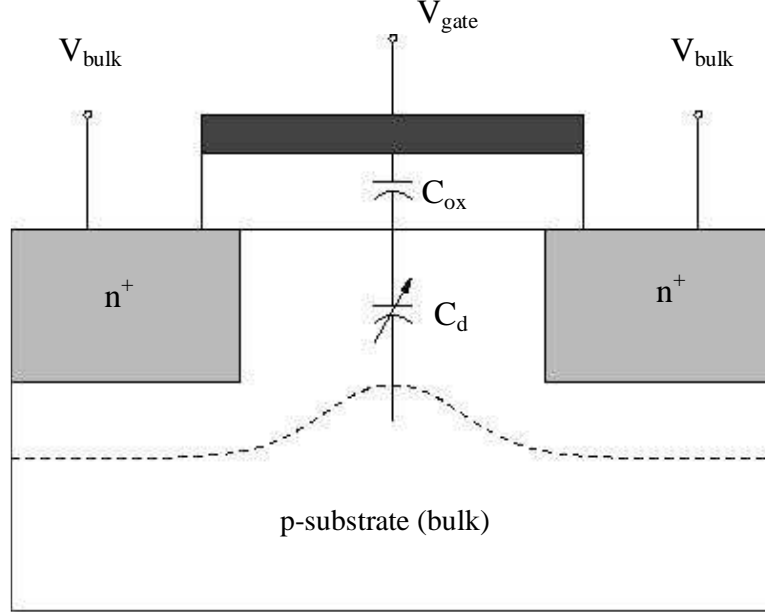


Figure 3.9: NMOS varactor

Depending on the voltage between the gate and the bulk  $V_{GB}$ , the MOS device works in different regions. In the case of an NMOS capacitor, when  $V_{GB}$  is greater than the threshold voltage  $V_t$ , the device is in the strong inversion region and behaves as a transistor. When  $V_{GB}$  is negative, the device is in accumulation region, where the voltage at the interface between the semiconductor and gate oxide is high enough to allow charge carriers to move freely. Thus, in both accumulation region and strong inversion region, the MOS capacitance  $C_{mos}$  is equal to the gate oxide capacitance  $C_{ox}$ , and

$$C_{ox} = \frac{\epsilon_{ox} A}{t_{ox}}, \quad (3.15)$$

where  $\epsilon_{ox}$  is the permittivity of the oxide,  $A$  is the transistor channel area and  $t_{ox}$  is

the oxide thickness.

Between the strong inversion and accumulation region, three more regions can be distinguished: moderate inversion, weak inversion, and depletion. In these regions, there are few mobile charge carriers at the gate oxide interface, which causes a decrease of  $C_{mos}$ . Thus,  $C_{mos}$  can be modeled as the series connection of the gate oxide capacitance  $C_{ox}$  and a variable depletion capacitance  $C_d$ ,

$$\frac{1}{C_{mos}} = \frac{1}{C_{ox}} + \frac{1}{C_d}. \quad (3.16)$$

The depletion capacitance varies with the voltage between the gate and the bulk, since this voltage controls the width of the depletion layer. The actual relationship between the depletion capacitance and the gate-to-bulk voltage is a complicated function, which will not be discussed here. Figure 3.10 shows the typical behavior of  $C_{mos}$  versus  $V_{GB}$  for small signals.

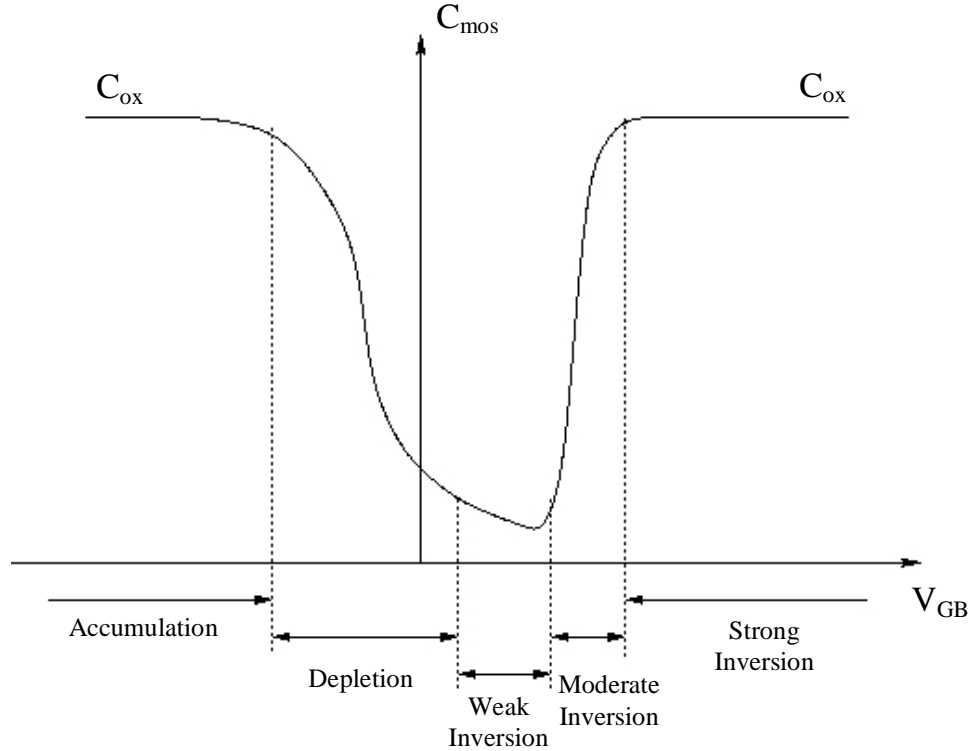


Figure 3.10: Capacitance in NMOS varactor

To obtain an almost monotonic function for  $C_{mos}$ , the MOS varactors can work in two different modes, inversion mode and accumulation mode. In inversion mode, the transistor only works in the inversion region and does not enter the accumulation region. This is accomplished by connecting the bulk to the highest DC voltage available in the circuit (i.e.,  $V_{dd}$ ) for PMOS, or the lowest DC voltage (i.e., ground) for NMOS, as shown in Figure 3.11. Inversion mode MOS varactors, or I-MOS, can be realized with both PMOS and NMOS transistors. NMOS varactors have lower parasitic resistance than PMOS varactors, but are more sensitive to substrate-induced noise [48].

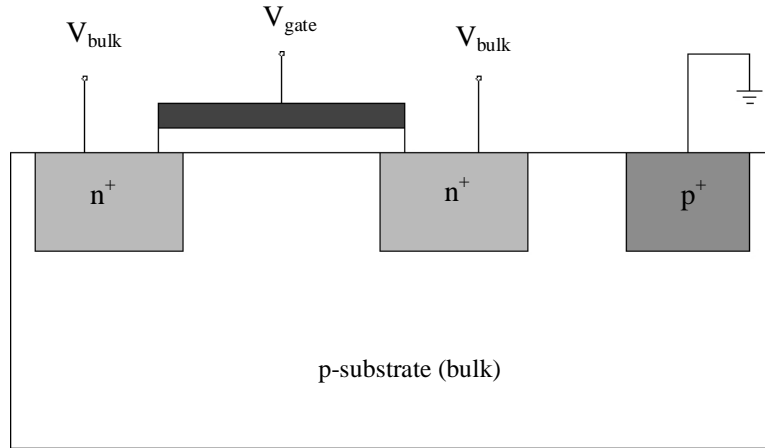


Figure 3.11: Inversion Mode MOS Varactor

In accumulation mode, on the other hand, the transistor works only in accumulation and depletion regions. This is accomplished by removing the drain and source diffusion ( $p^+$ ) from the MOS device, and replacing with the bulk contacts ( $n^+$ ), as shown in Figure 3.12. This MOS structure is often called “NFET in Nwell”.

Accumulation mode MOS varactors usually have larger tuning range and lower parasitic resistance, but are not supported by silicon foundries, which may require some trial-and-error in the design process [47].

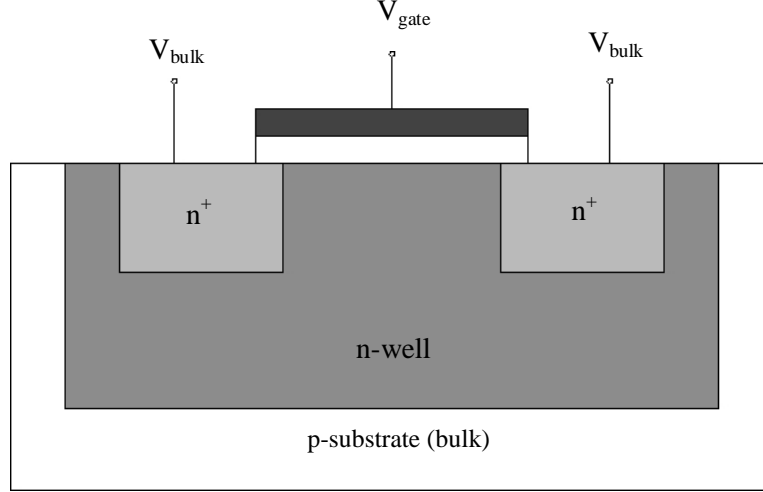


Figure 3.12: Accumulation Mode MOS Varactor

#### 3.1.4.3 MIM Capacitors

The Metal-Insulator-Metal (MIM) capacitor is an important type of capacitor in RF circuits. Its capacitance is fixed, and is given by

$$C = \frac{\epsilon_o \epsilon_r A}{d} \quad (3.17)$$

where  $A$  is the plate area,  $\epsilon_o$  is the dielectric constant in vacuum,  $\epsilon_r$  is the relative dielectric constant of the insulator, and  $d$  is the distance between the metal plates.

MIM capacitors are realized by implementing an additional metal layer, called capacitor top metal (CTM) layer, between the top two normal metal layers, in certain recent fabrication technologies. A capacitor is formed between the CTM layer and the second top most metal layer, and the CTM is connected to the rest of the circuits by via connection to the top metal layer. The CTM and second top most metal layers have a much smaller distance between them than any other metal layers, which gives much bigger capacitance per unit area, according to Equation 3.17.

MIM capacitors have low parasitics, high  $Q$ , good linearity, and high dynamic range. They are often used as coupling capacitors and bypass capacitors in RF circuits. For a variable capacitor application, if the tuning range is not a major concern, a MIM capacitor can be combined with MOS or junction varactors to form

a variable capacitor, which trades tuning range for higher  $Q$ .

#### 3.1.4.4 LIGA-MEMS Capacitor

LIGA-MEMS variable capacitors have been designed and fabricated [14]. One such capacitor is proposed for integration with the VCO circuit. The following description of its design, fabrication, simulation and testing results are based on Haluzan's Master of Science thesis [14].

##### 3.1.4.4.1 Capacitor Design and Fabrication

The capacitors were designed and simulated using Ansoft HFSS<sup>TM</sup>(High Frequency Structure Simulator) [49].

A LIGA-MEMS variable capacitor uses a cantilever beam three-plate configuration, as shown in Figure 3.13. In this configuration, the middle plate has one end fixed and the other end free to move. The surrounding two plates are fixed. The capacitance is formed between the cantilever beam (the middle plate) and the capacitance electrode (bottom plate). A voltage applied between the cantilever beam and the actuator electrode (top plate) causes the cantilever beam to deflect towards the actuator electrode and increases the capacitance gap. This reduces the capacitance between the cantilever beam and the capacitance electrode.

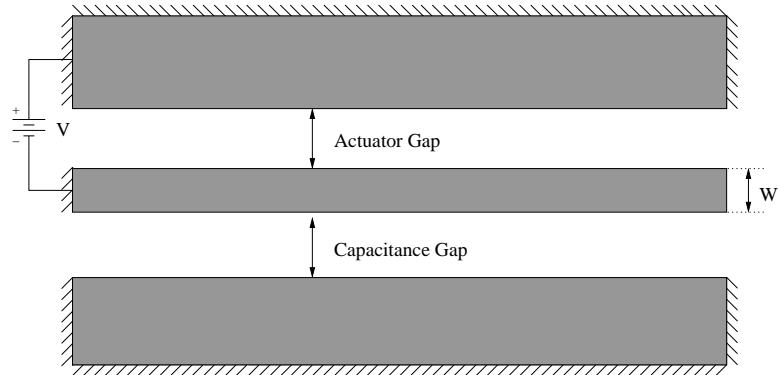


Figure 3.13: Three-Plate Cantilever Beam Capacitor

Figure 3.14 shows a top view of a three-plate cantilever beam capacitor. The actual dimensions of the capacitor to be used in this VCO application are shown in Table 3.1.

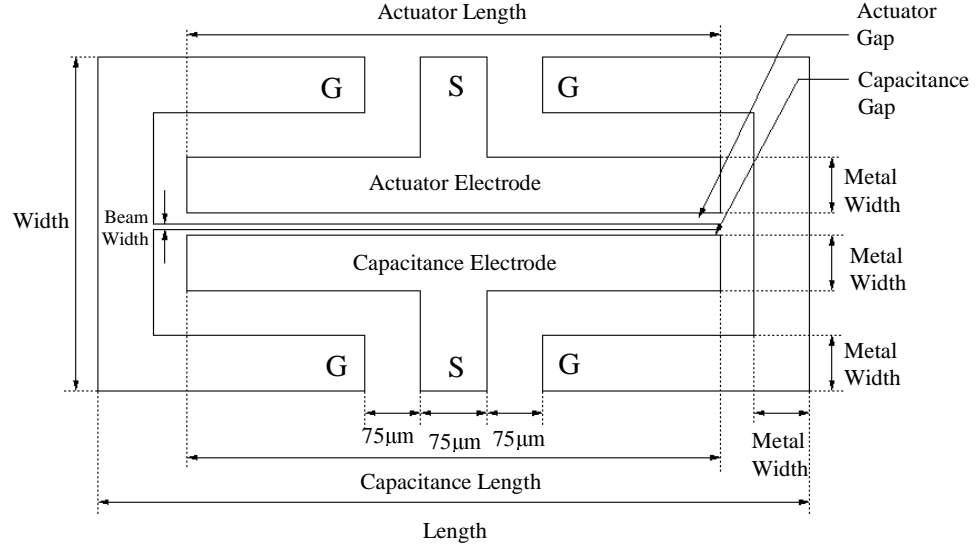


Figure 3.14: Top View of the Capacitor [14]

Table 3.1: LIGA-MEMS Capacitor Dimensions [14]

Length [ $\mu\text{m}$ ]	1950
Width [ $\mu\text{m}$ ]	772.5
Height [ $\mu\text{m}$ ]	100
Actuator Length [ $\mu\text{m}$ ]	1500
Capacitance Length [ $\mu\text{m}$ ]	1500
Metal Width [ $\mu\text{m}$ ]	150
Beam Width [ $\mu\text{m}$ ]	11.9
Actuator Gap [ $\mu\text{m}$ ]	6.0
Capacitance Gap [ $\mu\text{m}$ ]	1.6

The capacitors were fabricated at the Institute of Microstructure Technology (IMT), Forschungszentrum Karlsruhe (FZK), a national laboratory in Germany. An illustration of the fabrication steps is shown in Figure 3.15. The figure is not corresponding to actual shape or size of the capacitor.

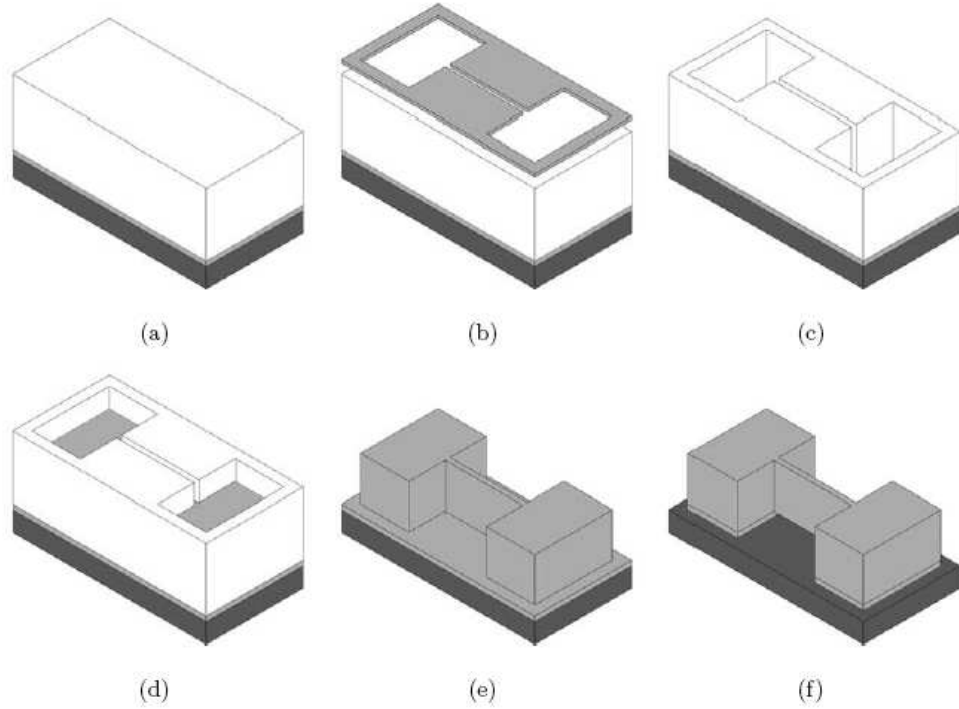


Figure 3.15: LIGA-MEMS Capacitor Fabrication Steps [14]

The capacitors were built on a 1 mm thick alumina substrate, with a 3  $\mu\text{m}$  oxidized titanium seed layer. A 150  $\mu\text{m}$  layer of polymethyl methacrylate (PMMA) photoresist was applied over the substrate and seed layer, as shown in Figure 3.15(a). Then PMMA was exposed to X-rays through a mask consisting of 20  $\mu\text{m}$  thick gold absorbers on a 2.7  $\mu\text{m}$  thick titanium membrane, as shown in Figure 3.15(b). The exposed regions of the photoresist were then dissolved with GG developer, as shown in Figure 3.15(c). The voids were filled with 100  $\mu\text{m}$  of electroplated nickel, as shown in Figure 3.15(d). The metal deposition started on the seed layer. The remaining resist was exposed to X-ray flood irradiation and removed with developer, which

leaves the metal structure, as shown in Figure 3.15(e). The structure was wet etched with 5% HF acid for two minutes to removed the seed layer. This process electrically isolated the capacitor structures, and also selectively released the thin beam, while still providing good adhesion of the large parts of the structure, as shown in Figure 3.15(f).

#### 3.1.4.4.2 Capacitor Specification

Figure 3.16 shows a scanning electron microscope (SEM) micrograph of one of the LIGA-MEMS variable capacitors fabricated.

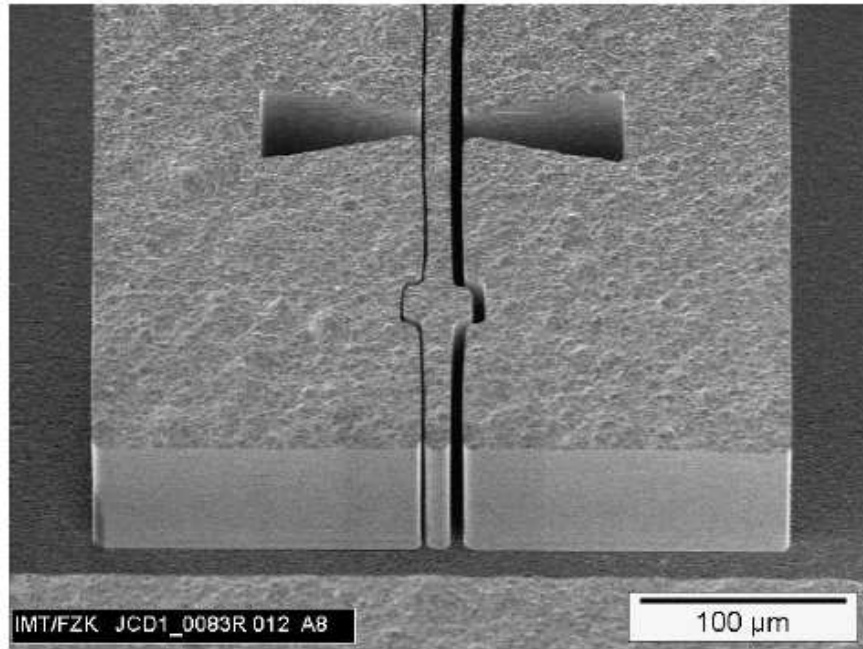


Figure 3.16: Micrograph of LIGA-MEMS Capacitor [14]

The fabricated capacitors were tested using an Agilent 8722ES vector network analyzer, which was connected to the devices through a Cascade ACP-40-W-GSG-150 microprobe.

Figure 3.17 shows the capacitor  $S_{11}$  parameter versus frequency from measurement. At 2.7 GHz in particular, which is the operational frequency of the VCO

application, the fabricated capacitor shows a  $Q$ -factor of 40.9 and a capacitance of 1.05 pF.

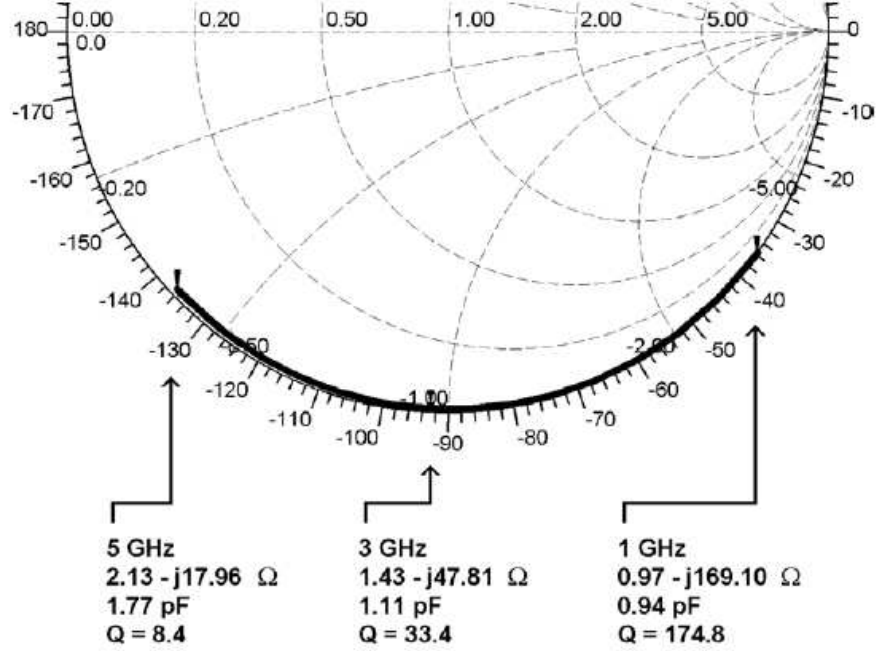


Figure 3.17: Measured LIGA Capacitor  $S_{11}$  [14]

The measured tuning range of such capacitors is approximately 1.2:1 [50].

#### 3.1.4.4.3 Capacitor Integration

Since the LIGA-MEMS variable capacitor was fabricated independently from the VCO core, methods of integrating the two together must be studied. The LIGA-MEMS capacitor was not designed for any specific use, thus it does not consist of any feature for easy integration. Wire bonding is likely the most appropriate method, though other methods are considered as well.

Wire bonding is an electrical interconnection technique using a thin wire to bring two metallic materials (wire and pad surface) into intimate contact. Wire bonding is the earliest technique of device assembly and is a standard procedure of IC packaging [51]. Wire bonding can be used to bond off-chip devices to CMOS chips.

The wires used in bonding are usually made of gold, aluminum, or copper. The bonding wires that connect CMOS chips and external devices are usually longer than internal metal connections within the chips. Thus, the bonding wires may present a considerable amount of inductance and possibly resistance as well. This must be taken into account in the design.

In order to fairly compare the contributions of the LIGA-MEMS capacitor and the CMOS varactor, the effects of the bonding wire should not be added to the VCO using the LIGA-MEMS capacitor alone. The VCO using CMOS varactor should somehow employ the bonding wire as well, so that any difference in the VCO performance would be the result of using different variable capacitors. Introducing bonding wires into integration may reduce the overall performance of the VCO. It is required for fair comparison, but not desirable for low-noise oscillator design. Thus, better integration methods should be investigated.

There are two ways to realize a comparison between VCO performance using a CMOS varactor and a LIGA-MEMS capacitor. The first method is to build two separated VCOs on the same chip, with the same components except for the variable capacitors. One of the VCOs is to connect to the CMOS varactor and the other is to connect to the LIGA-MEMS capacitor. The advantage of this approach is that it is easy to realize without worrying about switching between capacitors. However, this approach requires much more chip space, since all components except the variable capacitors need to be duplicated, while the spiral inductors occupy a large chip area. Also, interference can be an issue if two VCOs are built on the same chip. Isolating them from each other will be necessary. Not only are extra structures required to separate them, but also separate interconnections to the outside world must be provided, such as power supplies, grounds, output terminals, etc. This will further increase the chip size and require more interconnection pads. Another possible problem with this approach is that fabrication variation may exist between the two VCO cores though they are designed to be the same. This may cause unexpected difference in performance.

The second method is to build one VCO core and connect to the CMOS varactor

and the LIGA-MEMS capacitor alternatively. This will require chip area for only one VCO, and one set of interconnections as well, but how to switch between the capacitors will be an issue. To switch between the capacitors, one can either use a transistor switch to turn one of the capacitors on and the other off, or physically disconnect one and connect the other. Using a transistor switch allows to connect all components together and tests the VCO with either capacitors any time by alternating the switch. However, whether the switch can completely cut off the capacitor not in use without introducing any interference is not clearly known. Careful study and design are required. Furthermore, the transistor switch itself may present parasitics. On the other hand, physically connecting only one capacitor at a time guarantees no interference from the capacitor not in use, but removing a connection to a capacitor means cutting the bonding wires, which limits the freedom of choosing the capacitors for the VCO at any time. The second method is used in this research mainly because of the limited chip size.

## **3.2 Systematic Design**

### **3.2.1 Design Flow**

The design of the VCO started with a functional schematic using the software CAD tool ADS® [52] (Advanced Design System) by Agilent Technologies. The schematic design used generic transistor models and ideal passive components (some important parasitics were modeled using ideal passive components as well) to build and verify a functional VCO circuit.

The circuit was then laid out according to TSMC 0.18 micron process using Cadence Virtuoso® [53]. Each circuit component was extracted to find parasitics. These parasitics were then included in the ADS simulation. The circuit was then modified and re-laid out until the layout, including parasitics, satisfies the design specification.

The VCO circuit was designed to use a 3.3 V DC power supply. The operation frequency is between 2.6 GHz and 2.7 GHz. The circuit was designed to drive a

50  $\Omega$  load, so that it can be used as a device in the standard 50  $\Omega$  system.

### 3.2.2 CMOS Varactor

A combination of a MIM capacitor and NMOS varactors in inversion mode were used as the capacitive component in the resonant tank with certain frequency tuning ability. Figure 3.18 shows the ADS schematic of the varactor. In the functional design, a generic transistor model and ideal capacitor were used, while in post-layout simulation, extracted parasitics from layout were included in the component parameters.

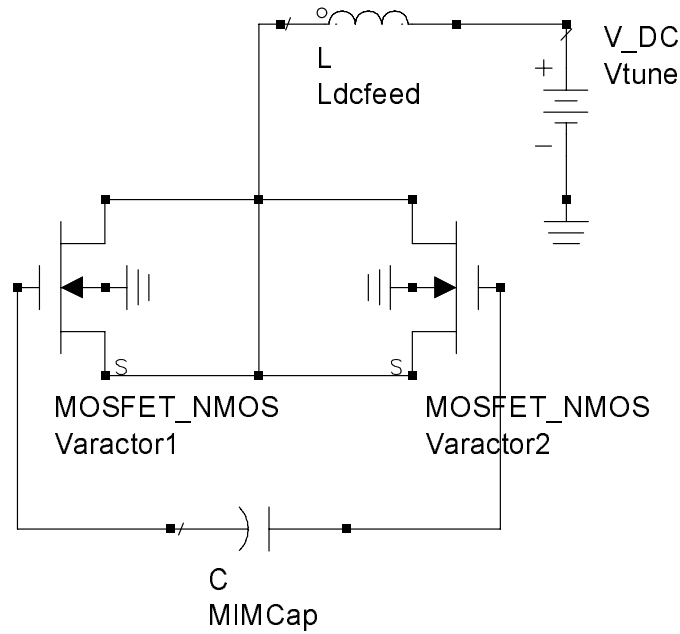


Figure 3.18: CMOS Varactor Schematic in ADS

The NMOS varactor pair is designed to be symmetric, with a DC tuning voltage between two identical NMOS varactors, to provide balanced properties for a fully differential system. The capacitance of the NMOS varactor pair is determined by the area of the MOSFET (width times length) and the external tuning voltage.

At 2.7 GHz, the final NMOS varactor pair has a capacitance of 0.228 pF at 0 V DC and 0.050 pF at 3.3 V DC. The MIM capacitor has a capacitance of 0.952 pF.

When it is added to the NMOS varactor pair, the combination provides a capacitance range from 1.18 pF to 1.00 pF over the tuning voltage from 0 V to 3.3 V DC, as shown in Figure 3.19. The three inductors are external DC feeds used to bias the transistors without loading them, and also block possible AC interference from DC power supplies. The actual inductance values are not required to be the same as shown in the figure as long as they are relatively big.

### 3.2.3 CMOS Inductors

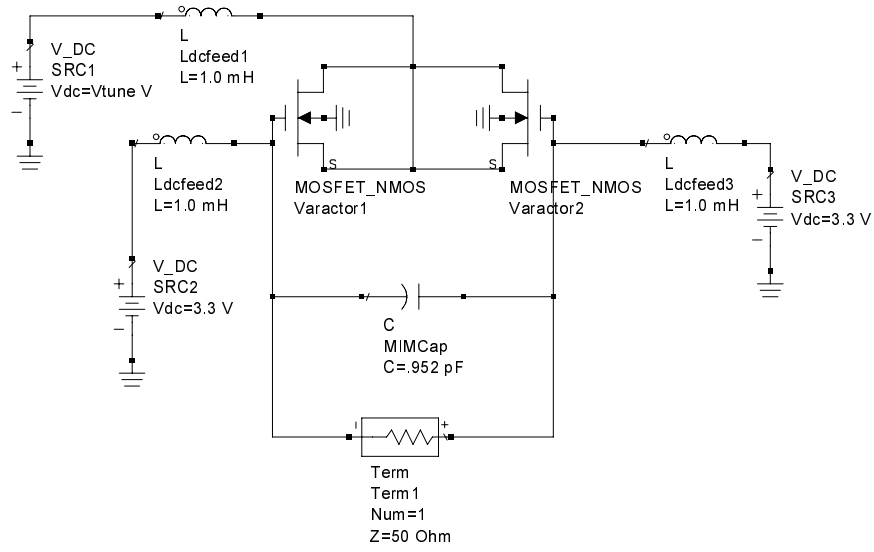
For a resonant frequency of 2.7 GHz with a capacitor of 1.14 pF, which is the simulated capacitance of the LIGA-MEMS capacitor, the inductance required would be approximately 3.0 nH based on the simple resonance in Equation 2.9. However, after taking account of the parasitics from other parts of the circuit, including active components, bonding wires, etc., the total inductance of the CMOS spiral inductors is reduced to 1.92 nH, with series resistance of  $5.8 \Omega$  based on ASITIC simulation.

For a differential mode design, the required inductance is provided by two identical on-chip inductors  $L_1$  and  $L_2$ , so that the DC power supply can connect to the resonant tank in balance. Figure 3.20 shows the ADS schematic of the overall resonant tank using CMOS varactors.

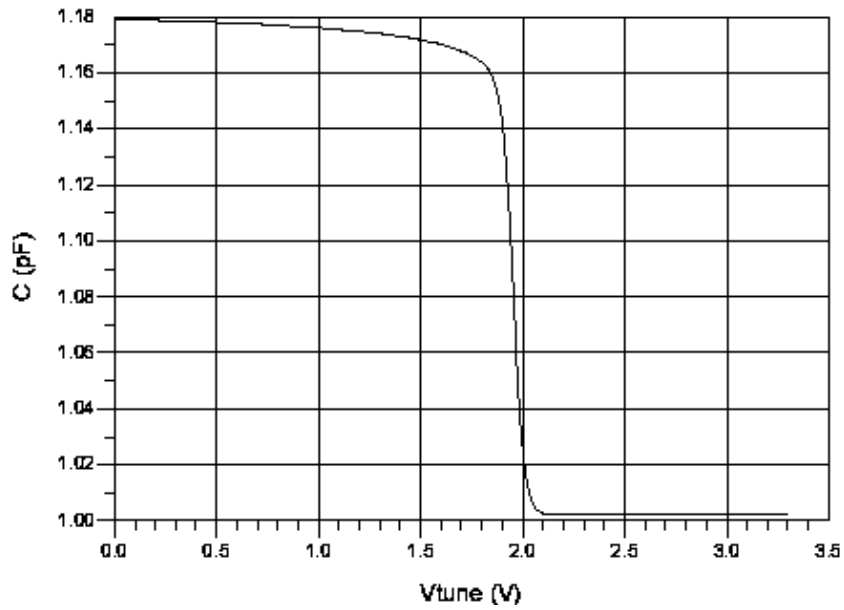
### 3.2.4 Bonding Wires

Bonding wires are used to connect the VCO core and the varactor or the LIGA-MEMS capacitor. Bonding wire, virtually a small non-ideal inductor, can be modeled as an inductor in series with a resistor.

The length of the bonding wires depends on the distance between the two pads to be connected, and varies with bonding process. The distance between pads for connecting the varactor to VCO core is  $300 \mu\text{m}$ . The distance between pads for connecting the LIGA-MEMS capacitor depends on how the chip and the capacitor are placed. Different lengths of bonding wires were modeled in ADS. Due to the bonding process, the bonding wires are not straight lines, but curve up and show a bridged shape. Thus, the length of the bonding wire is typically much longer than



(a) Schematic



(b) Results

Figure 3.19: CMOS Varactor Capacitance Simulation at 2.7 GHz

the distance between the pads, and is not a linear function of the distance. ADS simulates bonding wires using five linearized segments to represent a typical geometrical shape. Table 3.2 shows the estimated length, the equivalent series inductance and resistance of the bonding wire at 2.7 GHz with respect to the distance between

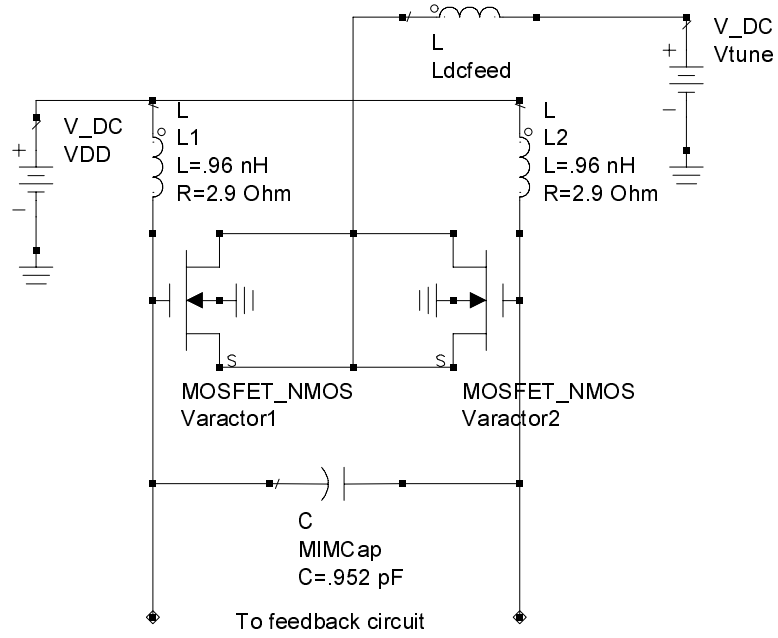


Figure 3.20: Resonant Tank Schematic in ADS

the connecting pads.

Table 3.2: Inductance and Resistance of Bonding Wires

Distance Between Pads [ $\mu\text{m}$ ]	Wire Length [ $\mu\text{m}$ ]	Series Inductance [nH]	Series Resistance [ $\Omega$ ]
100	1037	0.067	0.045
150	1107	0.088	0.048
200	1268	0.107	0.055
250	1452	0.126	0.063
300	1660	0.144	0.072
350	1867	0.163	0.081
400	2075	0.181	0.090
450	2282	0.200	0.099
500	2513	0.219	0.109

Since the actual bonding wire length required is difficult to estimate accurately, the distance between pads for connecting the varactor to the VCO core,  $300\text{ }\mu\text{m}$ , is used to model bonding wires in the VCO simulations for both the VCO with the varactor and with the LIGA-MEMS capacitor. The above bonding wire simulation is also used to determine the maximum length of bonding wires, for exceeding this would stop the VCO oscillating. The simulation shows that, when the LIGA-MEMS capacitor is placed more than  $3.2\text{ mm}$  away from the chip, the bonding wires would be long enough to produce too much parasitics and prevent the VCO from oscillating.

### 3.2.5 Transistors

To simplify the design and save chip area, the NMOS-only cross-coupled configuration is used. As shown in the simplified ADS VCO schematic diagram (Figure 3.21), M1 and M2 are the cross-coupled transistors. Since the output signal at this stage is not capable of providing enough current to drive a  $50\text{ }\Omega$  load, a driver is added using two transistors, M3 and M4.

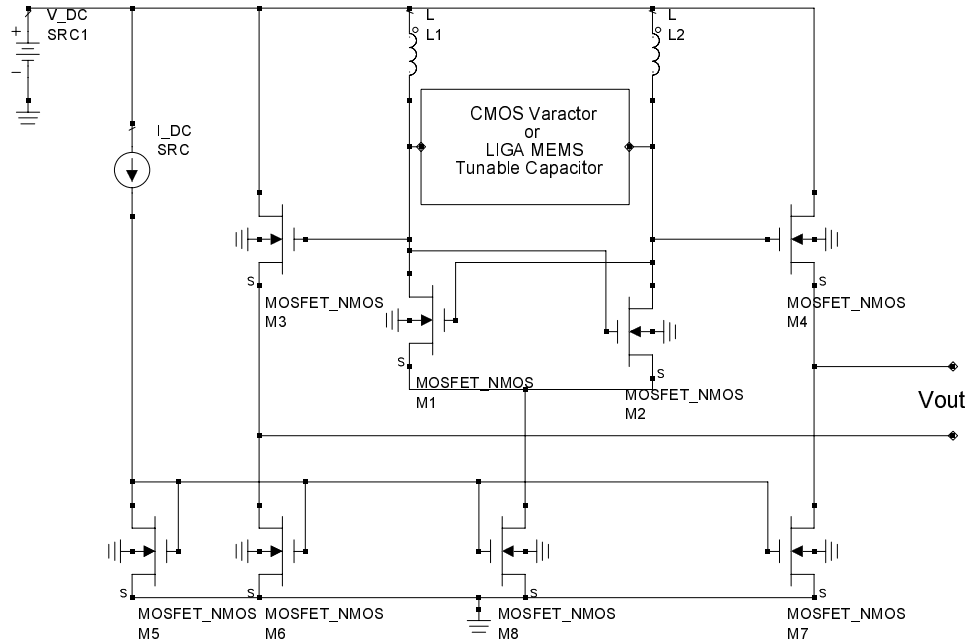


Figure 3.21: A Simple VCO Schematic in ADS

All the transistors require DC bias currents. The bias currents are set using current mirror formed by transistors M5, M6, M7 and M8. By matching the channel length and the gate and source voltage of M6, M7 and M8 to that of M5, the ratio of the current flow through M5, M6, M7 and M8 equals the ratio of their channel width. Thus, the bias currents are controlled by the DC current reference  $I_{DC}$ , which flows through M5 directly.

Due to the relatively large current through the devices, transistors in analog circuits are typically much wider than the transistors in digital circuits. Thus, a transistor with large width is usually implemented with multiple transistors in parallel, as shown in Figure 3.22. The effective width of the large transistors equals the number of small transistors multiplied by the width of the small transistors.

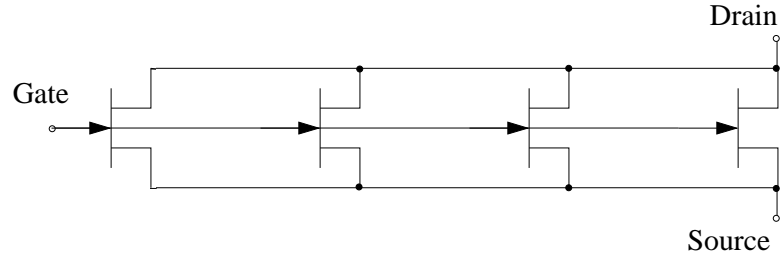


Figure 3.22: A Example of Multiple Transistors in Parallel

Table 3.3 summarizes the transistor parameters. Note that the width listed is the width of each small transistor.

Table 3.3: Transistors Parameters

Transistor	Length [ $\mu\text{m}$ ]	Width [ $\mu\text{m}$ ]	Multiples
M1 & M2	0.5	8.0	18
M3 & M4	2.0	8.0	16
M5	0.5	8.0	1
M6, M7 & M8	0.5	8.0	24

### 3.3 Analysis

Analysis on each part of the circuit was done throughout the design process to ensure the design meets the specific requirement. The analysis uses simplified models, theoretical equations and simulation results of particular components to check if parts of the circuit are functioning as they are intended. These analysis are not as accurate as simulations on the entire circuit, but provide quick checks on different components in the circuit. In this section, some important analysis is described.

The oxidation layer capacitance for M1 and M2 is 0.139 pF. The oxidation layer capacitance for M3 and M4 is 0.421 pF. These parasitic capacitances exist in the feedback circuit, and thus affect the oscillation frequency. Including these capacitance in Equation 2.9 along with the tank components, the resonant frequency can be tuned between 2.75 GHz and 2.91 GHz. This analysis does not include the inductance of bonding wires since it complicates the model. It is expected that the bonding wires will reduce the resonant frequency as they introduce more inductance.

For the transistors in the feedback circuit to provide sufficient transconductance, a biasing DC current of 17.7 mA is required. The current source generates 736  $\mu$ A DC current. The current mirror with a channel width ratio of 24 produces exact biasing current for the feedback circuit.

## 4. Circuit Layout

Circuit layout is the presentation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit. While a schematic usually implies ideal components and interconnections, layout, on the other hand, represents the real positions, interconnection and geometric shapes of the circuit, and largely affects the behavior of the circuit. In this chapter, the VCO circuit layout is presented.

### 4.1 Layout Basics

The TSMC 0.18 micron CMOS process is a typical n-well process. It starts with a lightly doped p-type substrate, creates the n-type well for the p-channel transistors, and builds the n-channel transistors in the native p-substrate. Gates are implemented with polysilicon. Up to six layers of metal can be used for interconnection. They are labeled as metal-1 to metal-6, with metal-1 closest to the substrate and metal-6 as the top metal layer. Different layers of metals can be connected by vias. The connections between metal-1 and the polysilicon layer, well, or substrate are called contacts.

There are design rules that must be obeyed in layout. These rules specify certain geometric constraints on the layout artwork so that the patterns on the processed wafer will preserve the topology and geometry of the designs. Although design rules do not necessarily represent the physical limits of the process capability, they are, in general, the best compromise between performance and yield [54]. Design rules include the minimum and maximum width of each layer, minimum spacing between wires or regions, minimum overlapping area for certain layers, and other rules for particular devices.

## 4.2 VCO Circuit Layout

Unlike digital circuits, an analog circuit cannot be automatically generated by software due to its complexity. For analog circuits, especially circuits in the GHz range, proper layout is critical. A poor layout generates unexpected parasitics and may cause circuit failures. Often it requires several runs of re-design to improve the layout to perform as expected.

The VCO circuit was laid out using Cadence Virtuoso® [53]. Each circuit component was drawn manually, and then extracted to find parasitics. These parasitics were then included in the simulation, which leads to modification and re-layout of the circuit.

### 4.2.1 Inductor Layout

The top most layer of metal (metal-6) was used for the inductors, because this is the thickest metal layer with the smallest resistance. It is also far away from the lossy silicon substrate. Figure 4.1 shows the inductor layout in Cadence (left) and the corresponding metal-1 patterned ground shield (right), which is placed underneath the inductor to reduce eddy currents and noise from the substrate. The dimensions have the unit of  $\mu\text{m}$ .

Since Cadence Virtuoso treats a metal spiral inductor as a piece of wire and does not recognize it as an inductor in extraction, the RF properties of the inductor must be sought using other software. Then a lumped element model of the inductor based on the simulation from the software can be used in the simulation of the circuit.

ASITIC version 10 [44], which contains a CMOS 0.18  $\mu\text{m}$  technology file to match the fabrication parameters, was used to extract the lumped element model for the inductors. The layout parameters and important lumped element model parameters of the inductors after extraction with ASITIC are summarized in Table 4.1.

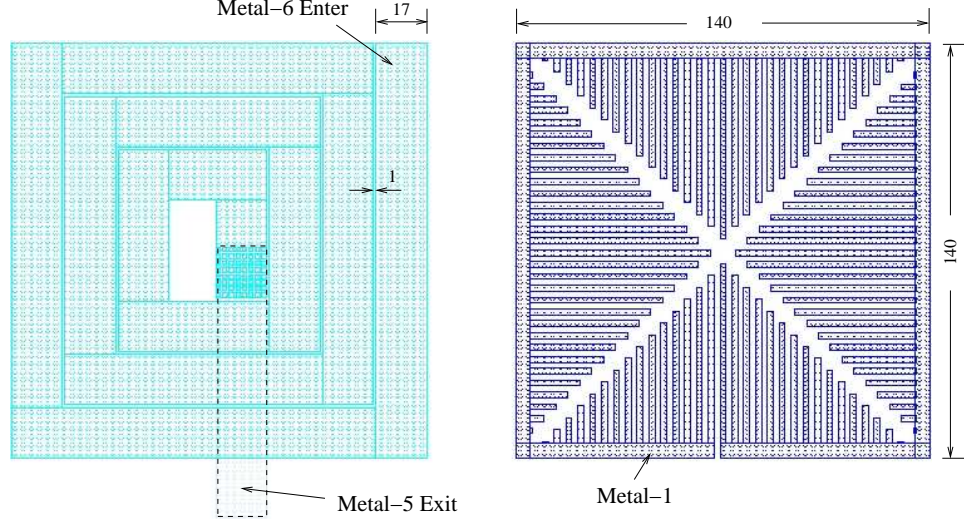


Figure 4.1: Cadence Inductor Layout (left) and PGS Layout (right)

Table 4.1: Spiral Inductor Parameters at 2.7 GHz

Width of the Spiral [ $\mu\text{m}$ ]	140
Width of the Trace [ $\mu\text{m}$ ]	17
Spacing [ $\mu\text{m}$ ]	1
Number of Turns	3.25
$L$ at 2.7 GHz [nH]	0.963
$R_s$ [ $\Omega$ ]	2.90
$Q$	5.65

#### 4.2.2 Transistor Layout

For differential circuits, two common methods are often used to reduce the effects of process variances. One is known as common-centroid layout. In this approach, transistors that need precision matching are realized with their fingers interdigitated [55].

The second method involves using dummy transistors outside of functional transistor fingers. These dummy transistors are included to provide greater matching

accuracy for functional transistors. Their gates are connected to the most negative power supply voltage (for n-channel transistors) to ensure they are always off.

Figure 4.2 shows an example transistor layout that implements the above methods. Transistors M1 and M2 are both divided into 3 fingers of equal width, and placed symmetrically to ensure any loss across the microcircuit would affect M1 and M2 in the same way. Dummy transistors are placed at both sides. The entire structure is placed inside a guarding ring with many substrate contacts to isolate noises. The actual transistor layout of the VCO circuit is similar to Figure 4.2, but differs in size and number of fingers. Figure 4.3 shows the active part of the VCO circuit, which includes all the transistors used in the VCO core.

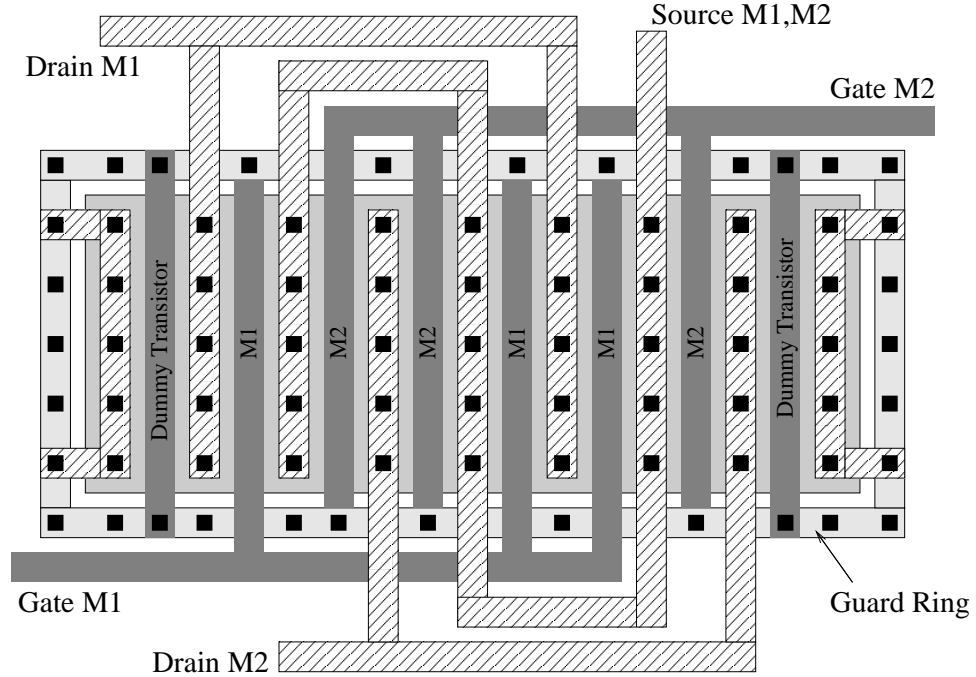


Figure 4.2: Common-Centroid Transistor Layout Example for Differential Circuits

### 4.2.3 Varactor Layout

The CMOS varactor was laid out on the same chip area as the VCO core, but not electrically connected to the VCO core. It is only connected to the pads. If the

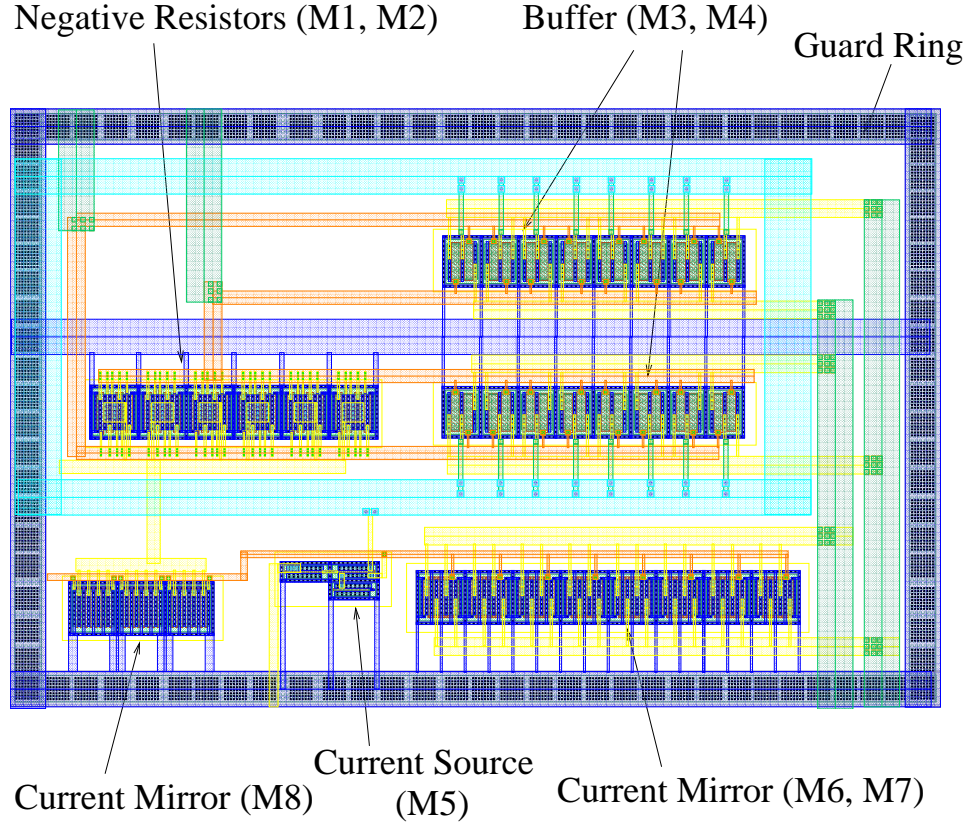


Figure 4.3: Active Part of the VCO Layout

CMOS varactor is to be used as the tuning capacitor for the VCO, it can be wire bonded to the VCO core through the pads. If the LIGA-MEMS capacitor is to be used, the CMOS varactor would remain unconnected.

The varactor used in this VCO application includes a MIM capacitor and a pair of NMOS varactors. The MIM capacitor, as shown in Figure 4.4, was formed using  $32 \times 32 \mu\text{m}^2$  of metal-5 and  $30 \times 30 \mu\text{m}^2$  of an extra metal layer CTM. CTM is located between metal-5 and metal-6, close to metal-5, and can be connected to the rest of the circuit through metal-6.

The NMOS varactor pair was laid out similar to the transistor layout. Multiple-gate fingers and guard ring techniques were applied, as shown in Figure 4.5.

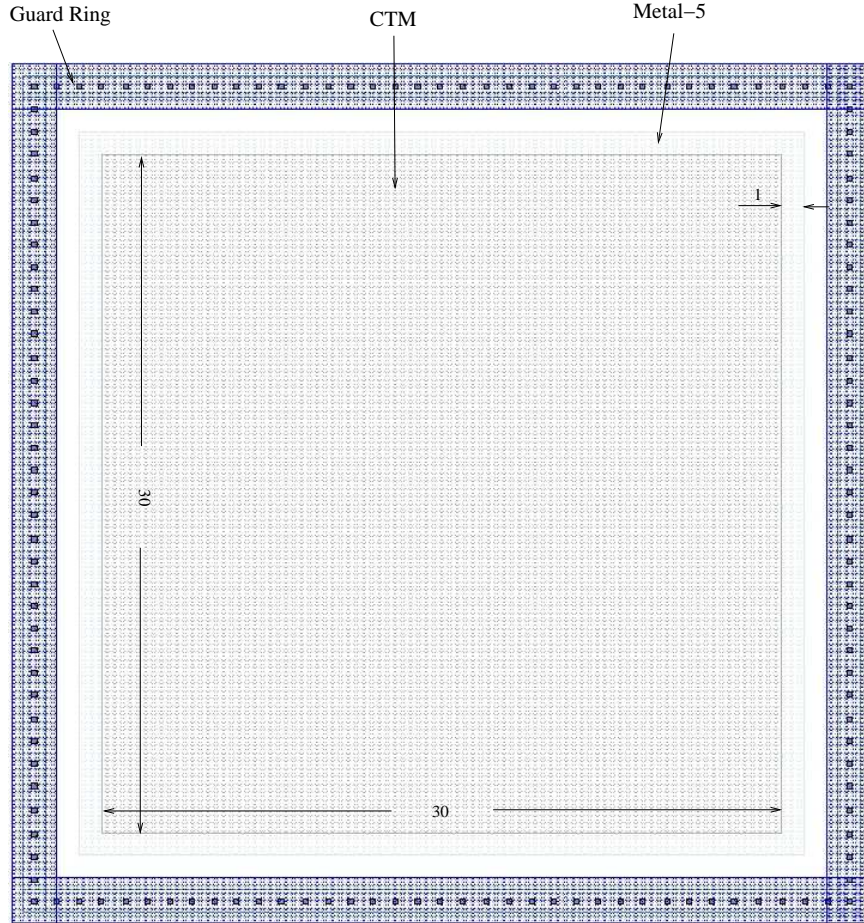


Figure 4.4: MIM Capacitor Layout

#### 4.2.4 VCO Chip Layout

A wide strip ( $30\ \mu\text{m}$ ) of metal-6 was used to form a square around the circuit to create a power ring. It is to be connected to the power supply. The use of the power ring is to reduce ohmic loss and parasitics that may occur to some parts of the circuit which are further away from the power supply connection, and thus deliver power supply voltage uniformly. For the same reason, metal-1 was used to form a ground ring.

Pads are metal plates at the edges of the chip area on which wires can be bonded. CMOS circuits connect to the packages, circuit boards or other circuits or equipments through the pads. Twenty pads were laid out in this design. They are used

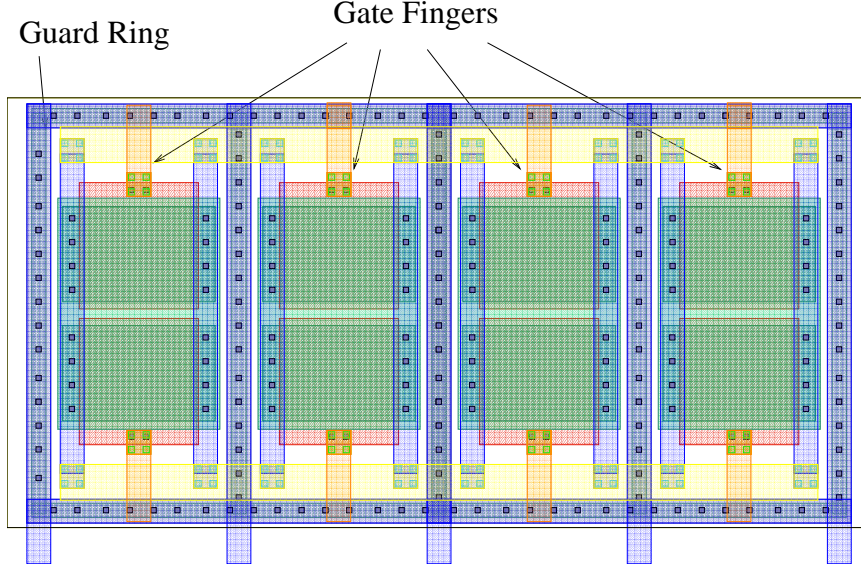


Figure 4.5: NMOS Varactor Pair Layout

for power supply, ground, output terminals, connections to the VCO core, connections to the CMOS varactor, tuning voltage, and two testing points, which are used for possible trouble shooting. There are two pads for each power supply, ground, output terminals and connections to the VCO core.

Six extra probing pads are included in the layout as a backup plan for integrating the LIGA-MEMS capacitor directly to the VCO chip. The probing pads are metal-6 plates that are  $100\text{ }\mu\text{m}$  wide and  $50\text{ }\mu\text{m}$  apart. They form ground-signal-ground connections for a microprobe. In case wire-bonding fails, these pads may provide an alternative. However, it was later suggested that these pads could seriously complicate the feedback circuit parasitics and affect the oscillation condition of the oscillator. This is to be explained further in Chapter 5.

The VCO chip occupies an area of  $1\text{ mm} \times 1\text{ mm}$ . This includes the VCO core, the spiral inductors, the CMOS varactor, the pads and other features. The VCO chip layout is shown in Figure 4.6.

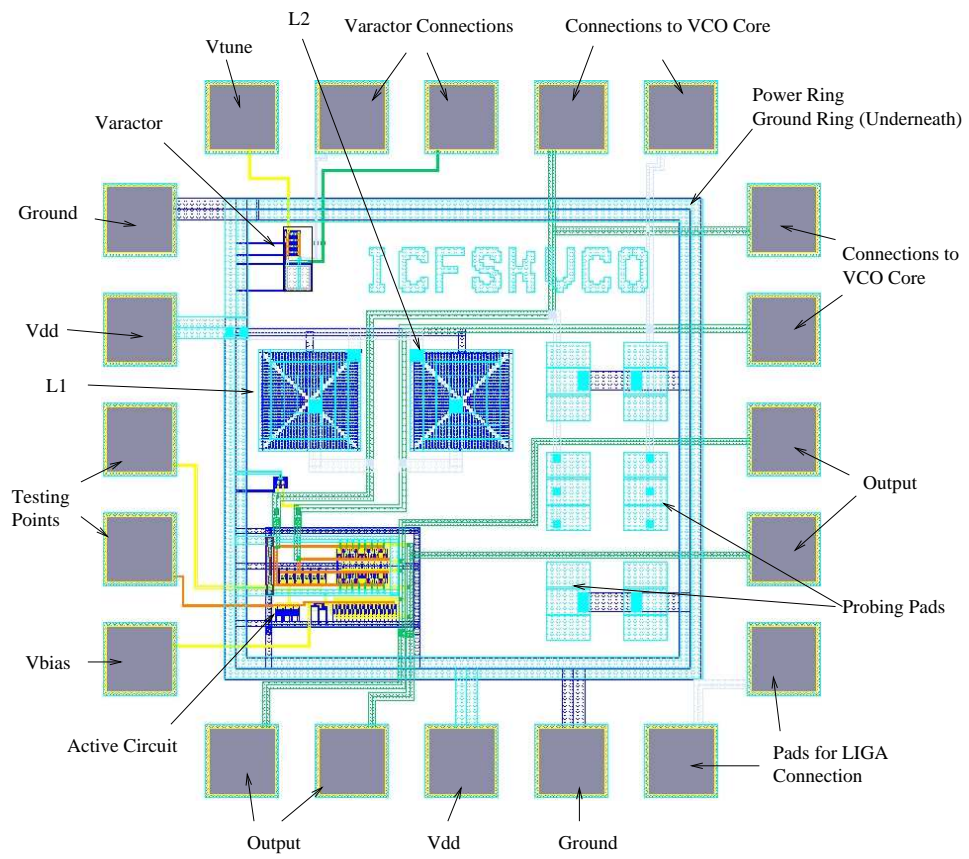


Figure 4.6: VCO Chip Layout

## 5. Results

In this chapter, simulation results and performance comparison, and a test procedure and measurement results of the fabricated VCO chip are presented. The difficulties encountered in LIGA-MEMS capacitor integration and possible solutions are also discussed.

### 5.1 Simulation Results

#### 5.1.1 Simulation Tool

The VCO simulation was performed using ADS. ADS is a powerful RFIC simulator that integrates a complete set of simulation technologies required in RFIC design. ADS can perform DC simulation, AC and S-parameter simulation, transient time-domain simulation, and Harmonic Balance (HB) simulation. ADS can easily simulate important parameters of the VCO, such as frequency and phase noise, while Cadence Virtuoso Spectre, which typically simulates the circuit in the time-domain, has disadvantages in frequency-domain simulation.

Harmonic Balance is a frequency-domain nonlinear simulation technique. It is very effective in simulating steady-state nonlinear circuits with multitone excitation. It is also effective in analyzing nonlinear noise while traditional SPICE-like linear noise analysis cannot predict the noise performance of a circuit with frequency-mixing effects.

ADS phase noise analysis computes the noise sidebands of the oscillator carrier frequency together with frequency conversion, amplitude-noise-to-frequency-noise conversion, frequency translation of noise caused by component nonlinearities in the presence of large-signal oscillator signals, and bias changes due to the oscillator signals.

ADS simulates phase noise using two methods: from the oscillator frequency sensitivity to noise and from small-signal mixing of noise. The frequency sensitivity to noise can be viewed as the oscillator changing its operating frequency due to frequency modulation caused by noise generated in the oscillator. The small-signal mixing of noise comes from the nonlinear behavior of the oscillator, where noise mixes with the oscillator signal and harmonics mix to sideband frequencies.

The sensitivity of the oscillation frequency is obtained with respect to any injected noise in the circuit. After summing all of the noise sources, the total spectral density of frequency fluctuations is obtained and converted to phase noise. This method is valid at small offset frequencies, but is not useful at very large offsets as the noise goes to zero instead of exhibiting a noise floor.

For the noise mixing analysis, the noise at the sidebands is obtained from a small-signal mixer analysis, where noise sources mix with the oscillator large signals to produce noise sidebands. The noise at these two sideband frequencies and their correlation is then used to compute the phase noise. The phase noise from a mixing analysis tends to be valid at large offset frequencies and will show a finite noise floor, but less accurate at small offset frequencies.

At offset frequencies neither too small nor too large, these two methods generate similar results. Combining frequency sensitivity method for very small offset and mixing analysis method for very large offset, a phase noise curve similar to Leeson's model can be generated.

### **5.1.2 Simulation Results Using CMOS Varactor**

The following simulation results are for the VCO circuit using the on-chip varactor. The simulation includes bonding wire connection between the varactor and the VCO core through the bonding pads on the chip. The DC power supply and the DC biasing voltage are set to 3.3 V. The differential outputs are connected to a 50  $\Omega$  resistor to represent the load. The voltage across the load and the current through the load are measured and used to calculate the power. Phase noise is also measured at the differential outputs.

With a varactor tuning voltage of 2.2 V, the VCO operates at 2.548 GHz, with an output power of -0.955 dBm. Figure 5.1 shows the output power of the VCO at different harmonic frequencies. Note that the even number of harmonics are largely eliminated due to the differential nature of the circuit.

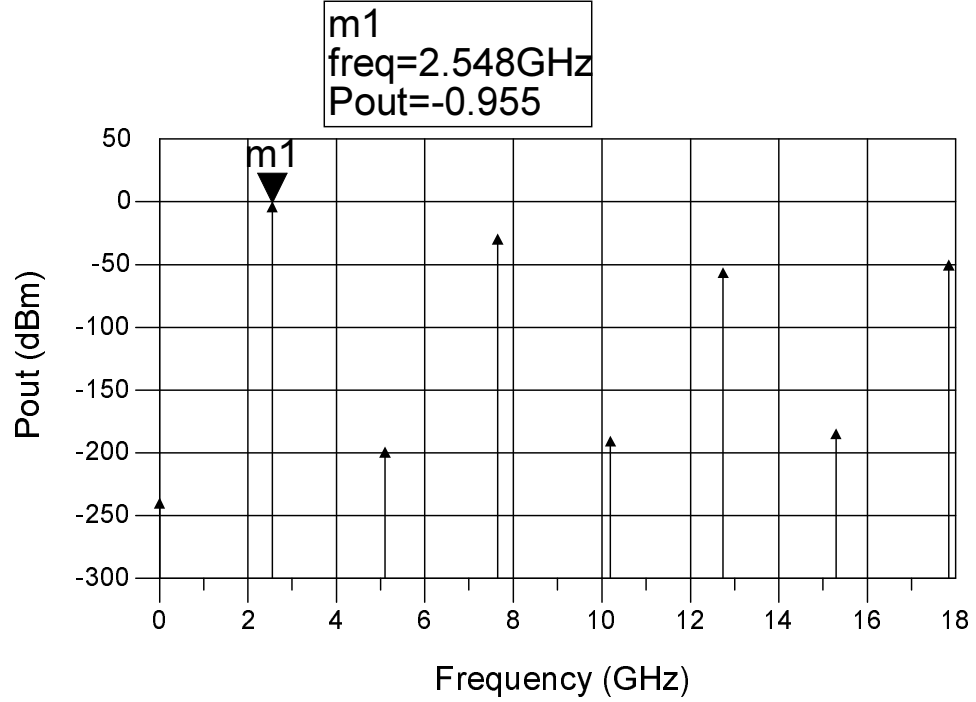


Figure 5.1: Output Power of VCO with Varactor

At 2.548 GHz, the phase noise of the VCO is shown in Figure 5.2. Both methods of simulating phase noise mentioned above were used. They agree with each other very closely and overlap as shown in Figure 5.2. In particular, at 100 kHz offset, both analyses show a phase noise of -89.1 dBc/Hz, and at 300 kHz offset, -102.7 dBc/Hz.

The Figure of Merit of the VCO for the offset frequency of 100 kHz was calculated to be -186.1, and for offset frequency of 300 kHz is -190.2.

Since the power supply voltage is 3.3 VDC, the varactor tuning voltage is allowed between 0 and 3.3 V. In this range, the VCO oscillation frequency varies from 2.433 GHz to 2.582 GHz, as shown in Figure 5.3.

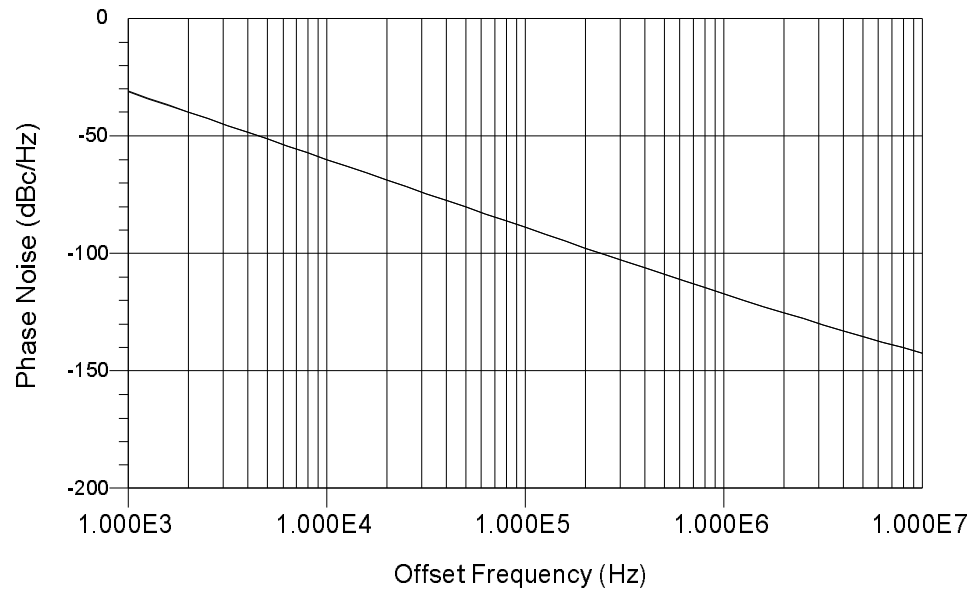


Figure 5.2: Phase Noise of VCO with Varactor

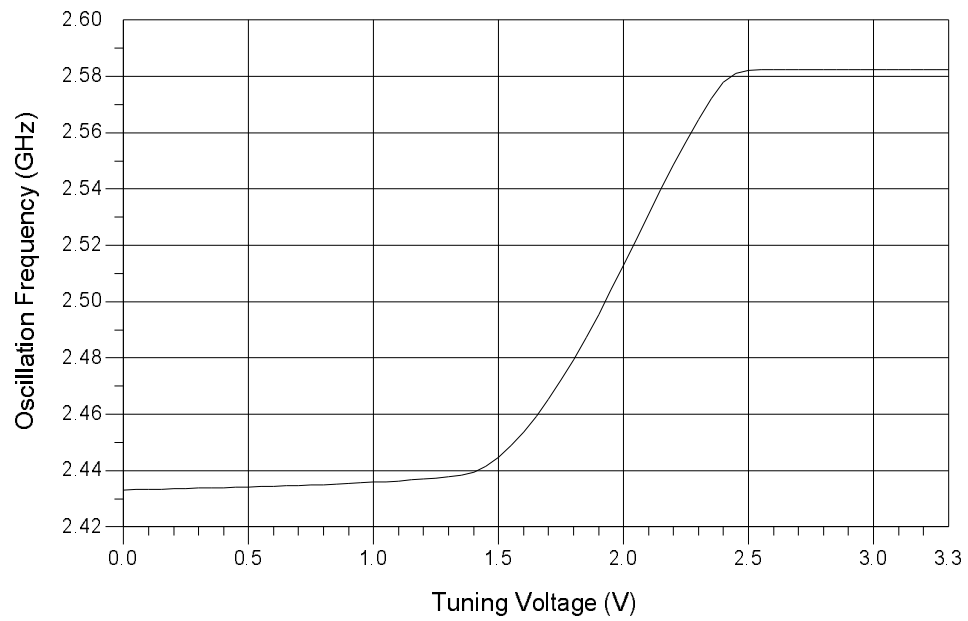


Figure 5.3: Frequency Tuning of the VCO with Varactor

Figure 5.4 summarizes the oscillation frequency, output power, and phase noise of the VCO over the tuning voltage between 1.3 V and 2.5 V, where frequency varies most obviously.

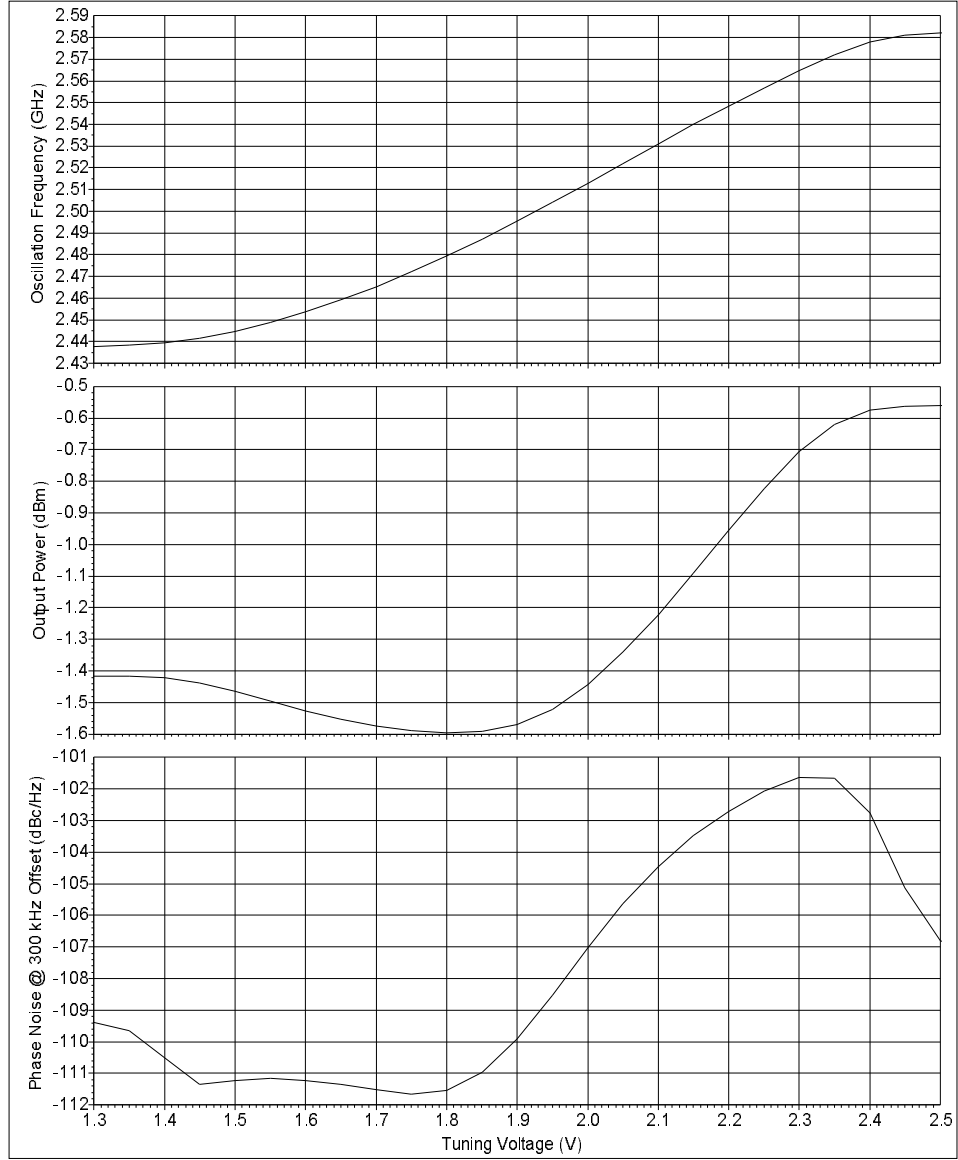


Figure 5.4: VCO Tuning

### 5.1.3 Simulation Results Using Fabricated LIGA-MEMS Capacitor

The following simulation results are for the VCO circuit using the fabricated LIGA-MEMS tunable capacitor data obtained from Haluzan's Mater of Science thesis [14]. The simulation setup was exactly the same as that for the VCO using on-chip varactor, except that an S-parameter data file, which represents the fabricated LIGA-MEMS capacitor, was used instead of the on-chip varactor circuit. This data

file contains the measurement result of the fabricated LIGA-MEMS capacitor.

With the fabricated LIGA-MEMS capacitor, the VCO operates at 2.557 GHz, with an output power of 0.121 dBm. Figure 5.5 shows the output power of the VCO at different harmonic frequencies.

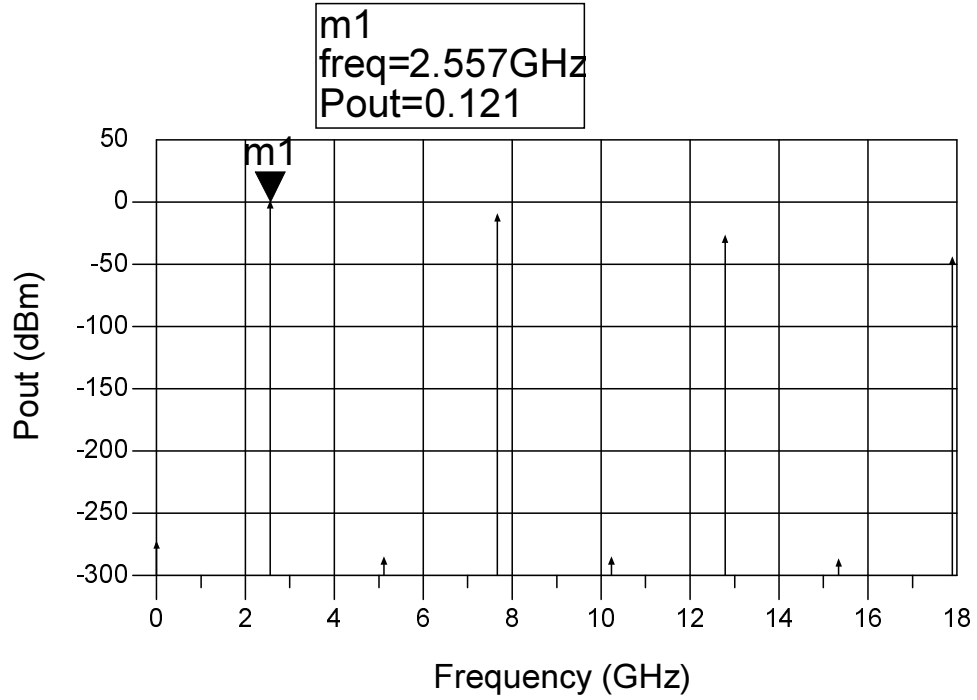


Figure 5.5: Output Power of VCO with Fabricated LIGA-MEMS Capacitor

At the oscillation frequency, the phase noise of the VCO is shown in Figure 5.6. The noise mixing analysis shows smaller phase noise values than the sensitivity to noise analysis for small offset frequencies. For offset frequencies between 100 kHz and 100 MHz, the two analysis agree with each other closely. In particular, at 100 kHz offset, sensitivity to noise analysis shows a phase noise of -96.3 dBc/Hz, and noise mixing analysis shows a phase noise of -96.6 dBc/Hz. At 300 kHz offset, both analysis show a phase noise of -109.1 dBc/Hz.

The Figure of Merit of the VCO for offset frequency of 100 kHz is calculated to be -192.6, and for offset frequency of 300 kHz is -195.5.

The VCO tuning simulation was not performed for the LIGA capacitor setup

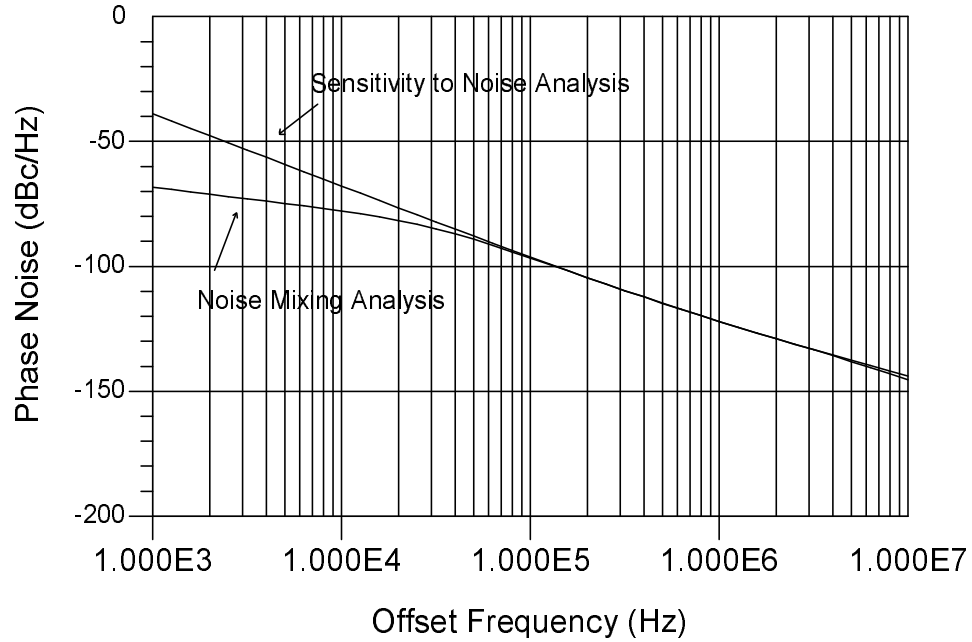


Figure 5.6: Phase Noise of VCO with Fabricated LIGA-MEMS Capacitor

since tuning of the fabricated LIGA-MEMS capacitor was not performed [14].

#### 5.1.4 Simulation Results Using Other Possible LIGA-MEMS Designs

The same simulation was performed for the VCO circuit using a similar LIGA-MEMS capacitor design. This capacitor has the same physical structure as the fabricated LIGA-MEMS capacitor, but using copper instead of nickel. Copper has higher conductivity than nickel, thus, the copper capacitor is assumed having potentially better electrical properties than the nickel capacitor. For instance, at 2.7 GHz, simulation shows the copper LIGA-MEMS capacitor has a Q-factor of 520. However, the copper LIGA-MEMS capacitor design has not been fabricated. Simulated S-parameter data for the copper capacitor was used in the VCO simulation. This demonstrates the VCO performance with a potentially higher quality LIGA-MEMS capacitor.

With the copper LIGA-MEMS capacitor, the VCO operates at 2.549 GHz, with an output power of 0.406 dBm. Figure 5.7 shows the output power of the VCO at

different harmonic frequencies.

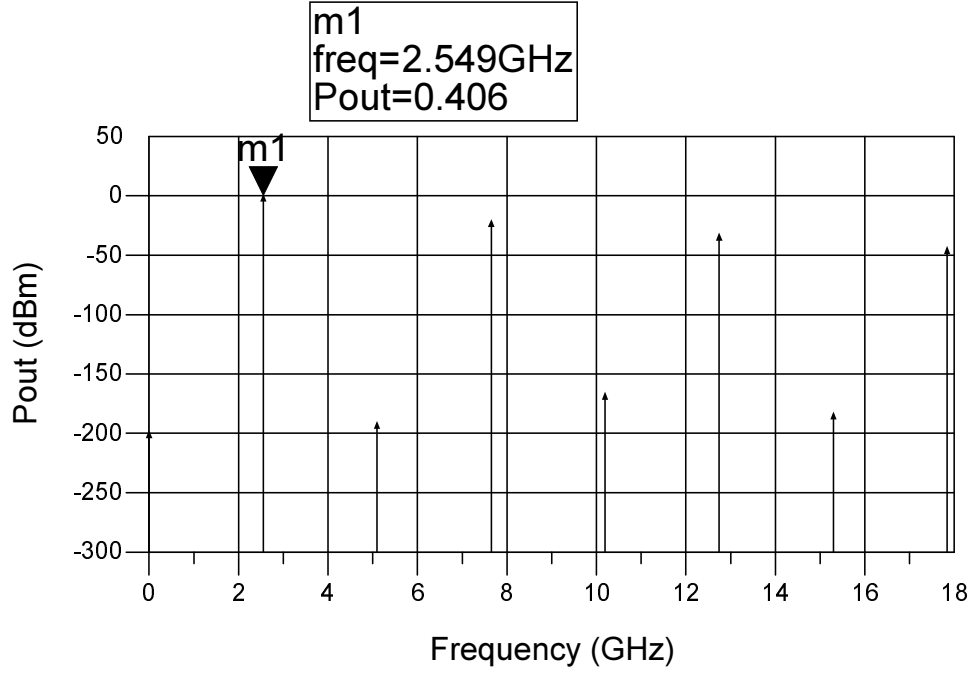


Figure 5.7: Output Power of VCO with Copper LIGA-MEMS Capacitor

At the oscillation frequency, the phase noise of the VCO is shown in Figure 5.8. The noise mixing analysis shows smaller phase noise values than the sensitivity to noise analysis for small offset frequencies. For offset frequencies greater than 20 kHz, the two analysis agree with each other closely. In particular, at 100 kHz offset, both analysis show phase noise of -94.2 dBc/Hz, and at 300 kHz offset, -107.5 dBc/Hz.

The Figure of Merit of the VCO for offset frequency of 100 kHz was calculated to be -189.8, and for offset frequency of 300 kHz was -193.6.

### 5.1.5 Performance Comparison

Table 5.1 summarizes the simulation results for the VCOs using three different capacitor models for comparison.

The comparison shows that, with very close operation frequency, both the VCO with fabricated LIGA-MEMS capacitor and the VCO with simulated copper LIGA-

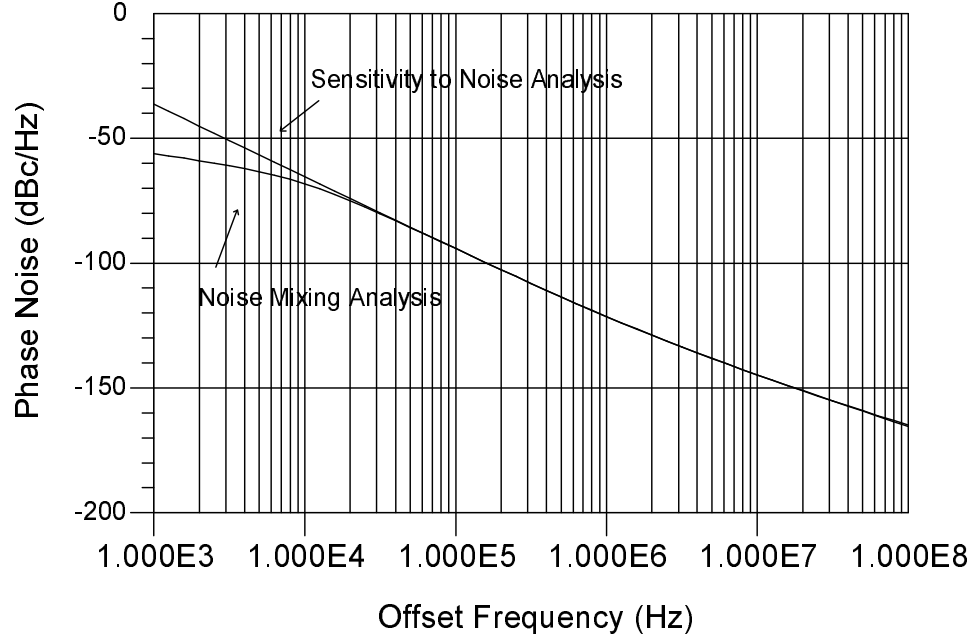


Figure 5.8: Phase Noise of VCO with Copper LIGA-MEMS Capacitor

Table 5.1: VCO Comparison

Capacitor Used	Oscillation Frequency (GHz)	Output Power (dBm)	Phase Noise @ 300 kHz offset (dBc/Hz)	FOM
CMOS Varactor	2.548	-0.955	-102.7	-190.2
Fabricated LIGA Cap.	2.557	0.121	-109.1	-195.5
Copper LIGA Capacitor	2.549	0.406	-107.5	-193.6

MEMS capacitor data have higher output power, lower phase noise and better figure of merit than the VCO with on-chip CMOS varactor. This confirms the prediction that high quality LIGA-MEMS capacitors can perform better than conventional CMOS varactors in terms of electrical properties in RF applications, providing that the capacitors are connected to the circuit core in the same method.

The comparison between the VCOs using the fabricated LIGA-MEMS capacitor and the simulated copper LIGA-MEMS capacitor data does not show a clear advantage of the high Q-factor component. The output power of the VCOs are different, which makes phase noise performance not the only consideration in comparison. Although figure of merit is used to evaluate the overall performance of the VCOs, it is not particularly valid for phase noise comparison. The VCO using the higher Q-factor copper LIGA-MEMS capacitor shows a little higher phase noise and smaller figure of merit value, though it has higher output power. It is believed that, the phase noise contributed by the fabricated LIGA-MEMS capacitor is relatively small comparing to the phase noise contributed by other noise sources. When a higher Q-factor capacitor is used, the phase noise from the capacitor is not largely reduced since it is already small, but the change, which affects the circuit behavior, may introduce more phase noise that was not considered in analyzing the resonant tank. This means that in order to further improve phase noise performance, other considerations, such as inductor Q-factor and biasing current, should be considered in addition to the capacitor.

## **5.2 Measurement Results**

### **5.2.1 Measurement**

The designed VCO was fabricated using the TSMC 0.18 micron CMOS process. The fabricated VCO comes both in loose die and 24-pin packages. Figure 5.9 shows the VCO on a loose die.

The first test was performed on the VCO in the 24-pin package since the package supplies easy connection between the chip and the testing equipments. Figure 5.10 shows the testing board on which the packaged VCO is mounted for testing. The testing board provides connections between the pins and the testing equipment. The DC power supply, biasing voltage and varactor tuning voltage are connected through BNC connectors. The differential output is connected to a SMA connector through a Mini Circuits ADT1-1WT RF transformer, which performs the balanced

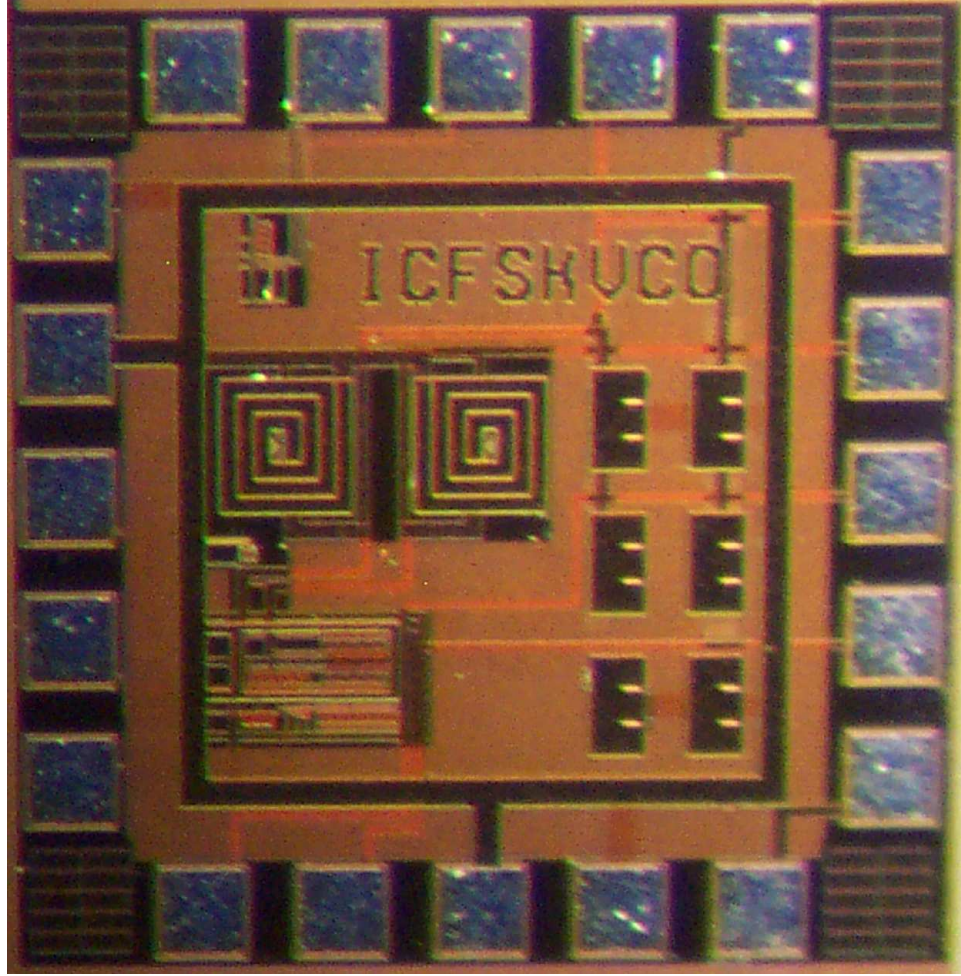


Figure 5.9: Fabricated VCO Chip

to unbalanced conversion required to connect to the test equipment. The varactor and the VCO core are wire-bonded at the corresponding pins. The DC voltage is provided by Tektronix PS280 DC power supplies. The output is connected to an Agilent 8564EC spectrum analyzer.

Due to the long bonding wires between the package pins and chip pads, this testing setup does not intend to measure any oscillation. Instead, the DC voltage levels at different points in the circuit were measured to verify the biasing conditions of the circuit. The simulated and measured DC voltages are summarized in Table 5.2, where  $V_{mirror}$  is the DC voltage at the current mirror transistors drain,  $V_{tail}$  is the DC voltage at the tail current transistor drain, and  $V_{op}$  and  $V_{om}$  are the DC voltages

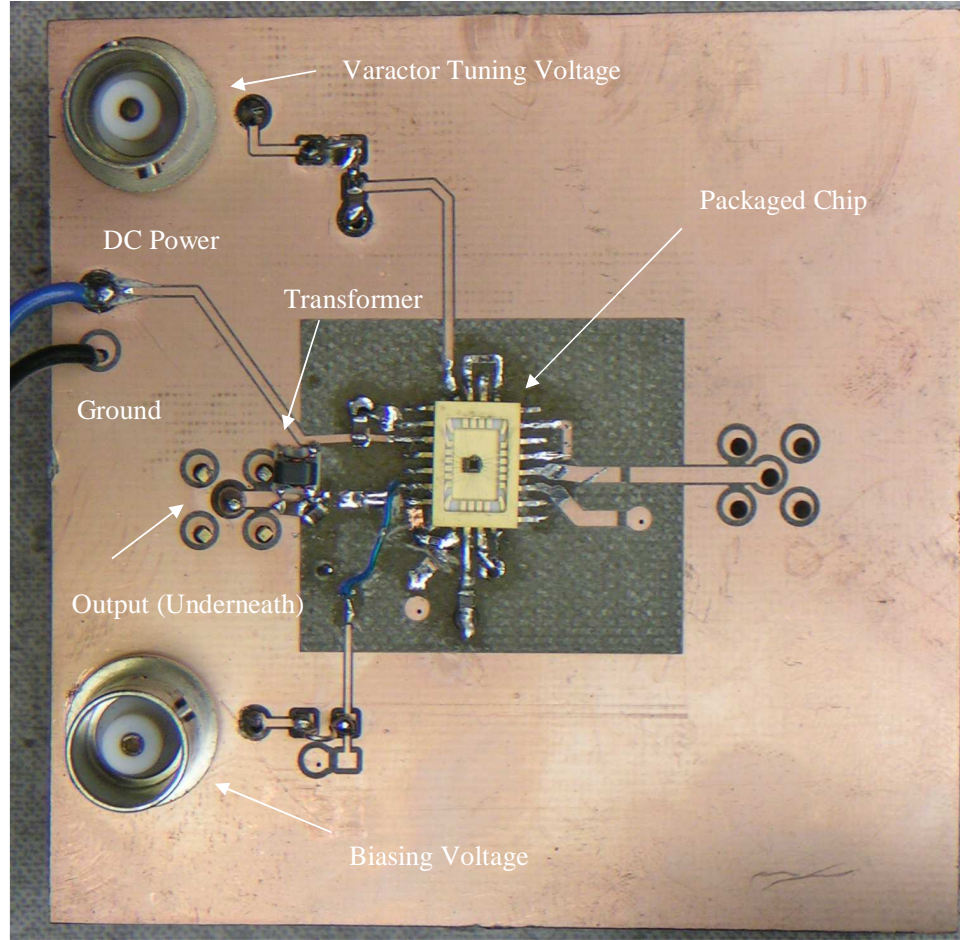


Figure 5.10: Packed VCO Chip On the Testing Board

at two output nodes.

Table 5.2: DC Voltage Levels In the VCO Circuit

DC Points	Simulated Value (V)	Measured Value (V)
$V_{mirror}$	1.41	1.41
$V_{tail}$	1.51	1.98
$V_{op}$	0.43	0.55
$V_{om}$	0.43	0.55

The measured DC voltages agree with simulation in general, with some variation. The variation may come from the difference between the simulated and actual transistors.

The next step in the testing was to wire bond the on-chip varactor to the VCO core directly at the die pads instead of through the package pins. This was achieved by manually cutting the corresponding bonding wires between the pads and the pins, and wire bond the required pads. The VCO chip was still connected to the testing equipments through the package as in the previous testing. Thus, long bonding wires between the die pads and the package pins remain, except the most critical ones that connect the varactor to the VCO core are as short as possible, minimizing unwanted bonding wire parasitics in the feedback circuit. Unfortunately, no oscillation signal was detected.

The next test was performed on a loose die. The loose die connects to the testing equipment through a new testing board shown in Figure 5.11. The loose die pads are all wire bonded to the testing board and then connect to the testing equipments similar to the previous test. This requires a large amount of manual work, but the unwanted bonding wires parasitics are greatly reduced because of the much shorter connections between the die pads to the testing board.

Unfortunately, no oscillation signal was detected at the expected frequency or any nearby frequencies. Some modifications were done to the testing board. Unnecessary connections were removed, including DC testing points and backup connections for power supply, ground, and outputs. This may help eliminate unexpected problems such as ground loop. In a later testing, the transformer was removed to further simplify the output circuit. The VCO differential outputs were connected through a  $50\ \Omega$  resistor directly. A wire loop, which can be considered as an antenna, was used to pick up any oscillation signal radiated near the circuit. No signal was found.

Attempt to wire-bond the fabricated LIGA-MEMS capacitor to the VCO circuit was not performed since no oscillation was observed with the on-chip varactor setup.

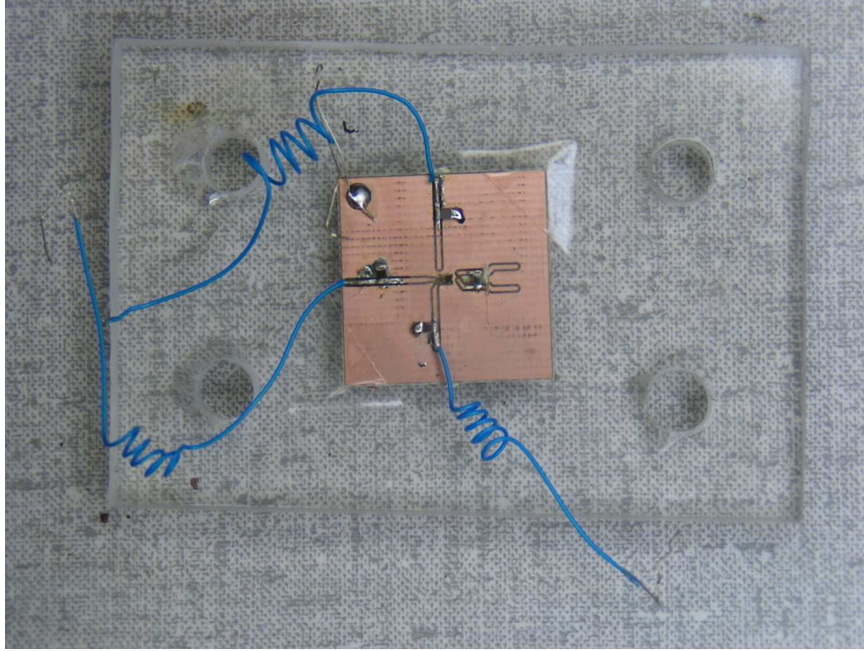


Figure 5.11: Loose Die VCO On the Testing Board

### 5.2.2 Discussion

The reason that the fabricated VCO does not oscillate is believed to be a failure in layout, whose parasitics were not properly modeled in the simulation. The negative resistance provided by the active components were not enough to compensate the extra losses that were not included in the simulation. There are several considerations that may cause the improper modeling.

The probing pads, which were designed as a backup integration/testing feature, were not included in the simulation because they appear as pieces of metal in the netlisting, which cannot be properly extracted. However, these pads may inherit parasitics which are large enough to affect the behavior of the VCO. The probing pads are made with metal-6 layer, and have the ground-signal-ground arrangement. To connect the signal pads, there are signal traces, using metal-5 layer, running underneath the ground pads. It was not realized that the parasitic capacitance between the signal traces and ground pads could be too big to be ignored, especially when the signal traces are directly connected to the feedback circuit. Later hand

calculation shows that each signal trace running underneath the ground pad has a capacitance of 0.05 pF. The signal pads, which have large area, may behave as inductors. The traces connecting the probing pads and the resonant tank are relatively long. They may behave as microwave stubs, further causing impedance loading. These factors together could seriously affect the oscillation starting condition of the VCO, especially since these parasitics are at the feedback side of the system.

The 20 pads at the edge of the chip were not properly modeled. These pads may inherit large capacitance. Although the effects of the pads that were used to connect the VCO to the testing board are usually negligible, the pads used to wire bond the VCO core and the varactor could affect the oscillation condition since they exist in the feedback circuit.

The inductor model used in the simulation could be improper. The inductor model was extracted using ASITIC, as described in the previous chapter. Although ASITIC is able to generate a lumped model for the inductors based on CMOS 0.18  $\mu\text{m}$  technology, it does not include PGS in the model. Since PGS reduces the loss due to lossy substrate, the model used in the simulation is not the complete  $\pi$ -model generated by ASITIC, but a simplified model based on the generated  $\pi$ -model. It is possible that the model used in the simulation is over-simplified, while the PGS does not reduce as much loss as originally expected. The inductor model from ASITIC is generated for a frequency of 2.7 GHz. In the simulation, this model is used with the assumption that the Q-factor is proportional to the frequency, which means the inductance and the equivalent series resistance remain constant over the simulation frequency range. This assumption could be invalid, especially in transient time when the instantaneous frequency could be far different from the steady-state frequency.

The resistance of the wires connecting different blocks of the circuit was not included in the simulation since the width of the wires was chosen to be large to ensure low resistivity, thus small resistance. The parasitic capacitance between the metal wires was not included either since the distance of the wires was chosen to be large to reduce the parasitic capacitance. However, these resistance and capacitance

may accumulate and become large enough to affect the system behavior.

Bonding wires could cause unwanted parasitics. Although these wires have been included in the simulation, the model could be inaccurate due to the fact that accurate wire length and shape is difficult to control with wire bonding. Also, due to lack of careful consideration of the pad arrangement before layout, the pads required wire bonding are in a position that increases difficulties in manual wire bonding. With the priority of avoiding bonding wires touching each other in the bonding process, bonding wires were made longer than usual and the chance of unexpected damage to the pads also increased.

The above factors are sources of parasitics that were not included in the simulation, but exist in the circuit. Some of them are difficult to model or estimate. To date, realistic estimates of some of the major unaccounted for parasitics have not completely stopped oscillation in the simulation, however, adding some of the roughly estimated parasitics into the simulation results in a serious drop in the oscillation frequency and output power. It is believed that with more complete and accurate parasitics included in the simulation, it may confirm the circuit will not oscillate.

## 6. Conclusion

### 6.1 Conclusion

The goal of this research is to develop a CMOS VCO as the first attempt to integrate CMOS RFIC with LIGA-MEMS devices and to exemplify potential advantage of LIGA-MEMS devices in RF circuits. To the author's knowledge, no LIGA passive component has been integrated with CMOS circuitries for RF applications. Previous works have concentrated on other types of MEMS devices, mostly CMOS compatible technologies. LIGA-MEMS devices benefit from their large vertical aspect ratios and thick metal layers. They are potentially suitable for microwave frequency circuits, whose performance relies on high quality passive components. However, capitalizing on these advantages requires effectively integrating such devices into RF ICs. This research focuses on investigating possible integrating methods and performance comparison the LIGA-MEMS capacitor and conventional CMOS varactor.

A VCO circuit has been designed to use either a CMOS on-chip varactor or the LIGA-MEMS capacitor as its tuning capacitor. Integration methods between the LIGA-MEMS capacitor and the CMOS VCO have been studied. It is concluded that wire-bonding is the only possible method at this stage. ADS simulation has been performed to investigate the advantages of using a LIGA-MEMS capacitor. Simulation result shows that the VCO using the fabricated LIGA-MEMS capacitor has a gain of 6.4 dB in phase noise at 300 kHz offset over the VCO using on-chip varactor. However, the simulation also shows that the VCO using a proposed higher Q-factor copper LIGA-MEMS capacitor does not have a clear advantage over the fabricated nickel LIGA-MEMS capacitor. This is a possible indication that CMOS on-chip inductor and active circuit are the major limiting factors for VCO phase

noise performance, once the initial CMOS varactor parasitics are overcome by the nickel LIGA-MEMS capacitor.

The VCO has been designed and fabricated using TSMC 0.18 micron CMOS process. The on-chip varactor has been wire-bonded to the VCO core. Unfortunately, the VCO did not oscillate in this setup. Attempts to integrate the LIGA-MEMS capacitor to the VCO core were not performed as a result.

Although the original objectives were not met, good progress has been made in investigating integrating a LIGA-MEMS capacitor to a CMOS VCO circuit. The result indicates that LIGA-MEMS device applications in CMOS circuits are promising for future work.

This research identifies the potential advantages of LIGA-MEMS devices as well as problems existing in integration. The results of this research can be helpful to future LIGA-MEMS device integration and other research in this area.

## **6.2 Recommendations for Future Work**

The following research is suggested on further investigating the LIGA-MEMS tunable capacitor integration to CMOS VCO, as well as on other possible integration of LIGA-MEMS devices and CMOS RF circuits.

### **6.2.1 Recommendations on VCO Design**

1. The VCO circuit should be considered for a redesign, focusing on accurate parameter extraction and simulation, to ensure successful oscillation. Design the VCO with larger negative resistance to compensate unexpected losses. Also consider phase noise optimization. In the previous chapters, besides the losses in the resonant tank, the active circuits make a significant contribution to the phase noise as well. This is not stated in the Leeson's phase noise model. As a result, improving resonant tank  $Q$ -factor gives less obvious improvement in the VCO phase noise performance. The new design could use other techniques such as tail current noise suppression [56] to reduce phase noise caused by active circuits, so that the advantages of using LIGA-MEMS capacitors could

be further exemplified.

2. Redesign the VCO circuit package. With the existing technologies, the most feasible method to integrate the CMOS chip and LIGA-MEMS capacitor without introducing too much additional parasitics is through flip-chip package technique. To realize the flip-chip integration, the CMOS chip and LIGA-MEMS capacitor have to be carefully laid out to match the size and connection pads. Because of the way the flip-chip integration method is implemented, the connection to the outside world, such as power supply, ground, and output, would be physically between the CMOS chip and the LIGA-MEMS capacitor. This would require careful design for future test, as it could be difficult to place the integrated VCO to the test board.
3. The VCO could eventually be designed to operate at higher frequency. The LIGA-MEMS tunable capacitor design was targeted in the 3 GHz to 10 GHz range. With higher frequencies, the advantages of the LIGA-MEMS capacitor would be more obvious as the CMOS passive components performance down grades. There are existing LIGA-MEMS tunable capacitor designs in the range of 0.2 pF to 0.6 pF [14], which are suitable for resonant tanks operating at a few GHz. On the CMOS side, with the shrink in transistor size, though the passive components would still have lower  $Q$  values comparing to MEMS devices, the active components are able to work reasonably well at higher frequencies.
4. Although the CMOS varactor has been designed to match with the LIGA-MEMS tunable capacitor, it is difficult to generate VCOs with exactly the same parameters, such as centre frequency, tuning range, and output power, using two different type of capacitors. Using the figure of merit can factor out some of the difference, however, the comparison cannot be fair in all aspects. On top of that, CMOS VCOs in practical systems will not use on-chip varactors with extra bonding wires. This makes the comparison less realistic. On the other hand, designing a VCO using LIGA-MEMS variable capacitor only and not using CMOS varactor may reduce complexity, chip area, and connec-

tions. Although there would be no direct comparison between the capacitors, the overall VCO may result good performance in respect to VCOs in similar operation range.

### **6.2.2 Recommendations on LIGA-MEMS Capacitor Design**

The LIGA-MEMS tunable capacitor layout should be modified to match the CMOS chip for integration. The modifications to be considered include:

1. The size of the LIGA-MEMS capacitor should be matched with the CMOS chip.
2. The LIGA-MEMS capacitor should include interconnection pads at proper locations for integration. The pads would also prevent the LIGA-MEMS capacitor from possible physical damage during integration.
3. The LIGA-MEMS capacitor should have physical protection that allows it be diced off the substrate, so that individual capacitor can be integrated.
4. Methods of reducing the actuation voltage for the LIGA-MEMS tunable capacitor closer to typical CMOS voltage would be advantageous, as external voltage off-chip would not be required.

### **6.2.3 Recommendations on Integrations & Fabrications**

Although beyond the scope of this research project, integrating other LIGA-MEMS devices with CMOS circuits remains an interesting research topic. Some suggestions on further exploring the potential of LIGA-MEMS devices in CMOS RF circuits are suggested based on the understanding of this research project.

1. For CMOS RF VCOs, inductors usually contribute more to phase noise than varactors because on-chip spiral inductors typically have smaller  $Q$  values than varactors. Thus, replacing on-chip spiral inductors with high  $Q$  MEMS-based inductors tends to improve VCO performance more obviously than replacing the on-chip varactor alone. In addition to many existing MEMS approaches

for high  $Q$  inductors, LIGA-MEMS inductors have been designed [43]. Integrating a LIGA-MEMS inductor, or a complete LIGA-MEMS resonant tank to a CMOS RF circuit can be considered. With LIGA-MEMS inductors replacing the spiral inductors, the VCO may perform with even lower phase noise.

2. Currently, CMOS circuits and LIGA devices can only be combined after fabrication because CMOS and LIGA fabrication process compatibility has not been realized. This introduces more process and may cause losses through interconnections. Compatibility in fabrication is desired. A post-CMOS LIGA processing method has been discussed [43]. This method proposes to fabricate LIGA devices on the reserved areas of the fabricated CMOS circuit. However, the feasibility of this method has not yet been fully investigated. Thus, further study on combining CMOS circuits and LIGA devices in processing level is required.

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