A MICROPROCESSOR-BASED SYSTEM FOR PROTECTING BUSBARS

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ABSTRACT

Electric power utilities have traditionally used electromechanical and solid-state relays for protecting busbars. Differential protection is generally used for this purpose. With the advent of digital technology, researchers and designers have made remarkable progress in the development of microprocessor-based relays. These relays use algorithms similar in principle to their electromechanical counterparts. Several algorithms, based on differential principle and suitable for implementation on microprocessors for protecting power system components, have been proposed in the past. However, a literature survey has revealed that very few algorithms for protecting busbars have been proposed in the past. Moreover, these algorithms do not have inherent immunity to current transformer (ct) saturation. The stability is achieved by using additional measures such as, using special circuitry, multiple algorithms and changing the restraint factor. These measures are not likely to be effective during severe ct saturation. The impact of ct ratio-mismatch is countered by using percentage-bias characteristics that reduces the sensitivity of the relay.

This thesis describes a technique that provides a new approach for protecting busbars. The technique uses positive- and negative-sequence models of the power system in a fault-detection algorithm. While the busbar voltages, and currents in the circuits connected to the busbar are used to detect faults, no information concerning the parameters of the power system is required. Only the arguments of the positive- and negative-sequence impedances computed by the relay are used to make trip decisions.

The performance of the proposed technique was studied by using data from simulations on the electromagnetic transient program, EMTDC. Results obtained for a sample system and an existing substation of SaskPower are presented. Different operating conditions of these systems and several busbar configurations were used in the performance evaluation. The effect of ct saturation and ratio-mismatch conditions was also studied. The results indicate that the proposed technique correctly distinguishes faults in a busbar protection zone from those outside the zone. Additionally, the technique is

stable during ct saturation and is not affected by ct ratio-mismatch. It can be applied to busbars of different configurations without any modifications.

The impact of ct saturation and ct ratio-mismatch on the performance of the proposed technique was investigated using the Discrete Fourier analysis technique. Various parameters, such as, presence of d.c. offset in the currents, mild and severe saturation of the cts, and different sampling frequencies have been considered. Also, the impact of the size of data-windows on the estimates of the current phasors is investigated. It is concluded that the decision generated by the technique is not affected by ct saturation. Also, independent computations made by individual relays makes the technique inherently immune to ct ratio-mismatch.

The proposed technique was implemented using a general purpose relay hardware. The hardware and software constituents of the prototype are presented in this thesis. The procedure for testing these relays by using a playback simulator is reported and selected test results are also included.

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Dedicated To Grandparents

Smt. Harnam Kaur	**Smt. Surjit Kaur**
S. Gajjan Singh Gill	**S. Kartar Singh Cheema**

The real owner of all achievements

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LIST OF SYMBOLS

CT, ct	Current transformer
Pt	Potential transformer
V_{kp} (pre-fault)	Phasor of the positive-sequence voltage at relay R_k before the occurrence of a fault
V_{kp} (fault)	Phasor of the positive-sequence voltage at relay R_k after the occurrence of a fault
V_{kn} (pre-fault)	Phasor of the negative-sequence voltage at relay R_k before the occurrence of a fault
V_{kn} (fault)	Phasor of the negative-sequence voltage at relay R_k after the occurrence of a fault
I_{kp} (pre-fault)	Phasor of the positive-sequence current at relay R_k before the occurrence of a fault
I_{kp} (fault)	Phasor of the positive-sequence current at relay R_k after the occurrence of a fault
I_{kn} (pre-fault)	Phasor of the negative-sequence current at relay R_k before the occurrence of a fault
I_{kn} (fault)	Phasor of the negative-sequence current at relay R_k after the occurrence of a fault
ΔV_{kp}	Phasor of the positive-sequence incremental voltage at the relay R_k
ΔV_{kn}	Phasor of the negative-sequence incremental voltage at the relay R_k
ΔI_{kp}	Phasor of the positive-sequence incremental current at the relay R_k
ΔI_{kn}	Phasor of the negative-sequence incremental current at the relay R_k
V_{th}	Thevenin voltage
TRIGGER	Indicator to detect fault
TPOS	Positive-sequence trip counter
TNEG	Negative-sequence trip counter
V_CHANGE	Pre-defined threshold for voltage change
I_CHANGE	Pre-defined threshold for current change
THRESHLD	Pre-defined limit for positive-sequence and negative-sequence trip counters
TRIP_SIGNAL	Decision of an individual delta-impedance relay [HIGH (1) or LOW (0)]
R, X	Resistive and reactive components of the impedance respectively
a	Phasor operator ($1.0\angle 120^0$)

1. INTRODUCTION

1.1. Background

An electric power system consists of four major divisions: generation, transmission, distribution, and utilization. An electric utility generates, transmits and distributes energy to a variety of consumers. Since power systems are spread over vast territories and comprise of large number of components, the probabilities of component failure, abnormalities and faults are significant. Occurrence of faults can damage equipment and injure personnel resulting in substantial monetary losses to utilities and consumers. Each system element should, therefore, be protected from damage due to faults and adverse operating conditions. Protective relays, which activate trip circuits of circuit breakers for isolating the faulted components from the power systems, are used for this purpose.

1.2. Protection of power systems

The major function of protective devices is to detect the occurrence of faults and to isolate the faulted sections from the power system. A power system is divided into protection zones, as shown in Figure 1.1, to achieve this objective. Each zone usually includes one major element and is protected by using a set of protective relays [1]. The relays, responsible for protecting a zone, operate and open circuit breakers to disconnect the zone from the remaining system when a fault occurs. The relays also alert operators and start equipment for recording the waveforms of system currents and voltages. Adjacent zones overlap to ensure that no part of the power system is left unprotected. Back-up relays are also provided to ensure isolation of the faulted equipment in case the primary relays fail to operate. The back-up relays usually operate after a time-delay and isolate not only the faulted zone but also the adjoining zone(s).

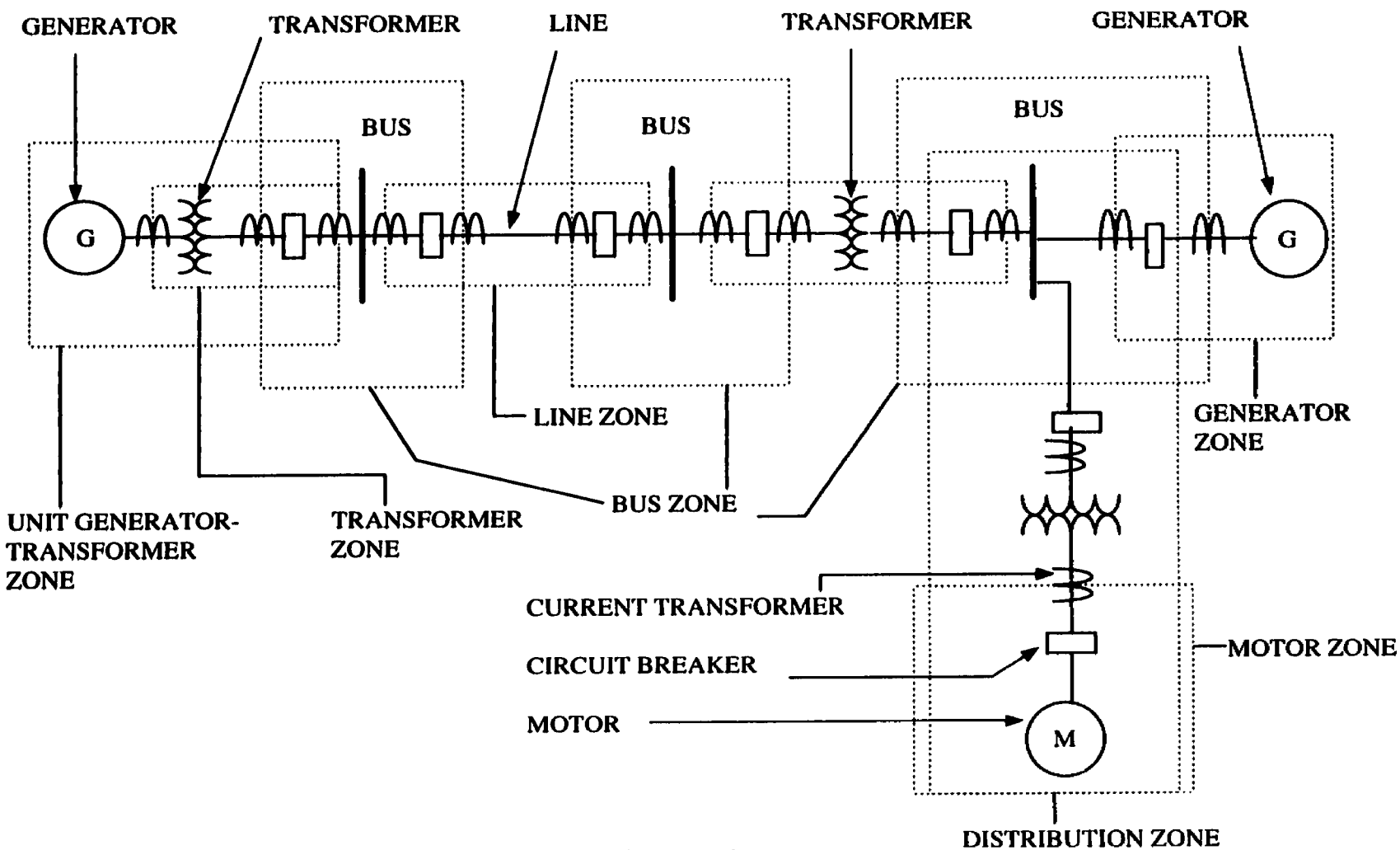


Figure 1.1. Typical relay protection zones in a power system.

Fuses, which were used as protective devices in the early developments of power systems, were, and are still, used for protecting lines and equipment. Fuses are effective and inexpensive but have inherent disadvantages, such as, their inability to discriminate between supply and load side faults, and inability to restore the circuit after the fault is cleared. Moreover, they must be replaced after each operation.

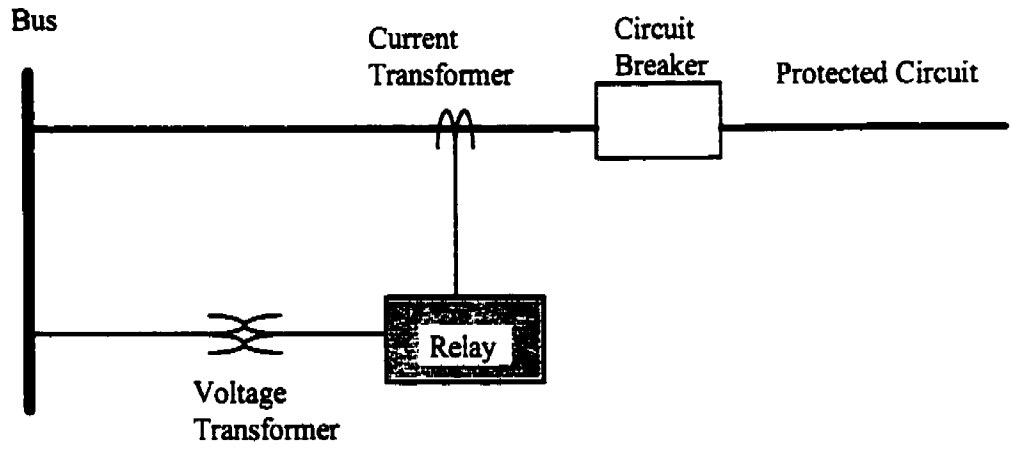
Development of electromechanical relays provided a significant improvement in the protection of power systems. The relays provided means for controlling the operating times and also provided the ability to reclose the circuits. This improved the sensitivity and selectivity of the protection schemes.

Solid state relays were introduced in early 1950s. These relays were not accepted initially by the users because of their inadequate designs and high failure rates of electronic components. Later developments utilized newer semiconductor technology and introduced improved designs. Several kinds of solid state and electromechanical relays are being used in power systems today [2]. Recent advances in the very large scale integrated circuits have led to the development of microprocessors and data acquisition chips. These have resulted in the development of digital relays.

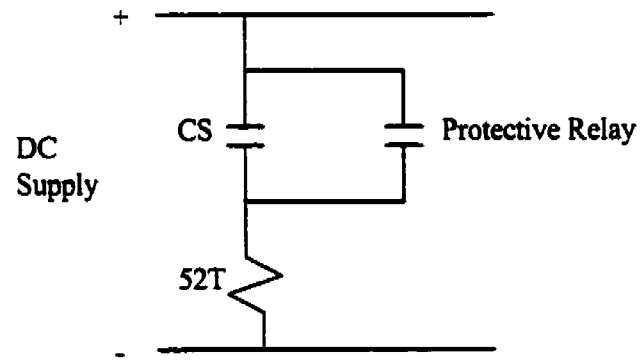
Relays energize trip circuits that result in opening the circuit breakers. The single-line diagram of a typical relay set up is shown in Figure 1.2(a). The functional block diagram of the dc trip circuit, used for opening the circuit breaker, is shown in Figure 1.2(b). The relay senses the system voltages and currents through voltage and current transformers respectively. The protective relay senses the occurrence of a fault and activates the trip relay which, in turn, closes the breaker contact (CS). This energizes the breaker coil (52T) and opens the circuit breaker to disconnect the faulted section from the rest of the power system.

1.3. A microprocessor-based relay

A relay that uses a microprocessor and software to process quantized signals for implementing the relay logic is being increasingly used in the power systems. Most of the research in the area of digital protection relates to the development of algorithms for



(a)



(b)

Legend CS -- Contactor switch
52T-- Breaker trip coil

Figure 1.2. (a) Single-line diagram of a protective relay arrangement (b) DC trip circuit.

specific applications. The following sections present a brief background of the evolution of microprocessor-based relays, their pertinent features and functionalities [3, 4, 5].

1.3.1. Historical background

In a paper [6] published in 1968, Rockefeller outlined the protection of all the equipment in a substation with a digital computer. This comprehensive paper, although speculative in nature and without any supportive experimental data, goes into substantial detail of the relaying programs for implementing on computers. This work led to the development and field installation of a system based on a process-control digital computer for protecting a transmission line of the Pacific Gas and Electric Company (PG&E) [7, 8]. The computer and its peripherals were large compared to conventional relays, used significantly more station battery power, and cost about ten times more than the conventional relays. While this uses an experimental installation, it introduced many design approaches that are in use today. Other experimental systems followed the PG&E project [9, 10, 11, 12, 13]. These systems advanced the numerical computation techniques, the economics, and the speed of tripping.

Prior to 1972, the experimental systems used curve-fitting techniques in the computer programs to estimate the phasors of voltages and currents from the quantized values of the samples [14]. The 1971 work of Ramamoorty [15] was the first to propose the use of the Discrete Fourier Transform (DFT) to compute phasors from quantized samples that is the primary computational method in most commercial microprocessor-based relays.

A commercial relay using a microprocessor appeared in 1979 [16]. This product was a frequency relay with small rotary switches for selecting set-points. This was an application in which a microprocessor could be used to produce economically viable design. As the technology of the microprocessor chips increased and the relay designers learnt how to use them, more relays appeared in the market. These included relays that performed extremely simple tasks without resorting to high-speed measurements. Hybrid

relays that measured parameters at high-speed using dedicated analog hardware also appeared in the market. Another use of the microprocessor chips was to perform complex logic for protection, monitoring and control. Minimum operating times of these relays were typically 2 to 2.5 periods of the nominal frequency. By the late 1980's, traditional and new relay manufacturers were offering sophisticated products for transmission line protection.

Most relays that are being marketed now are of the numerical type, which continuously take samples of line voltage and current signals, and quantize the samples to binary values many times in each period of the waveform. Elaborate computations are performed in microprocessors to convert the quantized values to useful measurements. These are then combined with the settings and the logical inputs to make decisions. In addition to the usual protection functions, microprocessor-based relays provide detailed records of voltage and current waveforms during faults, and calculate fault locations [17, 18]. The relay platforms also include facilities for monitoring software and hardware failures.

Many recent products offer multiple settings environments - upto eight sets of settings from which one can be selected for use in a variety of applications. One of the applications that benefits multiple settings is a relay that provides backup protection for a large number of line protection relays in a reconfigurable busbar scheme. The backup relay must protect a different line as the busbar configuration changes. The backup relay identifies the busbar configuration and invokes the appropriate settings without human intervention. Future microprocessor-based relays are likely to have facilities for performing more functions that might eliminate the need for peripheral devices, incorporate latest communications technology and have more sophisticated self-monitoring functionalities.

Some of the prominent centers of significant research in microprocessor-based relaying have been the University of Missouri [19, 20, 21], the Imperial College of Science and Technology in London [22, 23], the University of Calgary [24, 25] the University of Saskatchewan [26, 27, 28] and the University of Manitoba [29]. Major manufacturers of

electric utility equipment in USA, Europe and Japan have pursued active projects on microprocessor-based relays. Several Electric Power Utility organizations, such as the Pacific Gas and Electric Co., the Philadelphia Electric Co., and the Pennsylvania Power and Light Co. have worked on microprocessor-based relaying projects.

1.3.2. Functional blocks and operating features

The block diagram of a typical microprocessor-based relay is shown in Figure 1.3. The relay can be divided into analog input, digital input and digital output subsystems, and a microcomputer.

The input to a microprocessor-based relay consists of analog and digital signals derived from the power system. The levels of analog signals, system voltages and currents, are reduced to appropriate levels and are then applied to the analog input subsystem. The outputs from the subsystem are applied to the analog interface of the microcomputer. The digital input subsystem receives the status of circuit breakers and isolators. Isolation circuitry and transient protection is used in analog and digital input subsystems for protecting the relay from system transients. The outputs are provided through digital output subsystem.

The microcomputer, in a microprocessor-based relay, consists of a central processing unit, non-volatile memory (ROM), random access memory (RAM), analog interface, and communications hardware and appropriate software. The voltages and currents are sampled and quantized, and are fed into the microcomputer. In most digital relaying applications, the values of quantized samples complete with time stamps are stored in a RAM. These are transferred to permanent memory storage (local or remote) as soon as possible. A nonvolatile memory, ROM, is used for storing relay programs and settings. The relay logic is executed in the central processing unit.

Communication link enables the relay to share information with other devices. A self-diagnosis software resides in the relay and checks integrity of the relay at regular intervals. This feature allows the relay to remove itself from service, when a malfunction

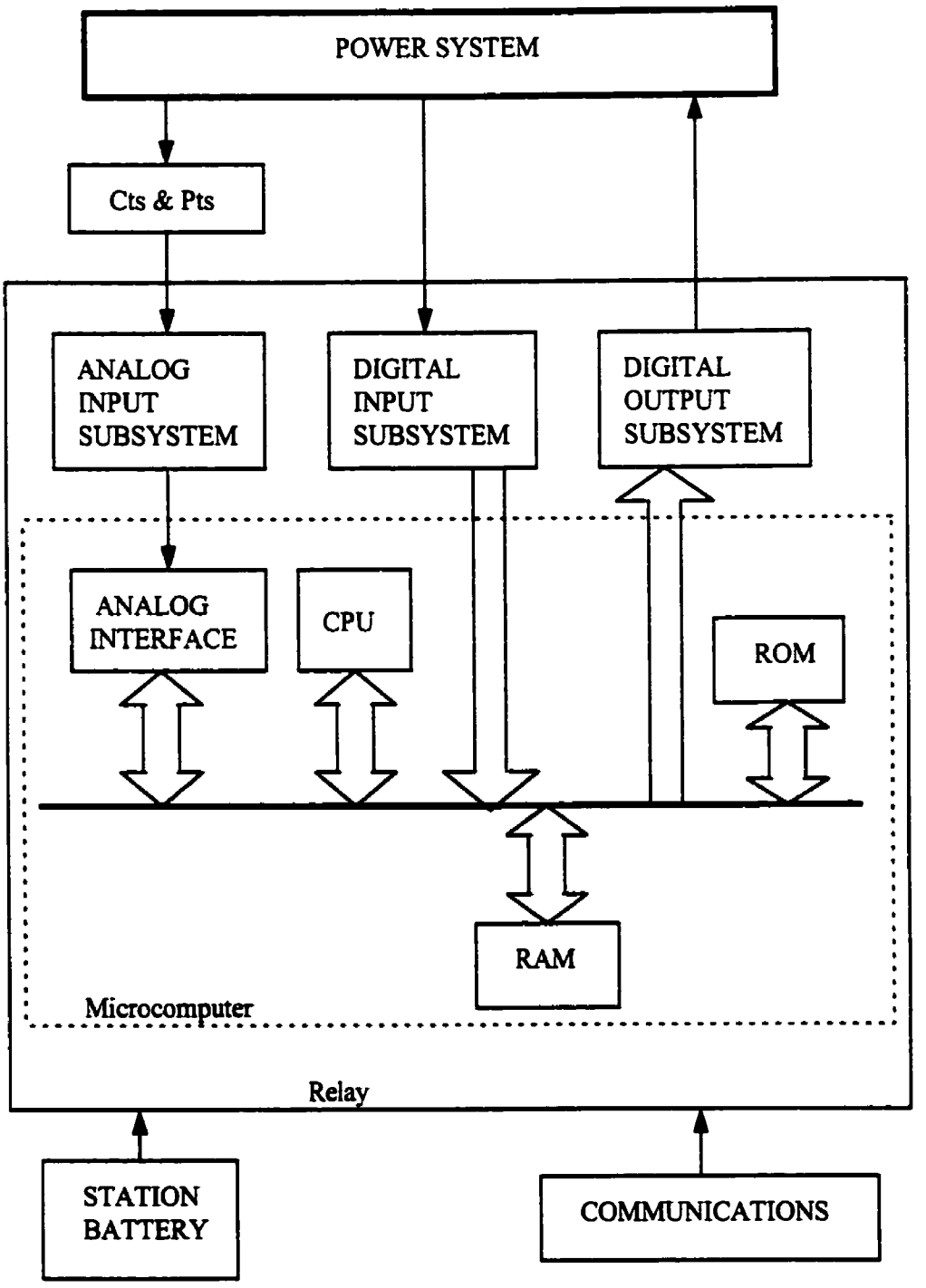


Figure 1.3. Typical functional block diagram of a microprocessor-based relay.

(component failure) occurs, and to alert the control center. Microprocessor-based relays are usually powered from the station battery which is provided with a battery charger. This ensures that the relays will operate during outages of the station ac supply.

1.3.3. Benefits

A microprocessor-based relay provides several benefits. These benefits can be summarized as follows:

(1). Economics

The cost of digital hardware has been steadily decreasing. The economic consideration has become favourable to the increasing acceptance of microprocessor-based relays in the utility industry.

(2). Performance

Properly designed microprocessor-based relays perform at least as well as the presently available electromechanical relays. The performance in this context includes operating speed, security and improved operating features resulting from the use of digital processors. For example, memory action is provided in a microprocessor-based relay without a major design effort; a complex operating characteristics is easily programmed in a microprocessor-based relay.

(3). Reliability

Digital equipment is perceived to fail more frequently than the components of electromechanical relays. However, most microprocessor-based relays are designed to monitor themselves at regular intervals by executing the software in conjunction with pre-specified data and comparing the results with those expected from a properly functioning device. In the event of results differing from the expected values, the microprocessor-based relays alert the operator of the equipment failure or impending failure. System reliability can be further increased by the relay monitoring its peripherals. These features increase the reliability but, unfortunately, increase the hardware and software costs also.

(4). Flexibility

Microprocessor-based relays can include multiple characteristics and have an option to select any one of those characteristics. Another factor that affects flexibility is the possibility of replacing the software of a microprocessor-based relay and changing its entire nature. Because some inputs to the relays in a substation are identical, a single transducer can provide an input to all microprocessor-based relays. It is also possible to design relays that can accept inputs from alternate devices in the case of failure of a transducer. These features increase the hardware and software costs that must be justified by the improvements in system operation.

(5). Background tasks

Since microprocessors handle the communication functions with ease, several microprocessor-based relays and systems are designed to collect data and transmit it to a prespecified location as a background task. Another task performed by some microprocessor-based relays is the post-fault analysis of the data collected during a fault. The relay computes the distance of a fault and provides the information for use by maintenance personnel immediately if the fault is of permanent nature and for future use if it is of temporary nature. Most microprocessor-based relays also collect sequence of events information locally, analyze it and provide the details and the results to a control computer.

(6). Byproducts

Microprocessor-based relays use digitized data that can be received over fiber optic links from electronic transducers installed in the substation. This approach results in savings from cabling costs and provide impetus for developing unified transducers and protection systems in the future.

1.4. Objective of the research

As pointed out in the previous sections, the protection of several elements of a power system is of paramount importance. The busbars, where various circuits converge, are a critical element of each power system. Since busbars are common nodes among

different circuits, occurrence of a fault on a busbar interrupts the supply to all circuits connected to that busbar. It is, therefore, necessary to provide an effective protection system for protecting busbars. Factors such as the use of different busbar configurations and saturation of cts involved in the protection scheme make the protection of busbars a complex issue. Appendix A presents a brief outline of busbar arrangements.

With the advent of digital technology, researchers and designers have made remarkable progress in the development of suitable algorithms for use in microprocessor-based relays. These algorithms use principles similar to their electromechanical counterparts. Significant improvements have taken place in transmission line and transformer protection but busbar protection using digital techniques has received almost no attention. A literature survey has revealed that very few algorithms for protecting busbars have been proposed in the past. Moreover, these algorithms are adversely affected by current transformer saturation and ratio-mismatch conditions. The reported algorithms use special circuitry and techniques to ensure correct relay operation during ct saturation.

The objective of the proposed research was to develop a microprocessor-based busbar protection system suitable for correctly identifying faults occurring inside and outside the protection zone of a busbar. The proposed algorithm must be stable during ct saturation and ct ratio-mismatch conditions. The theoretical basis describing the effect of these conditions on the proposed algorithm was to be developed and verified by carrying out studies consisting of different types of faults and their locations, and for different busbar and power system configurations. Also, the algorithm should be implementable in real-time and should provide decisions in reasonable time.

1.5. Outline of the thesis

The thesis is organized in seven chapters and ten appendices. The subject and organization of the thesis are described in the first chapter. It also presents a brief description of protection practices in power systems and important conclusions drawn from the review of literature on algorithms proposed in the past for digital protection of busbars.

Chapter 2 gives an overview of busbar faults and outlines the essential requirements of a busbar protection system. It also presents a review of the conventionally used differential protection scheme with respect to its underlying principle, limitations and associated remedies. A brief review of the previously proposed digital algorithms for busbar protection is included and their pertinent characteristics are discussed.

A fault-detection technique for protecting busbars is proposed in Chapter 3. The technique uses the concept of symmetrical components. The fault-detection characteristics of the proposed technique are presented. The procedure followed by the algorithm are described in a flow chart. Various computations performed to realize the technique are also described in detail.

The impact of ct saturation and ct ratio-mismatch is vital for all protection techniques. Chapter 4 presents a detailed analysis of the technique's performance when cts saturate or their ratios do not match. Discrete Fourier analysis technique was used to analyze the impact of ct saturation. Waveforms of currents from not-saturated and saturated cts were used as inputs, and the relative magnitudes and arguments of the computed phasors of currents were compared. Parameters, such as, dc offset in currents, mild and severe saturation of cts and different sampling frequencies were considered in the analysis. Also, data-windows of different sizes were considered. The reasons for the technique's stable performance during ct saturation and ratio-mismatch conditions have been established in Chapter 4.

Chapter 5 describes system modeling and data processing steps that are used for evaluating the performance of the proposed technique. The electromagnetic transient simulation package, EMTDC, was used to generate simulation data. Studies were conducted for two different power system configurations which included a sample system model and a SaskPower system model about its BRADA substation. Various types of busbar arrangements and operating conditions were used. Results obtained from the use of the simulated data are presented and discussed. The impacts of ct ratio-mismatch and ct saturation are also included.

The hardware and software used to build a prototype busbar protection relay using the proposed technique are described in Chapter 6. The test set-up and the testing procedure are explained. Settings of instrument transformers used for reducing the voltages and currents to the relay level are outlined. The test results obtained by implementing the developed protection system are presented in the chapter.

A brief summary of the conducted research and important conclusions drawn thereof are outlined in Chapter 7. This chapter is followed by a list of references. Appendix A presents a brief outline of busbar arrangements. The concept of symmetrical components, used for analyzing an unbalanced three-phase system by transforming it into a set of balanced networks, is explained in Appendix B. These networks, called sequence-networks, are briefly defined in this appendix. Appendix C describes the Least Error Squares (LES) algorithm which was used for estimating phasors. The design and frequency response of the anti-aliasing filters, used for off-line processing of the data, are presented in Appendix D.

The configuration and data of the power systems used for verification of the proposed technique are listed in Appendix E. An introduction to the EMTDC and ct model used in the simulations is given in Appendix F. Additional test results from simulations are provided in Appendix G. The hardware and software used for testing of the relay software is described in Appendix H. Appendix I describes the Real Time Playback (RTP) Simulator used for testing the implemented busbar protection system. Appendix J illustrates additional results obtained from the real-time testing of the developed protection system.

Specific contributions made by this thesis are as follows.

- An improved technique for protecting busbars has been developed. The technique is described in Chapter 3.
- A digital algorithm based on the proposed technique is also reported in Chapter 3.
- A detailed analysis showing the effect of ct saturation on the proposed technique has been carried out. This is presented in Chapter 4 and verified by the tests reported in Chapters 5 and 6. The effect of ct ratio-mismatch on the proposed technique is also

studied. The stable performance provided by the technique during ct saturation and ct ratio-mismatch is verified.

- A PC based fault-detection system that uses the proposed technique was designed, implemented and tested. The details are reported in Chapter 6.

1.6. Summary

This chapter has briefly introduced the concepts of power system protection. The evolution of microprocessor-based relays and their important features are described. The latest trends in the area of microprocessor-based protection are briefly mentioned. The importance of busbar protection has been underlined. The objectives of the reported research are outlined. The organization of the thesis is described and the specific contributions made by this research project are enumerated.

2. BUSBAR PROTECTION

2.1. Introduction

Faults on busbars are rare. However, an occurrence of a busbar fault can lead to a major shutdown. A bus-protection system, therefore, should be of high integrity. This chapter presents an overview of busbar-faults and essential requirements for a busbar protection scheme. Differential protection, conventionally used for protecting busbars, is briefly described. The limitations of this scheme and the additional features incorporated in differential relays are outlined. The previously proposed algorithms used in numerical bus-protection relays are also reviewed in this chapter.

2.2. Busbar faults and protection requirements

Busbar faults occur infrequently and account for only a small percentage (6 - 7 %) of power system faults [30]. Statistics on busbar faults are not widely published, but one that shows the relative frequency of different types of faults is illustrated in Table 2.1.

Table 2.1. Busbar fault statistics [31].

Reported Cause of Fault	Type and Number of Faults					Tot. No.	Tot. %
	1LG	2LG	3LG	3PH	unknown		
Flashover	20	6	1	—	—	27	21.0
Breaker failure	16	2	2	—	—	20	15.5
Switchgear insulation failure	19	2	—	—	1	22	17.0
Other insulation failure	4	1	1	3	—	9	7.0
Current Transformer failure	3	—	—	—	—	3	2.3
Disc. opened or grounded	8	1	5	1	—	15	11.6
Safety grounds left On	6	1	8	—	—	15	11.6
Accidental contact	5	—	2	—	—	7	5.4
Falling debris	4	1	—	1	—	6	4.7
Miscellaneous/unknown	2	1	—	1	1	5	3.9
Total for each fault type	87	15	19	6	2	129	
Percentage for each type	67.4	11.6	14.7	4.7	1.6		100.0

These statistics show that a majority of busbar faults short-circuit one of the phases to ground. The causes of the faults can be classified in the following categories.

(i) Insulation failure due to deterioration of material,

(ii) Flashover caused by prolonged and excessive over-voltages,

(iii) Failure of a circuit breaker to clear fault currents leading to its short circuit,

(iv) Human errors in operating and maintaining switchgear,

(v) Foreign objects falling across busbars and

(vi) Contact by animals, etc.

Damage to the equipment depends on the fault-duration, the fault-level and the withstand capability of the switchgear. The isolation of a busbar disrupts all the circuits connected to the busbar. The busbar protection system, therefore, must be carefully monitored to prevent inadvertent operations. A scheme that is simple in design and easy to apply is most likely to provide reliable service. To meet these requirements, a bus-protection system must satisfy the following criteria.

(i) High speed for promptly clearing faults to minimize damage and maintain system stability,

(ii) Stable for all external faults to avoid unnecessary interruption of supply,

(iii) Proper discrimination between zones - tripping a minimum number of circuit breakers, and

(iv) Reliable operation - avoid extensive damage to equipment, danger to personnel and disruption of service.

Differential protection is by far the most common method of providing busbar protection. A brief review of the differential principle is presented in the following section. Limitations and additional features that are incorporated in differential relays to prevent incorrect operations are also described.

2.3. Differential protection

Differential protection is invariably a prime candidate for protecting all components of power systems and is often selected to provide primary protection [32]. Traditionally, differential protection has been used for protecting most power transformers

and generators. During the last five years, differential protection of transmission lines has also become a viable technique. The basic principle of differential protection is discussed in this section. Special features that are incorporated in differential relays to prevent incorrect operations are briefly discussed.

2.3.1. The differential principle

The currents at the extremities of a zone are reduced in level by current transformers (cts) and are continuously compared. The operating coil of the relay is connected to the secondary windings of the cts in such a way that the current flowing through it is equal to the sum of the secondary currents of the cts. The differential principle can be described with the help of Figure 2.1.

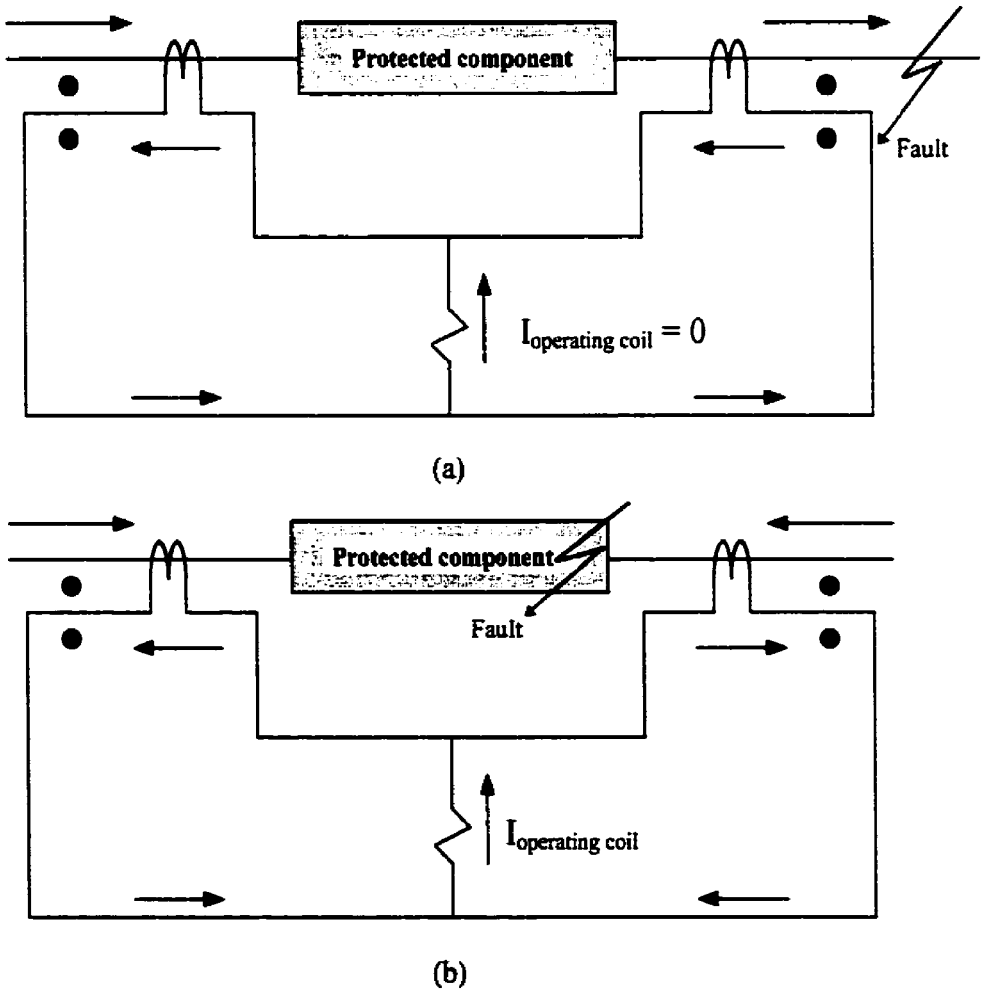


Figure 2.1. A basic differential scheme during (a) normal operation and external faults, and (b) internal faults.

Net current flowing through the operating coil of the differential relay is zero during normal operation and during external faults. A fault in the protection zone upsets this balance and causes a current to flow in the operating coil of the relay. This is shown in Figure 2.1(b).

2.3.2. Issues

A small amount of current normally flows in the operating coil because of mismatch of ct ratios and differences in characteristics of the cts. Phenomena of ct saturation and ratio-mismatch, which cause the differential relays to operate incorrectly, are described in the following sections.

2.3.2.1. CT saturation

Ct saturation occurs when the flux density required to produce the secondary current exceeds the limit that can be provided by the ct core. Whether, or not, a given ct will saturate depends on the following factors:

(i) CT ratio,

(ii) Core cross-sectional area,

(iii) Connected burden,

(iv) Level of remanent flux,

(v) Level of dc offset in the current, and

(vi) Material of the core.

A simplified circuit of a current transformer is shown in Figure 2.2 [33]. L_m represents the non-linear magnetizing inductance. R_m is the iron loss equivalent resistance. The currents that represent the reactive and active components of the magnetizing current are shown as I_m and I_r respectively. R_b is the load connected to the ct that is made up of the impedances of all leads and the relay coils. R_p and L_p represent resistance and leakage inductance of the primary winding. R_s and L_s represent the resistance and inductance of the secondary winding. E_s and V_s are the induced emf of the ct secondary winding and the voltage at the ct terminals respectively.

The primary winding of a ct is in series with the line and, therefore, carries the current that flows in the line. When a short-circuit occurs, the line current becomes large,

which also flows in the ct primary (I_p). The secondary current (I_s) also increases. Ideally, the secondary current should be proportional to the primary current. The ct must develop sufficient voltage (E_s) to make this current to flow in the secondary circuit. To generate this voltage, part of the primary current becomes the magnetizing current (I_e) that produces flux in the core of the ct.

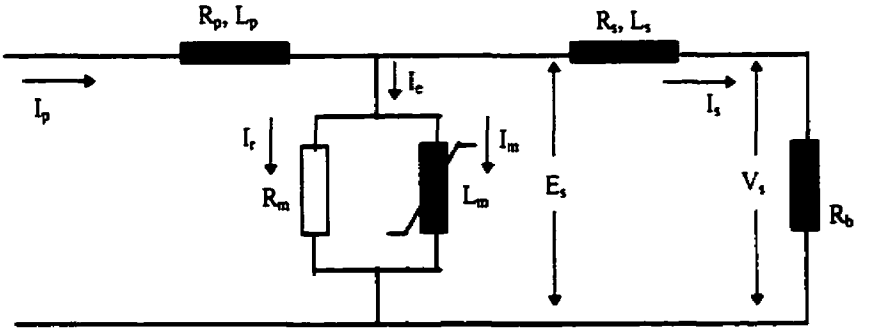


Figure 2.2. An equivalent circuit of a current transformer.

Normally, the magnetizing current is small and the secondary current remains proportional to the primary current for all practical purposes. If a ct has to develop a large voltage to overcome the voltage drop in the secondary circuit, the core flux levels must be high. If the flux approaches the saturation level, the exciting current (I_e) becomes large and the secondary current decreases. The secondary current of the ct in this case is less than its level had the ct not saturated. As the primary current increases beyond the saturation level, the core saturates during a part of the cycle only [34]. The result is that the secondary current becomes distorted.

Since the cts used in differential protection schemes are in series with the line, they carry large amounts of currents during internal and external faults. A high level of current can cause a ct to saturate resulting in different secondary currents out of the two cts. This results in the flow of a differential current in the operating element of the relay while the fault is outside the protection zone. Saturation of cts can, therefore, cause the differential relays to operate during external faults. It is essential that steps be taken to detect ct saturation and block the relay operation when it is necessary.

2.3.2.2. Ratio-mismatch

The ratios of various cts used in a differential protection scheme should be so selected as to provide no differential current during normal-operation and through-fault conditions. Any mismatch in the ratios of cts will result in a net current in the differential coil causing the relay to operate during through faults. The realization of exactly matching ct ratios is difficult in practice. As such, there always are some currents in the differential coils of the relays. To avoid incorrect operations of differential relays, additional features are employed; these are described in the next section.

2.3.3. Remedies

It is observed that the operation of a differential protection scheme in the simple form of Figure 2.1 is adversely affected by the characteristics of the cts. The lengths of the leads, connecting the cts to the relay, are not usually equal. The VA burdens on the cts, therefore, are not equal. This causes the cts to produce different outputs for the same levels of input currents. The consequence is that some current flows in the operating element of the differential relay during through faults.

The effect of ct saturation can be reduced by increasing the cross-section of the ct core. Also, a stabilizer resistance can be used in series with the operating coil of the relay, which increases the relay burden and reduces the difference between the magnetizing currents of the cts.

Differential relays are provided with a percentage-bias feature to avoid tripping due to ratio mismatch. The differential relays include restraints that are derived from the arithmetical sum of all the currents, which are rectified and added. The operating current is the vectorial sum of all the currents and the restraining current is their scalar sum. The differential current required to operate the relay must exceed a set percentage of the total restraint. The ratio of the operating current and restraining current expressed as a percentage is usually called the slope of the relay characteristic. A typical percentage-bias characteristic is shown in Figure 2.3.

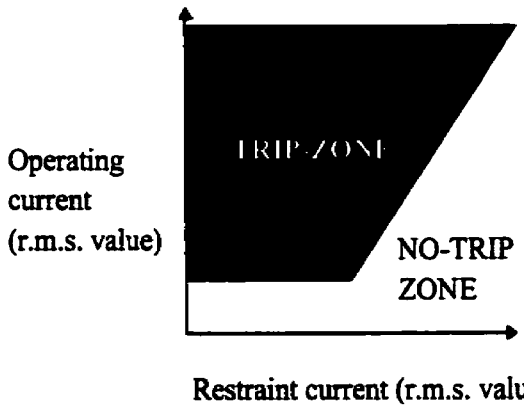


Figure 2.3. A typical percentage-bias differential relay characteristic.

The slope is adjustable and is usually made large enough to prevent the relay from operating due to ct mismatches. The differential current caused by ct ratio mismatch is countered by the restraining current keeping the relay from operating incorrectly [35]. This feature increases the security of the relay while it keeps its sensitivity at a reasonable level.

2.4. Digital algorithms for busbar protection

A literature survey has revealed that very few algorithms for protecting busbars have been proposed in the past. These algorithms are based on differential protection, and can be broadly divided into the following categories.

(i) Bay-oriented busbar protection system,

(ii) Half-cycle differential algorithm and

(iii) Algorithms using special circuitry.

These algorithms are adversely affected by current transformer (ct) saturation and ratio-mismatch conditions. As such, the algorithms use measures to ensure correct relay operation during ct saturation conditions. Both, special circuitry and techniques are used for the purpose. A brief description of these algorithms is provided in the following sections.

2.4.1. Bay-oriented busbar protection system

A numerical technique utilizing two independent algorithms has been proposed by Peck, Nygaard and Wadelius [36]. The proposed protection system is bay-oriented and

consists of installating bay units (BUs) close to the switchgear. The arrangement of the system using these units is shown in Figure 2.4. The bay units interface with the switchgear and act as data-acquisition units. They also process the inputs. The currents, applied to the bay units via current transformers, are filtered and then quantized. The samples are time-stamped so that appropriate samples are used by a central unit (CU) while implementing the protection algorithm. The central unit consists of a number of central processing units (CPUs), each performing a dedicated part of the protection algorithm. A separate master CPU supervises the other CPUs and enables the final trip command.

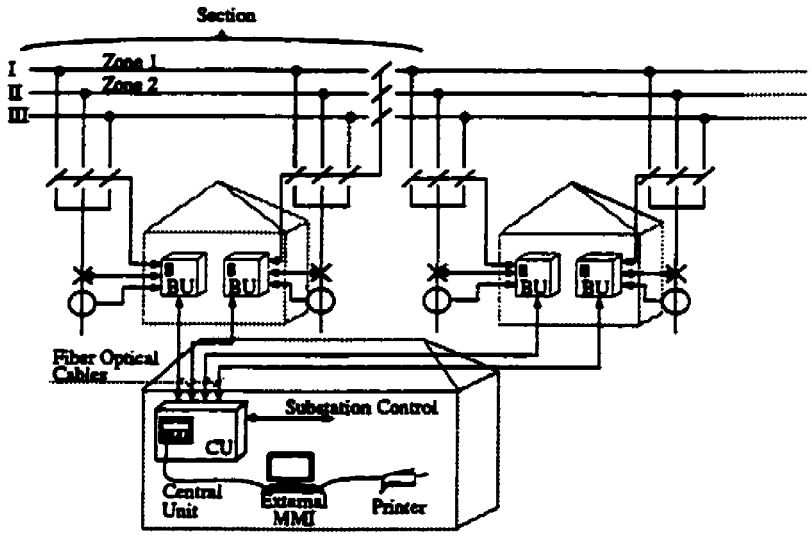


Figure 2.4. Busbar protection system arrangement using bay units [36].

Two protection algorithms are used for fault-detection; these are based on measuring the differential current and utilizing a restraint current to provide stability. One algorithm uses the instantaneous current samples and the other uses the fundamental frequency phasors calculated by the Discrete Fourier Transform.

These algorithms can be expressed by Equations 2.1 and 2.2.

$$RF = \frac{I_{Diff}}{I_{Rest}} = \frac{\left|\sum_{k=1}^{n} i_k\right|}{\sum_{k=1}^{n} |i_k|} \qquad (2.1)$$

$$RF = \frac{I_{Diff}}{I_{Rest}} = \frac{\left|\sum_{k=1}^{n} F_k(i_k)\right|}{\sum_{k=1}^{n} |F_k(i_k)|} \qquad (2.2)$$

where RF is the restraint factor, n is the number of circuits, and i_k and $F_k(i_k)$ are the instantaneous samples and fundamental frequency phasors respectively of each phase.

Every bay unit continuously monitors the currents of its bay. The computed values are transmitted to the CU, which calculates the sum of the currents and monitors the differential current. In the event of a fault, the differential current increases. As soon as its value exceeds a threshold and/or current in one or more bay units exceeds a threshold, implementation of the instantaneous and full-cycle algorithms is started. The instantaneous algorithm is executed only once. It uses three consecutive current samples taken by the bay units before any ct can saturate. The integrity of the current values is secured due to high sampling rate (48 samples/cycle) in the BU. The full-cycle algorithm is repeatedly applied until the fault is identified. The stability for ct saturation during external faults is achieved by adjusting the trip characteristics and the restraint factor used in the trip criteria.

Man machine interface (MMI) is used to communicate with the busbar protection system and is connected to the CU via a fibre-optic cable. The protection system can be configured and tested by using software accessed via the MMI.

2.4.2. Half-cycle differential algorithm

Forford and Linders [37] described a half-cycle bus differential relay which evaluates the situation in the period from the inception of the fault to the onset of ct saturation. The proposed relay makes the required measurements prior to ct saturation and rejects the information received from the cts when they are saturated.

The relay is based on high-impedance differential current principle. A schematic of this relay system is shown in Figure 2.5. It employs two line diodes for each phase of each circuit. These provide full wave rectification of each current in the relay. The total input

current develops a restraining voltage across a resistor. Any differential current due to ct ratio error or internal fault will flow through an adjusting resistor and a current isolating ct. The differential current output of this ct is rectified by a full wave bridge and is applied to resistor (R_D). The voltage across this resistor is used as differential voltage. The differential (V_D) and restraining (V_S) voltages are compared and used for closing the tripping contacts. The stability during ct saturation is achieved by increasing the resistor (R_D) to increase the restraint. During internal faults, the secondary fault current flows in the high-impedance differential circuit and the relay operates. The ability of this relay to operate prior to ct saturation is its main feature.

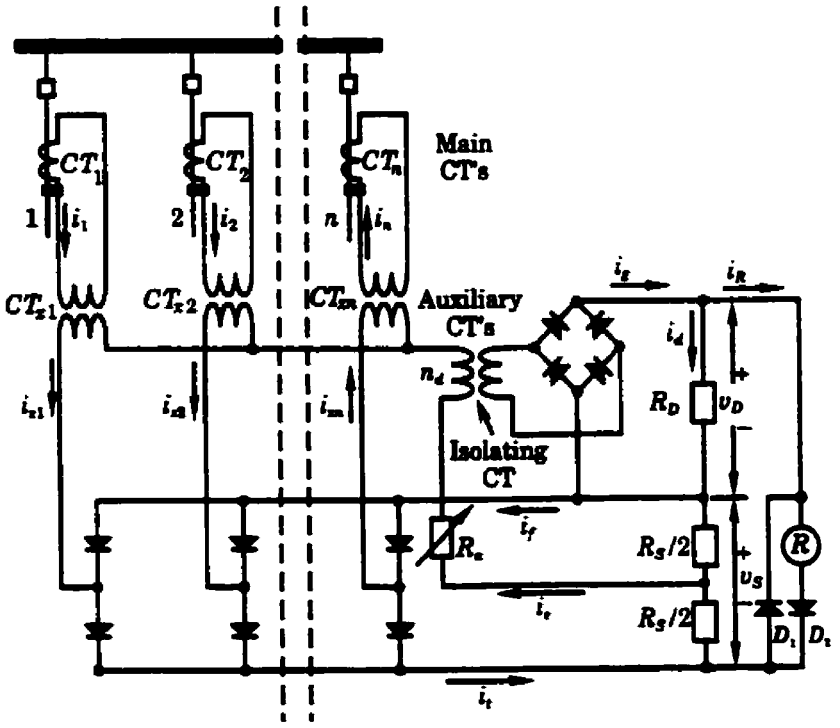


Figure 2.5. Schematic diagram of the half-cycle bus differential system [30].

2.4.3. Algorithms using special circuitry

Some digital algorithms that use special circuits to prevent improper operation of the relays during ct saturation have been proposed. These circuits include saturation detectors, countermeasure elements, and RC circuits. A brief review of these algorithms is presented in this section.

The waveform of a secondary current of a saturated ct consists of outputs of the 'saturation' and 'non-saturation' periods. There are no differential currents during the 'non-saturation' periods. Utilizing these facts, the low-impedance solid-state differential relays, which incorporate a ct saturation countermeasure have long been proposed. This principle has been implemented in a digital busbar protection [38] as well.

The countermeasure element, included in the relay, contains a waveform discriminating unit, which prevents an unwanted tripping when the differential current is significant due to ct saturation during external faults. The working of the waveform discriminating element is governed by the change in the instantaneous values of the differential and restraining currents. However, the ct output cannot be determined during the intervals between the sampling instants in digital relays. The algorithm suggests proper ct saturation countermeasure to overcome this drawback.

Royle and Hill [39] developed a technique for busbar protection that uses electronic detectors for detecting ct saturation, and semiconductor switches to short circuit the differential path for the portion of the cycle during which the secondary current from the ct is inadequate due to saturation. Figure 2.6 shows the saturation detector in a simplified form. The input ct feeds the differential circuit via the primary winding of an auxiliary transformer whose output develops a voltage across a resistor. A capacitor is charged to peak value of this voltage.

A comparator is used to compare the voltage (V) with half the voltage stored in the capacitor. When the voltage (V) is less than 0.5 V_c, the comparator produces an output signal to close the electronic switch connected across the 'Input ct'. Pulses produced by the comparator at each zero crossing of the current waveform are of short duration and shunt negligible current from the 'Input ct'. However, when the current transformer saturates, the waveform of the voltage V collapses during part of the cycle and the pulse width increases. This increased pulse operates the semiconductor switch to prevent the flow of current while the ct is saturated.

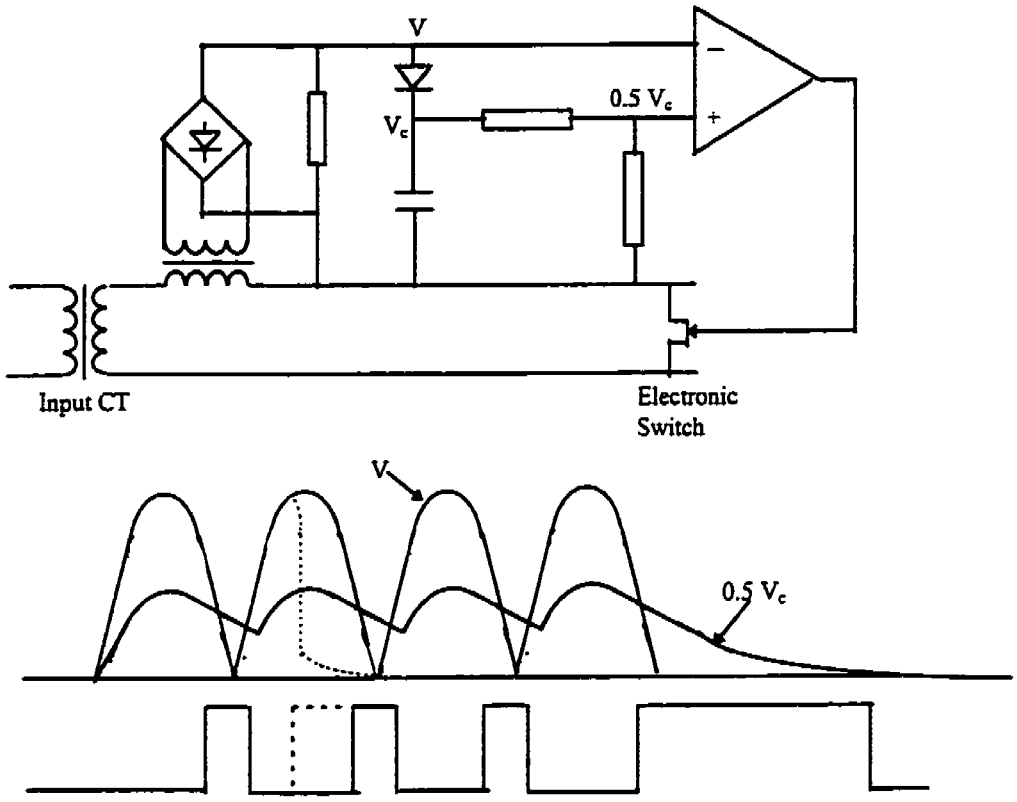


Figure 2.6. Saturation detector [39].

Kumar and Hansen [40] developed a busbar protection technique that is based on the low-impedance differential scheme. Requirements of fast trip and security against unwanted relay operations are achieved by multiprocessing. Three microcomputers are used for the purpose. The protection algorithm uses relationship between restraining and differential currents and a restraining factor. The sum of the rectified currents provides the restraining signal and the vectorial sum of the currents is rectified to provide the differential signal. The restraining signal is obtained by charging a capacitor provided in the output circuit. Undesired operations, during ct saturation, are eliminated using additional techniques. Advantage is taken of the fact that ct saturation does not set in immediately on the occurrence of the fault and a saturated ct recovers and transforms correctly at regular intervals. The method of ensuring stability assumes that the ct takes a prespecified time to saturate after the occurrence of a fault. This method, however, does not guarantee correct operation for severe ct saturation.

2.4.4. Discussion of the algorithms

Digital algorithms proposed in the past for protecting busbars have been reviewed in Sections 2.4.1 to 2.4.3. The following observations can be made from the review of the literature on these algorithms.

(i) The area of digital busbar protection has not been of active research. Very little work has been reported on the development of algorithms suitable for protecting busbars.

(ii) The phenomenon of ct saturation affects the protection schemes adversely and causes improper operations of the relays. Most algorithms proposed for busbar protection handle ct saturation by using special circuitry, and are based on the assumption that they function correctly. Use of additional circuitry in the protection scheme increases its complexity and, therefore, increases the possibility of incorrect operations due to malfunction of its components. Also, an increase in the number of components in the protection scheme increases the total cost.

(iii) No algorithm proposed in the past has inherent immunity to ct saturation. The stability of the algorithm during this condition is provided by using special means, such as, special circuitry, two algorithms working in conjunction and choice of restraint factor. Moreover, the correct operation is not guaranteed if the ct saturation is severe.

(iv) The effect of ct ratio-mismatch has not been explained for any of the previously proposed algorithms. In practice, matching the ratios of various cts of a protection scheme is an important consideration.

(v) The initial values of current and voltage thresholds are required to be selected. The correct implementation of the algorithms depends on the proper selection of these initial values.

(vi) The fact that cts do not saturate immediately on the occurrence of a fault has been the underlying principle used in some of the proposed relays.

These relays also require that resistors in their restraint circuits be adjusted to prevent incorrect operations during external faults. However, there always is a chance of selecting resistors of incorrect values that could affect the operation of the relay.

2.5. Summary

A brief outline of busbar faults and the essential requirements of a busbar protection system have been presented in this chapter. The principle of differential protection and its limitations have been described. Additional features incorporated in differential relays to ensure correct operation during ct condition have been discussed as well.

Previously proposed digital algorithms for protecting busbars have been briefly reviewed. It is noted that, unlike other power system components, the area of busbar protection has not been very active. The algorithms proposed for busbar protection use special circuitry to provide correct relay operation during ct saturation. Unfortunately, their correct operation during severe saturation of cts is not guaranteed.

3. THE PROPOSED TECHNIQUE

3.1. Introduction

The algorithms proposed in the past for protecting busbars have been briefly reviewed in Chapter 2. It is observed that no previously proposed algorithm has inherent immunity to ct saturation. The stability of the algorithms during this condition is achieved by using additional means, such as special circuitry, two algorithms working in conjunction and using restraint factors. Moreover, their correct operation on severe ct saturation is not guaranteed. The impact of ct ratio-mismatch is countered by using percentage-bias characteristics, which however reduces the sensitivity of the relay.

This chapter proposes a technique that distinguishes between the faults internal and external to the busbar protection zone. The technique [41] is based on the concept of symmetrical components, which has been employed previously for the development of protection algorithms for transmission lines [42], synchronous generators [43] and power transformers [44, 45, 46]. The technique uses positive- and negative-sequence models of the power system in a fault-detection algorithm. While the phase voltages and currents at the busbar are used to detect faults, no information on the parameters of the power system is required. The concept of symmetrical components is briefly explained in Appendix B.

3.2. Development of the technique

Figure 3.1 shows a busbar, B, which is connected to several circuits (1, 2,...j) and is protected by relays R_1, R_2, ...R_m, R_{m+1}, R_{m+2}, ...R_j that are installed on the circuits. Since these relays compute the incremental-impedances using the pre-fault and during-fault samples of the voltages and currents, they are designated as delta-impedance relays. These relays consider the current entering the busbar to be positive.

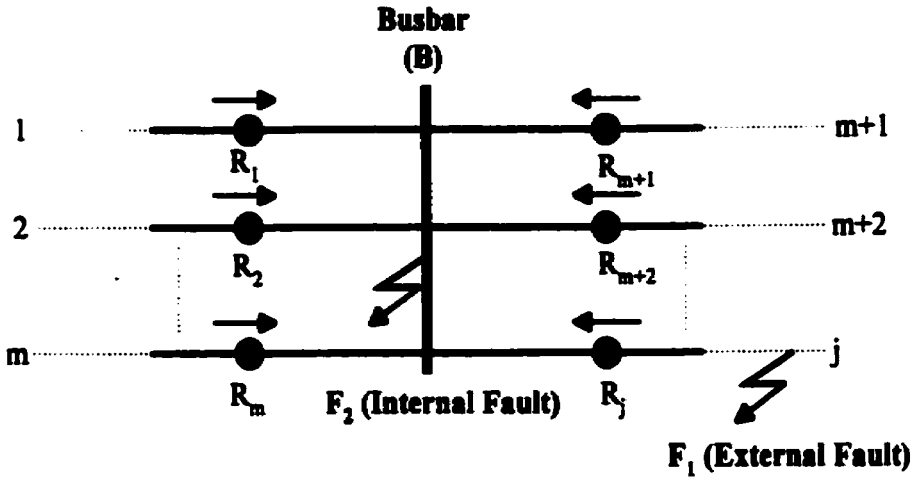


Figure 3.1. Busbar B and circuits connected to it considered for developing the proposed technique.

3.2.1. External fault

The pre-fault, during-fault and Thevenin equivalent circuits for an external fault (F_1 in Figure 3.1), on circuit j, can be represented by the sequence networks shown in Figures 3.2 and 3.3. The fault impedance Z_f, which includes the fault resistance and impedances of the sequence networks representing unbalanced faults, is shown in these figures.

The phasors of the positive-sequence incremental voltages, ΔV_{1p}, ΔV_{2p}, ..., ΔV_{mp}, $\Delta V_{(m+1)p}$, $\Delta V_{(m+2)p}$....., ΔV_{jp}, and the phasors of the incremental currents, ΔI_{1p}, ΔI_{2p}, ..., ΔI_{mp}, $\Delta I_{(m+1)p}$, $\Delta I_{(m+2)p}$....., ΔI_{jp}, at the relay locations can be defined as follows:

$$\Delta V_{kp} = (V_{kp})_{fault} - (V_{kp})_{pre\text{-}fault} \quad (3.1)$$

$$\Delta I_{kp} = (I_{kp})_{fault} - (I_{kp})_{pre\text{-}fault} \quad (3.2)$$

where:

$V_{kp\,(pre\text{-}fault)}$ is the phasor of the positive-sequence voltage at R_k before the occurrence of a fault,

$V_{kp\,(fault)}$ is the phasor of the positive-sequence voltage at R_k after the occurrence of a fault,

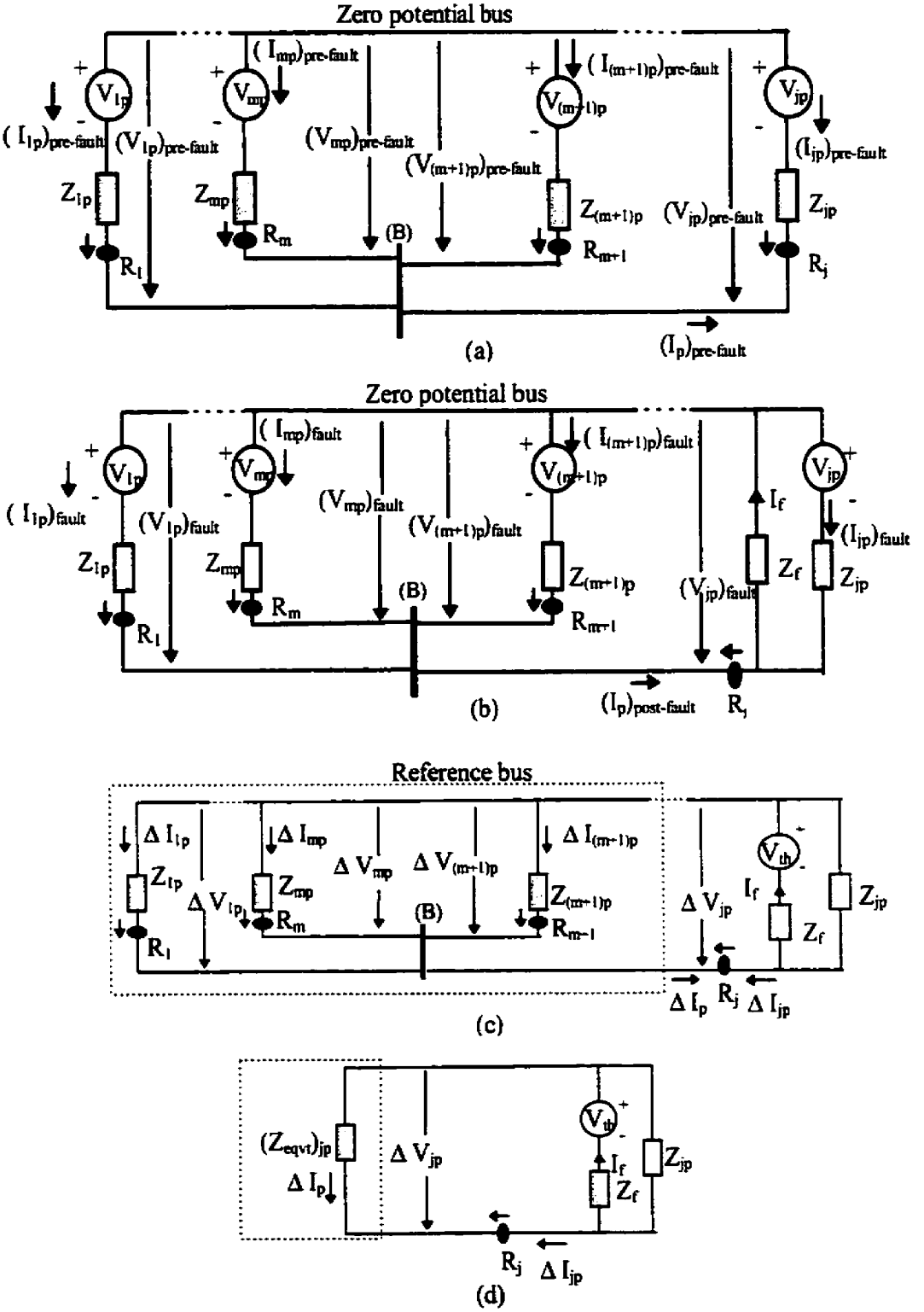


Figure 3.2. Positive-sequence (a) pre-fault, (b) during-fault, (c) Thevenin equivalent, and (d) equivalent circuits about relay Rj for an external fault at F_1.

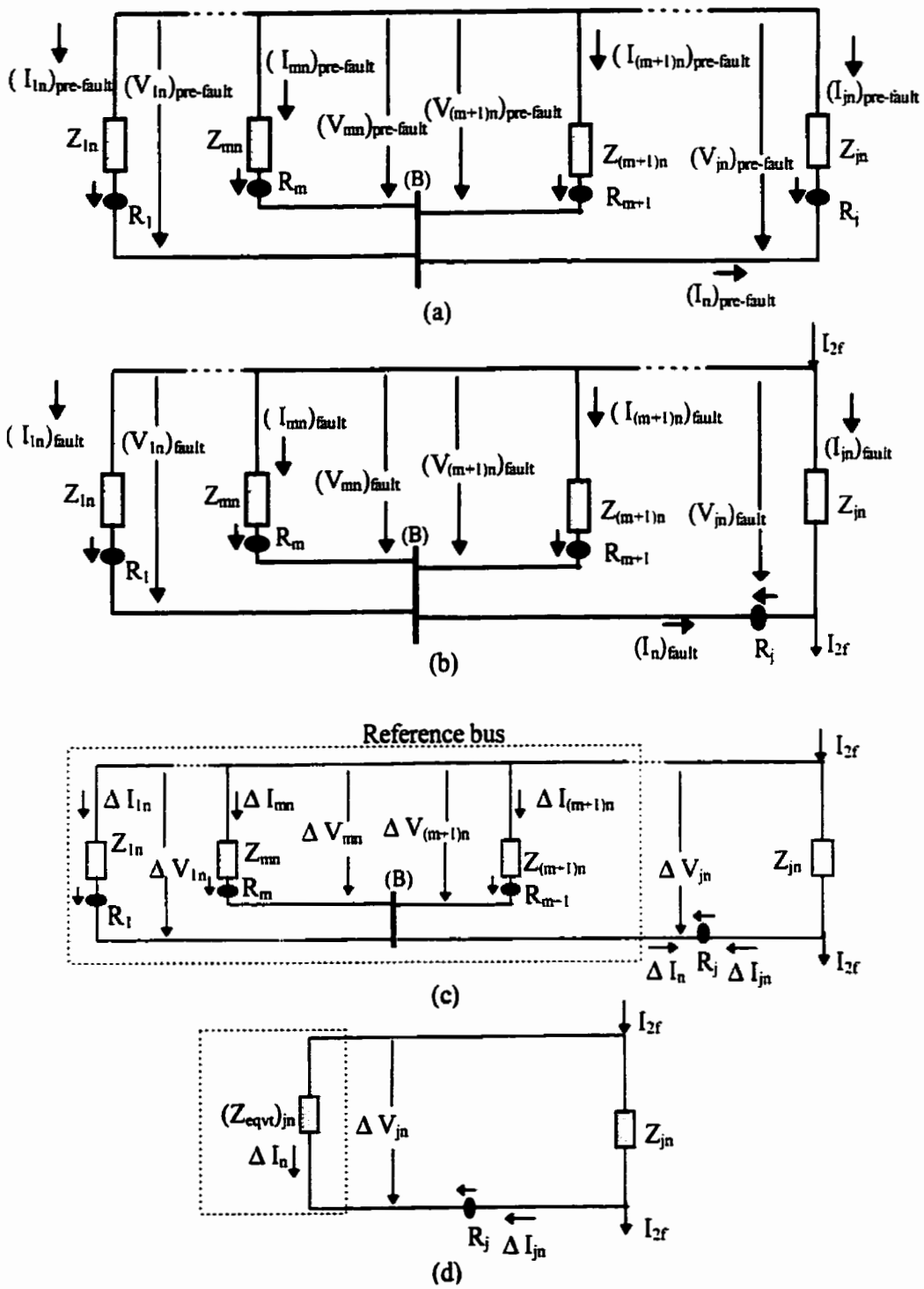


Figure 3.3. Negative-sequence (a) pre-fault, (b) during-fault, (c) Thevenin equivalent, and (d) equivalent circuits about relay R_j for an external fault at F_1.

$I_{kp\,(pre\text{-}fault)}$ is the phasor of the positive-sequence current at R_k before the occurrence of a fault,

$I_{kp\,(fault)}$ is the phasor of the positive-sequence current at R_k after the occurrence of a fault

and k=1, 2, ..., m, m+1, m+2, ...j.

Define Z_{1p}, Z_{2p}, ..., Z_{jp} as the equivalent positive-sequence impedances of the circuits and systems connected to terminals 1, 2, ... j of the busbar. It is clear from Figure 3.2 (c) that the phasor of the positive-sequence incremental voltage at relay R_1 can be expressed as

$$\Delta V_{1p} = - \Delta I_{1p} Z_{1p} . \tag{3.3}$$

Rearranging this equation provides the ratio of the positive-sequence voltage and current at the relay R_1.

$$\frac{\Delta V_{1p}}{\Delta I_{1p}} = - Z_{1p}. \tag{3.4}$$

Following a similar procedure, it can be shown that for an external fault, the ratios of the phasors of the positive-sequence voltages and currents at the relays R_2, ..., R_m, R_{m+1}, R_{m+2}, ..., R_{j-1}, which are provided on the healthy circuits, can be expressed by the following equation

$$\frac{\Delta V_{kp}}{\Delta I_{kp}} = -Z_{kp} \tag{3.5}$$

where k = 1, 2, ..., m, m+1, m+2, ..., j-1 ($k \neq j$).

The positive-sequence impedance seen by the relay R_j can be obtained by defining an equivalent circuit as shown in Figure 3.2 (d). The following equation expresses the voltage-current relationship in this case.

$$\Delta V_{jp} = (\Delta I_p)(-Z_{eqvt})_{jp} \tag{3.6}$$

where

$(Z_{eqvt})_{jp}$ is the equivalent positive-sequence impedance of the network seen from the location of relay R_j.

Because $\Delta I_p = -\Delta I_{jp}$, Equation 3.6 becomes

$$\Delta V_{jp} = (\Delta I_{jp})(Z_{eqvt})_{jp}. \tag{3.7}$$

The ratio of the phasors of the positive-sequence voltage and current as seen by relay R_j can be obtained by rearranging this equation.

$$\frac{\Delta V_{jp}}{\Delta I_{jp}} = (Z_{eqvt})_{jp} \tag{3.8}$$

The ratios of negative-sequence voltages and currents as seen by relays, except relay R_j, can be obtained by using a similar procedure. These ratios are

$$\frac{\Delta V_{kn}}{\Delta I_{kn}} = -Z_{kn} \tag{3.9}$$

where

Z_{kn} is the equivalent negative-sequence impedance of the circuits connected to terminals 1, 2, ... j-1 of the busbar,

ΔV_{kn} is the phasor of the negative-sequence incremental voltage at the location of relay R_k,

ΔI_{kn} is the phasor of the negative-sequence incremental current at the location of relay R_k

and k= 1, 2, ..., m, m+1, m+2, ..., j-1.

The ratio of the negative-sequence voltages and currents seen by relay R_j, located on the faulted circuit, can be expressed as follows.

$$(Z_{eqvt})_{jn} = \frac{\Delta V_{jn}}{\Delta I_{jn}} \tag{3.10}$$

where

$(Z_{eqvt})_{jn}$ is the equivalent negative-sequence impedance of the network seen from the location of relay R_j,

ΔV_{jn} is the phasor of the negative-sequence incremental voltage at the relay R_j and

ΔI_{jn} is the phasor of the negative-sequence incremental current at the relay R_j.

Similar procedure can be used for determining the ratios of sequence voltages and currents seen by the relays for external faults on other circuits. The preceding analysis shows that the impedance seen by the relay located on the faulted circuit will be in the first quadrant and the impedances seen by all other relays will be in the third quadrant.

3.2.2. Internal fault

Figure 3.1 shows a fault (F_2 in Figure 3.1) in the protection zone of the busbar. The pre-fault and during-fault positive-sequence networks for the internal fault are shown in Figures 3.4 (a) and (b) respectively. The Thevenin equivalent circuit is shown in Figure 3.4 (c).

Considering the equivalent circuit shown in Figure 3.4 (c) and using an approach similar to the approach used in Section 3.2.1, the ratios of the phasors of the positive-sequence and negative-sequence incremental voltages and currents as seen by different delta-impedance relays can be expressed by the equations.

$$\frac{\Delta V_{kp}}{\Delta I_{kp}} = -Z_{kp} \tag{3.11}$$

$$\frac{\Delta V_{kn}}{\Delta I_{kn}} = -Z_{kn} \tag{3.12}$$

where

Z_{kp} is the equivalent positive-sequence impedance of the circuits connected to the busbar,

Z_{kn} is the equivalent negative-sequence impedance of the circuits connected to the busbar

and k = 1, 2, ..., m, m+1, m+2, ..., j-1, j.

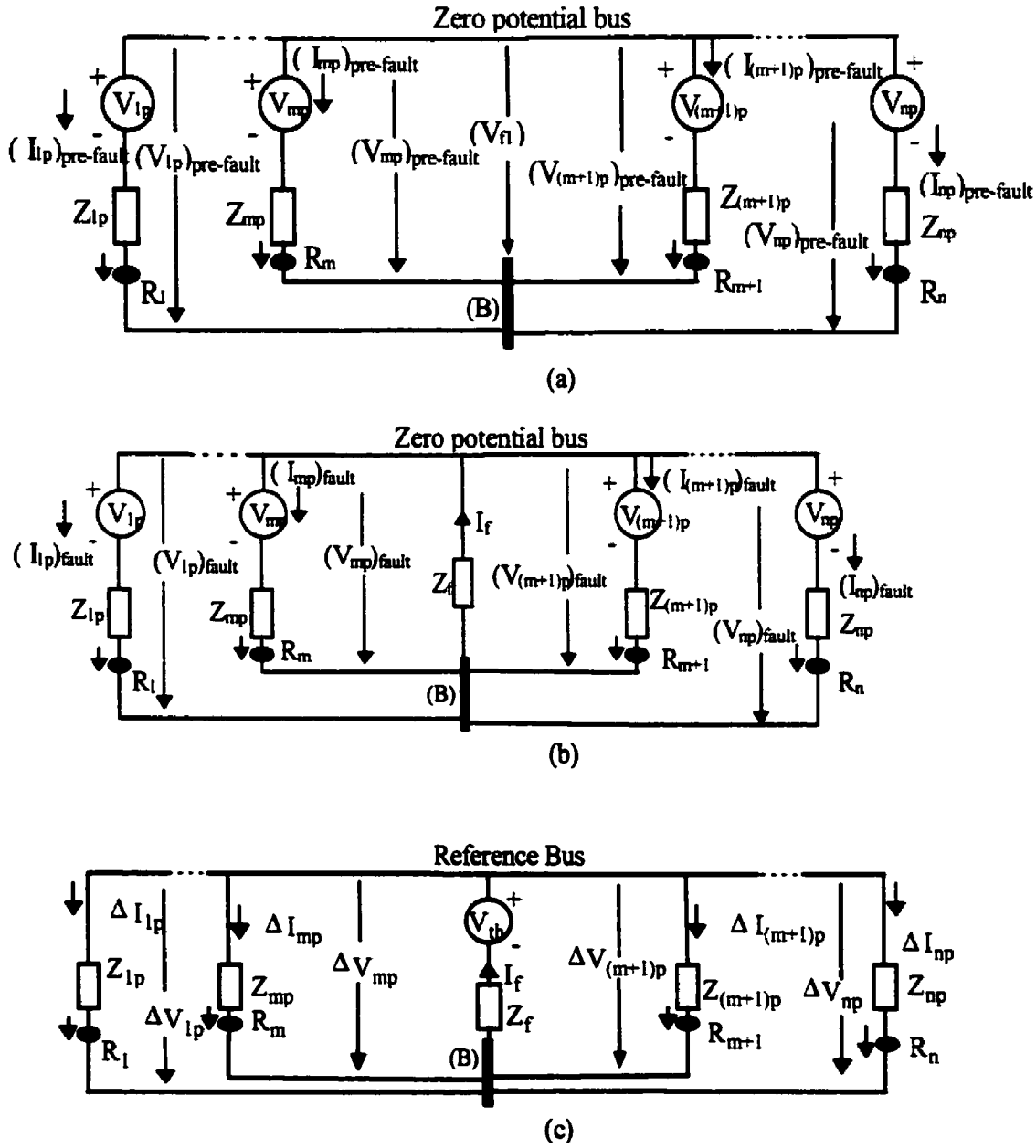


Figure 3.4. Positive-sequence (a) pre-fault, (b) during-fault, and (c) Thevenin equivalent circuits for an internal fault in the busbar (F_2).

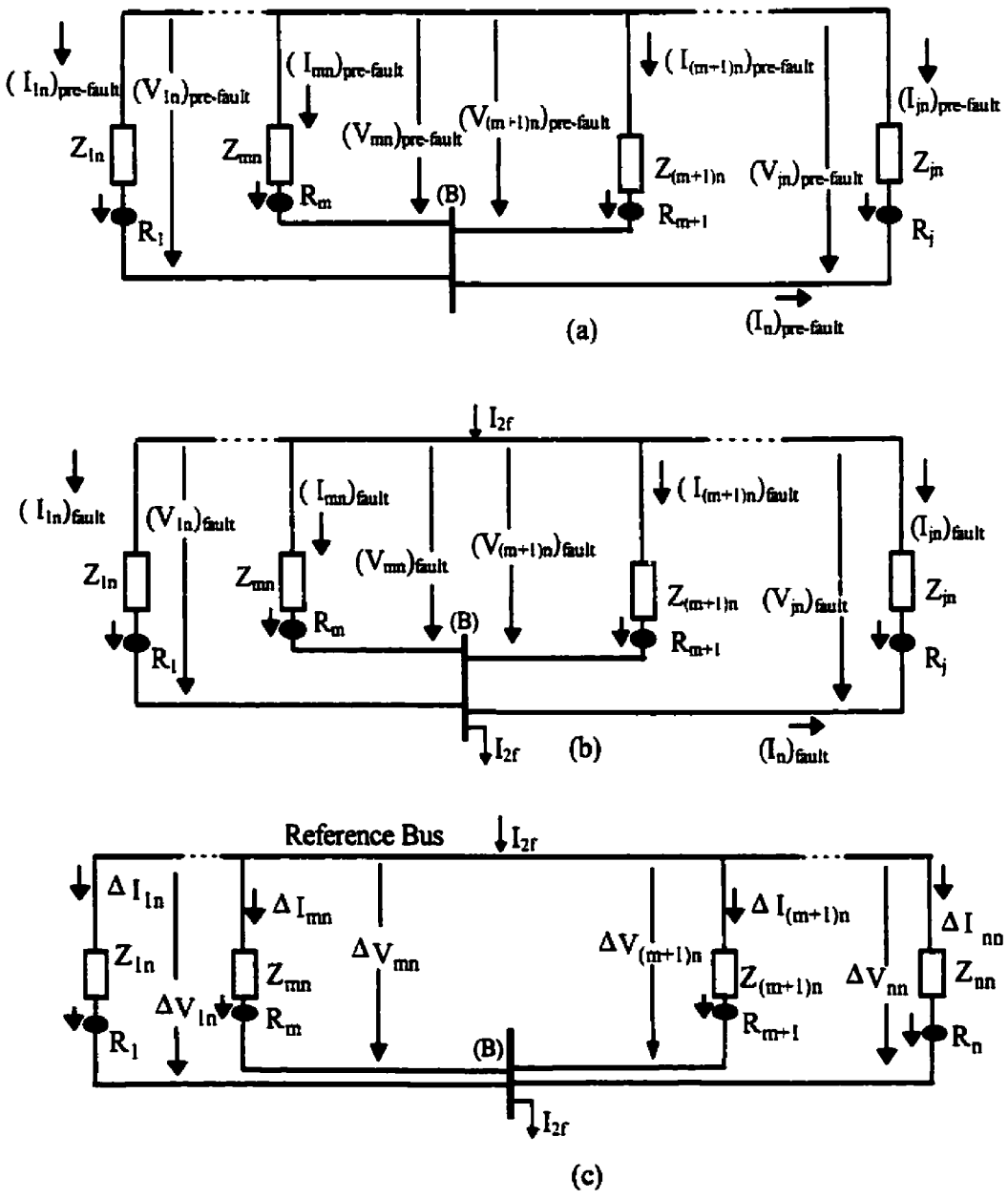


Figure 3.5. Negative-sequence (a) pre-fault, (b) during-fault, and (c) Thevenin equivalent circuits for an internal fault in the busbar (F_2).

3.2.3. Fault-detection characteristics

The presentations of Sections 3.2.1 and 3.2.2 lead to the following observations.

- The impedances seen by all the delta-impedance relays lie in the third quadrant of the impedance plane when a fault is in the protection zone of the busbar.
- The impedance seen by the relay located on the faulted circuit lies in the first quadrant when a fault is outside the protection zone of the busbar. The impedances seen by all other relays lie in the third quadrant.

These criteria are true for positive- as well as negative-sequence impedances seen by the relays and, therefore, can be used to distinguish faults outside the bus-protection zone from faults in the protection zone. The criteria can be translated into the fault detection characteristics shown in Figure 3.6.

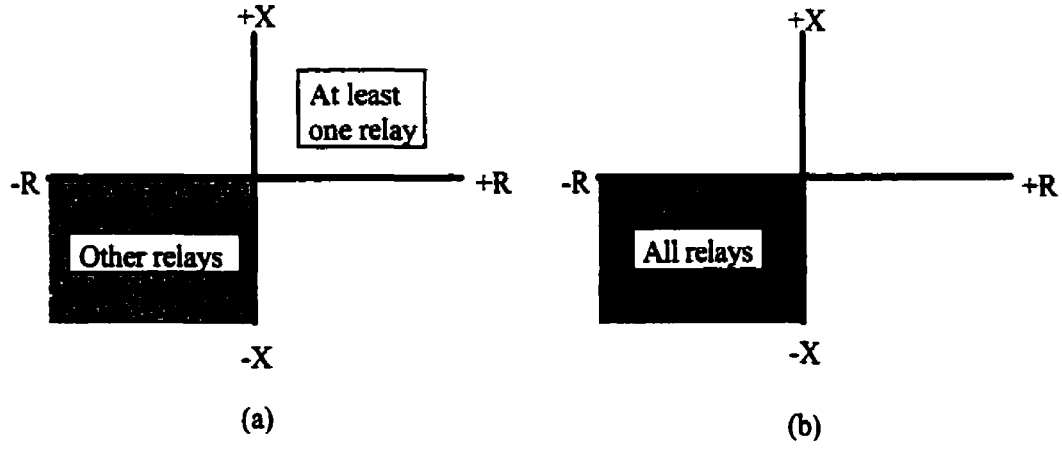


Figure 3.6. Fault-detection characterisitics for (a) an external fault and (b) an internal fault.

3.3. Protection algorithm

A digital algorithm based on the fault detection technique proposed in Section 3.2 has been developed for protecting busbars. Each delta-impedance relay used in the protection scheme executes the proposed algorithm, and the final decision is made by combining the observations made by all the relays. The algorithm uses the voltages and currents sampled simultaneously at a predefined rate. The following sections describe the procedure followed in executing the proposed algorithm.

3.3.1. Procedural steps and flow-chart

A flow chart of the proposed algorithm is displayed in Figure 3.7. The following steps are performed in the algorithm by the delta-impedance relay R_k (k=1, 2, ...j).

1. Initialize the trigger indicator, TRIGGER, and the trip counters, TPOSk and TNEGk of the positive- and negative-sequence impedances to zero.
2. Check if it is time to sample voltages and currents. If so, proceed to Step 3. Otherwise, wait until it is time to take samples.
3. Sample and quantize the phase voltages and currents.
4. Calculate the 60 Hz voltage and current phasors using the LES filters described in Appendix C.
5. Calculate the positive- and negative-sequence phasors and store the sequence-phasors in the processor's memory.
6. Compare the most recent voltage and current samples with the voltage and current samples from one cycle earlier. If the change is greater than a pre-defined threshold, V_CHANGE for voltage and I_CHANGE for current, then increase TRIGGER by one, else decrease TRIGGER by one if it is greater than zero.
7. Check if TRIGGER is equal to two. If so, proceed to Step 8, else revert to Step 2.
8. Compute the phasors of the positive- and negative-sequence incremental voltages and currents using Equations 3.1 and 3.2 respectively.

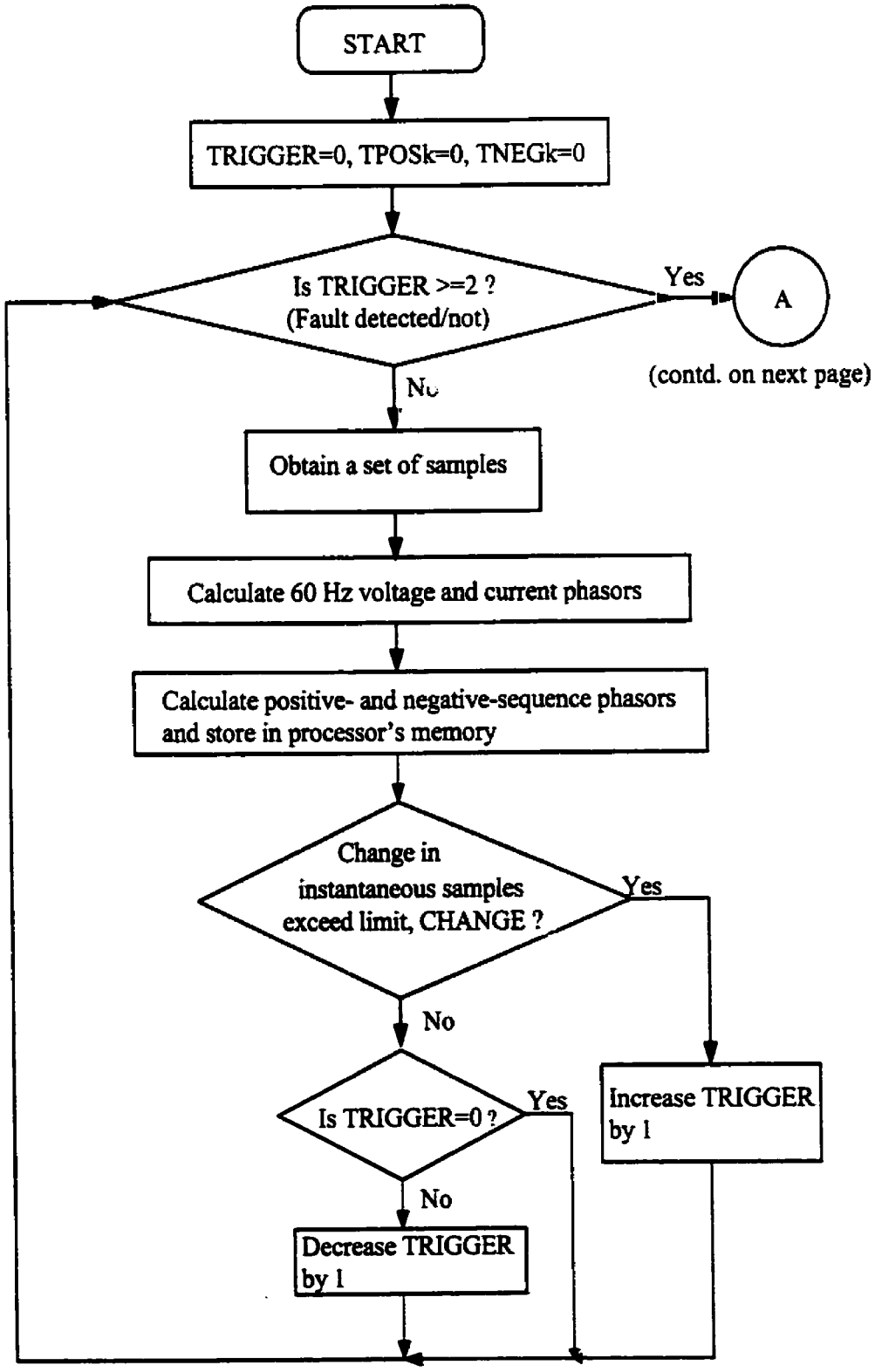


Figure 3.7. Flow chart of the proposed algorithm (pre-fault segment).

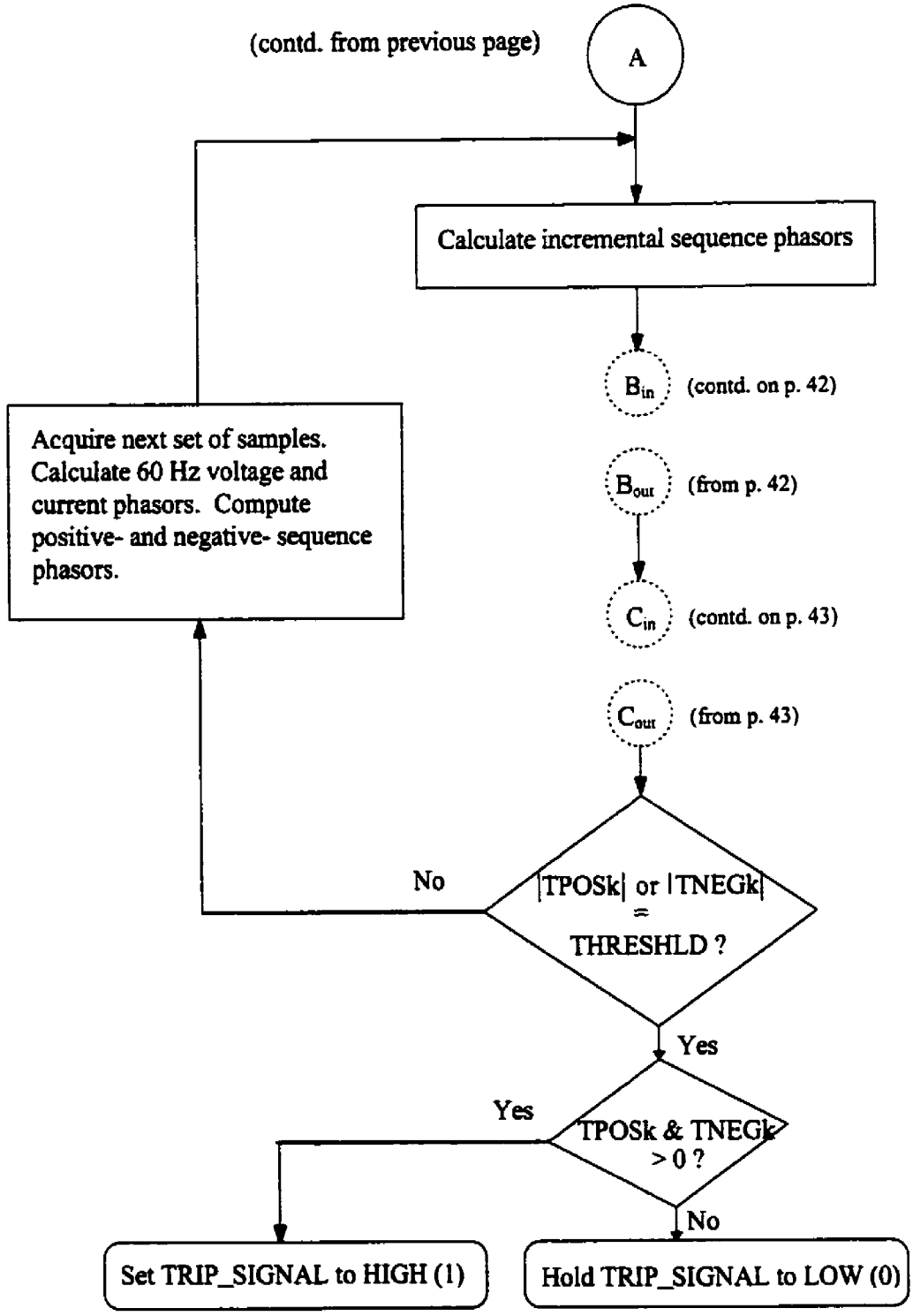


Figure 3.7 (contd.). Flow chart of the proposed algorithm (during-fault segment).

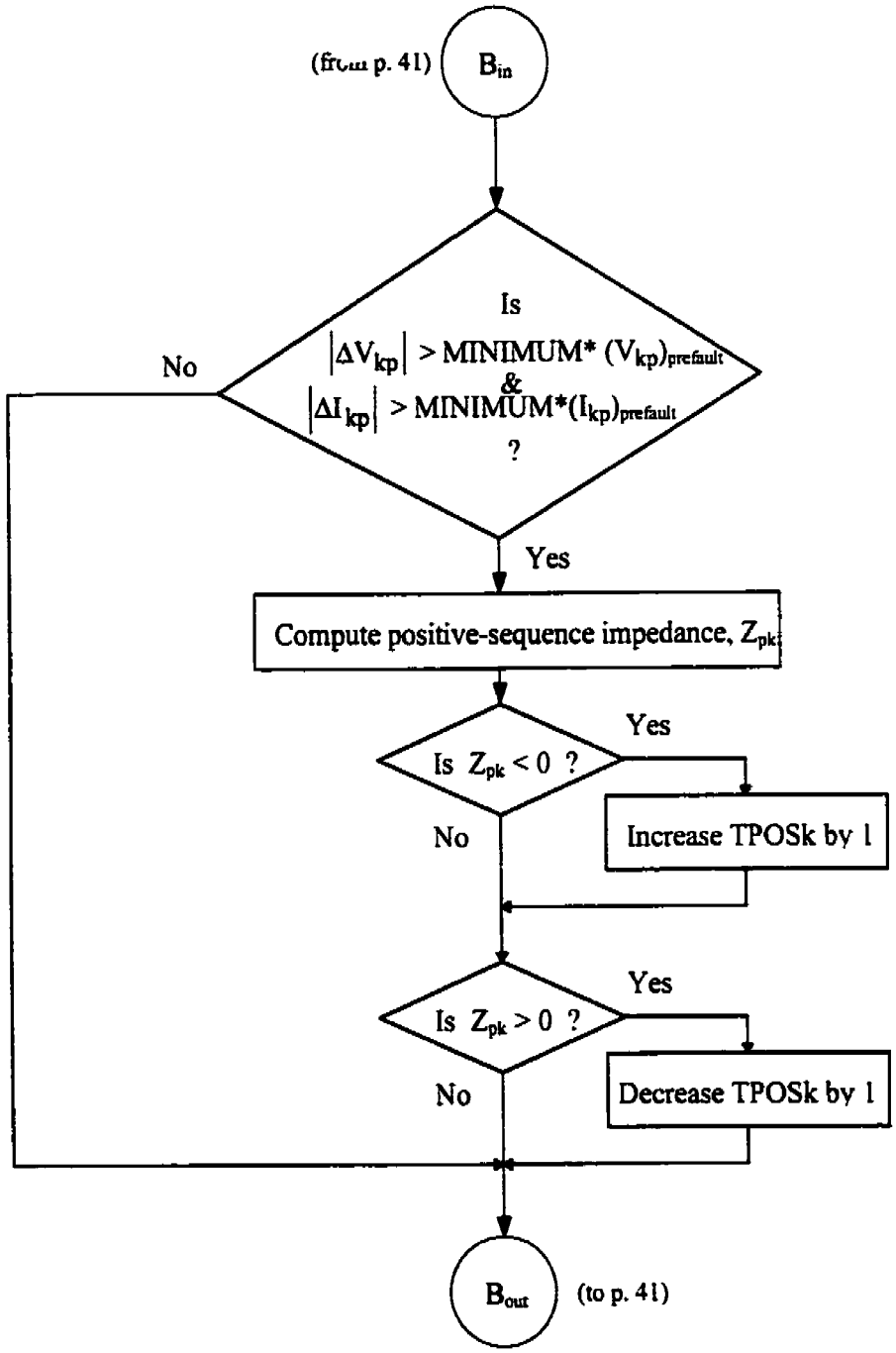


Figure 3.7 (contd). Segment for checking threshold of positive-sequence voltages and currents.

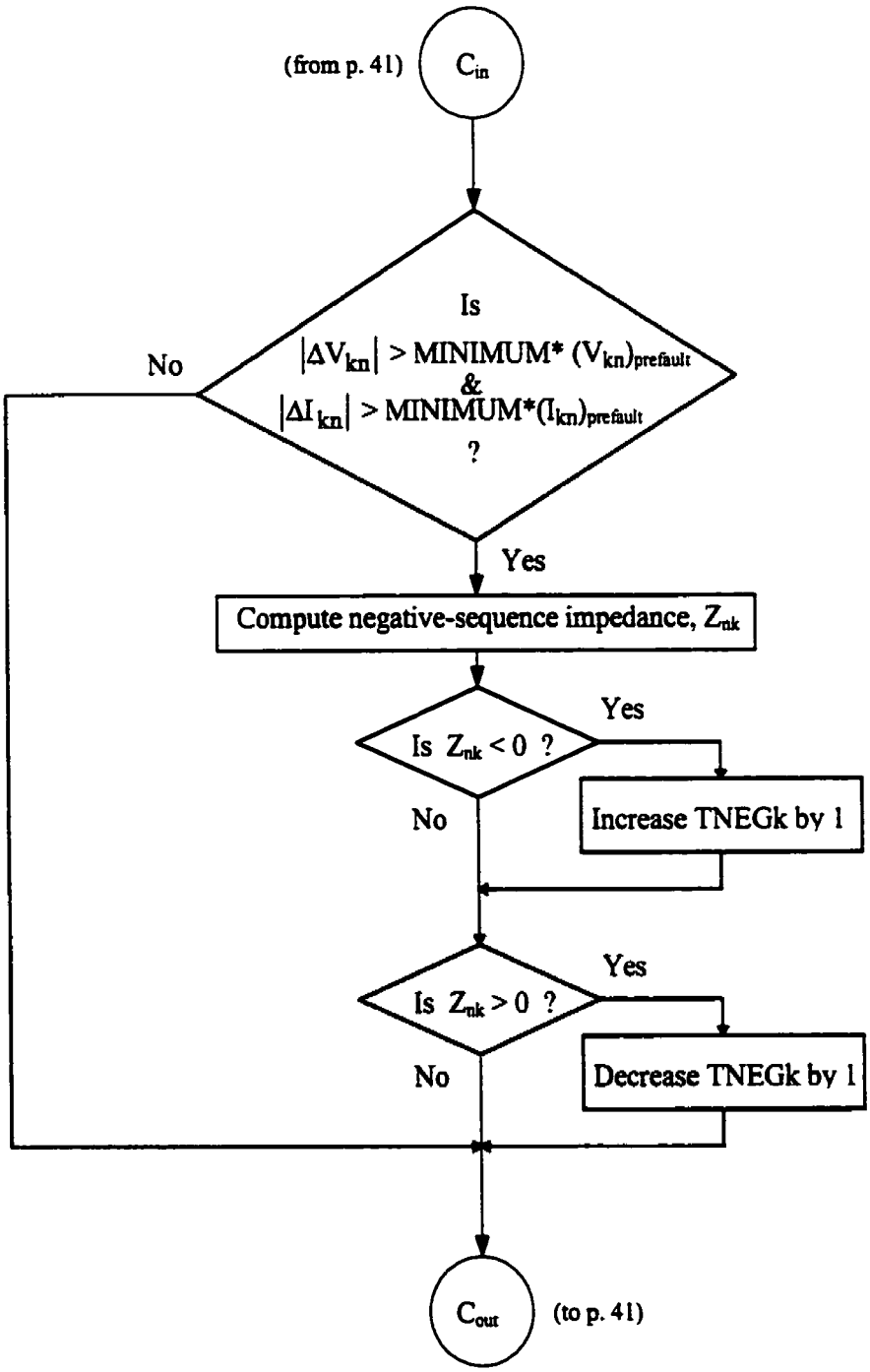


Figure 3.7 (contd). Segment for checking threshold of negative-sequence voltages and currents.

9. Check if the magnitudes of the phasors of the positive-sequence incremental-voltages and incremental-currents are greater than a predefined minimum value, MINIMUM, times the corresponding pre-fault values that were calculated in Step 5. If they are, compute the ratio of the phasors of the positive-sequence incremental voltage and current (Z_{pk}) seen by the relay, otherwise, proceed to Step 11.

10. Check if the positive-sequence impedance is in the third quadrant. If it is, increase the positive-sequence trip counter, TPOSk, by one. Decrease the trip counter by one if the impedance lies in the first quadrant.

11. Check if the magnitudes of the phasors of the negative-sequence incremental-voltages and incremental-currents are greater than a predefined minimum value, MINIMUM, times the corresponding pre-fault values that were calculated in Step 5. If they are, compute the ratio of the phasors of the negative-sequence incremental voltage and current (Z_{kn}) seen by the relay, otherwise proceed to Step 13.

12. Check if the negative-sequence impedance is in the third quadrant. If it is, increase the negative-sequence trip counter, TNEGk, by one. Decrease the trip counter by one if the impedance lies in the first quadrant.

13. Check if the value of either the positive-sequence trip counter or the negative-sequence trip counter has violated a pre-specified value, THRESHLD. If either counter has, proceed to Step 14, otherwise revert to Step 2.

14. Set trip signal (TRIP_SIGNALk) to HIGH (1) (LOW (0)) for positive (negative) values of trip counters.

15. Revert to Step 2.

The algorithm steps outlined above will be continuously executed by the relay until a trip signal is sent to the trip-logic for a fault in the protection zone of the busbar. However, for a fault outside the busbar protection zone, the relay continuously computes the impedances as long as the circuit breaker on the faulted circuit is opened and a signal to this effect is received by the relay.

3.3.2. Computations

The digital algorithm executes the steps outlined in Section 3.3.1. Various computations performed by the relays are briefly described in this section.

3.3.2.1. Voltage and current phasors and sequence quantities

The coefficients of orthogonal filters, which are designed off-line, are used for computing phasors. A Least Error Squares filter [47] designed for a data window of 25 samples taken at 1440 Hz was used in this work. At each sampling instant, voltage and current samples are obtained from each phase of the power system, are quantized, and are used for computing phasors. The computed voltage and current phasors are used for calculating the sequence-voltage and sequence-current phasors. The latest set of phasors and sequence-phasors are stored in a buffer. The data window is advanced to receive new samples. Appendix C describes the Least Error Squares filter used for estimating phasors.

3.3.2.2. Fault-inception

The voltage and current samples from each phase are used for detecting the inception of a fault. The most recent sample is compared with the corresponding sample taken one period earlier and the change in its value is calculated. If the change is greater than a pre-defined threshold, I_CHANGE for current and V_CHANGE for voltage, the associated trigger counter is incremented. Two successive increments of a counter establish the onset of a fault. Once the fault-inception is detected, the procedure for computing incremental-sequence phasors is initiated.

3.3.2.3. Phasors of incremental voltages and currents, and apparent impedances

As described before, phasors of sequence voltages and currents are computed using a data window of fixed length every time the samples are taken. The data window moves continuously such that a new sample is included at every sampling instant and the oldest sample is discarded. The movement of data window is illustrated in Figure 3.8.

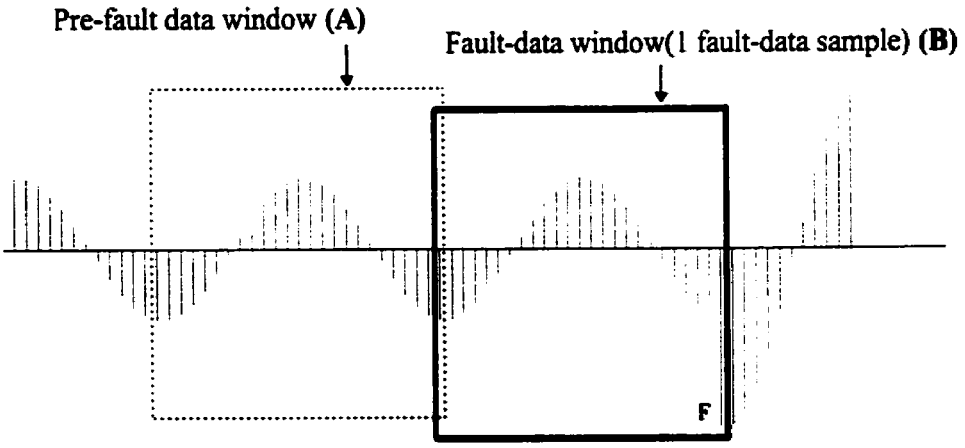


Figure 3.8. Data window for computing phasors.

The phasors of sequence voltages and currents calculated using twenty five consecutive windows are saved in memory. The phasors calculated after the occurrence of a fault (instant F in Figure 3.8) are used in conjunction with the corresponding pre-fault sequence phasors to compute the incremental sequence-phasors. For example, the phasors calculated using samples of data window B of Figure 3.8 are used along with the values of the sequence-phasors calculated using the pre-fault data window A. When the next sample is acquired, the fault data window is advanced by one sample from window B and the pre-fault phasor calculated by using the data window advanced by one sample from window A is used.

The incremental voltage and current phasors are used for calculating the sequence impedances seen by the relays. The arguments of the impedances are used in conjunction with the fault-detection characteristics of Figure 3.6 for detecting fault in the busbar zone.

3.3.2.4. Trip-counters

The arguments of impedances are noted for their sign. As discussed in Section 3.2.3, this sign forms the basis of determining if a fault is either inside or outside the protection zone of the busbar. To ensure secure decisions, two trip-counters based on

positive- and negative-sequence impedances are formed for each relay. These are incremented/decremented for a negative/positive value of the argument of the impedance. A decision is made by a relay when the absolute value of either of the two trip-counters reaches the pre-specified limit, THRESHLD. As soon as the trip-counter reaches the threshold, a TRIP_SIGNAL representing the decision of the delta-impedance relay is set. It is set HIGH (1), if the trip counter is positive and it is set LOW (0) if the trip counter is negative. The decision is passed on to the trip-logic.

3.3.2.5. Trip-logic

The trip-logic combines the decisions made by all the delta-impedance relays by using an AND gate logic circuit and provides the final decision. Figure 3.9 shows the trip-logic for the busbar protection system of Figure 3.1. In this figure, TRIP_SIGNALk, k=1, 2, ..., m, m+1, m+2,....., j, represent the decisions from the individual delta-impedance relays that are sent to the trip logic using appropriate communication system.

The output from the trip logic is used to trip the circuit breaker when a fault is in the busbar protection zone. However, if any of the input signals is LOW (0), the tripping of the circuit breaker is blocked.

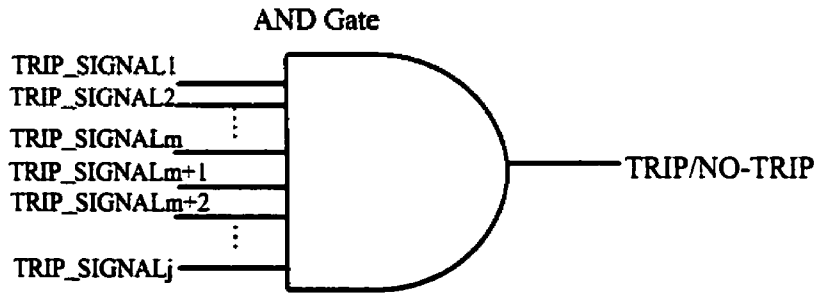


Figure 3.9. Trip logic.

3.4. Summary

A technique for protecting busbars has been presented in this chapter. The technique uses samples of the three-phase voltages and currents of the circuits connected to the busbar. The samples are used to compute positive- and negative-sequence voltage and current phasors which, in turn, are used to identify faults in the busbar protection

zone using the proposed technique. It is observed that the technique does not use the parameters of the power system components. Only the arguments of the impedances computed by the delta-impedance relays are used to identify the fault.

A digital algorithm based on the developed technique has been explained as well. The delta-impedance relays involved in the protection scheme would execute the algorithm. The details of the computations performed by the algorithm execution have also been presented.

4. IMPACT OF CT SATURATION AND CT RATIO-MISMATCH

4.1. Introduction

Relays make decisions while dc transient component are present in voltages and currents. To ensure that a relay makes decisions correctly, the waveforms of currents received from cts should not be distorted. Emphasis is, therefore, placed on the ability of cts to provide to protective relays current waveforms that are true representation of the primary currents.

This chapter examines in detail the impact of ct saturation and ct ratio-mismatch on the phasors computed by digital algorithms. Different levels of ct saturation, and different parameters used for phasor computations, such as sampling frequency and data-window alignment, are considered. The impact of ct saturation and ct ratio-mismatch conditions on the performance of the technique, proposed in Chapter 3, is also examined. The objective is to establish the reasons for stable performance of the proposed technique when cts saturate and (or) their ratios do not match.

4.2. CT saturation - Impact on phasor calculations

Current transformers are used to reduce the levels of currents experienced in power systems so that the currents may be conveniently applied to relays. Waveforms of currents generally provided by cts faithfully represent the primary currents until the ct core saturates. The saturation causes the waveform of the secondary current to distort. The extent of distortion depends on the magnitude of the remnant flux in the ct core, the presence of dc offset in the primary current and the ct burden. A saturated ct gradually recovers and the waveform of its secondary current starts to faithfully represent the primary current. An investigation of the transient performance of cts reveals that the waveforms provided by saturated cts have typical profiles shown in Figure 4.1.

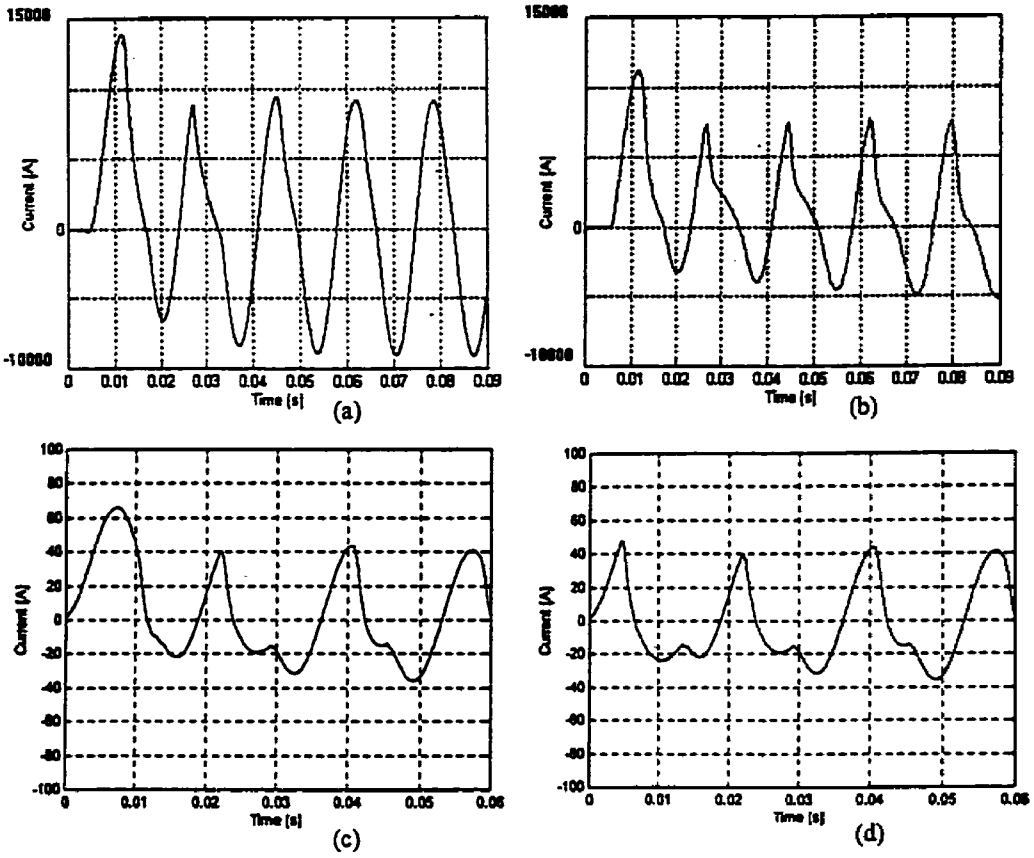


Figure 4.1. Typical waveforms of currents provided by saturated cts [33].

This figure shows that a ct does not saturate immediately after the occurrence of a fault. Also, ct saturation results in clipping a part of the waveform after a zero crossing. More severe the saturation is, more of the waveform is clipped.

The proposed technique uses the fundamental frequency phasors that are computed from quantized values of the waveform-samples. The impact of ct saturation on the computed values of the phasors was, therefore, studied. Important conclusions drawn from the study and an explanation of the effect of ct saturation on the performance of the proposed technique is provided in the following sections.

4.2.1. Procedure

The objective of analysis was to investigate the underlying phenomenon that affects the impedances calculated after cts saturate. The impact of ct saturation on the magnitudes and arguments of the computed phasors of the fundamental frequency was

studied. Discrete Fourier analysis technique was used for computing the phasors from quantized samples of the waveforms provided by unsaturated and saturated cts. The waveforms of the primary currents were considered to be sinusoids of the fundamental frequency with decaying dc offset. The outputs of saturated cts used in these studies resemble one of the waveforms shown in Figure 4.1. Different alignments of the data window and the current waveform were used. Selected results obtained from the analysis are presented in the next section. The effects of various factors on the results are also identified.

4.2.2. Results

The results obtained from the tests, when a sampling frequency of 480 Hz was used, are shown in Figure 4.2. This figure shows the simulated waveforms of currents provided by unsaturated and saturated cts. The magnitudes and arguments of the phasors, computed for two alignments of the data window, are shown as well.

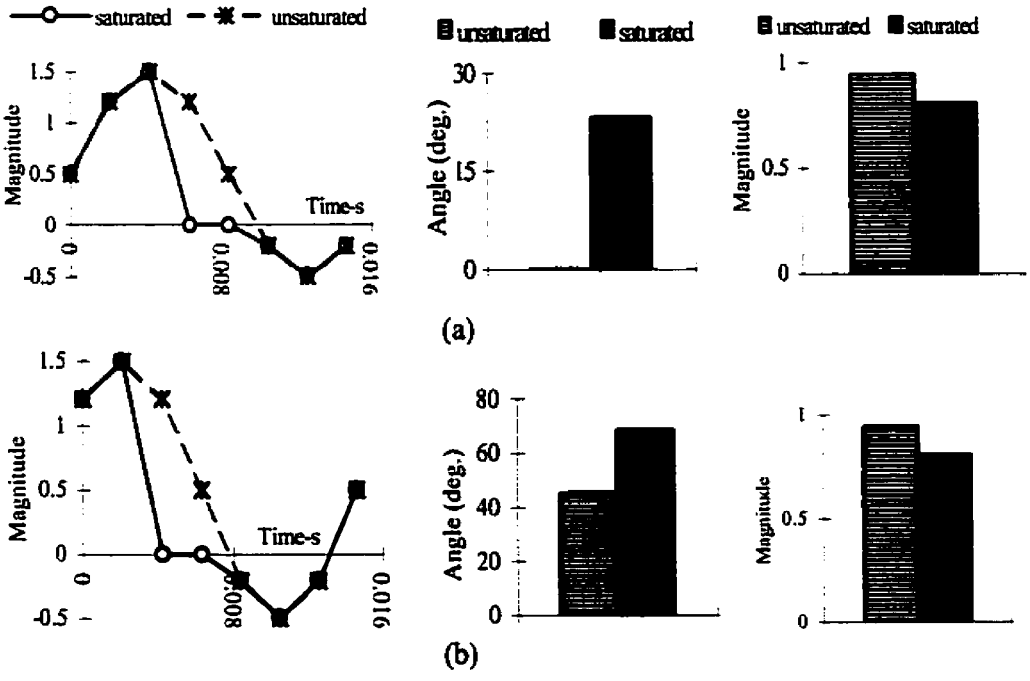


Figure 4.2. Waveforms of currents from unsaturated and saturated cts, and phasors calculated from the waveforms when two distinctly different alignments of the data window are used.

The waveform has about 50% dc offset. Moreover, a substantial part of the waveform representing output of the saturated ct is clipped. Additional studies revealed that the impact of saturation, on the magnitudes and arguments of phasors, was similar for other alignments of the data-window. A perusal of Figure 4.2 leads to the following conclusions.

- The magnitudes of the phasors computed from the outputs of saturated cts are always smaller than the magnitudes of the phasors computed from the outputs of not-saturated cts.
- The arguments of the phasors computed from the outputs of saturated cts are greater than the arguments computed from the outputs of unsaturated cts.

These observations were found true for all alignments of the data-window.

4.2.2.1. Effect of data-window movement

The data-window used for computing phasors from currents moves by one sample at a time. At each sampling instant, a new sample is included in the data-window and the oldest sample is discarded. Figure 4.3 shows the magnitudes and arguments of the computed phasors of currents provided by unsaturated and saturated cts for different alignments of the data-window. The profile of current waveforms from unsaturated and saturated cts are also shown in this figure. A sampling frequency of 480 Hz was used in this analysis.

A perusal of Figures 4.3 (a) to (h) reveals that the arguments of phasors calculated from the outputs of saturated cts are always greater than the corresponding arguments of phasors computed from the outputs of not-saturated cts. Also, the magnitudes of the phasors computed from waveforms provided by saturated cts are always smaller than the magnitudes of phasors calculated from waveforms of currents provided by not-saturated cts. These conclusions remain valid as the data window is advanced one sample at a time for the duration of one cycle.

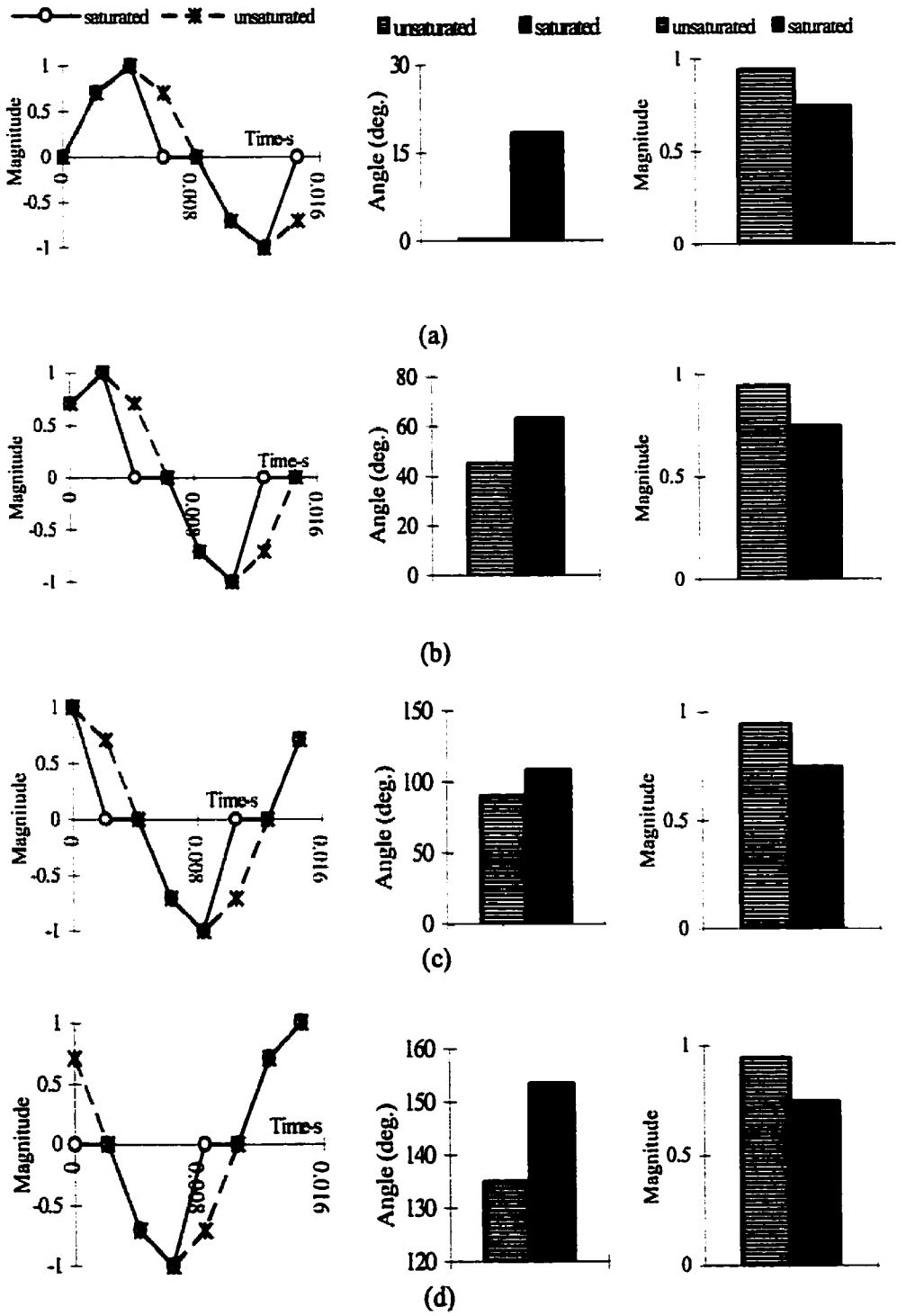


Figure 4.3. Waveforms of currents from unsaturated and saturated cts, and phasor arguments and magnitudes computed when the data window starts at (a) 0^0, (b) 45^0, (c) 90^0, and (d) 135^0.

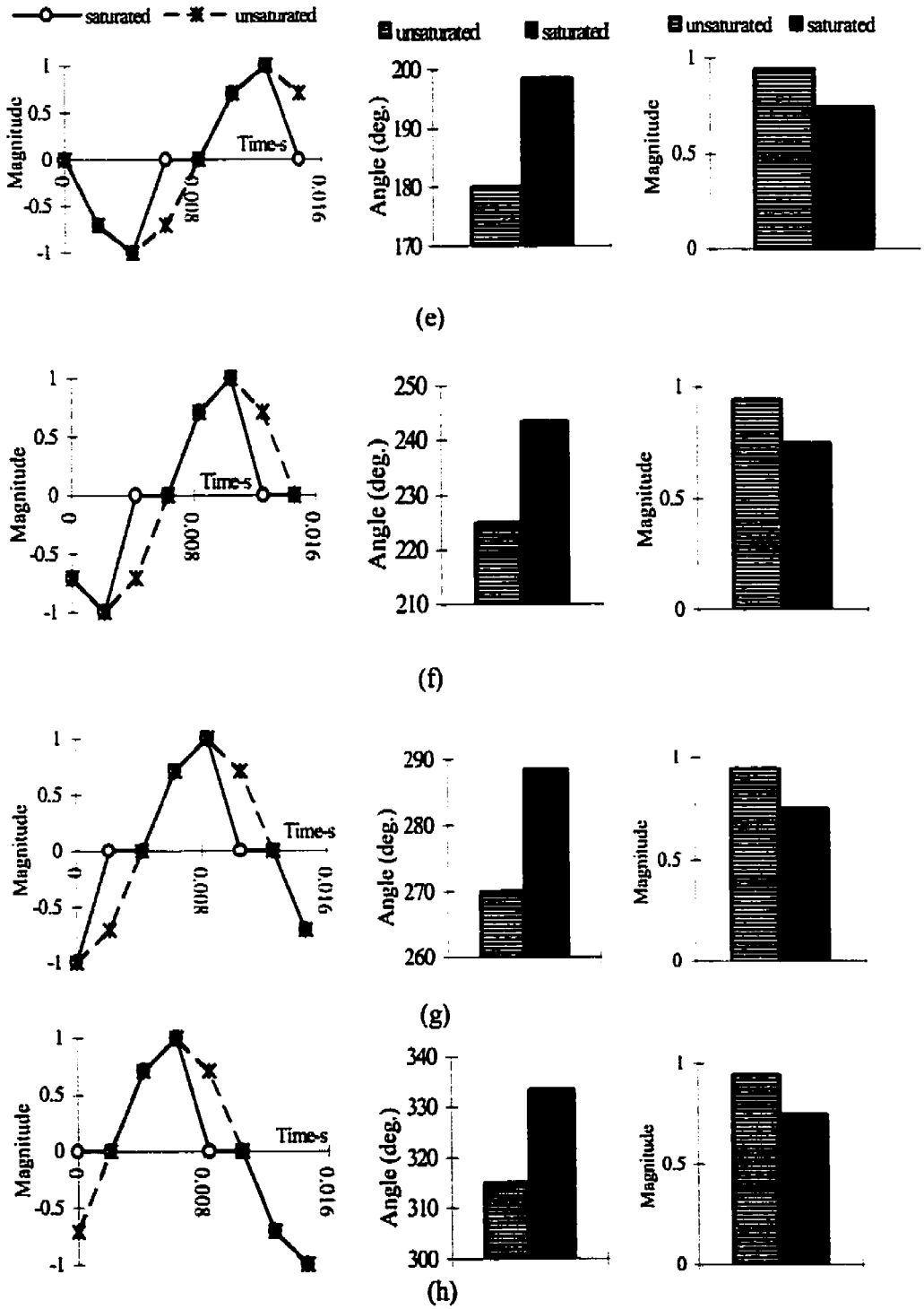


Figure 4.3 (contd.). Waveforms of currents from unsaturated and saturated cts, and phasor arguments and magnitudes computed when the data window starts at (e) 180^0, (f) 225^0, (g) 270^0, and (h) 315^0.

4.2.2.2. Effect of sampling frequency

Analysis reported in the previous section was repeated with different sampling frequencies. The phasors were calculated by using the Fourier analysis technique and sampling frequencies of 480 Hz, 720 Hz, 960 Hz and 1440 Hz were used. Table 4.1 gives an overview of the calculated arguments and magnitudes of the fundamental frequency phasors computed from the waveforms provided by an unsaturated ct and a saturated ct.

Table 4.1. The magnitudes and arguments of phasors calculated from the waveforms provided by an unsaturated ct and a saturated ct.

Sampling Freq. (Hz)	Unsaturated ct		Saturated ct		Difference
	Mag.	Arg. θ_u (deg)	Mag.	Arg. θ_s (deg.)	$\theta_s - \theta_u$ (deg.)
480	1.0	90.0	0.791	108.4	18.43
720	1.0	90.0	0.727	113.4	23.41
960	1.0	90.0	0.694	115.8	25.78
1440	1.0	90.0	0.661	118.1	28.07

A study of the results presented in the table reveals that the conclusions drawn in Section 4.2.2 are valid when other plausible sampling frequencies are used. The difference in arguments calculated from waveforms provided by unsaturated and saturated cts remains constant for a given sampling frequency and does not change with the alignment of the data-window.

4.2.2.3. Effect of the severity of ct saturation

Fourier analysis of waveforms provided by cts with different levels of saturation was carried out to investigate the impact of saturation on the trend observed in Sections 4.2.2.1 and 4.2.2.2. The results from an analysis, when a sampling frequency of 720 Hz was used, is illustrated in Figure 4.4. The arguments and magnitudes of computed phasors of the fundamental frequency are shown in the figure. The waveforms of the currents provided by unsaturated and saturated cts are also shown. This figure shows that, as expected, the waveform of the current become more distorted as the severity of ct

saturation increases. Increased distortion causes the magnitudes of the phasors to decrease to smaller values. The computed arguments of the phasors increase to larger values with increased saturation. Similar results were observed when other sampling frequencies and other data-window alignments were used.

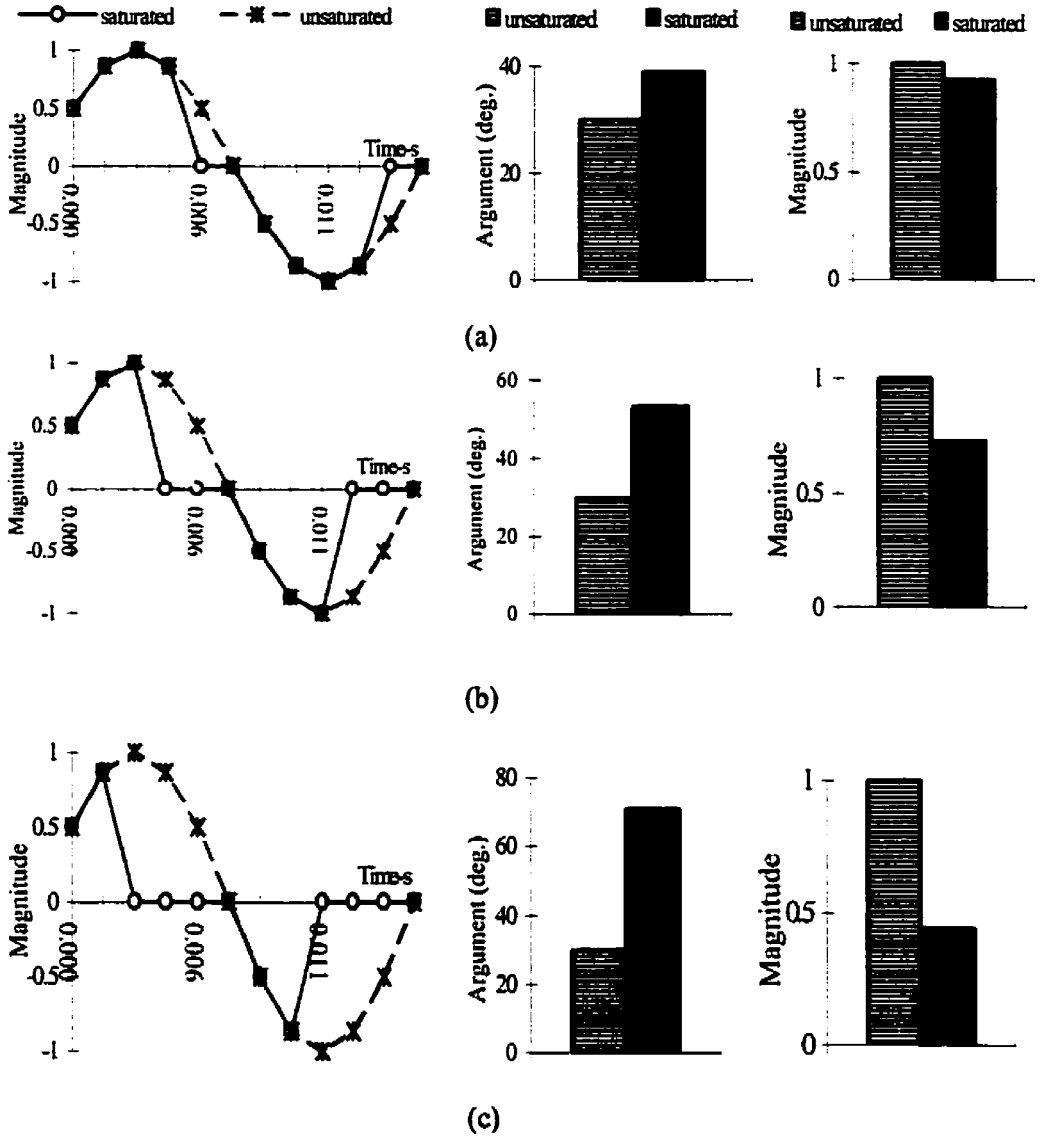


Figure 4.4. Waveforms of currents from unsaturated and, mildly, moderately and severely saturated cts, and phasor arguments and magnitudes calculated from the data representing the waveforms.

4.2.2.4. Effect of the data-window size

Data windows of different sizes are used by different algorithms for extracting the fundamental frequency component from a given signal. The effect of data-window size on the arguments and magnitudes of the computed fundamental frequency phasors was investigated. Figure 4.5 shows a typical result in which data-windows of 13 and 17 samples and the Least Error Squares algorithm were used. The sampling frequency of 720 Hz was used in these cases. This figure shows that the arguments of the fundamental frequency phasors of a saturated waveform are greater than the arguments if the waveform was provided by a ct that was not saturated. On the other hand, the magnitudes of the fundamental frequency phasors of a saturated waveform are smaller than the magnitudes if the waveform was provided by a ct that was not saturated. Investigations showed that these trends are also true when other sampling frequencies and other data-window alignments were used.

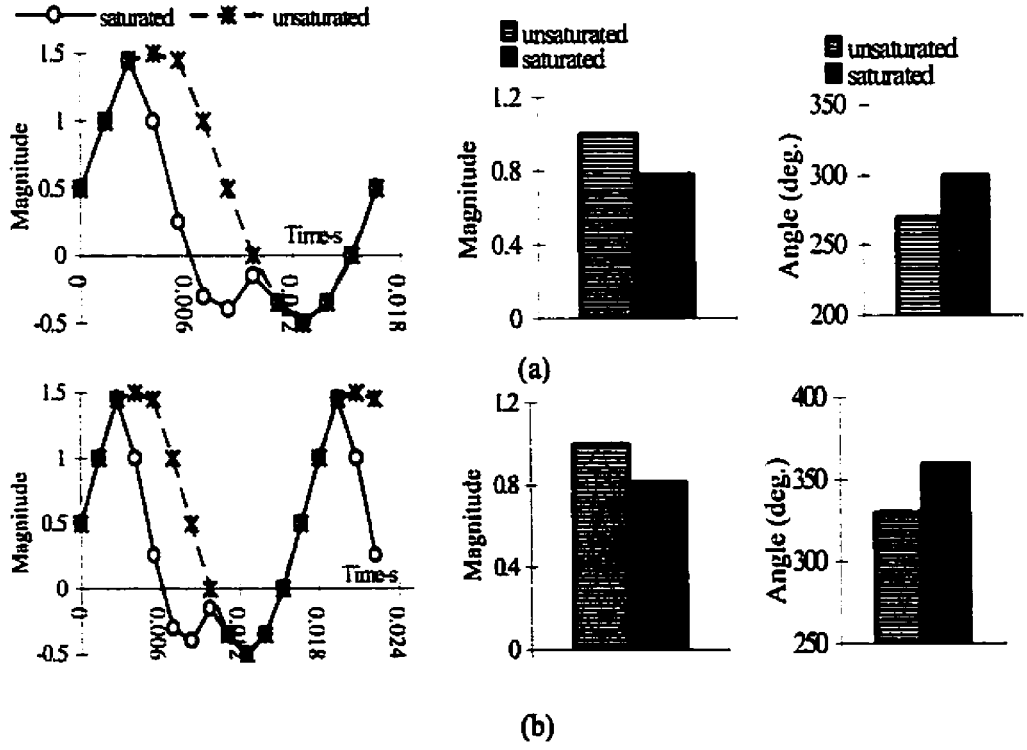


Figure 4.5. Waveshapes of currents from unsaturated and saturated cts, and phasors calculated by using data windows of (a) 13 samples and (b) 17 samples.

4.2.2.5. Effect of the cut-off frequency of anti-aliasing filter

An anti-aliasing filter is used to process signals before they are processed by the relaying software. This is done to prevent aliasing of signals. Cut-off frequency of the anti-aliasing filter is selected using the Nyquist criterion [48]. The analysis of Sections 4.2.2.1 to 4.2.2.4 was carried out without using anti-aliasing filters. The impact of the cut-off frequency of the filter on computed phasors is examined in this section.

Anti-aliasing filters of different cut-off frequencies were used to investigate their effect on the arguments and magnitudes of the computed fundamental-frequency phasors. Outputs of unsaturated and saturated cts were used as inputs to the filters. Cut-off frequency of the filter was set at different values for a given sampling frequency. The outputs of the filters were used to estimate the magnitudes and arguments of the fundamental frequency phasors for different data-window alignments. Table 4.2 lists the arguments of the fundamental frequency phasors when a particular alignment of the data-window at a sampling frequency of 720 Hz was used. Similar trends were observed from the results when other alignments of the data-window and other sampling frequencies were used. It is interesting to note that the differences between the arguments calculated from waveforms provided by not-saturated and saturated cts are approximately the same for all cut-off frequencies of the anti-aliasing filter.

Table 4.2. Impact of the cut-off frequency of the filter on the phasor arguments computed from waveforms provided by unsaturated and saturated cts.

Cut-off frequency	Phasor argument (deg.)		Difference (deg.)
(Hz)	unsaturated (θ)	saturated (θ')	(θ'-θ)
100	-31.07	-11.18	19.89
200	-33.53	-11.35	22.18
300	-39.61	-17.19	22.43
360	-30.00	-6.59	23.41
without filter	-30.00	-6.59	23.41

4.2.3. Discussion

As discussed in the previous section, the waveforms from saturated cts are distorted unlike those from not-saturated cts. The profile of the waveforms from saturated cts have typical form like those shown in Figure 4.1. The analyses and discussions, contained in Sections 4.2.1 and 4.2.2, describe the impact of ct saturation on the computed phasors. The presentations in these sections lead to the following conclusions.

1. The waveform of the output of a saturated ct has a typical profile in which a part of the cycle is distorted. Each cycle starts with the waveform that is similar to the waveform provided by a not-saturated ct. The waveform is subsequently distorted and the extent of distortion depends on the severity of saturation. The decaying dc component of the primary current is one of the major causes for causing cts to saturate.

2. The magnitudes of the fundamental-frequency phasors computed from data representing a waveform provided by a saturated ct is always smaller than the magnitudes that would have been calculated if the waveform was not distorted.

3. The arguments of the fundamental-frequency phasors computed from data representing a waveform provided by a saturated ct is always greater than the arguments that would have been calculated if the waveform was not distorted.

4. The difference in the relative magnitudes and arguments increase with increased severity of saturation. The difference, however, remains practically constant for a saturation level.

5. The relation between the arguments and magnitudes of the fundamental-frequency phasors computed from waveforms provided by not-saturated and saturated cts remain constant even when data-windows of different lengths (non-Fourier type filters) are used.

6. The cut-off frequency of the anti-aliasing filter has negligible effect on the differences between the arguments of phasors computed from the outputs of not-saturated and saturated cts.

The observations 2 and 3 are true for all alignments of the data-window and for different sampling frequencies. These observations hold good for the fundamental

frequency component and, therefore, are valid irrespective of the type of filter used for extracting the component.

4.3. Impact of CT conditions on the proposed technique

The effect of ct saturation and the ct ratio-mismatch on the conventional differential protection systems has always been a matter of concern. It is shown in this section that the proposed busbar protection system has inherent stability during ct saturation and ct ratio-mismatch conditions.

4.3.1. Effect of CT saturation

Figure 4.6 shows the impedances calculated by a relay, used for protecting a busbar (Figure 3.1), during an internal fault and an external fault if cts saturate or do not saturate. In the case of an external fault, the relay is assumed to be located on the faulted circuit connected to the busbar. As expected, the computed impedances are larger in magnitude if the ct is saturated because the magnitudes of the computed phasors of the currents are smaller. Because the argument of the current phasors becomes larger when a ct saturates, the argument of the calculated impedance becomes smaller. This is evident in Figures 4.6 (a) and (b).

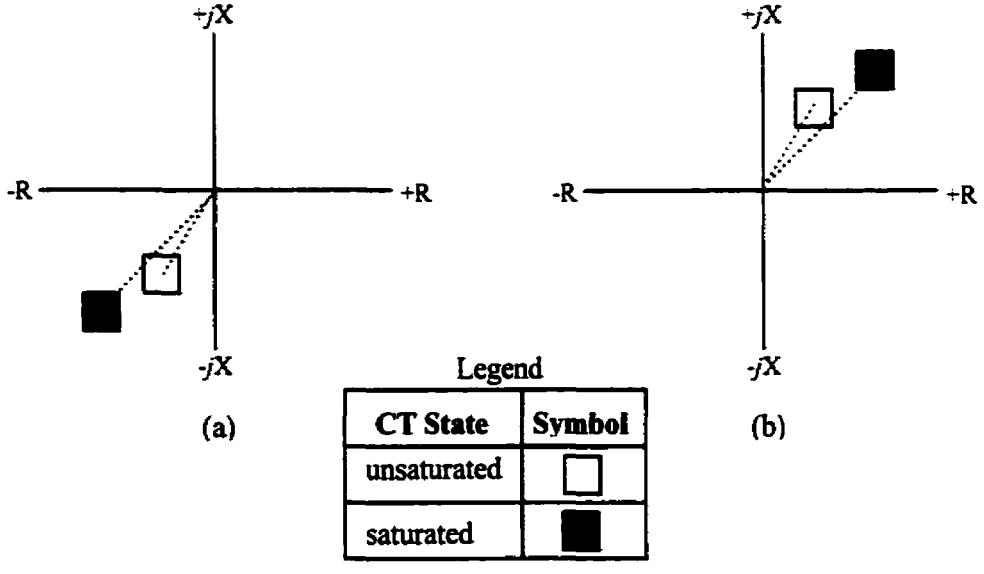


Figure 4.6. Effect of ct saturation on the impedance seen by the relay for (a) an internal fault and (b) an external fault.

This figure shows that the magnitude and argument of the computed impedances change but the trip-criteria continues to indicate the fault type (internal or external) correctly. Because the proposed technique calculates impedances that must be in the first or third quadrant, there is a wide range in which their calculated values can lie. This argument and extensive testing leads to the conclusion that the proposed technique performs correctly during ct saturation including severely saturated ct conditions.

4.3.2. Effect of CT ratio-mismatch

The proposed technique calculates the impedances using the voltage and current samples taken at the busbar end of the connected circuits. The changes in ct ratio from nominal value increases or decreases the magnitude of the current-phasor but does not change its argument as illustrated in Figure 4.7. If the ct ratio is less than nominal value, the magnitude of the current-phasor increases but the argument remains the same. As a result, the calculated magnitudes of the impedances decrease but the calculated arguments remain the same. On the other hand, if the ct ratio is more than nominal value, the magnitude of the current-phasor decreases but the argument remains the same. As a result, the calculated magnitudes of the impedances increase but the calculated arguments remain the same. The impedances, therefore, remain in the appropriate quadrant even if the ct ratio is not equal to nominal value. The effect of ct ratio-mismatch on the performance of a relay during internal and external faults is shown in Figure 4.8. These trends were observed in all the cases in which the ct ratios did not match.

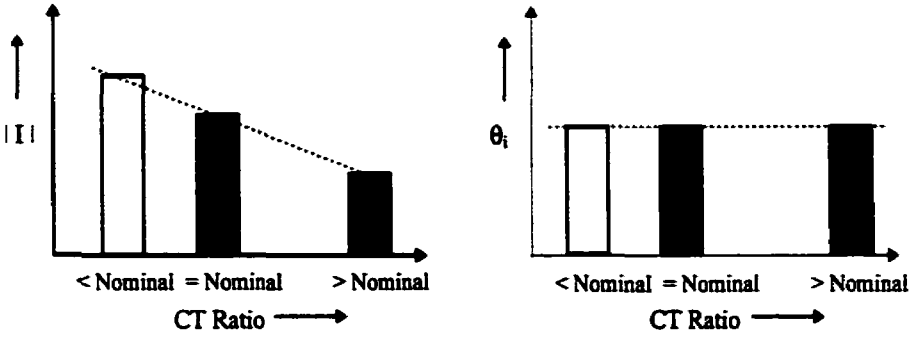


Figure 4.7 . Change of the computed magnitude and argument of the current phasor as the ct ratio changes.

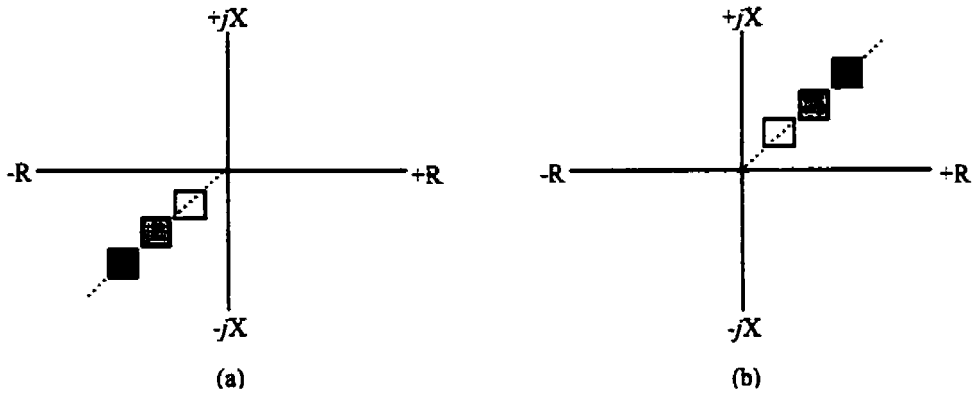


Figure 4.8. Drifts in the computed impedance due to errors in ct ratios for (a) an internal fault and (b) an external fault.

Because each relay computes the impedance independently, the ct ratio-mismatch at a relay location does not affect the performance of the technique. This is different from the conventional differential relays whose performance is adversely affected by mismatches in the ratios of various cts.

4.4. Summary

The phenomenon of ct saturation affects protection schemes adversely. A detailed analysis of the impact of ct saturation has been carried out and the results from the analyses have been presented. The effects of sampling frequency, movement of data-window and severity of ct saturation on the computations of arguments and magnitudes of the fundamental-frequency phasors have been demonstrated.

The studies have shown that the saturated cts produce current-waveforms of typical profiles. Fourier analysis of the waveforms reveals that the magnitude of the estimated fundamental-frequency phasor for a waveform of current provided by a saturated ct is smaller than the magnitude computed for a waveform provided by a not-saturated ct. Also, the arguments of the computed phasors are always greater if the ct saturates compared to the arguments if the ct does not saturate. These observations have been used to determine the effect of ct saturation on the performance of the proposed technique. The reasons for stable performance during ct saturation have, thus, been established.

5. PERFORMANCE EVALUATION

5.1. Introduction

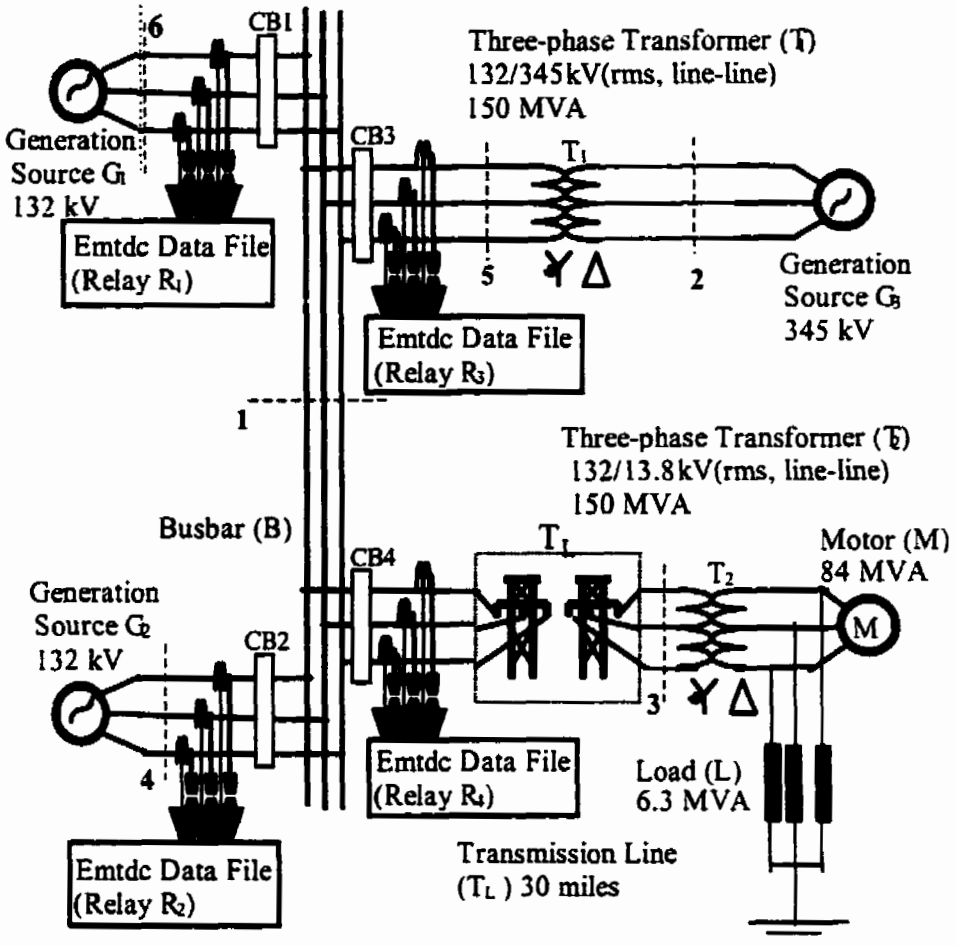
The proposed technique for correctly identifying internal and external faults in bus protection zones is presented in Chapter 3. Fault-detection characteristics of the relay are also established in that chapter. Two different power system configurations were used to verify the validity of the proposed technique. Different busbar arrangements and system operating-conditions were considered. The impacts of ct saturation and ratio-mismatch on the performance of the technique was also studied. Fault data were generated by simulating faults in power systems by using EMTDC [49], an electromagnetic transient program. This chapter describes the procedure used in the simulations and presents results showing that the proposed technique works well.

5.2. System modeling

The data for testing the proposed technique were generated on a Sun SPARC workstation using EMTDC - an electromagnetic transient program. Two model power-systems were selected for generating the fault data. These models are described in the following sections.

5.2.1. Model system

A typical power system used in this project is shown in Figure 5.1. In this figure, a busbar (B) is connected to systems represented by three equivalent sources G_1, G_2 and G_3, a motor M, and a static load L at the end of a transmission line, T_L. The busbar is protected by relays, R_1, R_2, R_3 and R_4, which are located at the busbar end of the circuits. The electrical parameters of the elements, shown in Figure 5.1, are given in Appendix D.



CB1, CB2, CB3, CB4 : Circuit breakers

Figure 5.1. Power system used for simulating data.

5.2.2. BRADA substation

The configuration of the BRADA substation and a model of the SaskPower transmission system were also used for testing the technique. Figure 5.2 shows the equivalent power system and parameters of the system components. The substation has two busbars to which five circuits, operating at 230 kV and 138 kV levels, are connected. The data for the substation was obtained from SaskPower. Details of the system parameters are provided in Appendix D.

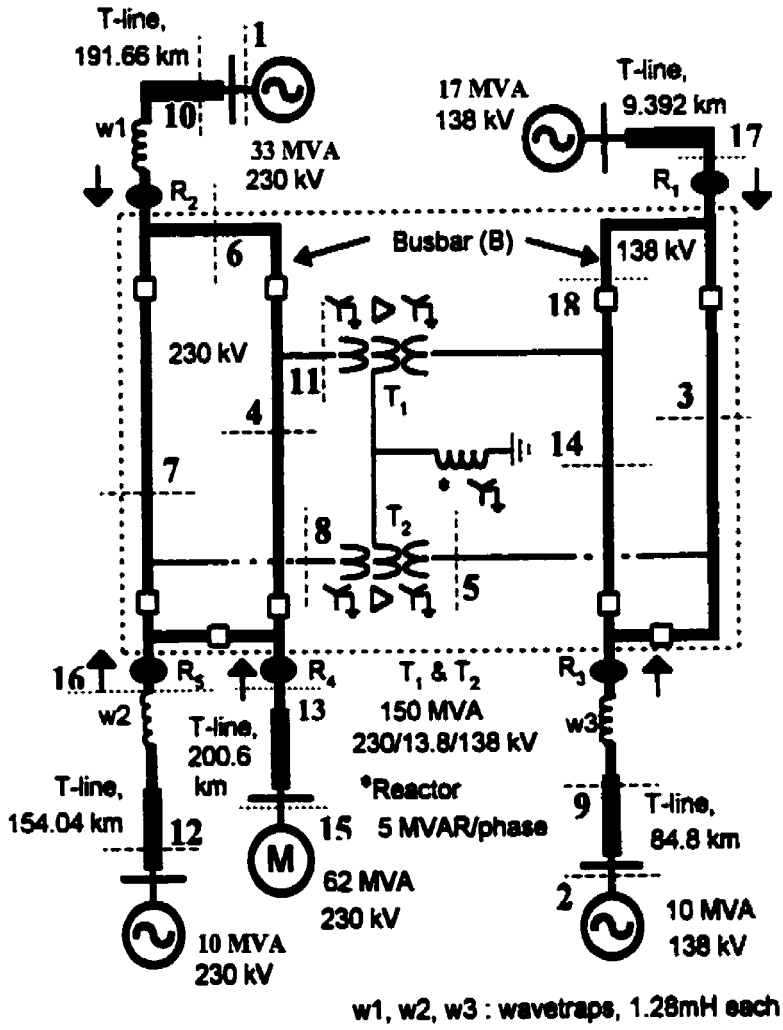


Figure 5.2. Bus configuration of the BRADA substation of SaskPower and the equivalent sources used for generating fault data.

The proposed technique was tested by using the data obtained from simulations of operating conditions of the substation. Faults of different types, and at various locations, were considered. The fault locations used in the studies are indicated in Figure 5.2.

5.3. Signal processing

The power system models described in the previous section were used in the simulation studies. An overview of the EMTDC software, which was used for generating

fault data, is given in Appendix E. The ct model [50] developed at the University of Manitoba, Canada was used in the studies. The fault data were generated from the simulations using calculation steps of 43.4 μs (23040 Hz). This calculation step provides a reasonable approximation to the continuous-time domain signals. The output from the EMTDC was then pre-processed using digital-equivalents of a 4th order Butterworth filter implemented on the MATLAB. The filtered data were re-sampled at 1440 Hz. Since the Nyquist criterion requires that all frequency components of 720 Hz and higher frequencies should be suppressed to prevent aliasing, cut-off frequency of 200 Hz was selected. Details of the anti-aliasing filter are given in Appendix F.

The Least Error Squares (LES) algorithm was used for computing the phasors of the fundamental frequency components from sampled (and quantized) data. The LES filters were designed for a data-window of 25 samples and a sampling rate of 1440 Hz. The proposed technique was implemented using a program written in ANSI C.

As stated in Chapter 3, the inception of a fault can be detected by comparing the recently quantized values of voltages and currents with those quantized one cycle earlier. The threshold for the changes in the instantaneous values, V_CHANGE, and I_CHANGE, were set at 3.5% and 10% respectively. The value of MINIMUM, the minimum magnitude of positive- and negative-sequence incremental voltages and currents, was set at 1% of the pre-fault values. To ensure sensitivity and to maintain security, the limits of the trip counter, THRESHLD, were set at ±6.

5.4. Test studies

Power system models, shown in Figures 5.1 and 5.2, were simulated for generating data that were used to check the performance of the proposed technique. Different types of faults were simulated and the voltages and currents at the relay locations were recorded in data files. Several busbar configurations and different operating conditions of the selected power systems were considered. The impacts of ct saturation and ct ratio-mismatch conditions were also studied. Selected test results are presented in this section.

5.4.1. Internal faults

Internal faults were simulated at various locations in the bus zone of the substation of Figure 5.1 and the BRADA substation. Some test studies are presented in the following sections; additional cases are presented in Appendix G.

5.4.1.1. Single phase-to-ground faults

Single phase-to-ground faults, at different locations in the selected substations were simulated with and without fault resistance. This section presents sample results from these studies.

A solid Phase B-ground fault was simulated on location 1 of the substation shown in Figure 5.1 except that the busbar was configured in the form of a ring as shown in Figure 5.3. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. Figure 5.4 shows the arguments and magnitudes of positive- and negative-sequence impedances computed by the relays R_1, R_2, R_3, and R_4. This figure shows that all the arguments of the sequence impedances lie in the third quadrant. This means that the fault is in the busbar protection zone. The positive-sequence (and negative-sequence) trip counters for the relays R_1 to R_4 are incremented and reach the threshold in 6 (6), 6 (6), 6 (6) and 6 (6) samples respectively. It took the algorithm seven samples to confirm that the fault was in the busbar zone. The algorithm, therefore, took 4.86 ms (i.e. 7/1440 ms) to make the final decision. The study was repeated in which cts of relays 1, 2 and 3 saturated. The positive- and negative-sequence trip counters of the relays R_1 to R_4 reached the threshold in 6 samples. The algorithm took 4.86 ms to make the decision in this case as well.

A Phase A-to-ground fault in the protection zone of the busbar was simulated at location 11 in the substation shown in Figure 5.2. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors

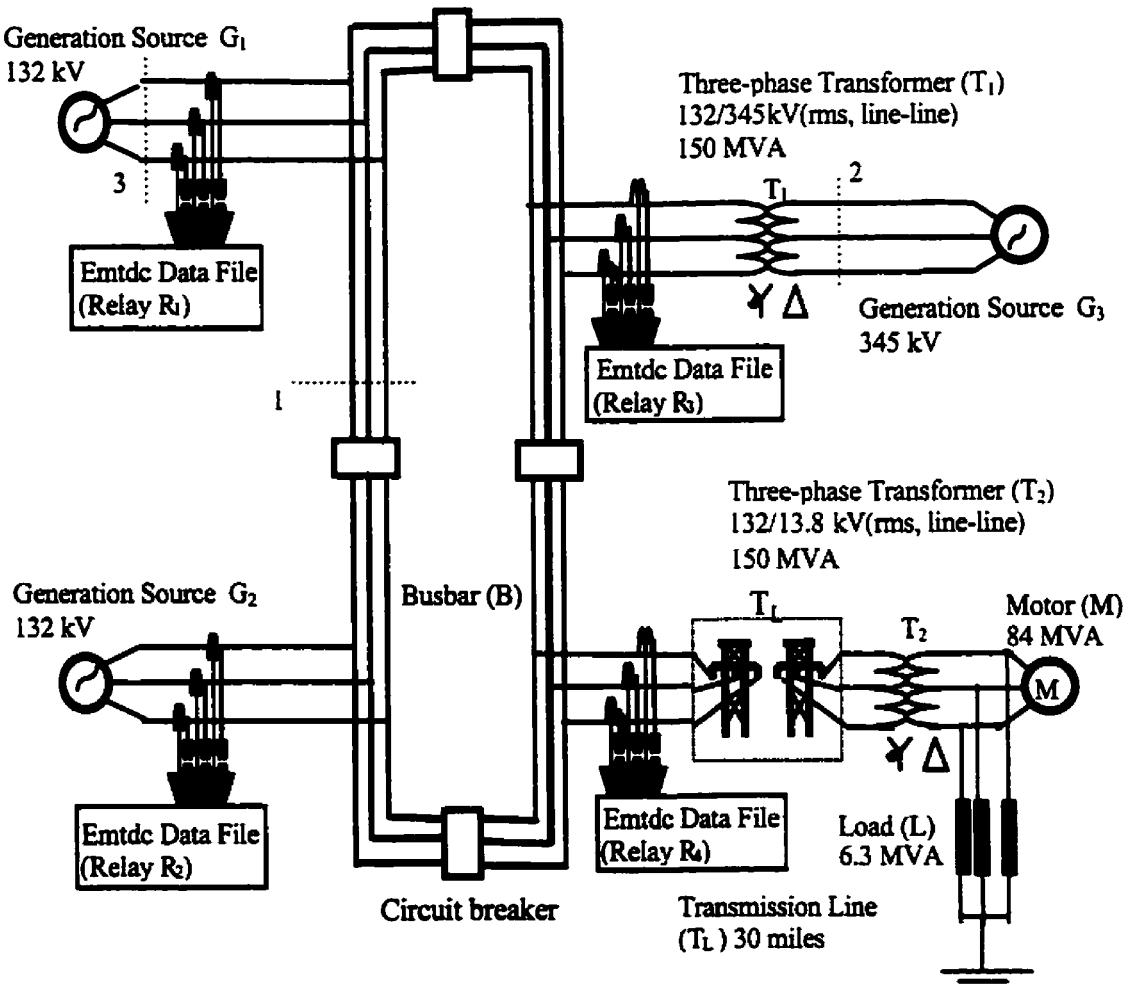


Figure 5.3. Power system, with ring bus configuration used in the simulations.

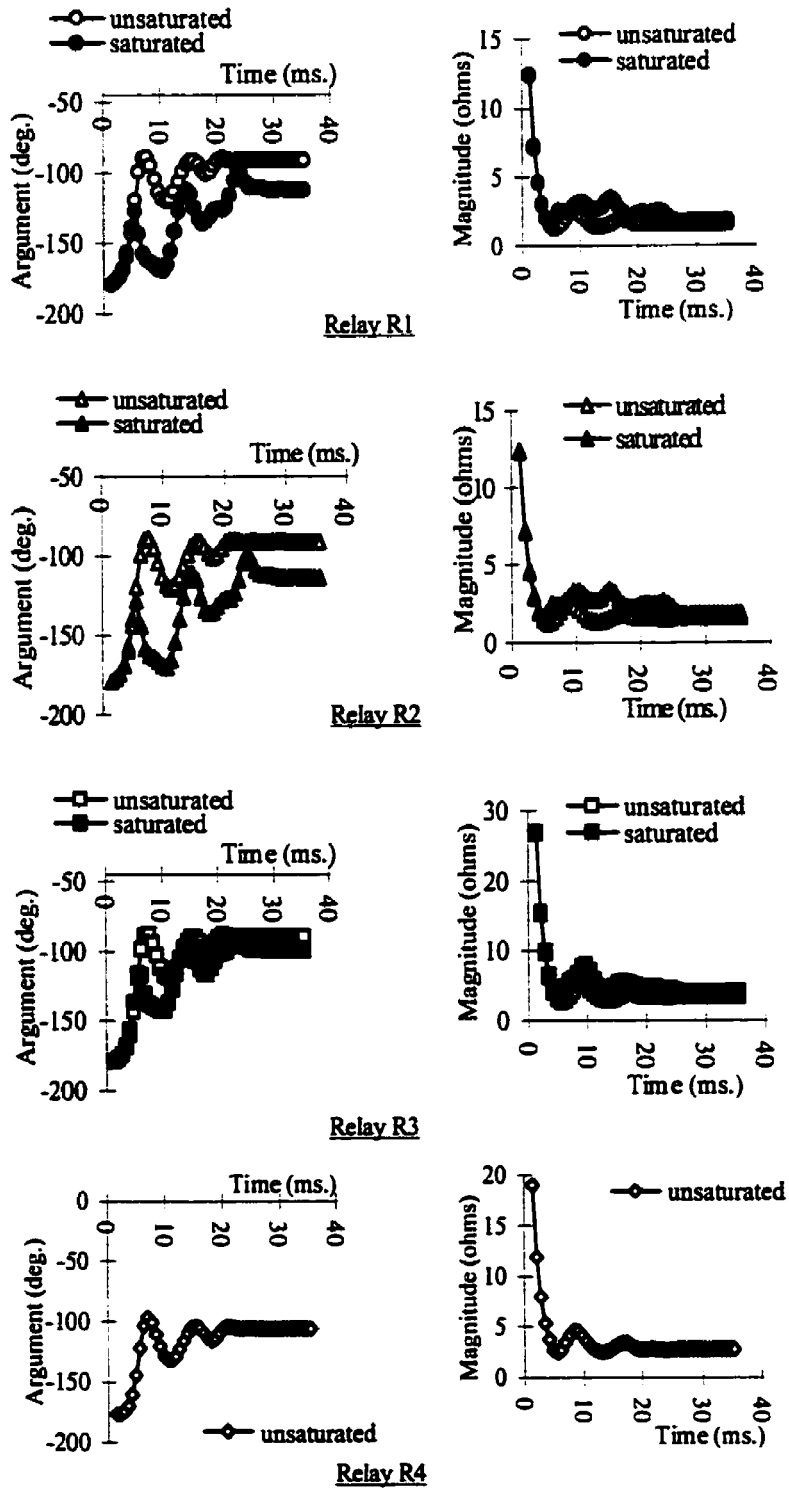


Figure 5.4 (a). Plots of the arguments and magnitudes of the positive-sequence impedance computed by the relays for Phase B-ground fault in the busbar protection zone of the substation of Figure 5.3.

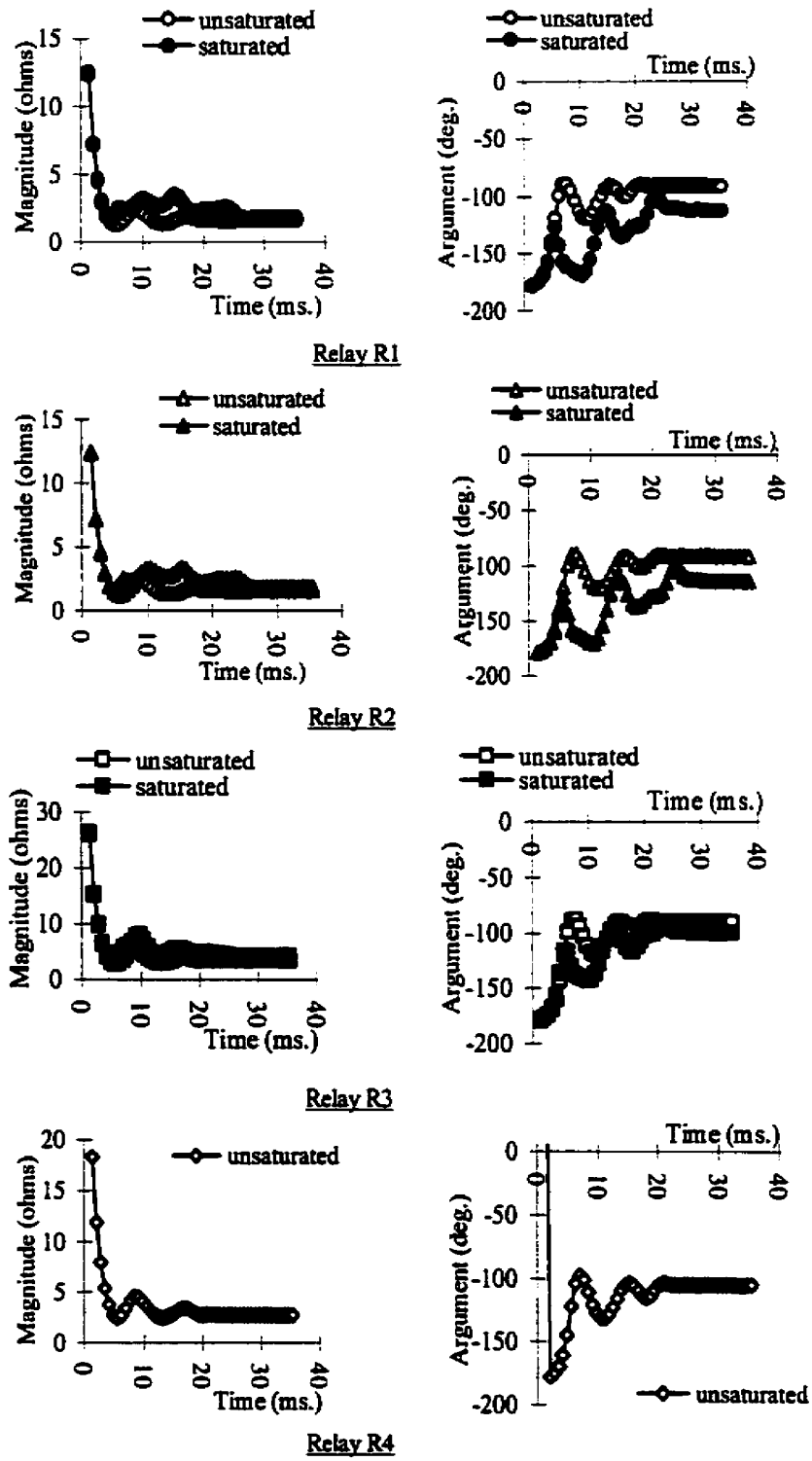


Figure 5.4 (b). Plots of the arguments and magnitudes of the negative-sequence impedance computed by the relays for Phase B-ground fault in the busbar protection zone of the substation of Figure 5.3.

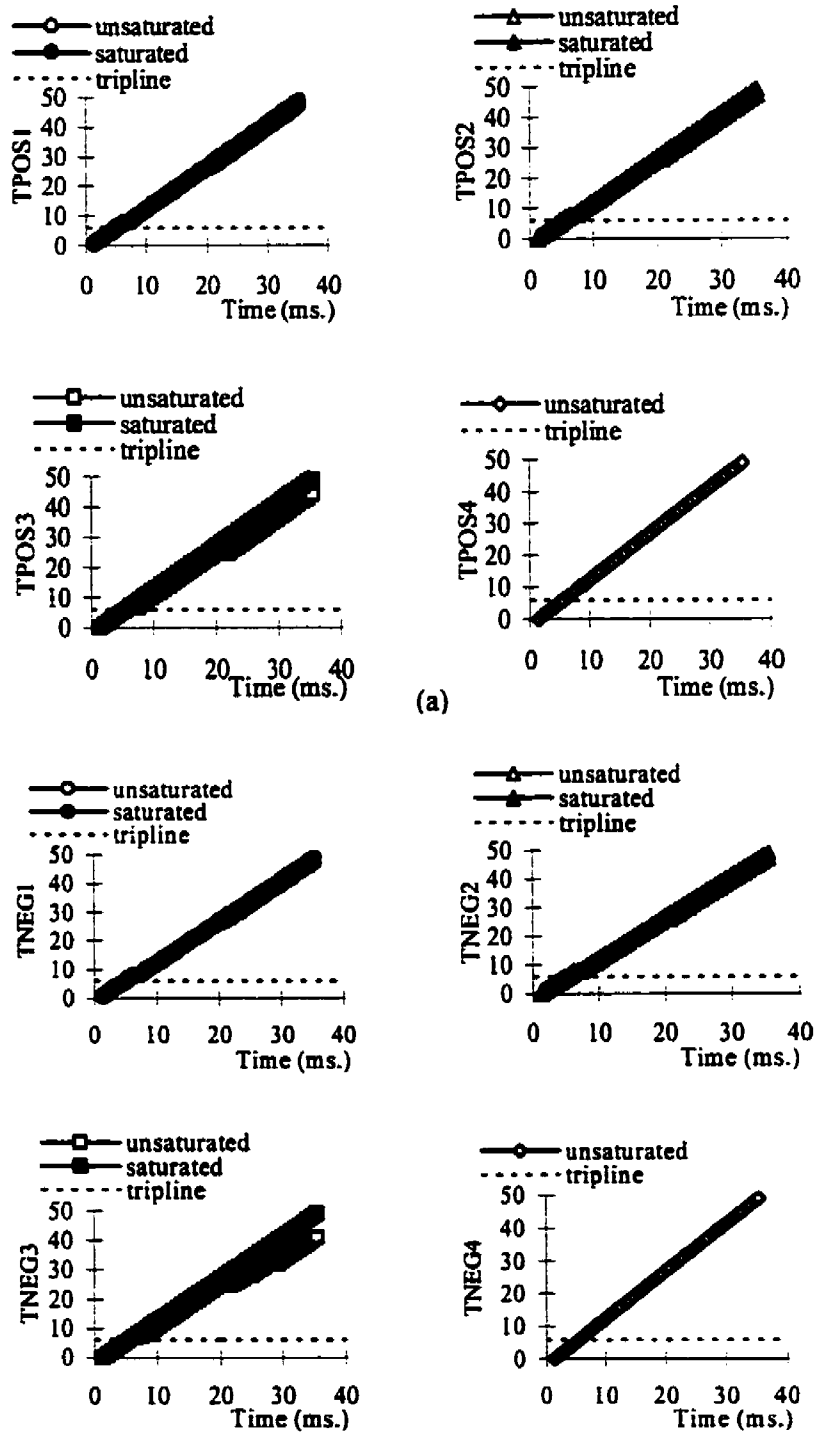


Figure 5.4 (c). Profile of the (a) positive-sequence, and (b) negative-sequence trip-counters for a Phase B-ground fault in the busbar protection zone of the substation of Figure 5.3.

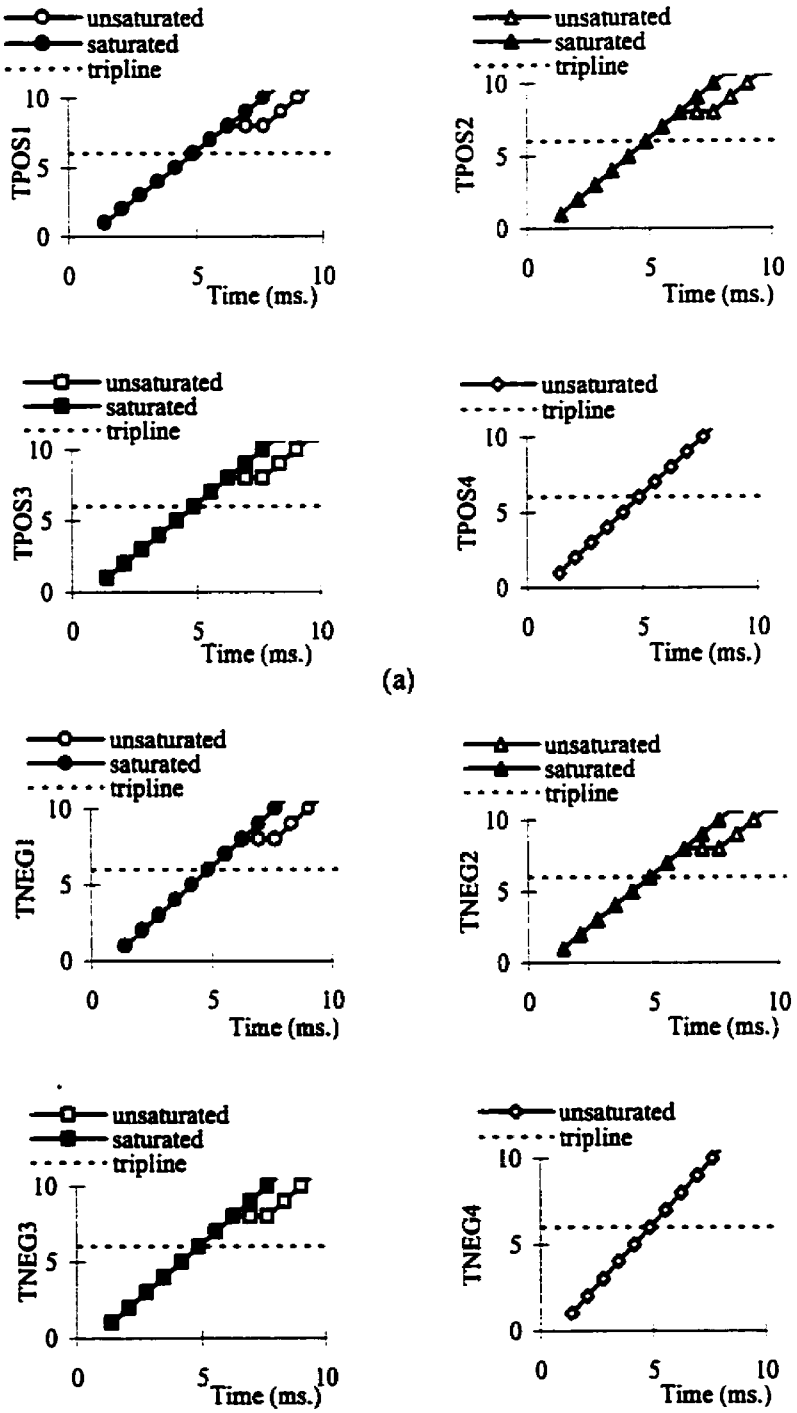


Figure 5.4 (d). Profile of the (a) positive-sequence, and (b) negative-sequence trip-counters (on expanded scales) for a Phase B-ground fault in the busbar protection zone of the substation of Figure 5.3.

of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. The profiles of voltage and current waveforms acquired at the relays are shown in Figure 5.5. Figure 5.6 shows the profile of the magnitudes and arguments of the sequence-impedances and the trip counters of the relays. For this case, the arguments of all the computed positive- and negative-sequence impedances lie in the third quadrant. This indicates that the fault is in the protection zone of the busbar. When the cts did not saturate, the positive-sequence (and negative-sequence) trip counters of the relays R_1, R_2, R_3, R_4, and R_5 reached the threshold in 6 (6), 9 (11), 8 (7), 9 (9) and 12 (12) samples respectively. At 13th sampling instant, the trip-logic confirmed that the fault was in the protection zone of the busbar. It took the algorithm 9.03 ms (i.e. 13/1440 ms) to make the final decision. When the ct of relay R_1 saturated, the positive- (and negative-) sequence trip-counters reached the threshold in 6 (6) samples. Since the cts located at relays R_2, R_3, R_4 and R_5 did not saturate, their sequence trip counters took the same time as before. In this case also, the algorithm took 9.03 ms to make a final decision.

5.4.1.2. Phase-to-phase faults

A solid Phase A-Phase B fault was simulated on location 1 of the substation shown in Figure 5.1 except that the busbar was configured as a breaker-and-half scheme as shown in Figure 5.7. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. Figure 5.8 shows the arguments and magnitudes of positive- and negative-sequence impedances computed by the relays R_1, R_2, R_3, and R_4. This figure shows that all the arguments of the sequence impedances lie in the third quadrant. This means that the fault is in the busbar protection zone. The positive-sequence (and negative-sequence) trip counters for the relays R_1 to R_4 reached the threshold in 6 (6) samples. After 7 samples, the algorithm confirmed that the fault was in the busbar zone. The algorithm took 4.86 ms (i.e. 7/1440 ms) to make the final decision. The study was repeated in which cts of relays 1 and 2 saturated. The positive- and negative-sequence trip counters

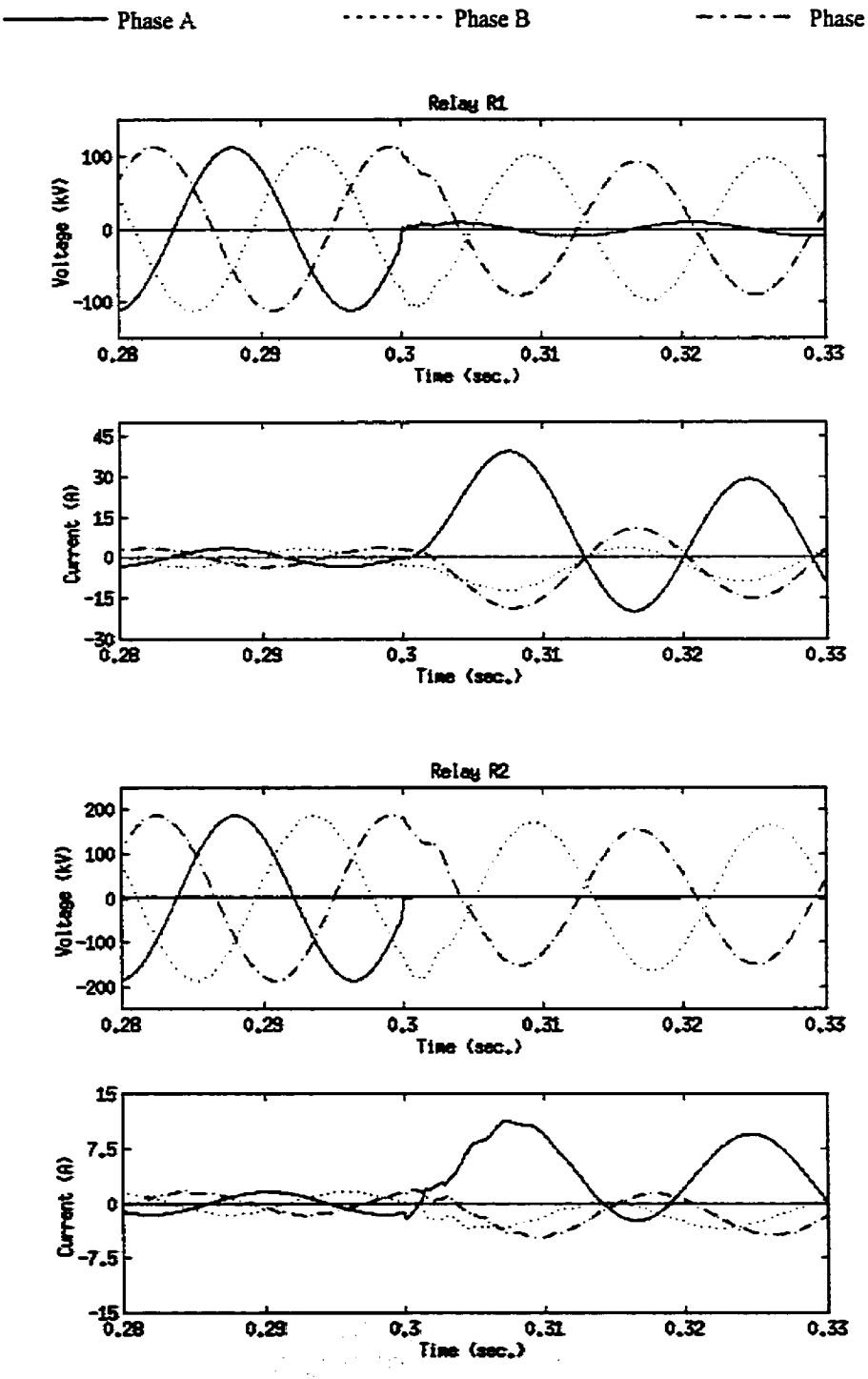


Figure 5.5. Profiles of phase voltage and current waveforms applied to the relays when a Phase A-ground fault at location 11 in Figure 5.2 was simulated, and no cts saturated.

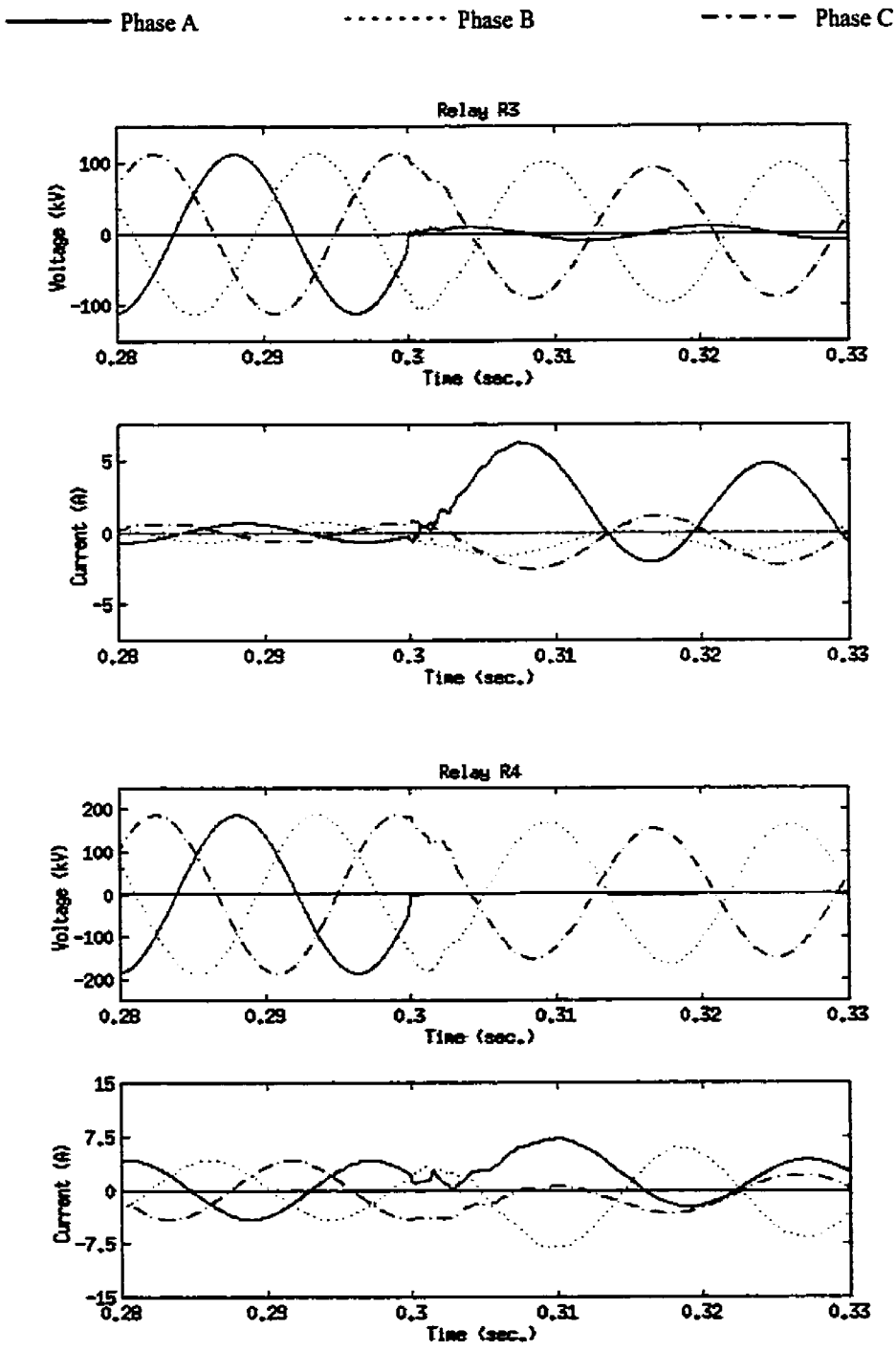


Figure 5.5 (contd.). Profiles of phase voltage and current waveforms applied to the relays when a Phase A-ground fault at location 11 in Figure 5.2 was simulated, and no cts saturated.

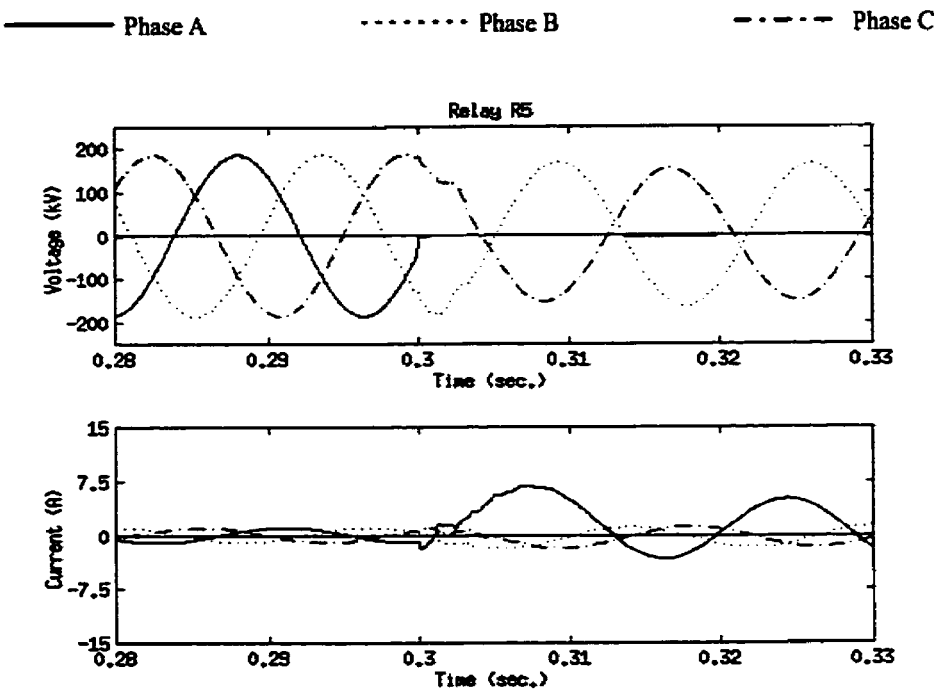


Figure 5.5 (contd.). Profiles of phase voltage and current waveforms applied to the relays when a Phase A-ground fault at location 11 in Figure 5.2 was simulated, and no cts saturated.

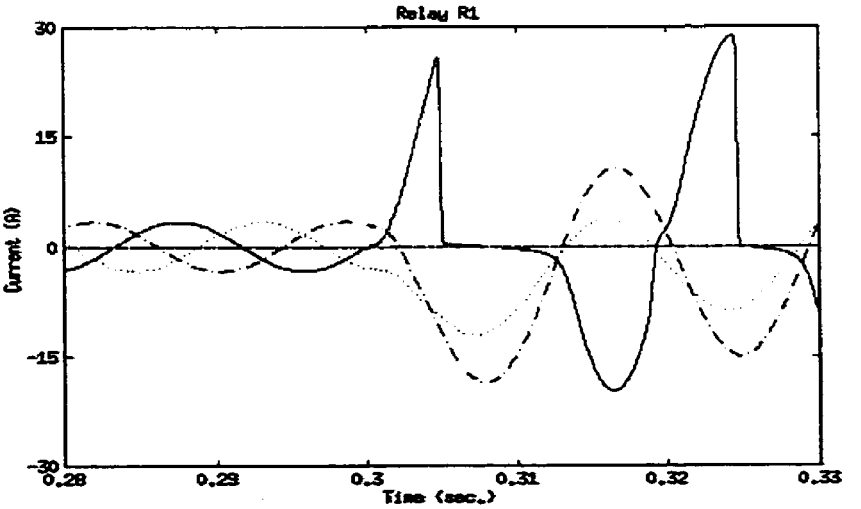


Figure 5.5 (contd.). Profiles of phase voltage and current waveforms applied to the relays when a Phase A-ground fault at location 11 in Figure 5.2 was simulated, and the ct saturated.

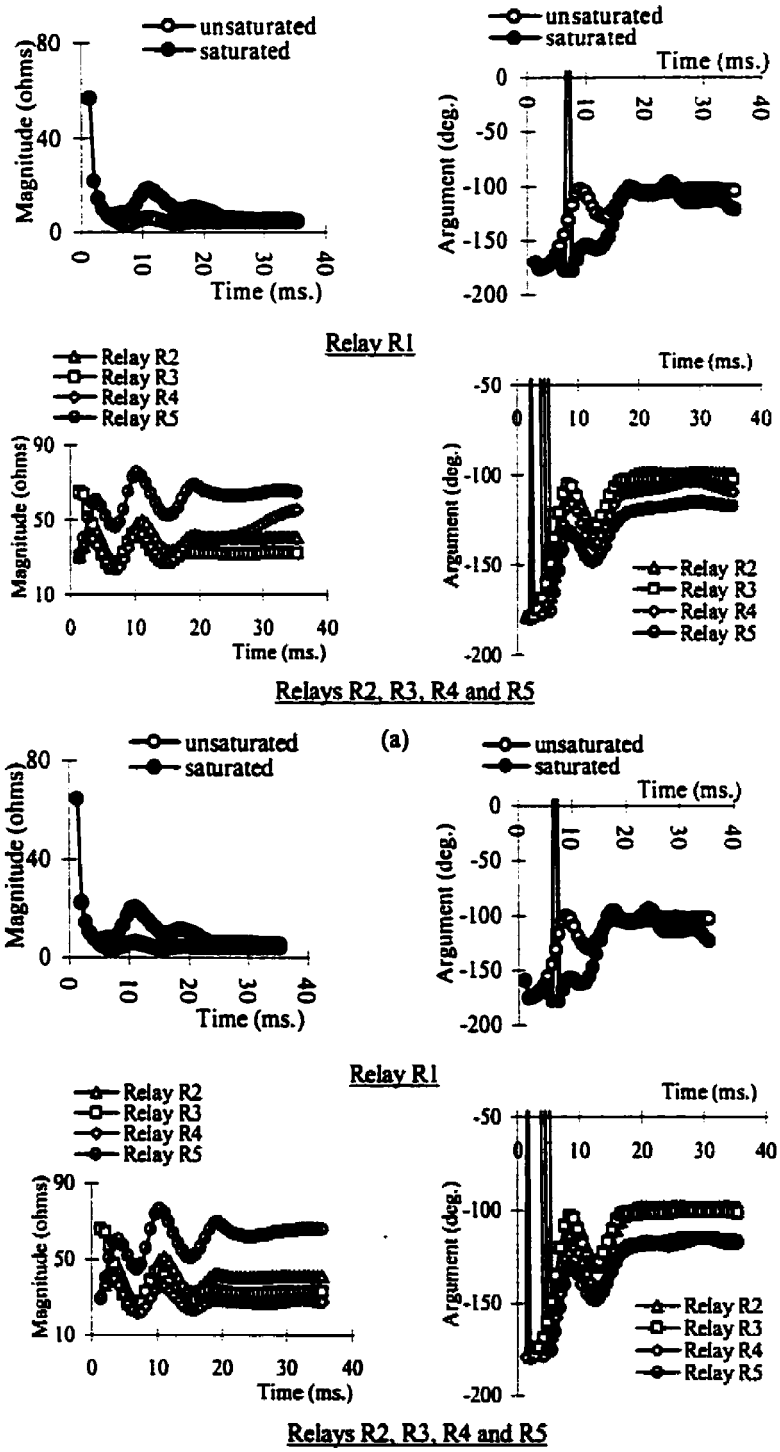


Figure 5.6 (a). Plots of the arguments and magnitudes of the (a) positive- and (b) negative-sequence impedances computed by the relays for a Phase A-ground fault in the busbar protection zone of the BRADA substation.

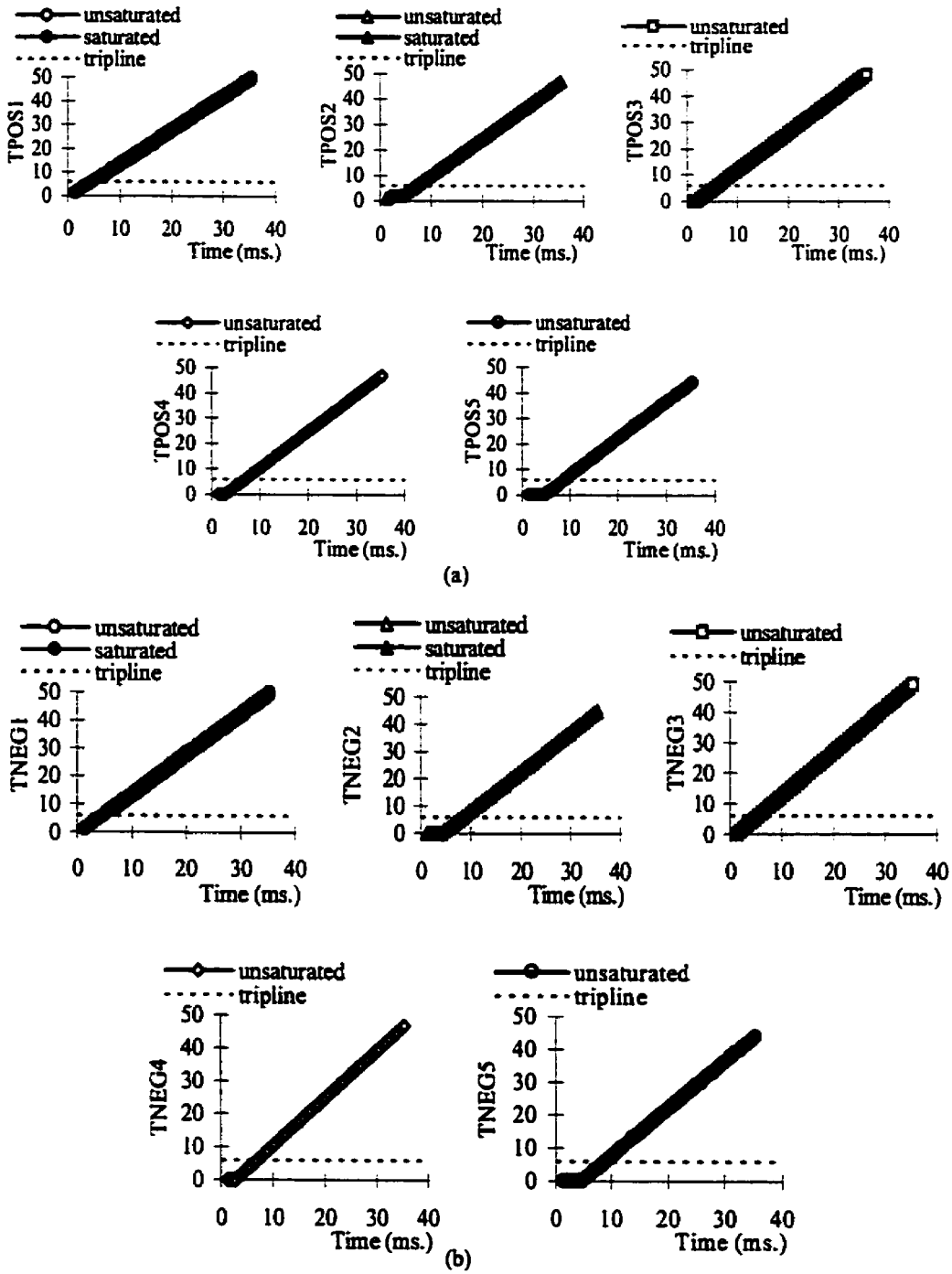
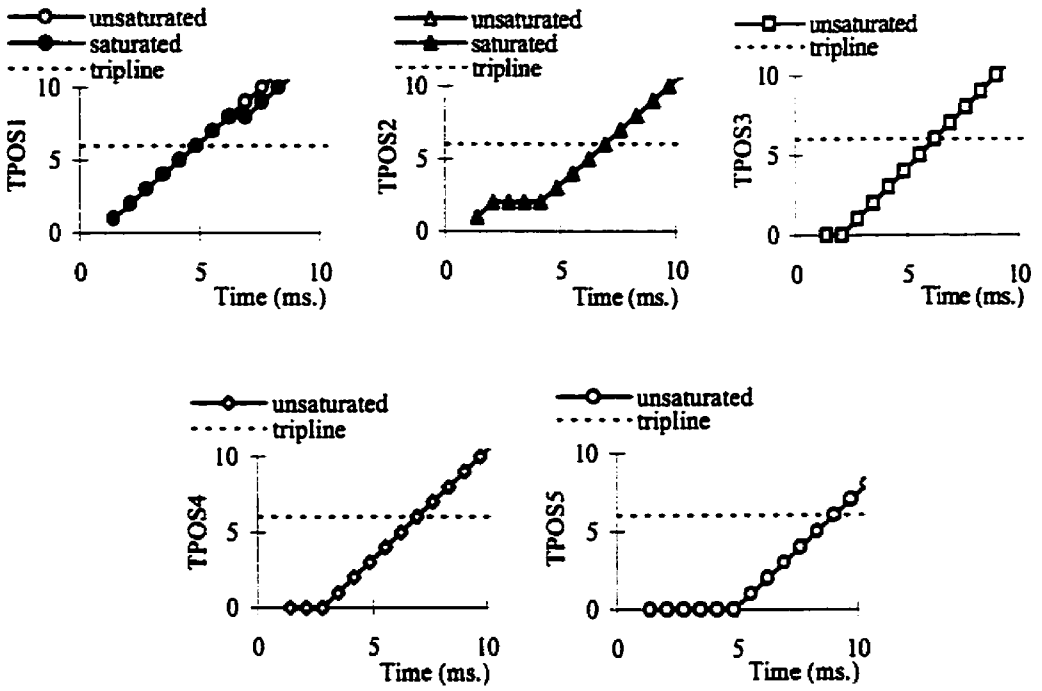
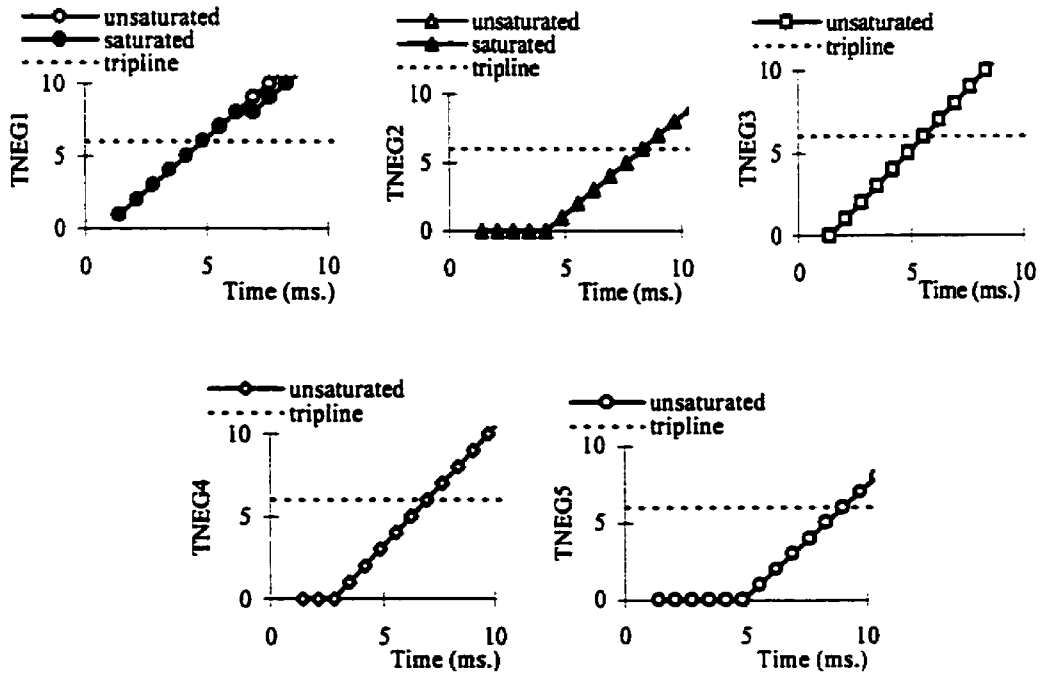


Figure 5.6 (b). Profiles of the (a) positive-sequence, and (b) negative-sequence trip-counters for a Phase A-ground fault at location 11 of the BRADA substation.



(a)



(b)

Figure 5.6 (c). Profiles of the (a) positive-sequence, and (b) negative-sequence trip-counters (on expanded scales) for a Phase A-ground fault at location 11 of the BRADA substation.

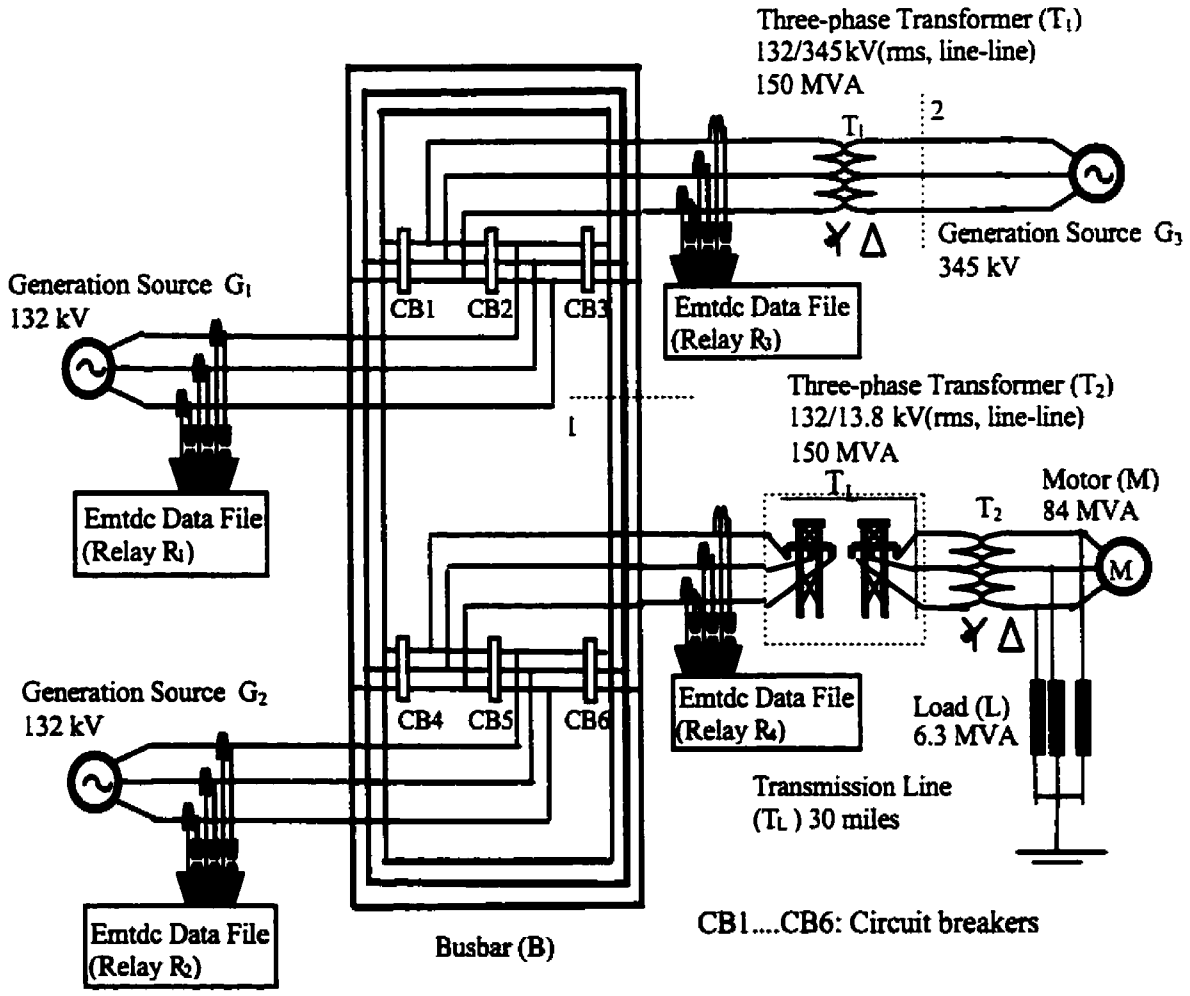


Figure 5.7. Power system with breaker-and-half bus configuration used in the simulations.

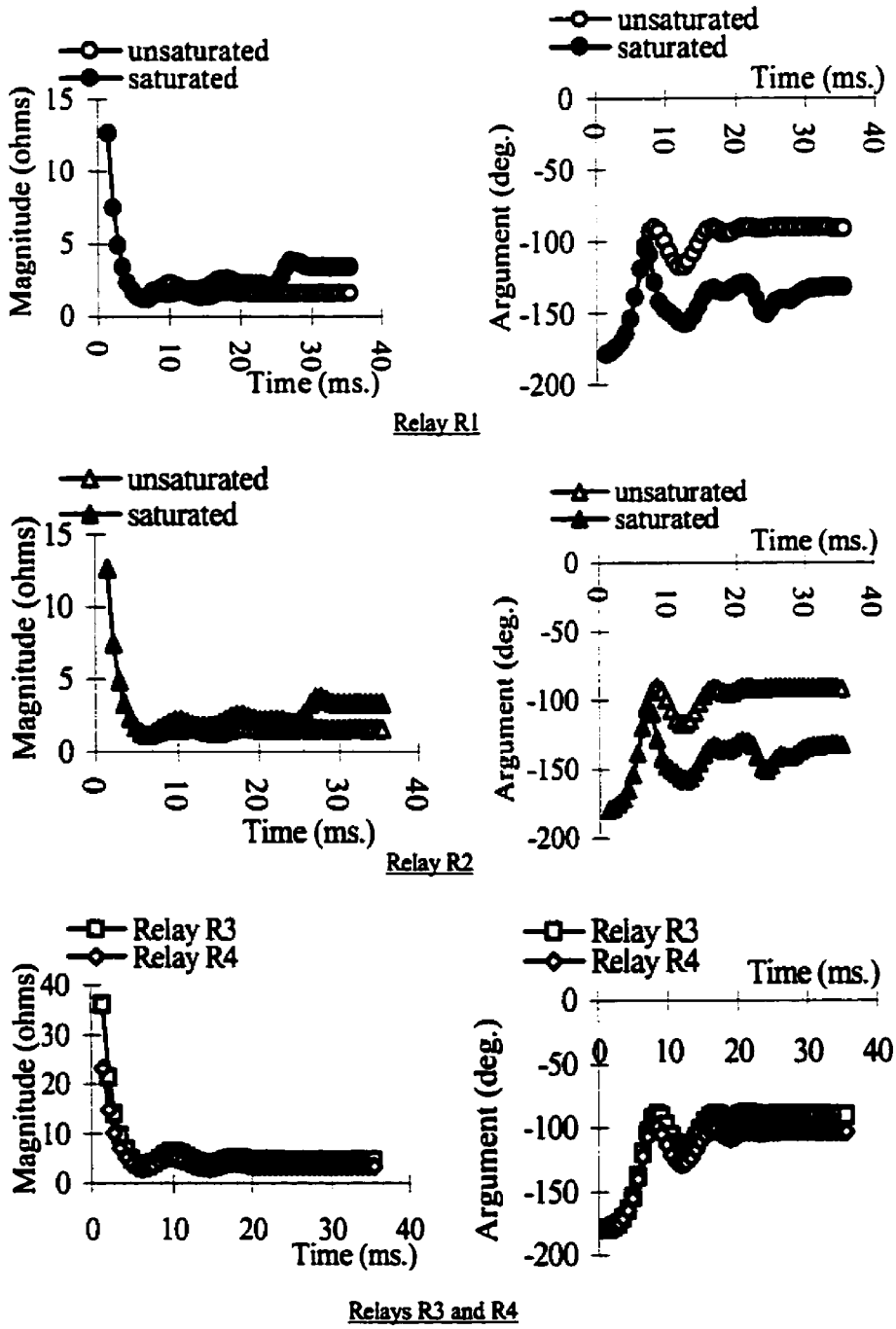


Figure 5.8 (a). Plots of the arguments and magnitudes of the positive-sequence impedances computed by the relays for Phase A-Phase B fault in the busbar protection zone of the substation of Figure 5.7.

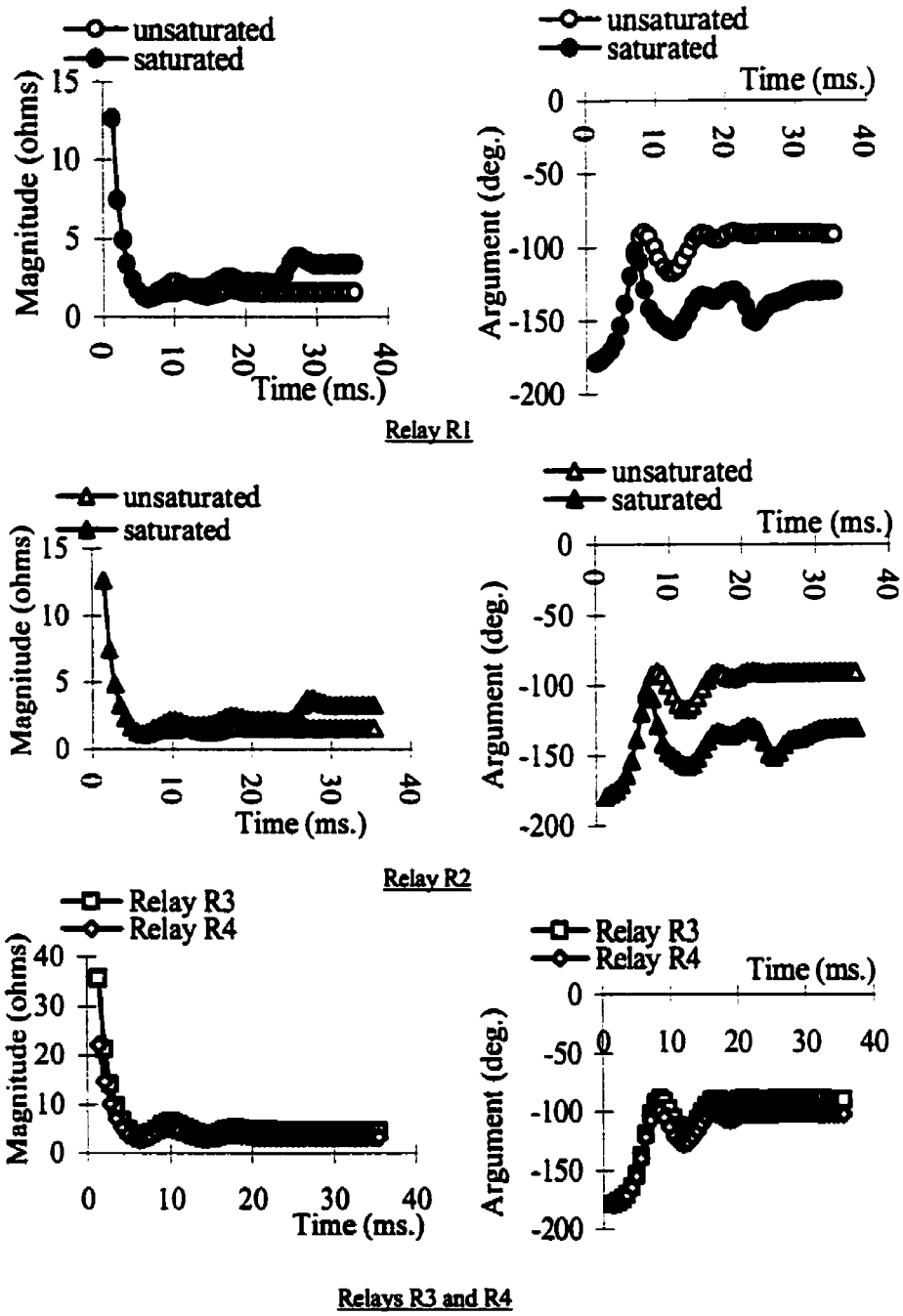


Figure 5.8 (b). Plots of the arguments and magnitudes of the negative-sequence impedances computed by the relays for Phase A-Phase B fault in the busbar protection zone of the substation of Figure 5.7.

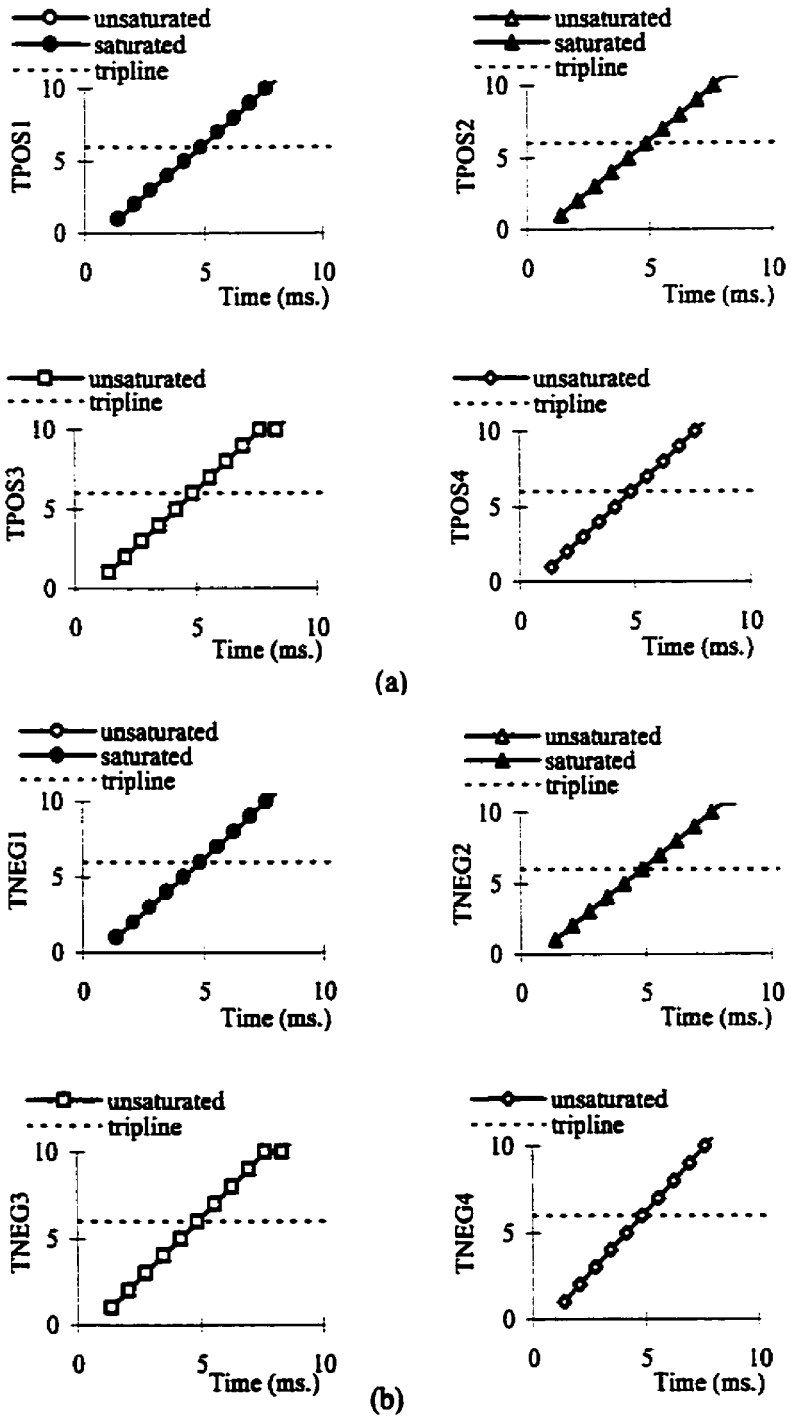


Figure 5.8 (c). Profile of the positive-sequence, and negative-sequence trip-counters for a Phase A-Phase B fault in the busbar protection zone of the substation of Figure 5.7.

of relays R_1 to R_4 reached the threshold in 6 samples. The algorithm took 4.43 ms to make the decision in this case.

A Phase A-Phase C fault in the protection zone of the busbar was simulated at location 14 in the substation shown in Figure 5.2. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. Figure 5.9 shows the profile of the magnitudes and arguments of the sequence-impedances and the trip counters of the relays. In this case, the arguments of all the positive- and negative-sequence impedances lie in the third quadrant. This indicates that the fault is in the protection zone of the busbar. When the cts did not saturate, the positive-sequence (and negative-sequence) trip counters of the relays R_1, R_2, R_3, R_4, and R_5 reached the threshold in 7 (7), 10 (9), 7 (7), 9 (8) and 14 (14) samples respectively. At 15th sampling instant, the trip-logic confirmed that the fault was in the protection zone of the busbar. It took the algorithm 10.42 ms (i.e. 15/1440 ms) to make the final decision. When the ct of relay R_1 saturated, the positive- (and negative-) sequence trip-counters reached the threshold in 7 (7) samples respectively. Since the cts located at relays R_2, R_3, R_4 and R_5 did not saturate, their sequence trip counters took the same time as before. In this case also, the algorithm took 10.42 ms to make a final decision.

5.4.1.3. Three-phase faults

A three phase-to-ground fault was simulated on location 1 of the substation shown in Figure 5.3. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. Figure 5.10 shows the arguments and magnitudes of positive-sequence impedances computed by the relays R_1, R_2, R_3, and R_4. This figure shows that all the arguments of the positive-sequence impedances lie in the third quadrant. This means that

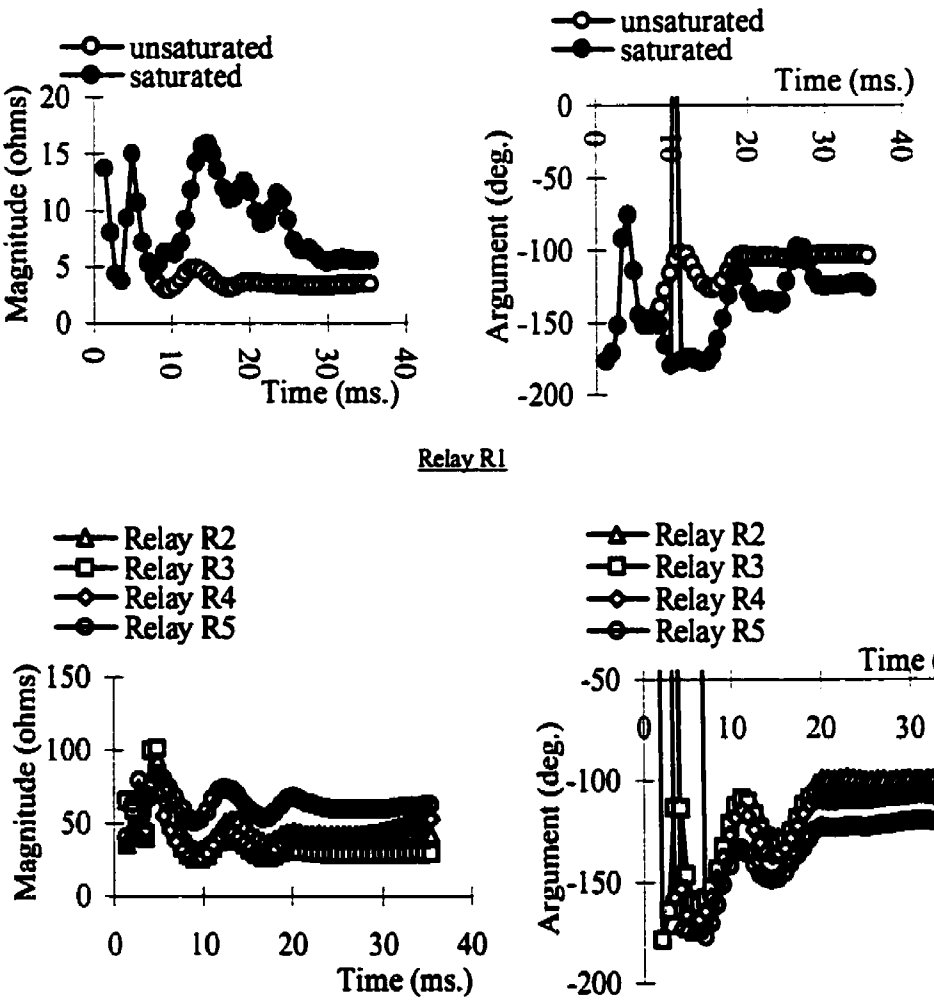
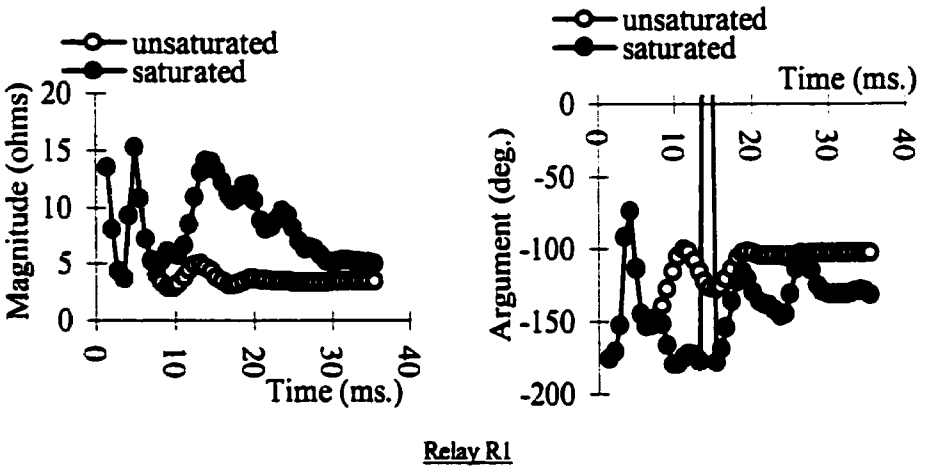


Figure 5.9 (a). Plots of the arguments and magnitudes of the positive-sequence impedances computed by the relays for a Phase A-Phase C fault in the busbar protection zone of the BRADA substation.



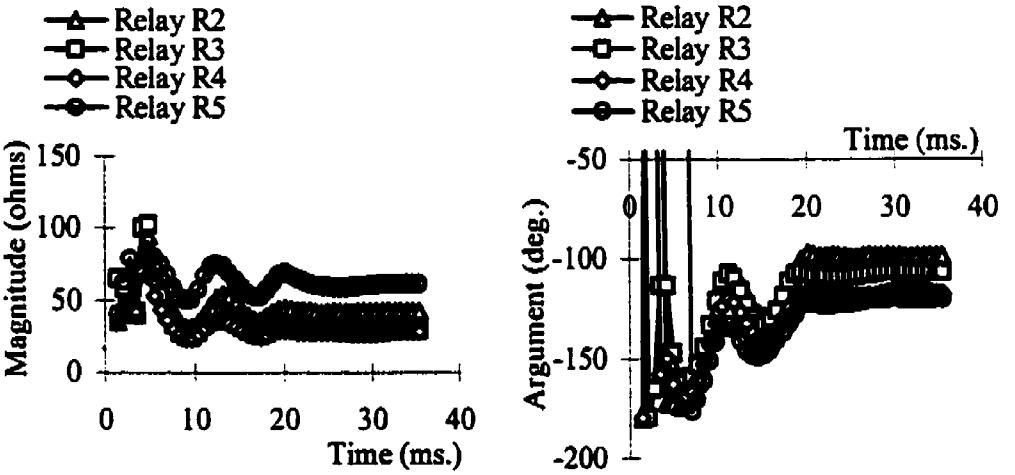


Figure 5.9 (b). Plots of the arguments and magnitudes of the negative-sequence impedances computed by the relays for a Phase A-Phase C fault in the busbar protection zone of the BRADA substation.

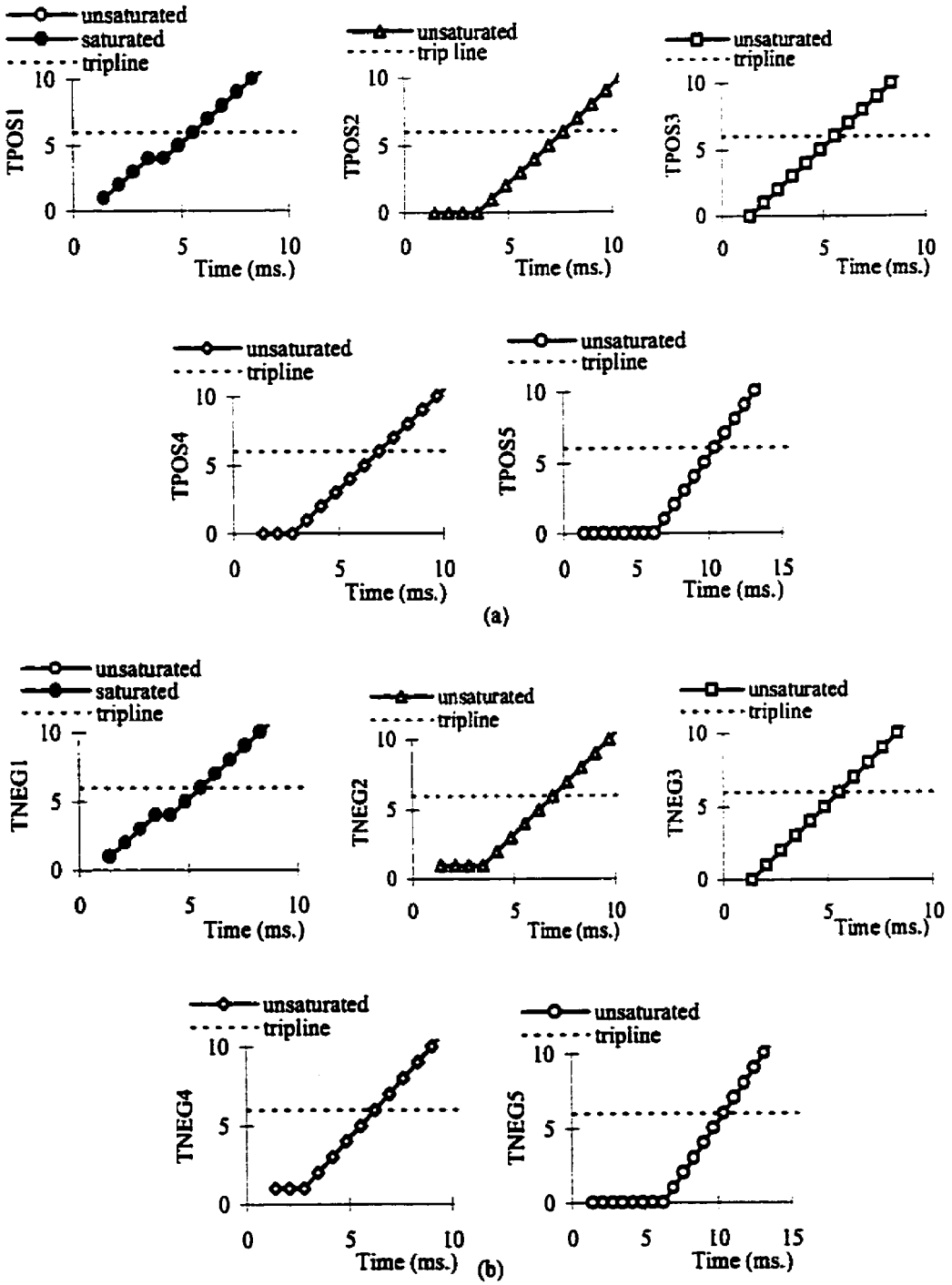


Figure 5.9 (c). Profiles of the (a) positive-sequence, and (b) negative-sequence trip-counters for a Phase A-Phase C fault at location 11 of the BRADA substation.

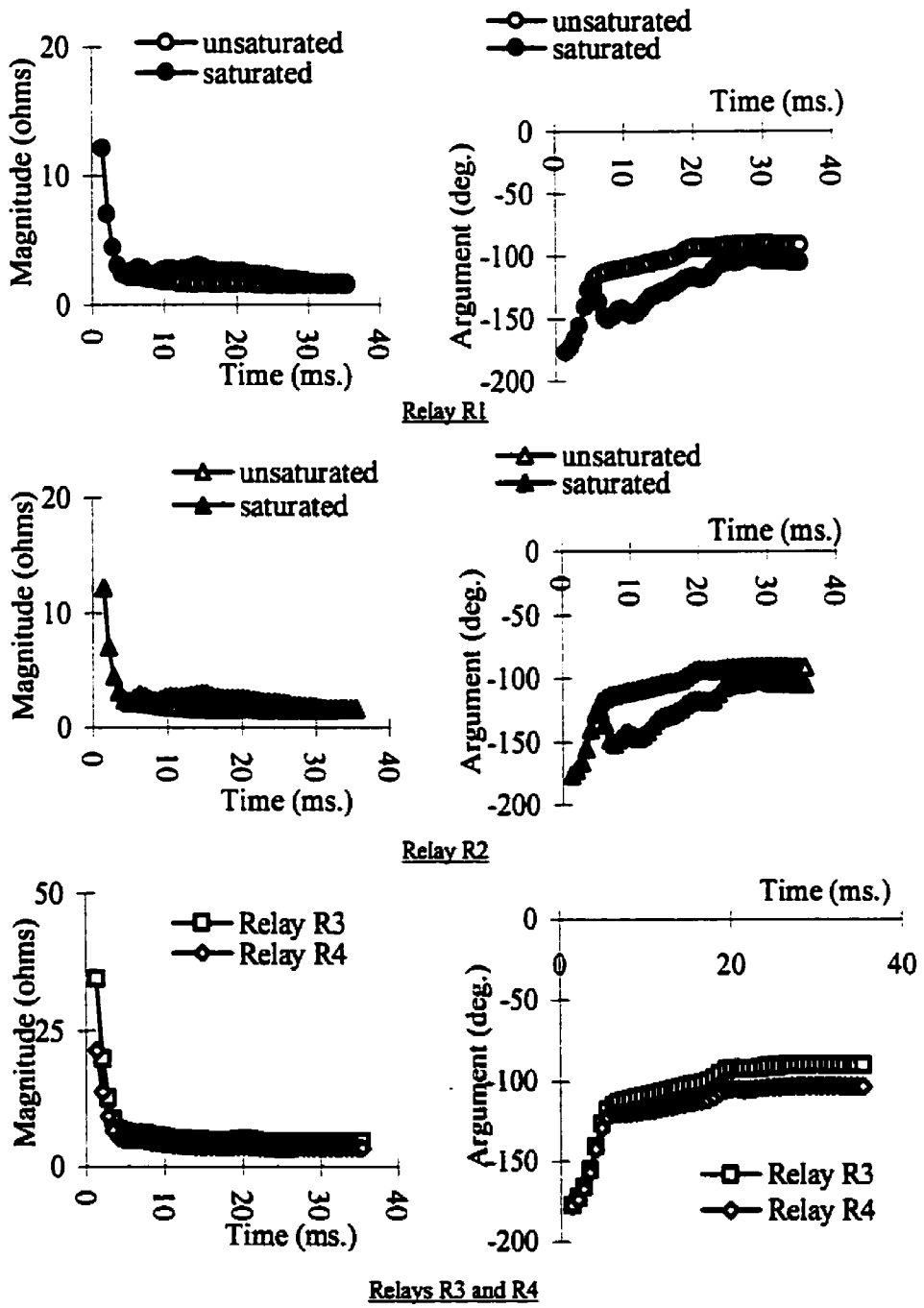


Figure 5.10 (a). Plots of the arguments and magnitudes of the positive-sequence impedances computed by the relays for a three phase-ground fault in the busbar protection zone of the substation of Figure 5.3.

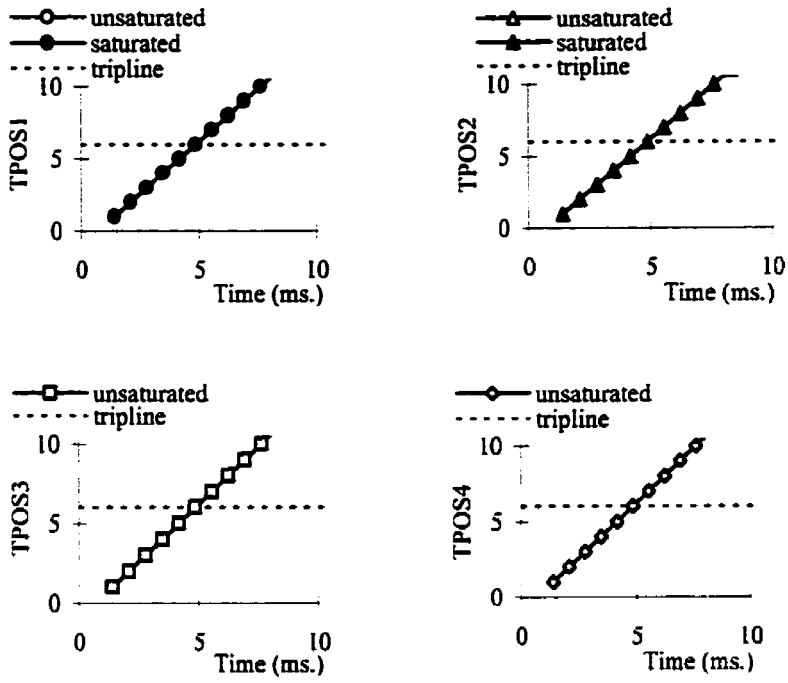


Figure 5.10 (b). Profile of the positive-sequence trip-counters for a three phase-ground fault in the busbar protection zone of the substation of Figure 5.3.

the fault is in the busbar protection zone. The positive-sequence trip counters for the relays R_1 to R_4 reached the threshold in 6 samples. After 7 samples, the algorithm confirmed that the fault was in the busbar zone. The algorithm took 4.86 ms (i.e. 7/1440 ms) to make the final decision. The study was repeated in which the cts of relays 1 and 2 saturated. The positive-sequence trip counters of relays R_1 to R_4 reached the threshold in 6 samples each. The algorithm took 4.86 ms to make the decision in this case. Because no negative-sequence voltages and currents were experienced during a three-phase fault, no conclusion was generated by those components.

A three phase fault in the bus protection zone was simulated at location 5 in the substation shown in Figure 5.2. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. Figure 5.11 shows the profile of the magnitudes and arguments of the

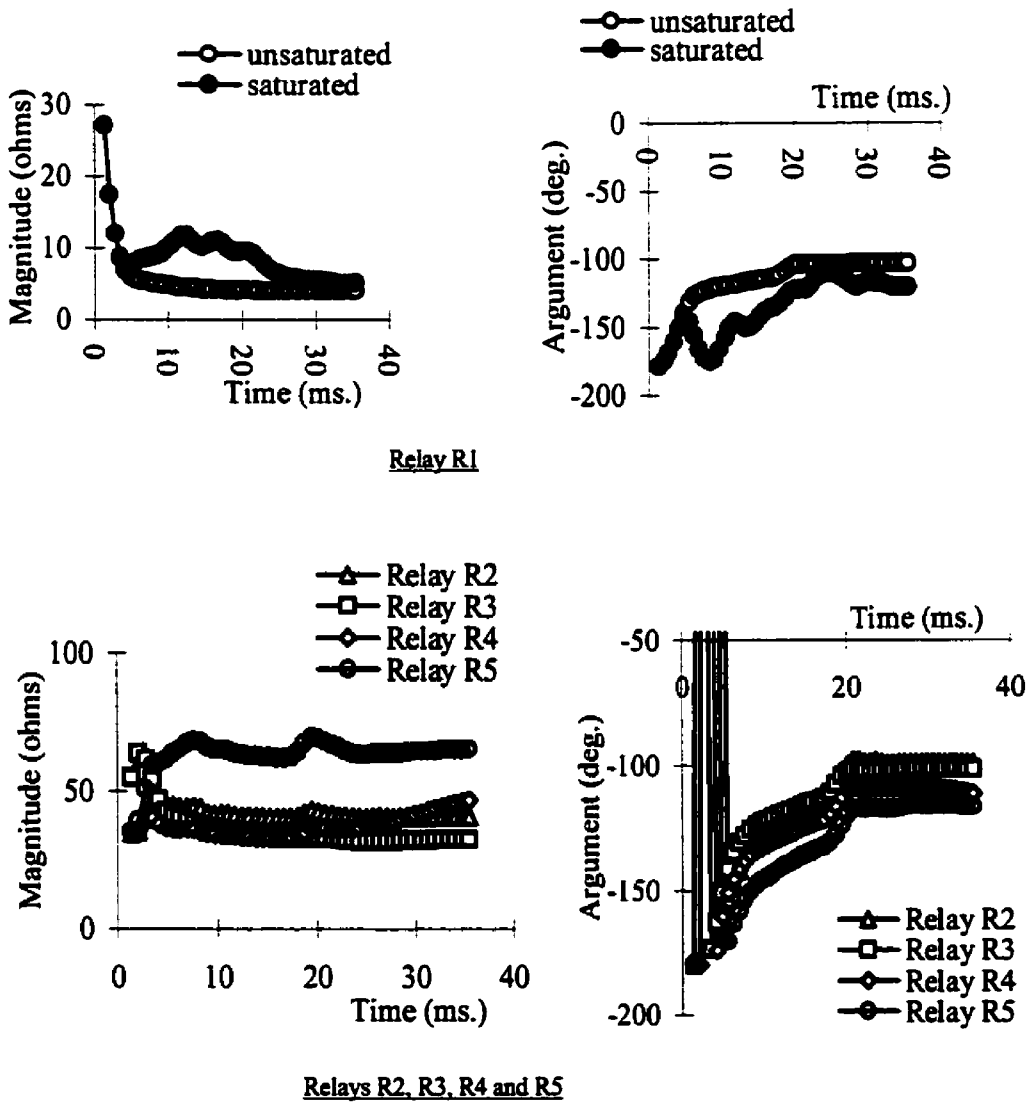


Figure 5.11 (a). Plots of the arguments and magnitudes of the positive-sequence impedances computed by the relays for a three phase fault in the busbar protection zone of the BRADA substation.

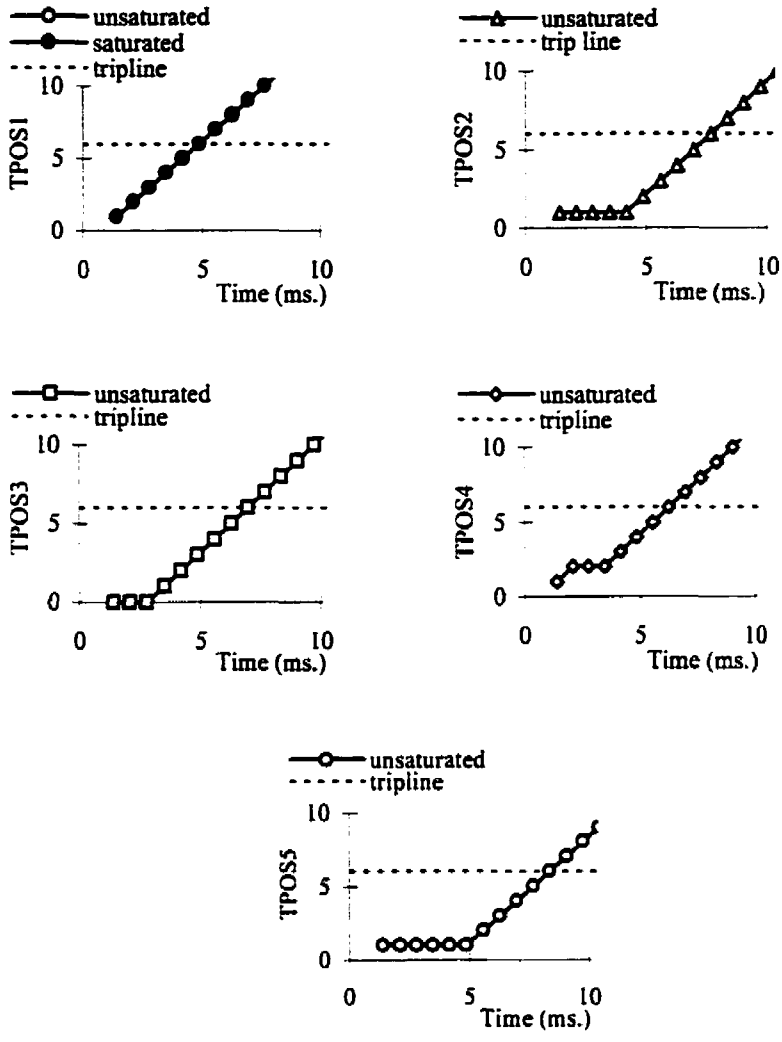


Figure 5.11 (b). Profiles of the positive-sequence trip-counters for a three phase fault at location 5 of the BRADA substation.

sequence-impedances and the trip counters of the relays. In this case, the arguments of all the computed positive-sequence impedances lie in the third quadrant indicating that the fault is in the protection zone of the busbar. When the cts did not saturate, the positive-sequence trip counters of the relays R_1, R_2, R_3, R_4, and R_5 reached the threshold in 6, 10, 9, 8 and 11 samples respectively. At the 12th sampling instant, the trip-logic confirmed the fault to be in the busbar protection zone. It took the algorithm 5.56 ms (i.e. 8/1440 ms) to make the final decision.When the ct of relay R_1 saturated, its positive-sequence trip-counter reached the threshold in 6 samples. Since the cts located at relays

R_2, R_3, R_4 and R_5 did not saturate, their sequence trip counters took the same time as before. In this case also, the algorithm took 8.33 ms to make a final decision.

5.4.2. External faults

Faults outside the bus-protection zone were simulated at selected locations in the power systems shown in Figures 5.1 and 5.2. Selected studies are presented in the following sections and additional studies are presented in Appendix G.

5.4.2.1. Single phase-to-ground faults

Single phase-to-ground faults, outside the bus protection zones of selected systems, were simulated. This section presents results of cases from the studies of both power system used for verification of the proposed technique.

A Phase C-ground fault was simulated on location 2 of the substation shown in Figure 5.3. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents, and sequence impedances were computed. Figure 5.12 shows the arguments and magnitudes of positive- and negative-sequence impedances computed by the relays. This figure shows that the arguments of the sequence impedances for relays R_1, R_2 and R_4 lie in the third quadrant. The arguments of the sequence-impedances for the relay R_3 lie in the first quadrant. This means that the fault is outside the busbar protection zone. The positive- (and negative-sequence) trip counters for the relays R_1, R_2 and R_4 are incremented and reach the threshold in 6 (6), 6 (6) and 7 (7) samples respectively. The positive- (and negative-sequence) trip counters for the relay R_3 are decremented and reach the threshold in 8 (8) samples. At the 9th sampling instant, the algorithm confirmed the fault to be in the busbar protection zone. The algorithm took 6.25 ms (i.e. 9/1440 ms) to make the final decision. The study was repeated in which ct of relay R_3 saturated. The positive-sequence and negative-sequence trip counters of relay R_3 reached the threshold in 8 samples. The trip-counters of the other relays took the same number of samples as in the previous case. The algorithm took 6.25 ms to make the decision in this case as well.

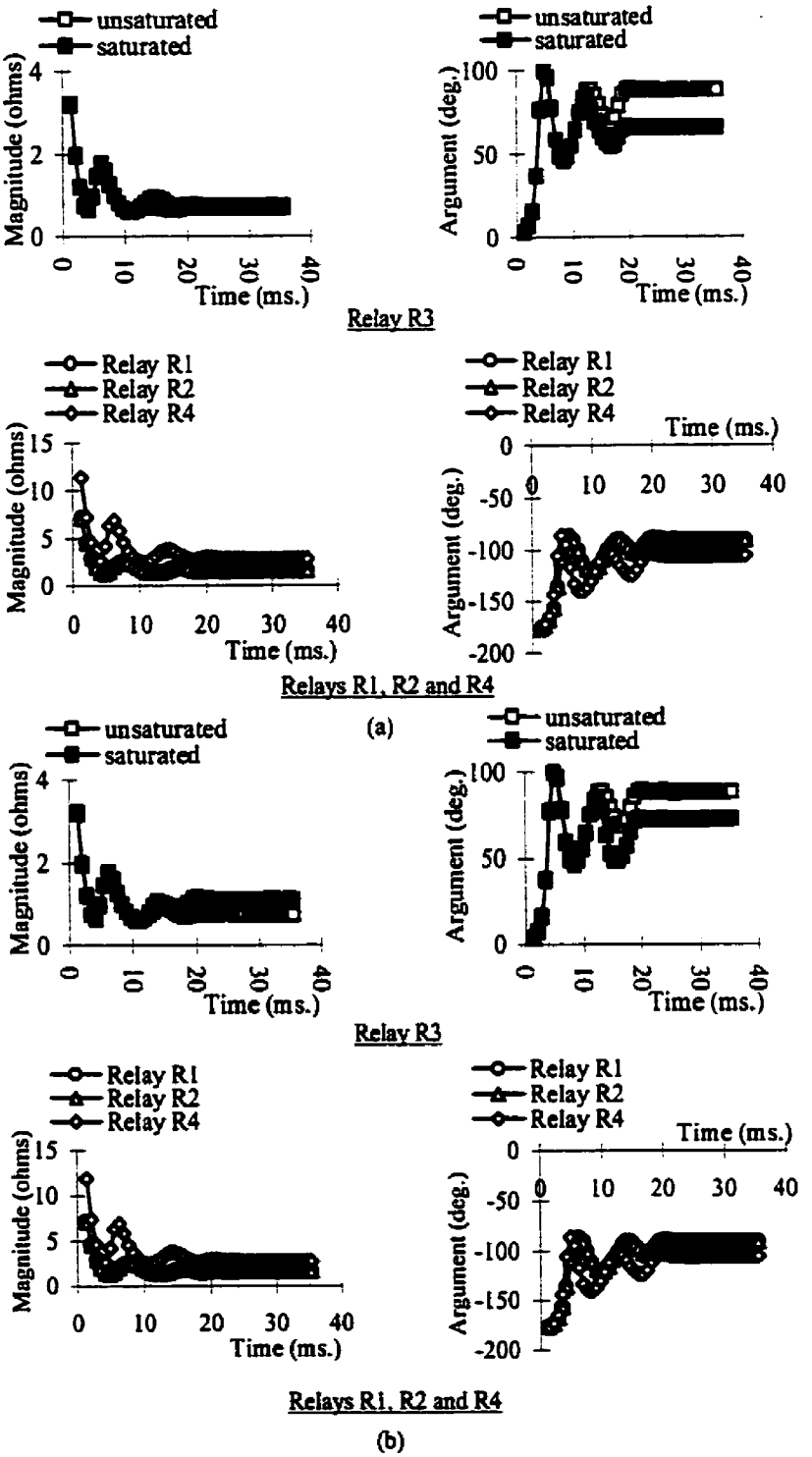


Figure 5.12 (a). Plots of the arguments and magnitudes of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase C-ground fault outside the busbar protection zone of the substation of Figure 5.3.

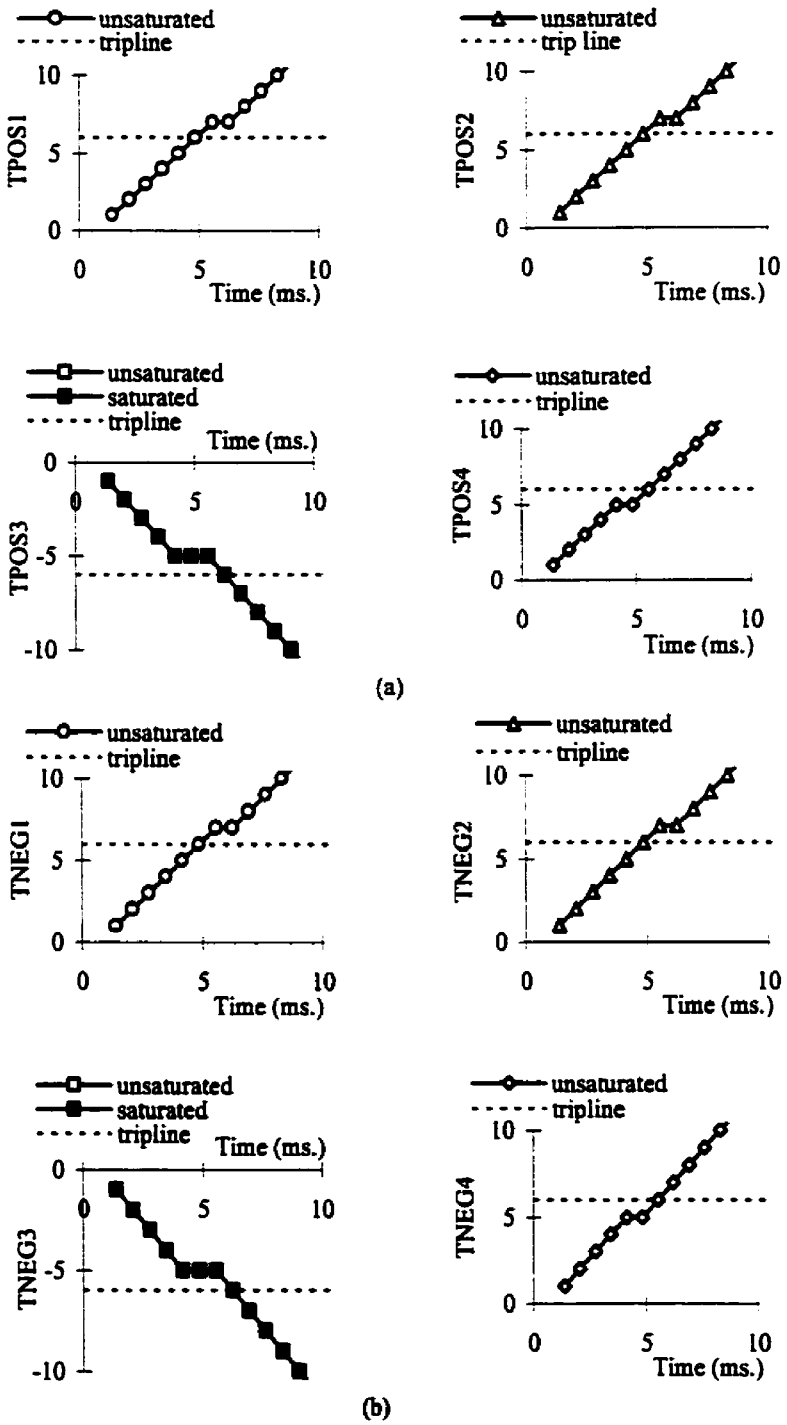


Figure 5.12 (b). Profile of the positive-sequence, and negative-sequence trip-counters for a Phase C-ground fault at location 2 of the substation shown in Figure 5.3.

A Phase A-to-ground fault outside the protection zone of the busbar was simulated at location 2 in the substation shown in Figure 5.2. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. Figure 5.13 shows the profile of the magnitudes and arguments of the sequence-impedances and the trip counters of the relays. In this case, the arguments of the computed positive-sequence and negative-sequence impedances of relays R_1, R_2, R_4, and R_5 lie in the third quadrant. The arguments of the computed positive-sequence and negative-sequence impedances computed by the relay R_3 lie in the first quadrant. This indicates that the fault is outside the protection zone of the busbar. When the cts did not saturate, the positive-sequence (and negative-sequence) trip counters of the relays R_1, R_2, R_3, R_4, and R_5 reached the threshold in 7 (7), 11 (11), 7 (7), 7 (9) and 12 (12) samples respectively. At the 13th sampling instant, the trip-logic confirmed that the fault was outside the protection zone of the busbar. It took the algorithm 9.03 ms (i.e. 13/1440 ms) to make the final decision. When the ct of relay R_3 saturated, the positive-sequence (and negative-sequence) trip-counters reached the threshold in 7 (7) samples respectively. Since the cts located at relays R_1, R_2, R_4 and R_5 did not saturate, their sequence trip counters took the same time as before. The algorithm took 9.03 ms to make a final decision in this case as well.

5.4.2.2. Phase-to-phase faults

A Phase A-Phase B fault was simulated on the 345 kV side of the power transformer T1 (location 2) of the power system shown in Figure 5.7. The fault was applied at 0.3 seconds. Figure 5.14 shows the performance of the algorithm. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. The computed sequence

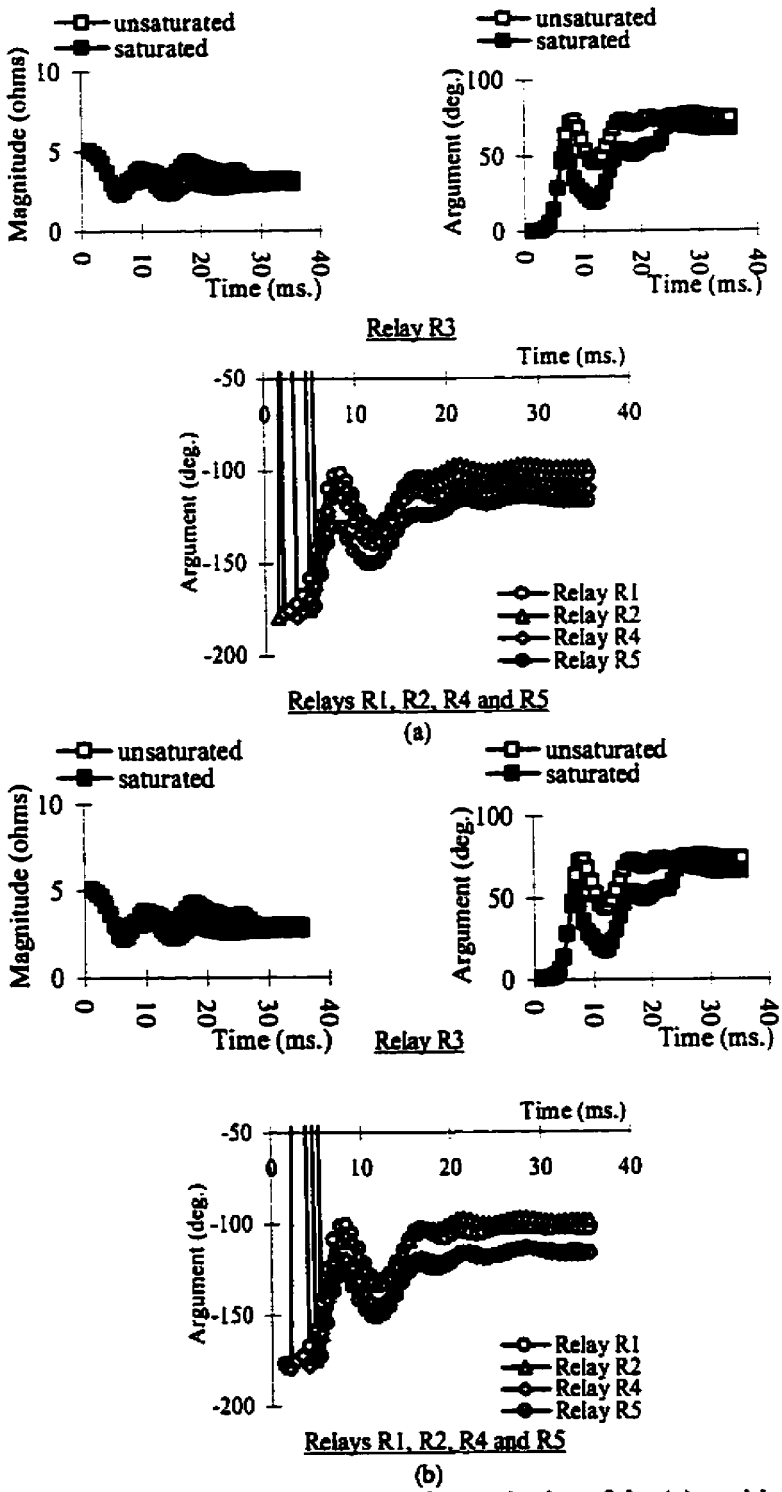


Figure 5.13 (a). Plots of the arguments and magnitudes of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase A-ground fault at location 2 of the system containing BRADA substation.

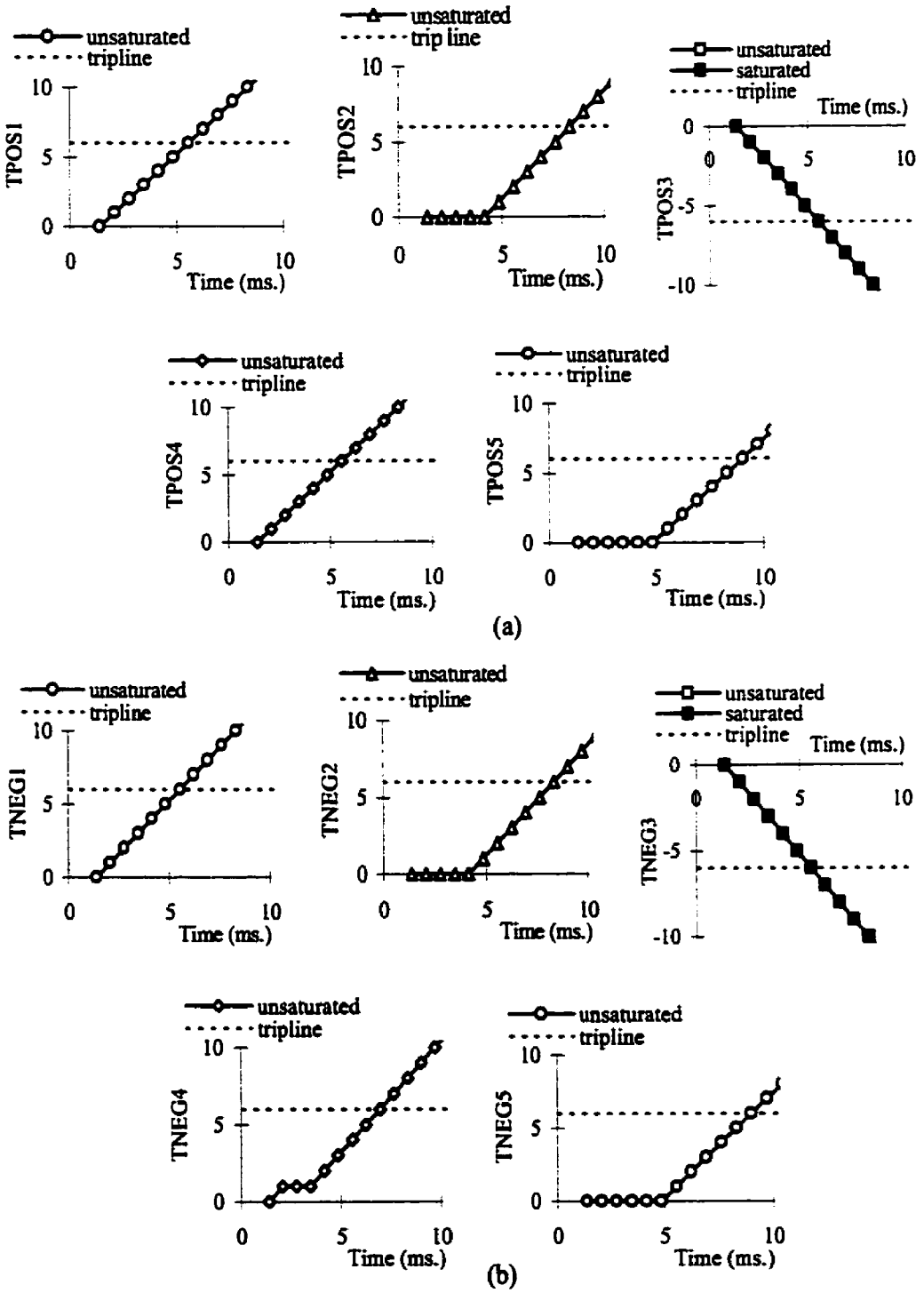


Figure 5.13 (b). Profiles of the (a) positive-sequence and (b) negative-sequence trip-counters for a Phase A-ground fault at location 2 of the system containing BRADA substation.

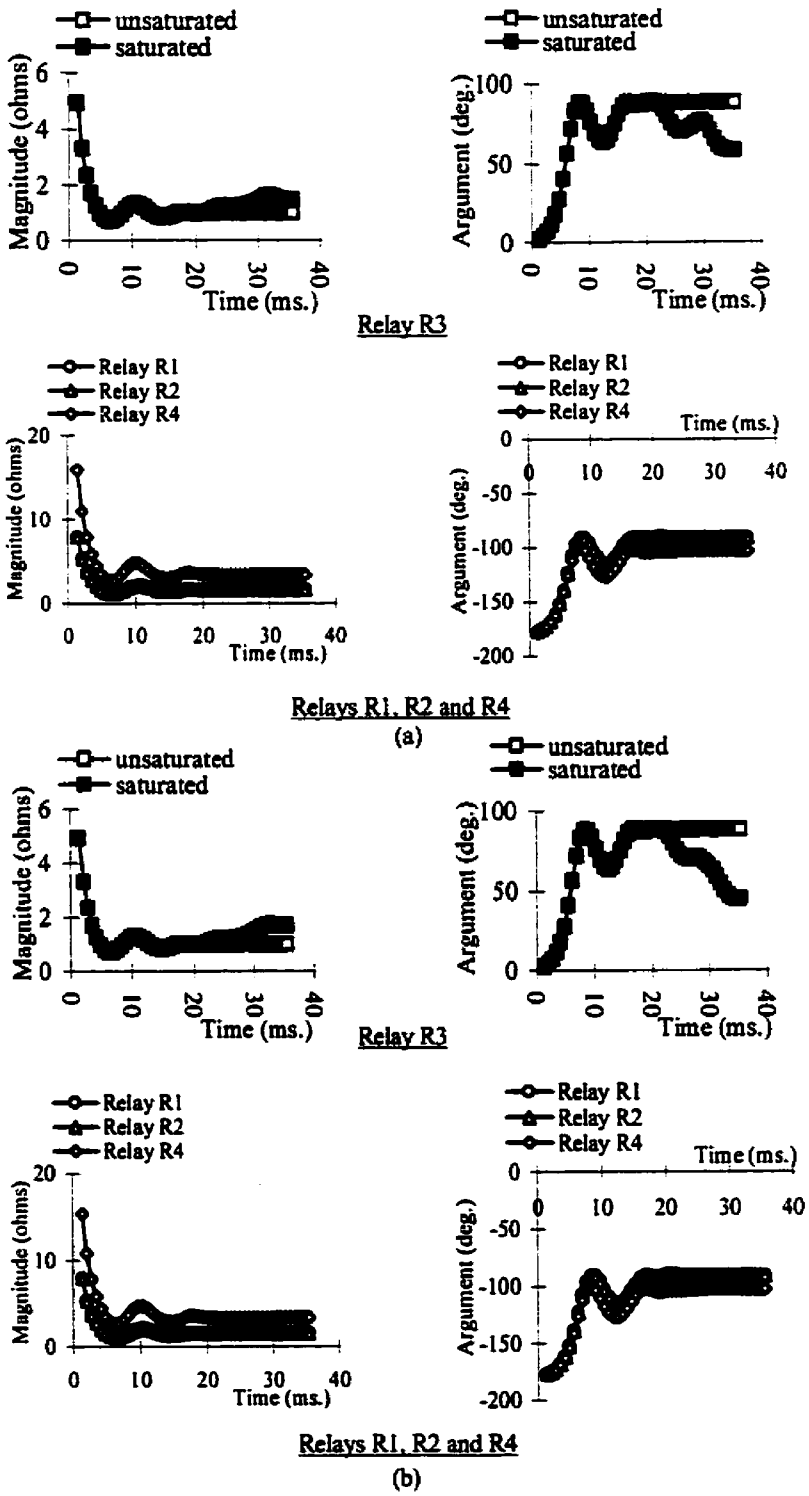


Figure 5.14 (a). Plots of the arguments and magnitudes of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase A-Phase B fault at location 2 of the system shown in Figure 5.7.

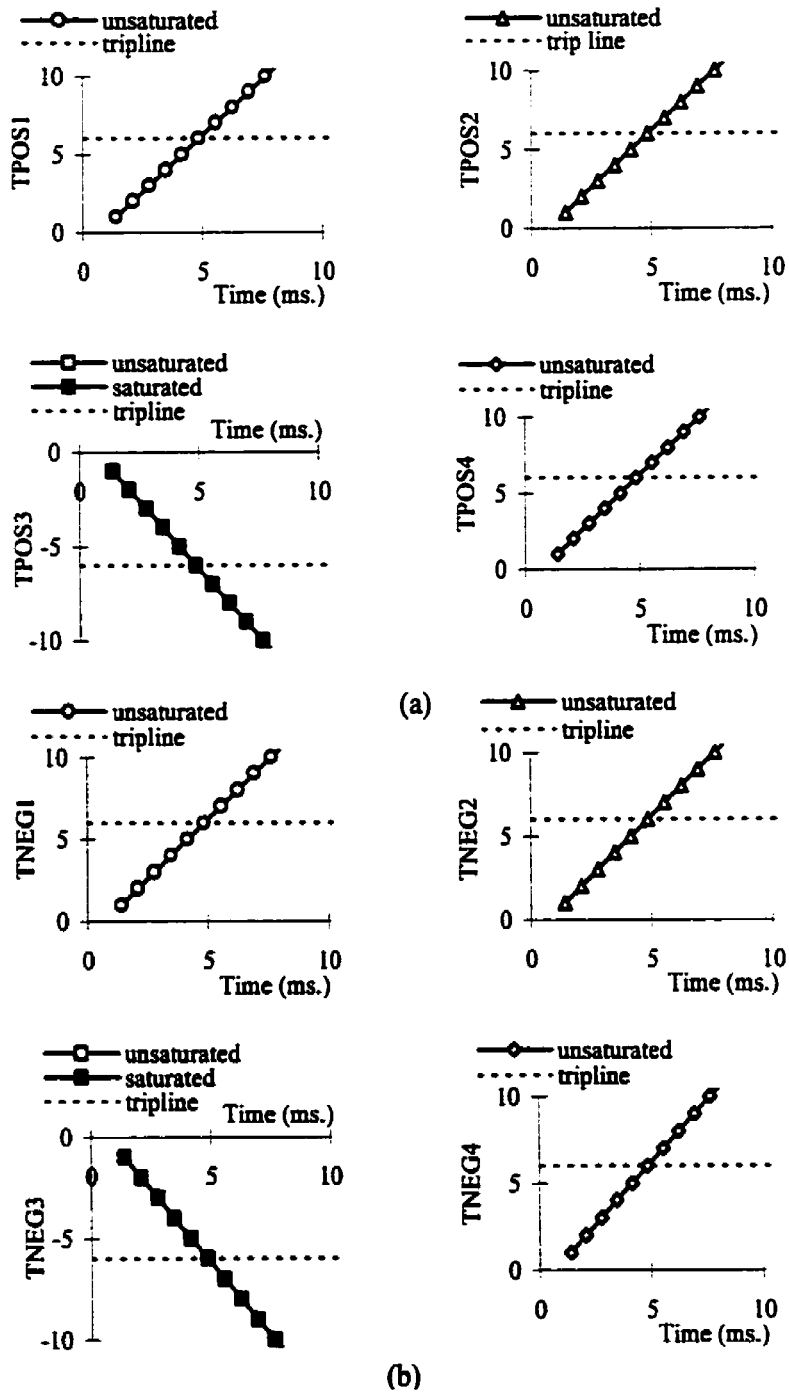


Figure 5.14 (b). Profile of the positive- and negative-sequence trip-counters for a Phase A-Phase B fault at location 2 of the system shown in Figure 5.7.

impedances and the profile of the positive-sequence and negative-sequence trip counters are shown in Figures 5.14 (a) and (b) respectively.

This figure shows that the positive- and negative-sequence impedances computed by relays R_1, R_2 and R_4 were in the third quadrant, whereas the sequence-impedances computed by the relay R_3 lie in the first quadrant. The trip counters associated with the positive-sequence and negative-sequence impedances computed by the relays R_1, R_2 and R_4 incremented whereas the trip counters of relay R_3 decremented. The trip counters reached their thresholds and it was decided that the fault was outside the protection zone of the busbar. The positive-sequence (and negative-sequence) trip counters for the relays R_1 to R_4 reached the threshold in 6 (6) samples respectively. At the 7th sampling instant, the algorithm confirmed that the fault was outside the busbar zone. The algorithm took 4.86 ms (i.e. 7/1440 ms) to make the final decision. The study was repeated in which the ct of relay R_3 saturated. The positive-sequence and negative-sequence trip counters of relays R_1 to R_4 reached the threshold in 6 samples. The algorithm took 4.86 ms to make the decision in this case as well.

A Phase A-Phase B fault outside the bus protection zone was simulated at location 9 in the substation shown in Figure 5.2. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. Figure 5.15 shows the profile of the magnitudes and arguments of the sequence-impedances and the trip counters of the relays. In this case, the arguments of the positive-sequence and negative-sequence impedances computed by relays R_1, R_2, R_4, and R_5 lie in the third quadrant. The arguments of the positive-sequence and negative-sequence impedances computed by relay R_3 lie in the first quadrant. This indicates that the fault is outside the protection zone of the busbar. When the cts did not saturate, the positive-sequence (and negative-sequence) trip counters of the relays R_1, R_2, R_3, R_4, and R_5 reached the threshold in 6 (6), 11 (10), 6 (6), 7 (9) and 12 (11) samples respectively. At the 12th sampling instant, the trip-logic confirmed that the fault was

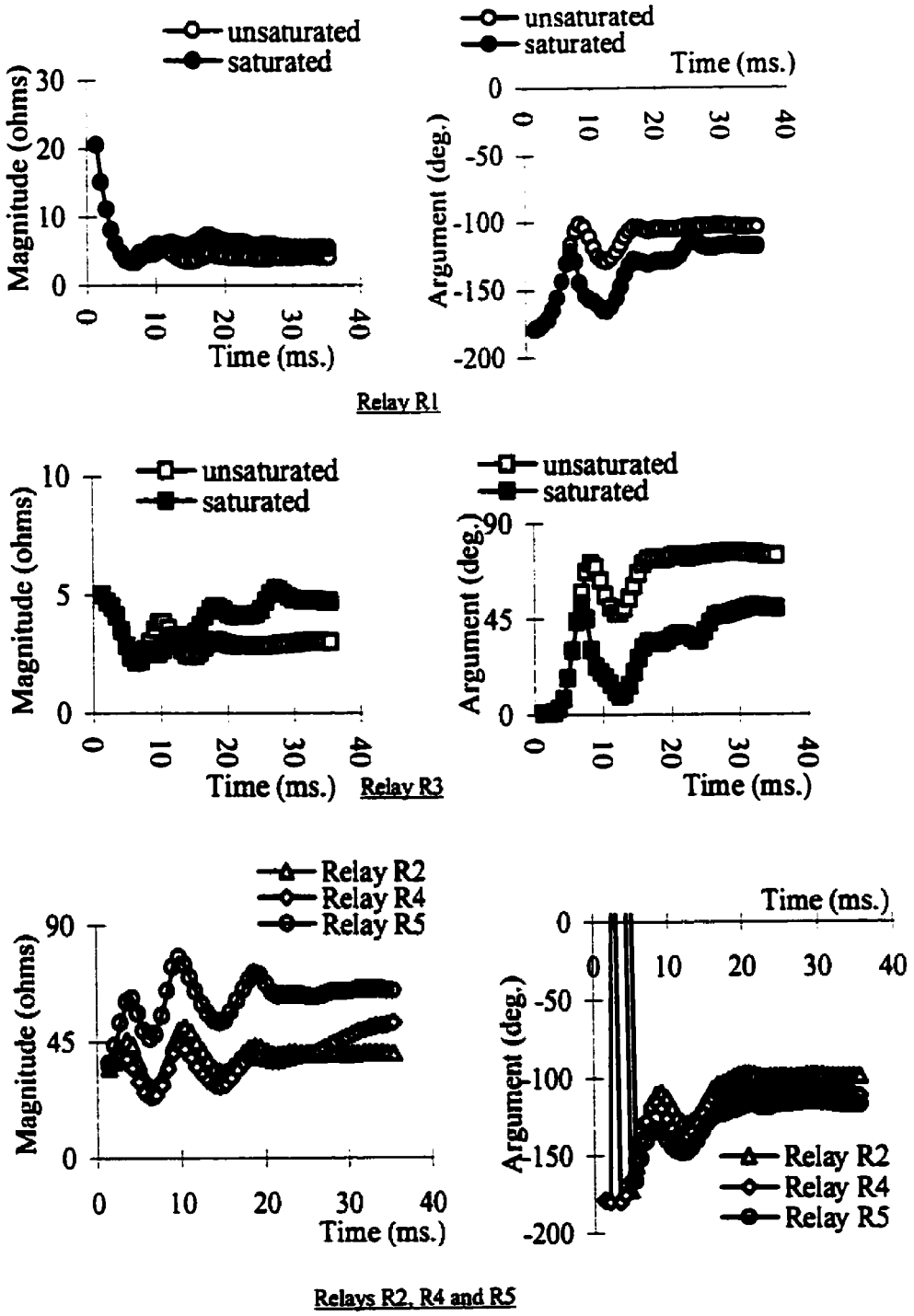


Figure 5.15 (a). Plots of the arguments and magnitudes of the positive-sequence impedances computed by the relays for a Phase A-Phase B fault outside the busbar protection zone (location 9) of the system containing BRADA substation.

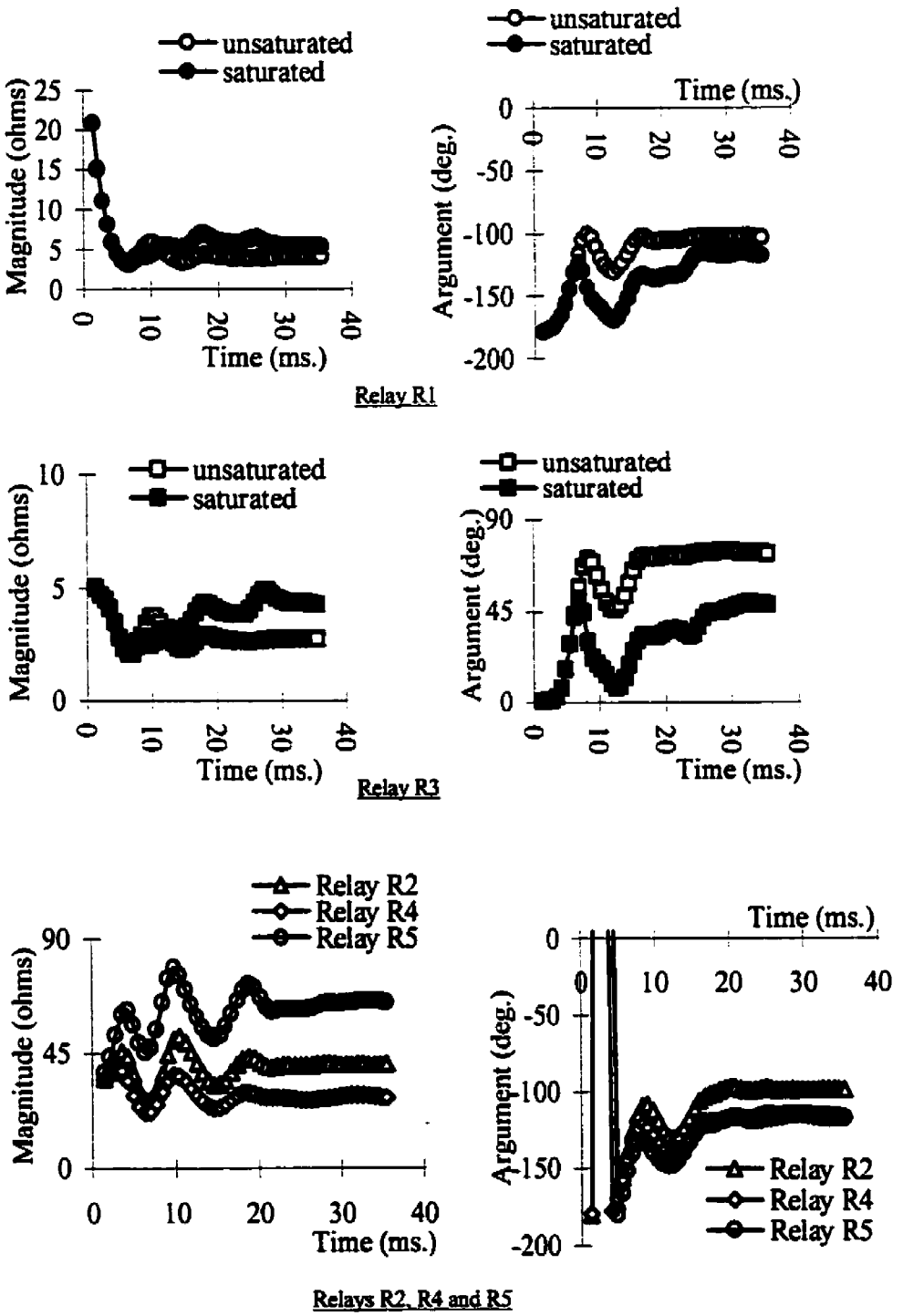


Figure 5.15 (b). Plots of the arguments and magnitudes of the negative-sequence impedances computed by the relays for a Phase A-Phase B fault outside the busbar protection zone (location 9) of the system containing BRADA substation.

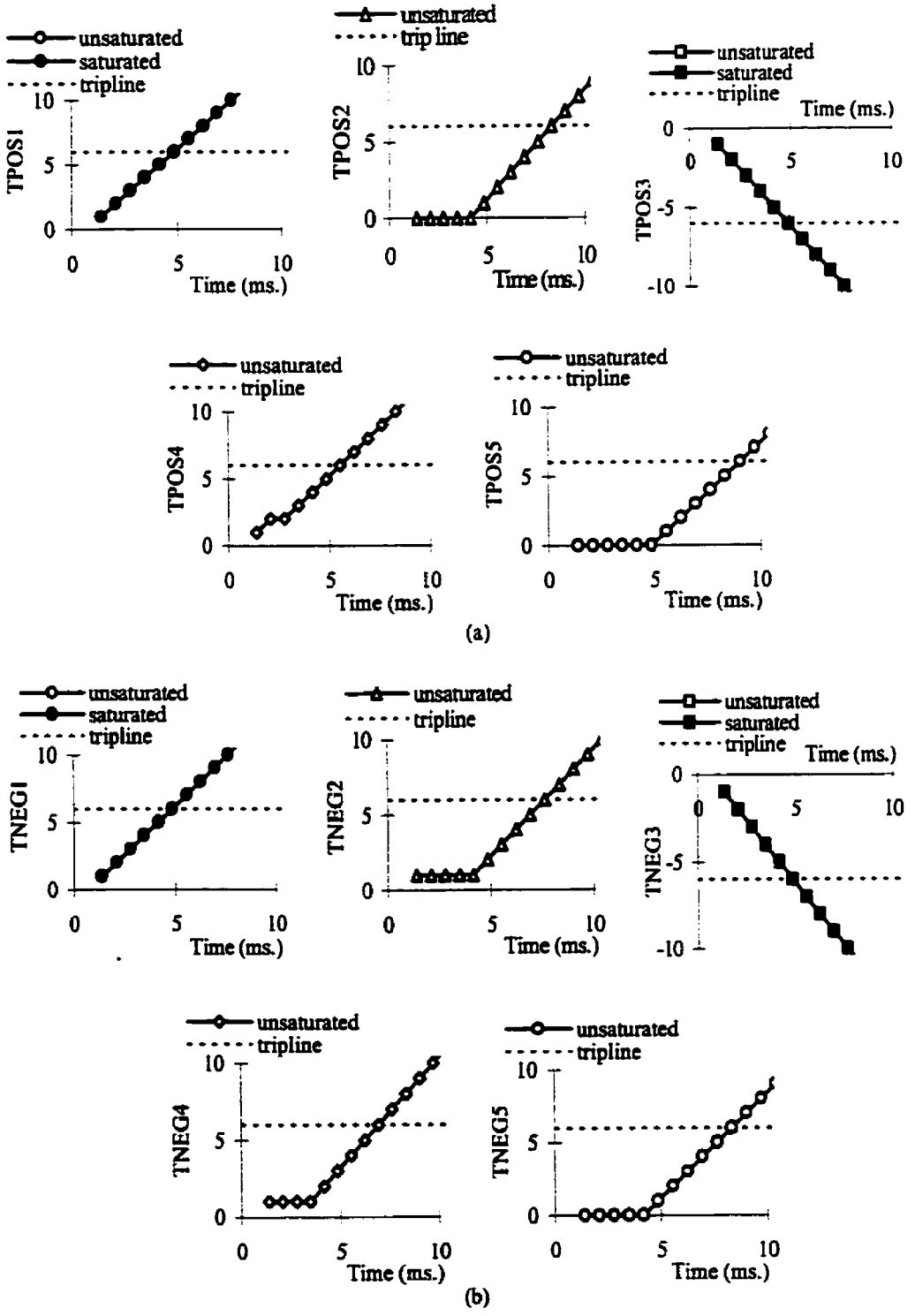


Figure 5.15 (c). Profiles of the (a) positive-sequence and (b) negative-sequence trip-counters for a Phase A-Phase B fault at location 9 of the system containing BRADA substation.

outside the protection zone of the busbar. It took the algorithm 8.33 ms (i.e. 12/1440 ms) to make the final decision. When the ct of relays R_1 and R_3 saturated, the positive- (and negative-) sequence trip-counters reached the threshold in 6 (6) samples. Since the cts located at relays R_2, R_4 and R_5 did not saturate, their sequence trip counters took the same time as before. The algorithm took 8.33 ms to make a final decision in this case as well.

5.4.2.3. Three-phase faults

A three phase fault was simulated at location 3 of the power system of Figure 5.3. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. Figure 5.16 shows the profile of the arguments and magnitudes of the positive-sequence impedances computed by the relays. This figure shows that the arguments of the sequence impedances computed by relays R_2, R_3, and R_4 lie in the third quadrant. The arguments of the sequence impedance computed by the relay R_1 lie in the first quadrant. This means that the fault is outside the busbar protection zone. The positive-sequence trip counters for the relays R_1 to R_4 reached the threshold in 6 samples each. At the 7th sampling instant, the algorithm confirmed that the fault was outside the busbar zone. The algorithm took 4.86 ms (i.e. 7/1440 ms) to make the final decision. The study was repeated in which cts of relays 1 and 2 saturated. The positive-sequence trip counters of relays R_1 to R_4 reached the threshold in 6 samples each. The algorithm took 4.86 ms to make the decision in this case. As no negative-sequence voltages and currents were experienced during a three-phase fault, no conclusion was generated by those components.

A three phase fault outside the bus protection zone was simulated at location 13 in the substation shown in Figure 5.2. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-

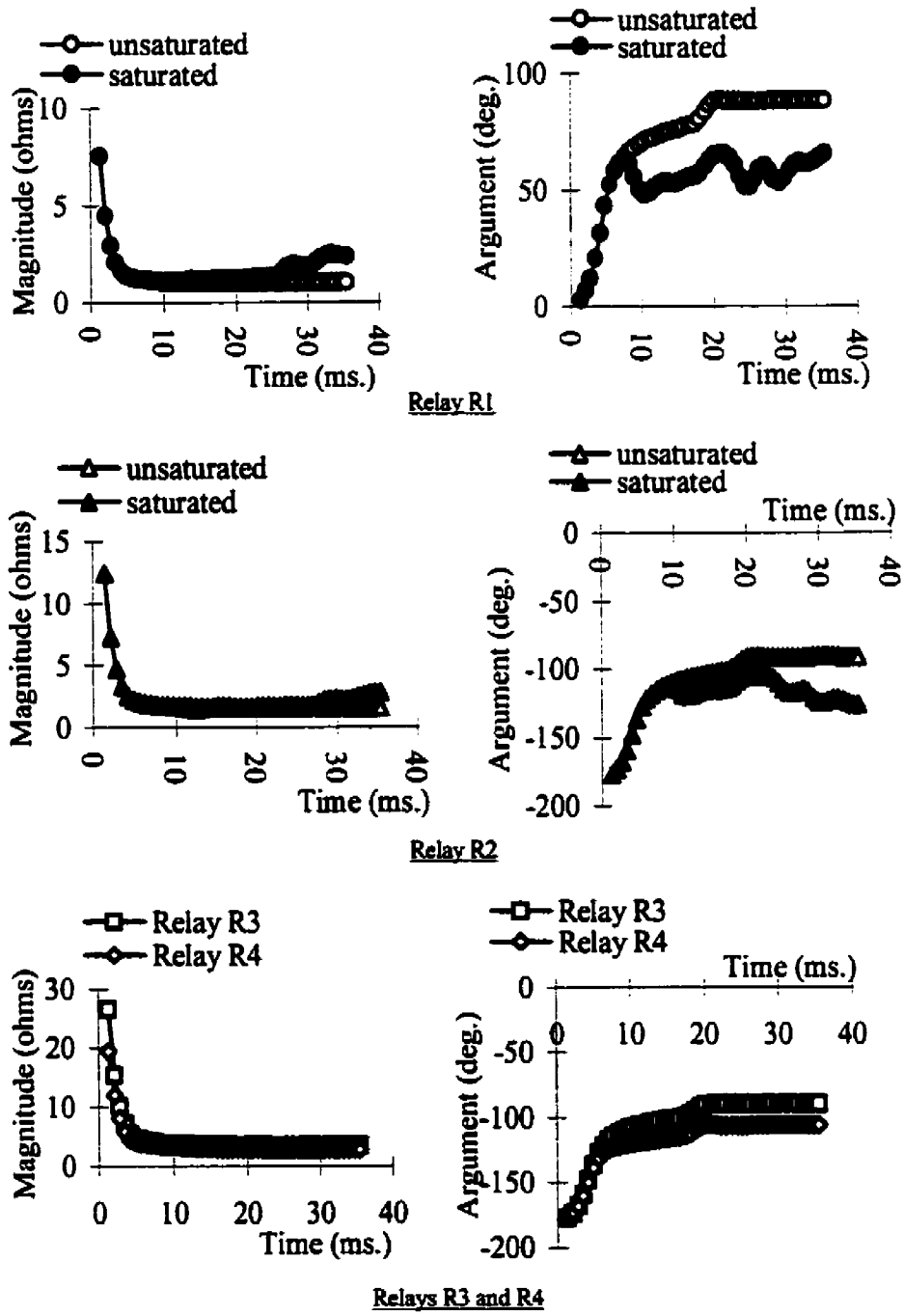


Figure 5.16 (a). Plots of the arguments and magnitudes of the positive-sequence impedances computed by the relays for a three phase fault at location 3 of the system shown in Figure 5.3.

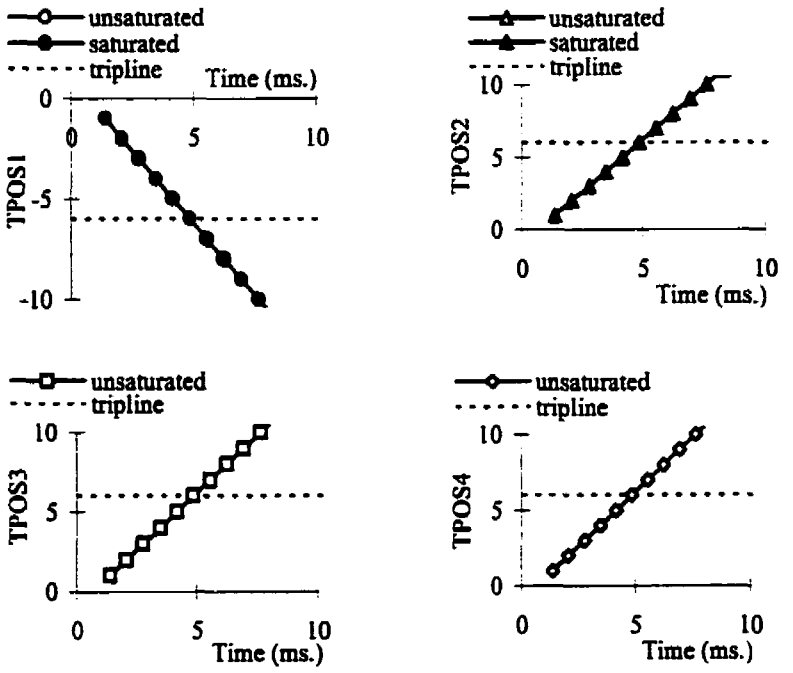


Figure 5.16 (b). Profile of the positive-sequence trip-counters for a three phase fault at location 3 of the substation of the system shown in Figure 5.3.

impedances were computed. Figure 5.17 shows the profile of the magnitudes and arguments of the sequence-impedances and the trip counters of the relays. In this case, the arguments of the positive-sequence impedances computed by relays R_1, R_2, R_3, and R_5 lie in the third quadrant. The arguments of the positive-sequence impedances computed by the relay R_4 lie in the first quadrant. This indicates that the fault is outside the protection zone of the busbar. When the cts did not saturate, the positive-sequence trip counters of the relays R_1, R_2, R_3, R_4, and R_5 reached the threshold in 6, 10, 8, 6 and 11 samples respectively. At the 12th sampling instant, the trip-logic confirmed that the fault was outside the protection zone of the busbar. It took the algorithm 8.33 ms (i.e. 12/1440 ms) to make the final decision. When the cts of relays R_1 and R_4 saturated, the positive-sequence trip-counters for these relays reached the threshold in 6 samples. Since the cts located at relays R_2, R_3, and R_5 did not saturate, their sequence trip counters took the same time as before. The algorithm took 8.33 ms to make a final decision in this case as well.

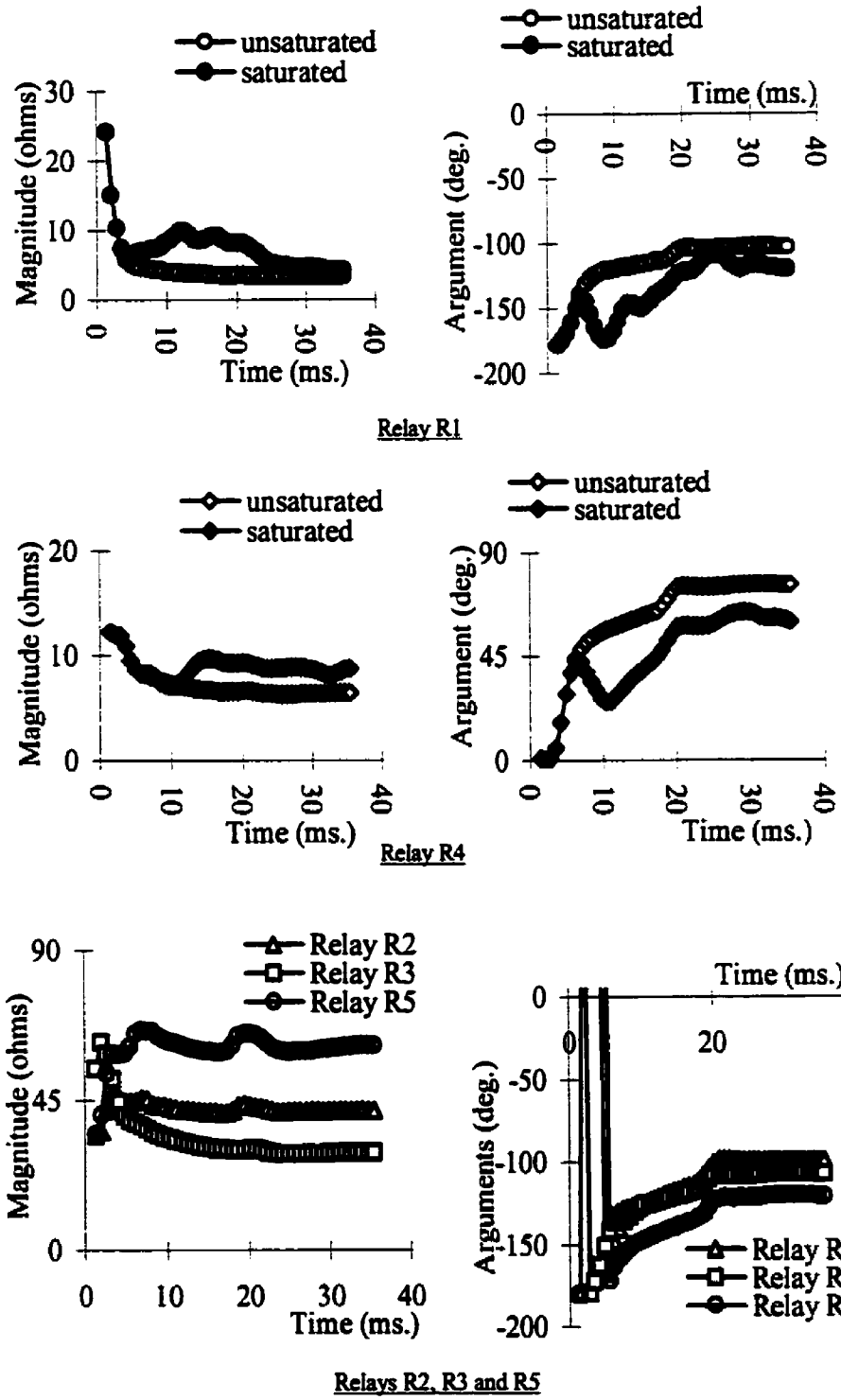


Figure 5.17 (a). Plots of the arguments and magnitudes of the positive-sequence impedances computed by the relays for a three phase fault at location 13 of the system containing BRADA substation.

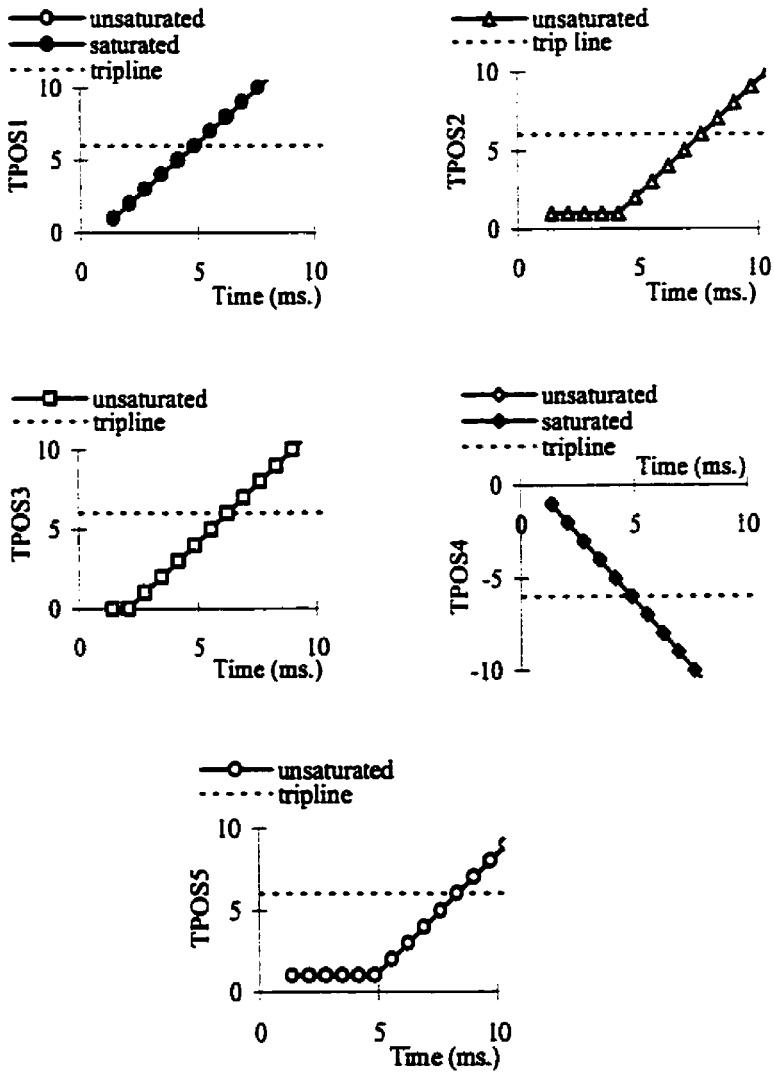


Figure 5.17 (b). Profiles of the positive-sequence trip-counters for a three phase fault at location 13 of the system containing BRADA substation.

5.4.3. Effect of ct ratio-mismatch

The effect of ct ratio-mismatch on the performance of the proposed technique was also investigated. Different levels of ratio-mismatch, between the cts used in the protection scheme, were simulated. Some results illustrating the impact of ratio-mismatch are presented in the following sections.

5.4.3.1. Internal faults

A Phase A to ground fault in the bus-protection zone (location 1 in the substation shown in Figure 5.1) was simulated. Nominal and off-nominal ct ratios were used at the relay locations. Table 5.1 shows the values of nominal and off-nominal ct ratios used at the relays.

Table 5.1. Ct ratios used for studying a Phase A to ground fault in the bus-protection zone (location 1 in the substation shown in Figure 5.1).

	Ct ratio		
Relay	Nominal	Off-nominal	
		Case 1	Case 2
R_1	300	250	600
R_2	300	250	600
R_3	300	250	600
R_4	75	50	200

Figure 5.18 shows the performance of the algorithm when three ct ratios were used. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. The magnitudes and arguments of positive-sequence and negative-sequence impedances computed by the relays are shown in Figures 5.18 (a) and 5.18 (b) respectively. These figures show that the arguments of the sequence-impedances computed by all the relays lie in the third quadrant. This led to the decision that the fault occurred in the protection zone of the busbar. Use of off-nominal ct ratios manifested in changes in the magnitudes of the impedances but did not change the arguments. Because the proposed technique based its decision on the arguments only, the changes in the magnitudes of the impedances did not have any impact on the decisions. This study illustrates the stability of the proposed technique when ct ratios do not match. The figure shows that the positive-

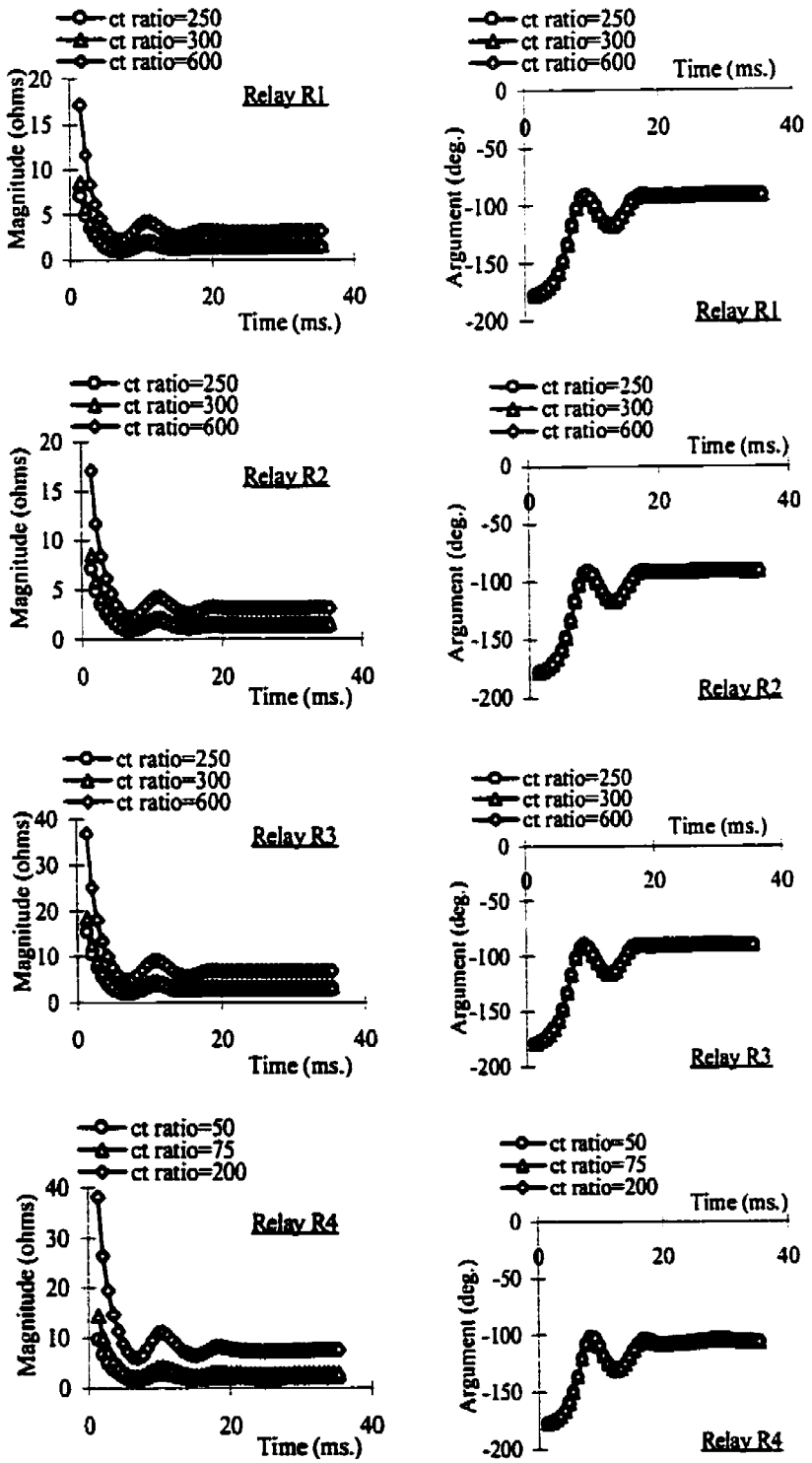


Figure 5.18 (a). Plots of the arguments and magnitudes of the positive-sequence impedances computed by the relays for a Phase A-ground fault in the busbar protection zone of the substation of Figure 5.1.

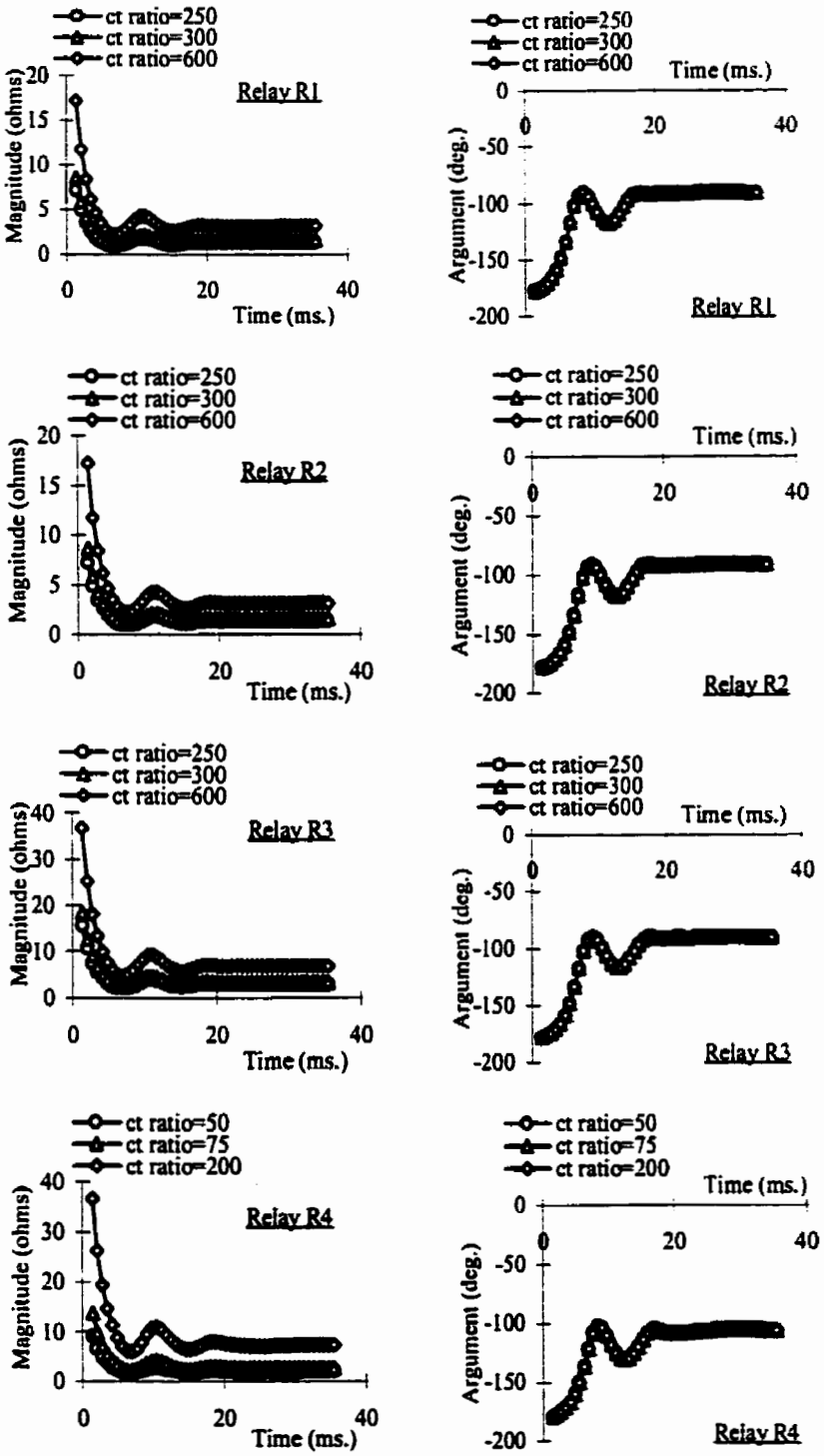


Figure 5.18 (b). Plots of the arguments and magnitudes of the negative-sequence impedances computed by the relays for a Phase A-ground fault in the busbar protection zone of the substation of Figure 5.1.

sequence and negative-sequence trip counters of all relays reached the threshold in 6 samples. The algorithm made the final decision after 4.86 ms (i.e. 7/1440 ms) in all cases.

A Phase C to ground fault in the bus-protection zone (location 5 in the substation shown in Figure 5.2) was simulated. Nominal and off-nominal ct ratios were used at the relay locations. Table 5.2 shows the values of nominal and off-nominal ct ratios used at the relays.

Table 5.2. Ct ratios used for studying a Phase C to ground fault in the bus-protection zone (location 5 in the substation shown in Figure 5.2).

	Ct ratio		
Relay	Nominal	Off-nominal	
		Case 1	Case 2
R_1	80	60	160
R_2	80	60	160
R_3	100	80	200
R_4	80	60	160
R_5	80	60	160

Figure 5.19 shows the performance of the algorithm when ct ratios do not match. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. The magnitudes and arguments of the positive-sequence and negative-sequence impedances computed for each ct ratio are shown in Figure 5.19 (a) and Figure 5.19 (b) respectively. These figures show that the arguments of the sequence-impedances computed by all the relays lie in the third quadrant. This led to the decision that the fault was in the protection zone of the busbar. Use of different ct ratios manifested in changes in the magnitudes of the impedances but did not change in the argument. Because the proposed technique based its decision on the arguments only, the changes in the magnitudes of the impedances did not have any impact on the decisions. This study illustrates the stability of the

proposed technique when ct ratios do not match. The figure shows that the positive-sequence and negative-sequence trip counters of the relays R_1, R_2, R_3, R_4 and R_5 reached the threshold in 6 (8), 9 (9), 8 (8), 8 (9) and 12 (12) samples respectively. The algorithm made the final decision in 9.03 ms (i.e. 13/1440 ms) in all cases.

5.4.3.2. External faults

A Phase B to ground fault outside the bus-protection zone (location 5 in the substation shown in Figure 5.1) was simulated. Nominal and off-nominal ct ratios were used at the relay locations. Table 5.3 shows the values of nominal and off-nominal ct ratios used at the relays.

Table 5.3. Ct ratios used for studying a Phase B to ground fault outside the bus-protection zone (location 5 in the substation shown in Figure 5.1).

	Ct ratio		
Relay	Nominal	Off-nominal	
		Case 1	Case 2
R_1	300	200	250
R_2	300	250	400
R_3	300	250	600
R_4	75	50	200

Figure 5.20 shows the performance of the algorithm when nominal and off-nominal ct ratios were used. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. The magnitudes and arguments of positive-sequence and negative-sequence impedances computed by the relays are shown in Figures 5.20 (a) and 5.20 (b) respectively. These figures show that the sequence-impedances computed by the relays R_1, R_2, R_4, and R_5 lie in the third quadrant. The sequence-impedances computed by the relay R_3 lie in the first quadrant. This led to the decision that the fault was outside the protection zone of the busbar. Use of off-nominal ct ratios manifested in changes in the

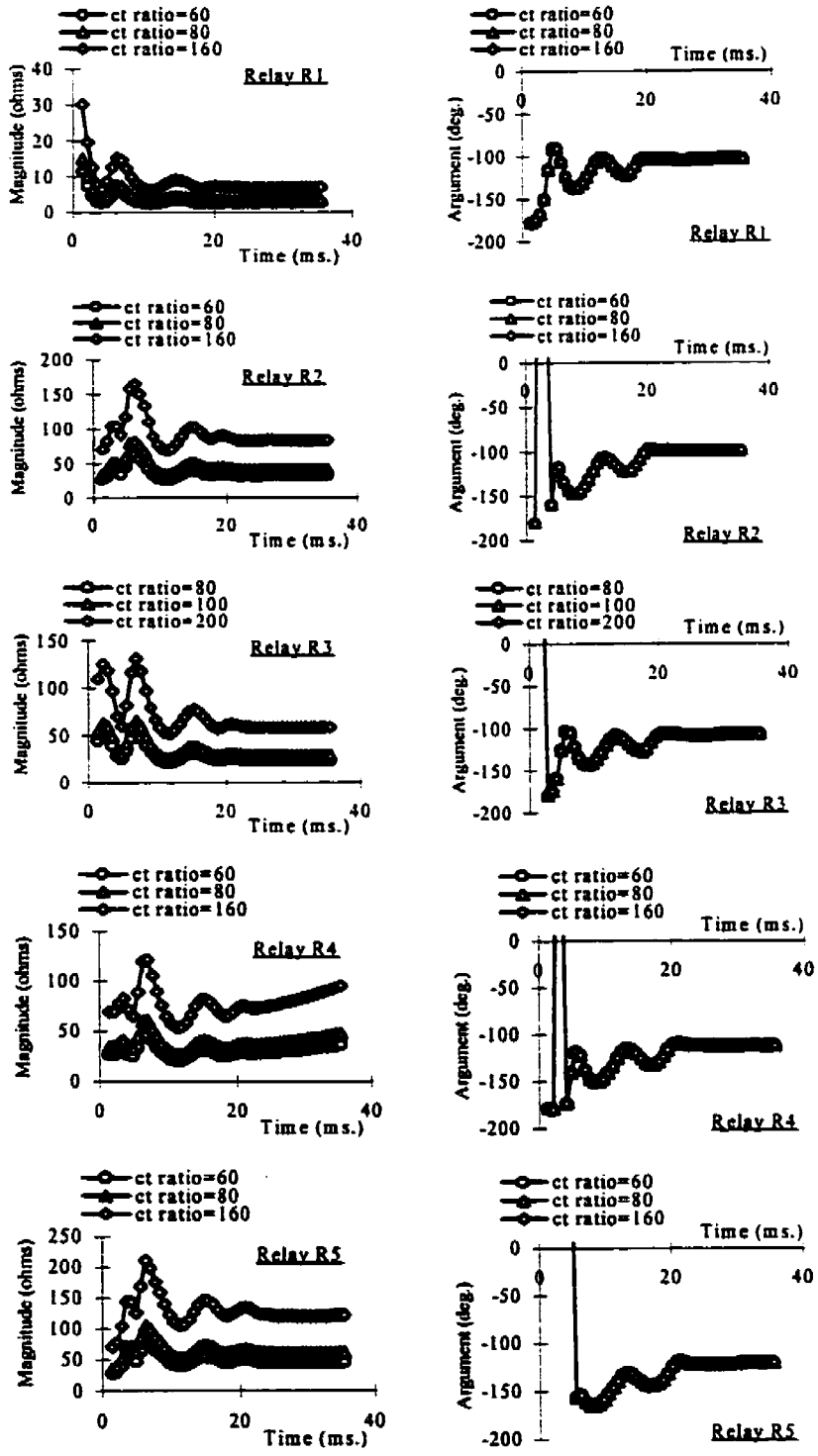


Figure 5.19 (a). Plots of the arguments and magnitudes of the positive-sequence impedances computed by the relays for a Phase C-ground fault in the busbar protection zone (location 5) of the BRADA substation.

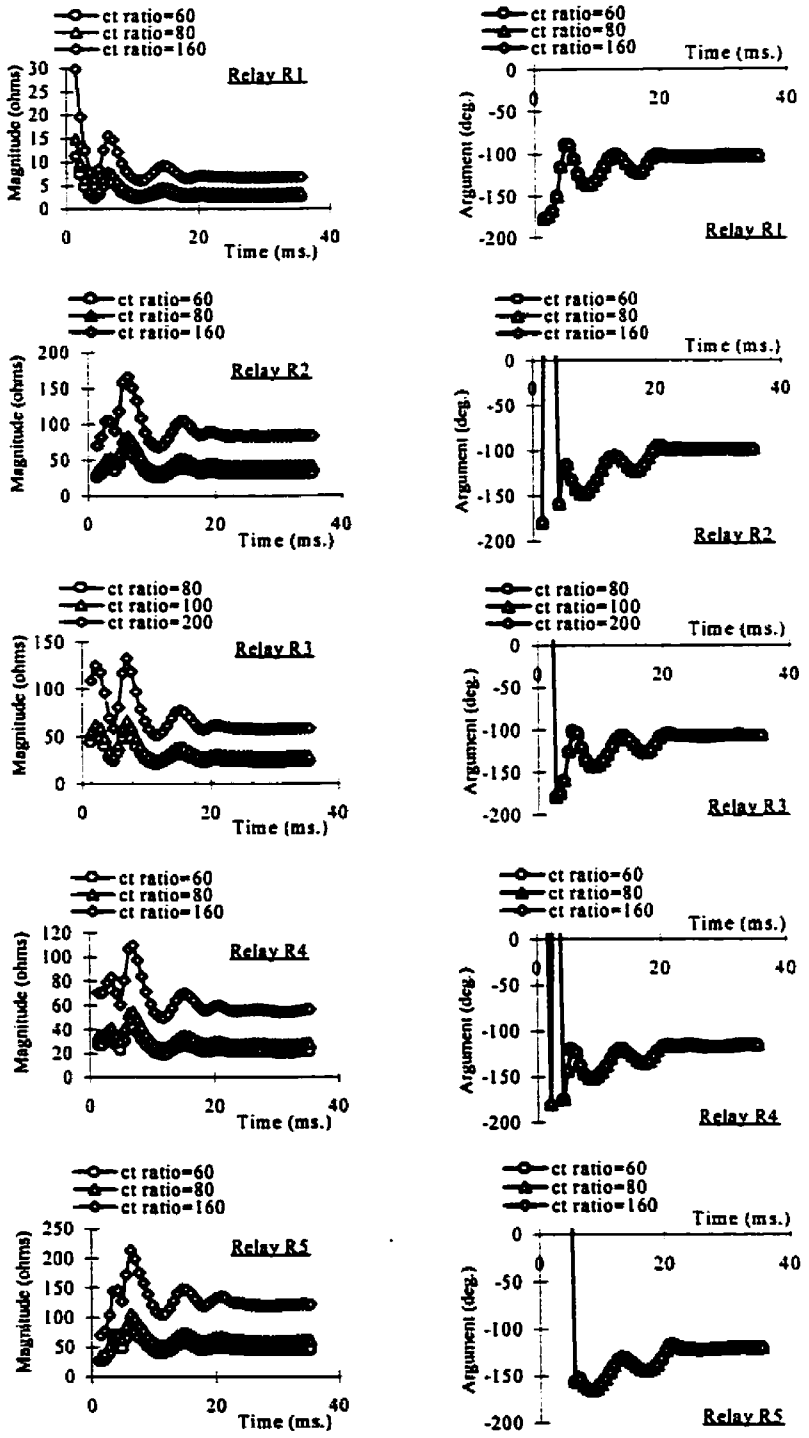


Figure 5.19 (b). Plots of the arguments and magnitudes of the negative-sequence impedances computed by the relays for a Phase C-ground fault in the busbar protection zone (location 5) of the BRADA substation.

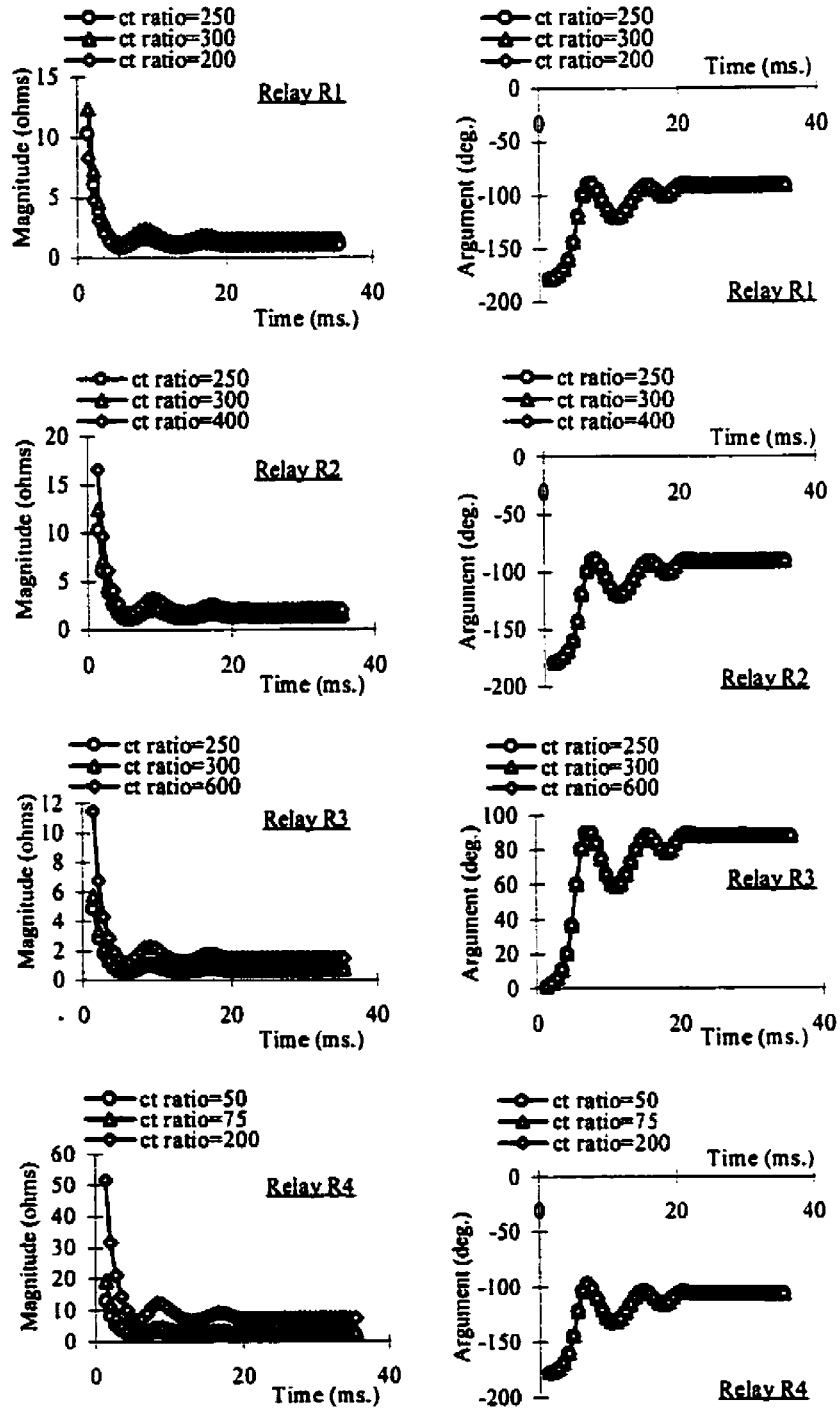


Figure 5.20 (a). Plots of the arguments and magnitudes of the positive-sequence impedances computed by the relays for a Phase B-ground fault outside the busbar protection zone (location 5) of the system shown in Figure 5.1.

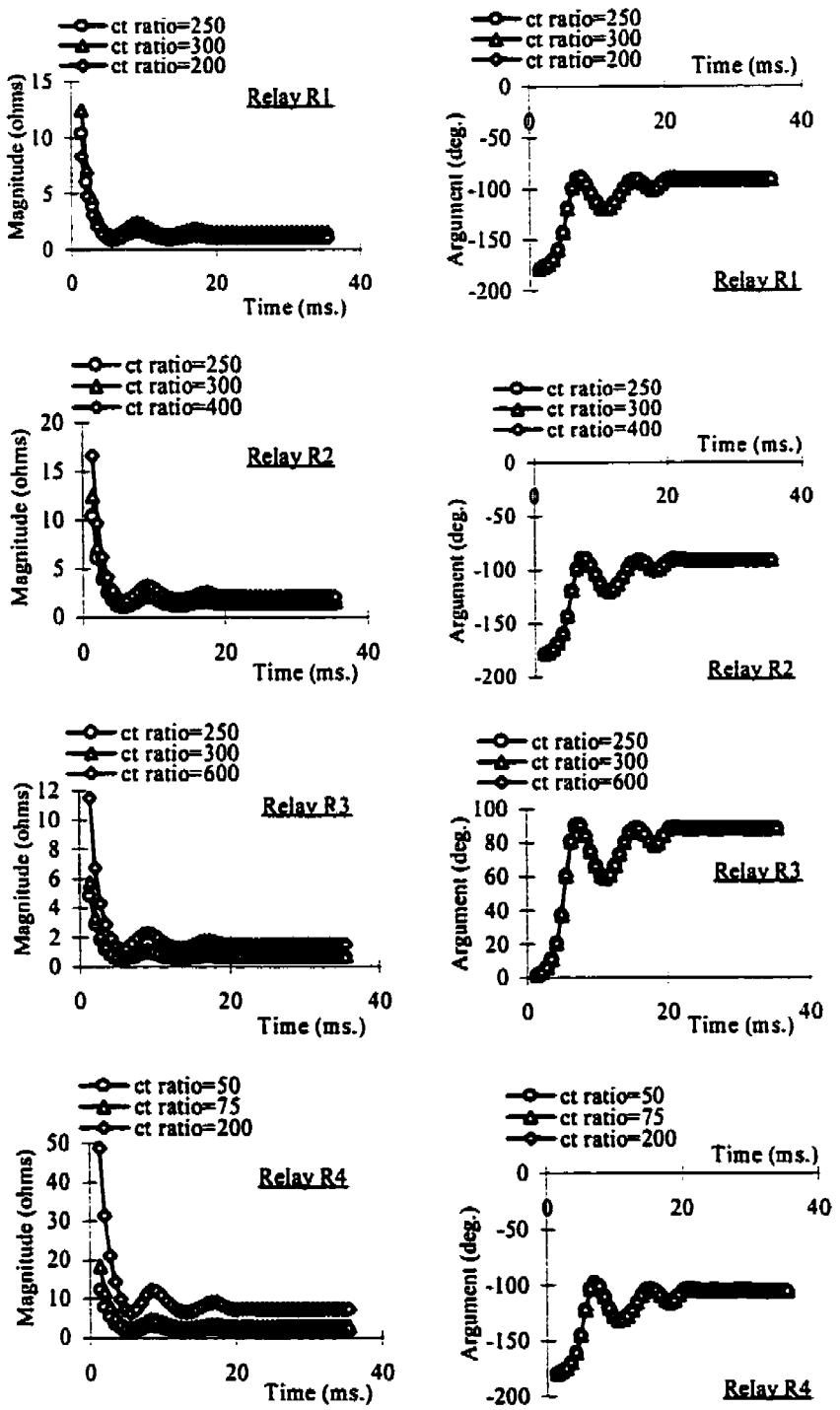


Figure 5.20 (b). Plots of the arguments and magnitudes of the negative-sequence impedances computed by the relays for a Phase B-ground fault outside the busbar protection zone (location 5) of the system shown in Figure 5.1.

magnitudes of the impedances but did not change the arguments. Because the proposed technique based its decision on the arguments only, the changes in the magnitudes of the impedances did not have any impact on the decisions. This study illustrates the stability of the proposed technique when ct ratios do not match. The figure shows that the positive-sequence and negative-sequence trip counters of all relays reached the threshold in 6 samples. The algorithm made the final decision in 4.86 ms (i.e. 7/1440 ms) in all cases.

A Phase A to ground fault outside the bus-protection zone (location 13 in the system shown in Figure 5.2) was simulated. Nominal and off-nominal ct ratios were used at the relay locations. Table 5.4 shows the values of nominal and off-nominal ct ratios used at the relays.

Table 5.4. Ct ratios used for studying a Phase A to ground fault outside the bus-protection zone (location 13 in the substation shown in Figure 5.2).

	Ct ratio		
Relay	Nominal	Off-nominal	
		Case 1	Case 2
R_1	80	160	400
R_2	80	160	500
R_3	100	200	600
R_4	80	160	300
R_5	80	60	160

Figure 5.21 shows the performance of the algorithm when nominal and off-nominal ct ratios were used. The inception of the fault was detected when the second set of samples were acquired. The phasors of voltages and currents were calculated using the second set and the subsequent samples. From these phasors, phasors of incremental sequence voltages and currents were computed. Finally, the sequence-impedances were computed. The magnitudes and arguments of positive-sequence and negative-sequence impedances computed for each ct ratio are shown in Figures 5.21 (a) and 5.21 (b) respectively. These figures show that the arguments of the sequence-impedances computed by the relays R_1, R_2, R_3, and R_5 lie in the third quadrant. The arguments of the

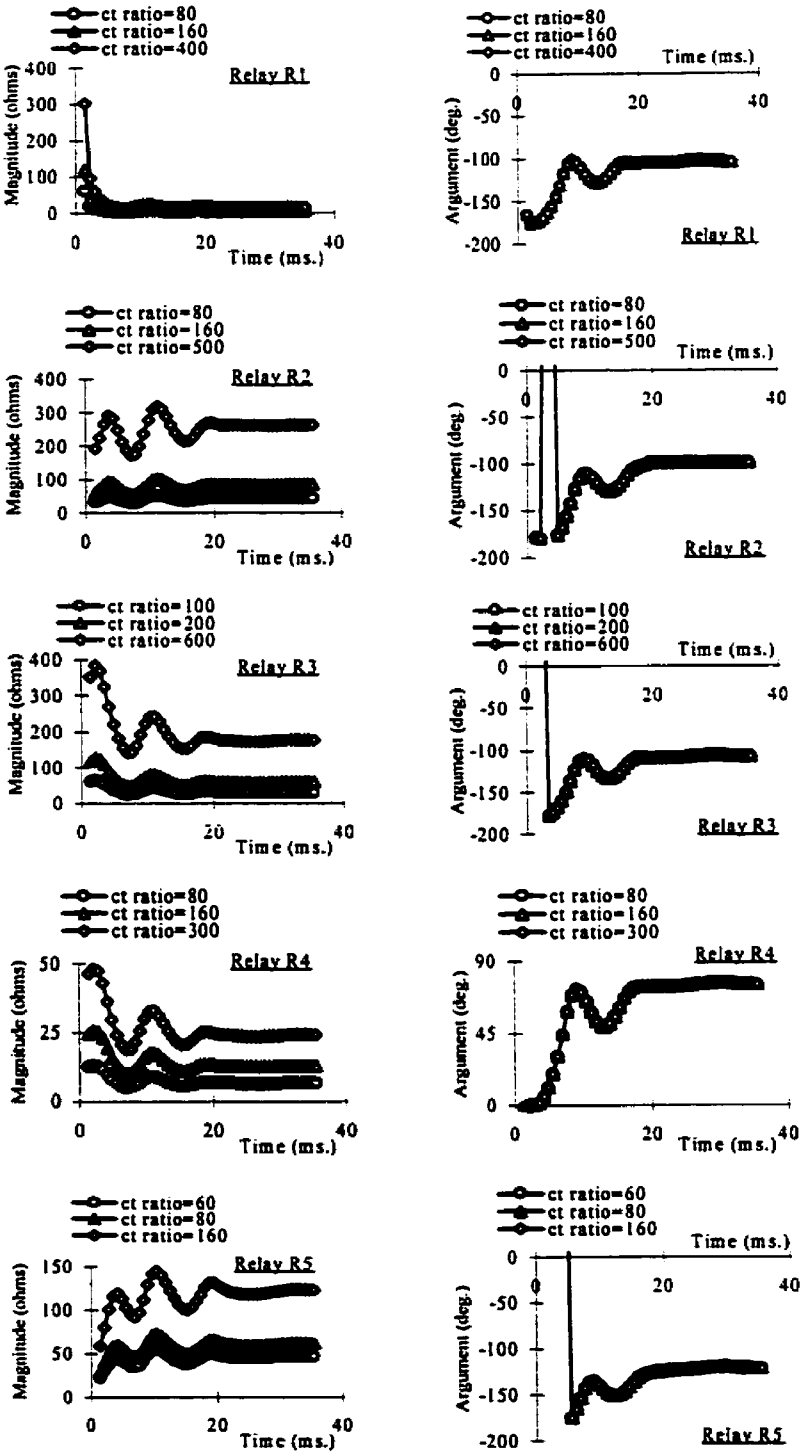


Figure 5.21 (a). Plots of the arguments and magnitudes of the positive-sequence impedances computed by the relays for a Phase A-ground fault at location 13 of the system containing the BRADA substation.

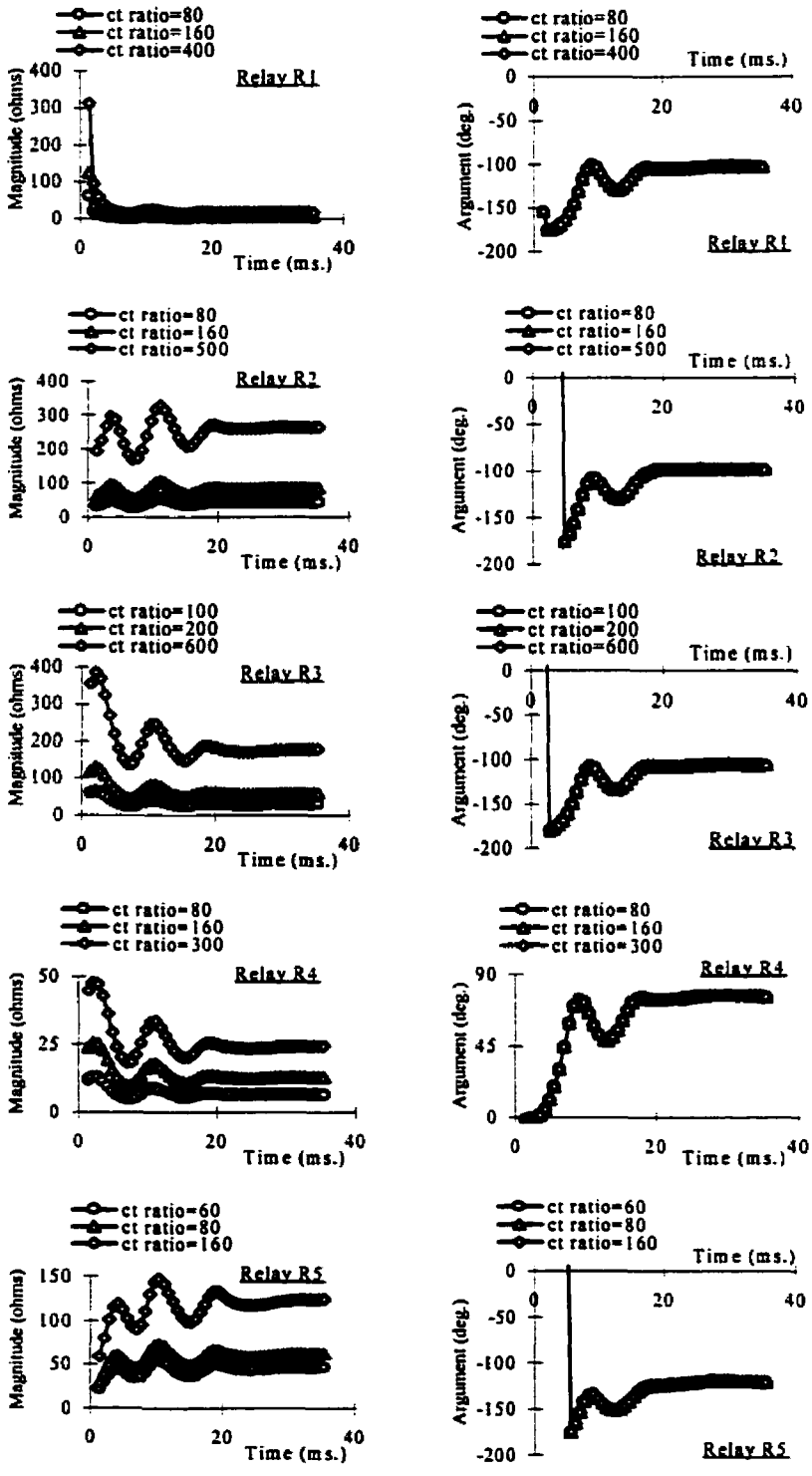


Figure 5.21 (b). Plots of the arguments and magnitudes of the negative-sequence impedances computed by the relays for a Phase A-ground fault at location 13 of the system containing the BRADA substation.

sequence-impedances computed by the relay R_4 lie in the first quadrant. This led to the decision that the fault was outside the protection zone of the busbar. Use of off-nominal ct ratios manifested in changes in the magnitudes of the impedances but did not change the arguments. Because the proposed technique based its decision on the arguments only, the changes in the magnitudes of the impedances did not have any impact on the decisions. This study illustrates the stability of the proposed technique when ct ratios do not match. The figure shows that the positive-sequence and negative-sequence trip counters of the relays R_1, R_2, R_3, R_4, and R_5 reached the threshold in 6 (6), 9 (11), 9 (8), 8 (9) and 12 (12) samples respectively. The algorithm made the final decision in 9.03 ms (i.e. 13/1440 ms) in all cases.

5.4.4. Summary of test results

Selected test results obtained during the performance evaluation phase of the proposed technique have been presented in Sections 5.4.2 and 5.4.3 in detail. Different types of faults at various locations in the simulated power systems were considered. The test studies considered different operating conditions of the power systems, four busbar configurations, and ct saturation. Tables 5.5 and 5.6 give a summary of the results obtained from the simulation studies reported in Appendix G.

5.5. Summary

The proposed busbar protection technique has been tested using data from simulations of two power system models. The procedure used for evaluating the performance of the proposed technique has been described in this chapter. Details of the system models used in the EMTDC simulations have been presented.

Different types of faults were simulated and data from these simulations were used to evaluate the technique proposed in Chapter 3. The impact of ct saturation and ct ratio-mismatch on the performance of the proposed technique has also been investigated. The test studies showed that the impedances seen by a relay when the ct to which it is connected saturated is higher in magnitude than the corresponding value when the ct was not saturated. The argument of the computed sequence impedances during ct saturation is

Table 5.5. Summary of the simulation studies, for the model power system shown in Figure 5.1, reported in Appendix G.

Fault location	Fault type	Busbar type	Post-fault samples needed for positive (and negative) sequence trip counters to reach threshold				Time (T)	Fig. (F)
			R1	R2	R3	R4		
1 (int.)	B-g, $R_f = 5\Omega$	single	9 (9)	9 (9)	9 (9)	9 (9)	6.25	G.1
3 (ext.)	A-C	single	20 (20)	20 (21)	17 (18)	17 (17)	13.89	G.2
1 (int.)	A-g	double	7 (7)	7 (7)	7 (7)	7 (7)	4.86	G.3
2 (ext.)	ABC	double	7 (-)	7 (-)	7 (-)	7 (-)	4.86	G.4
2 (ext.)	C-g $R_f = 15\Omega$	single	9 (9)	9 (9)	9 (9)	9 (9)	6.25	G.5
2 (ext.)	A-B	breaker-and-half	7 (7)	7 (7)	7 (7)	7 (7)	4.86	G.6
1 (int.)	A-g	ring	7 (7)	7 (7)	7 (7)	7 (7)	4.86	G.7
4 (ext.)	B-g, $R_f = 5\Omega$	ring	9 (9)	9 (9)	9 (9)	9 (9)	6.25	G.8
1 (int.)	ABC	breaker-and-half	7 (-)	7 (-)	7 (-)	7 (-)	4.86	G.9
1 (int.)	ABC	ring	7 (-)	7 (-)	7 (-)	7 (-)	4.86	G.10
1 (int.)	C-g	single	9 (9)	9 (9)	9 (9)	9 (9)	6.25	G.11
5 (ext.)	B-g	single	7 (7)	7 (7)	7 (7)	7 (7)	4.86	G.12
1 (int.)	A-B	breaker-and-half	7 (7)	7 (7)	8 (7)	7 (7)	4.86	G.13
2 (ext.)	B-C	breaker-and-half	7 (7)	7 (7)	7 (7)	7 (7)	4.86	G.14
1 (int.)	ABC-g, $R_f = 10\Omega$	double	7 (-)	7 (-)	7 (-)	7 (-)	4.86	G.15
6 (ext.)	ABC	double	7 (-)	7 (-)	7 (-)	7 (-)	4.86	G.16
1 (int.)	C-g	ring	9 (9)	9 (9)	9 (9)	9 (9)	6.25	G.17
1 (int.)	A-B	ring	7 (7)	7 (7)	8 (7)	7 (7)	4.86	G.18
6 (ext.)	A-g	ring	7 (7)	7 (7)	7 (7)	7 (7)	4.86	G.19
4 (ext.)	ABC	breaker-and-half	7 (-)	7 (-)	7 (-)	7 (-)	4.86	G.20

T: Fault-decision time (ms.) ; F: Reference figure in Appendix G.

Table 5.6. Summary of the simulation studies, for the power system shown in Figure 5.2, reported in Appendix G.

Fault location	Fault type	Post-fault samples needed for positive (and negative) sequence trip counters to reach threshold					Time (T)	Fig. (F)
		R1	R2	R3	R4	R5		
1 (ext.)	A-g	9 (9)	10 (8)	10 (9)	7 (10)	13 (12)	8.33	G.21
2 (ext.)	A-C	9 (9)	11 (11)	8 (8)	9 (10)	15 (15)	10.42	G.22
3 (int.)	ABC-g	7 (-)	11 (-)	9 (-)	9 (-)	12 (-)	8.33	G.23
4 (ext.)	B-g	8 (7)	12 (11)	10 (10)	9 (9)	12 (12)	8.33	G.24
5 (int.)	ABC	7 (-)	11 (-)	10 (-)	9 (-)	12 (-)	8.33	G.25
6 (int.)	B-C	8 (7)	12 (11)	10 (10)	9 (10)	11 (11)	7.64	G.26
7 (int.)	A-g	7 (7)	11 (12)	9 (8)	10 (10)	13 (13)	9.03	G.27
8 (int.)	C-g	7 (7)	11 (11)	10 (10)	9 (9)	13 (12)	8.33	G.28
9 (ext.)	A-B	7 (7)	12 (11)	7 (7)	8 (10)	13 (12)	8.33	G.29
10 (ext.)	B-C	8 (7)	7 (7)	10 (10)	9 (9)	12 (11)	7.64	G.30
5 (int.)	B-g	8 (7)	10 (12)	10 (10)	9 (9)	13 (12)	8.33	G.31
8 (int.)	A-B	7 (7)	10 (11)	10 (9)	9 (9)	12 (12)	8.33	G.32
18 (int.)	ABC	6 (-)	11 (-)	10 (-)	9 (-)	12 (-)	8.33	G.33
11 (int.)	C-g, R_f=10Ω	8 (8)	11 (11)	10 (10)	9 (9)	13 (12)	8.33	G.34
10 (ext.)	B-C	8 (7)	7 (7)	9 (9)	9 (9)	12 (12)	8.33	G.35
17 (ext.)	A-g, R_f=5Ω	9 (9)	12 (12)	9 (8)	10 (10)	12 (12)	8.33	G.36
15 (ext.)	ABC-g	6 (-)	11 (-)	9 (-)	7 (-)	12 (-)	8.33	G.37
6 (int.)	C-g, R_f=10Ω	8 (8)	11 (11)	9 (8)	9 (9)	13 (13)	9.03	G.38
15 (ext.)	B-g	7 (7)	11 (10)	9 (8)	8 (7)	12 (12)	8.33	G.39
16 (ext.)	ABC	7 (-)	11 (-)	9 (-)	10 (-)	7 (-)	7.64	G.40

T: Fault-decision time (ms.) ; F: Reference figure in Appendix G.

lower than the corresponding argument computed when the ct was not saturated. However, the impedances lies well within the fault-detection zone even when the cts are saturated. These observations are in agreement with the analysis presented in Section 4.2.3. The technique is stable when the ct ratios do not match. This can be attributed to the fact that the impedances calculated by each relay are independent of calculations performed by other relays.

The studies have shown that the proposed technique distinguishes correctly between internal and external faults. The stable performance of the proposed technique, during ct saturation and ct ratio-mismatch conditions, has also been established.

6. IMPLEMENTATION AND TESTING

6.1. Introduction

A digital technique for protecting busbars has been presented in Chapter 3. The technique was tested in off-line mode to evaluate its suitability. Configuration and data of a model system and an existing substation were used to verify the technique's performance. Samples of test results are presented in Chapter 5. The results show that the proposed technique is suitable for protecting busbars of different configurations without any modifications. Moreover, the technique provides stable performance during current transformer saturation and ratio-mismatch conditions.

The delta-impedance relays involved in the protection system were implemented using a general-purpose relay hardware. The hardware and software constituents of the prototype delta-impedance relays are presented in this chapter. The procedure for testing the delta-impedance relays by using a playback simulator is reported in the chapter and selected test results are also included.

6.2. The busbar protection system

Using the technique developed in Chapter 3, a busbar protection system has been developed. As explained in Section 3.3.2.5, individual decisions from the delta-impedance relays are used in the trip logic for final detection of the fault. The proposed protection system has been realized in practice by processing the voltages and currents at the individual relay locations. Each relay performs the procedural steps explained in Section 3.3.1 and transmits its decision to the trip logic shown in Figure 3.9. The implementations of all the delta-impedance relays are similar. As such the same are explained with respect to a single relay in the following sections.

6.3. The delta-impedance relay

This section describes the hardware and software components required for the real-time implementation of the proposed delta-impedance relay. The verification of the proposed technique, using these relays, as applied to an existing power substation is illustrated using sample test results.

6.3.1. Hardware

The proposed delta-impedance relay was implemented in the laboratory using a general-purpose relay hardware [51]. This includes four major components: low-pass filter boards, data-acquisition system (DAS) cards, a digital signal processing (DSP) card and a host personal computer. Figure 6.1 shows the organization of the hardware components. A brief description of these components is provided in the succeeding sections.

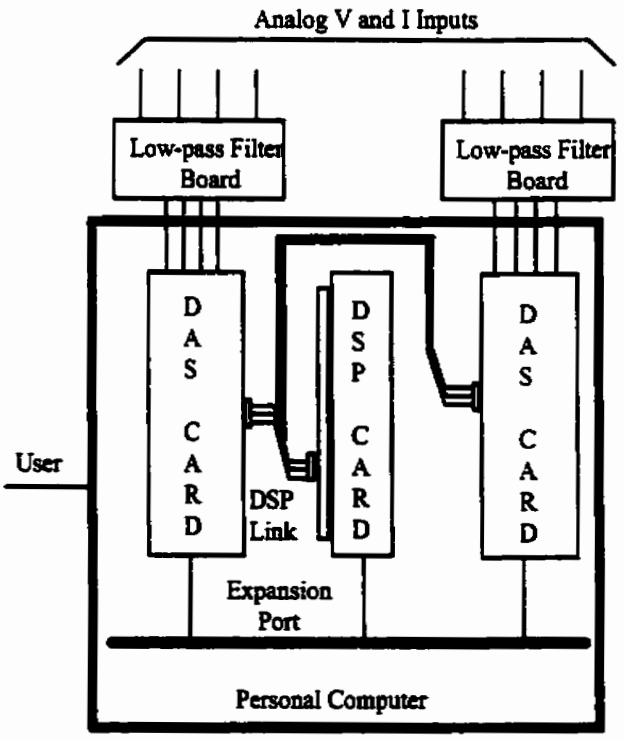


Figure 6.1. Hardware configuration of the proposed delta-impedance relay.

6.3.1.1. Low-pass filter boards

The low-pass filter is required to band-limit the analog current and voltage signals to the data-acquisition system and to prevent aliasing in samples of voltages and currents. Cut-off frequency of the low-pass filter depends on the frequency at which voltage and current signals are sampled by the data-acquisition system. A cut-off frequency of 200 Hz has been used in the test studies. Switched capacitor filters, designed using MF6CN-100 [52] are used. The circuit diagram of one channel of the low-pass filter is shown in Figure 6.2.

MF6CN-100 is a low cost, easy to use 6th order low-pass filter with 14-pin DIP packaging. They provide a wide range of cut-off frequency obtainable by changing the external clock frequency. The ratio of clock frequency to cut-off frequency is internally set to 100:1. A TTL logic compatible clock signal is provided to MF6CN-100 from a signal generator for cut-off frequency control.

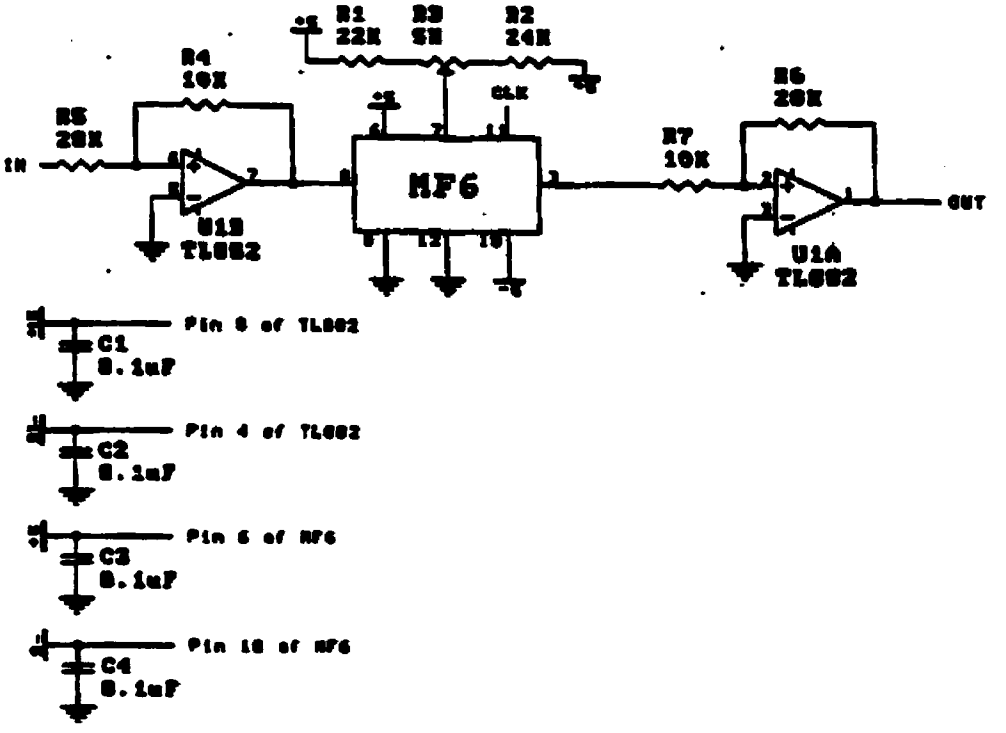


Figure 6.2. Circuit diagram of one channel of the Butterworth low-pass filter [52, 53].

Two operational amplifiers available from a TL082 chip [53] are provided at the input and output of the filter for the purpose of buffering the signals. As an additional feature, gain of the operational amplifier at the input of the filter is set to 0.5 while the operational amplifier at the output of the filter has a gain of 2.0. This feature extends the range of signals that can be filtered to ±5.0V from ±2.5V. Two filter boards each capable of handling four signal channels are used. The filters on these boards are powered from a ±15V power supply.

6.3.1.2. Data-acquisition system cards

The data-acquisition system consists of hardware that samples and quantizes signals at a specified rate (1440 Hz used for the present work). It employs two 4-Channel Analog Interface cards [54] to collect data from the eight channels. Each card supports four analog input channels and two analog output channels. Each card provides facilities that include four analog signal conditioning units, a quad sample/hold amplifier, an analog-to-digital conversion (ADC), a sample rate timer, and the control and status registers with the associated interrupt control.

Analog signal conditioning unit includes a unity gain low offset operational amplifier that buffers the input signal from the on-card low-pass filter. A ±2.5V analog input signal provides full scale operation of the ADC and it is necessary to limit the input signals below ±3.0V to prevent damage to the quad sample/hold chip. The signal conditioning block also has programmable 3rd order Butterworth low-pass analog filters to suppress unwanted high frequencies. They are suitable as anti-aliasing filters only if the sampling frequency is very much higher than the maximum input frequency component. However, in the present project, the sampling frequency is not very much higher than the input frequency component, an external low-pass filter, as described in the previous section, is used as an anti-aliasing filter.

The output from analog signal conditioning unit is fed to the quad sample/hold chip. It performs the sampling of input signals at a pre-defined sampling rate defined using the sample rate timer. The quad sample/hold also performs the multiplexing of the input

signals to a single analog-to-digital converter (ADC). The conversion of a channel, selected by the control register, presented to the ADC is initiated by a trigger signal to the ADC. The ADC indicates the end-of-conversion by setting the EOC bit high which is read by the DSP through the status register. The sample rate timer is a 16-bit up counter running at 8 MHz. The counter has a programmable input register from which the counter is loaded every time the maximum count value of FFFF (hexadecimal) is reached. Each card occupies a short PC slot and is powered from the bus. All control and data signals are transferred via 50-pin DSPLINK2 connector from the digital signal processing card.

6.3.1.3. Digital signal processing card

The PC/C31 card [55, 56], based around the 33.3 MHz TMS320C31 Digital Signal Processor from Texas Instruments [57], is used as a digital signal processor card. It is a full-height, two-thirds length card. It occupies one 16 bit PC slot and draws power from the PC bus.

Communication between the PC and the DSP card takes place over two autonomous interface. Memory-Mapped Interface, consist of DPRAM, allows fast information exchange between the PC and DSP without disrupting the process of either device. I/O-Mapped Interface provides access to various card facilities, such as reset and interrupts, through software programmable control registers. The PC/C31 card is equipped with Loughborough Sound Images Ltd.'s DSPLINK2 digital system expansion interface. It has a bi-directional bus that allows input/output directly to/from the DSP, without using the I/O bus on the PC. DSPLINK2 interface is used to communicate with the data acquisition system cards, described in the previous section. There are four maskable interrupts to the TMS320C31 DSP driven by DSPLINK2, PC and other optional peripheral devices. One such DSP card is used in the developed relay.

6.3.1.4. Host personal computer

The PC/C31 DSP card and data-acquisition (DAS) cards are placed into the expansion ports of an IBM compatible personal computer. This host PC provides facilities to:

(i) control the operation of the DSP and DAS cards,

(ii) debug the softwares and

(iii) access various memory locations and registers in the DSP.

A personal computer based on Intel Corporation's 486 processor, running at 66 MHz is used. The PC runs on Microsoft Windows for Workgroups Version 3.11 operating system.

6.3.2. Software

Three softwares are needed for implementing the prototype relay i.e. data-acquisition, relaying and user-interface softwares. Figure 6.3 shows the organisation of these softwares within the delta-impedance relay.

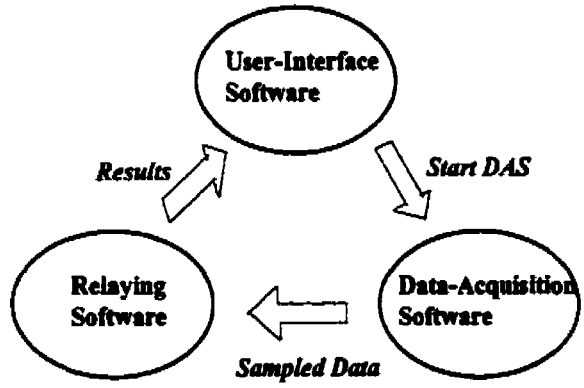


Figure 6.3. Organization of softwares within the delta-impedance relay.

6.3.2.1. Data-acquisition software

The data-acquisition software is used to initialise the data-acquisition system cards, control a sample-rate timer and acquire samples at successive sampling instants. It consists of two routines, a main routine and an interrupt service routine. The main routine initialises the system cards and loads the timer with the appropriate hexadecimal number which is stored in a specified DSP memory location. This number corresponds to the selected sampling rate, which is 1440 Hz. The main routine enables an interrupt after loading the timer which results in activation of the interrupt service routine. Interrupt service routine executes the functions related to data-acquisition such as sample-and-hold,

analog-to-digital conversion and initiates the execution of the relaying software after acquiring a set of samples.

6.3.2.2. Relaying software

An executable code of the relaying software is generated using TMS320 floating-point C compiler and then loaded into the memory of the DSP. Quantized samples obtained from DAS are used by this code to execute the proposed technique. ANSI C programming language has been used to develop the relaying software. The relaying software, based on the proposed fault-detection technique is executed by the individual delta-impedance relays. The relaying software carries out the following computations as explained in Section 3.3.2.

(a). Estimates the phasors and sequence-phasors from the voltages and currents samples obtained using the data-acquisition software.

(b). Detects the onset of fault by comparing the changes in magnitudes of the voltage (V_CHANGE) and current (I_CHANGE) phasors to be above a pre-specified threshold for three consecutive times. Unlike detection of the fault, carried out using sample magnitudes in simulation studies, phasor magnitudes are used in real-time testing of the technique. This is done keeping in view the limited resolution of the A/D converter and existence of large differences between the signal levels, particularly current, before and after the occurrence of a fault. As such, smaller magnitudes of the signals, before the onset of fault, can be affected by the presence of noise and may result in incorrect identification of the onset of fault. Use of phasor magnitudes, calculated from a collection of samples in a data window, ensures correct detection of fault-inception as the noise is removed by the filters used for estimating phasors.

(c). Computes the incremental-sequence phasors using pre-fault and fault samples after the fault has occurred.

(d). Calculates the sequence impedances using incremental current and voltage phasors.

(e). Forms trip counters using the arguments of the impedances and the fault-detection characteristics described in Section 3.2.3.

(f). Generates the trip-signal representing relay's decision.

The relaying software has the provision to record the samples of the voltages and currents in different phases acquired by the delta-impedance relays. The output results are reported in the form of data files which contain the profiles of the trip-counters and computed sequence impedances.

6.3.2.3. User-interface software

The user-interface software, developed in Visual Basic™ [58], is used to upload the results from the memory of the digital signal processor (DSP). PC/C31 IIL (Intelligent Interface Library) functions [59] are used in the development of this software. It has the flexibility of scanning the DSP board memory by selecting the corresponding start address and the number of individual data points required. The display of the developed user-interface is shown in Figure 6.4.

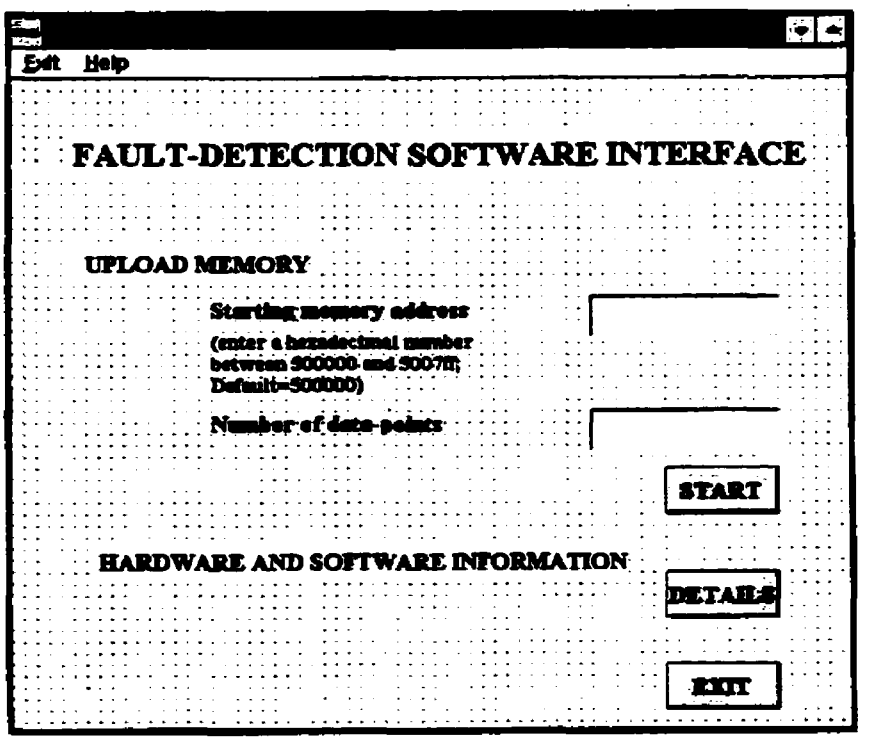


Figure 6.4. Display of the user-interface.

6.4. Testing

The proposed microprocessor-based system employing delta-impedance relays for protecting busbars was implemented and tested in the laboratory. This section describes the testing of the hardware and software followed by the test set-up, the power system configuration employed in the test studies and illustration of sample test results.

6.4.1. Hardware and software components

The hardware and software of the proposed relay used were tested individually for their correct functionality before combining them. This section explains the procedures adopted for the testing of these hardware and software components.

6.4.1.1. Low-pass filter

Low-pass filters were implemented in a circuit board with ICs and discrete components. Cut-off frequency of 200 Hz was selected for the low-pass filters. The filter was tested using a spectrum analyser. The frequency response of one of the filters built is shown in Figure 6.5. The response indicates that the filter performance is close to the expected response.

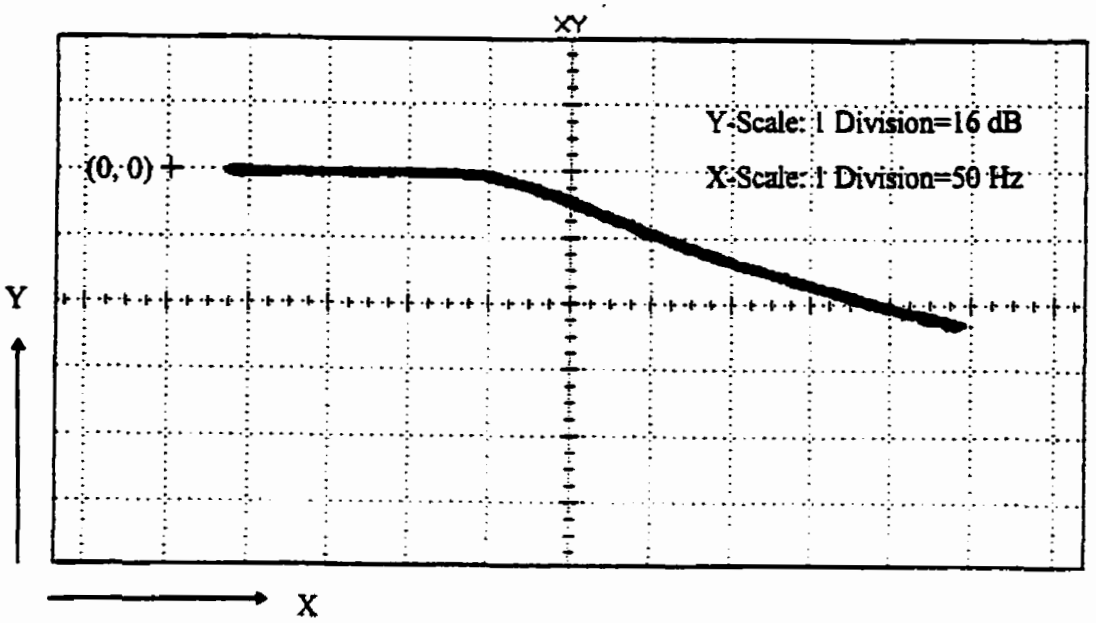


Figure 6.5. Frequency response of the sixth order Butterworth low-pass filter.

6.4.1.2. Data-acquisition software

Data acquisition software was tested by applying a sinusoidal test waveform from the FDF Dynamic Frequency Source [60] of the Doble Engineering Company. The level of the signal was first checked in an oscilloscope to ensure that it is less than ±2.0 Volt so that the data acquisition card is not stressed. Initial testing of the data acquisition software was done by using the MPC View C Source Debugger [61] available from Spectrum Signal Processing, manufacturer of DSP and DAS cards.

MPC View is a Windows based user-interface and it allows different functions like load, display and execution of the DSP code. It also allows data management facility and all data in the DSP including memory and registers can be viewed in a desired format: floating-point, hexadecimal or decimal. MPC View can also be interfaced with an Intelligent Interface Library (IIL).

Testing of the data acquisition system revealed that the on-board low-pass filters in the two DAS cards have significantly different group delays which has resulted in a phase-shift between the signals acquired by the two boards. The amount of phase-shift was determined and software compensation was provided to eliminate the undesired phase-shift between the signals acquired by the two boards.

6.4.1.3. Relaying software

The relaying software was tested by including a data file, containing simulated fault data, in the software. This data file was previously used for off-line testing of the proposed technique. The testing of the relaying software was done on a PC equipped with a TMS320C30 Evaluation module (EVM) [62]. The debugging of the program was done by using a TMS320C30 C Source Debugger [63]. Appendix H gives an overview of the testing system used and the procedures followed.

This testing of the relaying software is required to confirm that the software can be executed within the inter-sampling time. Benchmarking of the relaying software indicates that it can be executed within 0.412 millisecond for each pass of the program. This is much less than the available inter-sampling time of 0.694 millisecond for 1440 Hz

sampling frequency. Even if the software overhead for data acquisition is added, it is expected to be much less than the inter-sampling time. Results from these tests are similar to those obtained from the simulations on the UNIX workstation. This verifies the accuracy of the computations performed by the DSP.

6.4.1.4. User-interface software

The user-interface software, developed in Visual Basic™, used to upload the results from the memory of DSP was tested by running a test case. The values of the sequence-impedances computed by a delta-impedance relay and the associated trip counters were stored in the memory of DSP. The user-interface software was executed to upload these results to a data file. The flexibility of the user-interface software to scan the DSP board's memory by selecting the corresponding start address and the number of data points uploaded was also tested.

6.4.2. The busbar protection system

Individual delta-impedance relays were tested to verify the performance of the proposed busbar protection system. This section describes the test set-up and selected test results.

6.4.2.1. Test set-up

Figure 6.6 shows an overview of the complete test set-up. The various steps performed in testing of the proposed delta-impedance relay involve:

(a) generation of fault data using simulations,

(b) playback of the simulated data and

(c) testing of the relay.

Generation of fault data

The performance of the proposed delta-impedance relay was verified using the configuration and data of an existing substation (BRADA) of the SaskPower. The substation is of double busbar configuration and has five different circuits operating at 230 kV and 138 kV levels. Delta-impedance relays R_1 to R_5, as shown in Figure 6.7, are used

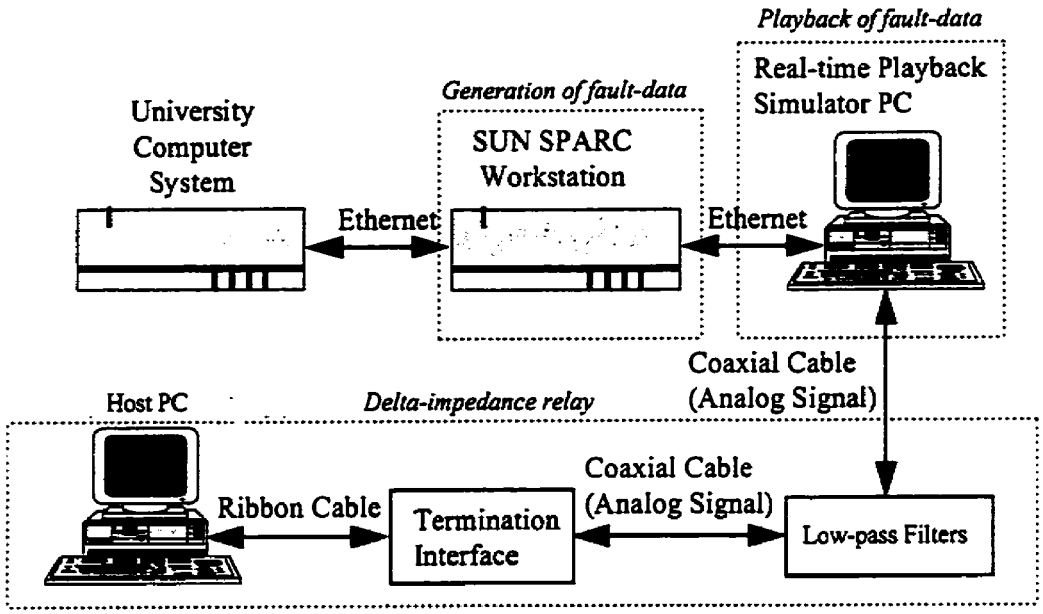


Figure 6.6. Testing arrangement for a delta-impedance relay.

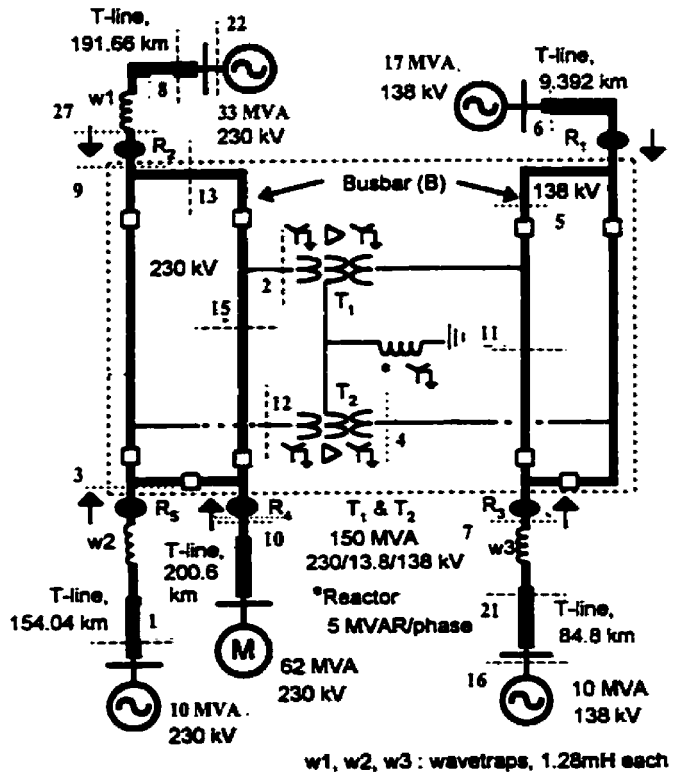


Figure 6.7. System model used for simulating data using the EMTDC.

for providing protection to the busbar (B). The data for two different operating conditions of the substation was used in the studies. Figure 6.7 also shows the power system model and the parameters of the system components used to generate the fault data. Various fault locations considered in the test studies are also indicated in the figure.

Faults were simulated, in the selected busbar system, on the SUN SPARC workstation using the PSCAD/EMTDC and the ct model using a time-step of 1.0/23040 seconds. Various levels of ct saturation, obtained by changing the burden, were used. A recorder component, used in the simulations, stored the voltage and current samples as playback files, which were used by Real-Time Playback Simulator to generate analog signals. Parameters of the recorder component are given in Appendix D.

Playback of the simulated data

Power System Analysis laboratory at the University of Saskatchewan, Canada has a personal computer equipped with hardware and software for use as a Real-Time Playback Simulator (RTPS) [64]. Data files containing fault data, generated by the PSCAD/EMTDC power system simulation software, can be played back using the RTPS to provide the corresponding analog signals. These analog signals were given as input to the delta-impedance relay for testing. Figure 6.8 shows a typical display of the RTPS wherein a fault waveform is shown being played back. The currents in the simulated power system were decreased from the system level to relay levels by using current transformers. Ct ratios of 80, 80, 100, 80 and 80 were used for the relays R_1, R_2, R_3, R_4 and R_5 respectively. Appendix I gives an overview of the RTPS.

The corresponding voltage signals were lowered in magnitude by a factor of 1000 for all the relays using potential transformers. These currents and voltages were further decreased by using auxiliary ct and pt ratios. This was accomplished by using the gain settings available in the RTPS software. This ensured that the current and voltage inputs to the DAS are well within the available range(±2.5V peak-to-peak). The ratio of auxiliary cts and pts at different relay locations are given in Table 6.1.

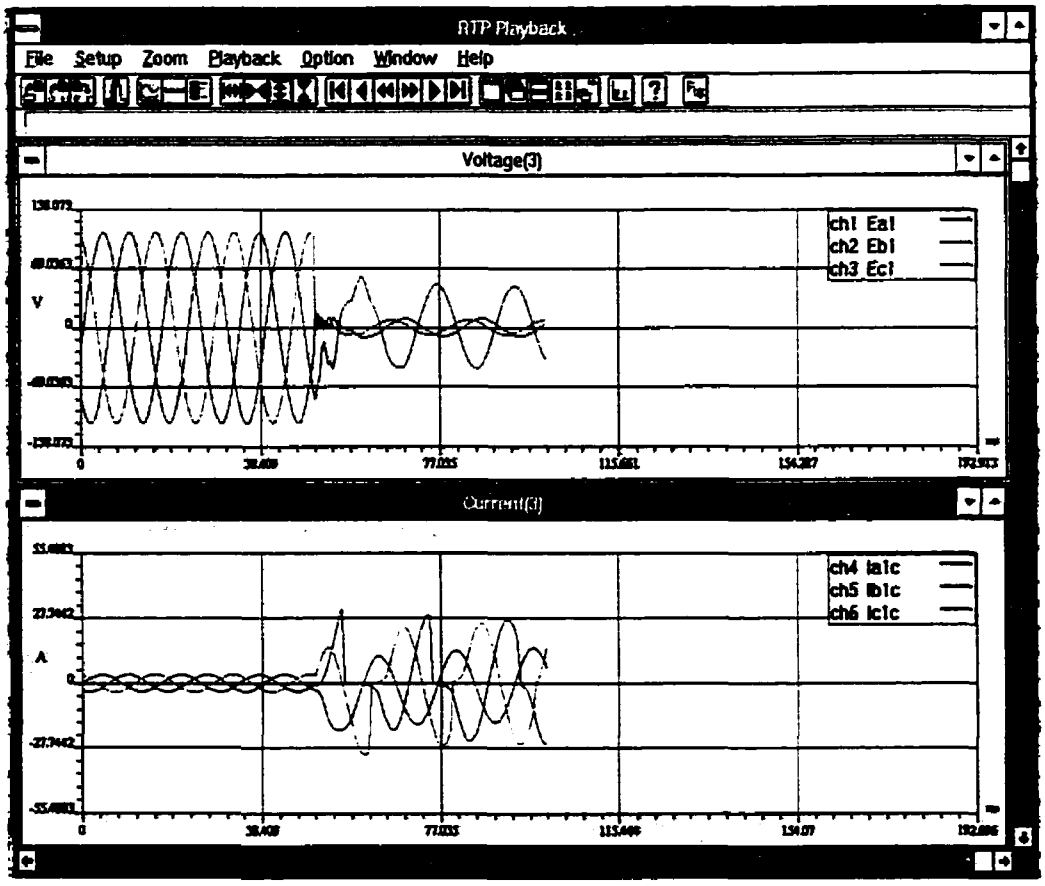


Figure 6.8. A fault waveform being played back by the Real Time Playback Simulator.

Table 6.1. Ratios of auxiliary pts and cts.

Relay	pt ratio	ct ratio
R_1	70	50
R_2	120	40
R_3	70	50
R_4	120	40
R_5	120	40

Relay testing

Tests were conducted using the five sets of voltages and currents samples obtained at the delta-impedance relay locations (R_1, R_2, R_3, R_4 and R_5 shown in Figure 6.7). Test set-up shown in Figure 6.6 was used for testing the relays. Each set of data results in an individual decision. These decisions were combined using the logic circuit shown in Figure 3.9 to provide the final fault-detection. The values of I_CHANGE and V_CHANGE used for detecting fault-inception were set at 30% and 15% of the pre-fault current and voltage magnitudes respectively. To ensure algorithm sensitivity and maintain security against false trips, the value of THRESHLD was set at six. Selected test studies are presented in the next section.

6.4.2.2. Results

The designed delta-impedance relay sampled the analog voltages and currents generated by RTPS at 1440 Hz. Results showing the performance of the proposed relay for different types of faults occurring at various locations in the selected power system are presented. The effect of ct saturation was also considered in the test cases.

Figure 6.9 demonstrates the performance of the proposed protection system for a single-phase-to-ground fault involving Phase A occurring at location 3 shown in Figure 6.7. Figure 6.9(a) shows the current waveforms, reconstructed using their samples obtained by the delta-impedance relay R_1.

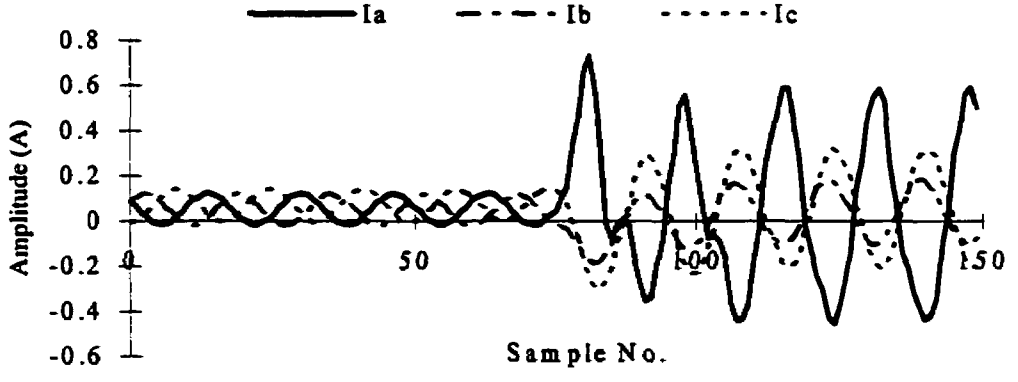
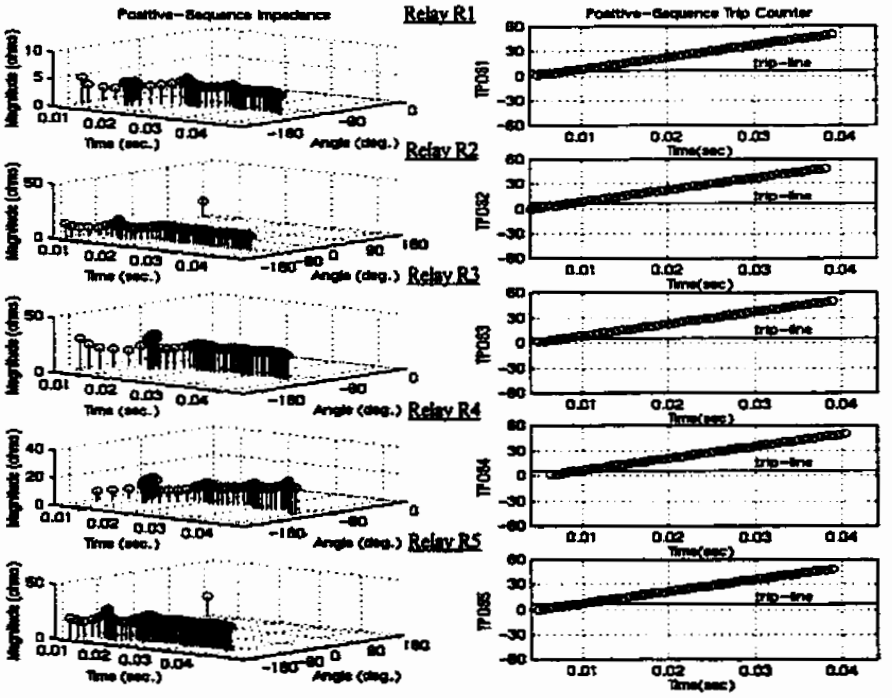


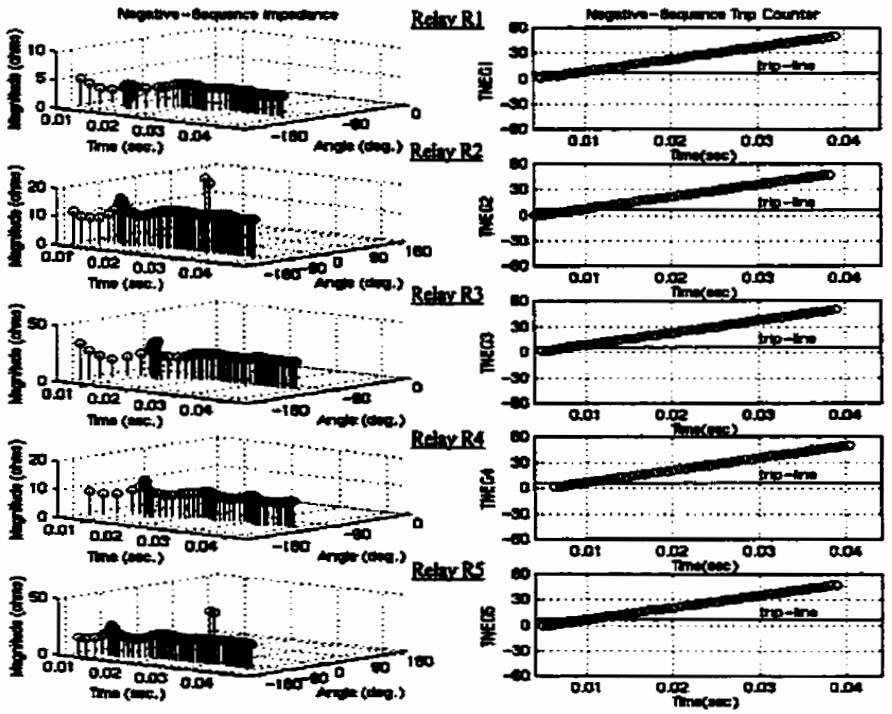
Figure 6.9 (a). Profile of the currents, reconstructed using data samples acquired by the delta-impedance relay R_1.

It takes 7, 6, 7, 9 and 7 fault samples by the relays R_1 to R_5 respectively to detect the onset of fault. After this delay, the incremental-sequence impedances are computed. The plots show that the argument of all the impedances computed by different delta-impedance relays lie in the third quadrant. This leads to the decision that fault is inside the protection zone of the busbar. Figures 6.9(b) and 6.9(c) show the profile of magnitudes and arguments of the positive-and negative-sequence impedances respectively which are computed from voltages and currents data obtained by the various delta-impedance relays indicated in Figure 6.7. From the plots of corresponding positive- and negative-sequence trip counters, shown in Figures 6.9(b), 6.9(c) and 6.9(d) respectively, it is observed that the trip-logic of the proposed system will issue a trip command in 14 fault samples i.e. 9.72 ms (14/1440). From Figure 6.9(a), it is seen that current in Phase A is highly saturated. However, the onset of saturation does not alter the decision made by the proposed technique.

Figure 6.10 shows the performance of the proposed system for an external fault involving phases A and B (location 21, Figure 6.7). Figure 6.10(a) shows the current waveforms, reconstructed from the samples acquired by the delta-impedance relays R_1 and R_3. The positive- and negative-sequence impedances computed from the voltages and currents samples obtained at different locations are shown in Figures 6.10(b) and 6.10(c) respectively. The plots of corresponding trip counters are also shown in these figures and Figure 6.10(d). The detection of fault-inception by the relays R_1 to R_5 takes 5, 6, 5, 9 and 7 fault samples respectively. After this delay, the sequence impedances are computed at the individual relay locations. It is seen that the impedance-argument computed for all the relays except the relay R_3 lie in the third quadrant. The argument of the impedances computed by the relay R_3 is positive. As such, it is concluded that the fault is external to the busbar protection zone. The profile of trip counters indicate that the trip-logic will establish the fault in 14 fault samples i.e. 9.72 ms (14/1440). The saturation of cts installed for phases A and B at relays R_1 and R_3, however, does not affect the decision made by the proposed technique.



(b)



(c)

Figures 6.9 (b) & (c). Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-ground internal fault (location 3, Figure 6.7).

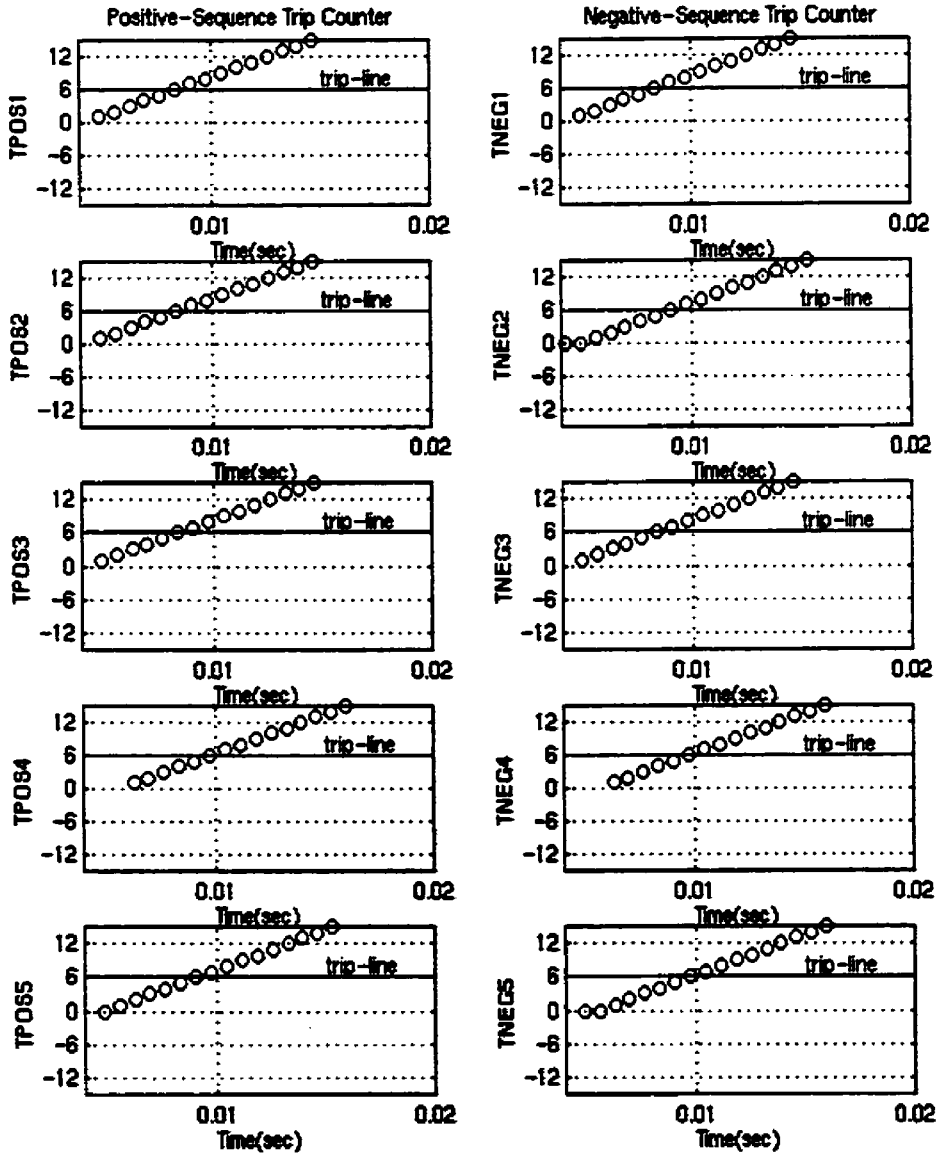


Figure 6.9 (d). Plots of positive-sequence and negative-sequence trip counters (on expanded scale) for Phase A-ground internal fault (location 3, Figure 6.7).

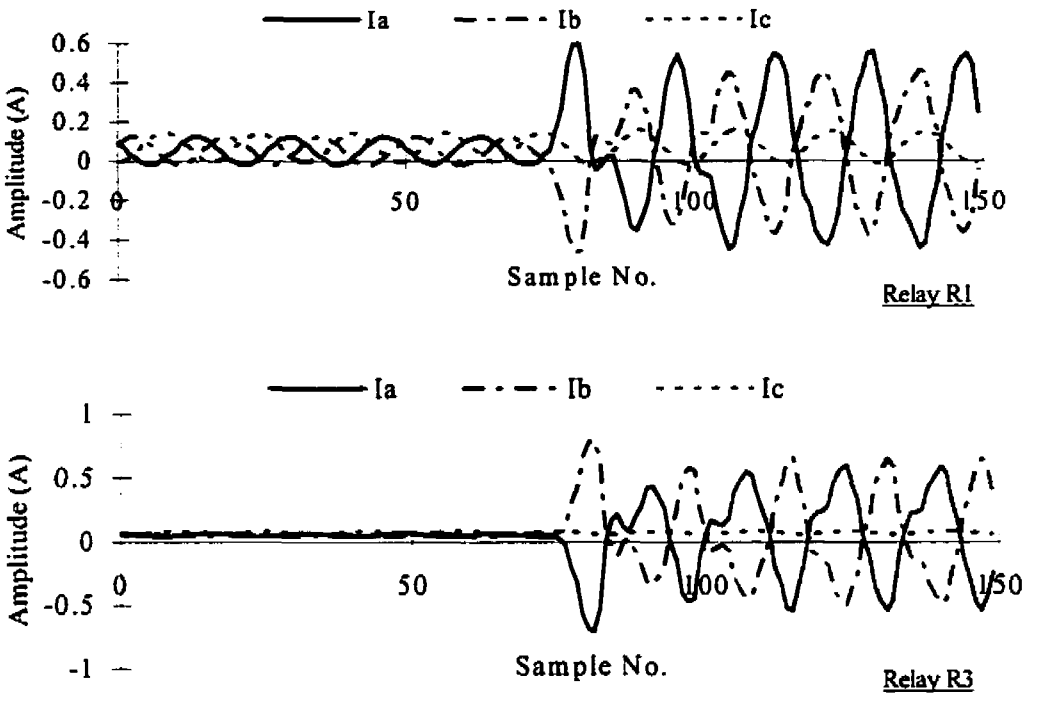
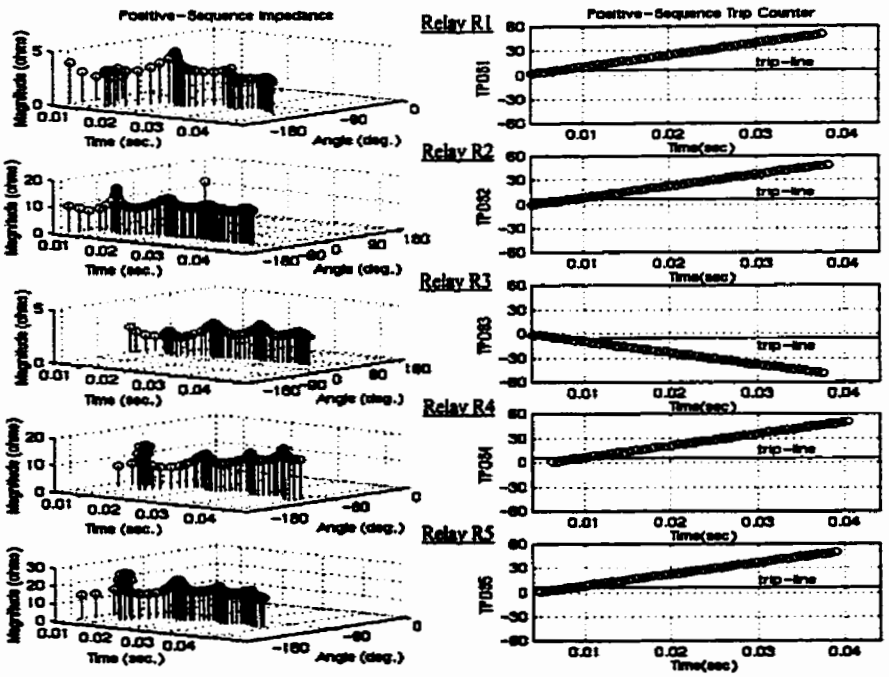
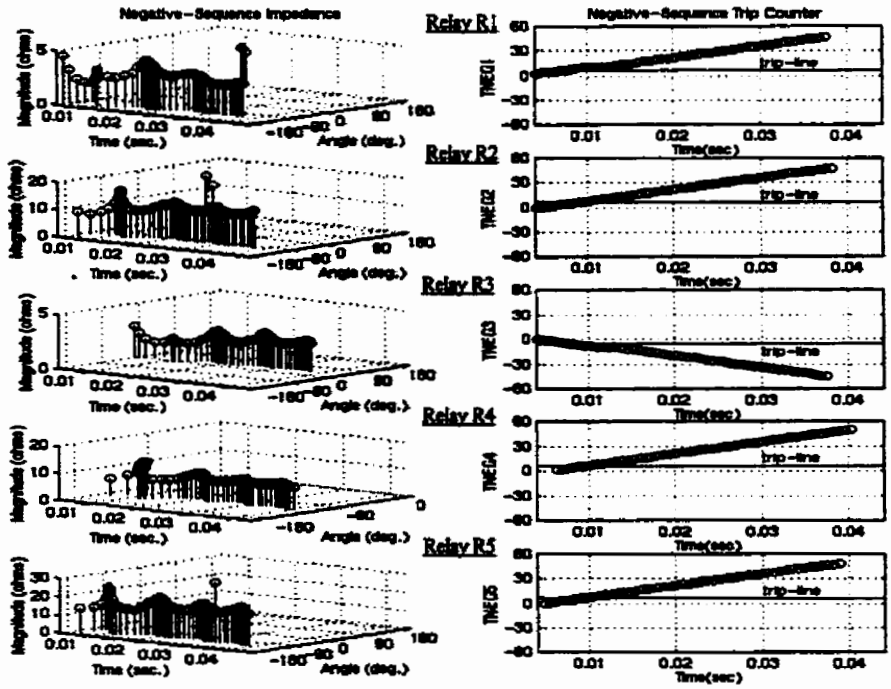


Figure 6.10 (a). Profile of the currents, reconstructed using data samples acquired by the delta-impedance relays R1 and R3.

Figure 6.11 demonstrates the performance of the proposed protection system for a Phase A-Phase B fault occurring at location 5 shown in Figure 6.7. It takes 5, 9, 9, 11 and 8 fault samples by the relays R_1 to R_5 respectively to detect the onset of fault. After this delay, the incremental-sequence impedances are computed. The plots show that the argument of all the impedances computed by different delta-impedance relays lie in the third quadrant. This leads to the decision that fault is inside the protection zone of the busbar. Figure 6.11 shows the profile of magnitudes and arguments of the positive-sequence and negative-sequence impedances respectively which are computed from voltages and currents data obtained by the various delta-impedance relays shown in Figure 6.7. The profiles of trip counters are also shown in the figure. From the plots of corresponding positive- and negative-sequence trip counters, it is observed that the trip-logic of the proposed system will issue a trip command in 16 fault samples i.e. 11.11 ms (16/1440).



(b)



(c)

Figures 6.10 (b) & (c) Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-Phase B external fault (location 21, Figure 6.7).

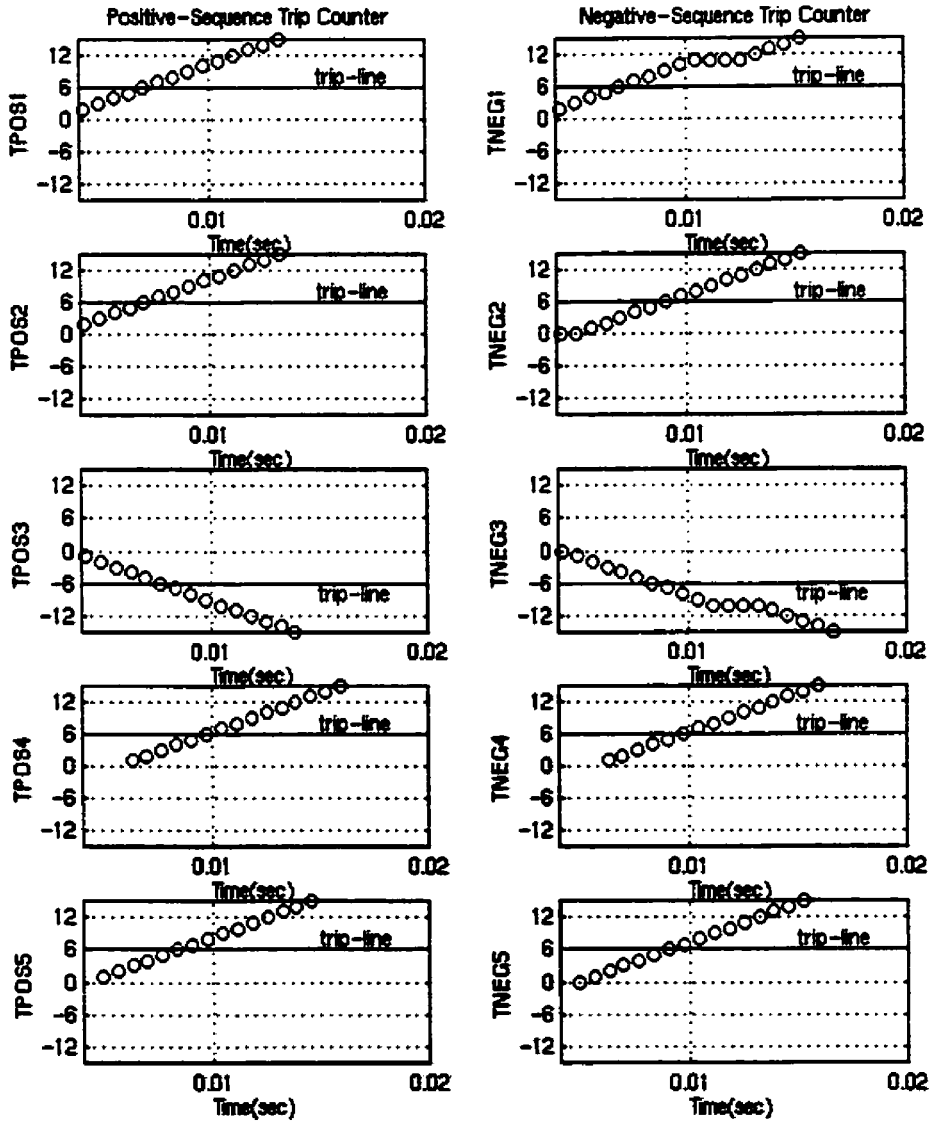
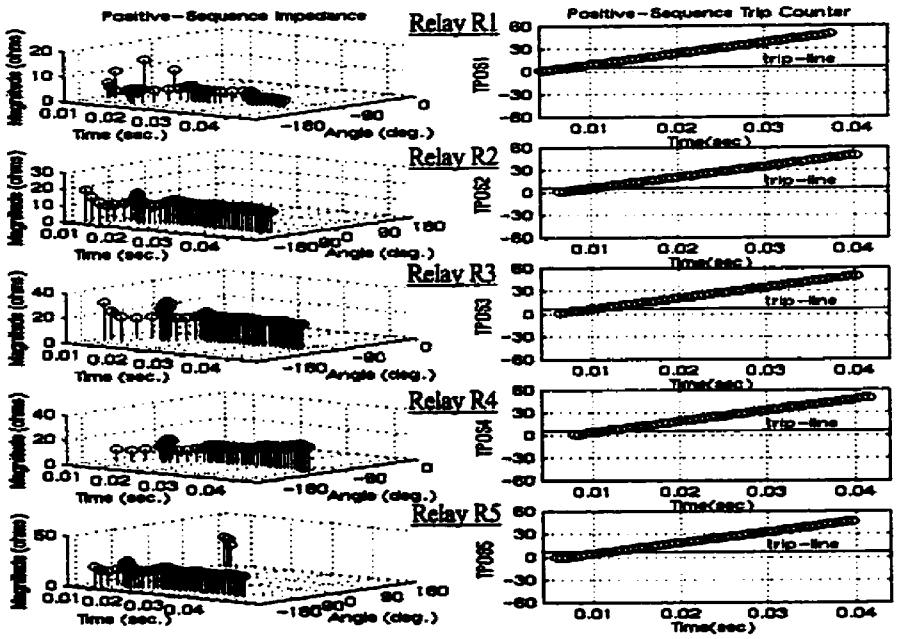
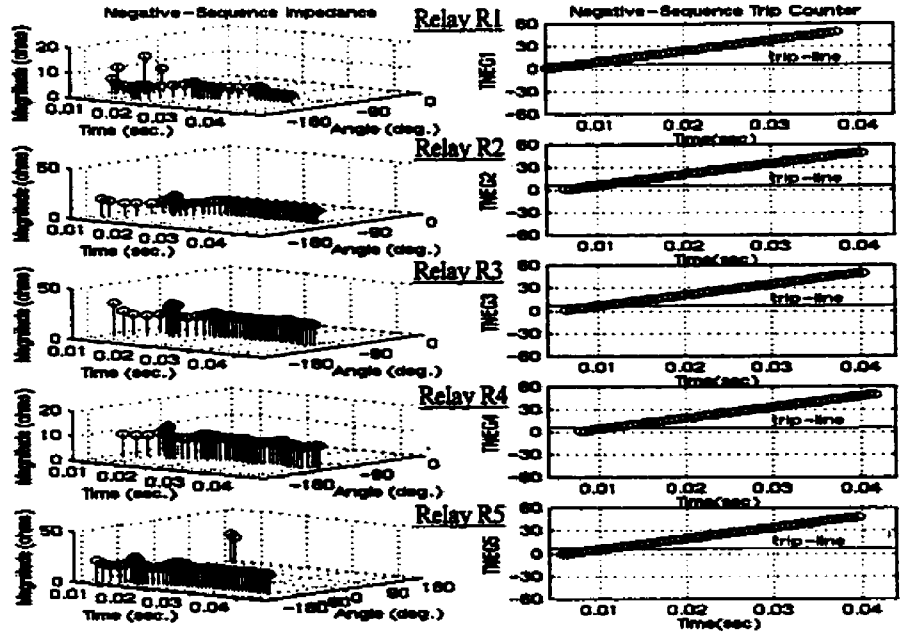


Figure 6.10 (d). Plots of positive-sequence and negative-sequence trip counters (on expanded scale) for Phase A-Phase B external fault (location 21, Figure 6.7).



(a)



(b)

Figure 6.11 (a). Profiles of (a) positive-sequence and (b) negative-sequence impedance magnitude, argument and the trip counters for Phase A-Phase B internal fault (location 5, Figure 6.7).

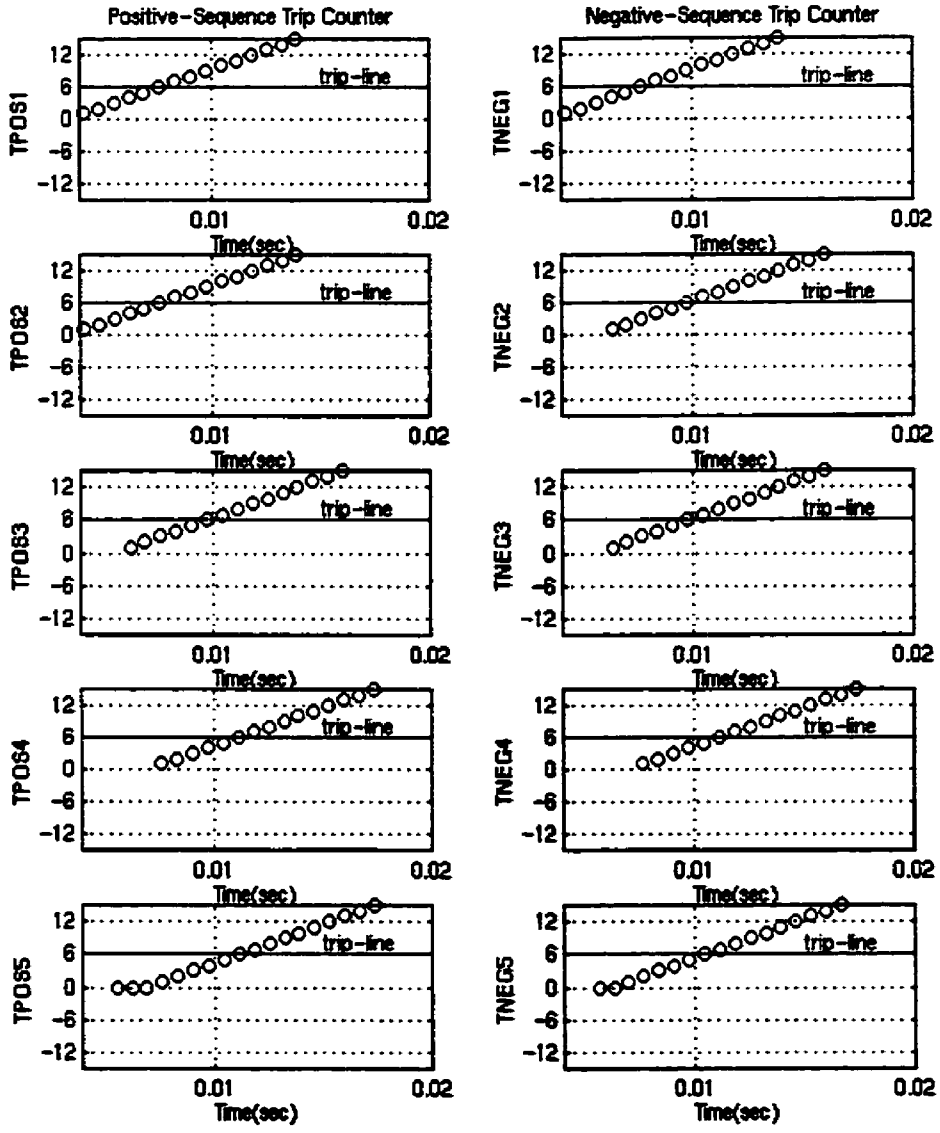


Figure 6.11 (b). Plots of positive-sequence and negative-sequence trip counters (on expanded scale) for Phase A-Phase B internal fault (location 5, Figure 6.7).

6.5. Additional test results

The performance of the delta-impedance relays was tested in the laboratory by simulating various types of faults at different locations in the power system configuration shown in Figure 6.7. The test studies also included faults occurring through fault resistance of different magnitudes.

Table 6.2 presents a summary of sample test results. The number of fault samples required for the positive- and negative-sequence trip-counters to reach the threshold limit and, thus, the time required for making a final decision on fault-detection for each test case are also shown in this table. Various fault locations indicated in the table are shown in Figure 6.7. Plots of positive- and negative-sequence impedances computed by different relays for the results outlined in Table 6.2 are presented in Appendix J.

6.6. Summary

This chapter described the implementation and testing of the proposed technique. The proposed system is explained to be composed of delta-impedance relays which execute the fault-detection algorithm based on the proposed technique. The implementation of these relays require hardware and software. These constituents of the relays are described and their pertinent characteristics are outlined.

The testing of the proposed relays involves prior testing of the associated hardware and software. The details of testing hardware and software have been presented. The complete set-up used in testing the proposed protection system has been shown. Various steps involved to carry out the test studies such as generation of fault data, playback of data and the relay testing are explained.

For the considered test cases, each of the prototype delta-impedance relays was tested by playing back simulated data using a Real Time Playback Simulator. The test results show the reconstructed waveforms of test signals, the calculated impedances and the trip counters. The final fault-decision times are also given. These trip times are in the range of 9.0 to 13.5 ms.

Table 6.2. Summary of additional test cases from real-time testing.

Fault location	Fault type	#Samples required for detecting fault and positive and negative-sequence trip counters to reach threshold					Fault-decision		Ref. Fig. (F_J)
							[a]F	[b]T	
		R1	R2	R3	R4	R5			
1	B-g (ext.)	5,10,10	5,10,11	5,10,11	12,17,17	3,20,20	20	13.89	J.1
2	A-g (int.)	7,12,12	6,12,13	7,12,13	9,14,14	7,13,14	14	9.72	J.2
3	A-g (int.)	7,12,12	6,12,13	7,12,12	9,14,14	7,13,14	14	9.72	J.3
4	C-g (int.)	6,11,11	4,9,9	6,11,11	12,17,17	4,11,10	17	11.81	J.4
5	A-B (int.)	5,19,20	6,11,12	4,10,11	8,13,13	5,12,13	19	13.19	J.5
6	A-g (ext.)	9,14,14	8,14,14	7,12,12	18,23,23	5,12,13	23	15.97	J.6
7	A-g (ext.)	7,12,12	7,12,13	4,11,12	9,14,14	7,14,15	14	9.72	J.7
8	B-g (ext., R_f=20 Ω)	6,11,11	3,10,11	4,9,10	13,18,18	6,11,11	18	12.5	J.8
9	B-g (int.)	5,10,10	6,11,11	4,10,10	11,16,16	4,11,12	16	11.11	J.9
13	C-g (int.)	6,13,12	4,10,9	7,12,12	13,18,18	4,10,10	18	12.5	J.10
10	A-B-C (ext.)	5,10,-	4,10,-	4,10,-	5,10,-	3,10,-	10	6.94	J.11
11	C-g (int., R_f=10 Ω)	7,13,13	6,11,11	6,11,11	13,18,18	4,10,10	18	12.5	J.12
12	A-g (int., R_f=5 Ω)	7,12,12	6,12,13	6,11,12	10,15,15	7,14,14	15	10.42	J.13
12	A-B-C (int.)	4,9,-	3,9,-	5,10,-	9,14,-	4,11,-	14	9.72	J.14
13	B-C (int.)	5,10,10	4,10,10	4,10,9	10,15,15	3,10,10	15	10.42	J.15
15	B-g (int.)	4,10,10	5,10,10	5,11,11	9,14,14	5,11,11	14	9.72	J.16
16	A-C (ext.)	12,17,17	12,17,17	4,11,9	22,27,27	12,17,17	27	18.75	J.17
4	B-C (int.)	4,9,9	4,10,10	4,9,9	11,16,16	3,11,10	16	11.11	J.18
13	A-C (int.)	5,12,11	9,14,14	8,13,13	11,16,16	8,15,14	16	11.11	J.19
13	C-g (int.)	6,12,13	3,9,9	5,10,10	12,17,17	3,10,9	17	11.81	J.20
4	A-g (int.)	7,12,12	7,12,14	6,11,12	9,14,14	7,13,14	14	9.72	J.21
21	A-B (ext.)	5,10,10	6,12,13	5,11,12	9,14,14	7,12,13	14	9.72	J.22
22	A-g (ext.)	9,14,14	10,15,15	8,13,13	21,26,26	9,14,15	26	18.06	J.23
13	A-g (int.)	7,12,12	7,13,14	6,11,11	9,14,14	7,13,14	14	9.72	J.24
4	A-B-C (int.)	5,10,-	3,10,-	4,9,-	9,14,-	3,10,-	14	9.72	J.25
1	A-g (ext.)	7,12,12	8,13,14	6,11,13	17,22,22	6,12,11	22	15.28	J.26
27	A-B-g (ext.)	5,10,21	5,10,18	5,10,18	8,13,17	4,11,20	13	9.03	J.27
12	C-g (int., R_f=10 Ω)	6,13,13	4,9,9	9,14,14	12,17,17	3,10,9	17	11.81	J.28
4	A-g (int.)	7,12,12	4,11,11	4,11,11	9,14,14	5,11,11	14	9.72	J.29
5	A-B-C-g (int.)	4,9,-	4,10,-	4,9,-	9,14,-	3,10,-	14	9.72	J.30
12	A-B-g (int.)	5,10,20	5,10,16	5,10,17	8,13,17	4,10,19	13	9.03	J.31
1	B-g (ext., R_f=20 Ω)	7,13,13	4,9,9	11,16,16	12,17,17	4,10,9	17	11.81	J.32
13	A-g (int.)	6,11,11	6,12,13	7,12,12	9,14,14	7,13,15	14	9.72	J.33

In (a,b,c) values in the cells, a: Fault samples needed for fault detection, b &c: Fault samples needed for positive-sequence and negative-sequence trip counters to reach threshold (THRESHLD) respectively.
* R_f: Fault resistance.

[a] F : No. of fault samples; [b] T : Time (ms.); F_J : Reference figure in Appxendix J.

It is concluded that the performance exhibited by the delta-impedance relays is satisfactory and the faults occurring inside and outside the protection zone of the busbars are correctly identified. This validates the feasibility of the proposed busbar protection technique for practical applications. Also, the feasibility of implementing the proposed technique using commercially available hardware components has been established.

7. SUMMARY AND CONCLUSIONS

A power system occasionally experiences faults which can cause extensive damage to the equipment besides injury to personnel. This results in substantial monetary losses to utilities and consumers. A system element should, therefore, be protected from damage due to faults and abnormal operating conditions.

The first chapter of the thesis has described power system protection concepts and developments leading to and including the use of microprocessor-based relays. Majority of the research work in this area has concentrated towards developing suitable algorithms for protecting different power system equipments.

An overview of busbar faults and the essential requirements for a busbar protection scheme has been presented in Chapter 2. Differential protection, conventionally used for protecting busbars, is briefly described. The principle, and limitations of differential relays, and the additional features incorporated in them are outlined.

The advent of digital technology has lead to the introduction of microprocessor-based systems for busbar protection. A literature survey has revealed that very few algorithms for protecting busbars have been proposed in the past. Moreover, these algorithms are adversely affected by ct saturation and ct ratio-mismatch conditions. The reported algorithms use different working principles to achieve correct relay operation even when the cts saturate. Special circuitry and techniques have been used in the past for the purpose. Use of additional circuitry in a protection scheme increases the complexity of a scheme and increases the possibility of incorrect operation due to malfunction of circuit components. Also, an increase in the number of components in a protection scheme increases the total cost.

No algorithm proposed in the past has inherent immunity to ct saturation. Moreover, their correct operation on severe ct saturation is not guaranteed. Also, no

algorithm handles the ct ratio-mismatch satisfactorily. The previously proposed digital algorithms for protecting busbars are reviewed in Chapter 2.

A technique, based on the concept of symmetrical components, has been developed for protecting busbars; the technique has been reported in Chapter 3. It uses fundamental frequency voltage and current phasors computed from quantized samples of bus voltage and quantized samples of currents in the circuits connected to the bus. The computed phasors are used to calculate the positive- and negative-sequence phasors. These sequence-phasors are manipulated to estimate the positive- and negative-sequence impedances. The relay uses the arguments of the impedances to distinguish between the faults in the protection zone from those outside the zone. The proposed technique has been verified for its application to busbars of different configurations. Fault-detection characteristics and an algorithm based on the proposed technique have also been described in Chapter 3.

The impact of ct saturation on the developed technique has been investigated and reported in Chapter 4. Studies have revealed that the magnitudes of the fundamental frequency phasors computed from the outputs of saturated cts are always smaller than the magnitudes of the phasors computed from the outputs of unsaturated cts. Also, the arguments of the phasors computed from the output of saturated cts are greater than the arguments of the phasors computed from the outputs of not-saturated cts. Since the proposed fault-detection technique requires that the arguments of the sequence-impedances lie in the first and/or the third quadrants, there is a wide range in which they can lie. The change in arguments due to ct saturation, therefore, does not affect the decisions made by the technique. This fact proves the ability of the technique to provide correct decisions during ct saturation. The effect of ct ratio-mismatch on the performance of the technique has also been discussed in Chapter 4.

Chapter 5 evaluates the performance of the proposed technique. Fault-data generated from simulations of power system models including the BRADA substation of SaskPower were used for this purpose. The power system were simulated on a SUN SPARC workstation using the simulation software PSCAD. Faults were applied at

different locations in the system. The simulated fault data were pre-processed using anti-aliasing filters.

A program written in ANSI C was used to implement the proposed technique. Test studies were carried out for different types of faults in the system models and for different operating conditions. Also, several busbar configurations were considered in the evaluation process. The impact of ct saturation and ct ratio-mismatch on the performance of the technique were investigated. Test results showed that the proposed technique correctly detects the faults that occur inside and outside the busbar protection zone. Also, the stability of the proposed technique during ct saturation and ct ratio-mismatch has been verified.

It has been shown that the impedance seen by a relay when a ct saturates is higher in magnitude and lower in argument than that observed if the ct does not saturate. However, the impedances remain well within the fault-detection zones. This confirmed the theoretical basis developed in Chapter 4. Test studies have shown that the decisions made by the technique are not affected by mismatch of ct ratios. This results from the fact that the impedances calculated from the data obtained by the relays included in the protection scheme are independent of each other. This has made the proposed technique inherently immune to mismatch of the ct ratios.

The proposed technique has been implemented using commercially available general-purpose relay hardware. The hardware and the software designed for implementing the proposed fault-detection technique has been described in Chapter 6. The testing of individual hardware and software components, involved in the implementation, have been described in the chapter as well. The individual relays of the busbar protection system have been tested by playing back the fault data using a Real Time Playback (RTP) Simulator. Test results have also been reported in Chapter 6. Numerous tests have shown that the proposed technique is capable of detecting faults in the busbar protection zone and provides trip decisions with operating times ranging from 9.0 ms to 13.5 ms.

The objective of this research was to develop and test a microprocessor-based system for protecting busbars. The developed system should be stable during ct saturation and ct ratio-mismatch conditions. It should also be implementable in microprocessor-based relay. The work reported in this thesis shows that the objectives have been successfully met. Specifically, this thesis has made the following contributions.

1. A technique for protecting busbars has been proposed and an algorithm based on the technique has been developed. While phase voltages and currents are used to detect faults, parameters of the power system are not used. Only the arguments of the sequence-impedances computed by the relays are used to make decisions.

2. The effects of ct saturation and ct ratio-mismatches on the proposed technique have been described and evaluated. It has been shown that the technique is not affected adversely by ct saturation and ct ratio-mismatches.

3. Viability of the proposed technique to provide microprocessor-based protection for busbars has been demonstrated by implementing the proposed technique in a prototype.

REFERENCES

[1]. Warrington, A. R. van C., *Protective Relays-Their Theory and Practice*, Chapman and Hall Ltd., London, 1979.

[2]. Madhava Rao, T. S., *Power System Protection-Static Relays*, McGraw Hill Book Company, New York, 1981.

[3]. Sachdev, M. S. (Course Coordinator), "Advancements in Microprocessor Based Protection and Communication", IEEE Tutorial Course, *IEEE Power Engineering Society*, NJ, 1996.

[4]. Sachdev, M. S. (Course Coordinator), "Microprocessor Relays and Protection Systems", IEEE Tutorial Course (88EH0269-1-PWR), *IEEE Power Engineering Society*, NJ, 1987.

[5]. Sachdev, M. S. (Course Coordinator), "Computer Relaying", IEEE Tutorial Course (79EH0148-7-PWR), *IEEE Power Engineering Society*, NJ, 1979.

[6]. Rockefeller, G. D., "Fault Protection with a Digital Computer", *Trans. IEEE, Power Apparatus and Systems*, Vol. PAS-88, No. 4, April 1969, pp. 438-461.

[7]. Gilchrist, G. B., Rockefeller, G. D. and Udren, E. A., "High-Speed Distance Relaying Using a Digital Computer, Part I-System Description", *IEEE Trans. on Power Apparatus and Systems*, Vol. 91, No. 3, May/June 1972, pp. 1235-1243.

[8]. Rockefeller, G. D. and Udren, E. A., "High-Speed Distance Relaying Using a Digital Computer, Part-II", *IEEE Trans. on Power Apparatus and Systems*, Vol. 91, No. 3, May/June 1972, pp. 1244-1258.

[9]. Phadke, A. G., Ibrahim, M. and Hlibka, T., "Computers in EHV Substation: Programming Considerations and Operating Experience", *CIGRE Study Committee*, No. 34 Colloquium, Philadelphia, Oct. 1975.

[10]. Phadke, A. G., Ibrahim, M. and Hlibka, T., "A Digital Computer System for EHV Substations: Analysis and Field Tests", *IEEE Trans. on Power Apparatus and Systems*, Vol. 95, No. 1, Jan./Feb. 1976, pp. 291-301.

[11]. Breingan, W. D., Chen, M. M. and Gallan, T. F., "The Laboratory Investigation of a Digital System for the Protection of Transmission Lines", *IEEE Trans. on Power Apparatus and Systems*, Vol. 98, No. 2, Mar./Apr. 1979, pp. 350-368.

[12]. Gallan, T. F., Van Name, J. M. and Eskie, E. J., "500 kV Faults Staged to Test

Experimental Relaying System", *Electric Light & Power*, Vol. 57, No. 5, May 1979, pp. 44.

[13]. Gallan, T. F., Chen, M. M. and Breingan, W. D., "A Digital System for Directional-Comparison Relaying", *IEEE Trans. on Power Apparatus and Systems*, Vol. 98, No. 3, May/June 1979, pp. 948-956.

[14]. Mann, B. J., "Real Time Computer Calculation of the Impedance of a Faulted Single-Phase Line", *IE Australia*, Vol. EE4, March 1969, pp. 26-28.

[15]. Ramamoorty, M., "A Note on Impedance Measurement Using Digital Computers", *IEEE-IERE Proceedings, Institute of Electronic and Radio Engineers*, Bangalore, India, Nov.-Dec. 1971, Vol. 9, No. 6, pp. 243-247.

[16]. Westinghouse Electric Corporation, "Type MDF Microprocessor Frequency Relay", *Bulletin No.* I. L. 41-505A.

[17]. Sachdev, M. S. and Agarwal, R., "Accurate Fault-Location Estimates from Digital Impedance Relay Measurements", Developments in Power System Protection, *IEE Conference* Publication No. 249, London, April 1985, pp. 180-184.

[18]. Kondow, R., Sugiyama, Y. and Yamada, M., "Microprocessor-Based Fault Locator", Developments in Power System Protection, *IEE Conference* Publication No. 249, London, April 1985, pp. 188-192.

[19]. Walker, L. N. and Ogden, A. D., "Computer Control Unit for Power System Substation", paper presented at *Midwest Power Symposium*, 1968.

[20]. Walker, L. N., Ogden, A. D., Ott, G. E. and Tudor, J. R., "Implementation of High Frequency Transient Fault Detector", Paper No. 70CP 140-PWR, *IEEE Winter Power Meeting*, New York, January 1970.

[21]. Walker, L. N., Ogden, A. D., Ott, G. E. and Tudor, J. R., "Special Purpose Digital Computer Requirements for Power System Substation Needs", Paper No. 70CP 142-PWR, *IEEE Winter Power Meeting*, New York, January 1970.

[22]. Cory, B. J., "Protective Relaying by Digital computer", *IEEE Conference on Systems, Networks and Computers*, Mexico, January 1971.

[23]. Cory, B. J., Dromey, G. and Murray, B. E., "Digital Systems for Protection", *CIGRE* 1976, Report No. 34-08.

[24]. Hope, G. S. and Jura, S. J., "Detecting Transmission Line Abnormalities by Computer", *Instrument Technology*, February 1971, pp. 39-45.

[25]. Hope, G. S., Bell, D. H. and Jura, S. J., "Development of a Computer Interface for Transmission Line Protection", *Proceedings of the 7th IEEE PICA Conference*, 1971,

pp. 486-491.

[26]. Sachdev, M. S. and Wind, D. W., "Trends in Power System Protection with Real-Time Digital Computers", *Transactions of the Canadian Electrical Association*, Vol. 11, No. 3, 1972, Paper No. 72-SP-143, pp. 1-12.

[27]. Sachdev, M. S. and Wind, D. W., "An On-Line Digital Computer Approach for Generator Differential Protection", *Transactions of the Canadian Electrical Association*, Paper No. 73-SP-149, Vol. 12, No. 3, 1973, pp. 1-6.

[28]. Sachdev, M. S. and Wind, D. W., "Generator Differential Protection Using a Hybrid Computer", *IEEE Transactions on Power Apparatus and Systems*, Vol. 92, No. 6, Nov./Dec. 1973, pp. 2063-2072.

[29]. McLaren, P. G. and Redfern, M. A., "Fourier-Series Techniques Applied to Distance Protection", *Proceedings of the IEE (London)*, Vol. 122, No. 11, Nov. 1975, pp. 1301-1305.

[30]. Anderson, P. M., *Power System Protection*, McGraw-Hill, IEEE Press Power Engineering Series, 1999, Piscataway, NJ, USA.

[31]. GEC Measurements, *Protective Relays Application Guide*, General Electric Company p.l.c. of England, 1975.

[32]. Blackburn, J. Lewis, *Protective Relaying-Principles and Applications*, Marcel Dekker Inc., New York and Basel, 1987.

[33]. Kojovic, Ljubomir, "Current Transformer Application Considerations and Transient Behavior Analysis Using EMTP/ATP", *Systems Engineering Reference Bulletin SE9406*, Cooper Power Systems, Franksville, WI, November 1994.

[34]. Bean, Richard L. Jr., Nocholas Chackan, Moore, Harold R., Wentz, Edward C., *Transformers for the Electric Power Industry*, Westinghouse Electric Corporation, Power Transformer Division, 1979.

[35]. Mason, C. R., *The Art and Science of Protective Relaying*, General Electric Company, NY, 1956.

[36]. Peck, D. M., Nygaard, B. and Wadelius, K., "A New Numerical Busbar Protection System with Bay Oriented Structure", *5th Int. Conf. On Developments in Power System Protection*, IEE Pub. No. 368, 1993, pp. 228-231.

[37]. Forford, T. and Linders, J. R., "A Half-cycle Bus Differential Relay and its Application", *IEEE PES Winter Meeting*, New York, N. Y., Jan. 27-Feb. 01, 1974, pp. 1110-1120.

[38]. Andow, F., Suga, N., Murakami, Y. and Inamura, K., "Microprocessor-Based

Busbar Protection Relay", *5th Int. Conf. On Developments in Power System Protection, IEE* Pub. No. 368, 1993, pp. 103-106.

[39]. Royle, J. B. and Hill, A., "Low Impedance Biased Differential Busbar Protection for Application to Busbars of Widely Differing Configurations", *4th Int. Conf. On Developments in Power System Protection, IEE* Pub. No. 302, 1989, pp. 40-44.

[40]. Kumar, A. and Hansen, P., "Digital Bus-Zone Protection", *IEEE Computer Applications in Power*, Vol. 6, No. 4, 1993, pp. 29-34.

[41]. Sidhu, T. S., Gill, H. S. and Sachdev, M. S., "A New Approach to Busbar Protection", Proceedings of the *IEEE, Region 10 Conference (TENCON '98)*, Dec. 17-19, 1998, New Delhi, India, pp. 432-435.

[42]. McLaren, P. G., et al., "New Directional Element for Numerical Distance Relays", *IEEE Trans. on Power Delivery*, Vol. 10, No. 2, 1995, pp. 666-75.

[43]. Sidhu, T. S., Sunga, B. and Sachdev, M. S., "A Digital Technique for Stator Winding Protection of Synchronous Generators", *Electric Power Systems Research*, Vol. 36, 1996, pp. 45-55.

[44]. Sidhu, T. S., Gill, H. S. and Sachdev, M. S., "A Power Transformer Protection Technique With Stability During Current Transformer Saturation and Ratio-Mismatch Conditions", *IEEE Trans. on Power Delivery*, Vol.14, No. 3, July 1999, pp.798-804.

[45]. Sidhu, T. S., Gill, H. S. and Sachdev, M. S., "A Transformer Protection Technique With Immunity to CT Saturation and Ratio-Mismatch Conditions", *Canadian Conference of Electrical and Computer Engineering*, Waterloo, Ontario, May 24-28, Vol. I, 1998, pp. 285-288.

[46]. Sidhu, T. S., Gill, H. S. and Sachdev, M. S., "A Numerical Technique Based on Symmetrical Components for Protecting Three-winding Transformers", ID# 98-327-1, accepted for publication in the *Electric Power Systems Research.*

[47]. Sachdev, M. S. and Baribeau, M. A., "A New Algorithm for Digital Impedance Relays", *IEEE Trans. on Power Apparatus and Systems*, Vol. 98, No. 6, Nov./Dec. 1979, pp. 2232-40.

[48]. Oppenheim, Alan V. and Schafer, Ronald W., *Digital Signal Processing*, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1975.

[49]. Manitoba HVDC Research Centre, EMTDC *User's Manual* version 2.02, Winnipeg, Manitoba, 1986.

[50]. FTP Site:ftp://ftp.ee.umanitoba.ca/pub/PSCAD/PSCAD_ EMTDC /outgoing/ct_cvt/.

[51]. Sidhu, T. S., Sachdev, M. S. and Das, R., "Modern Relays: Research and Teaching Using PCs", *IEEE Computer Applications in Power*, Vol. 10, No. 2, April 1997, pp. 50-55.

[52]. National Semiconductor Corporation, *Linear Databook 2*, 1987.

[53]. Texas Instruments Inc., *Linear Circuits, Operational Amplifiers, Databook*, Volume 1, 1992.

[54]. Spectrum Signal Processing Inc., *4 Channel Analog I/O Board User's Manual: Version 2.1*, 1988.

[55]. Spectrum Signal Processing Inc., *PC/C31 Real Time Application Board Technical Reference Manual: Version 1.06*, 1995.

[56]. Spectrum Signal Processing Inc., *PC/C31 Board User Guide: Version 1.04*, 1995.

[57]. Texas Instruments Inc., *TMS320C3x User's Guide: Revision F*, 1992.

[58]. Microsoft Corporation, *Microsoft visual Basic Programming system for Windows, Programmer's Guide and Language Reference: Version 3.0*, 1993.

[59]. Spectrum Signal Processing Inc., *PC/C31 Intelligent Interface Library Windows Support Software User Manual: Version 1.01*, 1995.

[60]. Doble Active Sources™, *Model FDF Dynamic Frequency Source*, Watertown, MA, U.S.A., 1982.

[61]. Spectrum Signal Processing Inc., *MPC View for PC/C31, User Manual: Version 1.01*, 1995.

[62]. Texas Instruments Inc., *Digital Signal Processing Applications with the TMS320C30 Evaluation Module, Selected Application Notes, Microprocessor Development systems: Revision A*, 1991.

[63]. Texas Instruments Inc., *TMS320C3x C Source Debugger User's Guide, Microprocessor Development systems: Revision F*, 1991.

[64]. Manitoba HVDC Research Centre, *Real Time Playback (RTP) and PSCAD/EMTDC Recorder Component User's Guide*, Winnipeg, 1997.

[65]. De Haas, J., Bielders, M. J. J., Sidler H. F. A., Vos, C. W. M. and Zantinge, J. F., "Comparative Analysis of Different Types of Substation Configurations", *CIGRE International Conference on Large High Voltage Electric Systems*, Article No. 23-11, 1984, pp. 1-6.

[66]. Stevenson, William D. Jr., *Elements of Power System Analysis*, McGrawhill, New

York, 1982.

[67]. Westinghouse Electric Corporation, *Electrical Transmission and Distribution Reference Book*, East Pittsburgh, PA, Fourth Edition, 1950, Line 23 (D) of Boston Edison Company, page 792.

[68]. Swift, G. W., "The Spectra of Fault-Induced Transients", *IEEE Transactions on Power Apparatus and Systems*, Vol. PAS-98, No. 3, May/June 1979, pp. 940-947.

[69]. IEEE Power System Relaying Committee, "Fault Induced Wave Distortion of Interest to Relay Engineers", *IEEE Transactions on Power Apparatus and Systems*, Vol. PAS-104, December 1985, pp. 3574-3584.

[70]. Texas Instruments Inc., *TMS320C30 Floating-Point DSP Optimizing C Compiler, Microprocessor Development systems, User's Guide: Revision A*, 1991.

[71]. Texas Instruments Inc., *TMS320C30 Floating-Point DSP Assembly Language Tools, Microprocessor Development systems, User's Guide: Revision A*, 1991.

Appendix A. BUSBAR ARRANGEMENTS

Substations differ in configurations based on operational considerations. Whether single or multiple busbars are necessary will depend mainly on how the system is operated and on the need for sectionalizing, to avoid excessive breaking capacities. Account is also taken of the need to isolate parts of the installations for purposes of cleaning and maintenance, and also of future extensions. Major substation configurations and their associated features are described as under.

Single busbars

Single busbar configuration is suitable for smaller installations (most dc switchboards, small ac substations and some generating stations). Figure A.1 shows a typical single busbar substation. It uses a single set of busbars. All generators, feeders and transformer circuits are connected to it. A sectionalizer allows the station to be split into two separate parts and the parts to be disconnected for maintenance purposes. This is also the least expensive scheme.

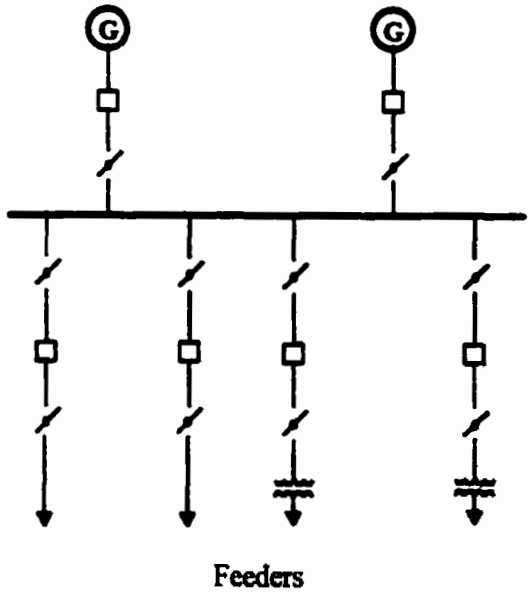


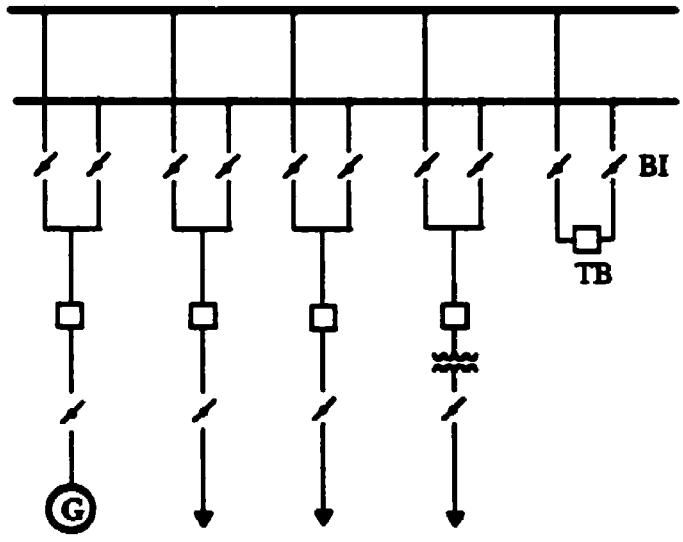
Figure A.1. A typical single busbar system.

Some of its disadvantages include shutdown of the entire substation when the busbar or a circuit-breaker failure occurs, difficulty in performing maintenance and need for total shutdown when the substation is to be extended.

Duplicate busbar system

Major substations are usually equipped with duplicate busbars to increase flexibility during the operation of the substation and for doing maintenance on the equipment. Normally, one set of busbars is in use while the other remains available for use in the event of a busbar fault in the substation. This scheme includes a busbar-coupler circuit breaker and two isolators. Each incoming and outgoing feeder is connected to both busbars by a circuit breaker and two isolators as shown in Figure A.2.

In this scheme, an appropriate sequence of operations must be used to transfer circuits from one set of busbars to the other. The busbar-coupler circuit breaker is used to synchronize the systems connected to these busbars. The isolators are used to select the busbars and to disconnect the circuit breaker for maintenance.



TB = Busbar-tie Breaker

BI = Busbar-tie Isolator

Figure A.2. A typical duplicate busbar system.

This configuration facilitates maintenance on busbars, testing and commissioning of new feeders, and operating an existing feeder at a different voltage to compensate for abnormal voltage drops. The disadvantage of this scheme is that all the circuits connected to a busbar are interrupted in the event of a busbar fault.

Breaker-and-a-half ($1\frac{1}{2}$) *system*

As the name implies, it requires one and a half circuit breakers per circuit because each pair of circuits is controlled by three circuit breakers. All breakers are normally closed. Uninterrupted supply is thus maintained even if one busbar fails. The branches can be connected by a linking breaker as shown in Figure A.3. The flexibility and reliability are high but relaying and reclosing are complex to implement.

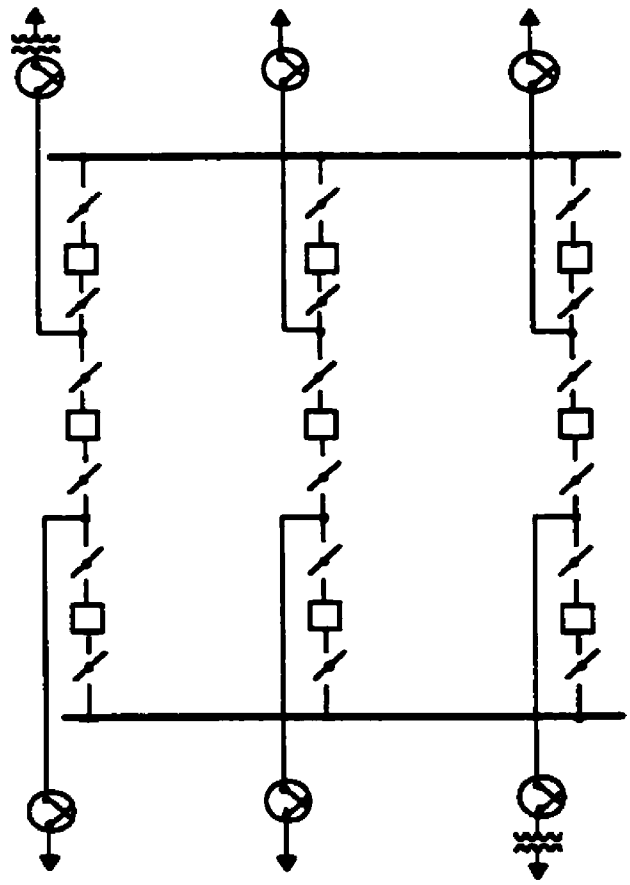


Figure A.3. A typical breaker-and-a-half system.

Ring busbars

Some major substations use the mesh arrangement, called a ring busbar, as shown in Figure A.4. Each branch requires only one circuit-breaker, and yet each breaker can be isolated without interrupting the power supply in the outgoing feeders. to take a circuit out of service, two adjacent circuit breakers must be opened. This scheme has a low initial and ultimate cost and provides flexibility in operation for maintenance of breakers. The arrangement, however, makes protective relaying and automatic reclosing complex. The ring busbar layout is often used as the first stage of $1\frac{1}{2}$ breaker configurations.

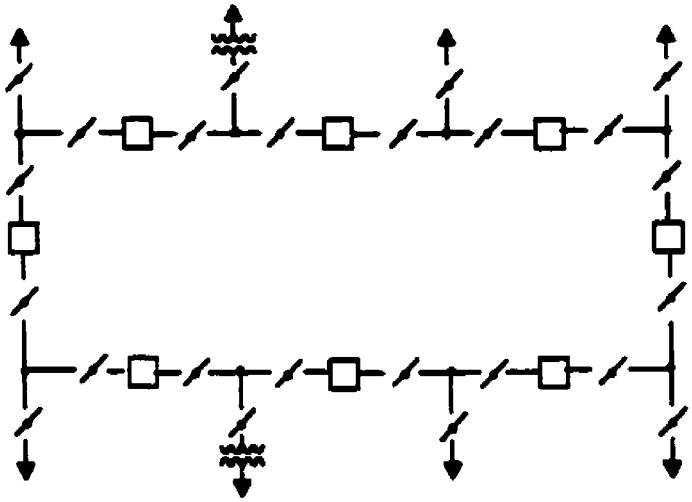


Figure A.4. A typical mesh substation.

Two circuit-breaker system

Used in major substations, this scheme has two circuit-breakers in each circuit. There is no bus-coupler circuit-breaker. This arrangement, also called a double-busbar-double-breaker scheme, is shown in Figure A.5. It is considered to be one of the best suited configurations for high voltage substations [65] but also is the most expensive alternative. Use of two circuit-breakers increases operational flexibility. That is, since each circuit has two circuit breakers, it can be connected to either busbar. Any busbar and any circuit breaker can be taken out of service for maintenance without interrupting connection to the feeders.

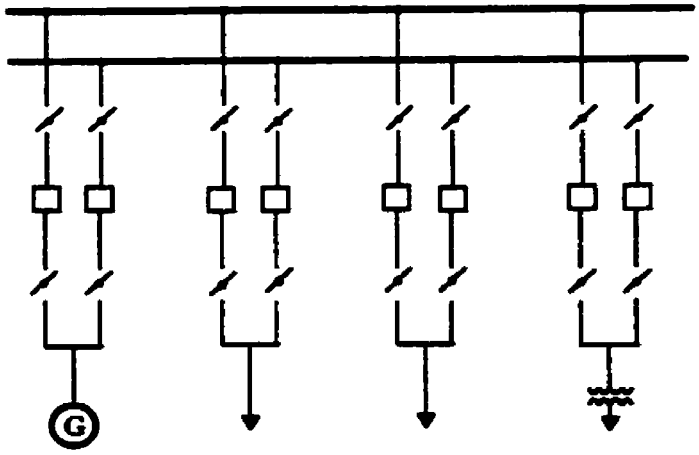


Figure A.5. A typical two-circuit breaker system.

Multiple busbar system

This system, shown in Figure A.6, consists of more than two sets of busbars. This layout is frequently provided with a bypass bus. Any busbar can be isolated for maintenance. A circuit can be readily transferred from one busbar to another using the busbar-tie breaker and busbar selecting switches. It is used for vital installations feeding electrically separate networks or if rapid sectionalizing is required in the event of a fault to limit the short-circuit power. However, it is not a popular scheme because it is not cost effective and its performance does not surpass the two-circuit-breaker, breaker-and-a-half and mesh arrangements. In this scheme, a circuit breaker cannot be serviced without interrupting power supply to a line.

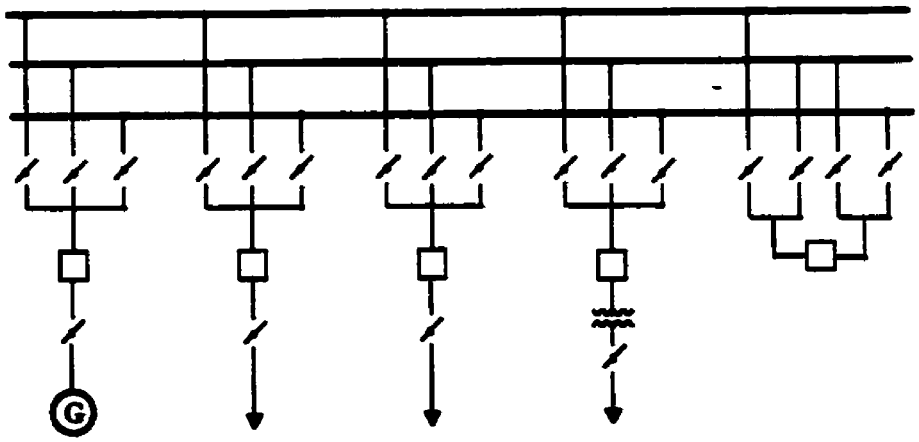


Figure A.6. A typical multiple busbar system.

Appendix B. SYMMETRICAL COMPONENTS & SEQUENCE-NETWORKS

Symmetrical components

The method of symmetrical components was first proposed by C.L. Fortescue and has been found very useful in analyzing unbalanced polyphase circuits. The concept of symmetrical components allows decomposition of any unbalanced 3-phase system of vectors (whether representing currents or voltages) into three balanced systems of vectors which are called its 'symmetrical components'. The balanced set of phasors are-positive-sequence, negative-sequence and zero-sequence components. Figure B.1 shows the relation between the unbalanced set of phasors and the corresponding symmetrical components.

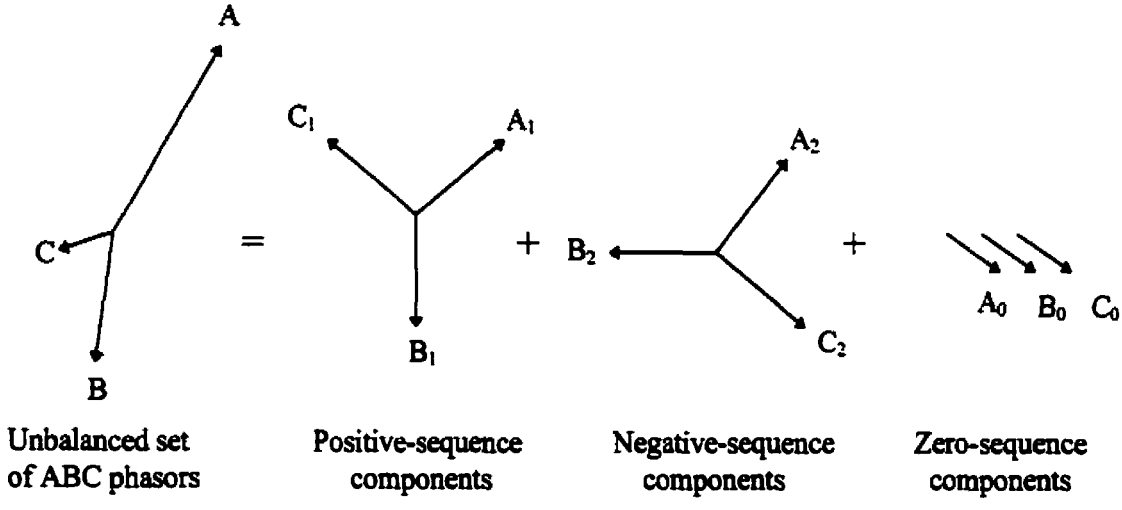


Figure B.1. Decomposition of an unbalanced set of ABC phasors in symmetrical components.

Positive-sequence components are the balanced systems of 3-phase vectors having the same phase sequence as the unbalanced set unlike the negative-sequence components which have an opposite phase sequence from the original unbalanced set of phasors. Zero-sequence components are equal in magnitude and are in phase with each other.

In equation form, symmetrical components for an unbalanced set of voltages can be written as

$$V_a = V_{a1} + V_{a2} + V_{a0}$$

$$V_b = V_{b1} + V_{b2} + V_{b0}$$

$$V_c = V_{c1} + V_{c2} + V_{c0} \quad . \tag{B.1}$$

Also,

$$V_{b1} = a^2 V_{a1}\ ,\ V_{c1} = a V_{a1}\ ,\ V_{b2} = a V_{a2}\ ,\ V_{c2} = a^2 V_{a2}\ ,\ V_{b0} = V_{c0} = V_{a0} \tag{B.2}$$

where:

- a is an operator that causes a phase shift of 120 degrees and is defined as -0.5 + j 0.866,
- a^2 is an operator that causes a phase shift of 240 degrees and is defined as -0.5 - j 0.866.

From Equations (B.1) and (B.2), it follows that

$$\begin{aligned} V_a &= V_{a1} + V_{a2} + V_{a0} \\ V_b &= a^2 V_{a1} + a V_{a2} + V_{a0} \\ V_c &= a V_{a1} + a^2 V_{a2} + V_{a0} \quad . \end{aligned} \tag{B.3}$$

In matrix form,

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} V_{a0} \\ V_{a1} \\ V_{a2} \end{bmatrix}$$

The symmetrical components can, thus, be represented in terms of the unbalanced set of phasors as

$$\begin{bmatrix} V_{a0} \\ V_{a1} \\ V_{a2} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad . \tag{B.4}$$

Sequence-networks

The voltage drop caused by current of a particular sequence depends upon the impedance offered to the current of that sequence. Therefore, sequence-impedances are termed positive-, negative- and zero-sequence impedance depending upon the respective sequence currents [66].

The analysis of an unsymmetrical fault in a symmetrical system consists of finding the symmetrical components of the unbalanced currents flowing in the circuit. Since the sequence current of one type differs from the other, and causes voltage drop of like sequence only, it may be considered to flow in an independent network composed of the impedances to the current of that particular sequence only. The single-phase equivalent circuit comprising impedances to current of one sequence type only is called the sequence-network for that particular sequence. This network shows all the paths for the flow of current of that sequence in a system.

The method of symmetrical components, thus, involves determination of sequence impedances to form sequence-networks and their appropriate connections to analyze a fault.

Appendix C. LEAST ERROR SQUARES ALGORITHM

Sachdev and Baribeau [47] described the Least Error Squares (LES) approach for developing a digital filter which explicitly takes account of the decaying d.c. components in the system voltages and currents. This curve-fitting technique is based on minimizing the mean-square error between the actual and assumed waveforms. The technique uses the coefficients of the designed filter to compute the real and imaginary components of the voltage and current phasors. In designing the LES filter, the power system currents and voltages are modeled as a combination of an exponentially decaying dc component, a fundamental frequency component and harmonics of specified order.

Consider that the waveform of a voltage can be modeled as

$$v(t) = A_0 e^{-t/\tau} + \sum_{n=1}^{N} A_n \sin(n\omega_0 t + \theta_n). \qquad (C.1)$$

where:

- $v(t)$ is the instantaneous value of the voltage at any time t,
- τ is the time constant of the decaying dc component,
- N is the highest order harmonic component present in the voltage,
- ω_0 is the fundamental frequency of system in radians/seconds,
- A_0 is the initial value of the dc offset at time t=0,
- A_n is the peak value of the n^{th} harmonic component, and
- θ_n is the phase angle of the n^{th} harmonic component.

The Taylor series expansion for the decaying dc component gives

$$e^{(-t/\tau)} = 1 - \left(\frac{t}{\tau}\right) + \left(\frac{1}{2}\right)\left(\frac{t}{\tau}\right)^2 - \left(\frac{1}{6}\right)\left(\frac{t}{\tau}\right)^3 + \ldots \qquad (C.2)$$

Applying the trigonometric identity sin(A+B)=sinAcosB+cosAsinB and using the first two terms of the Taylor series expansion of the decaying dc component, Equation (C.1) becomes

$$v(t) = A_0 - \left(\frac{A_0}{\tau}\right)t + \sum_{n=1}^{N} A_n\left[\sin(n\omega_0 t)\cos\theta_n + \cos(n\omega_0 t)\sin\theta_n\right]. \qquad (C.3)$$

If the fourth and higher order harmonics are assumed to be removed by the anti-aliasing filter, and $t = t_1$, Equation (C.3) becomes

$$\begin{aligned} v(t_1) = A_0 - \left(\frac{A_0}{\tau}\right)t_1 &+ (A_1\cos\theta_1)\sin(\omega_0 t_1) + (A_1\sin\theta_1)\cos(\omega_0 t_1) + \\ &(A_2\cos\theta_2)\sin(2\omega_0 t_1) + (A_2\sin\theta_2)\cos(2\omega_0 t_1) + \\ &(A_3\cos\theta_3)\sin(3\omega_0 t_1) + (A_3\sin\theta_3)\cos(3\omega_0 t_1). \end{aligned} \qquad (C.4)$$

This equation can be expressed as

$$v(t_1) = a_{11}x_1 + a_{12}x_2 + a_{13}x_3 + a_{14}x_4 + a_{15}x_5 + a_{16}x_6 + a_{17}x_7 + a_{18}x_8. \qquad (C.5)$$

where:

$x_1 = A_0$, $x_2 = -\left(\frac{A_0}{\tau}\right)$, $x_3 = A_1\cos\theta_1$, $x_4 = A_1\sin\theta_1$, $x_5 = A_2\cos\theta_2$, $x_6 = A_2\sin\theta_2$,

$x_7 = A_3\cos\theta_3$, $x_8 = A_3\sin\theta_3$, and

$a_{11}=1$, $a_{12}=t_1$, $a_{13}=\sin(\omega_0 t_1)$, $a_{14}=\cos(\omega_0 t_1)$, $a_{15}=\sin(2\omega_0 t_1)$, $a_{16}=\cos(2\omega_0 t_1)$,

$a_{17}=\sin(3\omega_0 t_1)$, $a_{18}=\cos(3\omega_0 t_1)$.

The voltage signal is sampled at intervals of Δt s. Equation (C.5) can be rewritten in the following form by substituting $t_1 = \Delta t, 2\Delta t, \ldots\ldots, m\Delta t$ as follows.

$$v(\Delta t) = a_{11}x_1 + a_{12}x_2 + a_{13}x_3 + a_{14}x_4 + a_{15}x_5 + a_{16}x_6 + a_{17}x_7 + a_{18}x_8$$

$$v(2\Delta t) = a_{21}x_1 + a_{22}x_2 + a_{23}x_3 + a_{24}x_4 + a_{25}x_5 + a_{26}x_6 + a_{27}x_7 + a_{28}x_8$$

$$\vdots$$

$$v(m\Delta t) = a_{m1}x_1 + a_{m2}x_2 + a_{m3}x_3 + a_{m4}x_4 + a_{m5}x_5 + a_{m6}x_6 + a_{m7}x_7 + a_{m8}x_8. \qquad (C.6)$$

The a-coefficients can be redefined as follows:

$a_{m1}=1$, $a_{m2}=m\Delta t$, $a_{m3}=\sin(\omega_0 m\Delta t)$, $a_{m4}=\cos(\omega_0 m\Delta t)$, $a_{m5}=\sin(2\omega_0 m\Delta t)$,

$a_{m6}=\cos(2\omega_0 m\Delta t)$, $a_{m7}=\sin(3\omega_0 m\Delta t)$, $a_{m8}=\cos(3\omega_0 m\Delta t)$.

If S voltage samples are expressed as equations and S>8, the resulting equations can be written in the matrix form as

$$\underset{Sx8}{[A]}\ \underset{8x1}{[x]} = \underset{Sx1}{[v]}. \tag{C.7}$$

The unknowns, [x], can be calculated as follows

$$[x]=[A]^{+}[v]. \tag{C.8}$$

where $[A]^{+}$ is the left pseudo-inverse of [A] and is given by

$$[A]^{+} = [\,[A^{T}]\,[A]\,]^{-1}\,[A^{T}]. \tag{C.9}$$

The elements of the rows of $[A]^{+}$ are the coefficients of the LES filter that can be used for estimating the real and imaginary components of the fundamental frequency and harmonic frequency phasors of the voltages. These elements can be computed a priori in the off-line mode because Δt is known. The peak value of the fundamental frequency component can then be calculated by using the equation

$$V_1 = \sqrt{x_3^{\,2} + x_4^{\,2}} \tag{C.10}$$

where x_3 and x_4 are the sum of the multiplications of the elements of the 3rd and 4th rows of $[A]^{+}$ and the voltage samples. Similar procedure can be used for computing the fundamental frequency components of the currents. A one cycle LES algorithm attenuates high-frequency components, noise and the decaying component.

For the work reported in this thesis, sampling frequency of 1440 Hz was used. The time instant coinciding with the thirteenth sample was considered to be zero. The filter coefficients, for estimating the real and imaginary components of the fundamental frequency phasors of voltages and currents, are given in Table C.1. The real and imaginary components of the fundamental frequency phasor are calculated by multiplying the coefficients with the samples. The transfer function of the cosine and sine filters in the z-plane is given by

$$H(z) = C[-12]z^{-12} + C[-11]z^{-11} + C[-10]z^{-10} + C[-9]z^{-9} + C[-8]z^{-8} + C[-7]z^{-7} + C[-6]z^{-6} + C[-5]z^{-5} + C[-4]z^{-4} + C[-3]z^{-3} + C[-2]z^{-2} + C[-1]z^{-1} + C[0]z^{0} + C[1]z^{1} + C[2]z^{2} + C[3]z^{3} + C[4]z^{4} + C[5]z^{5} + C[6]z^{6} + C[7]z^{7} + C[8]z^{8} + C[9]z^{9} + C[10]z^{10} + C[11]z^{11} + C[12]z^{12} \quad (C.11)$$

The magnitude response of the LES algorithm is obtained by using the numerical values of the filter coefficients and substituting z with $e^{j\omega\Delta t}$ in Equation C.11 and evaluating the resulting equation. The responses are shown in Figure C.1.

Table C.1. The filter coefficients for a 25 point LES filter based on a sampling rate of 1440 Hz.

Coefficient Number	Cosine Coefficients	Sine Coefficients
C[-12]	0.316490	-0.042553
C[-11]	-0.021568	-0.078721
C[-10]	-0.041667	-0.073942
C[-9]	-0.058926	-0.057153
C[-8]	-0.072169	-0.043440
C[-7]	-0.080494	-0.019795
C[-6]	-0.083333	-0.001773
C[-5]	-0.080494	0.023341
C[-4]	-0.072169	0.039894
C[-3]	-0.058926	0.060699
C[-2]	-0.041667	0.070396
C[-1]	-0.021568	0.082267
C[0]	0.000000	0.081560
C[1]	0.021568	0.082267
C[2]	0.041667	0.070396
C[3]	0.058926	0.060699
C[4]	0.072169	0.039894
C[5]	0.080494	0.023341
C[6]	0.083333	-0.001773
C[7]	0.080494	-0.019795
C[8]	0.072169	-0.043440
C[9]	0.058926	-0.057153
C[10]	0.041667	-0.073942
C[11]	0.021568	-0.078721
C[12]	-0.316490	-0.042553

It is observed from the frequency response that the filters attenuate components of higher frequencies.

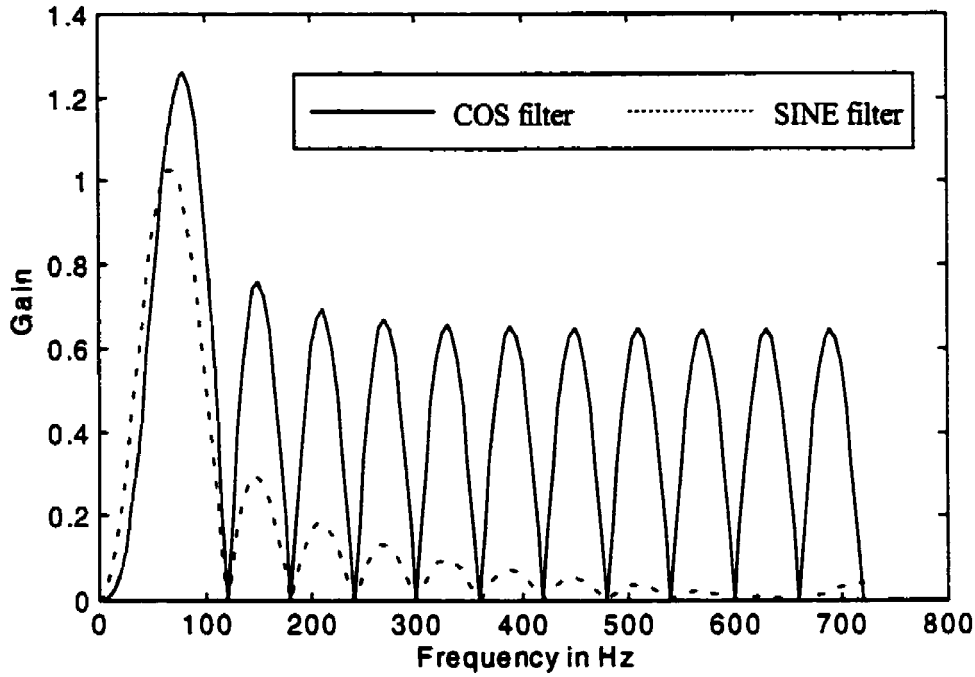


Figure C.1. Frequency response of least error squares filter having a data window of 25 samples.

Appendix D. SYSTEM DATA

As described in Chapter 5, a model system model and an existing substation of the SaskPower were used for verifying the performance of the proposed technique. This appendix presents a more detailed outline of these system configurations and the data of various system parameters used in these models. All parameters are based on a rated three-phase base MVA of 100.

D.1. Model system

Figures D.1 to D.4 shows the model systems simulated using the PSCAD/EMTDC software. Four different configurations including ring, single, double and breaker-and-half were considered. Also, two different operating conditions of the system were considered utilizing load flow technique. The electrical parameters of various components involved in the model system are given in Tables D.1 to D.7.

Table D.1. Equivalent source data.

Parameter	Source S1	Source S2	Source S3
Rated volts (L-L, RMS) (kV)	132.0	132.0	345.0
Initial phase (deg.)	10.9878	10.6407	0.0
Positive-sequence RRL			
Resistance (series) (ohms)	0.1742	0.1742	1.1903
Resistance (parallel) (ohms)	5000.0	5000.0	5000.0
Inductance (parallel) (H)	0.0139	0.0139	0.0947
Zero-sequence RL			
Resistance (parallel) (ohms)	50.0e+06	50.0e+06	50.0e+06
Inductance (parallel) (H)	0.0035	0.0035	0.0237

Table D.2. Load data.

Motor load (M)		Static load (L)	
Load MVA (MVA)	84.0	Load MVA (MVA)	6.3
Rated RMS phase voltage (kV)	7.967	L-L voltage, RMS (kV)	13.8
Horse power (H.P.)	100000.0	Resistive component (ohms)	0.1028
		Reactive component (H)	0.0002

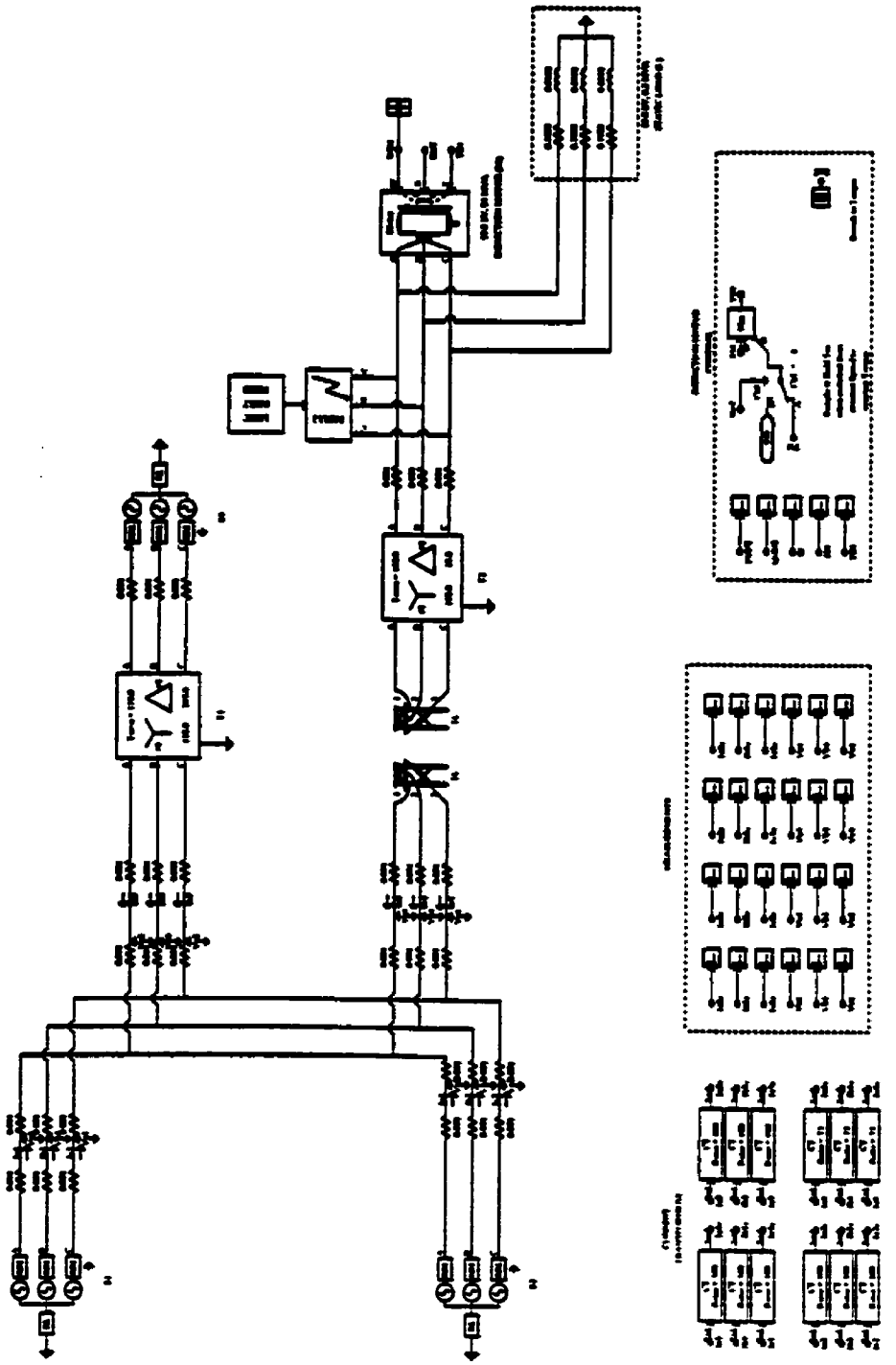


Figure D.1. Single busbar configuration of the model system in PSCAD.

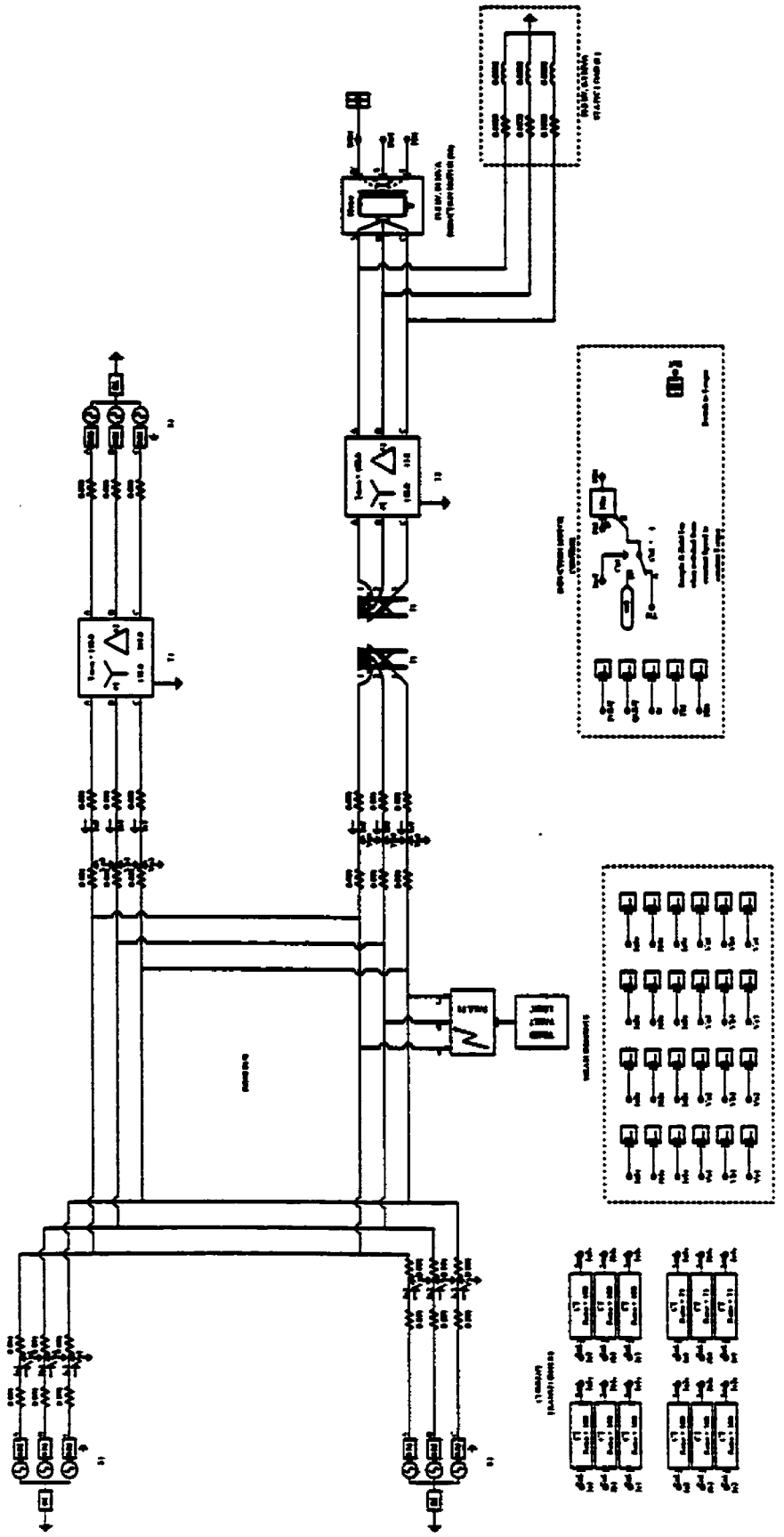


Figure D.2. Ring busbar configuration of the model system in PSCAD.

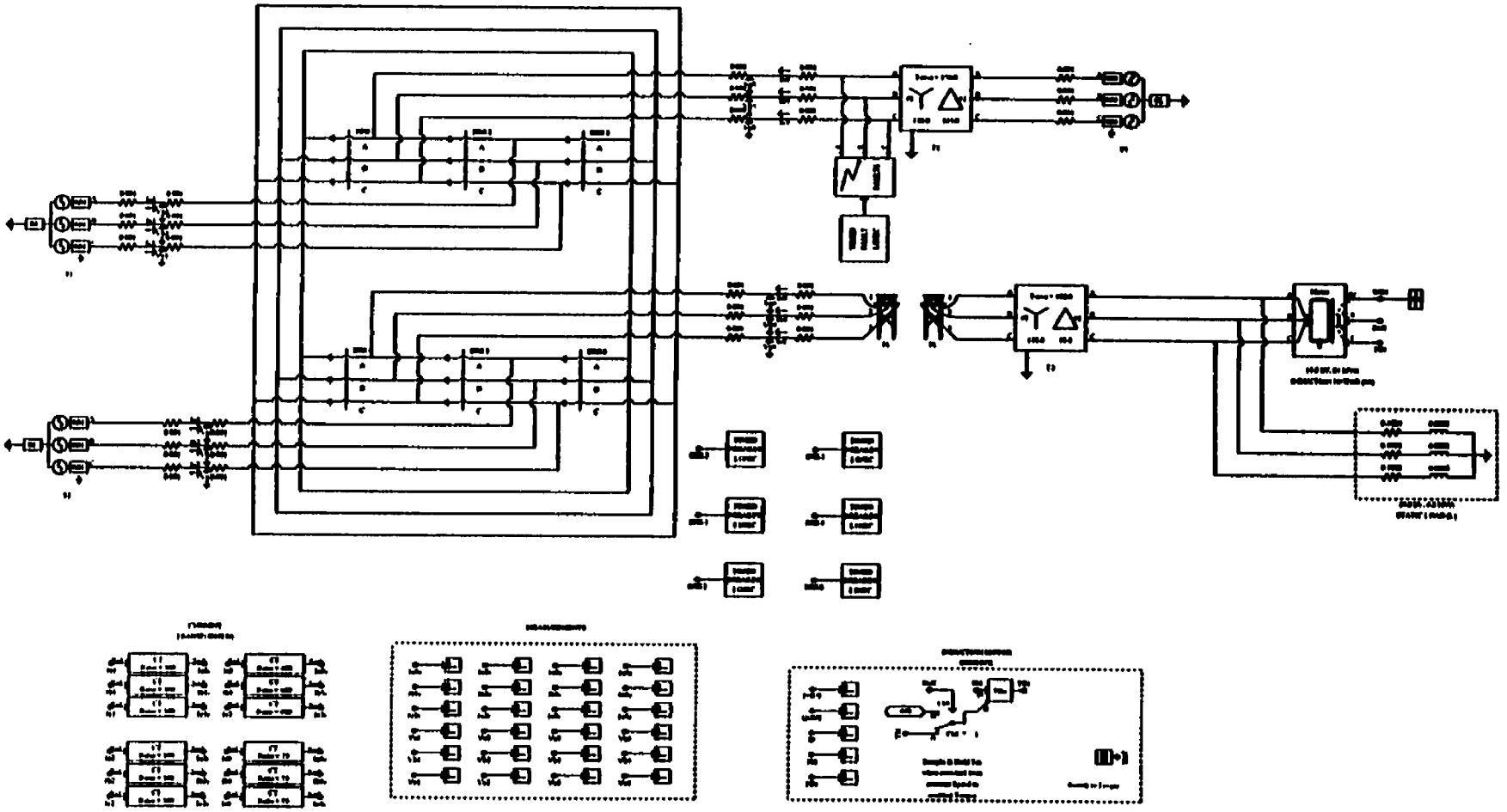


Figure D.3. Breaker-and-half busbar configuration of the model system in PSCAD.

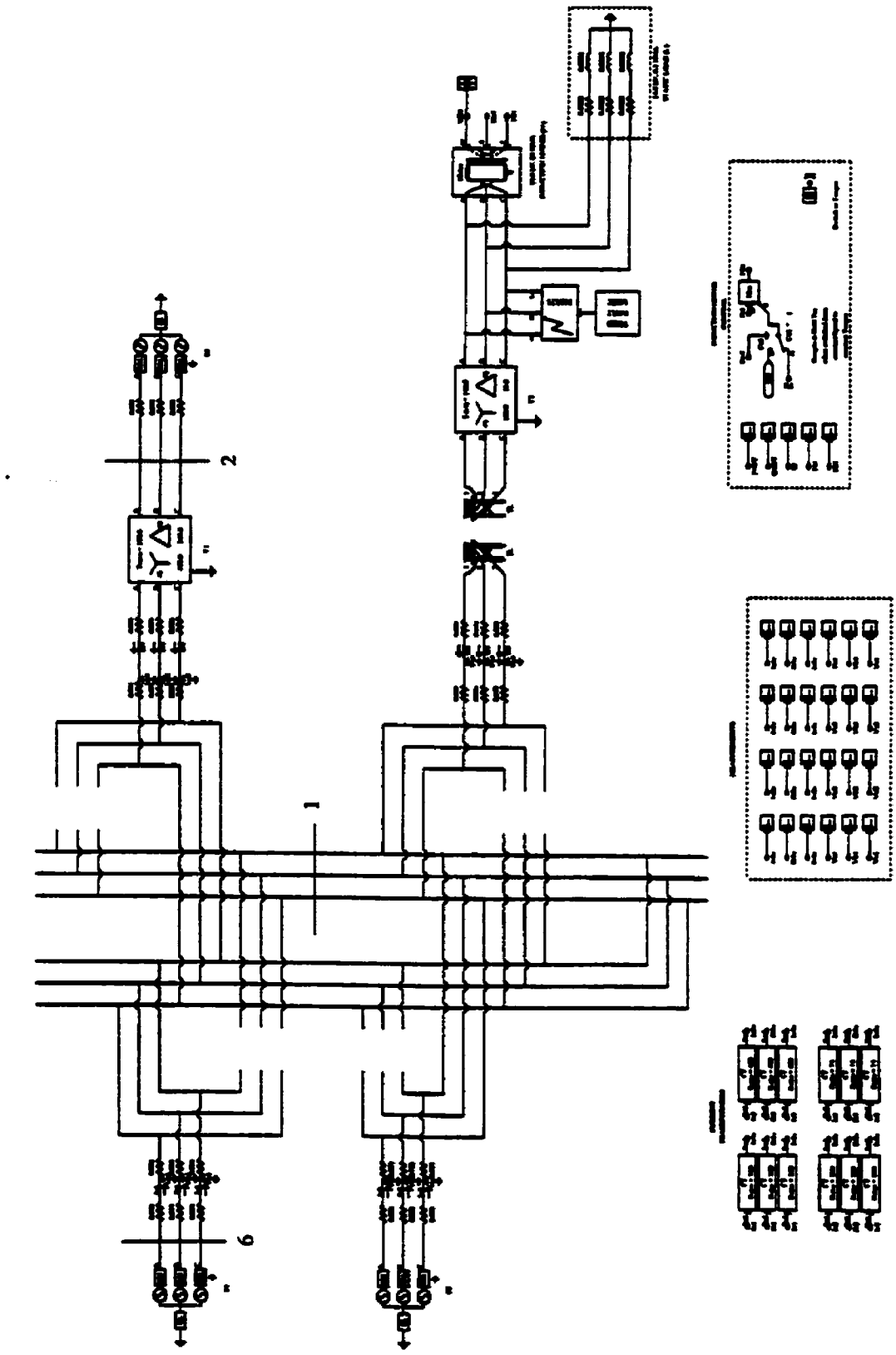


Figure D.4. Double busbar configuration of the model system in PSCAD.

Table D.3. Transformer data.

Parameter	Transfrmr. T1	Transfrmr. T2
3-phase MVA (MVA)	150.0	100.0
Pos.-seq. leakage reactance (p.u.)	0.05333	0.08
Winding # 1		
Connection type	Y	Y
L-L voltage, RMS (kV)	132.0	132.0
Winding # 2		
Connection type	Δ	Δ
L-L voltage, RMS (kV)	345.5	13.8

Table D.4. Transmission line (TL) data [67].

Parameter	Value/Type
Line length (kms.)	51.2
Ground resistivity (ohm-m)	100.0
Voltage (L-L, RMS) (kV)	132.0
Conductor name	Chukar
Other properties	Ideally transposed
	Frequency-dependent model
Number of bundles	3
Number of ground wires	1

Conductor and Ground wire data

Conductor		Ground wire	
Parameter	*Value*	*Parameter*	*Value*
Number of sub-cond.	1	Cond. name	7/16 Steel
Sub-cond. radius (cm)	2.03454	Cond. radius (cm)	0.55245
Sub-cond. spacing (cm)	0.001	Horizontal Distance X (m)	0.0
Horizontal Distance X (m)	-10.0,-10.0,-10.0	Height at Tower Y (m)	34.5736
Height at Tower Y (m)	17.3736, 21.336, 25.908	DC resistance (ohms/km)	2.8645
DC resistance (ohms/km)	0.03206		

Table D.5. Current transformer data.

Parameter	Value
Burden resistance (ohms)	0.5 - 40.0
Burden inductance (H)	0.8e-03

Table D.6. Simulation parameters.

Name	Value
Time-step (μs.)	43.4028
Print-step (ms.)	0.0434028

Another operating condition of the formulated system was devised using the load flow technique. The data of all the system components except the sources was maintained same. Table D.7 shows the data of various sources used for the second operating condition of the formulated system.

Table D.7. Source data for second operating condition of the formulated system.

Parameter	Source S1	Source S2	Source S3
Rated volts (L-L, RMS) (kV)	132.0	132.0	345.0
Initial phase (deg.)	0.0	4.5025	8.7949
Positive-sequence RRL			
Resistance (series) (ohms)	0.1742	0.1742	1.1903
Resistance (parallel) (ohms)	5000.0	5000.0	5000.0
Inductance (parallel) (H)	0.0139	0.0139	0.0947
Zero-sequence RL			
Resistance (parallel) (ohms)	50.0e+06	50.0e+06	50.0e+06
Inductance (parallel) (H)	0.0035	0.0035	0.0237

D.2. An existing substation

Figure D.5 shows the simulated model of the SaskPower substation used for testing the proposed busbar protection technique. The substation is of double busbar configuration and has five different circuits operating at 230 kV and 138 kV levels. Currents and voltages were recorded for five different locations as shown in the figure. Two different operating conditions of the substation has been used in the studies. The parameters of various system components and the recorder icon used for testing the technique for real-time are given in Tables D.8 to D.12.

Figure D.5. Simulated model of BRADA system in PSCAD.

Table D.8. Equivalent source data.

Parameter	S(NBF)	S(CCK)	S(GLN)	S(LMR)
Rated volts (L-L, RMS) (kV)	138.0	230.0	138.0	230.0
Initial phase (deg.)	-6.0	0.0	-2.0	-4.0
Positive-sequence RRL				
Resistance (series) (ohms)	8.85546	11.3735	55.13238	155.7905
Resistance (parallel) (ohms)	5000.0	5000.0	5000.0	5000.0
Inductance (parallel) (H)	0.074762	0.82802	0.57915	1.24757
Zero-sequence RL				
Resistance (parallel) (ohms)	50.0e+06	50.0e+06	50.0e+06	50.0e+06
Inductance (parallel) (H)	0.04701	0.063859	0.05213	0.20572

Table D.9. Load data.

Motor load (M)		Static load (L)	
Load MVA (MVA)	43.4	Load MVA (MVA)	18.4
Rated RMS phase voltage (kV)	132.79	L-L voltage, RMS (kV)	230.0
Horse power (H.P.)	50.0	Resistive component (ohms)	2766.0
		Reactive component (H)	1.838
Total load (p.u.)		60+j15 @ 100 MVA	

Table D.10. Transformers (T1 & T2) data.

Parameter	Value
3-phase MVA (MVA)	150.0
Winding # 1	
Connection type	Y
L-L voltage, RMS (kV)	138.0
Winding # 2	
Connection type	Δ
L-L voltage, RMS (kV)	13.8
Winding # 3	
Connection type	Y
L-L voltage, RMS (kV)	230.0
Pos.-seq. leakage reactance	
Winding #1 - Winding #2 (p.u.)	0.0773
Winding #1 - Winding #3 (p.u.)	0.0367
Winding #2 - Winding #3 (p.u.)	0.1213
Reactor connections	
Connection type	Y
Inductance/phase (H)	0.0583

Table D.11. Transmission line data.

Parameter	NBF	BNG	MWS	LMC	CCK	LMR
Line length (kms.)	3.184	6.208	200.0	1.76	189.9	152.28
Ground resistivity (ohm-m)	10.0	10.0	6.0	10.0	10.0	10.0
Voltage (L-L, RMS) (kV)	138.0	138.0	230.0	230.0	230.0	230.0
Conductor name	Hawk	Hawk	Drake	Drake	Drake	Drake
Number of bundles	3	6	3	6	3	3
Number of ground wires	2	2	2	2	2	2

Conductor data

Parameter	T-line			
	NBF	MWS	CCK	LMR
No. of sub-cond.	1	1	1	1
Sub-cond. radius (cm)	0.880872	1.136904	1.136904	1.136904
Sub-cond. spacing (cm)	45.72	45.72	45.72	45.72
Horizontal Distance X (m)	-0.76195, -4.41931, -5.94321	-6.25, 0.0, 6.25	-6.2484, 0.0, 6.2484	-6.25, 0.0, 6.25
Height at tower Y (m)	14.47705, 14.47705, 11.398772	18.0, 18.0, 18.0	19.99488, 19.99488, 19.99488	18.0, 18.0, 18.0
Sag at mid-span (m)	4.205964	9.82	10.36252	10.99
DC resistance (ohms/km)	0.11713	0.07054	0.07054	0.07054

Parameter	T-line	
	BNG	LMC
No. of sub-cond.	1	1
Sub-cond. radius (cm)	0.880872	1.136904
Sub-cond. spacing (cm)	45.72	45.72
Horizontal Distance X (m)	-0.762, -4.4196, -5.9436, 0.762, 4.4196, 5.9436	-7.1, -5.9, 0.0, 8.6, 7.4, 1.5
Height at tower Y (m)	14.478, 14.478, 11.39952, 11.39952, 14.478, 11.39952	18.0, 23.2, 18.0, 18.0, 23.2, 23.2
Sag at mid-span (m)	4.2064	10.99
DC resistance (ohms/km)	0.11713	0.07054

Ground wire data

Parameter	T-line					
	NBF	BNG	MWS	CCK	LMC	LMR
Cond. name	7/16 Steel	7/16 Steel	7/16 Steel	7/16 Steel	7/16 Steel	7/16 Steel
Cond. radius (cm)	0.397	0.397	0.397	0.397	0.397	0.397
Horizontal dist. (m)	-2.74302, 2.74302	-2.74302, 2.74302	-3.3, 3.3	-3.68808, 3.68808	-3.33, 4.83	-3.3, 3.3
Height at tower (m)	16.91529	16.9164	23.4	25.29674	27.8	23.4
Sag at mid-span (m)	2.666825	2.667	6.56	6.888028	9.87	9.87
DC resistance (ohms/km)	5.73	5.73	5.73	5.73	5.73	5.73

Table D.12. Current transformer data.

Parameter	Value
Burden resistance (ohms)	0.5 - 40.0
Burden inductance (H)	0.8e-03

Table D.13. Recorder icon, sliders and comparator data.

Parameter	Value
(i) Recorder data	
Output file format	RTP
Recording time step (μs.)	217
Low pass filtering enable	never
System frequency (Hz)	60
Number of 12-bit analog channels	7
Instrument transformer ratio (kV/V or kA/A)	1.0 (Pri./Sec.)
(ii) Sliders	
Start time (sec.)	0.65
End time (sec.)	0.75
(iii) Comparator	
Configuration	
Output type	Level
Level data	
Output when A>B	1
Output when A<=B	0
Real-time constant (B) (sec.)	0.7
TIME (A) (sec.)	simulation time

Table D.14. Simulation parameters.

Name	Value
Time-step (μs.)	43.4028
Finish time (ms.)	750
Print-step (ms.)	0.0434028

The resistive and reactive components of the wavetraps used in the simulations were 0.005788 ohms and 0.00128 H respectively. The second operating condition of the existing substation was simulated using the data available for the same. The Table D.15 gives the values of the equivalent source parameters utilized for this operating condition. The data for other components was maintained the same as used for the first operating condition, the data for which is presented above.

Table D.15. Equivalent source data.

Parameter	S(NBF)	S(CCK)	S(GLN)	S(LMR)
Rated volts (L-L, RMS) (kV)	138.0	230.0	138.0	230.0
Initial phase (deg.)	-5.0	0.0	-1.0	-3.0
Positive-sequence RRL				
Resistance (series) (ohms)	10.797948	11.4264	31.974876	122.1461
Resistance (parallel) (ohms)	5000.0	5000.0	5000.0	5000.0
Inductance (parallel) (H)	0.0937	0.8016	0.66093	1.3281
Zero-sequence RL				
Resistance (parallel) (ohms)	50.0e+06	50.0e+06	50.0e+06	50.0e+06
Inductance (parallel) (H)	0.048933	0.062638	0.0522	0.2057

Appendix E. EMTDC & CT MODEL

This appendix gives a brief description of the power systems simulation software, EMTDC [49], which was used for the generation of simulated fault data for the power systems, and the ct model used to simulate ct saturation and ratio-mismatch conditions. Complex power system networks can be modeled using EMTDC to represent practical systems. A user interface, called Power Systems Computer Aided Design (PSCAD), enables the user to select preprogrammed models of power system components which are used to graphically build the power system networks. The built-in library of PSCAD includes models of voltage and current sources, machines, transmission lines, switches, measuring instruments, transformers and control blocks and many other power system apparatus models.

Compilation of the PSCAD network generates FORTRAN source code. The source code is then compiled using EMTDC which generates executable code that runs in the UNIX environment of the SunSPARC workstation. Fault data generated by EMTDC was stored in a file. This data file was used for testing the proposed protection algorithm.

The ct model used in the research project was downloaded from the ftp site of the University of Manitoba [50]. This model was initially written by Dr. J. Mohan Lucas and later revised by Dr. W.W.L. Keerthipala and Dr. Rohitha P. Jayasinghe respectively. The model can be represented as in Figure E.1.

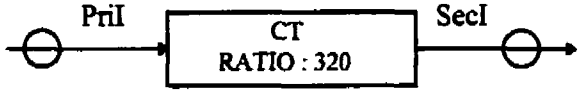


Figure E.1. CT model.

The model has two wire labels for representing the primary and secondary currents of the current transformer respectively. The primary wire label is given the same name as the current label used in the EMTDC simulation model. The secondary wire label then gives the equivalent ct output for the given input current. The ct ratio can be selected in the model. Saturation state of the ct can be simulated by using very high value for the burden resistance. Typical burden impedance in practice is much less than the values used in the model. The default values for the saturation and loss characteristics match with those of the 'silectron 53' core material.

Appendix F. ANTI-ALIASING FILTER DESIGN

The fault voltages and currents are associated with decaying dc, fundamental frequency (60 Hz) and high frequency components [68, 69]. The high frequency components result due to traveling wave phenomenon and their frequencies depends on the distance to the fault. Non-linearities in the power system produce harmonics of 60 Hz components.

Depending on the sampling rate of voltages and currents, some of the high frequency components can appear as components of power frequency [48]. An anti-aliasing filter was designed to pre-process the voltage and current samples obtained by simulation before being presented to the LES algorithm. The principle of anti-aliasing dictates that the cut-off frequency of the low-pass filter should be less than or equal to one-half of the sampling frequency of the LES algorithm. The sampling frequency of least error squares algorithm used to estimate the fundamental frequency components of voltage and current signals was selected as 1440 Hz. A 4th order Butterworth filter with a cut-off frequency of 200 Hz was selected as an anti-aliasing filter. The filter was designed using a Matlab program. Equation F.1 gives the transfer function for the designed filter.

$$\frac{Y(z)}{X(z)} =$$

$$\frac{1.0x10^{-5}(0.0515546 + 0.2062183z^{-1} + 0.3093274z^{-2} + 0.2062183z^{-3} + 0.0515546z^{-4})}{(1.0z^{-1} - 3.8574847z^{-2} + 5.5825215z^{-3} - 3.5921775z^{-3} + 0.8671489z^{-5})} \quad (F.1)$$

Figure F.1 shows the magnitude response of the designed low-pass filter.

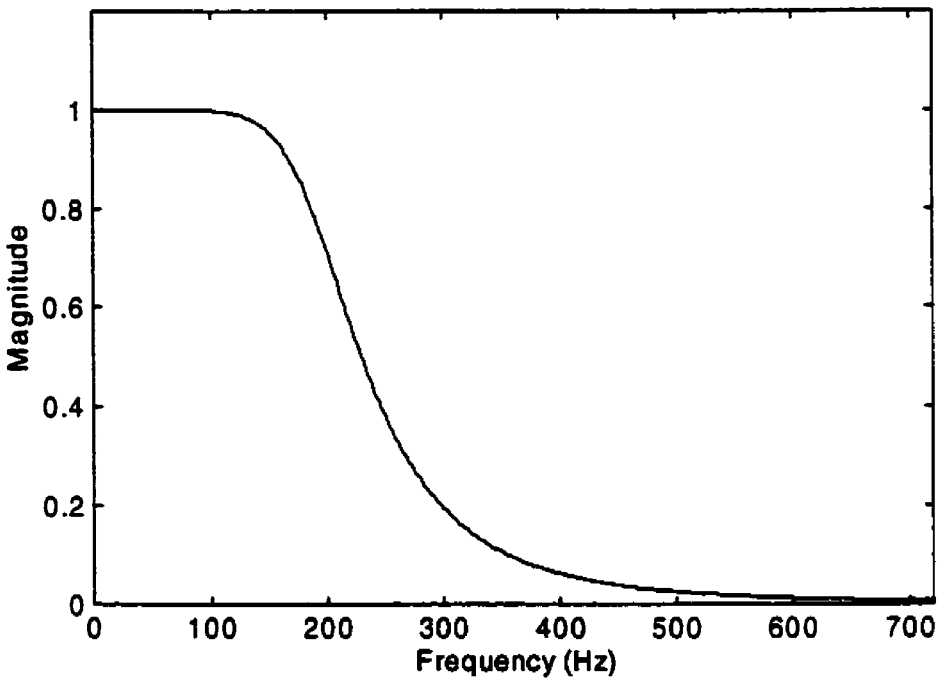


Figure F.1. Magnitude response of anti-aliasing filter.

Appendix G. ADDITIONAL SIMULATION RESULTS

Selected test results illustrating the performance of the proposed technique for busbar protection have been presented in Chapter 5. Different types of faults at various locations in the simulated power systems were considered. The studies considered different operating conditions of the power systems, four busbar configurations, and ct saturation. This appendix provides additional test results, obtained from simulation studies, for various types of faults and current transformer conditions for the system models considered in performance evaluation. Figures G.1 to G.40 show the plots of the arguments of sequence-impedances seen by the relays. Tables 5.5 and 5.6 (in Chapter 5) give a summary of the results presented in this appendix. This includes the fault location and type, busbar configuration, post-fault samples required by different relays to reach threshold and the time required by the proposed technique to make final decision on the type of faults.

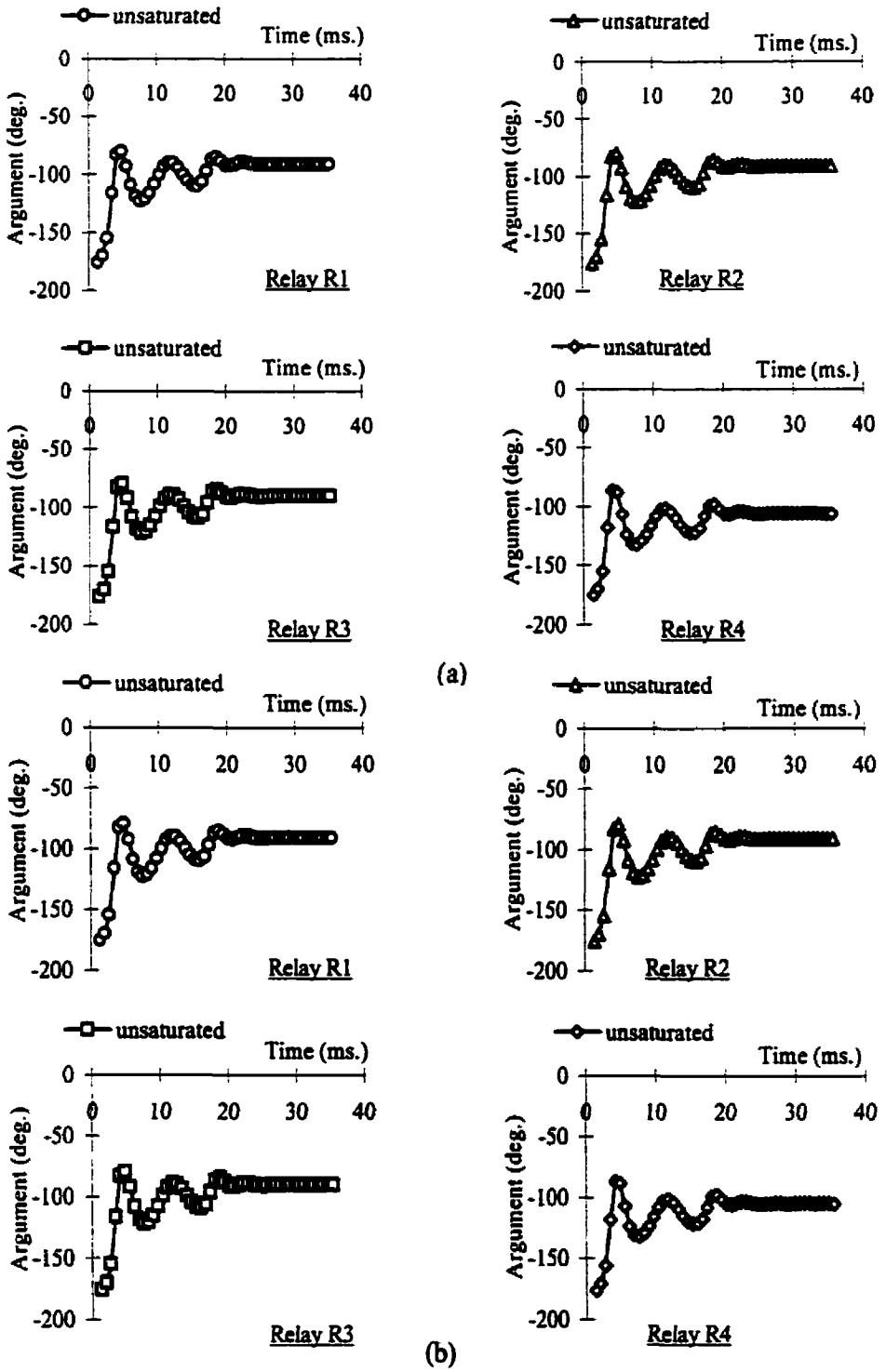


Figure G.1. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase B-ground fault in the busbar protection zone (location 1) of the substation of Figure 5.1.

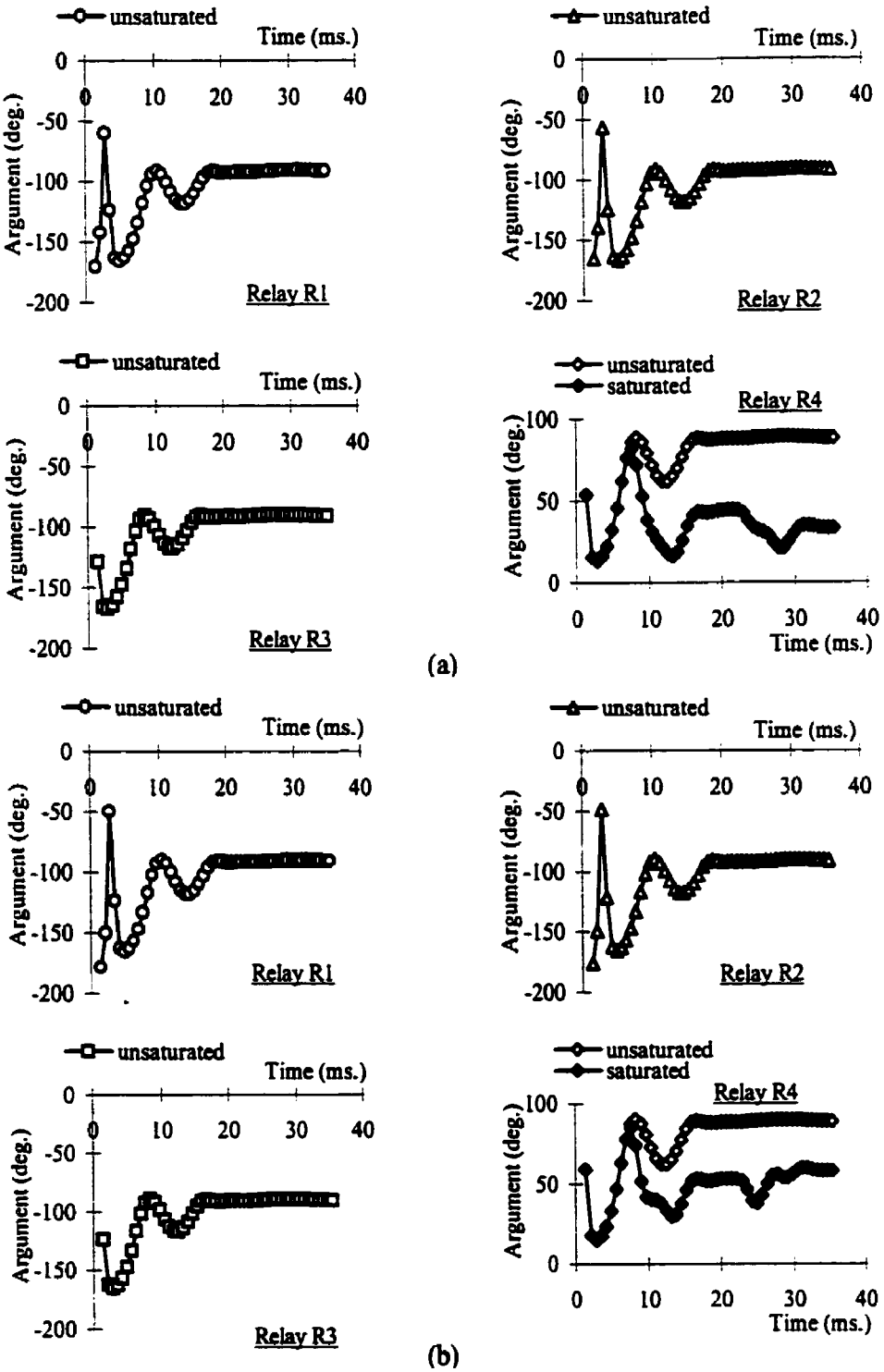


Figure G.2. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase A-Phase C fault outside the busbar protection zone (location 3) of the substation of Figure 5.1.

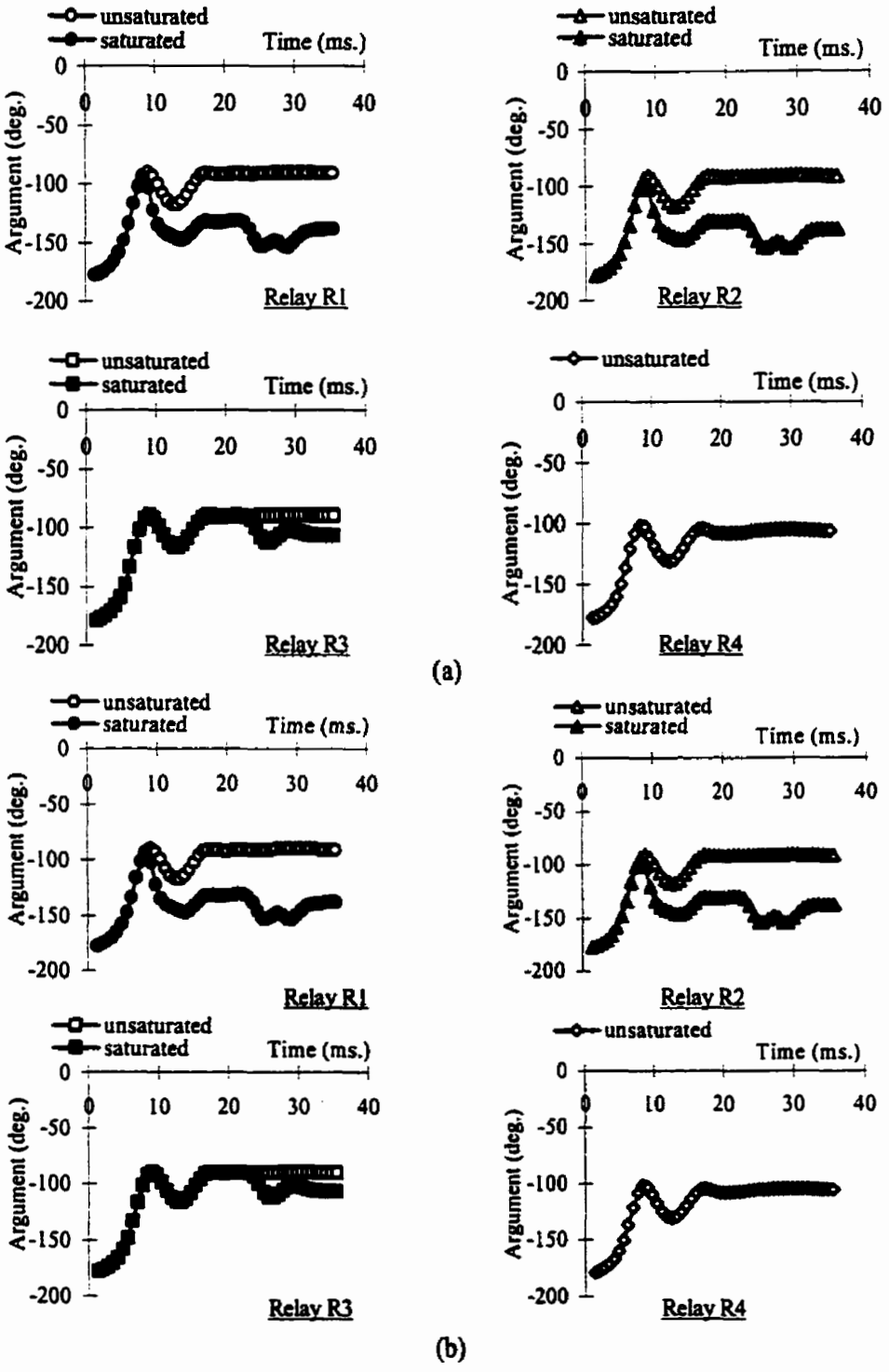


Figure G.3. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-ground fault in the busbar protection zone (location 1) of the substation of Figure D.4 (p. 178).

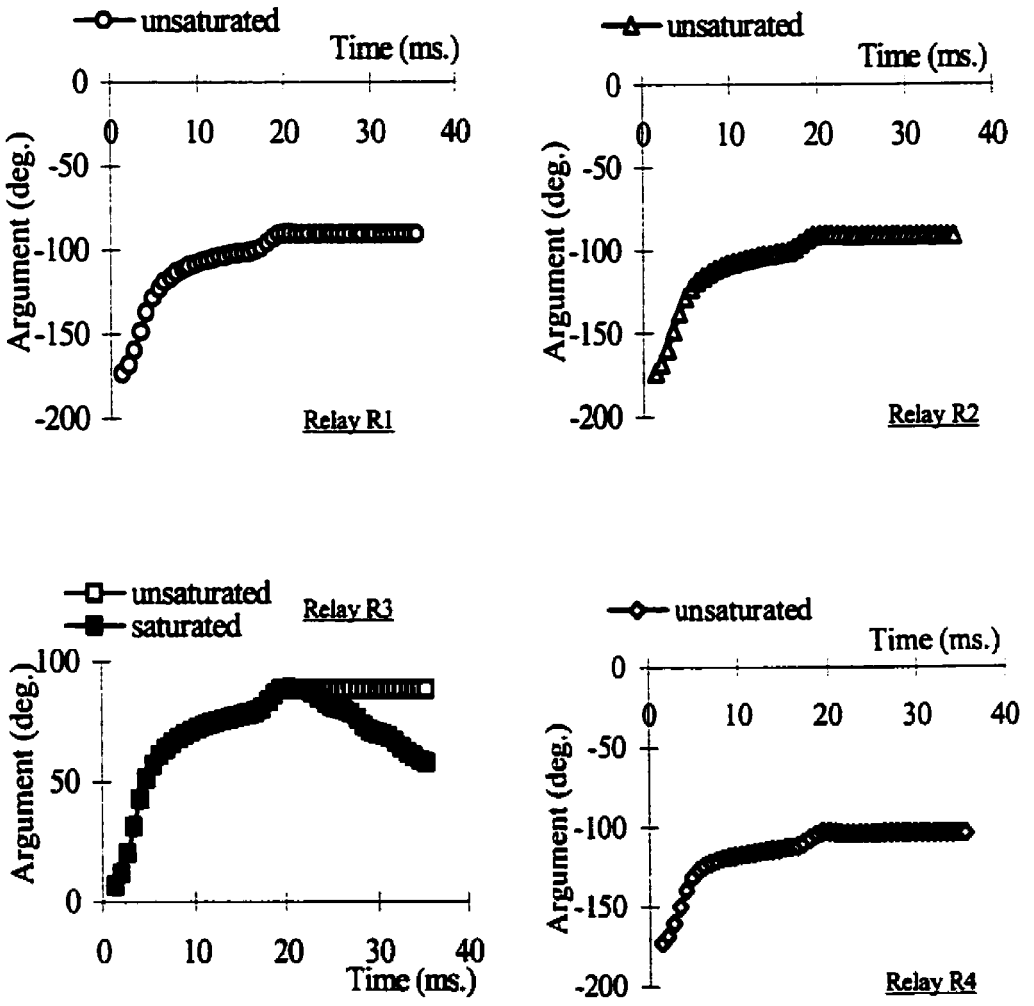
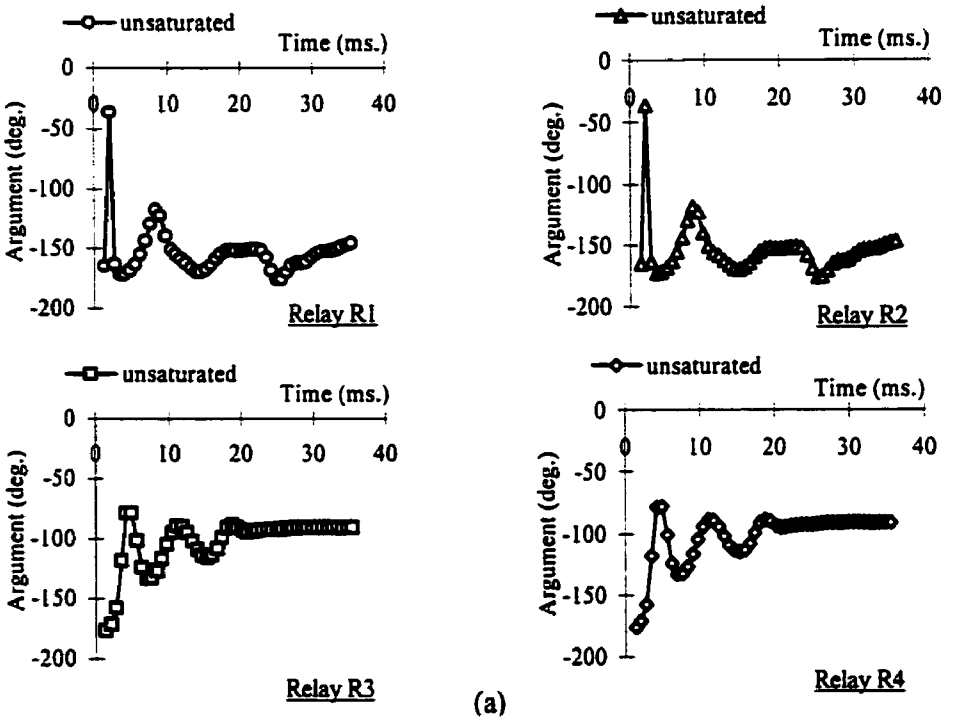
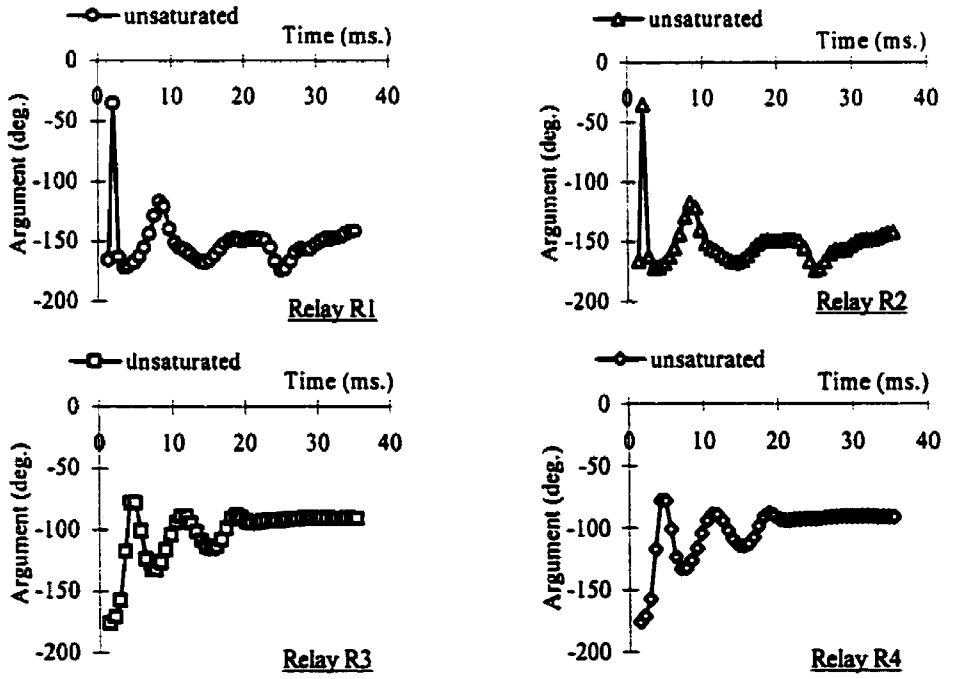


Figure G.4. Plots of the arguments of the positive-sequence impedances computed by the relays for a three phase fault outside the busbar protection zone (location 2) of the substation of Figure D.4 (p. 178).



(a)



(b)

Figure G.5. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase C-ground fault outside the busbar protection zone (location 2) of the substation of Figure 5.1.

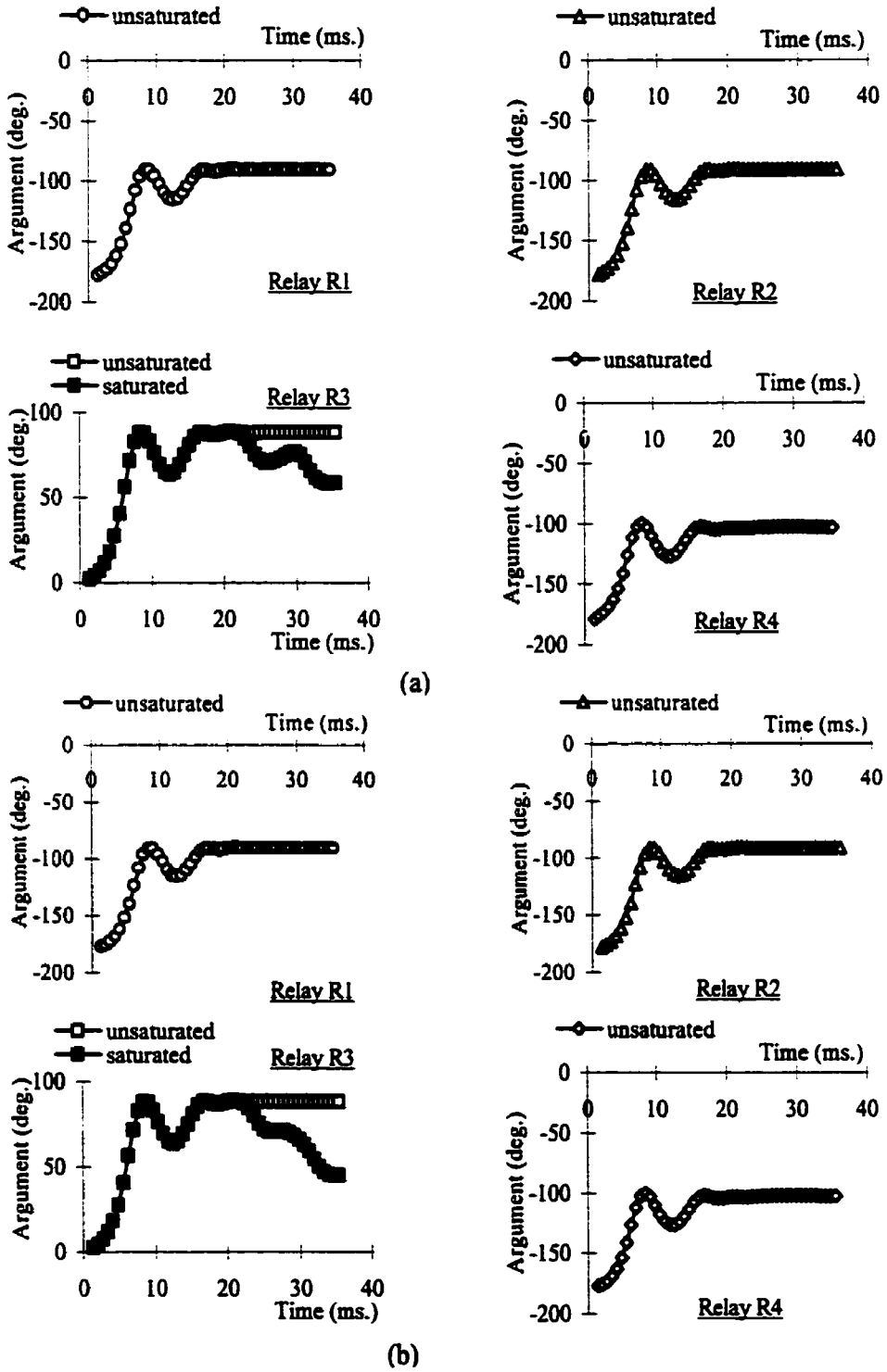


Figure G.6. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase A-Phase B fault outside the busbar protection zone (location 2) of the substation of Figure 5.7.

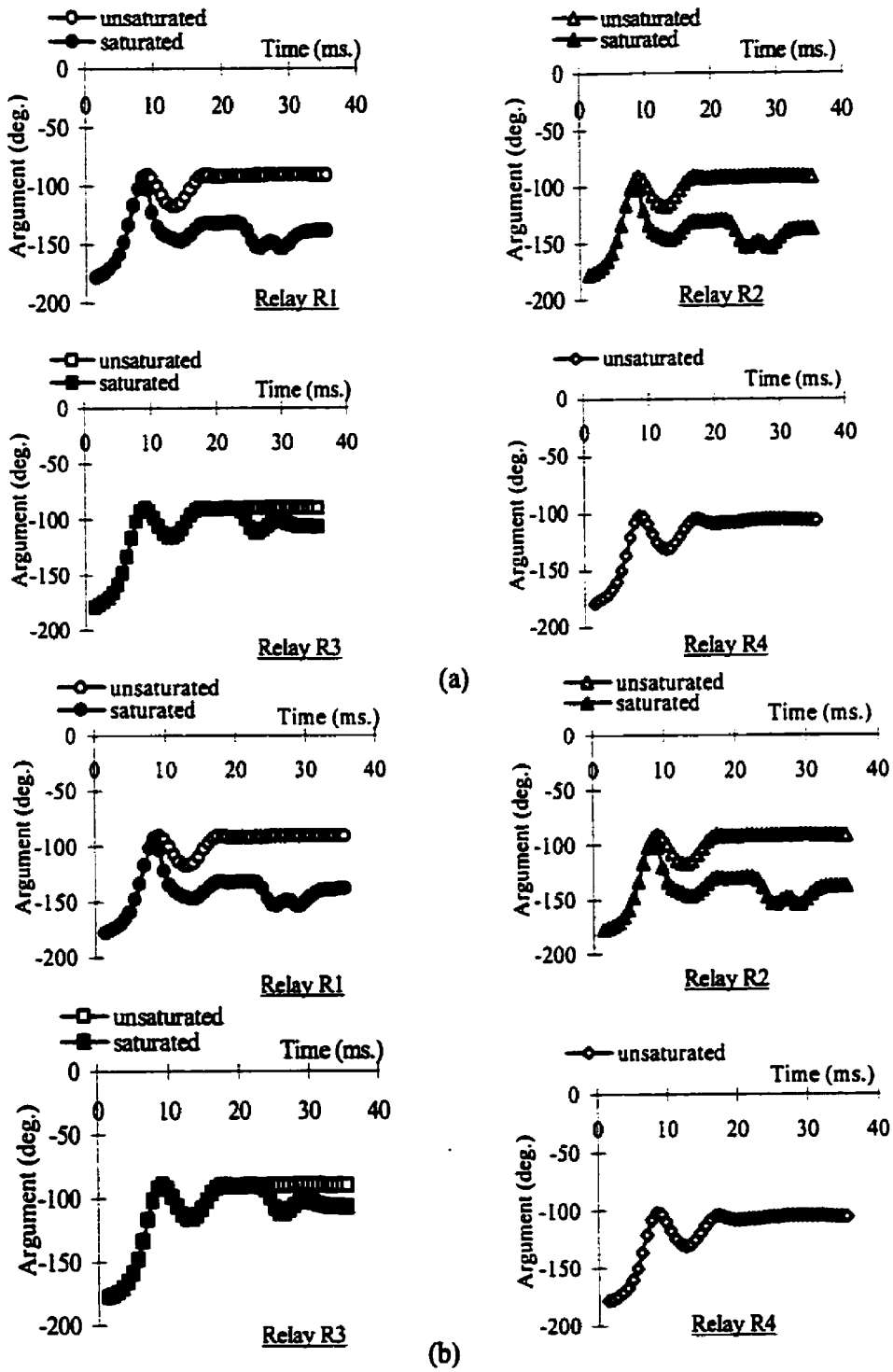


Figure G.7. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-ground fault in the busbar protection zone (location 1) of the substation of Figure 5.3.

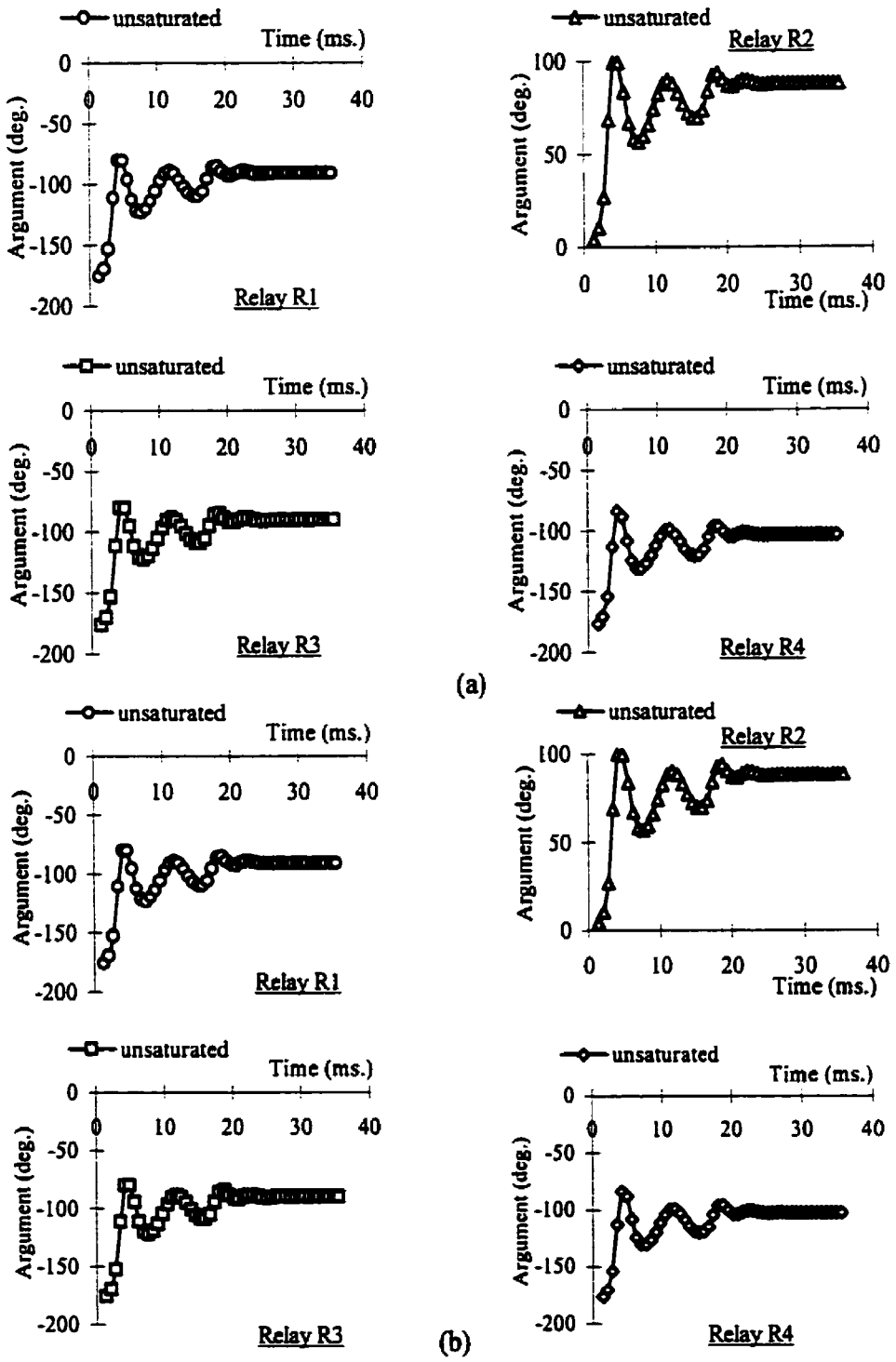


Figure G.8. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase B-ground fault outside the busbar protection zone (location 4) of the substation of Figure 5.3.

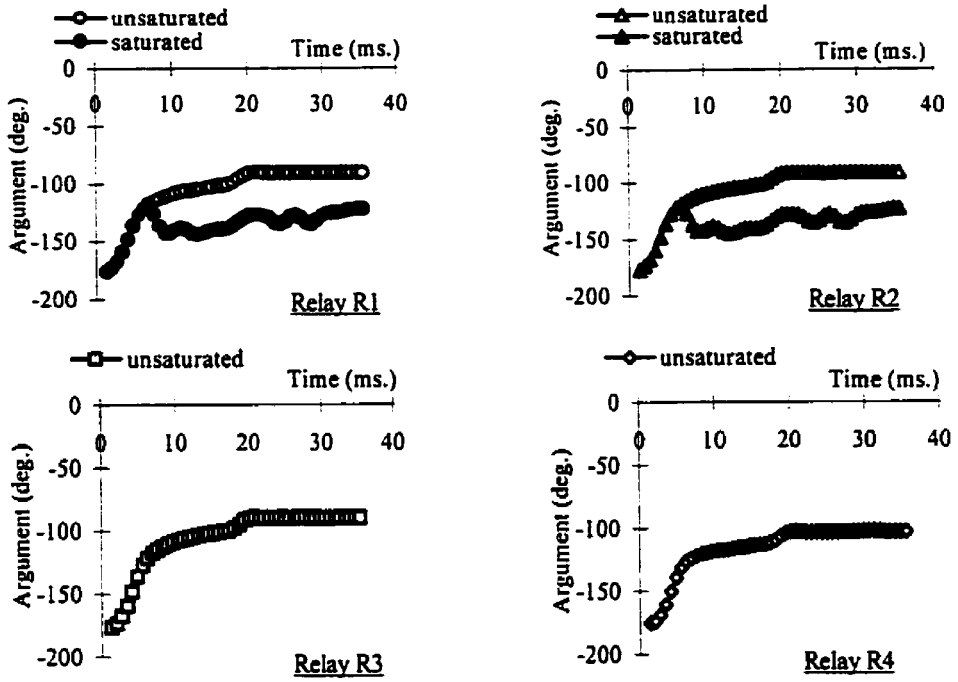


Figure G.9. Plots of the arguments of the positive-sequence impedances computed by the relays for a three phase fault in the busbar protection zone (location 1) of the substation of Figure 5.7.

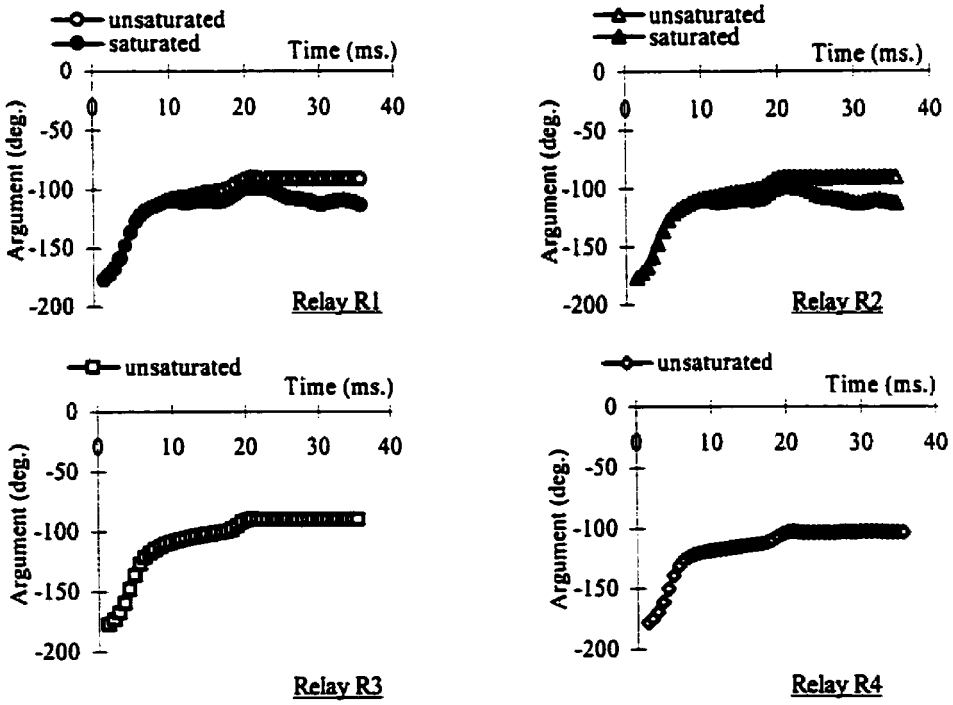


Figure G.10. Plots of the arguments of the positive-sequence impedances computed by the relays for a three phase fault in the busbar protection zone (location 1) of the substation of Figure 5.3.

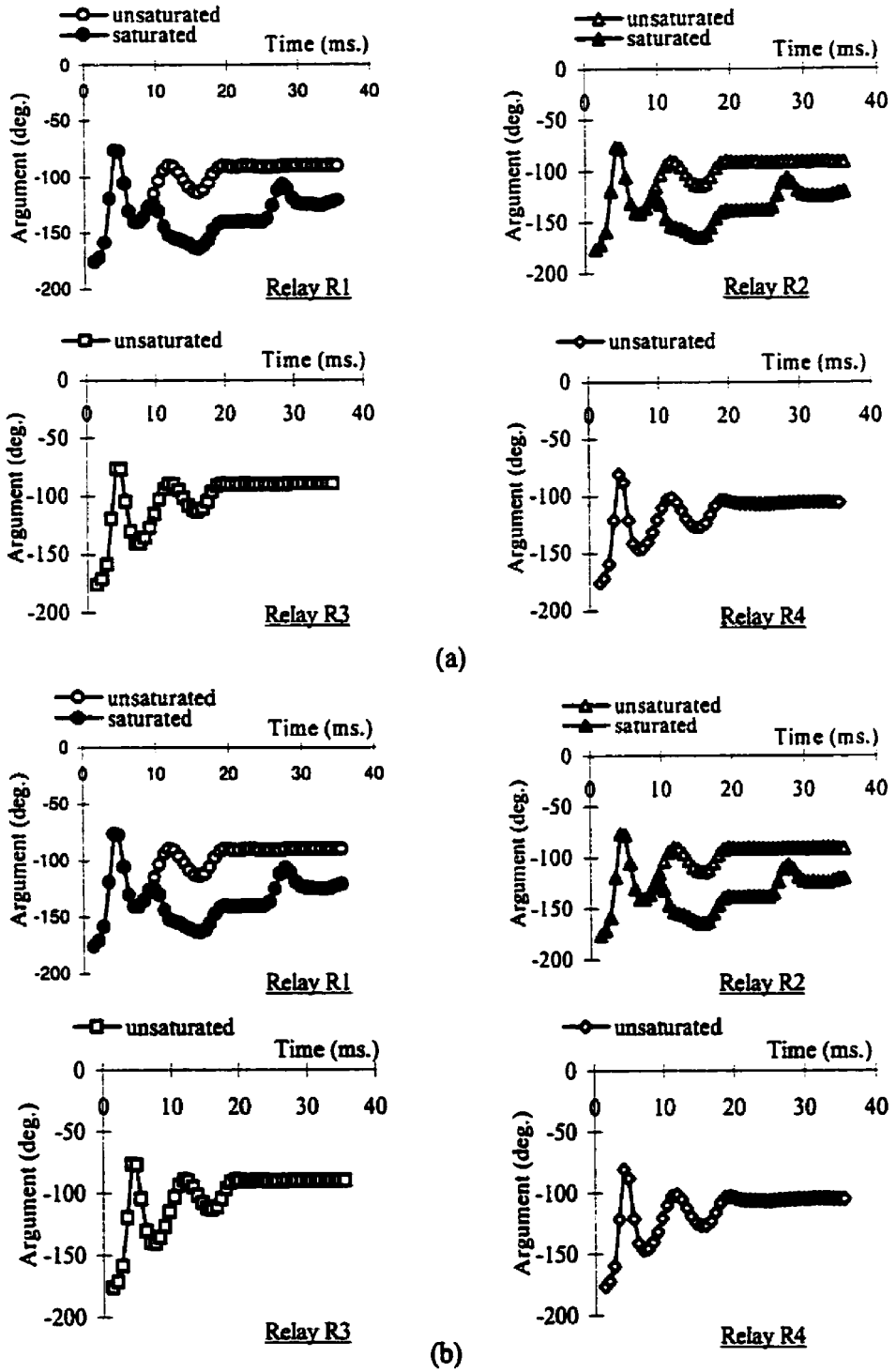


Figure G.11. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase C-ground fault in the busbar protection zone (location 1) of the substation of Figure 5.1.

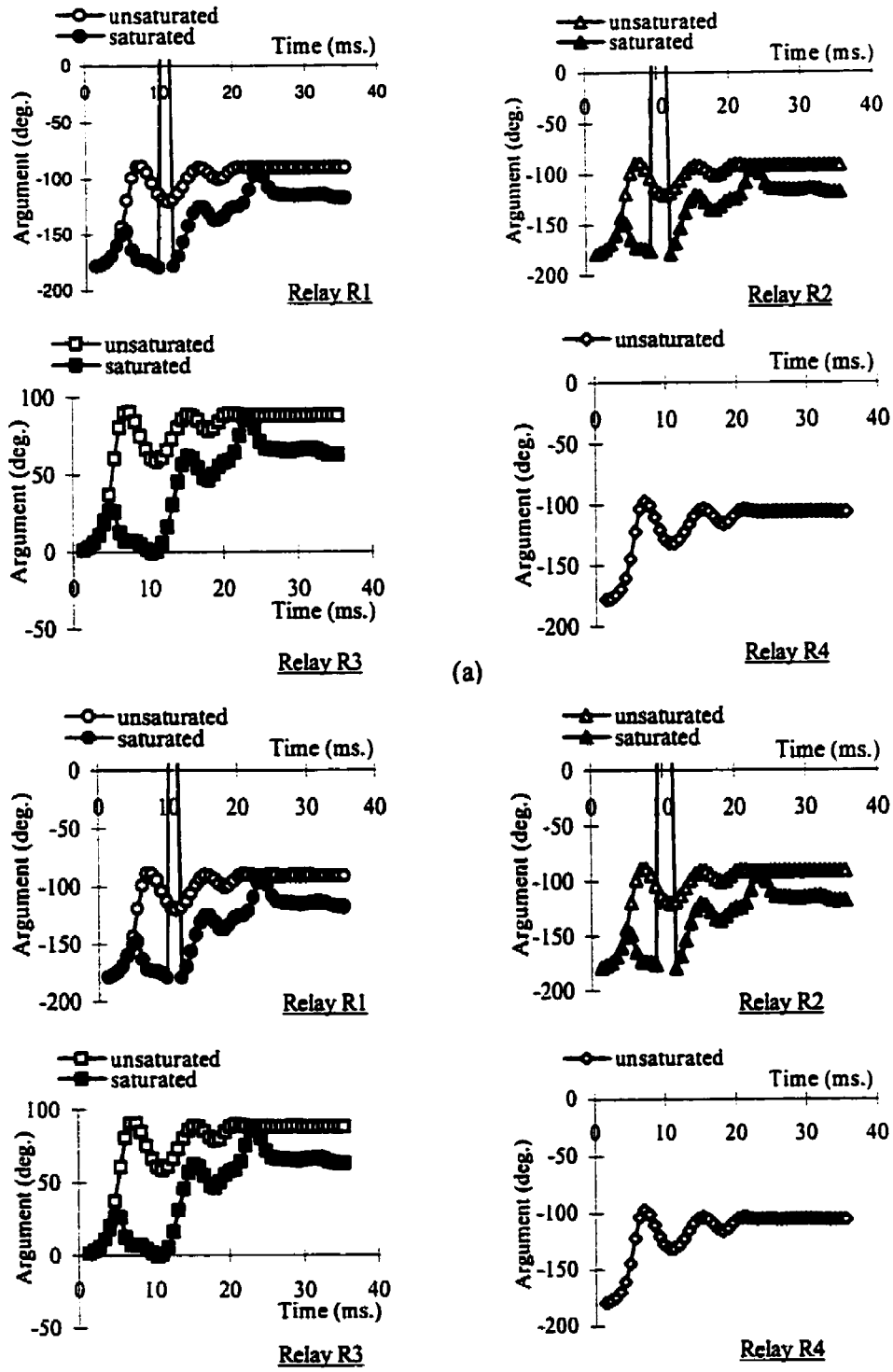


Figure G.12. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase B-ground fault outside the busbar protection zone (location 5) of the substation of Figure 5.1.

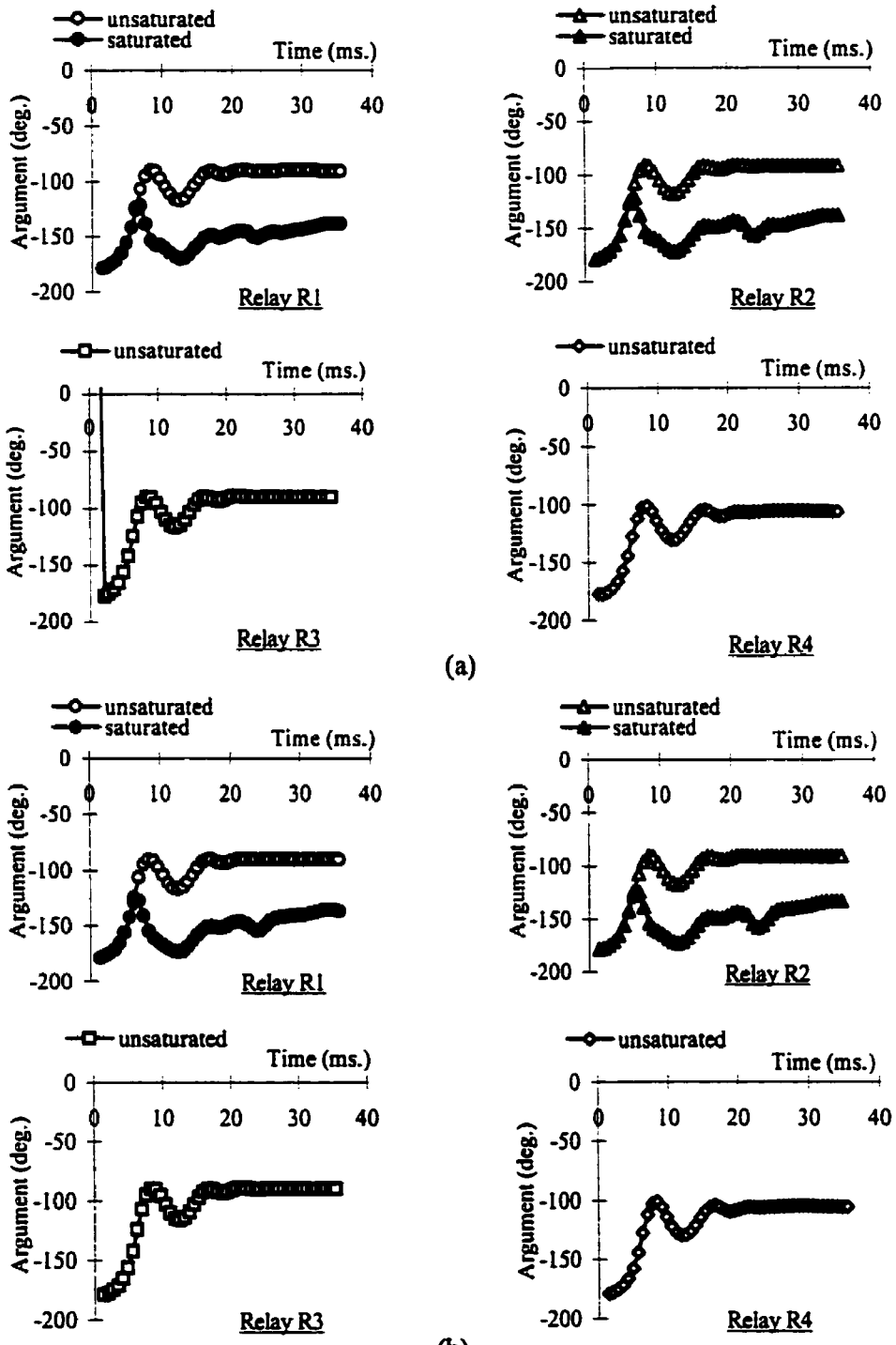


Figure G.13. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-Phase B fault in the busbar protection zone (location 1) of the substation of Figure 5.7.

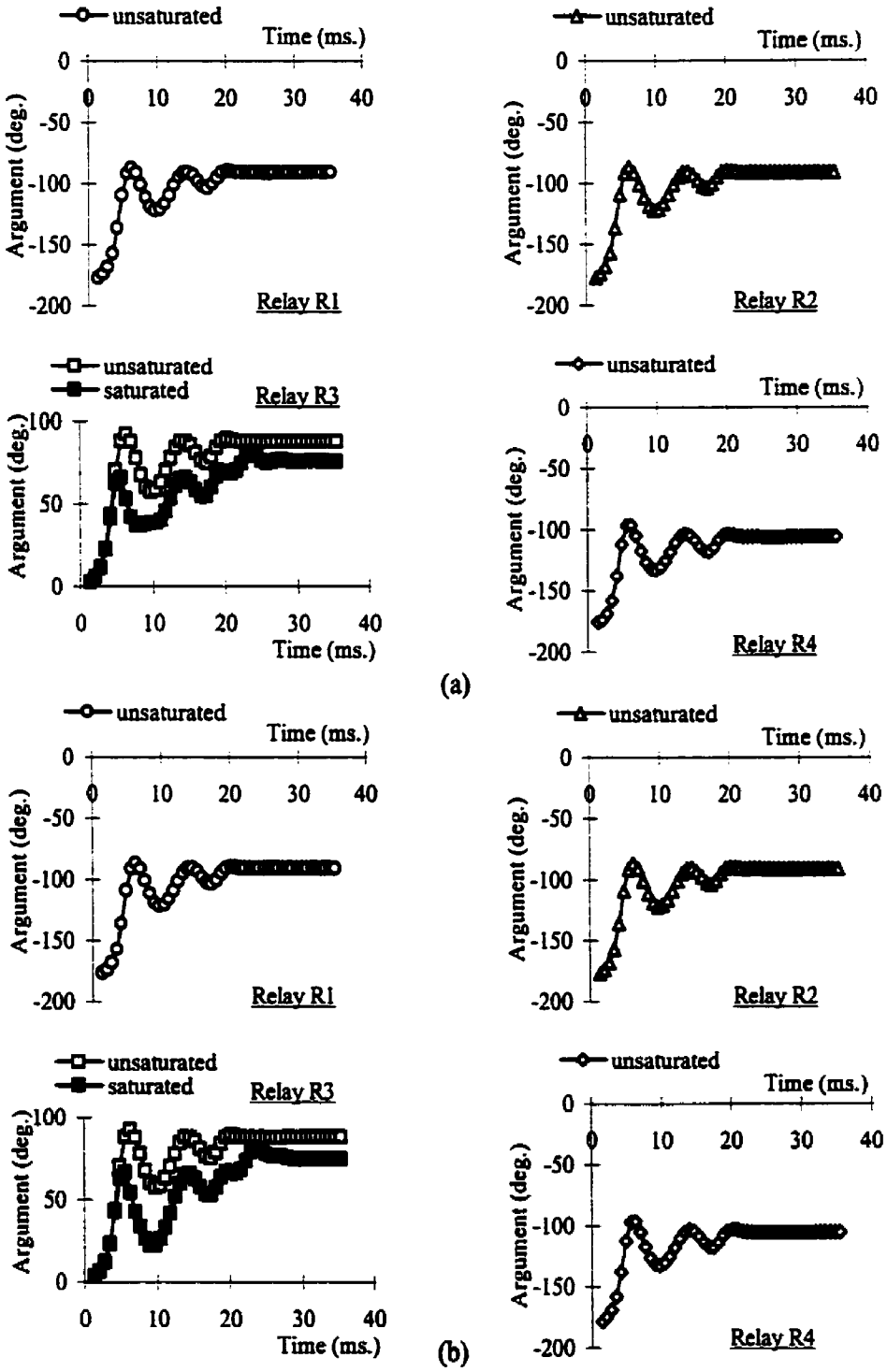


Figure G.14. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase B-Phase C fault outside the busbar protection zone (location 2) of the substation of Figure 5.7.

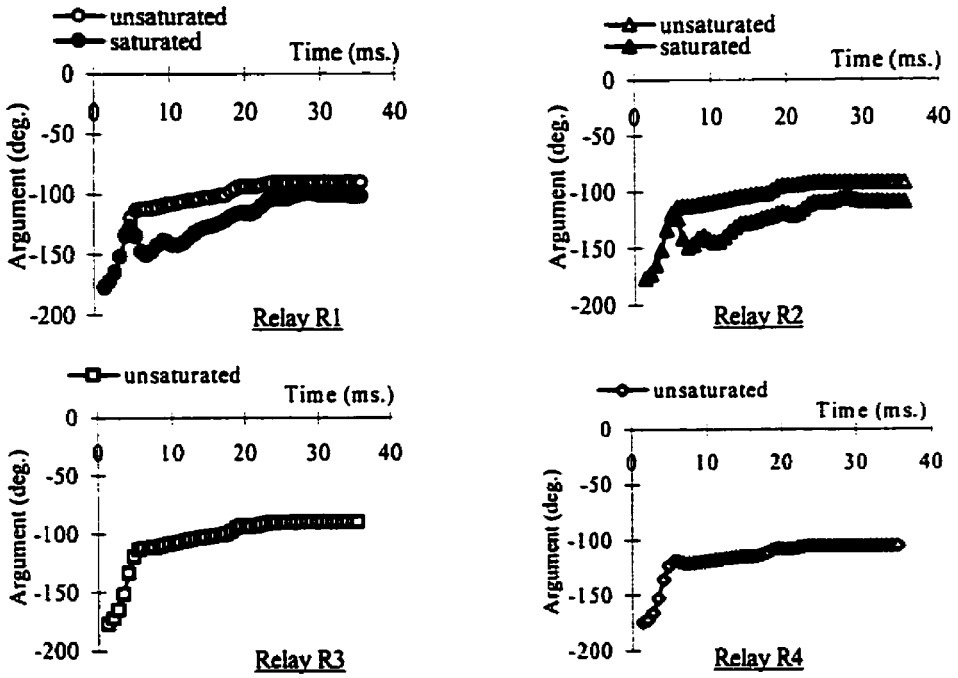


Figure G.15. Plots of the arguments of the positive-sequence impedances computed by the relays for a three phase-ground fault in the busbar protection zone (location 1) of the substation of Figure D.4 (p. 178).

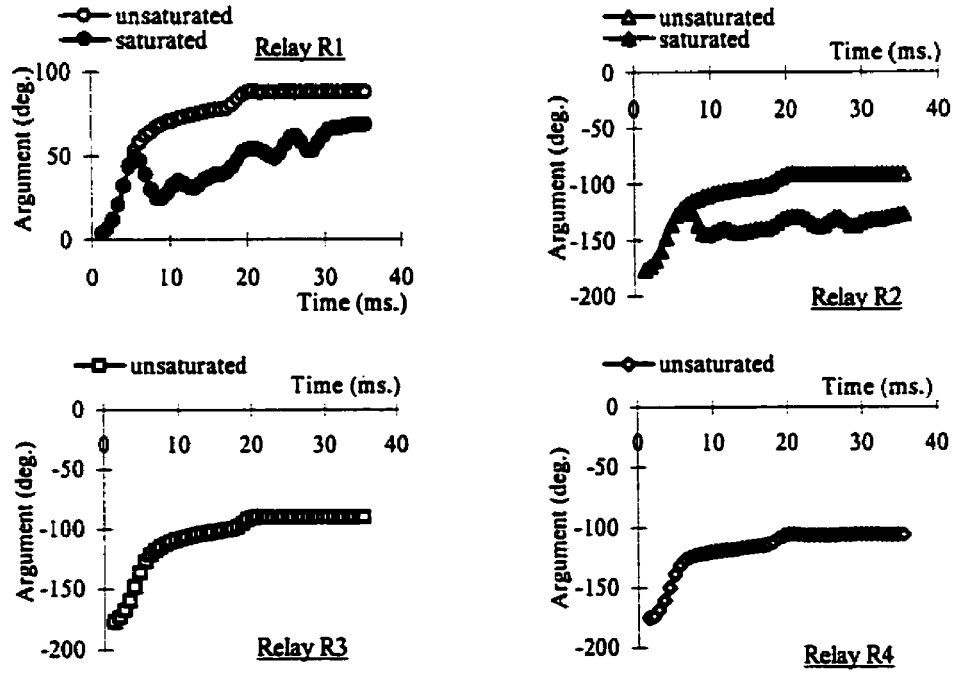


Figure G.16. Plots of the arguments of the positive-sequence impedances computed by the relays for a three phase fault outside the busbar protection zone (location 6) of the substation of Figure D.4 (p. 178).

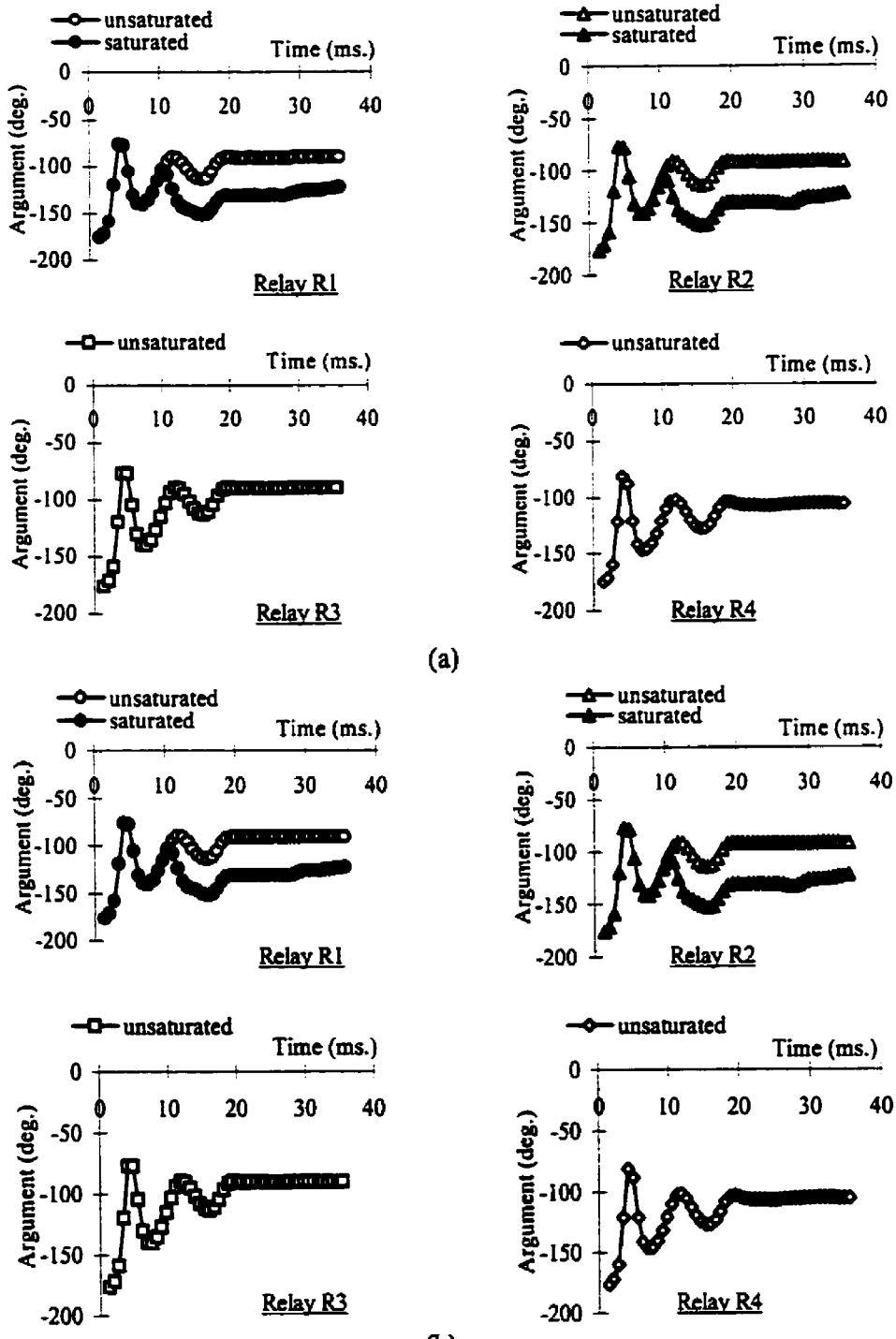


Figure G.17. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase C-ground fault in the busbar protection zone (location 1) of the substation of Figure 5.3.

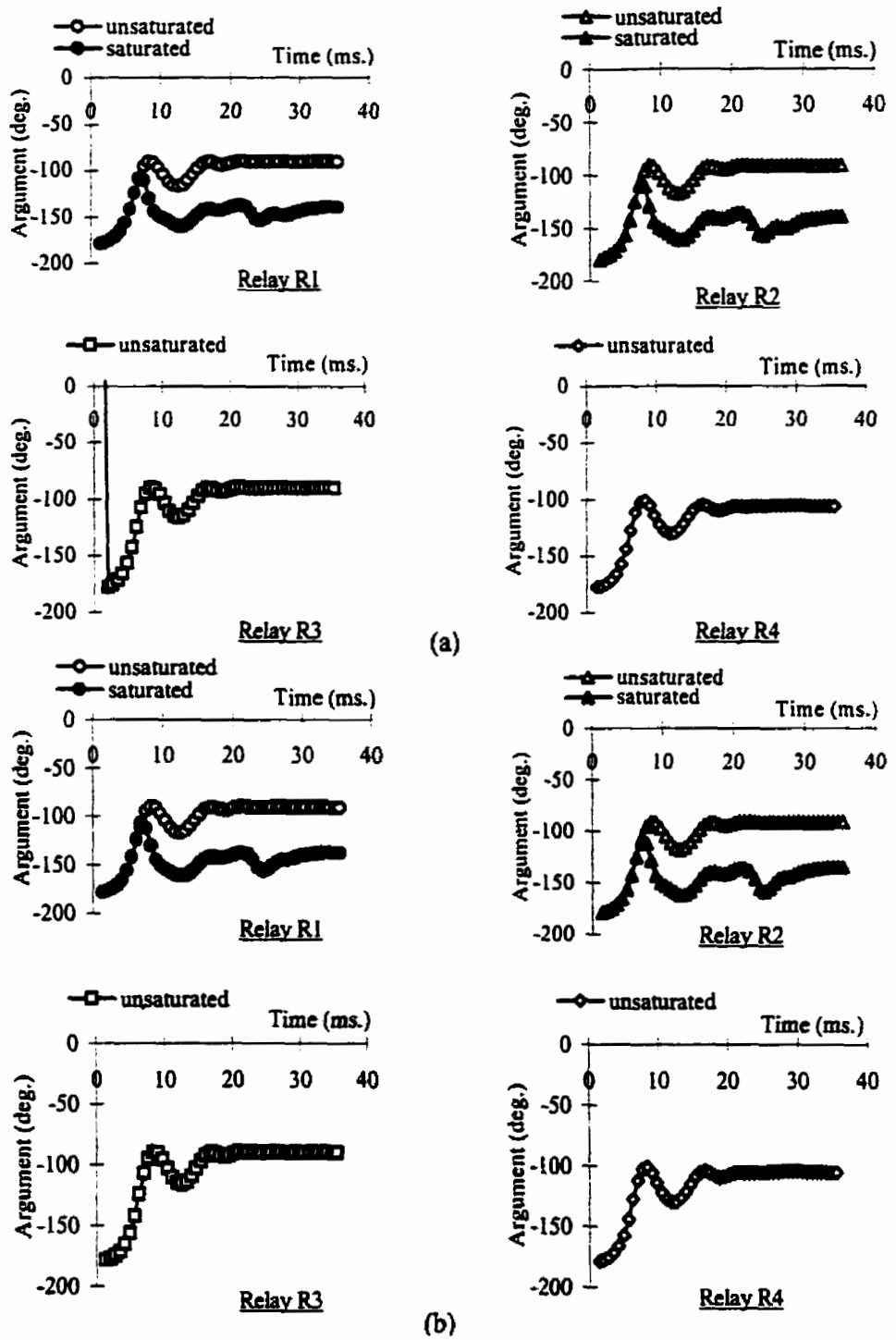


Figure G.18. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for Phase A-Phase B fault in the busbar protection zone (location 1) of the substation of Figure 5.3.

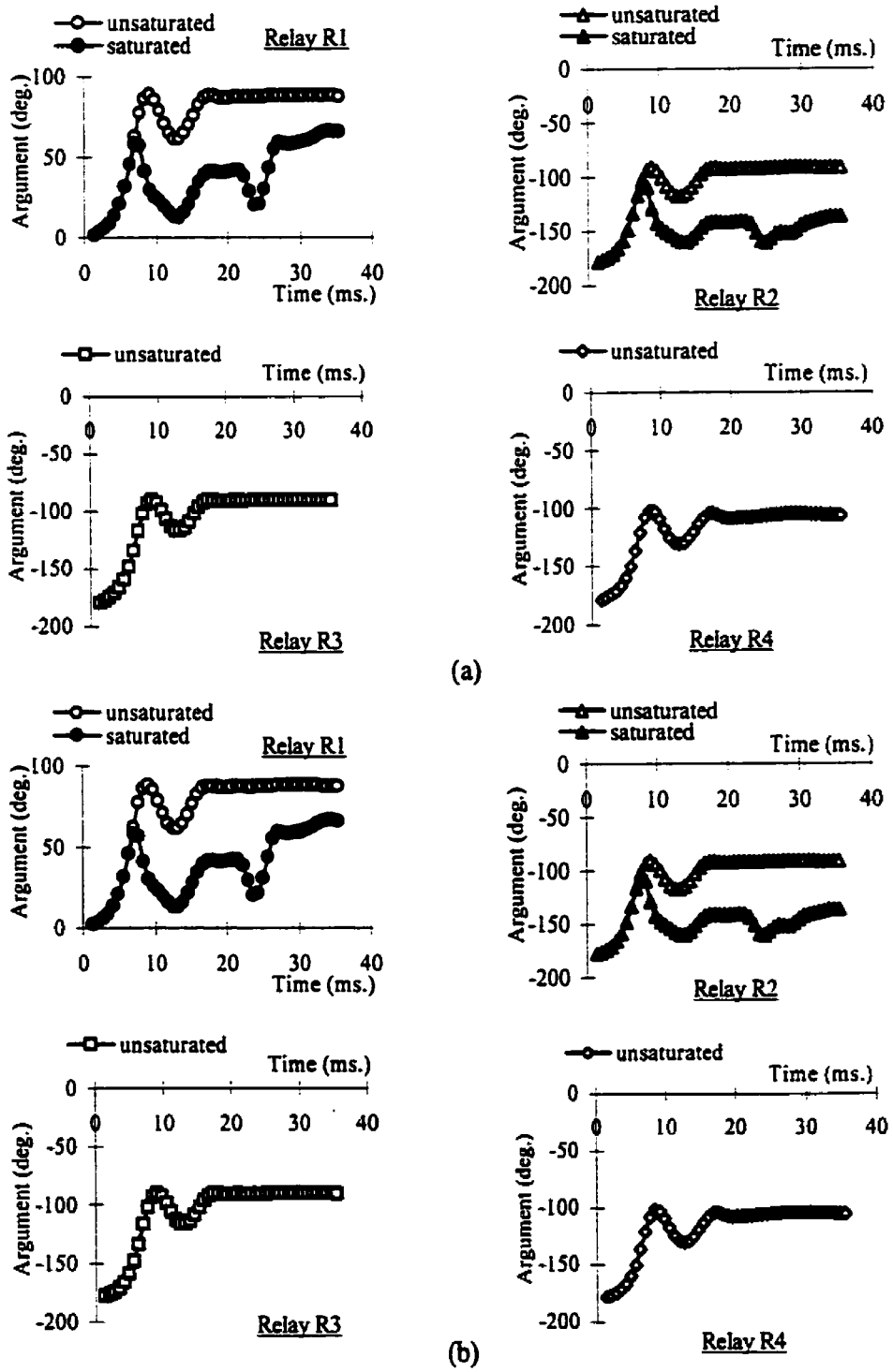


Figure G.19. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase A-ground fault outside the busbar protection zone (location 6) of the substation of Figure 5.3.

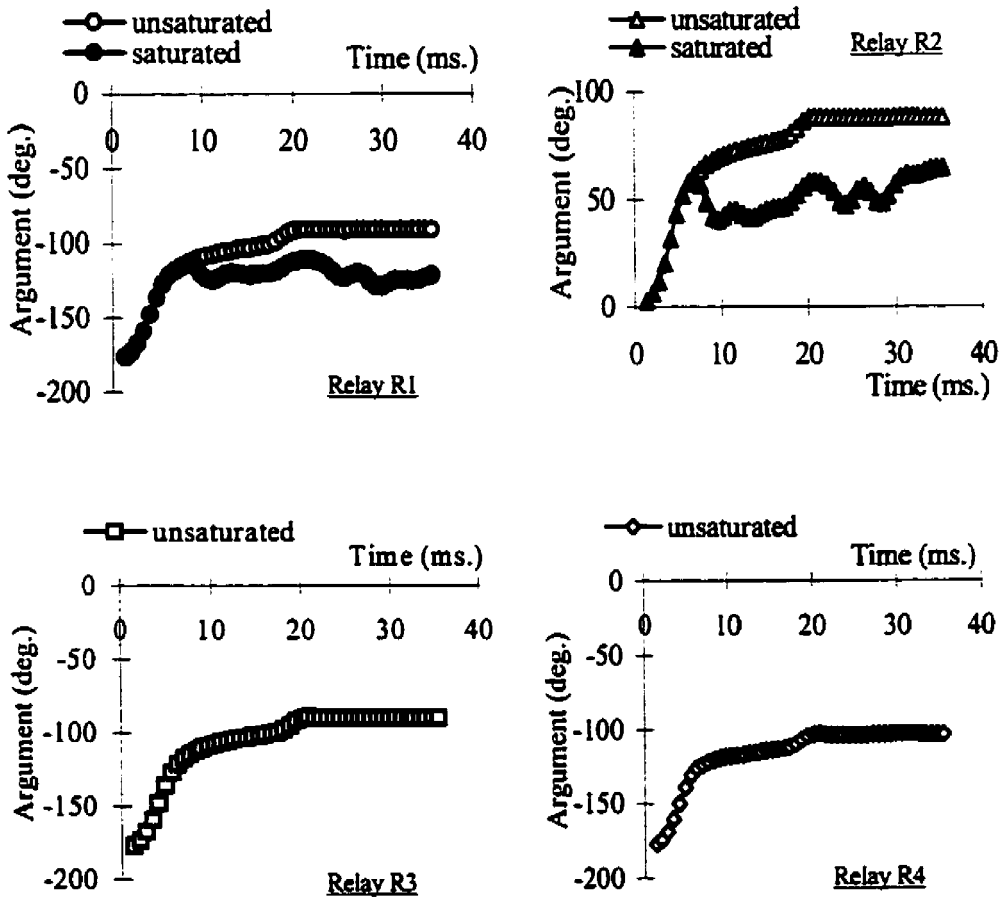


Figure G.20. Plots of the arguments of the positive-sequence impedances computed by the relays for a three phase fault outside the busbar protection zone (location 4) of the substation of Figure 5.7.

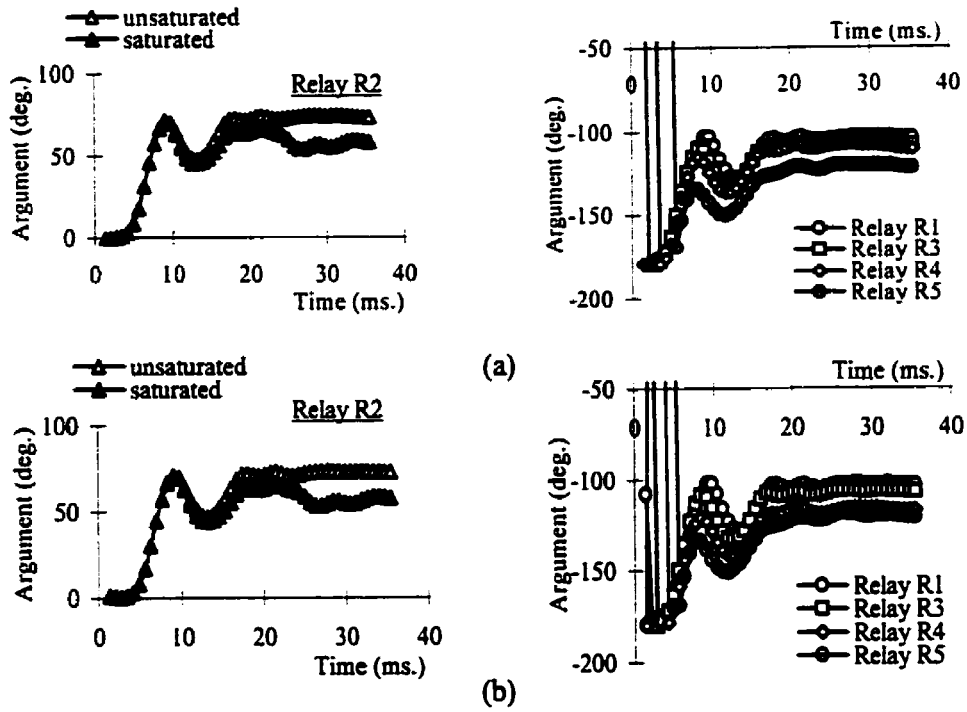


Figure G.21. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase A-ground fault at location 1 of the system containing BRADA substation.

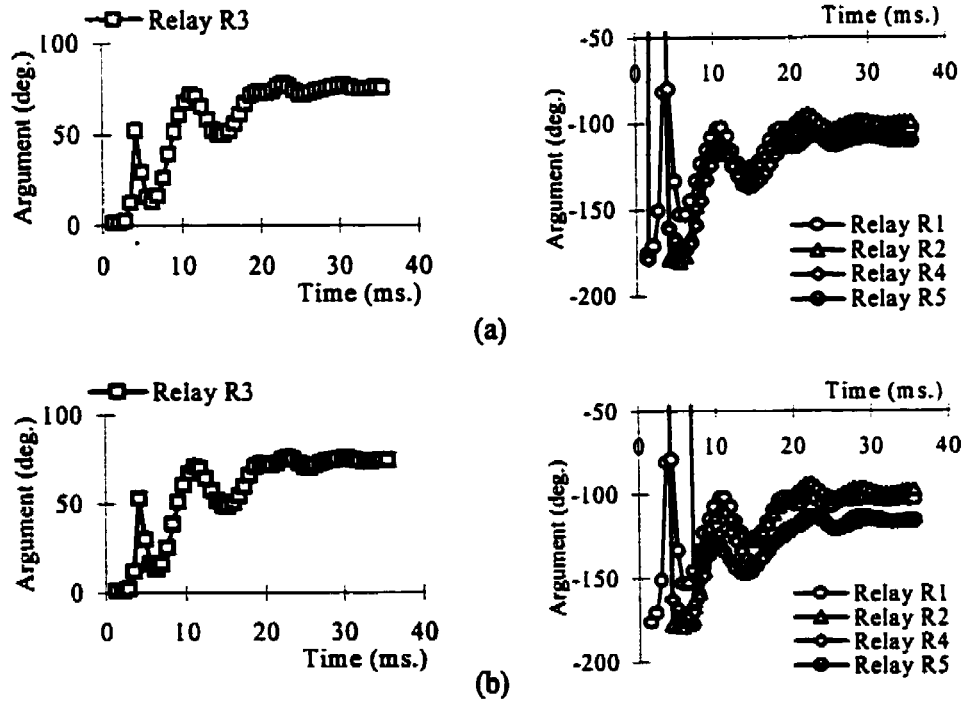


Figure G.22. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase A-Phase C fault at location 2 of the system containing BRADA substation.

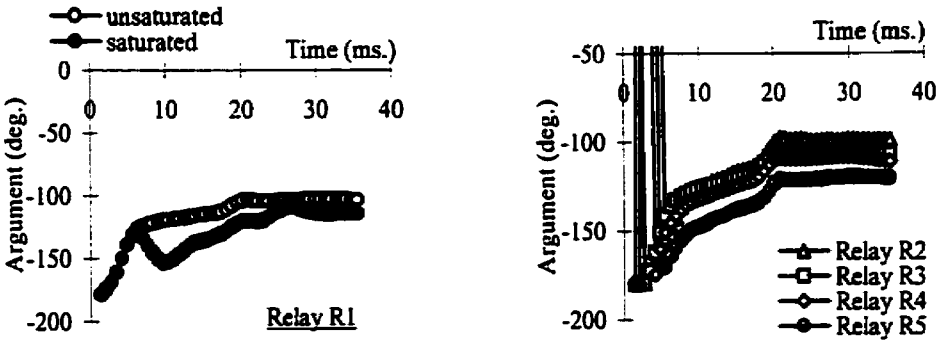


Figure G.23. Plots of the arguments of the positive-sequence impedances computed by the relays for a three phase-ground fault in the busbar protection zone (location 3) of the BRADA substation.

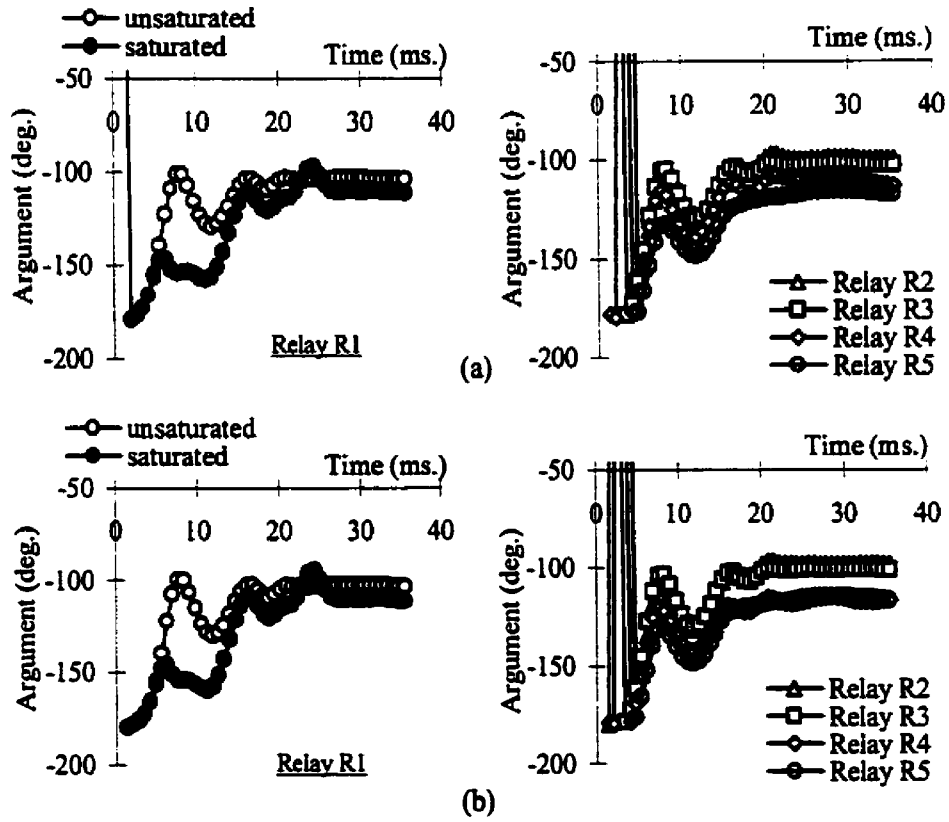


Figure G.24. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase B-ground fault at location 4 of the system containing BRADA substation.

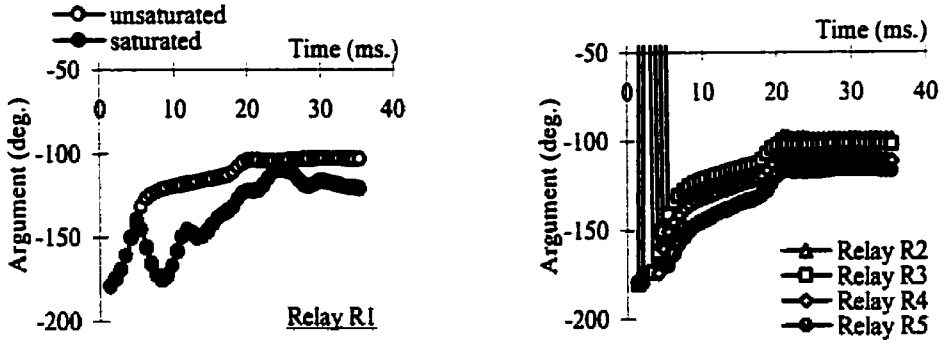


Figure G.25. Plots of the arguments of the positive-sequence impedances computed by the relays for a three phase fault in the busbar protection zone (location 5) of the BRADA substation.

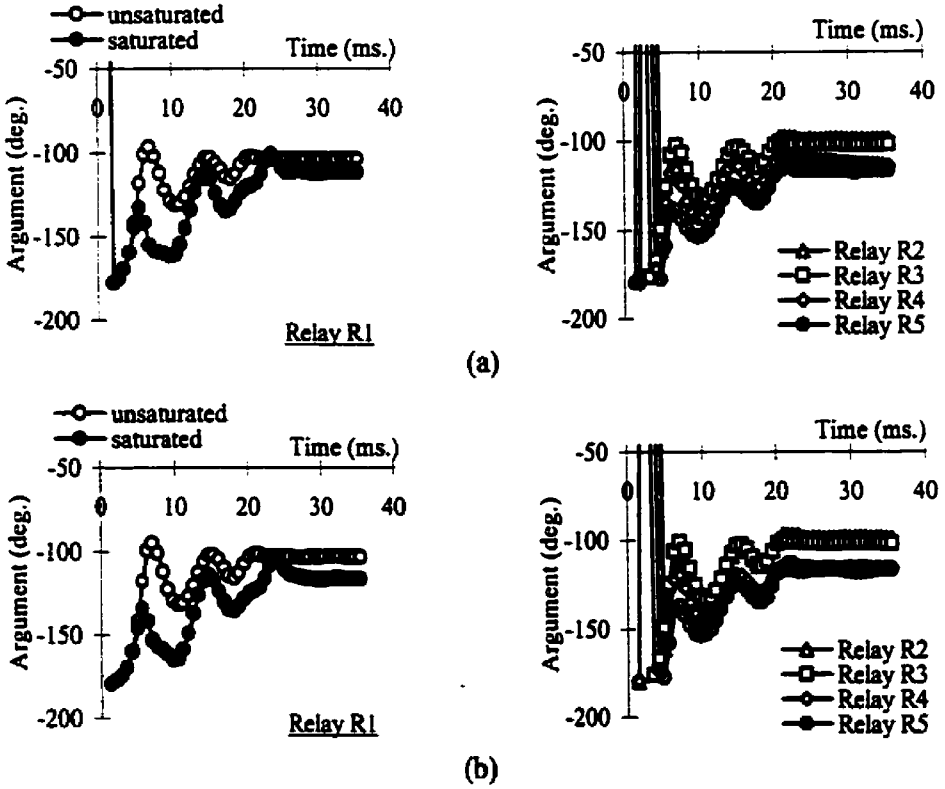


Figure G.26. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase B-Phase C fault in the busbar protection zone (location 6) of the BRADA substation.

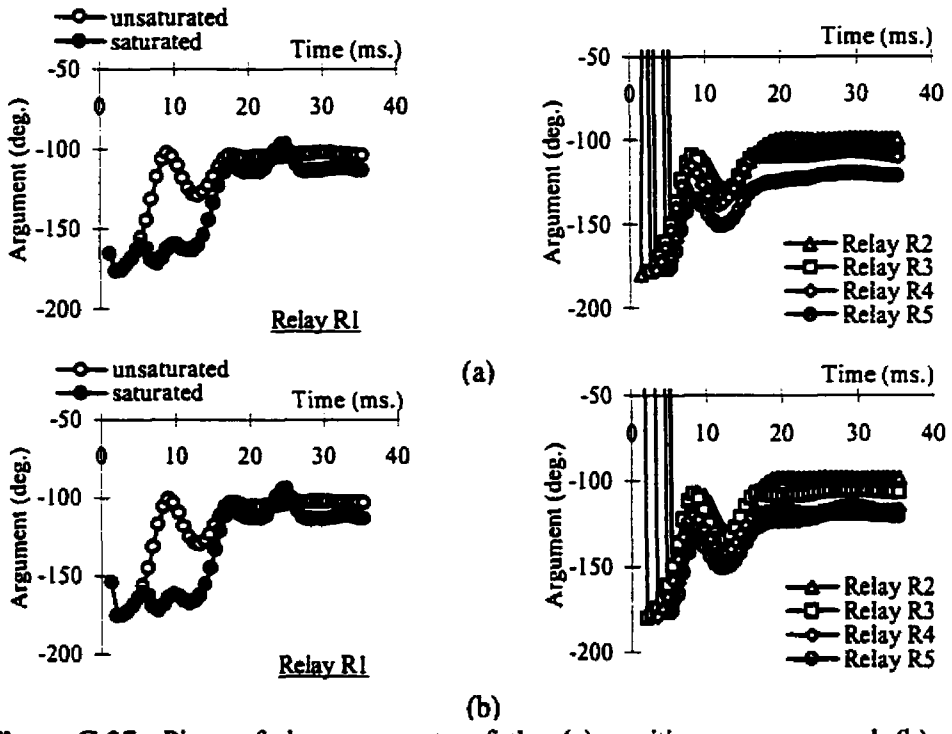


Figure G.27. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase A-ground fault in the busbar protection zone (location 7) of the BRADA substation.

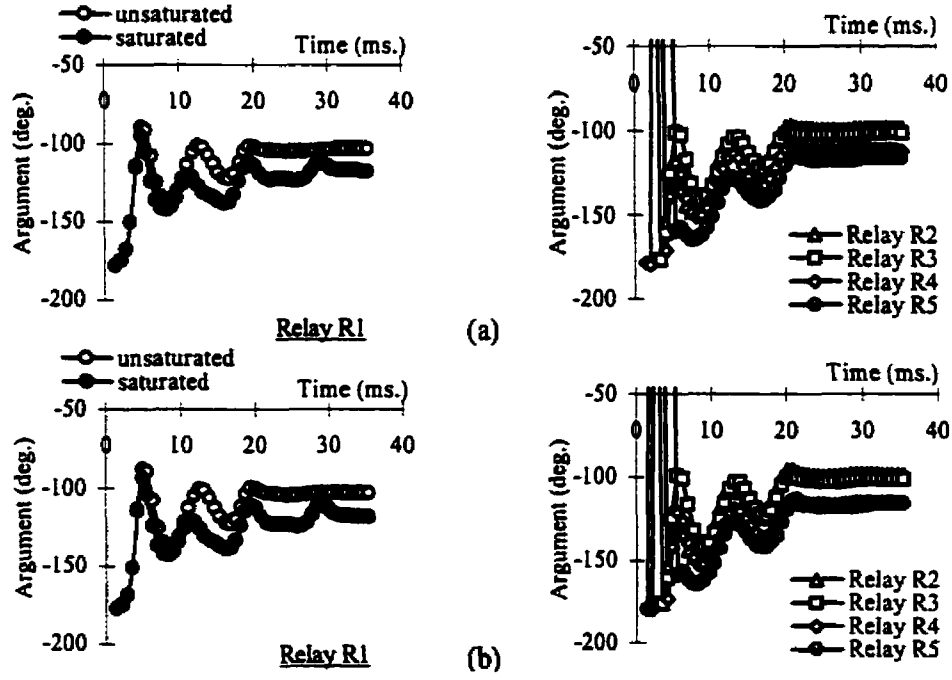


Figure G.28. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase C-ground fault in the busbar protection zone (location 8) of the BRADA substation.

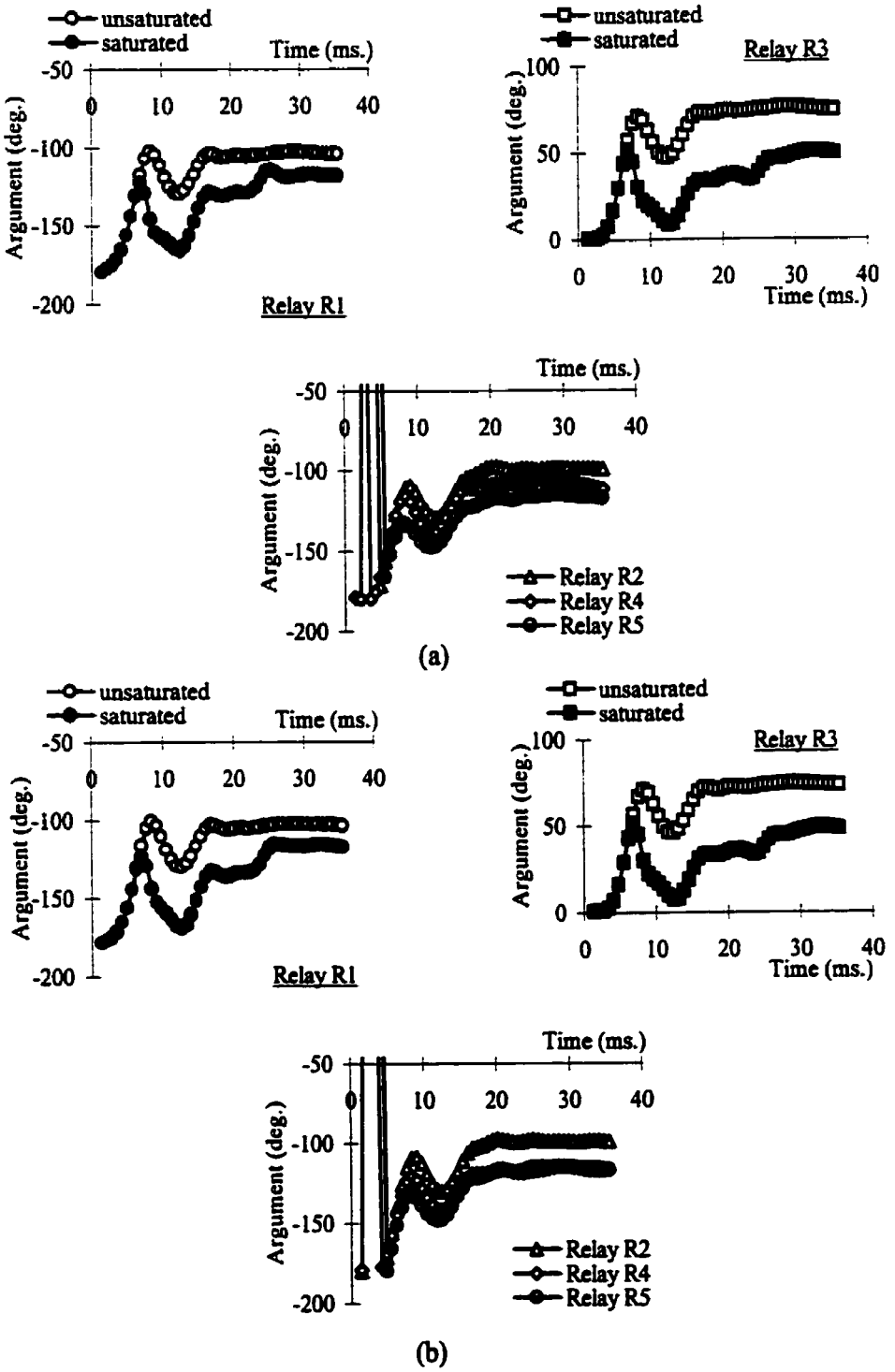


Figure G.29. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase A-Phase B fault at location 9 of the system containing BRADA substation.

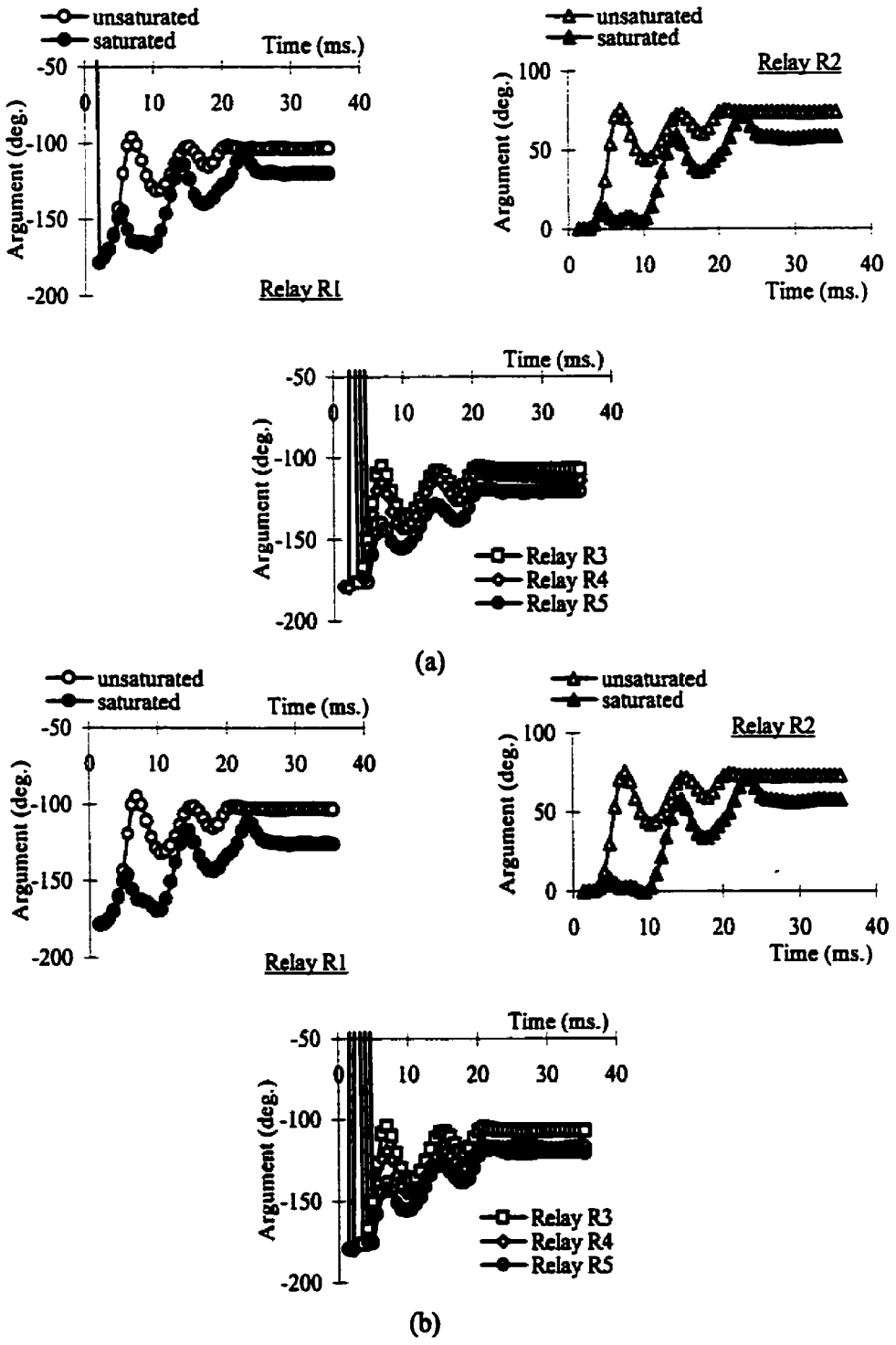


Figure G.30. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase B-Phase C fault at location 10 of the system containing BRADA substation.

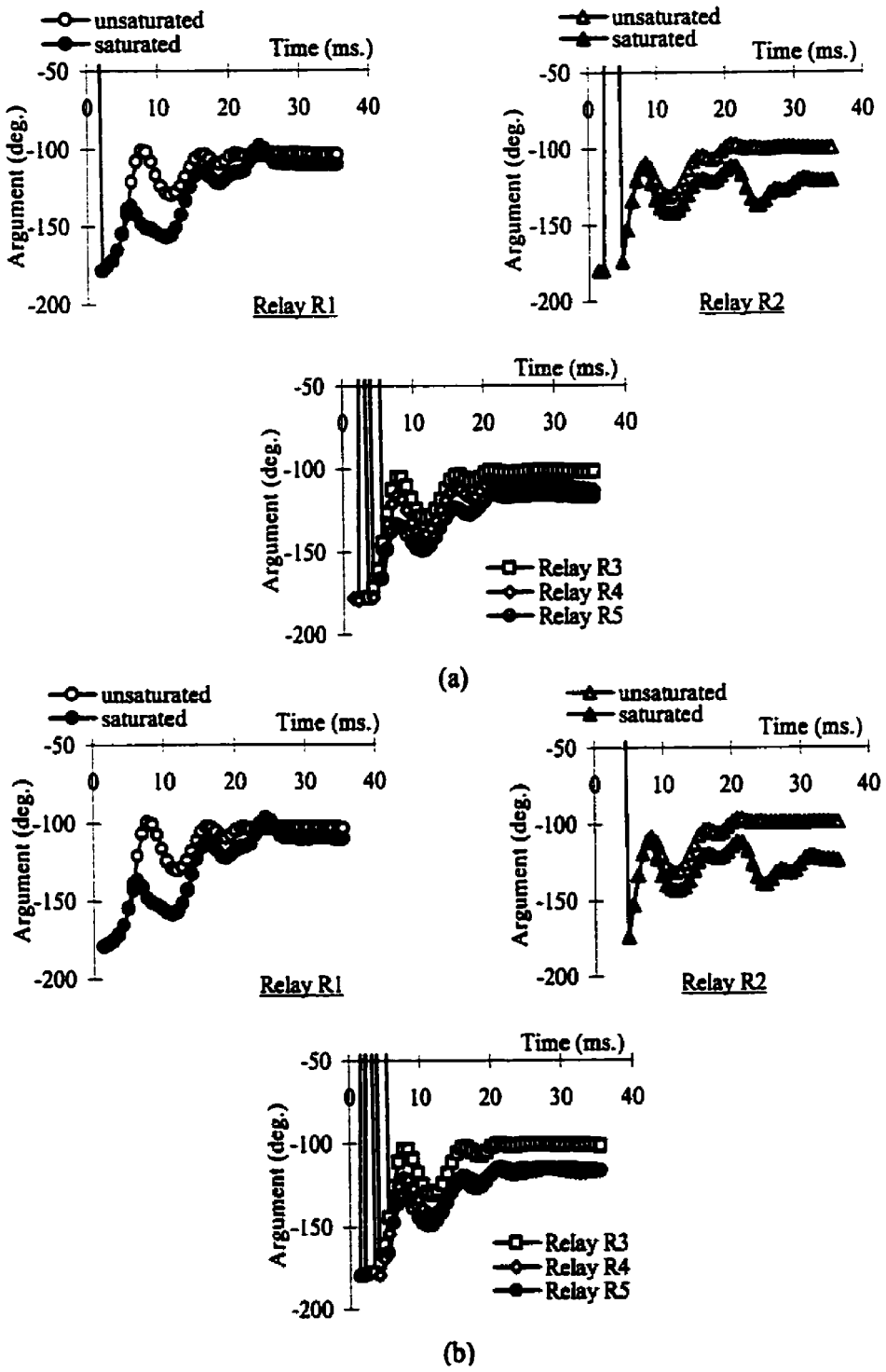


Figure G.31. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase B-ground fault in the busbar protection zone (location 5) of the BRADA substation.

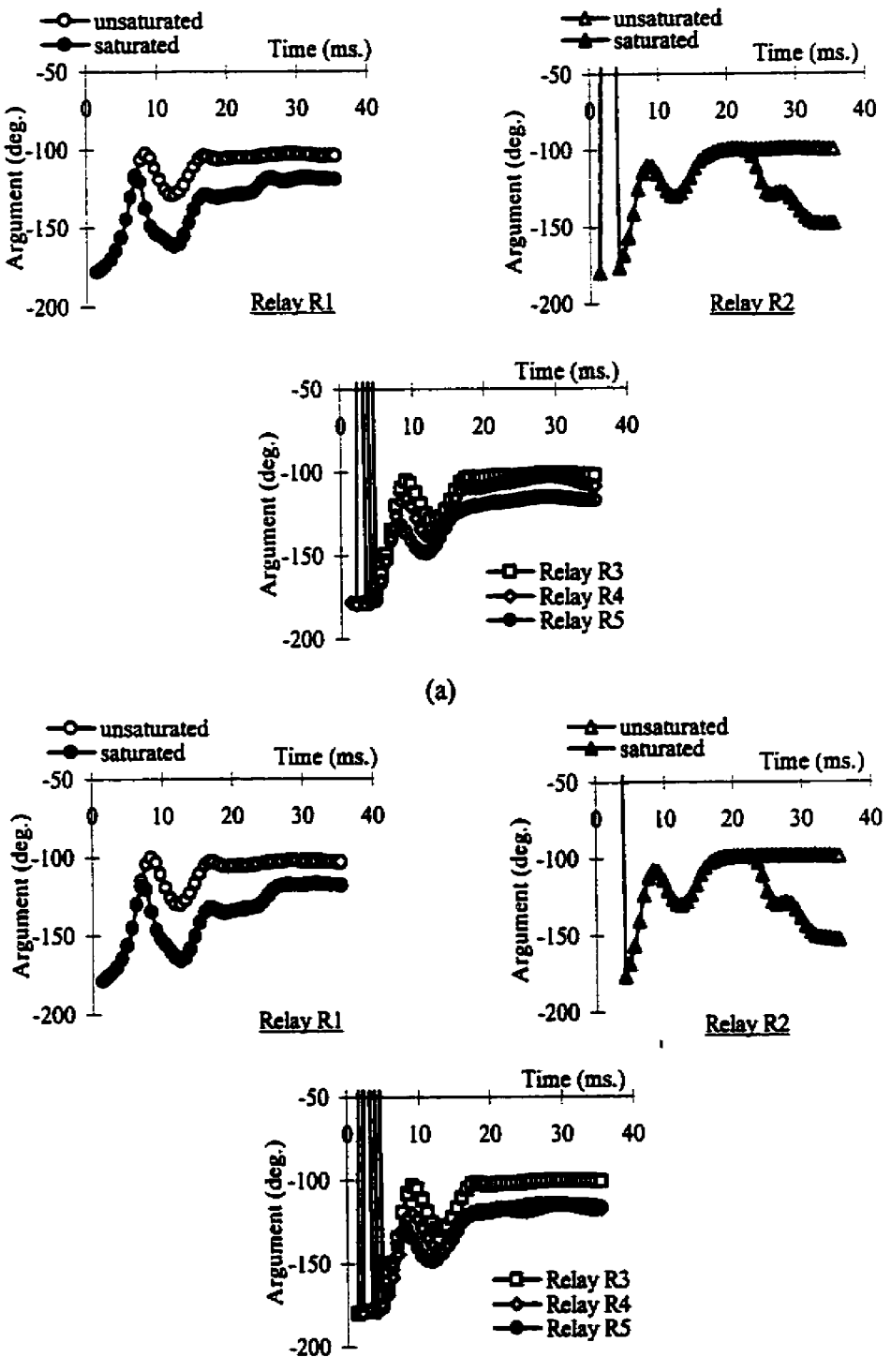


Figure G.32. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase A-Phase B fault in the busbar protection zone (location 8) of the BRADA substation.

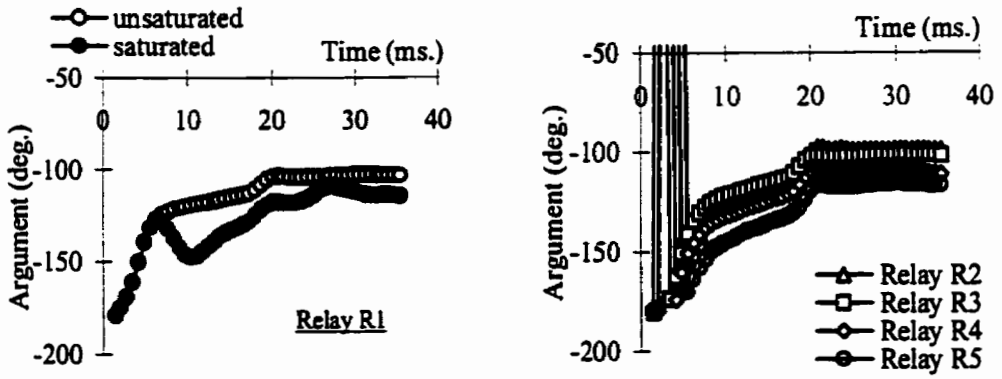


Figure G.33. Plots of the arguments of the positive-sequence impedances computed by the relays for a three phase fault in the busbar protection zone (location 18) of the BRADA substation.

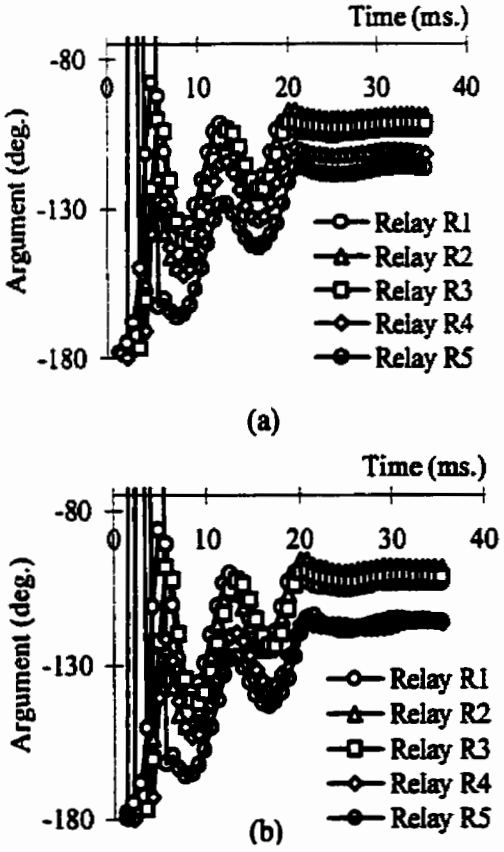


Figure G.34. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase C-ground fault in the busbar protection zone (location 11) of the BRADA substation.

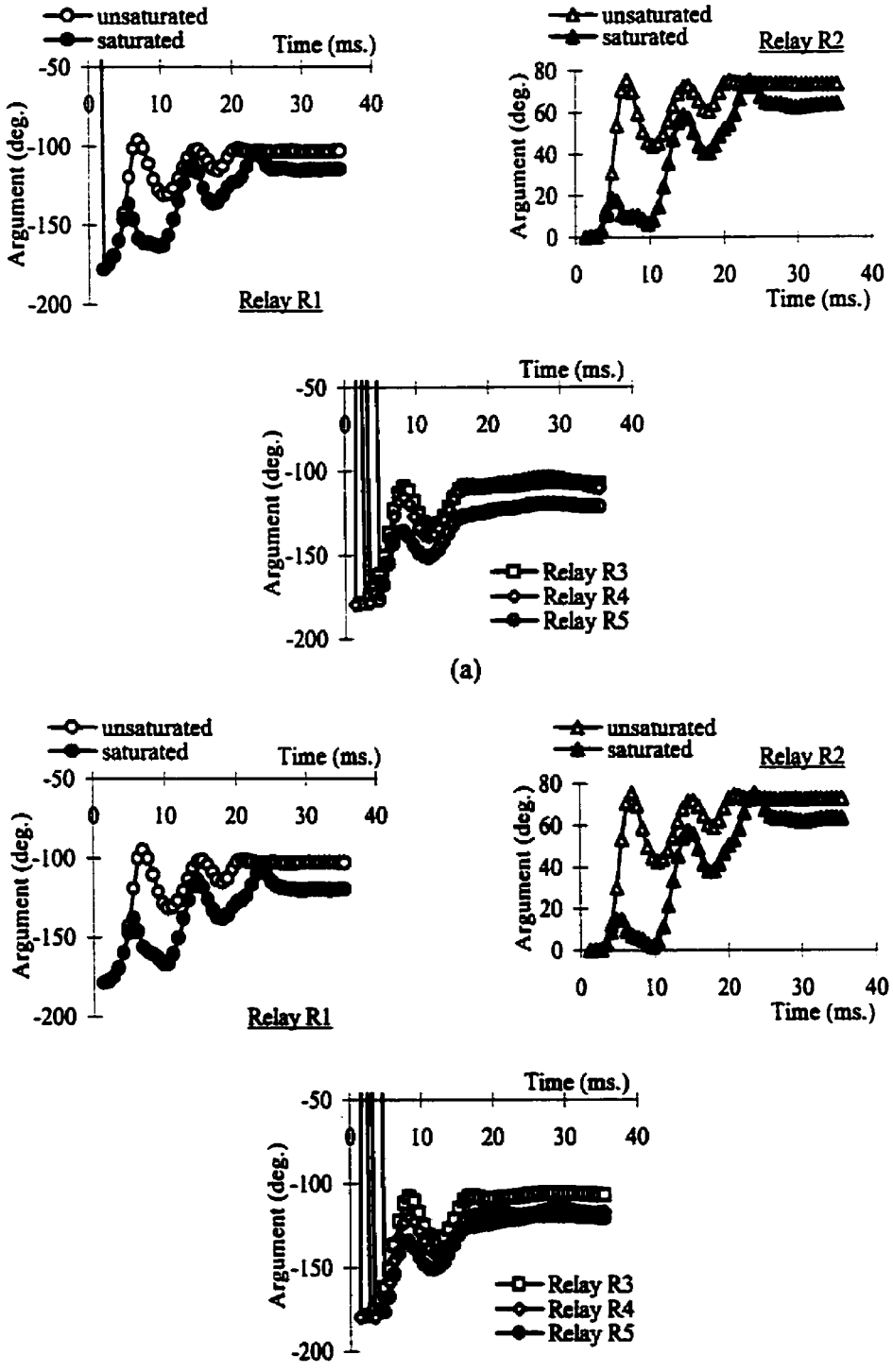


Figure G.35. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase B-Phase C fault at location 10 of the system containing BRADA substation.

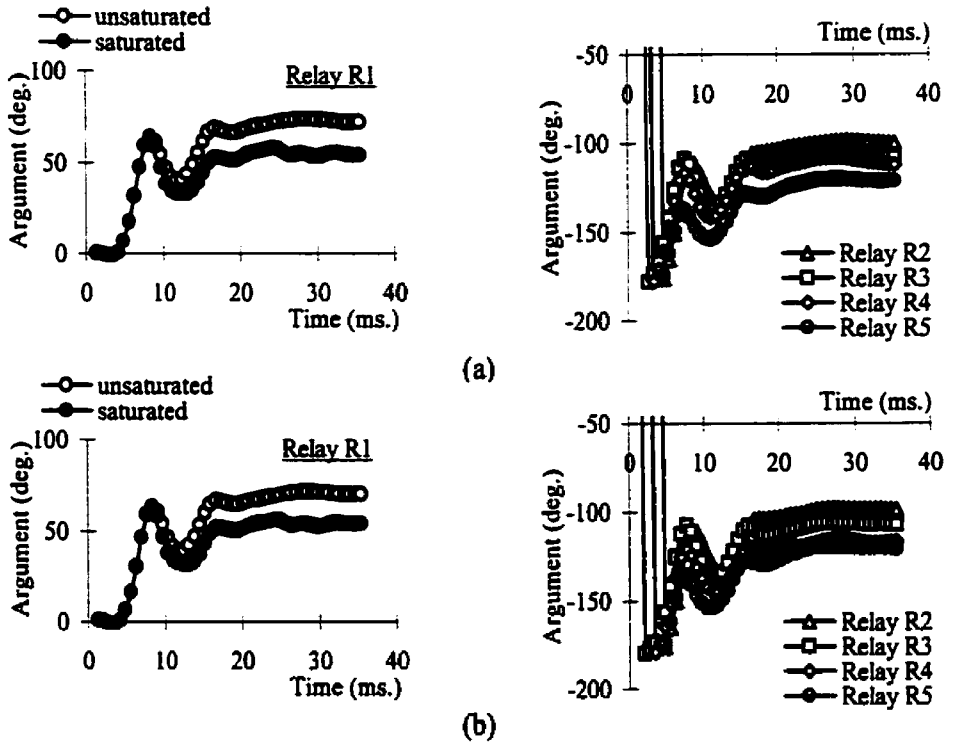


Figure G.36. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase A-ground fault at location 17 of the system containing BRADA substation.

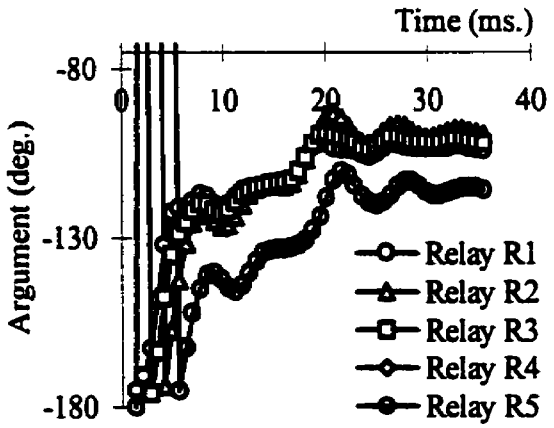


Figure G.37. Plots of the arguments of the positive-sequence impedances computed by the relays for a three phase-ground fault at location 15 of the system containing BRADA substation.

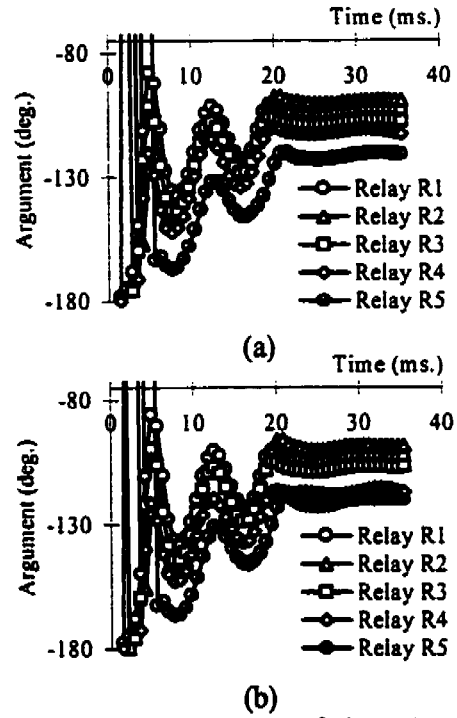


Figure G.38. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase C-ground fault in the busbar protection zone (location 6) of the BRADA substation.

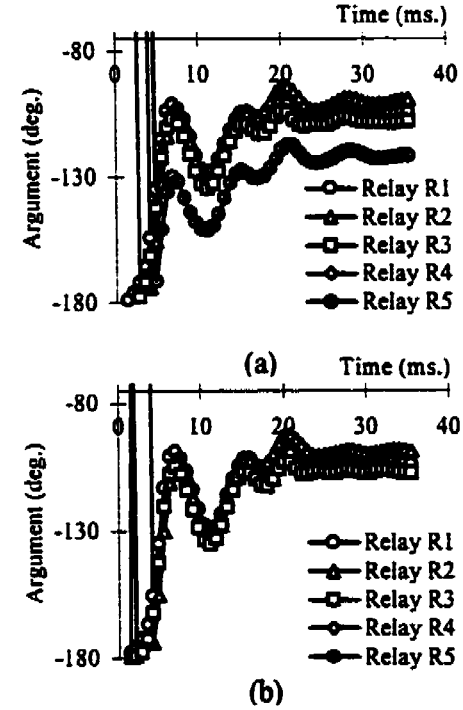


Figure G.39. Plots of the arguments of the (a) positive-sequence and (b) negative-sequence impedances computed by the relays for a Phase B-ground fault at location 15 of the system containing BRADA substation.

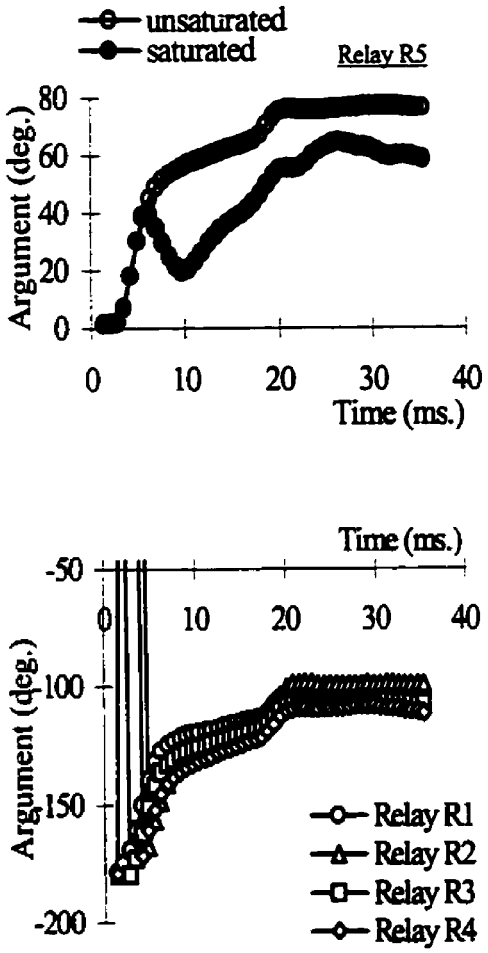


Figure G.40. Plots of the arguments of the positive-sequence impedances computed by the relays for a three phase fault at location 16 of the system containing BRADA substation.

Appendix H. TESTING THE RELAYING SOFTWARE

This section gives a brief overview of the TMS320C30-based system that was used for testing the relaying software. An IBM-compatible PC was used as the host machine in the system. The TMS320C30 Evaluation Module (EVM) is a development tool from Texas Instruments and was used for executing and debugging applications program using the TMS320C30 C source debugger. Floating-point DSP applications can be evaluated and developed using the module. Each EVM includes a PC bus compatible card and software package.

H.1 Hardware

The hardware components of the EVM card include:

TMS320C30, a 33-MFLOPS, 32-bit floating-point DSP,

16K-word zero-wait-state SRAM, allowing on-board coding of the algorithms,

Port for host-PC communications and

Multiprocessor serial port providing connections to multiple EVMs.

Loading of the code is done through the emulation port. A shared bi-directional 16-bit register is used for communication between the host and TMS320C30 after the code has been loaded since there is no direct host access into the TMS320C30 memory. The TMS320C30 has direct interface to SRAM which supports zero wait-state memory accesses on primary bus.

H.2. Software

The system has software tools to develop, debug, benchmark and run real-time algorithms. These include the TMS320C3x assembler/linker, C source debugger and an optimizing ANSI C compiler, a program loader and example applications software.

The EVM provides a window-based mouse-driven user-interface that enables downloading, execution and debugging of assembly code or C code.

H.3. Testing Procedure

Testing of the relaying software was performed using code generation and execution steps. The ANSI C program written for the relaying software was converted to the DSP code, which is executed after loading into the DSP.

The TMS320C30 floating-point C compiler consists of three different programs: the parser, the optimizer (optional), and the code generator. C source file is an input to the parser which checks for syntax and semantic errors, and produces an internal representation of the program called an intermediate file. The optimizer is an optional pass that is executed before code generation.

The intermediate file provides input to the optimizer which produces a highly efficient version of the code in the same format as the intermediate file. The intermediate file from parser or optimizer (if used) provides input to the code generator. The code generator produces an assembly language source file. This provides input to an assembler which generates a Common Object File Format (COFF) file. The output file from assembler provides an input to the linker which produces an executable COFF object file <program_name.out> [70, 71].

DSP Code Generation Process

1. Develop the relaying software in ANSI C programming language.
2. Include a data file from PSCAD simulation into the relaying software.
3. Compile, assemble, and link the C source file using the single command:

   cl30 <program_name.c> -z <program_name.cmd>

<program_name.cmd> represents the command file used to allocate blocks of code and data into the memory. This is necessary while linking the program. In general, initialized sections (e.g. executable code, tables for preinitializing variables, strings constants) are linked into ROM or RAM whereas uninitialized sections (e.g. global variables, system stack, dynamic allocation using malloc, calloc) must be linked into RAM.

After code generation process, three files are generated: <program_name.obj>, <program_name.map>, and <program_name.out>. The map file, <program_name.map>, shows the memory configuration, section composition and allocation, and various symbols used in the program with their storage addresses in the memory. The file with extension 'obj' is an executable object file. The output file, <program_name.out> is loaded into the memory of the TMS320C30 DSP for execution.

Execution of the DSP Code

1. The output file, <program_name.out>, from the linker is loaded into the evaluation module (EVM) in TMS320C30-based DSP board using the commands given below:

   evm30
   reset
   load <program_name.out>

2. The loaded file is executed by using the 'run' command and the execution can be stopped by pressing the <escape> key.

3. The variables of interest can be displayed using following commands:

   disp *(int *) 0x000XXX , for integer variables or
   disp *(float *) 0x000XXX , for floating-point variables.

   0x000XXX is the memory address at which the selected variable resides and is known from the map file. Variable name can be used instead of memory address.

4. Time taken to run the program on DSP can be obtained by using the process of benchmarking. Benchmarking involves creating breakpoints at the start and the end of the program and is carried out using the following command steps:

   evm30
   reset
   load <program_name.out>
   ba 0x000XXX (0x000XXX is the program start memory location)
   ba 0x000YYY (0x000YYY is the program end memory location)

```
run
runb
? CLK
```

Complete program execution time including all passes through the program, in number of clock cycles of the DSP, is displayed on the screen. Program execution time in millisecond is calculated from the single-cycle instruction execution time which is 60 nanosecond for the TMS320C30. Time taken to execute a section of the program can also be calculated by using a similar procedure.

Appendix I. REAL TIME PLAYBACK (RTP) SIMULATOR

This section gives a brief overview of the Real Time Playback (RTP) Simulator from the Manitoba HVDC Research Centre. This simulator plays back, in real time, test signals generated from PSCAD/EMTDC power systems simulation software (Appendix E) or on-line recordings in COMTRADE format. These digital signals are converted into analog signals which are used for testing real-time systems including protective relays, fault location and other monitoring systems. The RTP Simulator was used for testing the implemented busbar protection system. Hardware and software aspects of the system are described below.

I.1 Hardware

The hardware is composed of a standard personal computer (PC) package fitted with the necessary additional hardware cards and output/input ports. The system is composed of four separate components: a tower case, display monitor, keyboard and mouse pointing device. The tower case encloses, among others, the following main items:

150 MHz Intel Pentium processor,
2.1 GB Hard Drive,
8x CD-ROM,
32 MB RAM
1.4 MB Floppy Drive,
National Instruments 10-channel, 12-bit D/A (Digital to Analog) card and
Front panel with 10 BNC connectors for access to the D/A card outputs.

I.2. Software

The operating system of the PC that is used as RTP Simulator is Microsoft Windows for Workgroups Version 3.11. In addition to a number of other programs, the main RTP software package (version 1.2) is also installed in a separate directory. This software enables interfacing with PSCAD/EMTDC (version 2.0) power systems

simulation software. The waveforms of the signals that are loaded from PSCAD for playback can be previewed using this software. On user command, the software plays these signals back through the output connectors.

The RTP Simulator software package includes an installation routine that introduces a recorder icon into the component pallet in DRAFT module of the PSCAD. There can be up to 9 recorders in a given power system simulation each having a maximum of 10 analog channels. System parameters to be recorded are selected by the user along with start and end times. The recordings can be user selected for COMTRADE or RTP format. The recordings are stored in a separate file, during Runtime. The name of the file is selected by the user in the recorder icon in DRAFT module. The standard PSCAD output ASCII file is not affected by this process.

The generated recording file (with extension PBK) is then ported to the RTP Simulator for playback. Porting of these files can be done through the network connections or by the use of floppy disks. The former is preferable for speed of transfer and to avoid the size limitation of floppy disks.

When RTP playback software is started, any previously recorded files can be loaded for viewing on the screen and can be played back. When playback is initiated, RTP Simulator plays the first cycle in each channel repeatedly to create a pre-transient steady state waveform. Once the playback command is given, the RTP Simulator plays the transient data and then plays the last cycle repeatedly to create post-transient waveform. The last cycle is repeated 500 times by default, which can be reduced or increased by users.

Appendix J. ADDITIONAL IMPLEMENTATION RESULTS

Selected results from real-time testing of the proposed system for busbar protection have been presented in Chapter 6. Different types of faults at various locations in the simulated power system were considered. This appendix provides additional implementation results for various types of faults and current transformer conditions. Figures J.1 to J.33 show the plots of the sequence-impedances seen by the relays and the corresponding trip counters. Table 6.2 (in Chapter 6) gives a summary of the results presented in this appendix. This includes the fault location and type, samples required for detecting fault and, positive-sequence and negative-sequence trip counters to reach threshold and the time required by the proposed technique to make final decision on the type of faults.

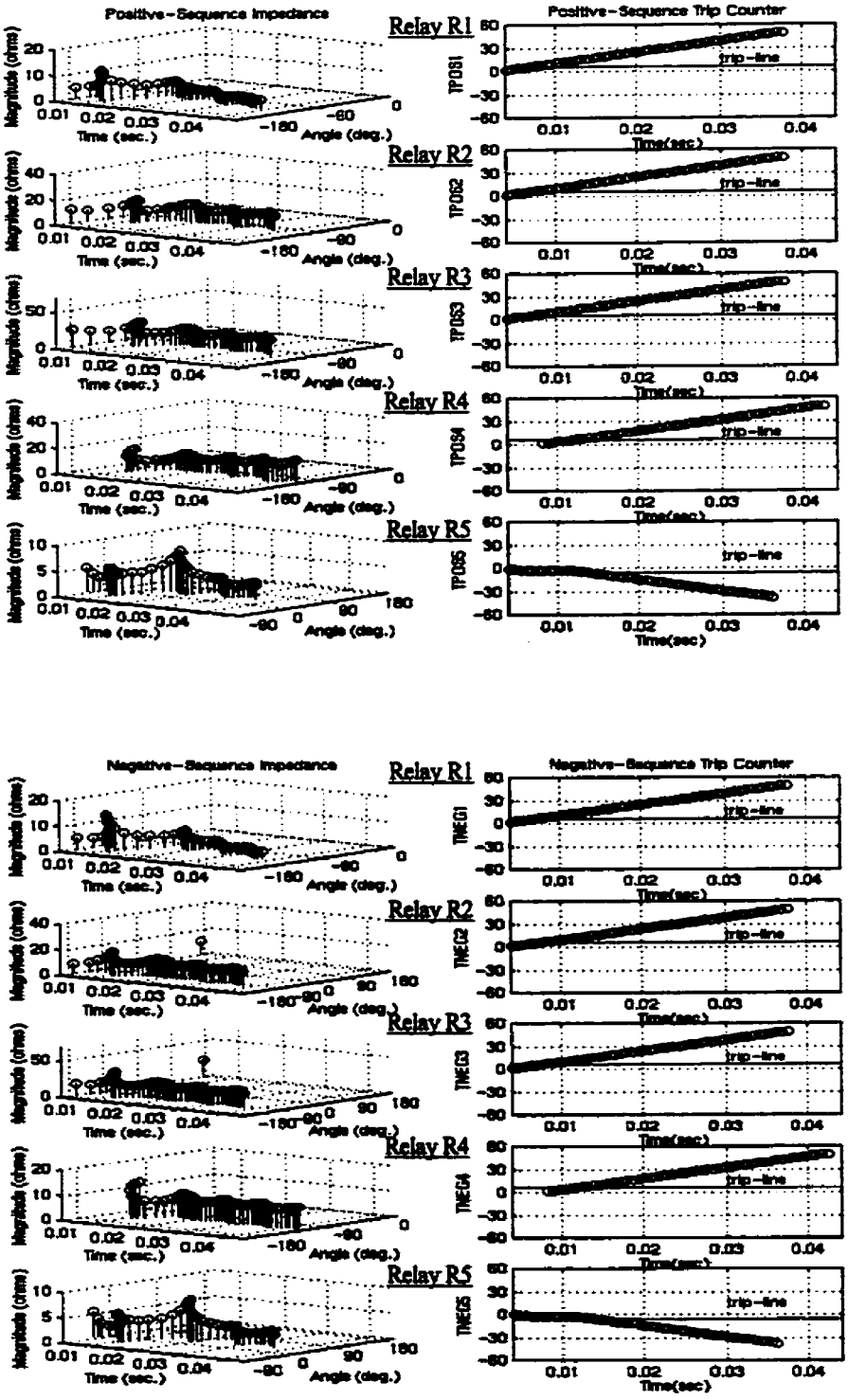


Figure J.1. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase B-ground external fault (location 1, Figure 6.7).

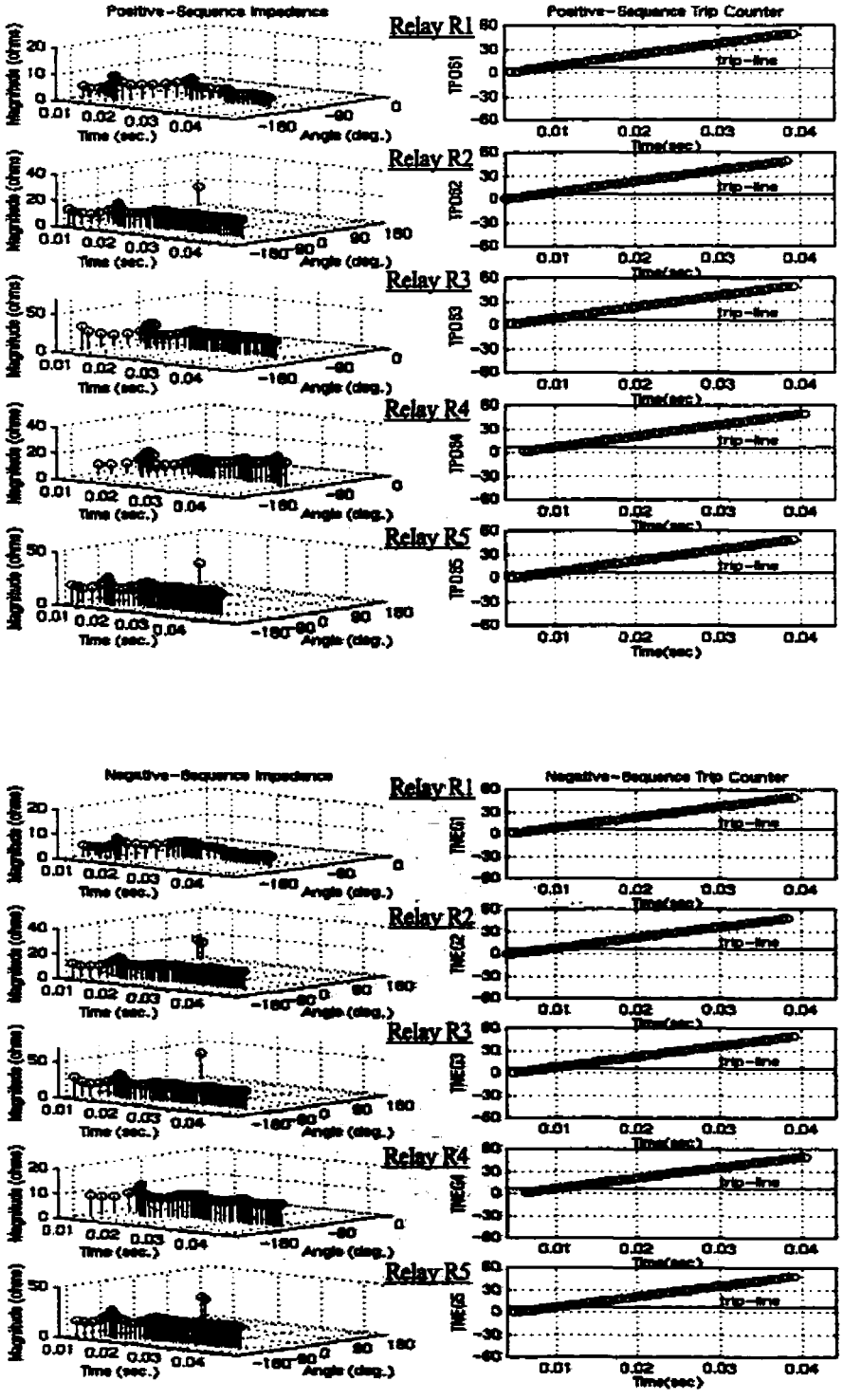


Figure J.2. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-ground internal fault (location 2, Figure 6.7).

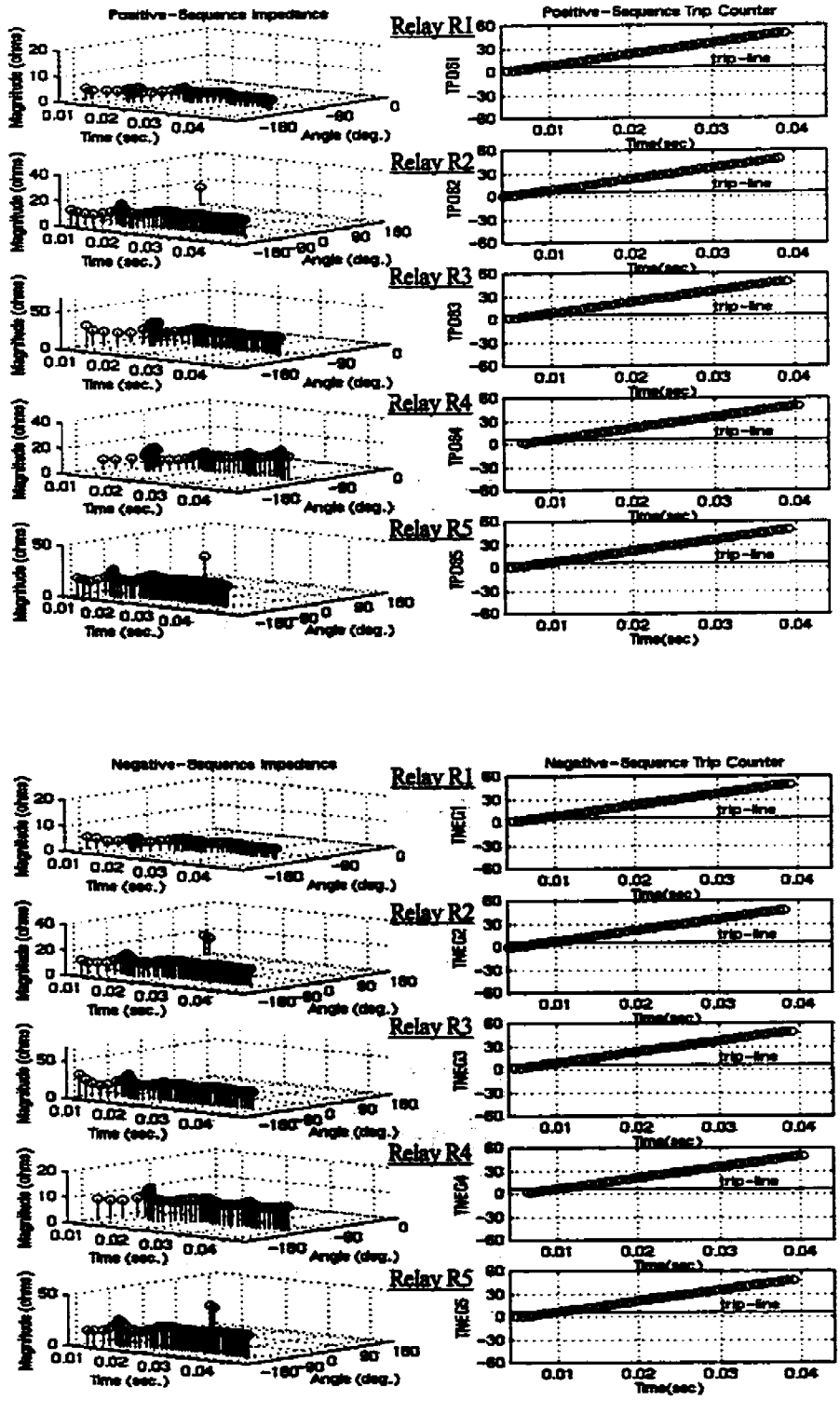


Figure J.3. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-ground internal fault (location 3, Figure 6.7).

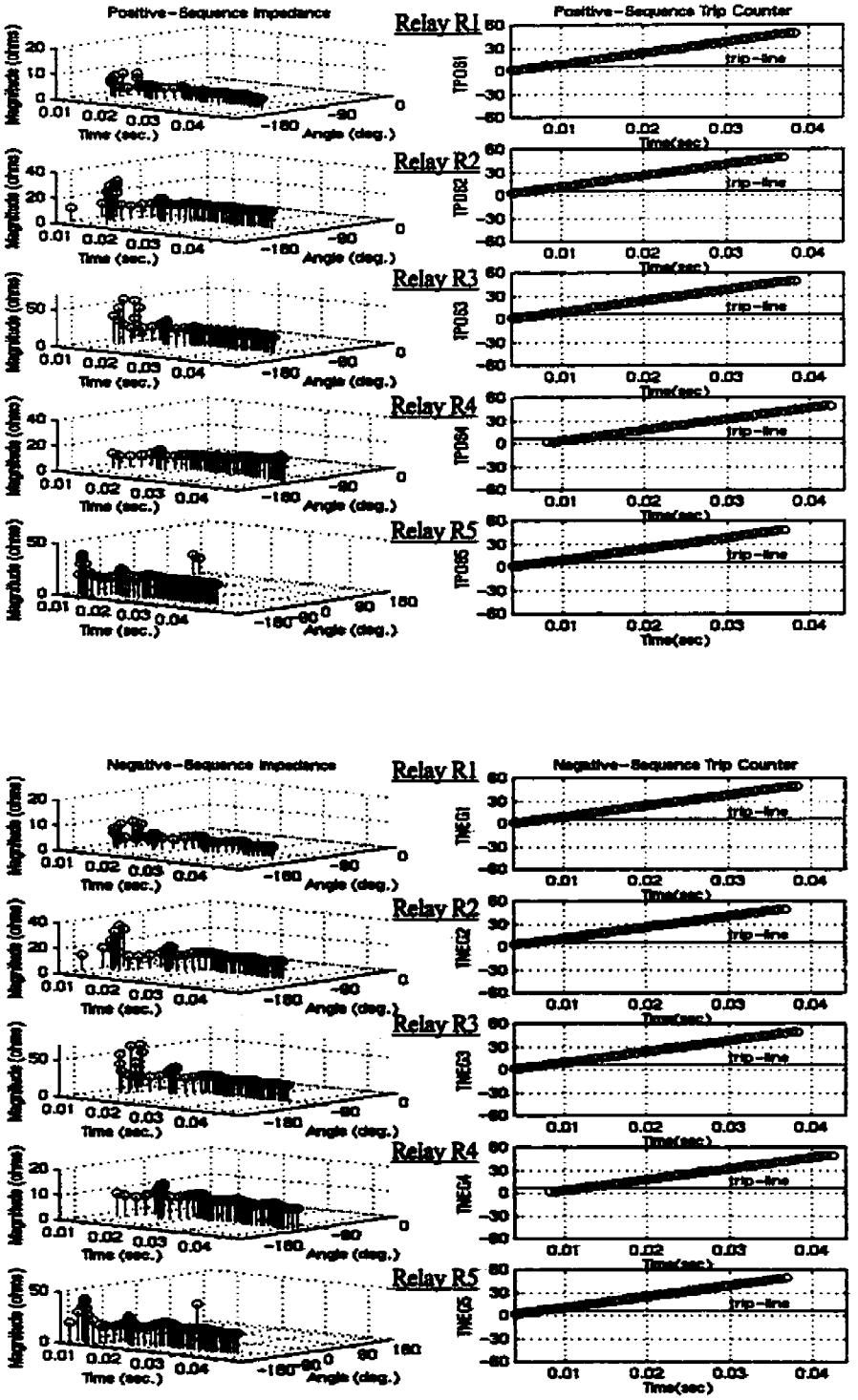


Figure J.4. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase C-ground internal fault (location 4, Figure 6.7).

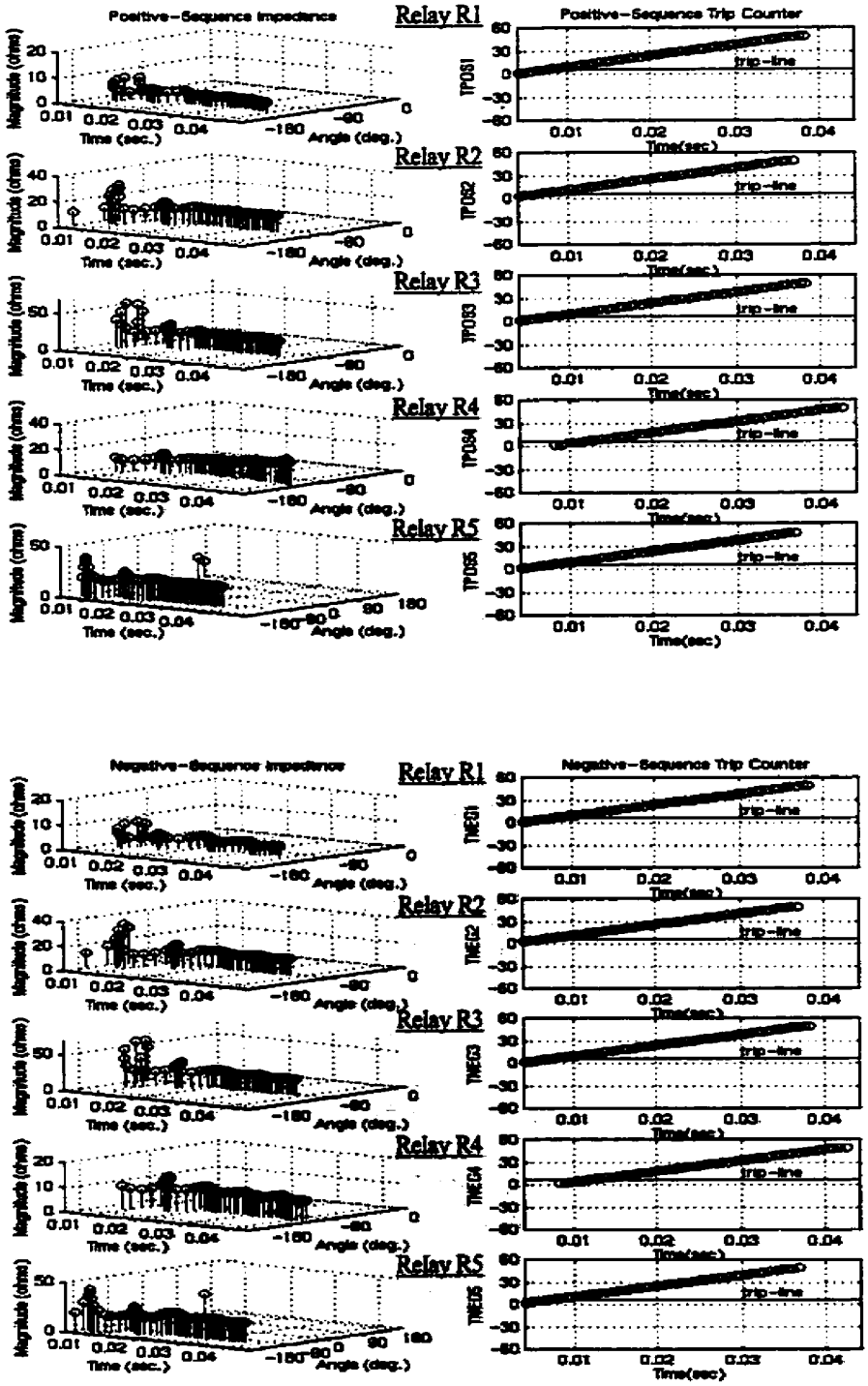


Figure J.5. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-Phase B internal fault (location 5, Figure 6.7).

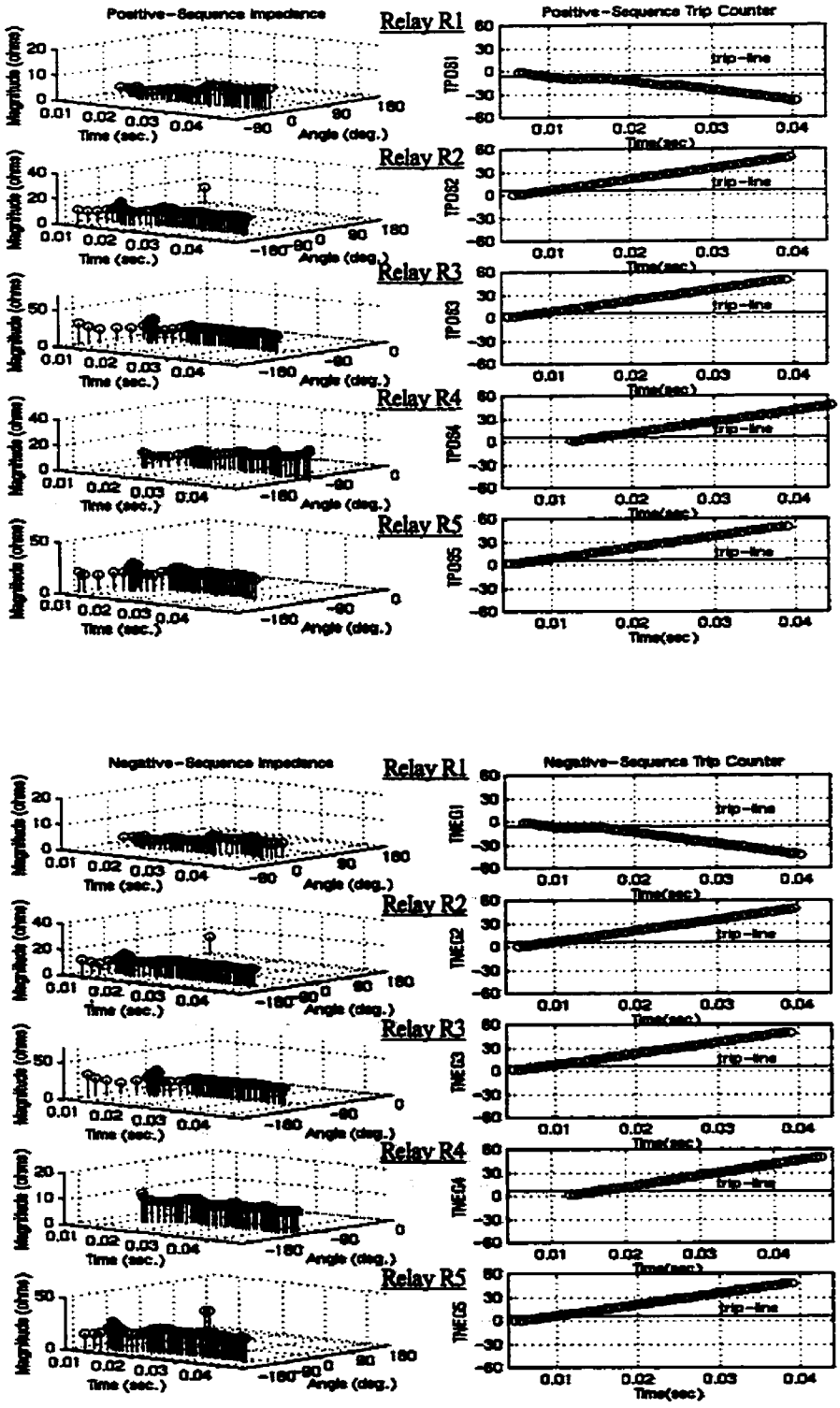


Figure J.6. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-ground external fault (location 6, Figure 6.7).

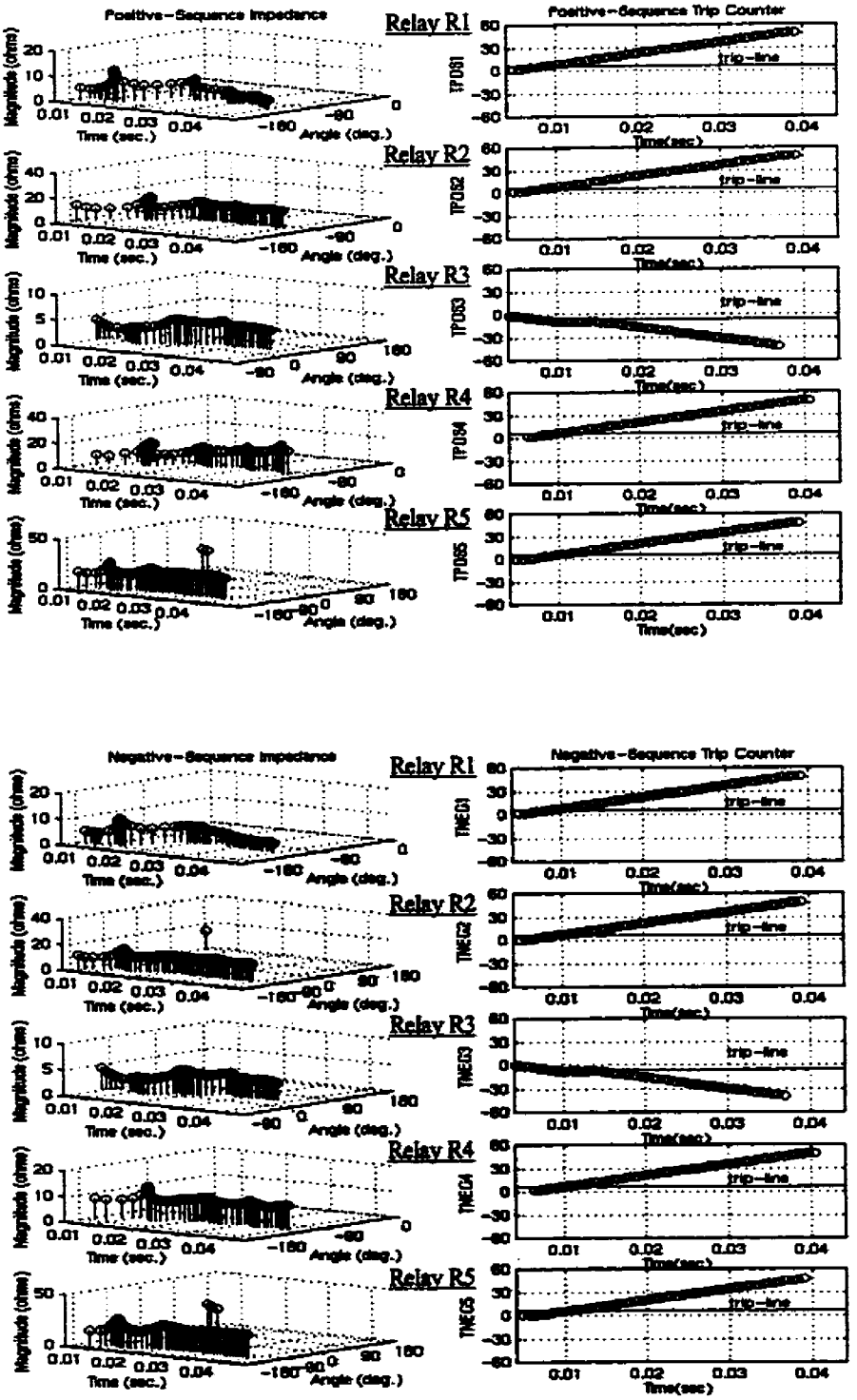


Figure J.7. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-ground external fault (location 7, Figure 6.7).

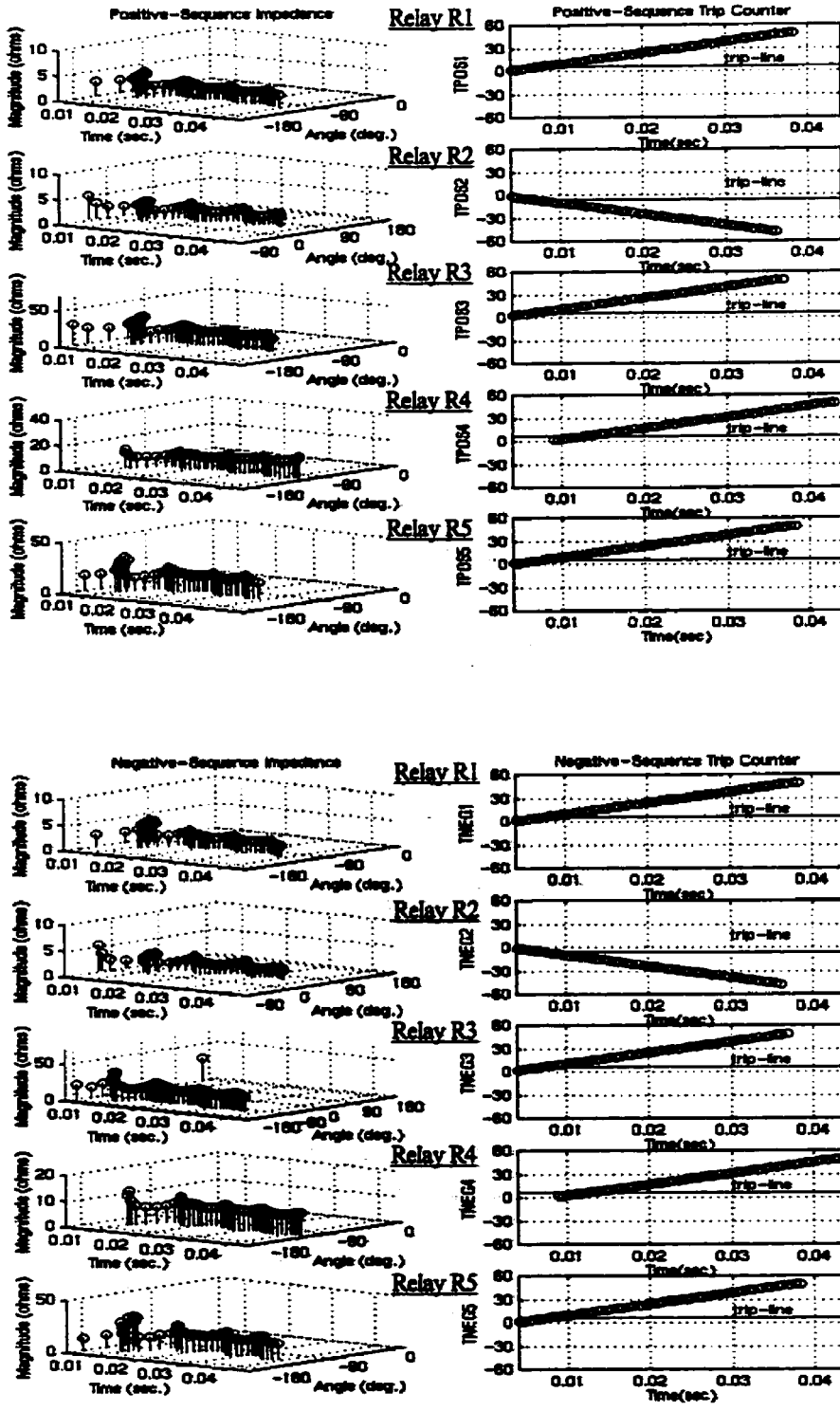


Figure J.8. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase B-ground external fault (location 8, Figure 6.7).

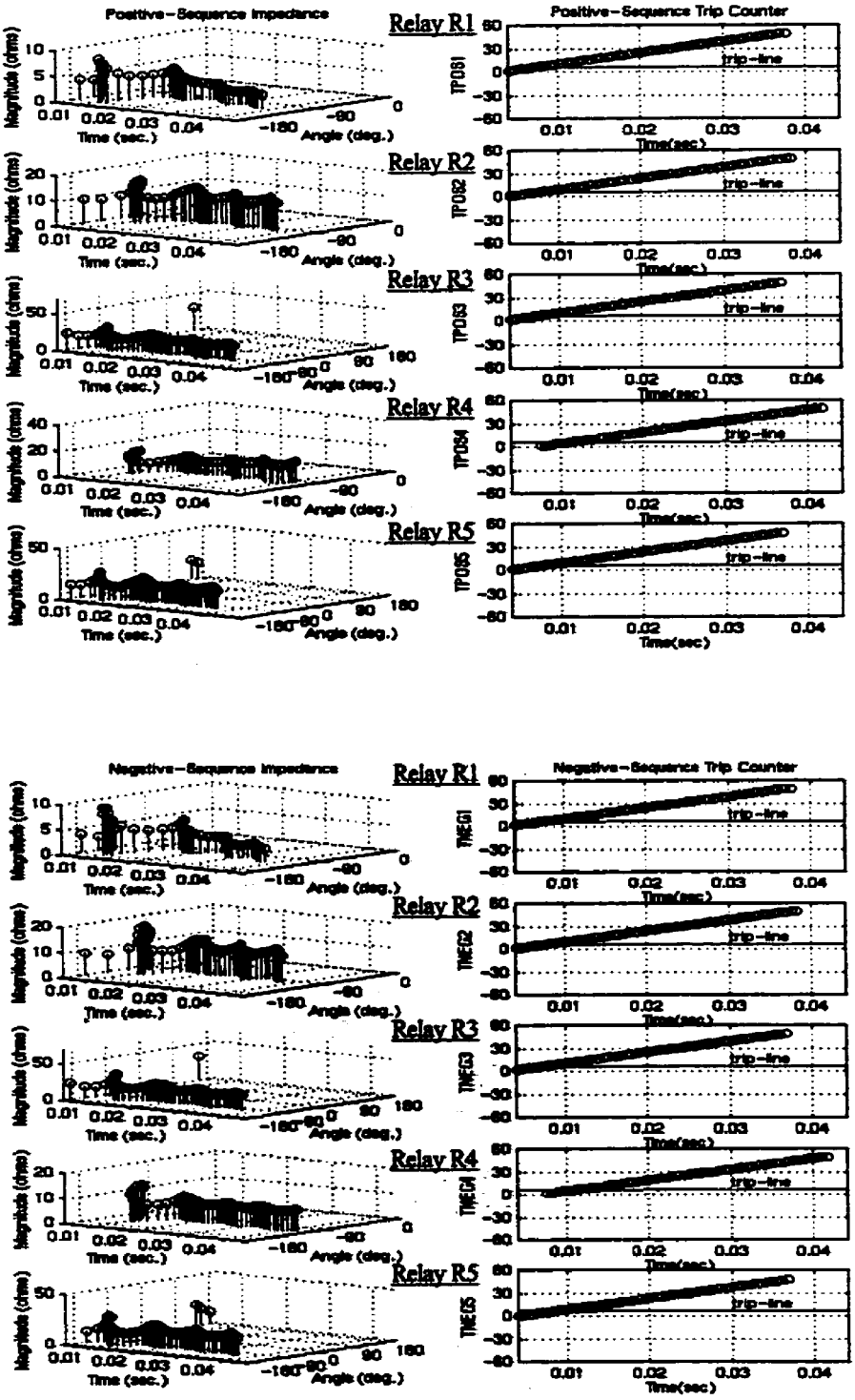


Figure J.9. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase B-ground internal fault (location 9, Figure 6.7).

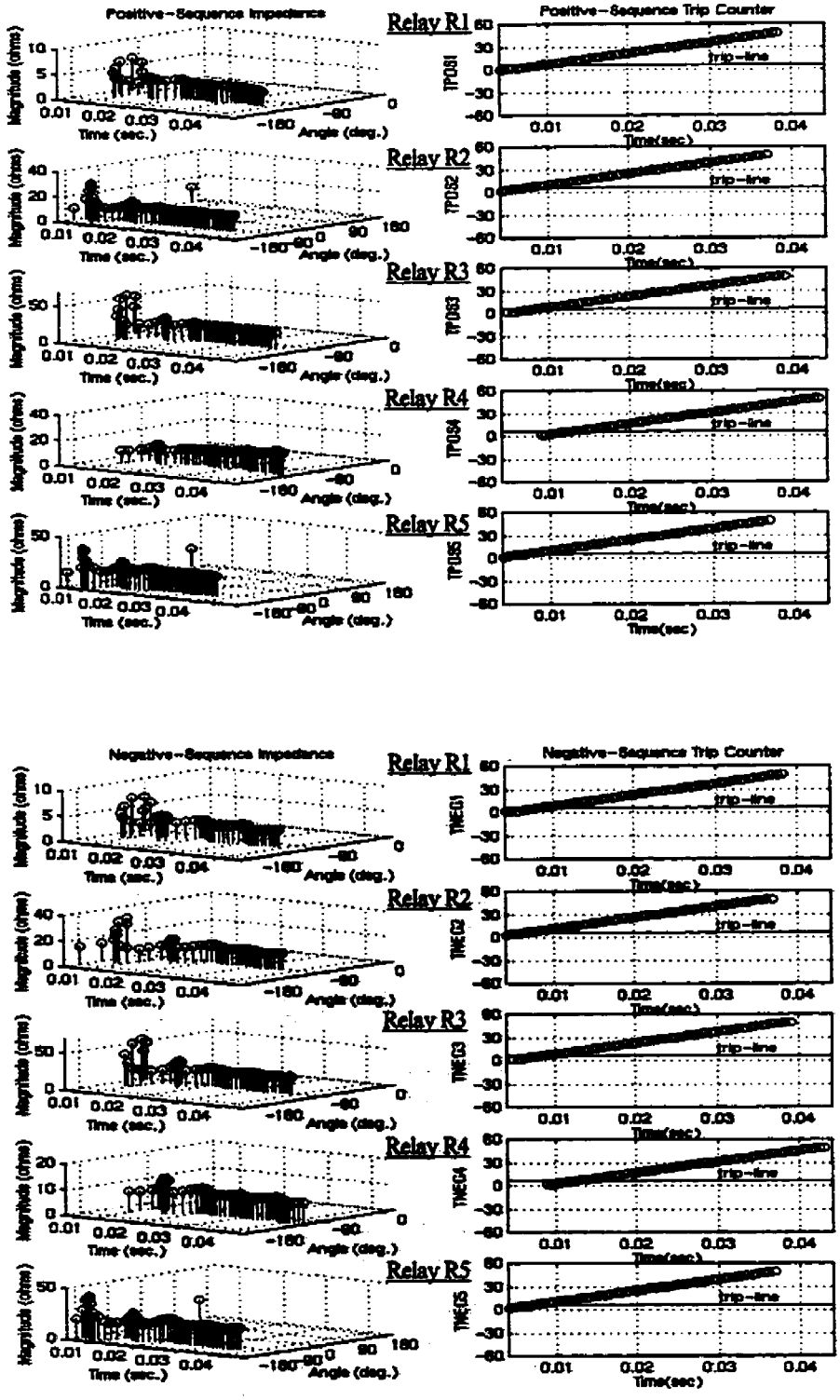


Figure J.10. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase C-ground internal fault (location 13, Figure 6.7).

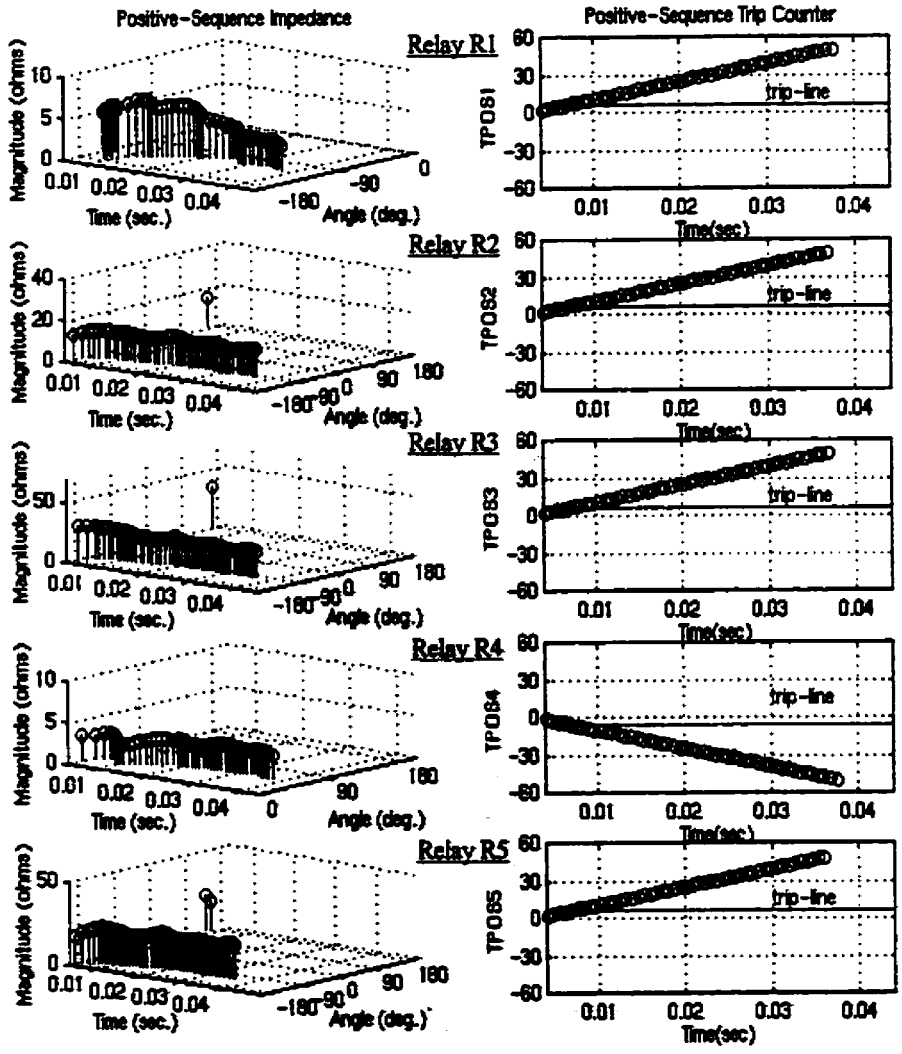


Figure J.11. Profiles of sequence-impedances' magnitude, argument and the trip counters for a three phase external fault (location 10, Figure 6.7).

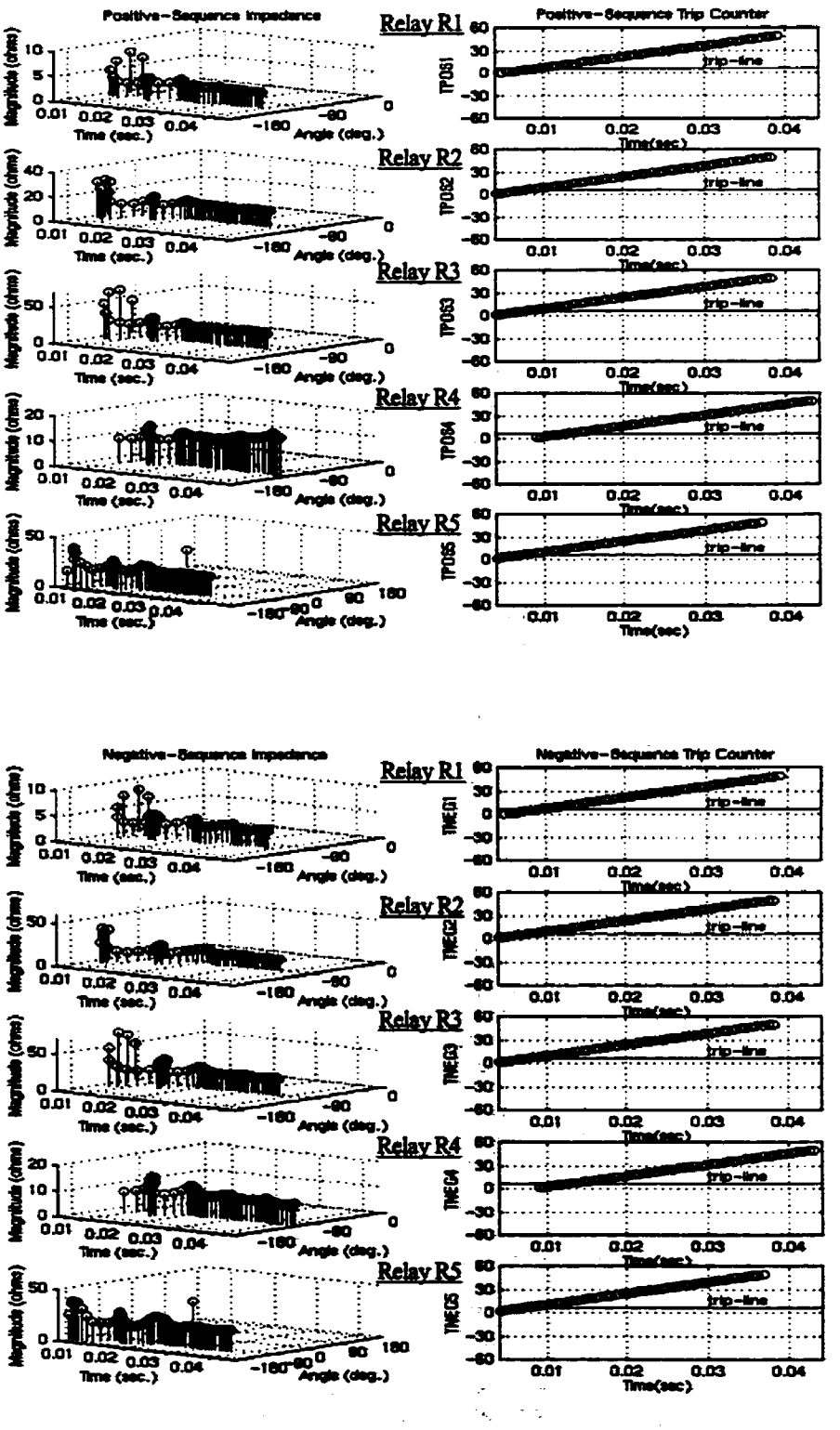


Figure J.12. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase C-ground internal fault (location 11, Figure 6.7).

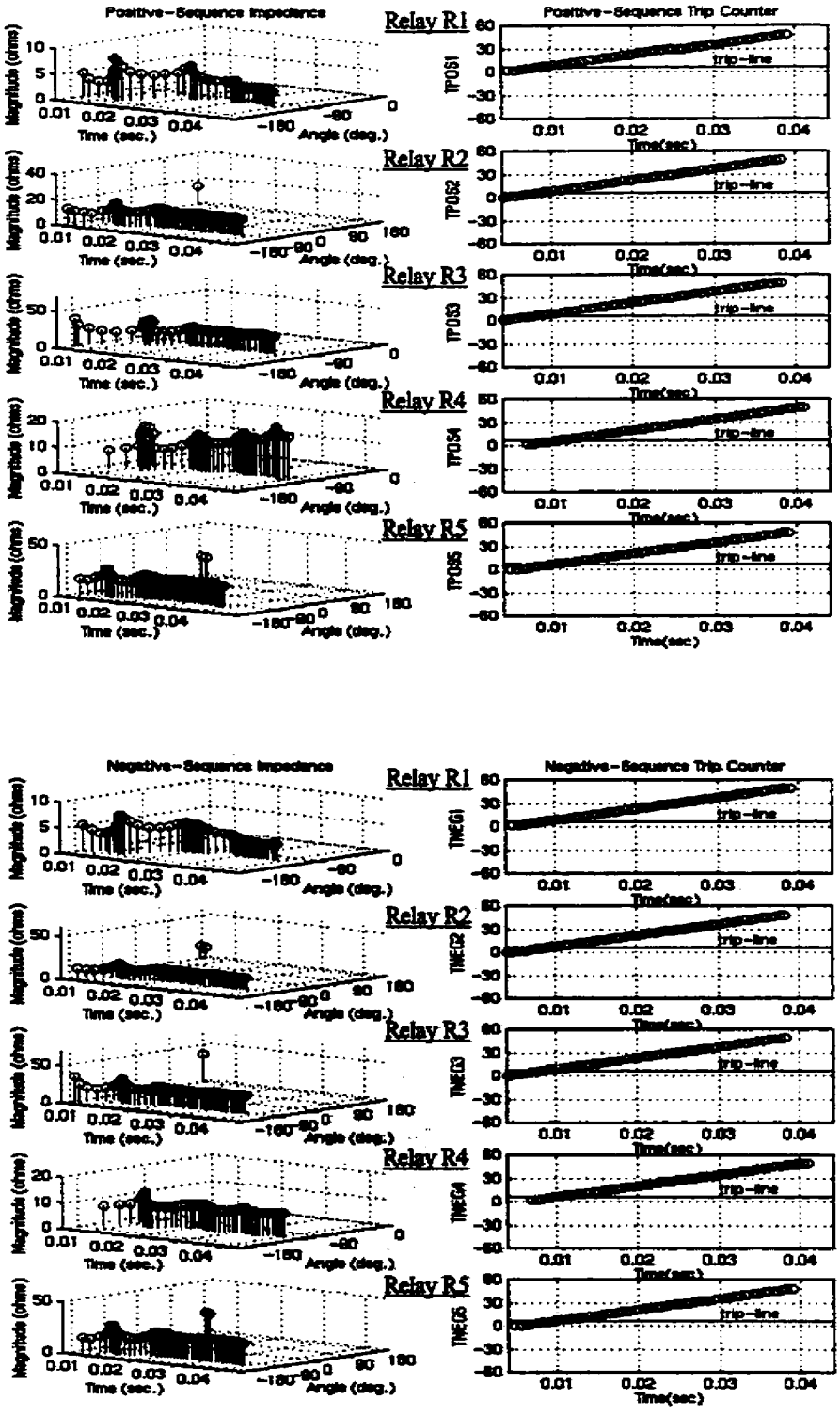


Figure J.13. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-ground internal fault (location 12, Figure 6.7).

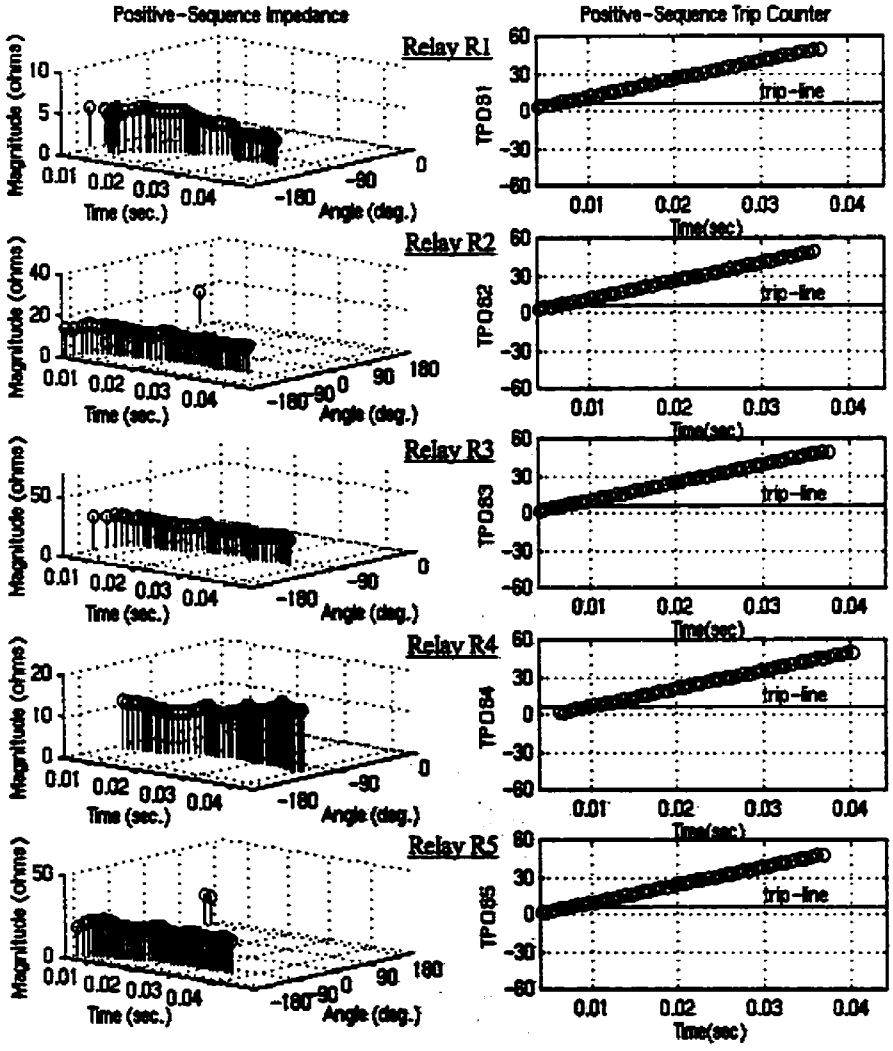


Figure J.14. Profiles of sequence-impedances' magnitude, argument and the trip counters for a three phase internal fault (location 12, Figure 6.7).

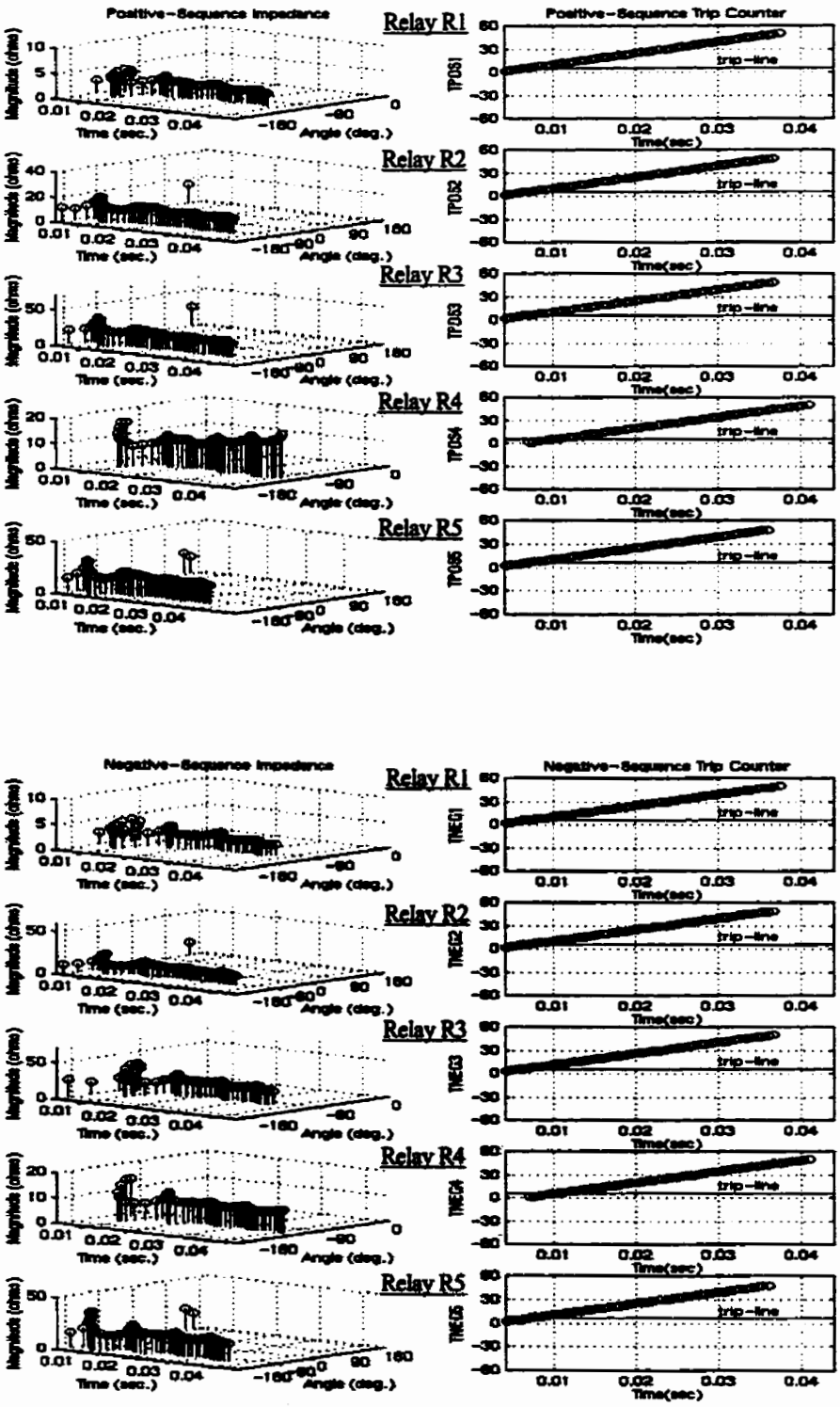


Figure J.15. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase B-Phase C internal fault (location 13, Figure 6.7).

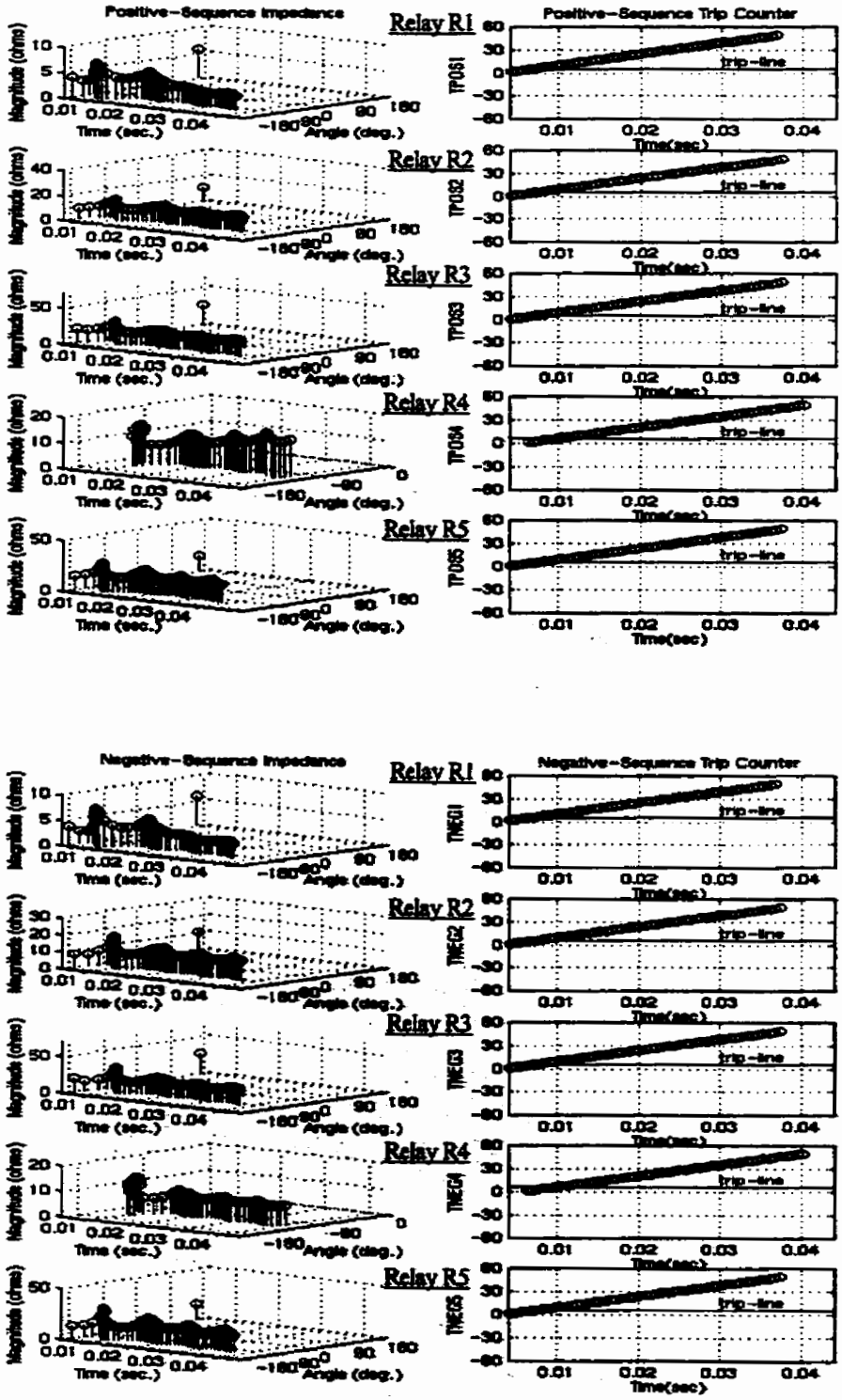


Figure J.16. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase B-ground internal fault (location 15, Figure 6.7).

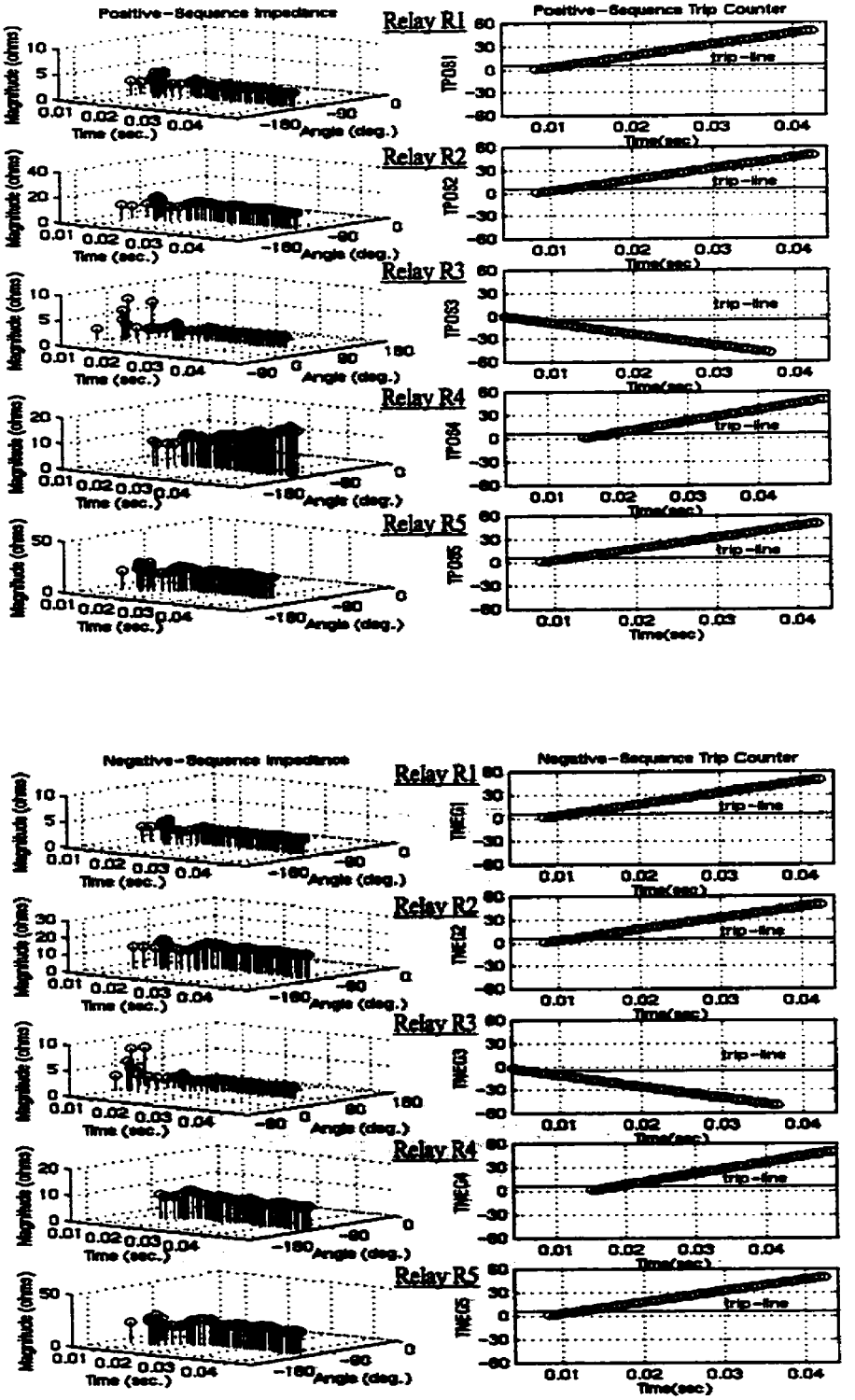


Figure J.17. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-Phase C external fault (location 16, Figure 6.7).

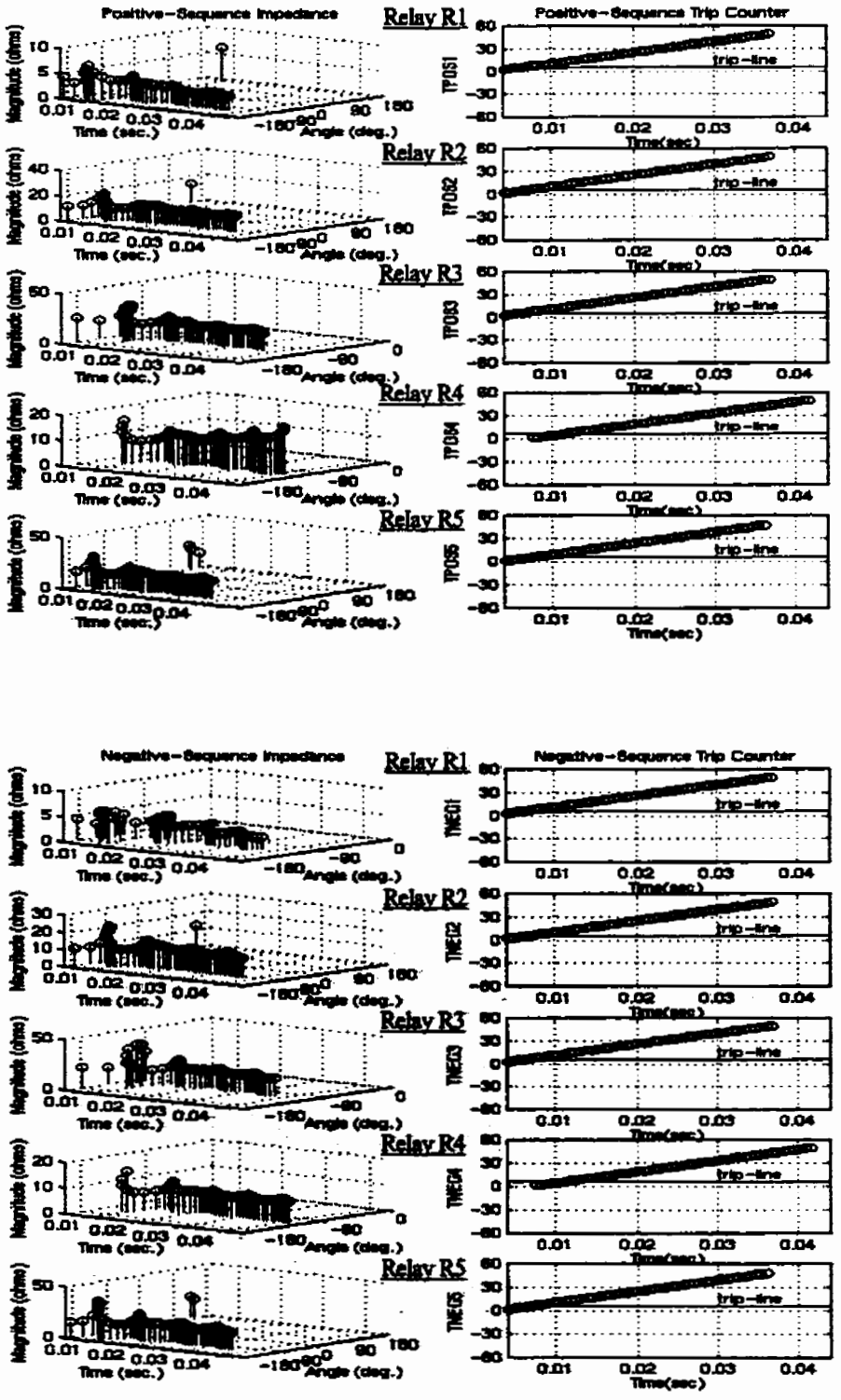


Figure J.18. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase B-Phase C internal fault (location 4, Figure 6.7).

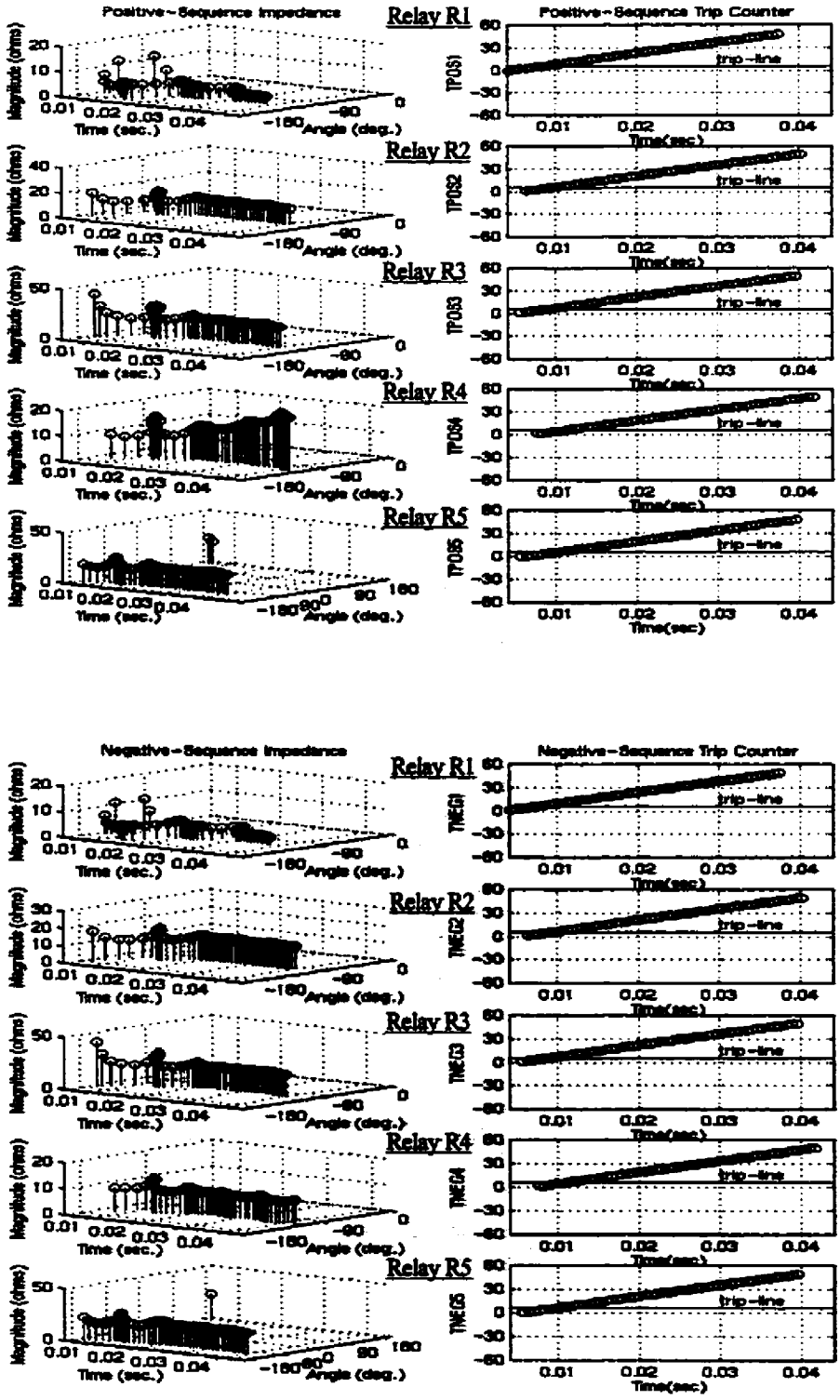


Figure J.19. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-Phase C internal fault (location 13, Figure 6.7).

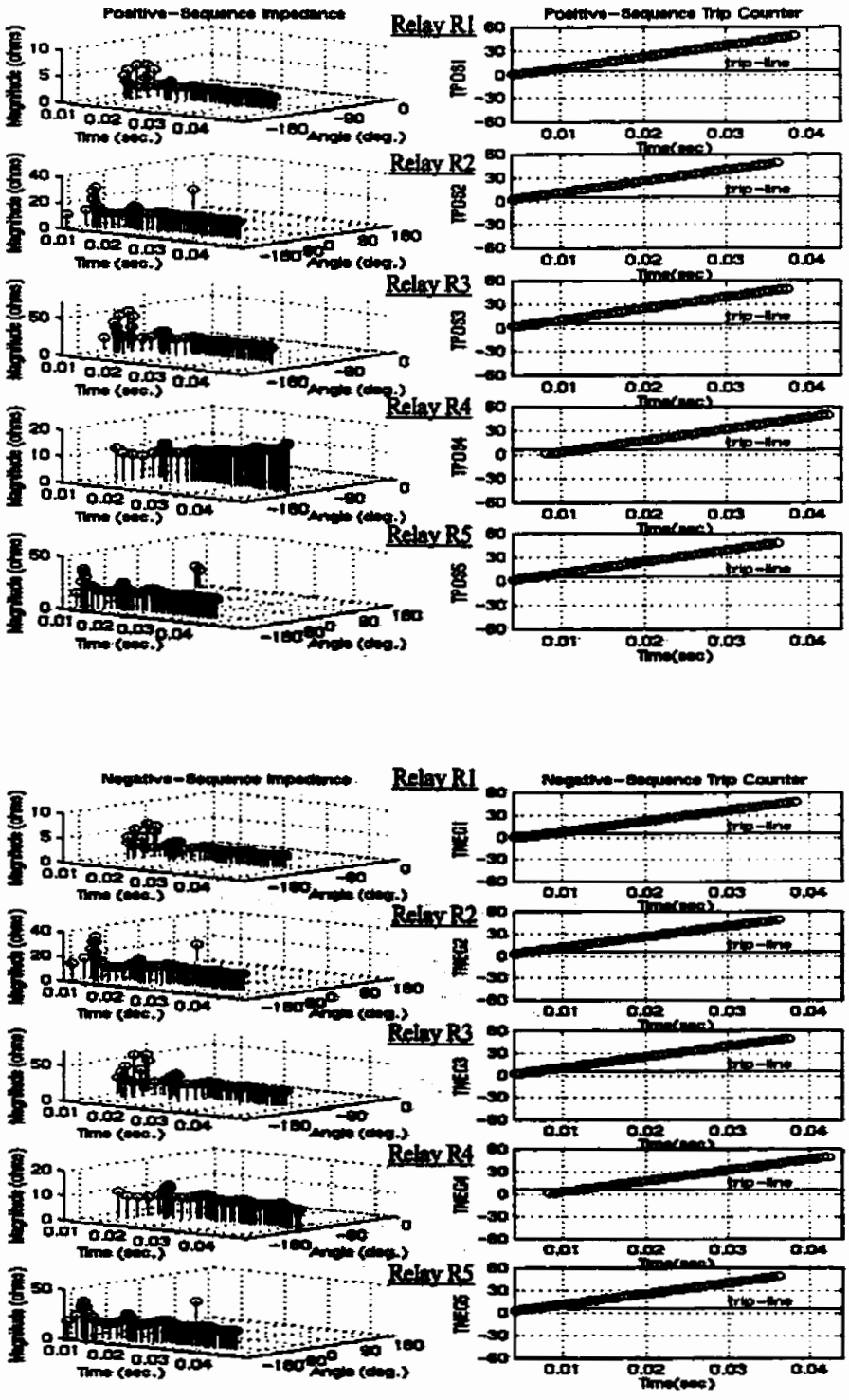


Figure J.20. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase C-ground internal fault (location 13, Figure 6.7).

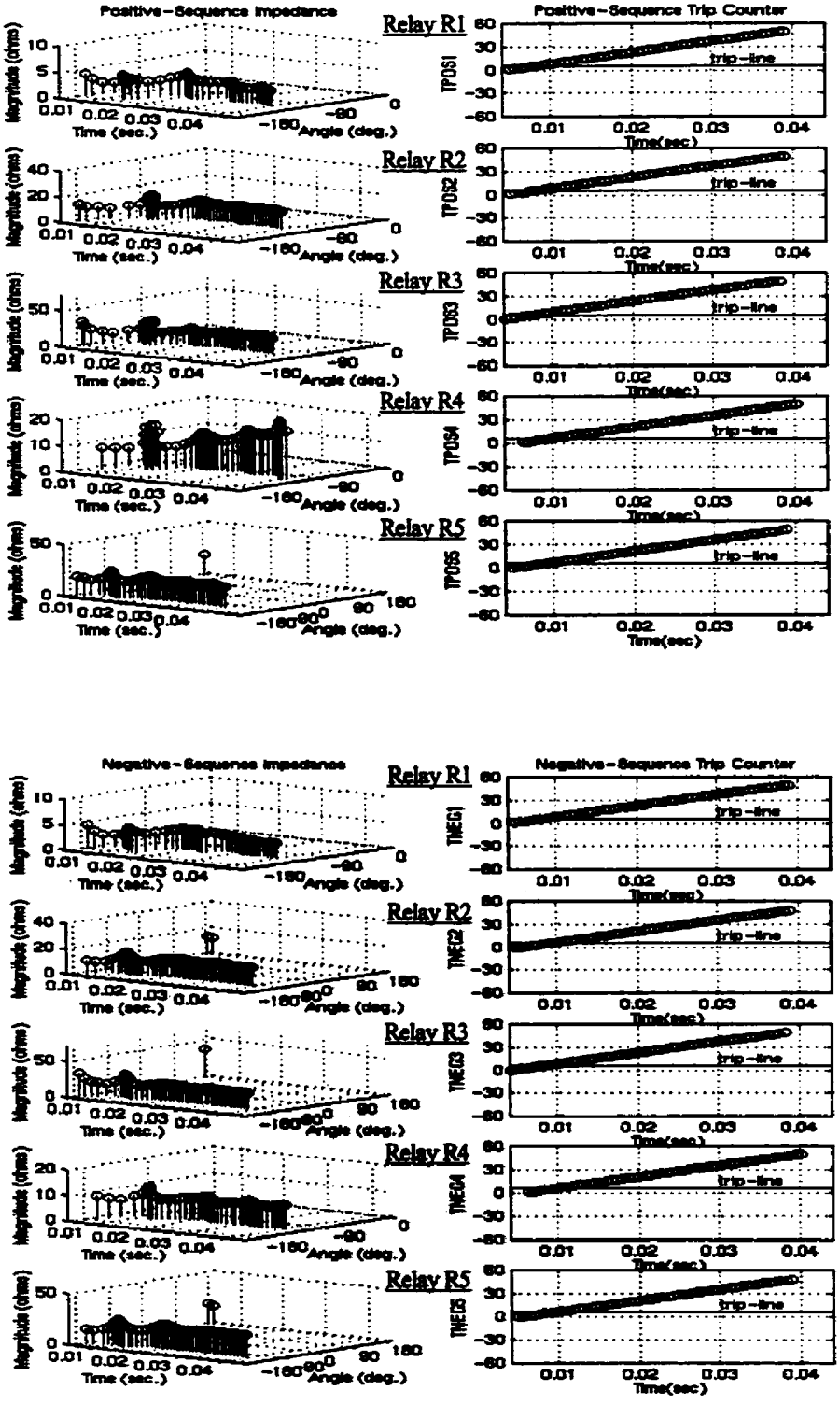


Figure J.21. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-ground internal fault (location 4, Figure 6.7).

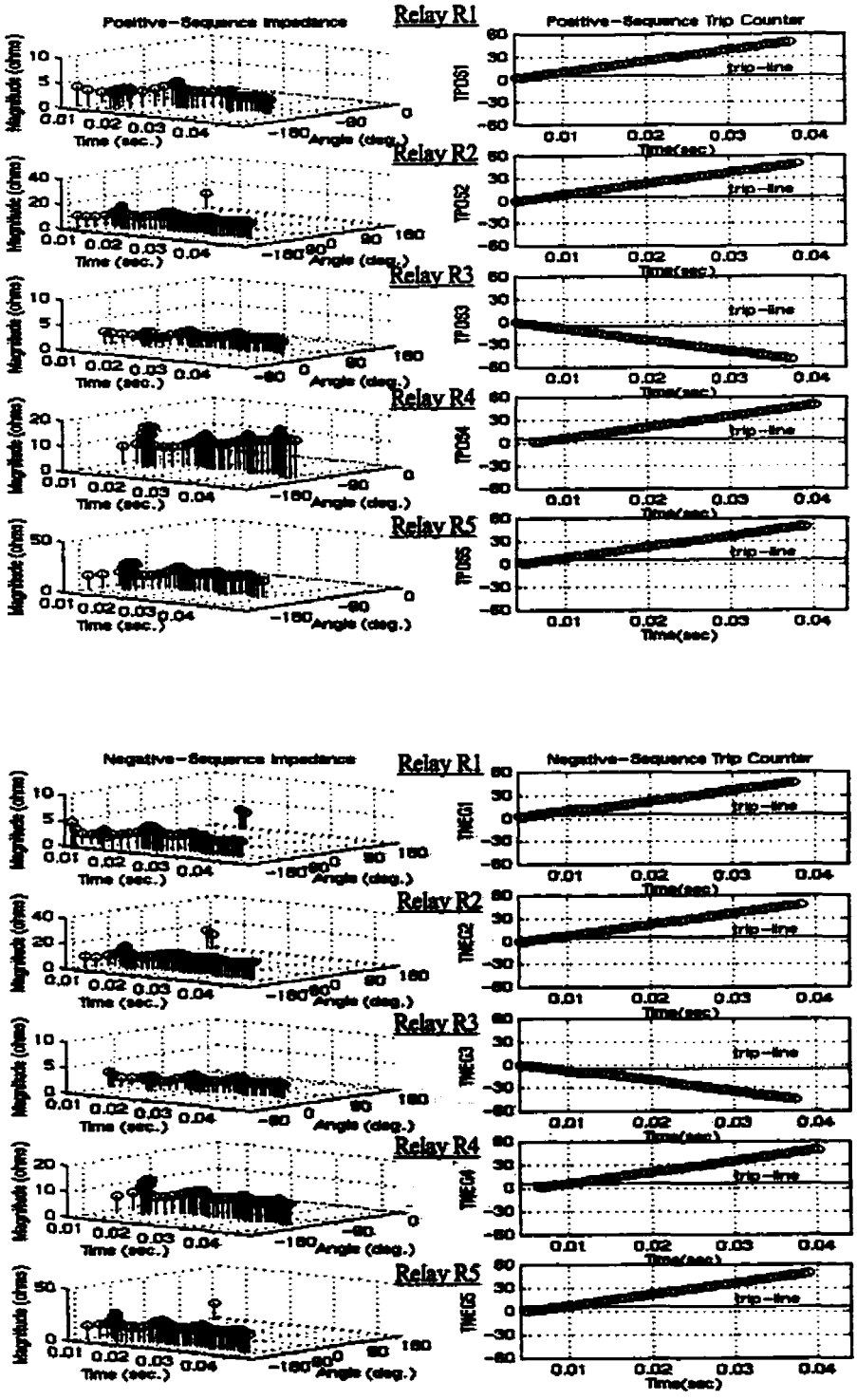


Figure J.22. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-Phase B external fault (location 21, Figure 6.7).

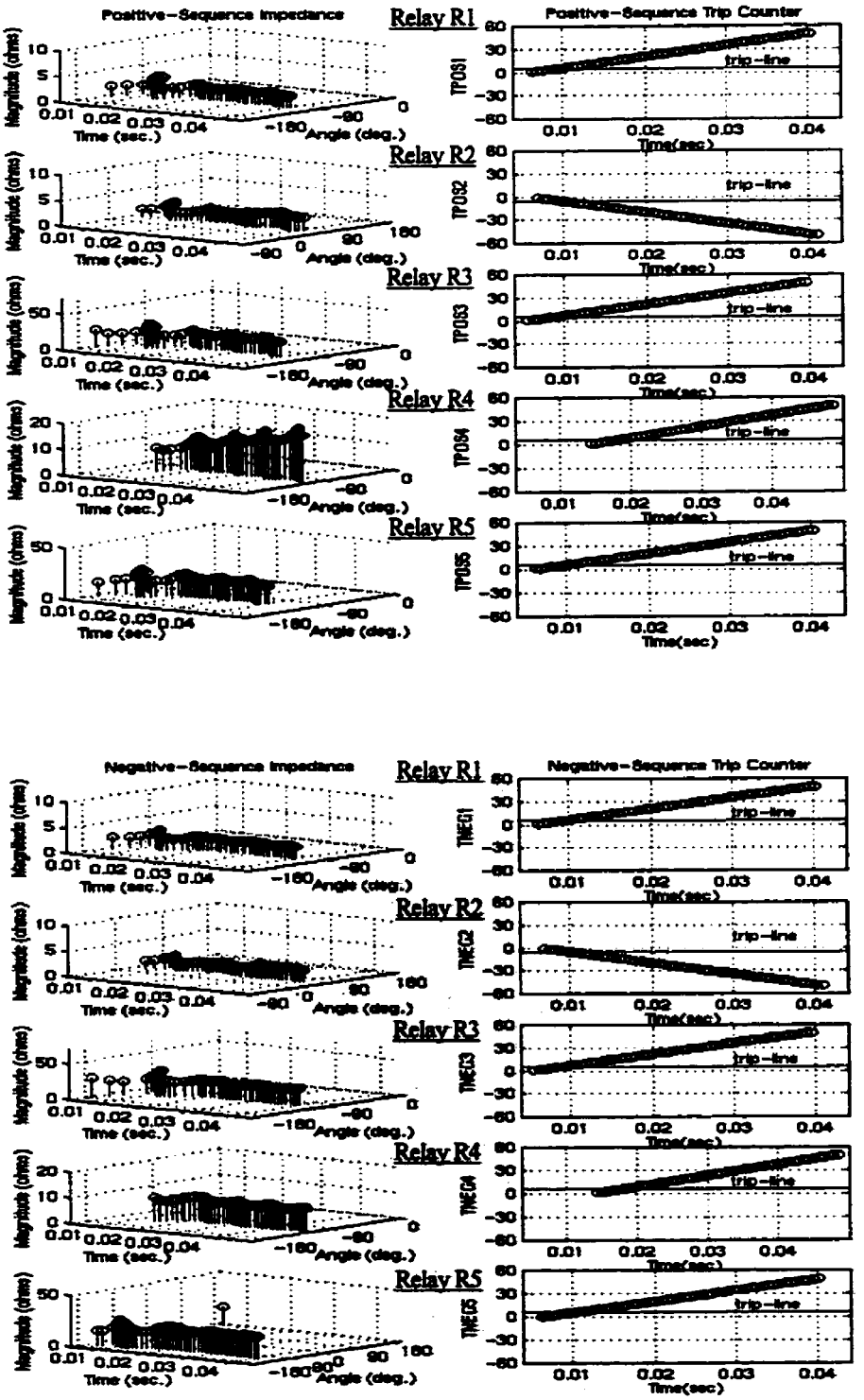


Figure J.23. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-ground external fault (location 22, Figure 6.7).

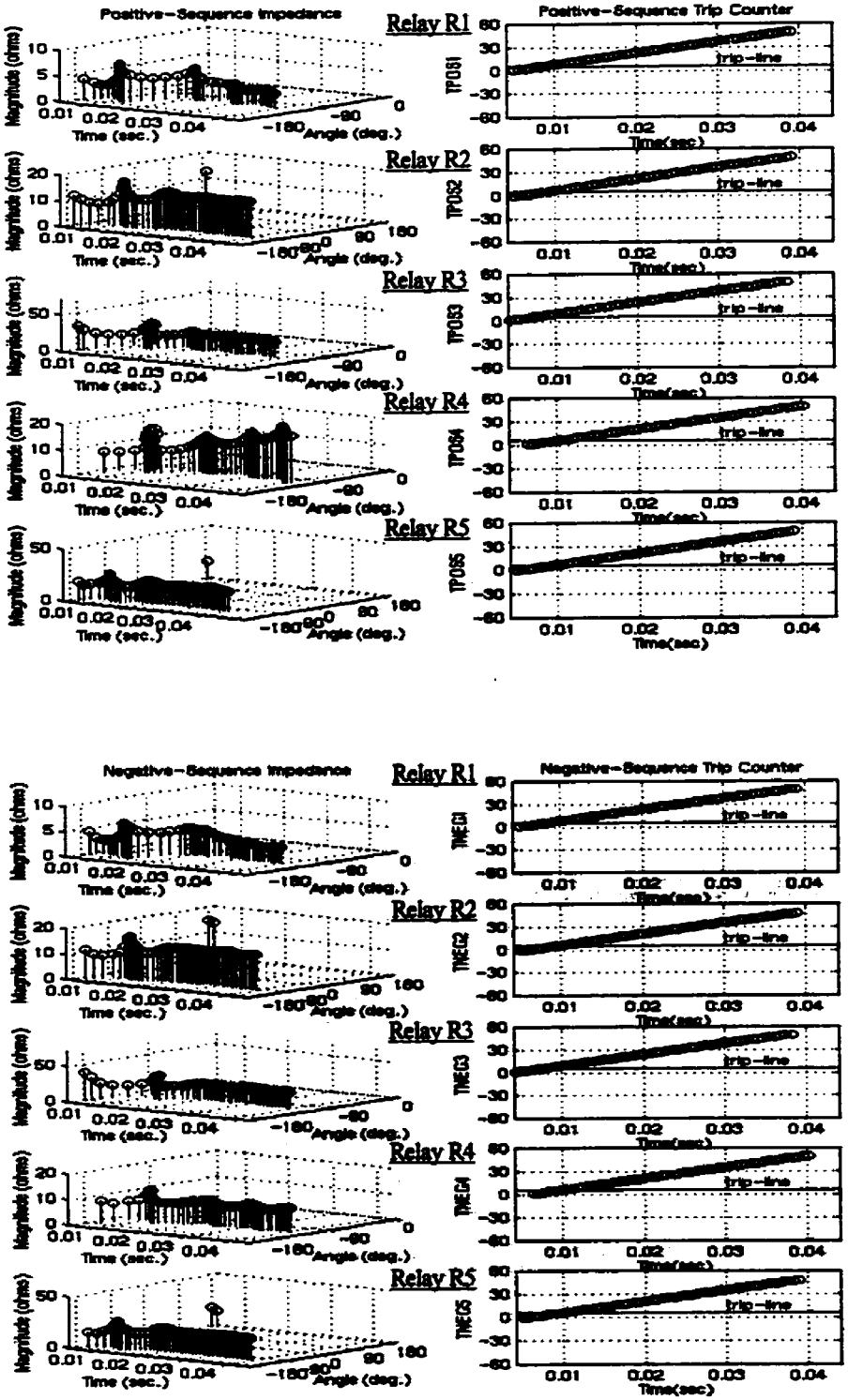


Figure J.24. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-ground internal fault (location 13, Figure 6.7).

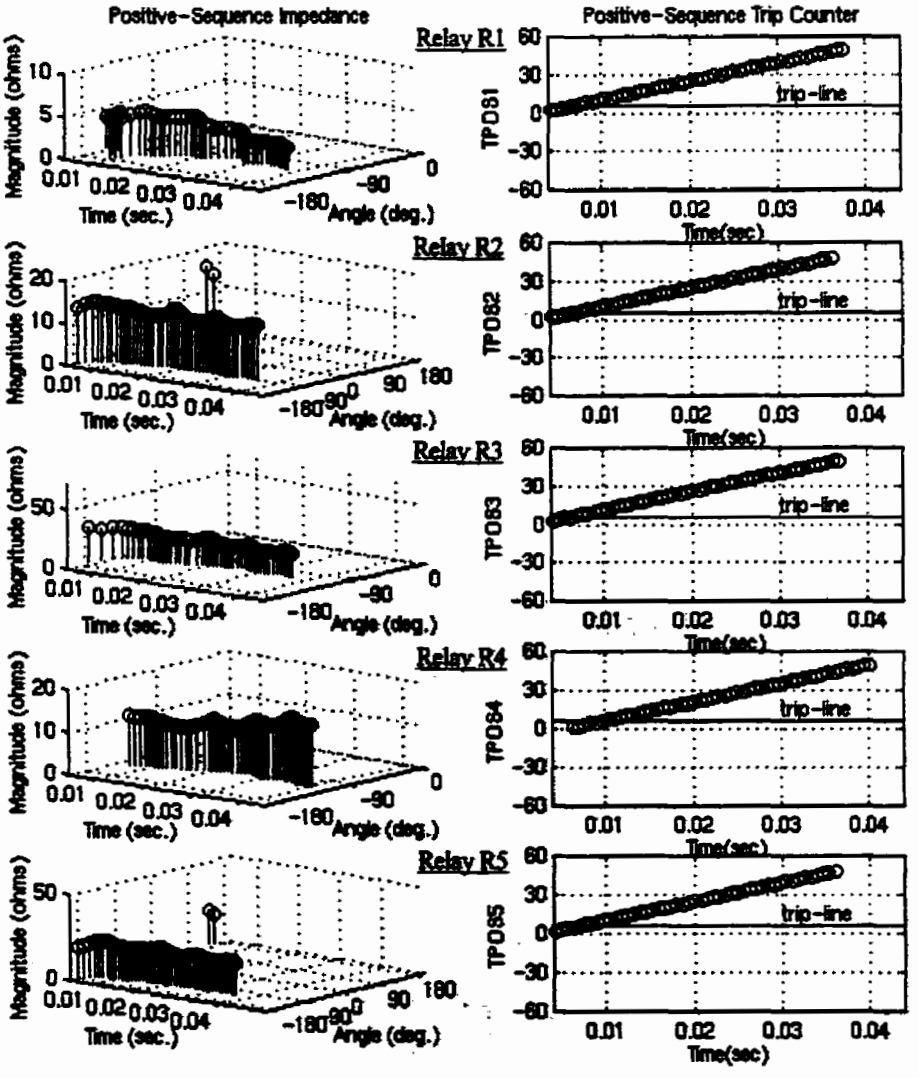


Figure J.25. Profiles of sequence-impedances' magnitude, argument and the trip counters for a three phase internal fault (location 4, Figure 6.7).

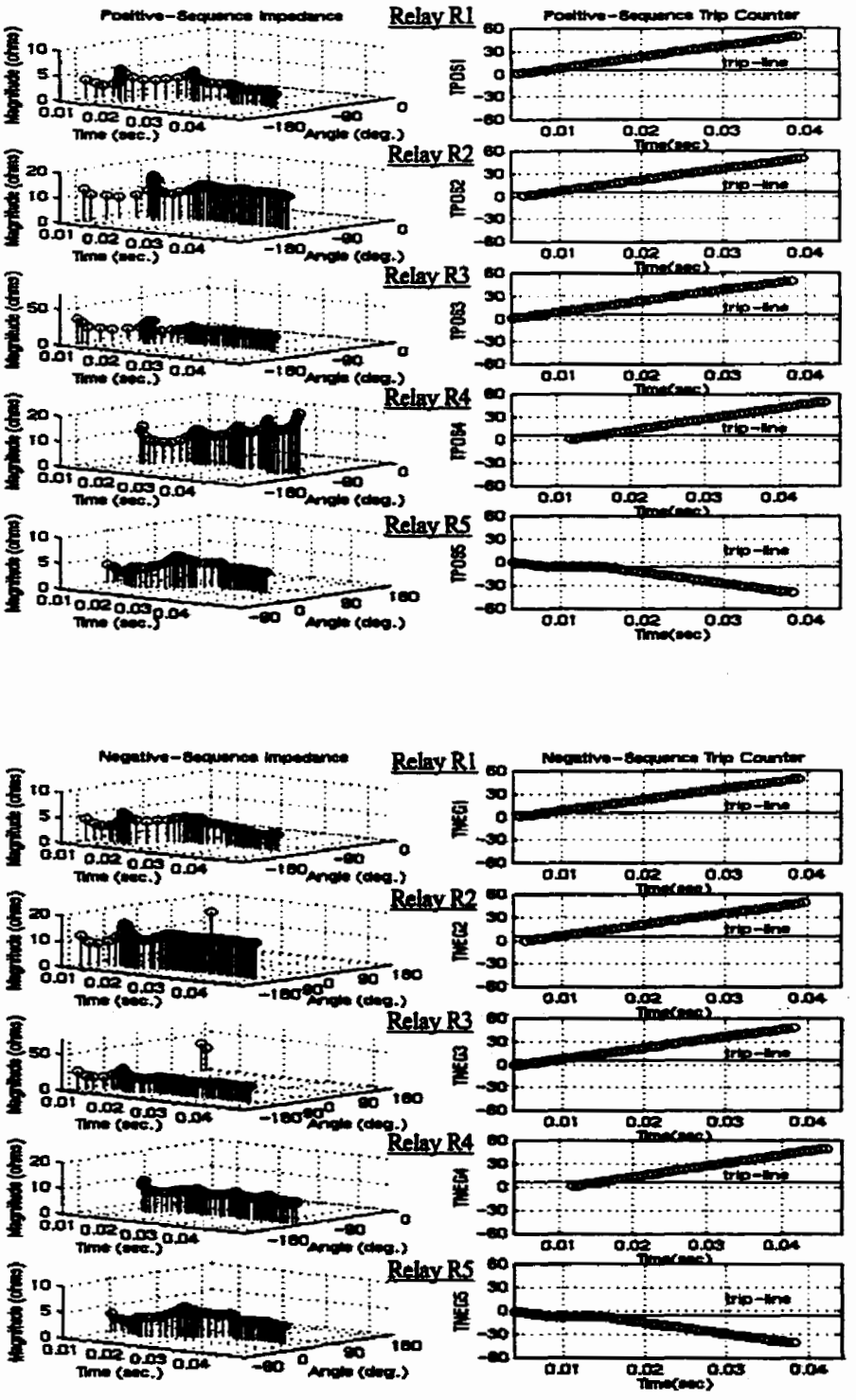


Figure J.26. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase B-ground external fault (location 1, Figure 6.7).

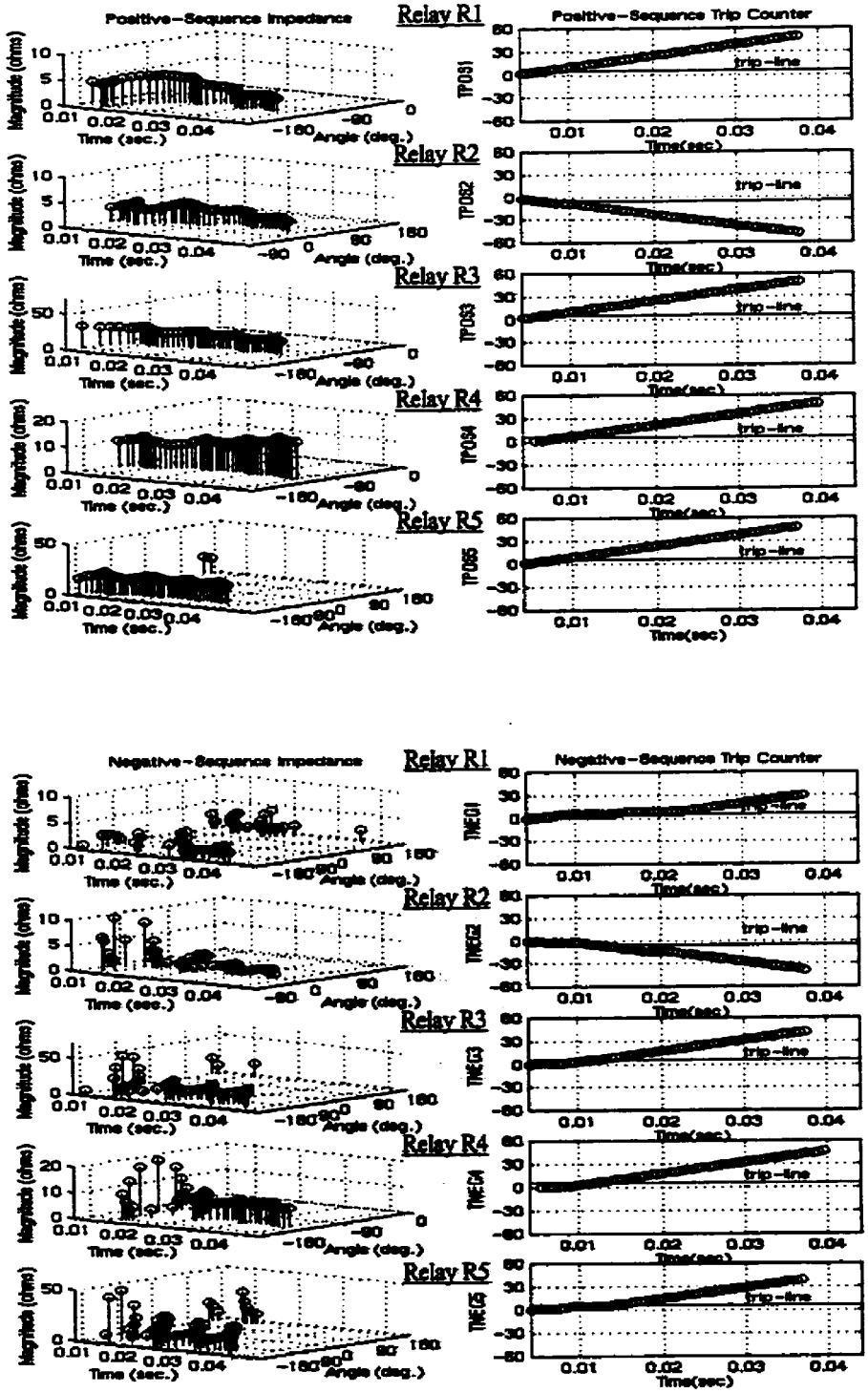


Figure J.27. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-Phase B-ground external fault (location 27, Figure 6.7).

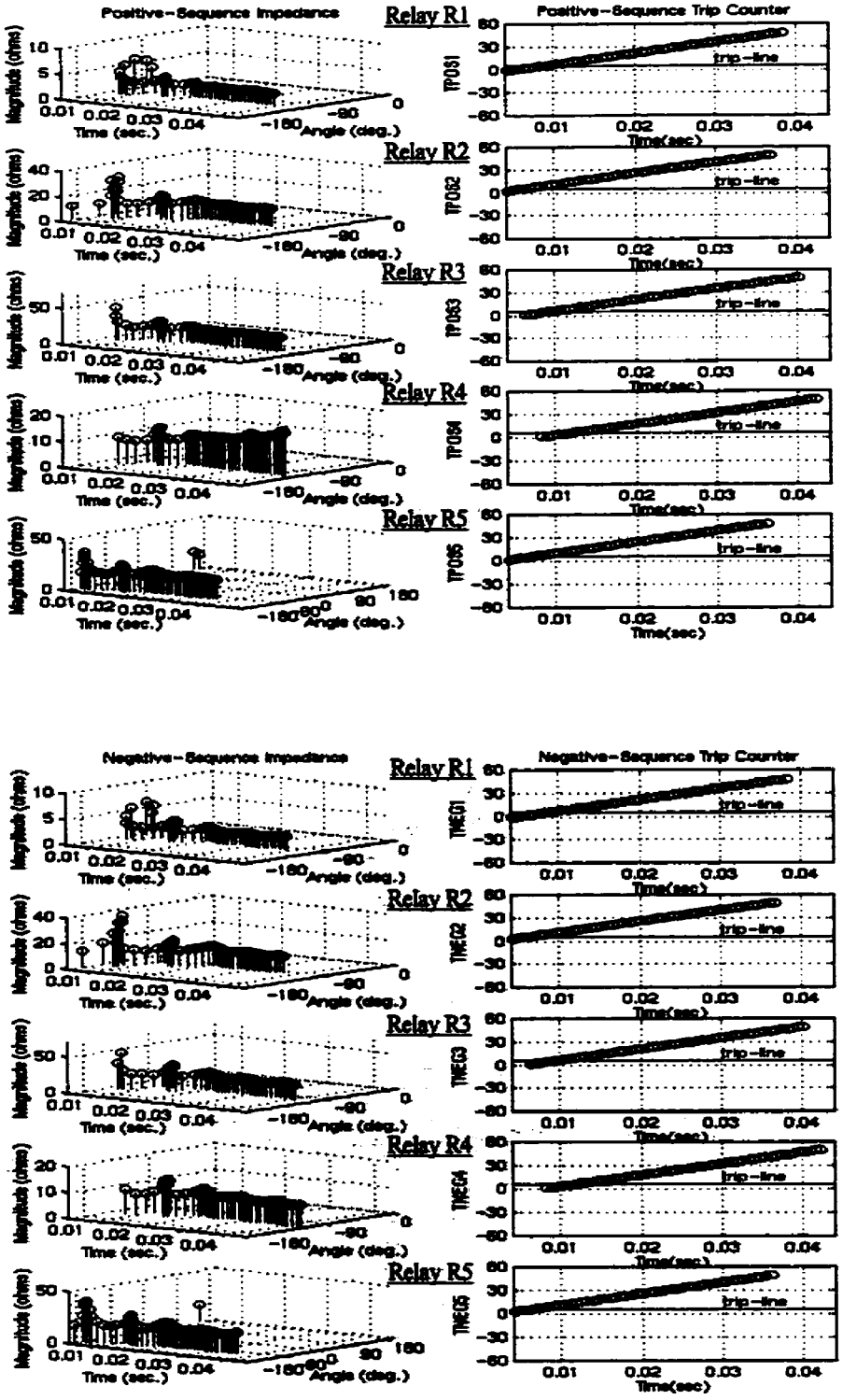


Figure J.28. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase C-ground internal fault (location 12, Figure 6.7).

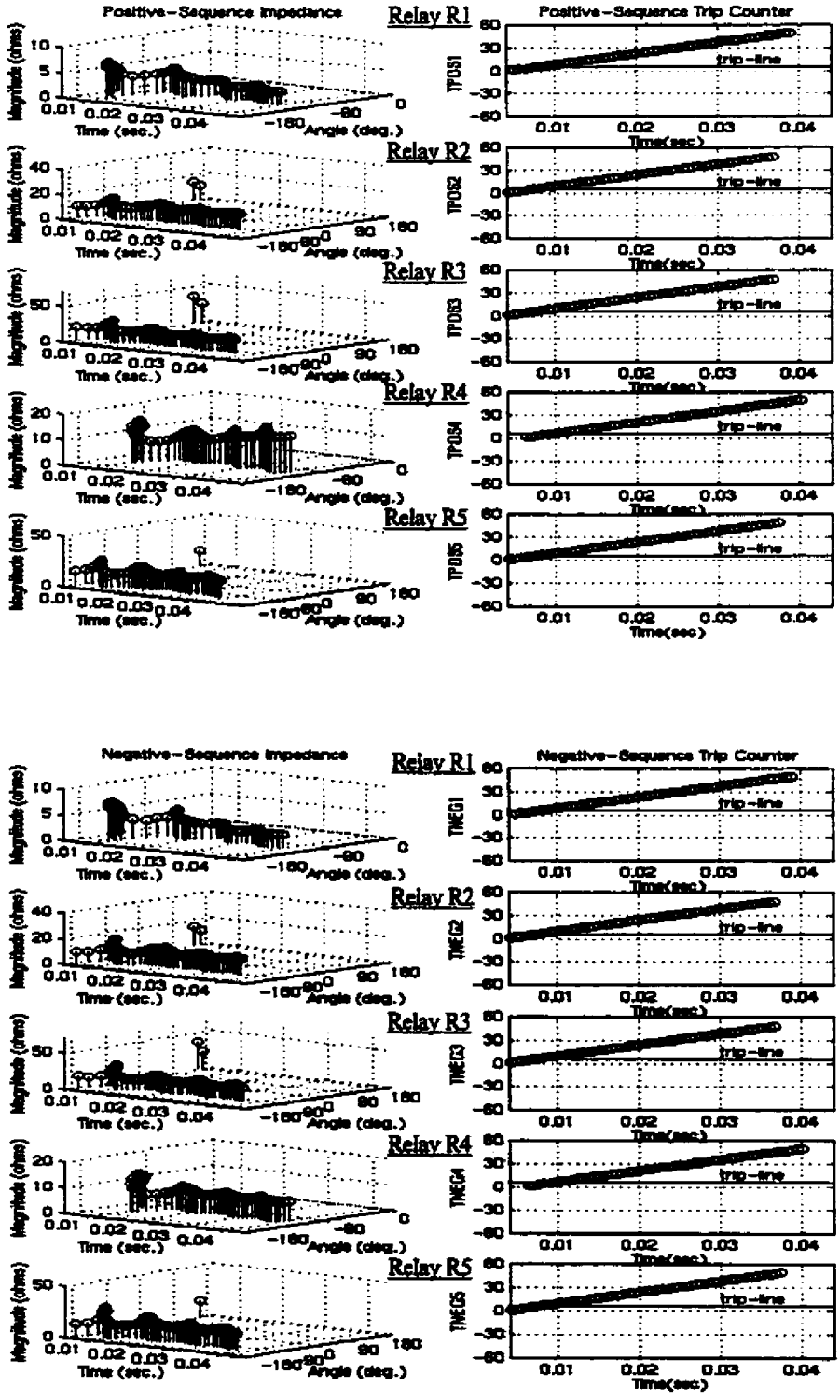


Figure J.29. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-ground internal fault (location 4, Figure 6.7).

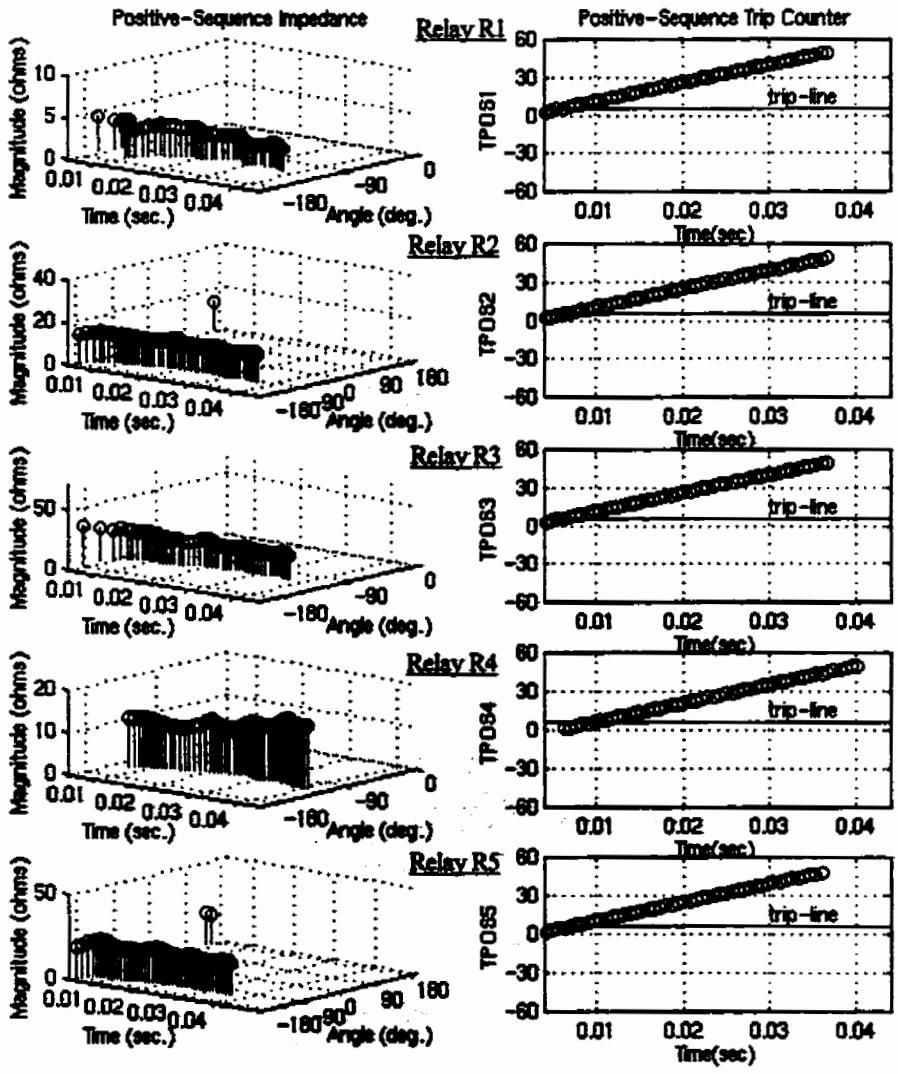


Figure J.30. Profiles of sequence-impedances' magnitude, argument and the trip counters for a three phase-ground internal fault (location 5, Figure 6.7).

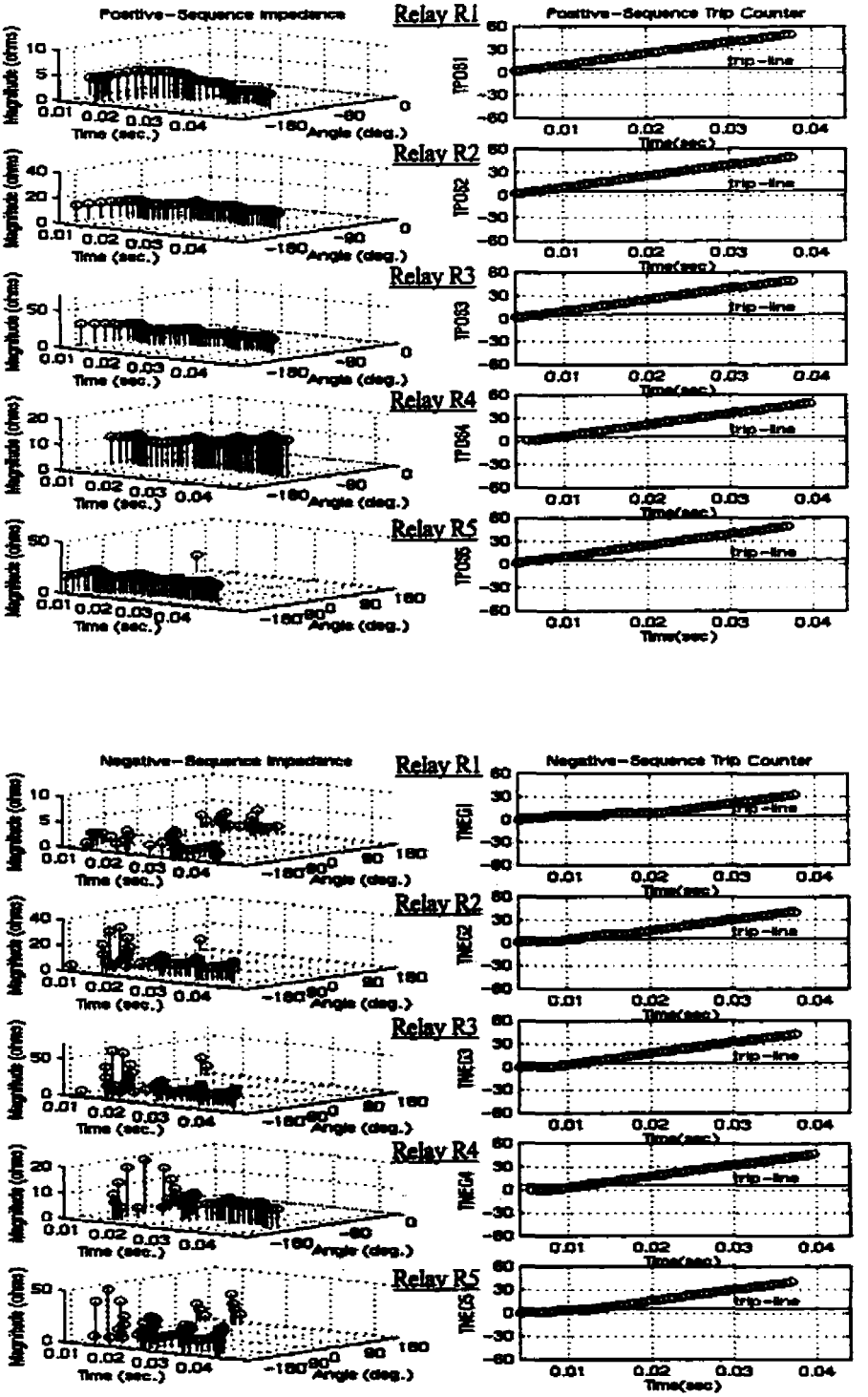


Figure J.31. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-Phase B-ground internal fault (location 12, Figure 6.7).

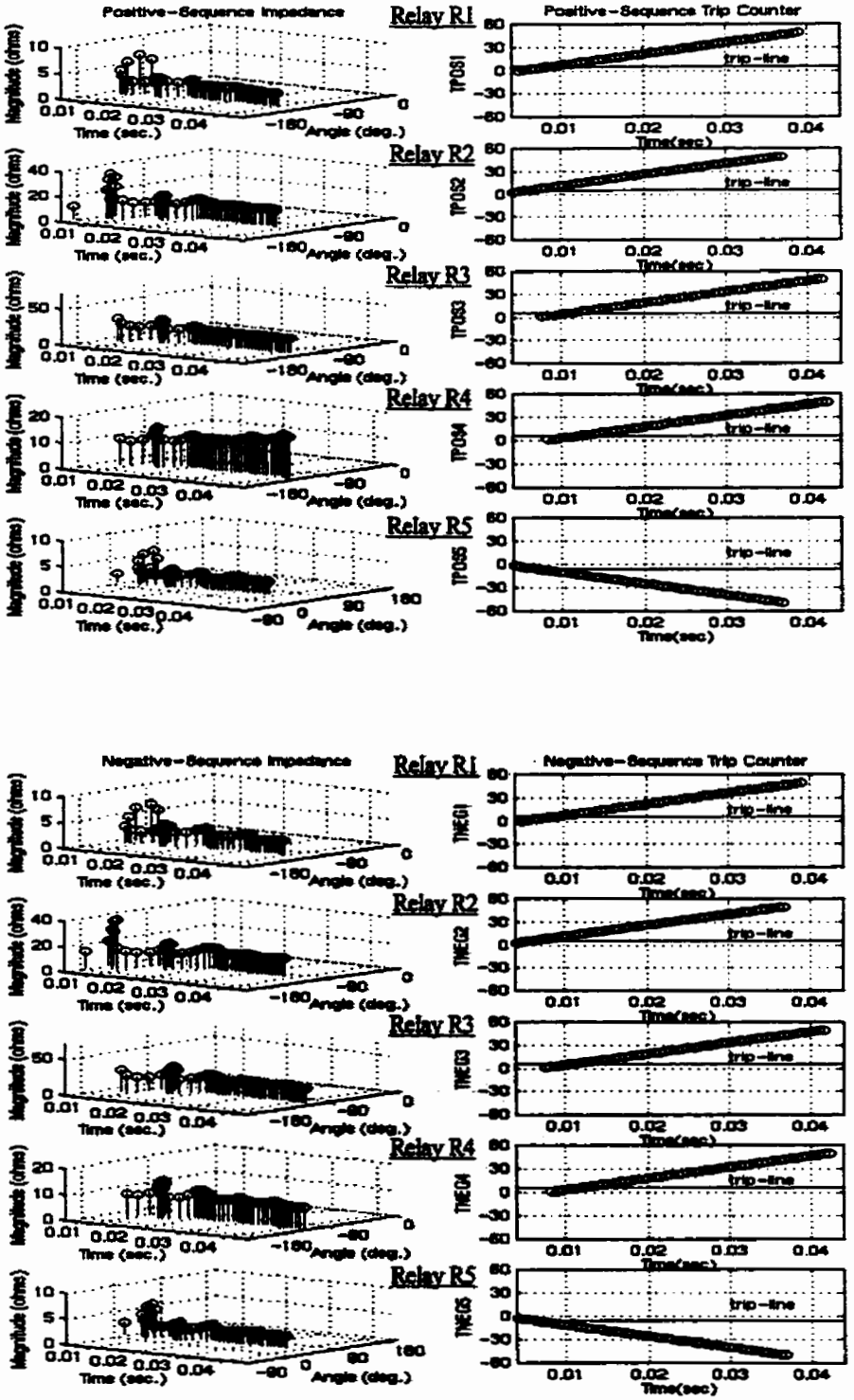
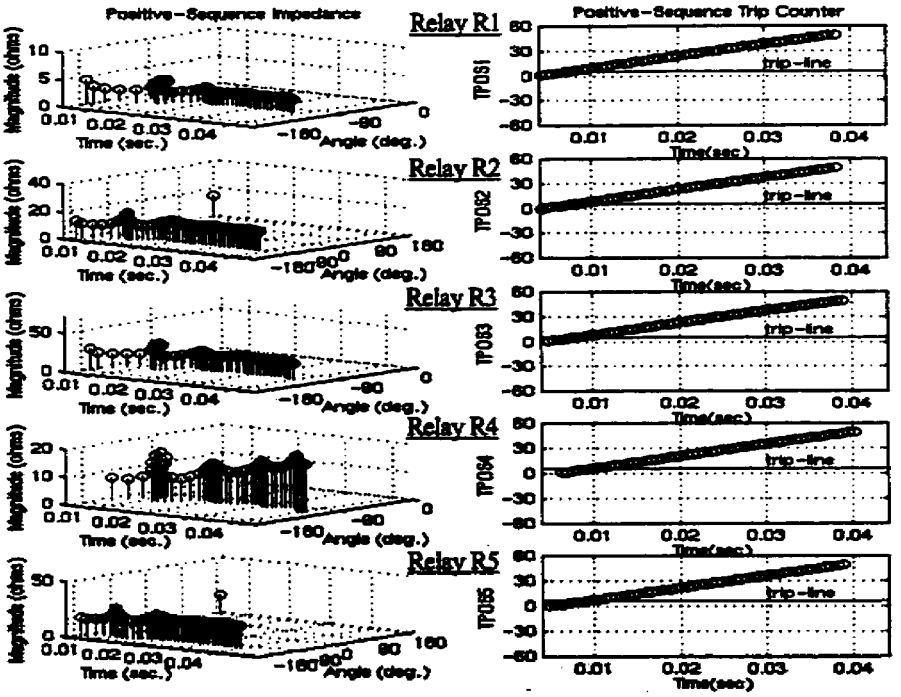


Figure J.32. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase B-ground external fault (location 1, Figure 6.7).



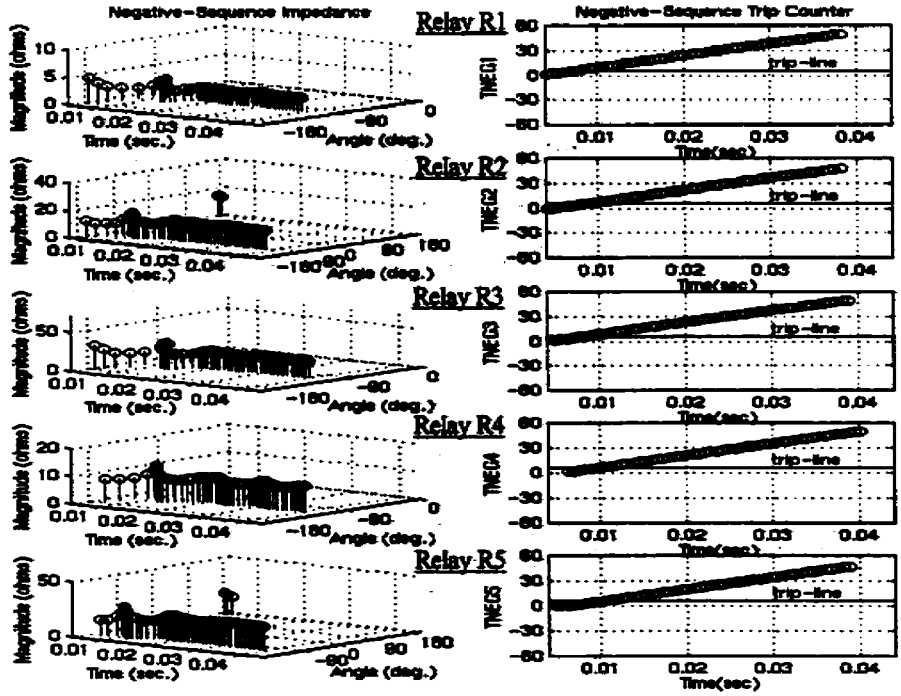


Figure J.33. Profiles of sequence-impedances' magnitude, argument and the trip counters for Phase A-ground internal fault (location 13, Figure 6.7).