# FEASIBILITY STUDY OF USING A DIGITAL COMPUTER AS A VARIABLE-AMPLITUDE VARIABLE-FREQUENCY OSCILLATOR

A Thesis

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by

*ZAIPUNA OBEDI YONAH*
Saskatoon, Saskatchewan
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UNIVERSITY OF SASKATCHEWAN

DEPARTMENT OF ELECTRICAL ENGINEERING

CERTIFICATION OF THESIS WORK

We, the undersigned, certify that Zaipuna Obedi YONAH, candidate for the Degree of Master of Science in Electrical Engineering, has presented his thesis on the subject Feasibility Study Of Using A Digital Computer As A Variable-Amplitude Variable Frequency Oscillator that this thesis is acceptable in form and content, and that this student demonstrated a satisfactory knowledge of the field covered by his thesis in an oral examination held on August 12, 1988.

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of Computational Science

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# FEASIBILITY STUDY OF USING A DIGITAL COMPUTER AS A VARIABLE-AMPLITUDE VARIABLE-FREQUENCY OSCILLATOR

Student:
Zaipuna O. Yonah

Supervisors:
Dr. A.M. El-Serafi
Prof. A.E. Krause

M.Sc. Thesis Presented to
The College of Graduate Studies and Research.
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## ABSTRACT

Previous studies have shown that a dual-excited synchronous generator ( a machine which has two identical field windings on the rotor: one on the d-axis and the other on the q-axis) can run asynchronously at any speed and still generate voltage at constant frequency. This capability of the generator can be utilized for variable-speed constant-frequency operation if the windings are both excited by slip frequency alternating currents. The main problem in such schemes is the design of a source which can supply such control signals whose frequency changes with the slip.

This thesis is a feasibility study of using a digital computer as a variable-amplitude variable-frequency oscillator; which generates the two-phase sinusoidal excitation control signals for the dual-excited synchronous generator. In this thesis, the oscillator control methodology is formulated and experimentally verified. The performance of the oscillator is experimentally investigated. The experimental results of the methodology verification and the oscillator performance tests are presented. The results show that it is feasible to use a digital computer as a variable-amplitude variable-frequency oscillator. The oscillator software-based design is flexible for generating different types of signal waveforms. By a single control variable, the software can be configured to vary the oscillator frequency range, and to greatly reduce (almost eliminate) the harmonic distortion of the output signals. Some recommendations for further research are included.

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# LIST OF SYMBOLS

| | |
|---|---|
| $\beta_n$ | phase angle of $n^{\text{th}}$ harmonic. |
| $\gamma$ | phase angle, a function of field windings parameters. |
| $\theta_n$ | angle corresponding to $n^{\text{th}}$ sample of an oscillating signal. |
| $\omega_0$ | generator synchronous angular frequency (radians/second). |
| $\omega$ | fundamental angular frequency. |
| $\phi_d$ | magnetic flux along the direct-axis. |
| $\phi_q$ | magnetic flux along the quadrature-axis. |
| $\phi_m$ | peak amplitude of the rotating field. |
| $\overline{\Phi}$ | resultant magnetic field riding on the rotor. |
| $\phi_{dm}$ | peak amplitude of $\phi_d$. |
| $\phi_{qm}$ | peak amplitude of $\phi_q$. |
| $A_d$ | peak value of amplified $v_{fd}$. |
| $A_q$ | peak value of amplified $v_{fq}$. |
| A/D | analog-to-digital. |
| D/A | digital-to-analog. |
| $b$ | number of pairs of reference D/A data buffers. |
| $e$, $e(t)$ | terminal voltage error signal. |
| $e[n]$ | $n^{\text{th}}$ sample of the terminal voltage error signal. |

$f_{da}$ frequency of the D/A output signals.

$f_{sa}$ D/A sampling frequency.

$K_e$ terminal voltage error constant with units $[\text{Volts}]^{-1}$.

$K_{ref}$ reference multiplication factor.

$K_v$ multiplication factor.

$K_v[n]$ multiplication factor corresponding to the $n^{\text{th}}$ sample of the voltage error signal.

$K_s$ slip constant with units $[\text{Volts}]^{-1}$.

$L$ length of each D/A data buffer.

$m$, $n$ positive integer.

$M$ number of samples per D/A buffer.

$M_h$ number of subdivisons per time step.

$n_0$ generator synchronous speed.

$n_r$ rotor speed.

$n_\phi$ speed of the rotating magnetic field relative to the rotor.

$N$ number of samples per cycle of each output signal.

$N_P$ number of cycle parts of each output signal in a D/A data buffer.

$N_{FC}$ number of full-cycles of each output signal in a D/A data buffer.

$N_{HC}$ number of half-cycles of each output signal in a D/A data buffer.

$N_{QC}$ number of quarter-cycles of each output signal in a D/A data buffer.

$P$ number of reference D/A data buffers.

$PDA$ phase delay angle, phase distortion.

$s_a$ dimmensionless slip variable defined as $\frac{n_0 - n_r}{n_0}$.

$s(t)$ slip signal.

$s[n]$ $n^{\text{th}}$ sample of the slip signal.

$T_{da}$ period of the oscillator output signals.

$T_{ad}$ A/D intersample time for each sampled signal.

$T_{sa}, T_{sa}'$ D/A intersample time for each output signal.

$\Delta T$ intersample time for two consecutive samples in a D/A data buffer.

$t_n$ time corresponding to $n^{\text{th}}$ clock pulse.

$v(t)$ A voltage signal.

$v_{fd}$ excitation voltage fed to the direct-axis field winding.

$v_{fq}$ excitation voltage fed to the quadrature-axis field winding.

$V_n$ $n^{\text{th}}$ harmonic of the voltage signal $v(t)$.

$V_k$ $k^{\text{th}}$ DFT coefficient of the voltage signal $v(t)$.

$v[n]$ $n^{\text{th}}$ sample of the voltage signal $v(t)$.

# Chapter 1

# INTRODUCTION

## 1.1. General

In recent years, increasing emphasis has been placed on the development and the use of renewable energy sources, such as wind [1, 2, 3, 4, 5], for electrical power generation. There is also a growing demand to generate electricity for specialized applications, such as in aircraft and mobile vehicles, using variable-speed prime movers. Wind-turbines and aircraft engines are some of the examples of variable-speed prime movers.

The power from a wind turbine or an aircraft engine is random in nature [6], and as such is not easily controllable. A conventional synchronous generator driven by a variable-speed shaft generates a variable-frequency voltage, which has limited applications. Thus, the general problem in such variable-speed schemes is to generate electricity at constant frequency as in the case of the conventional constant-speed constant-frequency (CSCF) generator systems. Several efforts have been made to design such variable-speed constant-frequency (VSCF) generator systems. These are capable of:

1. being driven directly from a variable-speed shaft, and
2. supplying alternating current (a.c.) electric energy at a constant frequency.

## 1.2. Variable-Speed Constant-Frequency Schemes

This section briefly points out several methods for designing variable-speed constant-frequency systems. One method is that of regulating the speed by mechanical techniques to obtain a constant-speed shaft from a variable-speed shaft. Variable gear-ratio units and blade position controllers are extensively used in wind powered plants [5] to convert a variable-speed variable-frequency setup to a constant-speed constant-frequency arrangement. Hydraulic pump-motor arrangements, as conversion schemes, are employed in aircraft power generation units [5, 6]. However, the drawbacks of these schemes include the following:

1. mechanical parts wearout,
2. low control speed with almost no flexibility, and
3. leakages in the hydraulic setups.

These factors deteriorate the effectiveness of the frequency control [7] of such schemes.

Another method employs the direct current (d.c.) links. Rectifiers are used to convert the variable-frequency a.c. power to d.c. This is then inverted to constant-frequency a.c. [4, 5, 8]. The main problem with the use of inverters is the harmonic generation [9, 10].

The third method, which is gaining attention recently, is that of using special purpose generator setups. These special purpose generators are designed to generate voltage at a constant frequency in spite of the variation in the prime mover speed. Several generator schemes have been suggested for

variable-speed constant-frequency operation. These schemes use either synchronous or induction generators.

Velayudhan [11, 12] reported a scheme employing a slip-ring induction generator. The speed-torque characteristic of the machine under constant load is adjusted to match the input power by adjusting the external resistance connected in the rotor circuit of the generator. The method is uneconomical, since electric power has to be dissipated in the external rotor resistance. This reduces the efficiency of the setup, and the heat dissipation in the rotor circuit requires special cooling systems [11].

The use of induction machines as synchronous generators have been also reported in the literature [6, 13, 14]. In such a scheme, three-phase variable-frequency excitation currents are fed to the generator rotor as illustrated in Figure 1-1. The frequency of the excitation currents is proportional to the rotor slip. The underlying principle is that the variable-frequency excitation currents produce a rotating magnetic field. This field rotates in the machine airgap such that the armature frequency becomes constant. The excitation currents are supplied from a cycloconverter. The use of cycloconverters is always accompanied with the generation of undesirable harmonics. These harmonics cause heating problems in the generator [9]. Also, excessive harmonics may interfere with the performance of the control equipment [13].

A synchronous generator can be made suitable for variable-speed constant-frequency applications by the use of the two-axis rotor excitation

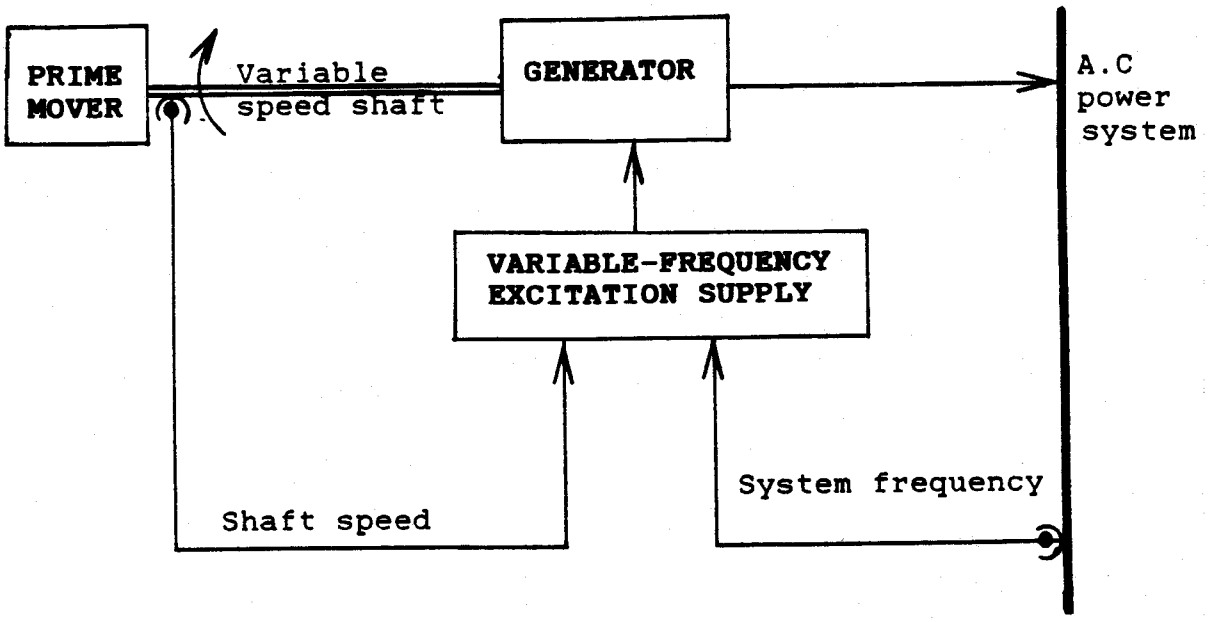



**Figure 1-1:** A block diagram of variable-speed constant-frequency setup using a variable-speed driven generator.

technique [15, 16]. For this application, the machine requires an a.c. excitation source. The excitation currents must be alternating with a frequency proportional to the rotor slip. The effect is to have a magnetic field rotating relative to the rotor speed such that a constant armature frequency is maintained.

The theoretical explanation of the two-axis machines is well presented in references [15, 16, 17, 18]. A cross-section of the many different practical systems which advocate the two-axis excitation technique is given in references [7, 19, 20, 21].

## 1.3. Generation of Frequency Controlled Signals

The two-axis generators have to be supplied from special a.c. excitation sources. Frequency controlled signals must be fed to the generator rotor in such a way that they determine the frequency at which the voltage is generated. There are several ways in which the frequency control signals may be generated. The common technique is to use cycloconverters. This technique has some disadvantages. Cycloconverters generate undesirable harmonics [9, 13, 16, 22], which cause heating problems within the generator. Practical cycloconverters have complex control circuitry. This results in poor flexibility.

## 1.4. The Dual-Excited Synchronous Generator

A dual-excited synchronous generator (DESG) [15, 16] is one of the machines which can be used for variable speed constant frequency schemes. It uses the two-axis excitation technique. The rotor of a dual-excited synchronous generator is constructed such that for each pole, it has two sets of field windings which are:

1. electrically in quadrature with each other (displaced a 1/2-pole pitch, that is, 90 electrical degrees from each other), and
2. are externally accessible.

Figure 1-2 shows a typical schematic diagram of a dual-excited synchronous generator. The principle of operation and the excitation requirements of the dual-excited synchronous generator are discussed in the following sections.

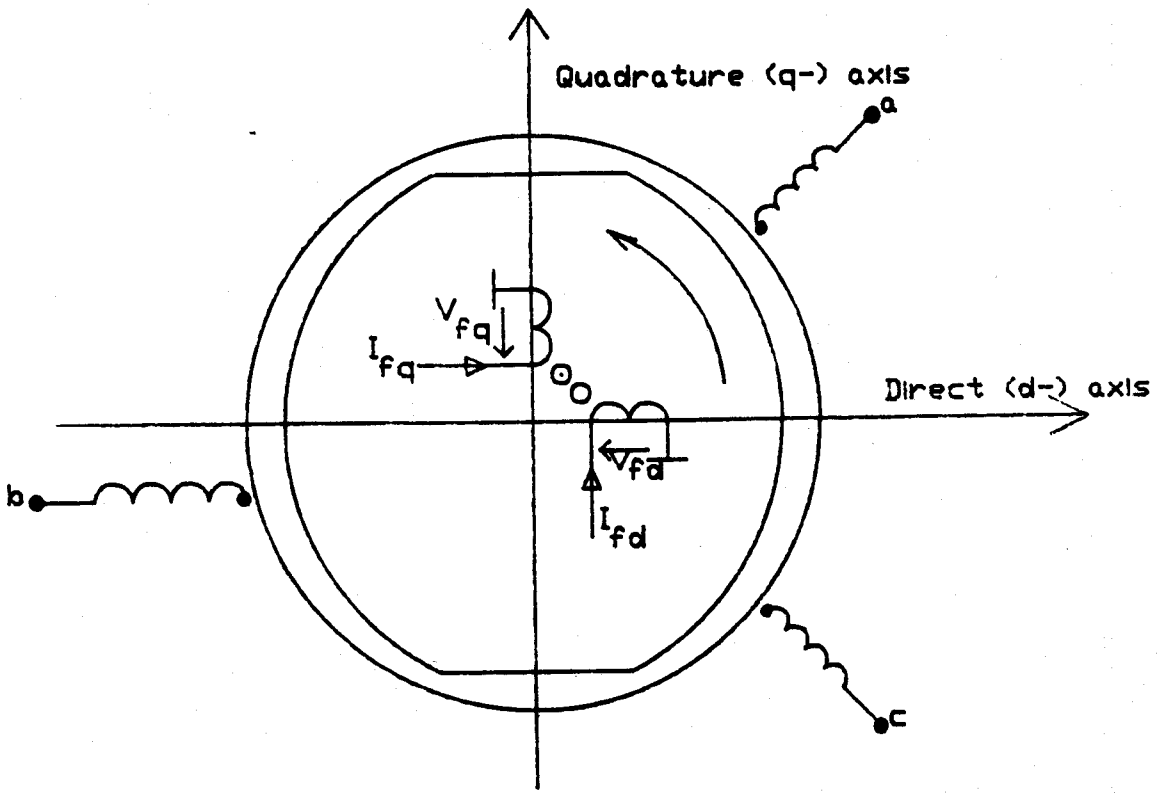



**Figure 1-2:** A schematic diagram of a dual-excited synchronous generator.

### 1.4.1. Operation of the Dual-Excited Synchronous Generator

Two excitation sources $v_{fd}$ and $v_{fq}$ supply the d- and q- axes field windings (in the rotor) respectively. The current in the d-axis winding produces a flux $\phi_d$ along the d-axis. The current in the q-axis winding produces a flux $\phi_q$ along the q-axis. These two fluxes, $\phi_d$ and $\phi_q$, produce a resultant flux $\overline{\Phi}$ in the airgap of the generator (see Figure 1-3).

Due to the displacement of 90 electrical degrees between the two field windings, the flux $\bar{\Phi}$ can be described as:

$$\bar{\Phi} = \phi_d + j\phi_q \tag{1.1}$$

$$|\bar{\Phi}| = \sqrt{\phi_d^2 + \phi_q^2} \tag{1.2}$$

where j is the complex plane notation.

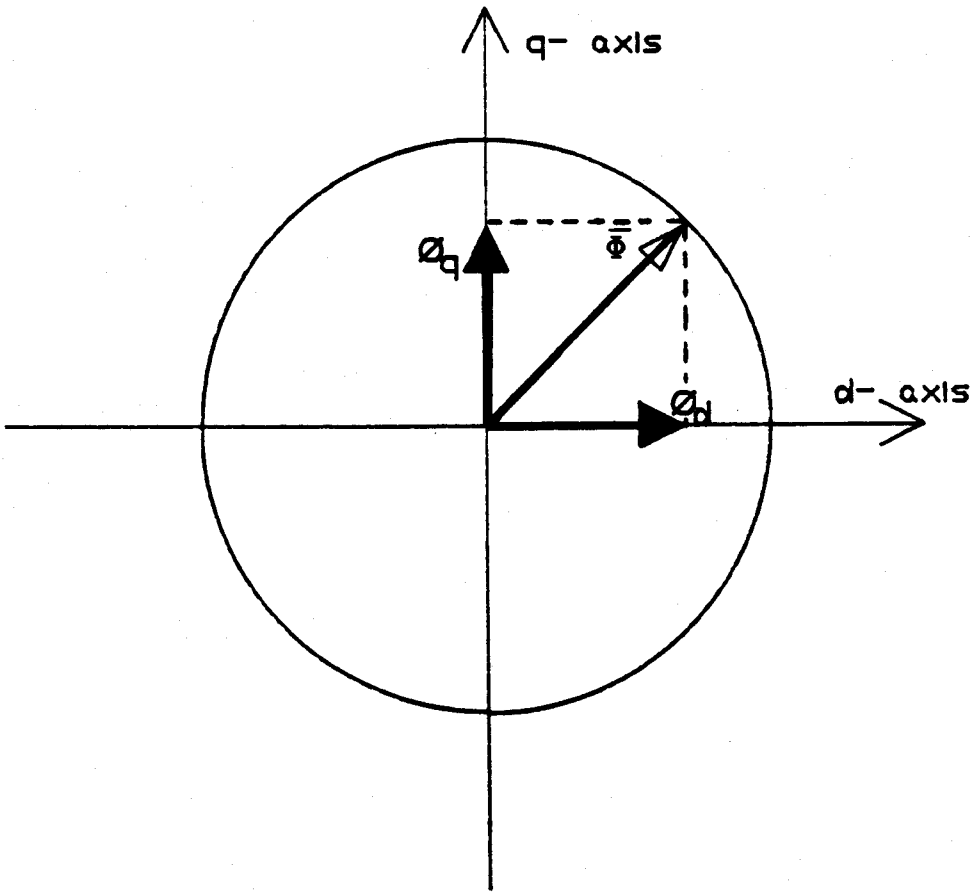



**Figure 1-3:** Two orthogonal fluxes $\phi_d$ and $\phi_q$ in a d-q plane in a dual-excited synchronous generator.

When the field windings are excited by d.c. sources, the fluxes $\phi_d$ and

$\phi_q$ are constant, and the resultant flux $\overline{\Phi}$ is stationary with respect to the rotor [21]. When the excitation currents are alternating, the resultant flux rotates at a relative angular speed with respect to the rotor. The pattern of rotation of the resultant flux depends on the maximum values of $\phi_d$ and $\phi_q$, and the phase shift between the two fluxes.

This thesis is based on the case when the two voltages $v_{fd}$ and $v_{fq}$ are:

1. sinusoidal, with respective amplitudes of $V_{fd}$ and $V_{fq}$, modulated by a voltage error signal,
2. 90 degrees phase shifted from one another, and
3. are functions of the time varying angle $\theta = 2\pi(s_a f_o)t$, with the slip $s_a$ modulating the synchronous frequency of the generator, $f_o$.

The two sources may be described as:

$$v_{fd} = V_{fd}(e)\cos(\omega_\phi t) \tag{1.3}$$

$$v_{fq} = V_{fq}(e)\sin(\omega_\phi t) \tag{1.4}$$

where: $\omega_\phi = s_a\omega_o t$,
$\omega_o = 2\pi f_o$,
e - is the terminal voltage error.

In steady state operating conditions, $v_{fd}$ and $v_{fq}$ are controlled such that, the currents in the d-axis and q-axis field windings produce fluxes $\phi_d$ and $\phi_q$ of the form:

$$\phi_d = \phi_{dm}\cos(\omega_\phi t + \gamma) \tag{1.5}$$

$$\phi_q = \phi_{qm}\sin(\omega_\phi t + \gamma) \tag{1.6}$$

where $\gamma$ is an angle which depends on the field winding parameters.

These two sinusoidal fluxes produce a resultant flux, $\overline{\Phi}$, of the form:

$$\overline{\Phi}=\phi_{dm}\cos(\omega_\phi t + \gamma)+j\phi_{qm}\sin(\omega_\phi t + \gamma) \tag{1.7}$$

For $\phi_{dm}$ not equal to $\phi_{qm}$, $\overline{\Phi}$ traces an ellipse in the d-q plane. Elliptical rotation of $\overline{\Phi}$ is known to cause heating problems [15, 21]. Thus a circular rotation is preferred. To achieve this, depending on the construction of the field windings, the excitation currents are adjusted so that $\phi_{dm}$ equals $\phi_{qm}$. Consequently:

$$\overline{\Phi} = \phi_m\{\cos(\omega_\phi t + \gamma) + j\sin(\omega_\phi t + \gamma) \tag{1.8}$$

or equivalently:

$$\overline{\Phi} = \phi_m \exp(j\{\omega_\phi t + \gamma\}) \tag{1.9}$$

where $\phi_m$ is the magnitude of $\overline{\Phi}$.

Equations (1.8) and (1.9) describe a flux with magnitude $\Phi_m$, rotating at an angular speed of $s_a\omega_o$ relative to the rotor. The dual-excited synchronous generator operates asynchronously to satisfy the relation:

$$n_o = n_r + n_\phi \tag{1.10}$$

for subsynchronous speeds and

$$n_o = n_r - n_\phi \tag{1.11}$$

for supersynchronous speeds,

where: $n_o$ - is the synchronous speed of the generator,
$n_\phi$ - is the field rotation speed relative to the rotor,
$n_r$ - is the rotor speed.

The variable $n_o$ is a regulated parameter in a variable-speed constant-frequency scheme. Since $n_r$ is variable (from a variable-speed prime mover), $n_\phi$ is electrically controlled such that it is directly proportional to slip as in Equations (1.3) and (1.4). This means that an electrical rotation is dynamically superimposed on a mechanical rotation to realize a constant armature frequency.

### 1.4.2. Excitation Requirements

The following are the excitation requirements of a dual-excited synchronous generator operated in asynchronous mode.

1. The two sources must generate sinusoidal voltages with the following properties at any instant of time.
    a. The two signals must have equal frequencies.
    b. The frequency of the signals must be proportional to the rotor slip.
    c. The two signals must be 90 degrees phase shifted from each other.
    d. The amplitudes of the signals must be controlled by the terminal voltage errors.
2. A power amplifier is required to amplify the signals to the rated current excitation levels of the generator.
3. The slip and the terminal voltage error signals must be measured continuously.

## 1.5. Thesis Objective

This thesis is a feasibility study of using a digital computer to generate excitation control signals for a dual-excited synchronous machine operated at variable speed. The computer acts as a programmable oscillator which generates the two-phase variable-frequency control signals, in accordance with the excitation requirements of the dual-excited synchronous generator.

### 1.5.1. Initial Specifications

It is assumed that the following are available:

1. a dual-excited synchronous generator,
2. the slip signal $s(t)$, and
3. the voltage error signal $e(t)$.

The main purpose of the study is to determine whether or not it is feasible to achieve the excitation requirements discussed in section 1.4.3, using direct digital control. The oscillator functions are:

1. to generate two sinusoidal signals of equal frequencies, preferably of equal amplitudes, and continuously (in real time) 90 degrees phase shifted from each other,
2. to track the slip and the voltage error signals in on-line mode, and
3. to change dynamically the frequency and the amplitude of the two signals, using the slip and the voltage error information.

### 1.5.2. The Proposed Variable-Amplitude Variable-Frequency Digital Oscillator

The inputs to the oscillator are two analog voltage signals. One is the slip signal $s(t)$, and the other is the terminal voltage error signal, $e(t)$. The outputs are two sinusoidal signals of equal frequency and amplitude, and are 90 degrees phase shifted from each other at any instant of time. The frequency of the signals is proportional to the rotor slip. The amplitude deviations from a reference value $V_{ref}$ are proportional to the voltage error signal. A block diagram of the oscillator is shown in Figure 1-4, and that of the frequency supply is shown in Figure 1-5. A block diagram of a variable-frequency-constant-frequency scheme using a dual-excited synchronous generator and the excitation supply is shown in Figure 1-6.

### 1.5.3. The Scope of Study

The study focuses on the conceptual level of the digital oscillator, to determine the procedures to be followed by the oscillator to generate the control signals for the dual-excited synchronous generator.

The thesis describes the development of an experimental digital oscillator on a VAX-11/780 computer. The VAX computer supports two real time Laboratory Peripheral Accelerator (LPA11-K) subsystems. The setup is used to conduct tests to determine the validity of the digital technique in meeting the specified excitation conditions of the dual-excited synchronous generator. The main purpose of the tests is to establish the relevant information required for the design of a practical computer based supply unit.

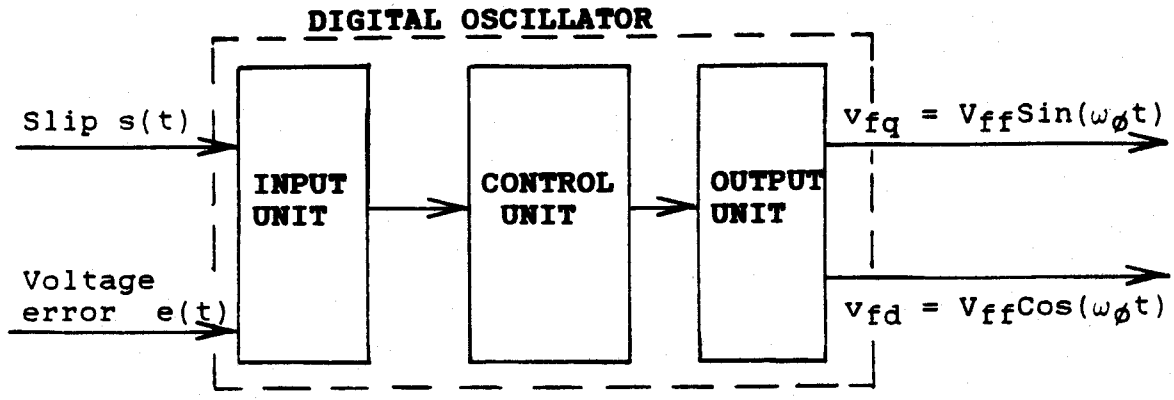



**Figure 1-4:** A block diagram of the proposed variable-amplitude variable-frequency oscillator.

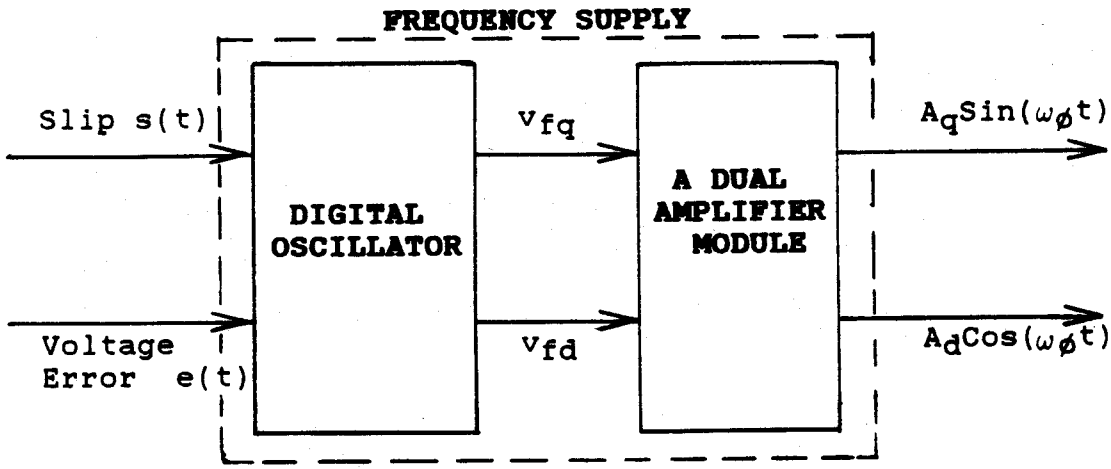



**Figure 1-5:** A block diagram of the programmable variable-amplitude variable-frequency two-phase excitation system.

The following are the potential areas identified for investigation:

1. the quality of the generated signals,
2. the control of the output frequency,
3. the control of the output amplitude, and
4. data processing procedures.

The proposed solution has a multi-process structure. In a multi-process system, several processes take place simultaneously. Consequently, the programs for the test setup are developed and structured on the basis of a modular programming technique. Modularity is expected to:

1. simplify the development task when the technique is implemented on a microcomputer,
2. allow each of the software components to be individually designed, documented, and tested,
3. allow each of the modules to be modified as parameters vary, procedures change, or system configuration is upgraded, and
4. provide a user with the flexibility of selecting or configuring control strategies from a pre-programmed set of algorithms contained in the computer memory.

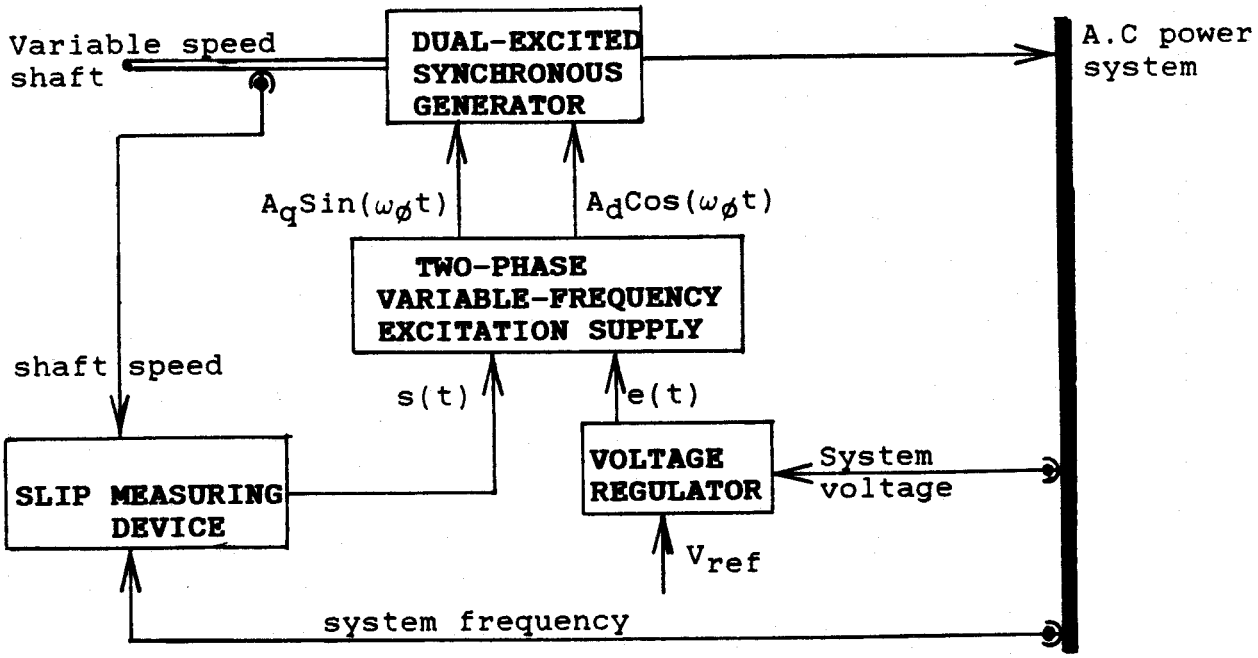



**Figure 1-6:** A block diagram of a variable-speed constant-frequency scheme employing a dual-excited generator.

# Chapter 2

# THE DIGITAL VARIABLE-AMPLITUDE VARIABLE-FREQUENCY OSCILLATOR

## 2.1. Introduction

A dual-excited synchronous generator (DESG) is used to implement a variable-speed constant-frequency generator setup. The principle of operation is to supply slip-frequency a.c. currents to the two field windings of the generator. By this means, the excitation system provides an airgap field that rotates at a constant speed relative to the stator. Under these conditions, the stator output frequency remains constant.

A direct digital approach is chosen to generate the two-phase excitation signals. This chapter presents a conceptual digital variable-amplitude variable-frequency oscillator. The digital control for both the amplitude and the frequency of the oscillator outputs is described. The real-time constraints associated with the methodology are also presented. A discussion on the areas investigated during the study is included, as well as the reasons for the investigations.

## 2.2. An Overview of The Oscillator

The block diagram of the proposed digital variable-amplitude variable-frequency oscillator was shown in Figure 1-4. The oscillator has an input unit, a control unit, and an output unit. Figure 2-1 shows the conceptual block diagram of the oscillator. The oscillator outputs are fed into an amplifier unit. The oscillator and the amplifier unit form the excitation unit. A description of each block is given in the following sections.

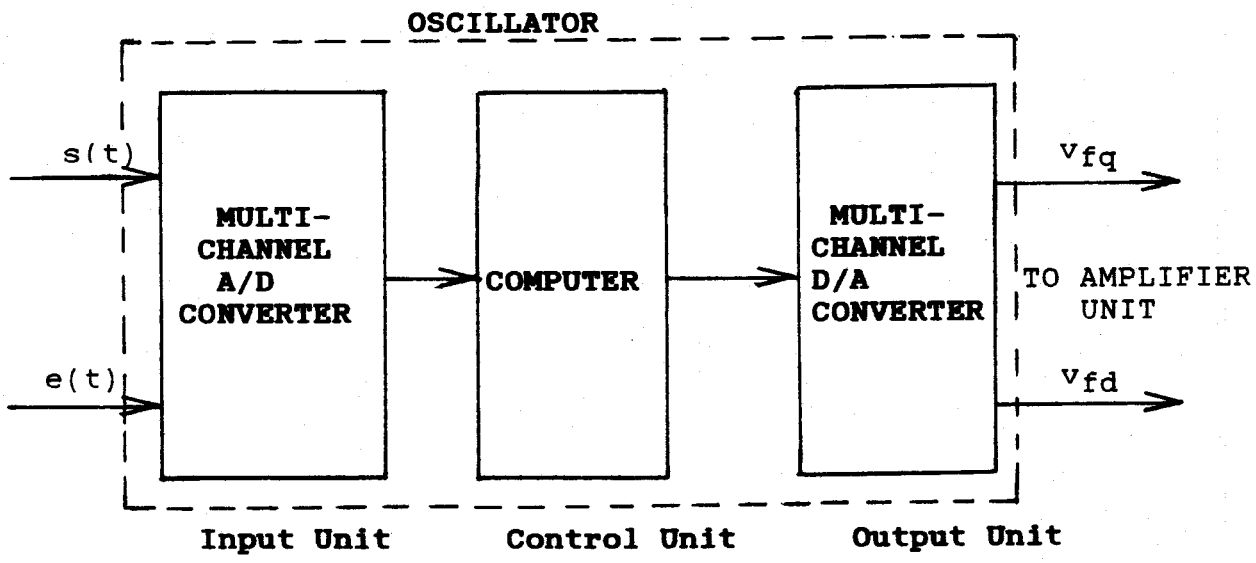



**Figure 2-1:** A conceptual block diagram of the proposed digital variable-amplitude variable-frequency oscillator.

### 2.2.1. The Input Unit

The input block is mainly a dedicated analog-to-digital (A/D) data acquisition system. It accepts two input signals: the slip signal $s(t)$ and the voltage error signal $e(t)$. The system has temporary memory buffers for storing the sampled data before it is processed.

### 2.2.2. The Control Unit

The control unit is a microprocessor assembly. It can be a dedicated computer. This unit handles all the control and the coordination tasks. In this unit, the input data is processed to update the output variables used to adjust the amplitude and the frequency of the output signals.

### 2.2.3. The Output Unit

The output unit has a programmable clock and a dedicated digital-to-analog (D/A) converter system. This unit performs the signal generation as explained in section 2.3.3.

### 2.2.4. The Amplifier Unit

A power amplifier is necessary to amplify each signal to the rated excitation current levels of the generator field. The gain variation for amplification can either be superimposed on the output signals before amplification or set in programmable amplifiers. The first case requires variable-amplitude variable-frequency signals. This case depends on:

1. the supply of the digital-to-analog converter, and
2. the computational complexity involved in changing the contents of the D/A buffers before being emptied.

For the second case, programmable amplifiers should be used. This requires constant-amplitude variable-frequency signals. Furthermore, a gain signal is required to set the gains of the amplifiers.

However, no power amplifier was built or used during the study. This section emphasizes that the oscillator is useful only if a proper power amplifier is available.

## 2.3. Formulation of The Digital Methodology

This section presents the derivations of the techniques used to control the frequency and the amplitude of the output signals. Relevant to the derivations is the fact that analog information is input to the computer through an A/D interface, and the processed information is output from the computer through a D/A interface.

The A/D and D/A conversions are sampling operations. Such operations require stable driving real-time clocks. The following discussion assumes the availability of the multi-buffered devices, such as the LPAs [23], which control the A/D and D/A interfaces driven by programmable real-time clocks.

The A/D sampling process must be driven at a constant frequency, which is a requirement of data processing algorithms [24]. The A/D sampling frequency is selected high enough to avoid aliasing problems [25, 26, 27, 24, 28, 29].

In the following sections the digital-to-analog conversion is regarded as a signal generation technique. In the discussion, $f_{sa}$ denotes the D/A sampling rate, $T_{sa}$ denotes the D/A intersample time per signal, and $f_{da}$ denotes the frequency of the output signals. For the case of analog-to-digital conversion, $f_{ad}$ denotes the A/D sampling rate, and $T_{ad}$ denotes the A/D intersample time for each sampled input signal.

### 2.3.1. The Technique for Frequency Variation

Consider a digital-to analog conversion process taking place under continuous sampling at a sample rate of $f_{sa}$. Consider also that the output of the digital-to-analog converter is a continuous alternating signal. An angle $\theta_n$ in radians can be associated with the oscillating signal at any instant of time $t_n$ (see Figure 2-2), such that:

$$\theta_n = 2\pi f_{da} t_n \tag{2.1}$$

where: $\theta_n$ - is the angle corresponding to the $n^{\text{th}}$ sample,
$t_n$ - is the time corresponding to the $n^{\text{th}}$ sample, and
$f_{da}$ - is the frequency of the D/A output signal.

The reciprocal of the sampling frequency $f_{sa}$ gives the intersample time $T_{sa}$:

$$T_{sa} = \frac{1}{f_{sa}} \tag{2.2}$$

At the $n^{\text{th}}$ clock pulse, the real-time $t_n$ is given by:

$$t_n = nT_{sa} \tag{2.3}$$

In terms of $n$ and $T_{sa}$, the angle $\theta_n$ can be expressed as:

$$\theta_n = 2\pi f_{da} n T_{sa} \tag{2.4}$$

and explicitly:

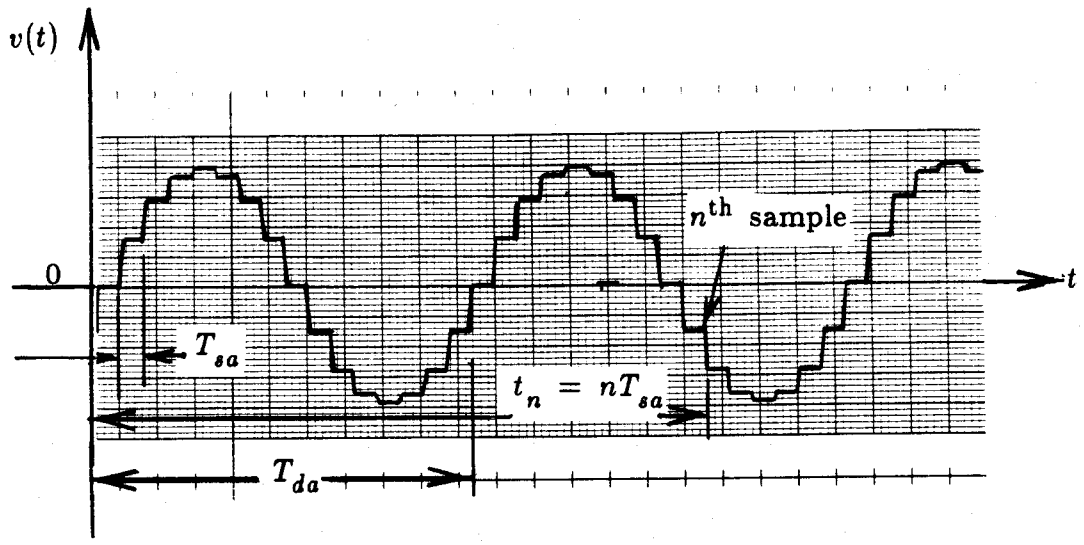



**Figure 2-2:** Oscillating voltage output from a D/A converter.

$$f_{da} = \frac{\theta_n}{2\pi n T_{sa}} \tag{2.5}$$

During the sampling process, $n$ is automatically varied by the clock. The value of $T_{sa}$ is fixed by the sampling frequency, and $\theta_n$ is the angle at the $n^{th}$ clock tick. If the factor $\frac{\theta_n}{n}$ in Equation (2.5) is a constant, then, the frequency $f_{da}$ can be varied by changing the value of $T_{sa}$, which is achieved by changing the sampling rate $f_{sa}$. Thus, changing the D/A sampling frequency changes the frequency of the output signals. This enables the generation of variable frequency signals.

The use of this technique to generate signals demands the execution of both the A/D and the D/A sampling processes continuously. This obser-

vation suggests that the two processes must not share the same driving clock.

### 2.3.2. Signal Waveform

This study uses the sine and the cosine functions. The angle $\theta_n$ is identified as a common argument of both functions. These two functions are orthogonal [24, 28]. The choice of these two functions fulfils the excitation condition of 90 degrees phase shift between the excitation signals for a dual-excited synchronous generator. The digital sine and cosine data are numerically generated. The data is then stored in the computer memory, ready for conversion to analog values.

Numerically, a cycle of $2\pi$ radians is divided into $N$ subdivisions of equal size such that the $m^{\text{th}}$ subdivision correspond to an angle:

$$\theta_m = \frac{2\pi m}{N} \tag{2.6}$$

where: $0 \leq \theta_m < 2\pi$, $m$=0,1,2,...,$N$−1.

For each angle $\theta_m$, there exist values of a sine and a cosine ordinate given by:

$$\left.\begin{aligned} \cos(\theta_m) &= \cos(\frac{2\pi m}{N}) \\ \sin(\theta_m) &= \sin(\frac{2\pi m}{N}) \end{aligned}\right\} \tag{2.7}$$

Apparent from Equation (2.7) is that, $T_{sa}$ has no effect on both $\cos(\theta_m)$ and $\sin(\theta_m)$. Therefore, the waveform of the output signals is

defined by setting each of the angles $\theta_m$ to a constant. The distortion of the waveform depends only on the value of $N$. As well, the values of $\cos(\theta_m)$ and $\sin(\theta_m)$ are independent of the signal frequency, $f_{da}$.

### 2.3.3. Continuous Signal Generation

A cycle of each of the two sinusoidal functions is first divided into $P$ equal-sized integral parts. These cycle parts are labelled 0,1,2,3,....,$P-1$. Each of these $P$ parts is subdivided into $M$ equal divisions. The ordinates corresponding to $M$ subdivisions of each function are numerically computed and then stored in a one dimension data buffer $[BUF]$ of length $L$ ($L$=2$M$). This process initializes a set of $P$ data buffers. In each buffer, the ordinates are organized in alternating positions as:

$$[BUF] = \begin{bmatrix} \sin(\theta_o) \\ \cos(\theta_o) \\ \sin(\theta_1) \\ \cos(\theta_1) \\ \vdots \\ \sin(\theta_{M-1}) \\ \cos(\theta_{M-1}) \end{bmatrix} \tag{2.8}$$

The arrangement of the ordinates in each buffer allows simultaneous signal generation. The P buffers are contiguous. They are arranged to form a ring structure as illustrated in Figure 2-3. The total number of samples per cycle of each function is:

$$N = PM \tag{2.9}$$

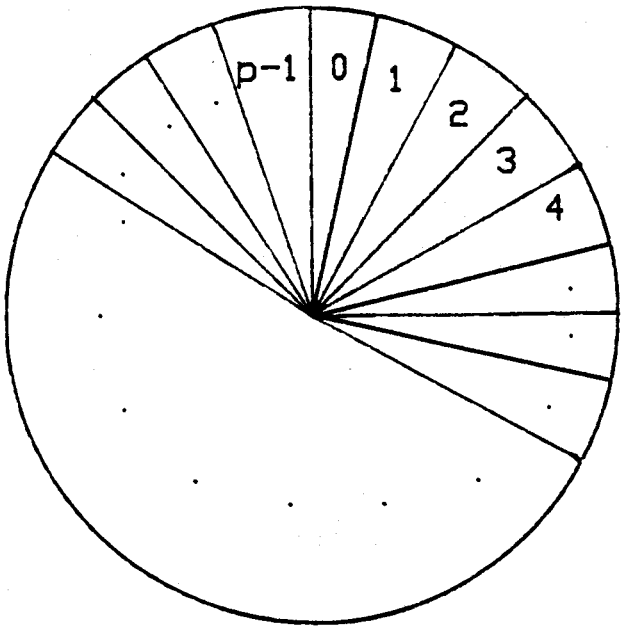



**Figure 2-3:** A ring buffer structure.

The ring buffer structure allows the buffers to be reused during the sampling process. In this case, a copy or a modification of each of the $P$ buffers is emptied after every $2PM$ clock pulses. In this way, a continuous signal generation is achieved.

### 2.3.4. The Dual Control of Frequency and Amplitude

The other excitation condition is that the two sinusoidal output signals should have equal frequencies at any instant of time. This is achieved by the use of one real time clock to control the D/A sweep generating the two signals. At the $n^{th}$ clock tick, the same $n$ is used to identify $\sin(\theta_n)$ and $\cos(\theta_n)$. Evident from Equation (2.5) is that changing $T_{sa}$ changes $f_{da}$, which is the frequency of both signals. The control of the amplitude depends on the control option as discussed in section 2.2.4. Of interest here is the case in which the amplitude control is carried out before amplifying the output signals.

The D/A data is modified by multiplying each of the entries of a labelled buffer by a predetermined factor $K_v$. The result is a modified buffer $[BUF]'$ for emptying:

$$[BUF]' = K_v.[BUF] \tag{2.10}$$

Each time an amplitude change is to be effected, both the sine and the cosine ordinates are multiplied by the same factor $K_v$. As a result, the two output signals are adjusted to have equal peak amplitudes. The equal amplitude output signals are chosen for convenience purposes. Proper gains will be set on the amplifiers taking into consideration the field winding data.

## 2.4. The Multiplication Factor for Amplitude Control

The amplitude of the output signals must be varied such that the amplitude deviations from the reference value $V_{ref}$ are proportional to the voltage error signal $e(t)$. The reference signals in this study are of unit amplitude. The variation of the amplitude (as discussed in section 2.3.4) is achieved by multiplying the samples of the reference signals by an appropriate factor $K_v$. For each sample $e[n]$ of the voltage error signal, the factor $K_v[n]$ is determined as follows:

$$K_v[n] = K_{ref} \pm K_e e[n] \tag{2.11}$$

where: $K_{ref}$ - is the reference multiplication factor,
$K_e$ - is the voltage error constant with units $[volt]^{-1}$, and
$e[n]$ - denotes the $n^{th}$ sample of the voltage error signal.

The positive sign in Equation (2.11) corresponds to a positive-amplitude modulation, and the negative sign corresponds to a negative-amplitude modulation [30].

## 2.5. The Frequency Control Function

This section describes the relationship between the slip and the output frequency of the oscillator. Consider the case where the ring buffer is set to have only one cycle part ($P$=1,$N$=$M$), that is, one full-cycle of each function. The ordinates are loaded in alternating sequence as illustrated by Equation (2.8). For this case, $L$=2$N$. The use of one driving clock to control the signal generation sets the signals to have equal periods, and therefore equal frequencies. For a D/A intersample time of $T_{sa}$ per signal, the value of the time periods is given by:

$$T_{da} = \frac{LT_{sa}}{2} \tag{2.12}$$

Corresponding to a signal frequency:

$$f_{da} = \frac{2}{LT_{sa}} \tag{2.13}$$

For a variable-speed operation with a dual-excited synchronous generator, the D/A sampling frequency $f_{sa}$ must be changed dynamically in proportion to the slip signal $s(t)$. Two cases are now considered as regards to the slip interpretation. The first case is theoretical and is used to derive the general frequency control function. The second case is that of operating the generator at a non-zero slip, which is practical.

### 2.5.1. The General Frequency Control Function

This case is evident from the functional Equations (1.3) and (1.4). The control of the frequency of the output signals can be shown to be:

$$f_{da} = s_a f_o \tag{2.14}$$

where: $f_o$ - is the system synchronous frequency,
and $s_a$ - is the dimensionless slip variable.

Solving for $T_{sa}$ from Equations (2.13) and (2.14), the following control expression is obtained:

$$T_{sa} = \frac{2}{Lf_o s_a} \tag{2.15}$$

This control function shows that the intersample time is inversely proportional to the slip. The variable $T_{sa}$ can explicitly be used to update

the D/A sampling frequency as slip varies. The application of the control function has the following constraints.

1. $T_{sa}$ can never be negative, but slip can.

2. A zero sampling frequency corresponds to zero frequency output (at zero slip). The control law would set an infinite value of $T_{sa}$. The setting is impractical with digital systems. Hence, d.c. excitation can not be realized by sampling control.

3. Infinite sampling frequency corresponds to an infinite slip. The sampling setting at such extremes equals zero ($T_{sa} = 0$). The setting is likely to cause a "divide by zero" error in the digital system. This condition is an obvious design constraint. The other constraint associated with large values of slip is the supply of excitation power. It is known [7, 19] that the larger the slip, the more excitation power is required. Thus, an infinite excitation power is required to generate power at an infinite slip. This is not practical.

### 2.5.2. Operation at Non-Zero Slip

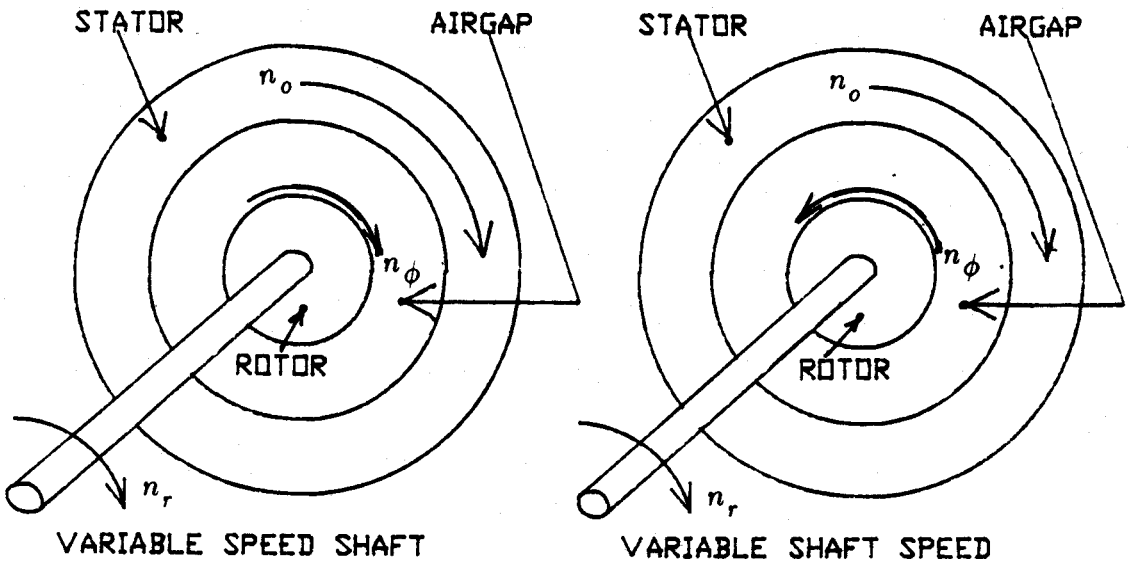
This case eludes the constraints pointed out in section 2.5.1. The dual-excited synchronous generator, performing as an asynchronous generator [15], is driven at speeds within a predetermined speed range. The speeds in this range are here referred to as usable shaft-speeds. The speeds can be super-synchronous or subsynchronous. Corresponding to the usable shaft-speed range is a usable slip-range. The slip is negative for supersynchronous speeds, and is positive for subsynchronous speeds. Since it is a problem to achieve the d.c. excitation by sampling control, the generator operation is limited to speeds either below or above the synchronous speed. Hence, the sign of the slip must be established before the generator is put into operation.

Excitation power is supplied to the rotor at slip frequency, when the slip is positive. In this case, the rotor excitation has to produce a field in the airgap rotating in the same direction as the rotor ( see Figure 2-4(a)). The direction of rotation of the field is set by the way the two-phase rotor is supplied from the two-phase excitation supply. Reversal in the connection of one of the phases reverses the direction of rotation of the field.

Excitation power flows out of the rotor at slip frequency, when the slip is negative. Now, the rotor excitation has to produce a field in the airgap rotating in a direction opposite to that of the rotor (see Figure 2-4(b)). The direction of the field rotation sets the sign of the slip. Once the sign is set, the slip information can be interpreted without the sign. Operation outside the usable slip-range is not acceptable, and shutdown may be necessary.

### 2.5.3. Slip Range for Technique Verification

A slip-range of $0 < |s_a| \leq 1.0$ is considered adequate for the technique verification. The oscillator uses the absolute values of the slip. In practice, the sign of the slip has to be implemented externally, by proper choice of the phase-sequence connection to the rotor windings. Figure 2-5 shows the variation in the speed $n_\phi$ of the rotating field corresponding to the usable slips and shaft-speeds for a synchronous speed $n_o$. The negative values of $n_\phi$ correspond to the direction of rotation opposite to that of the rotor. The positive values of $n_\phi$ correspond to the rotation in the same direction as that of the rotor.




(a) Relatively $n_o = n_r + n_\phi$ (b) Relatively $n_o = n_r - n_\phi$

**Figure 2-4:** Operation of the dual-excited synchronous generator at (a) subsynchronous speeds, (b) supersynchronous speeds.

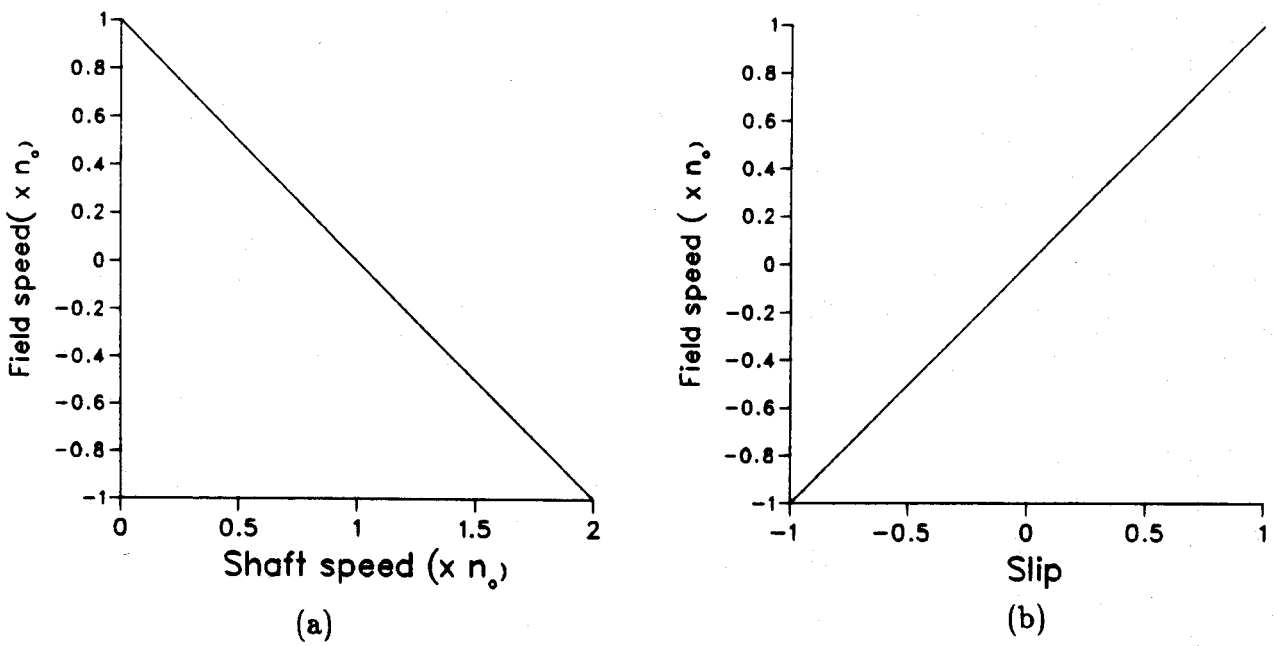



**Figure 2-5:** (a) Usable shaft-speeds, (b) Usable slip-range.

The choice of the direction of rotation of the airgap field relative to the direction of the rotor is dependent on the availability of an appropriate power amplifier. The power amplifier has to supply power to the rotor when operating at subsynchronous speeds. The amplifier has to facilitate the power flow out of the rotor when operating at supersynchronous speeds.

### 2.5.4. The Actual Slip Values

The slip signal, $s(t)$, is a voltage signal. The signal is selected such that the slip values are proportional to the instantaneous values of the signal. The actual slip values have no dimension. Therefore, each sample $s[n]$ of the slip signal has to be converted to the actual slip value $s_a[n]$ by multiplying it by a constant $K_s$, that is:

$$s_a[n] = K_s s[n] \tag{2.16}$$

where: $s[n]$ is in volts,
$K_s$ has the units $[\text{volt}]^{-1}$,
and $s[n]$ denotes the $n^{\text{th}}$ sample of the slip signal $s(t)$.

When $K_s = 1.0\ [\text{volt}]^{-1}$, the actual slip value $s_a[n]$ is numerically equal to the sample value $s[n]$. In this case, the units may be ignored in programming the system.

## 2.6. Areas for Investigation

Four potential areas were identified in chapter 1 for investigation, namely, the quality of the generated signals, the frequency control, the amplitude control, and the data processing procedures. These areas are explained further in the following sections.

### 2.6.1. The Quality of the Generated Signals

Of particular interest here is the waveform distortion. The latter is a relevant indicator on whether or not filtering is to be performed on the output signals. This area is thoroughly investigated for steady state conditions. The results are reported in Chapter 4.

### 2.6.2. The Frequency Control

Typical of any real-time clock is that there are fixed combinations of clock frequency and integer values of counter presets. The combinations allow only a subset of possible frequencies. An investigation was necessary to establish adequate D/A sampling frequencies. It is shown that one value of the number of samples per cycle ($N$) and one range of clock settings $T_{sa}$ are not adequate to provide control flexibility. A study on different combinations of $N$ and $T_{sa}$ exposed more control possibilities. The details of this study are reported in Appendix B.

### 2.6.3. The Amplitude Control

The accuracy of converting a sequence of digital numbers to an analog signal is dependent on:

1. the number of quantization levels of the digital-to-analog converter used [29],
2. the hardware structure of the converter, and
3. the d.c. supply to the converter hardware.

The investigation of this area provides details useful for selecting a suitable size of a digital-to-analog converter. The results of this study are included in Chapter 4.

### 2.6.4. The Data Processing

The input data has to be processed to estimate the slip and voltage errors. A study on the characteristics of the possible slip and voltage error signals would provide some details useful in the selection or the design of the real-time algorithms for data processing. Equally useful is a study on the efficiency, speed of response, and accuracy of the selected algorithms. The study of this area is recommended for future research. In this thesis, the slip and the voltage error signals are assumed to be available. The algorithms used for data processing are described in a separate Internal Report referred to as reference [31]. The overall software structure is described in section 3.3.

# Chapter 3

# OSCILLATOR IMPLEMENTATION: HARDWARE AND SOFTWARE DESCRIPTION

## 3.1. Introduction

The digital-to-analog (D/A) conversion was discussed in section 2.3 as a technique to generate variable-frequency sinusoidal signals. The methodology uses numerically generated data for output signals. This data is to be converted to analog values by a digital-to-analog converter driven by a programmable real-time clock. In section 2.3.1, it was shown that the variation of the D/A sampling frequency varies the frequency of the output signals.

An experimental oscillator was implemented on the VAX-11/780 computer to evaluate the validity of this signal generation methodology. The VAX supports two real-time Laboratory Peripheral Accelerators (LPA11-Ks) which are 16-bit-devices. Both the LPAs are peripheral devices to the VAX-computer. Each LPA consists of two microcomputers that handle the real-time I/O processing [23]. These LPAs control a set of A/D and D/A converters, and real-time clocks. The LPAs are connected to the VAX proces-

sor through a UNIBUS adapter. This chapter describes the hardware and the software components of the test setup.

## 3.2. Hardware Description

### 3.2.1. Experimental Setup

The block diagram of the experimental setup used to verify the signal generation technique is shown in Figure 3-1. The setup is organized such that the input, the control, and the output blocks are distinguishable.

The input block is comprised of:

1. two function generators (HP MODEL 3310A/WAVETEK MODEL 180),
2. a 16-channel, 12-bits, analog-to-digital converter hardware (+/-5V supply), and
3. a programmable clock capable of driving the A/D converter to sample up to 15,000 samples per second.

The analog-to-digital converter circuitry and the clock are controlled via one of the LPAs identified as LPA0 in Figure 3-1. The two function generators were used to simulate the slip and the voltage error signals.

The control unit is the host VAX-11/780 computer, to which a video monitor and a keyboard are interfaced for interactive user operations.

The output unit is implemented on the second LPA subsystem identified as LPA1 in Figure 3-1.

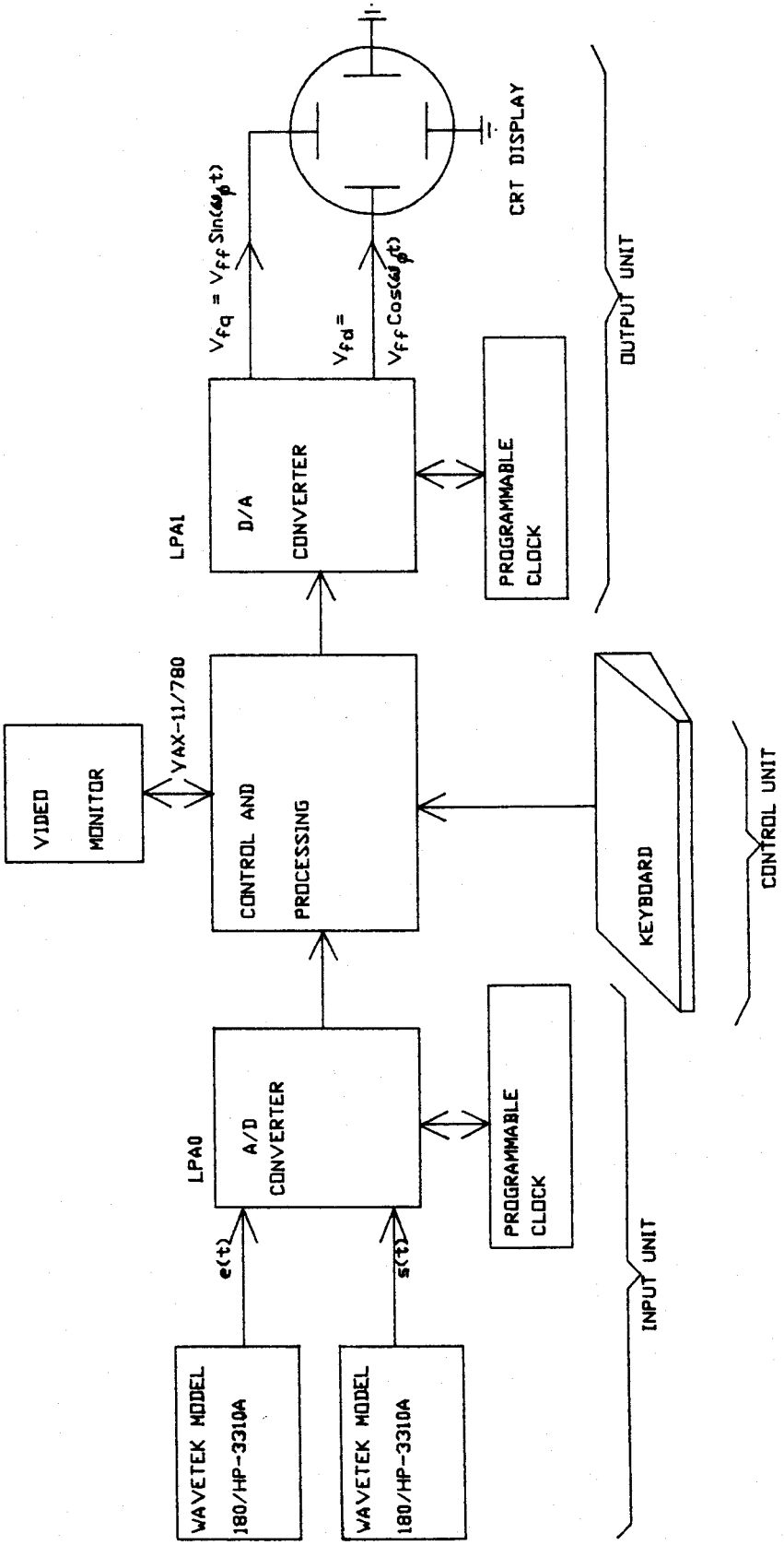



**Figure 3-1:** A block diagram of the experimental set up.

The components of this unit are:

1. a 4-channel, 12-bits, digital-to-analog converter hardware (+/- 5V supply),

2. a programmable clock capable of driving the D/A converter to sample up to 15,000 samples per second, and

3. a dual channel oscilloscope for displaying the output signals.

### 3.2.2. The Motivation to Use The LPAs

The VAX-11/780 is a time sharing computer. Both LPA11-K subsystems have real-time hardware. Since each LPA is a separate microcomputer system that handles the I/O processing, both data acquisition and processing may be performed simultaneously. Thus, the time sharing of the VAX does not affect the data acquisition processes. Instead, the VAX, as a host processor, supervises both the acquisition and the processing operations. The other inducements are as follows.

1. The LPA subsystems are available.

2. Each LPA has a programmable clock. The rate of each clock may be changed under program control.

3. The LPAs operate as an integral part of the VAX/VMS operating system. These subsystems are programmable in VAX-FORTRAN. The VAX/VMS operating system supports several program-accessible procedures that provide access to the LPAs [23].

4. Each LPA functions as a multi-buffered device. This feature favours the use of the ring buffered structure discussed in section 2.3.3.

## 3.3. Software Description

The LPA11-K arrangement was programmed such that the application programs run under the supervision of a real-time executive VAX-program. This section presents the structure of the test software, and the data flow when the programs are running.

### 3.3.1. The Software Structure

As shown in Figure 3-2, the software has a multi-process structure with three real-time processes. The processes are here referred to as process A, B, and C. Process A is the supervisor of the test software. The functions of process A are:

1. to initialize and configure the test software,
2. to start and stop processes B and C when requested, and
3. to generate the sine and the cosine data values for signal generation.

Process B is a real-time A/D process. This process acquires the slip and the voltage error data at a set sampling frequency. It then processes the acquired data to extract the slip and the voltage error information by using resident algorithms. The slip information is used to update the D/A sampling frequency as discussed in section 2.4. The voltage error information is used to update the D/A multiplication factor $K_v$ as discussed in section 2.3.4. Process B drives the analog-to-digital hardware of the LPA0.

Process C is a real-time D/A process. The main function of this process is to change the amplitude of the output signals using the $K_v$ set-

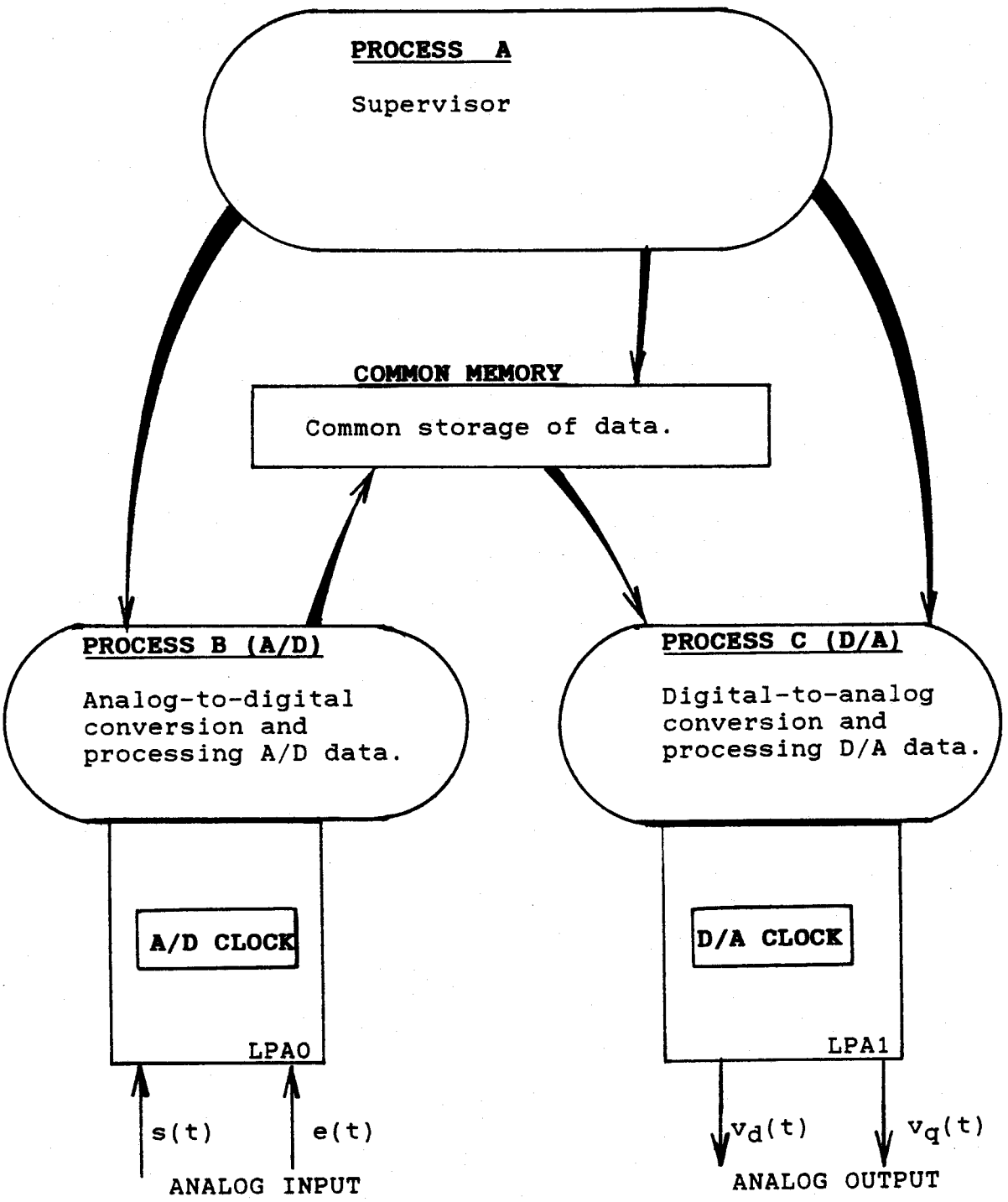



**Figure 3-2:** Multi-process structure of the test software.

tings from process B. First, it accesses a D/A data buffer, regarded as empty, fills it with modified D/A data; and then, releases the buffer to the LPA1 for D/A conversion to analog signals.

### 3.3.2. Interprocess Data Flow

The test software executes in two stages, namely:

1. the initialization stage, and
2. the continuation (dynamic) stage.

#### 3.3.2.1. The Initialization Stage

The flow diagram of Figure 3-3 shows the flow of data during the initialization stage. The supervisor, process A, performs the following tasks:

1. sets the initial sampling rates for processes B and C,
2. sets the initial multiplication factor $K_v$,
3. computes the sine and the cosine ordinates, and stores the data in memory, ready to be loaded into D/A data buffers, and
4. starts the data transfer requests for processes B and C. When the software is configured for the oscillator mode, process C is started first. Before process B is activated, the output signals are of constant amplitude and constant frequency. The amplitude and the frequency of the output signals start to change immediately after process B is activated.

#### 3.3.2.2. The Continuation Stage

Figure 3-4 is a flow diagram showing the flow of data during the continuation stage. Both processes B and C operate under continuous sampling. Process B is activated each time an A/D data buffer is filled with data by the LPA0. While active, process B uses the A/D data to compute the slip and the voltage error corresponding to a time frame; then, it sets the D/A

sampling rate and the multiplication factor $K_v$ for the output signals. After processing the entire A/D buffer, process B releases the buffer to the LPA0 for refilling with new data.

Similarly, process C is activated each time a D/A data buffer is emptied by the LPA1. This process adjusts the amplitude of the data in the D/A buffer. After modifying the buffer, process C releazes the buffer to the LPA1 for emptying.

The software is organized such that processes B and C execute continuously. While processes B and C are active, process A is suspended. In the waiting state, process A monitors the keyboard for requests to stop processes B and C, or change the A/D sampling rate. The details of the actual modules are summarized in Appendix B, and the listing of the programs can be found in reference [31]. Appendix B is reproduced from chapter 1 and 2 of the internal report.

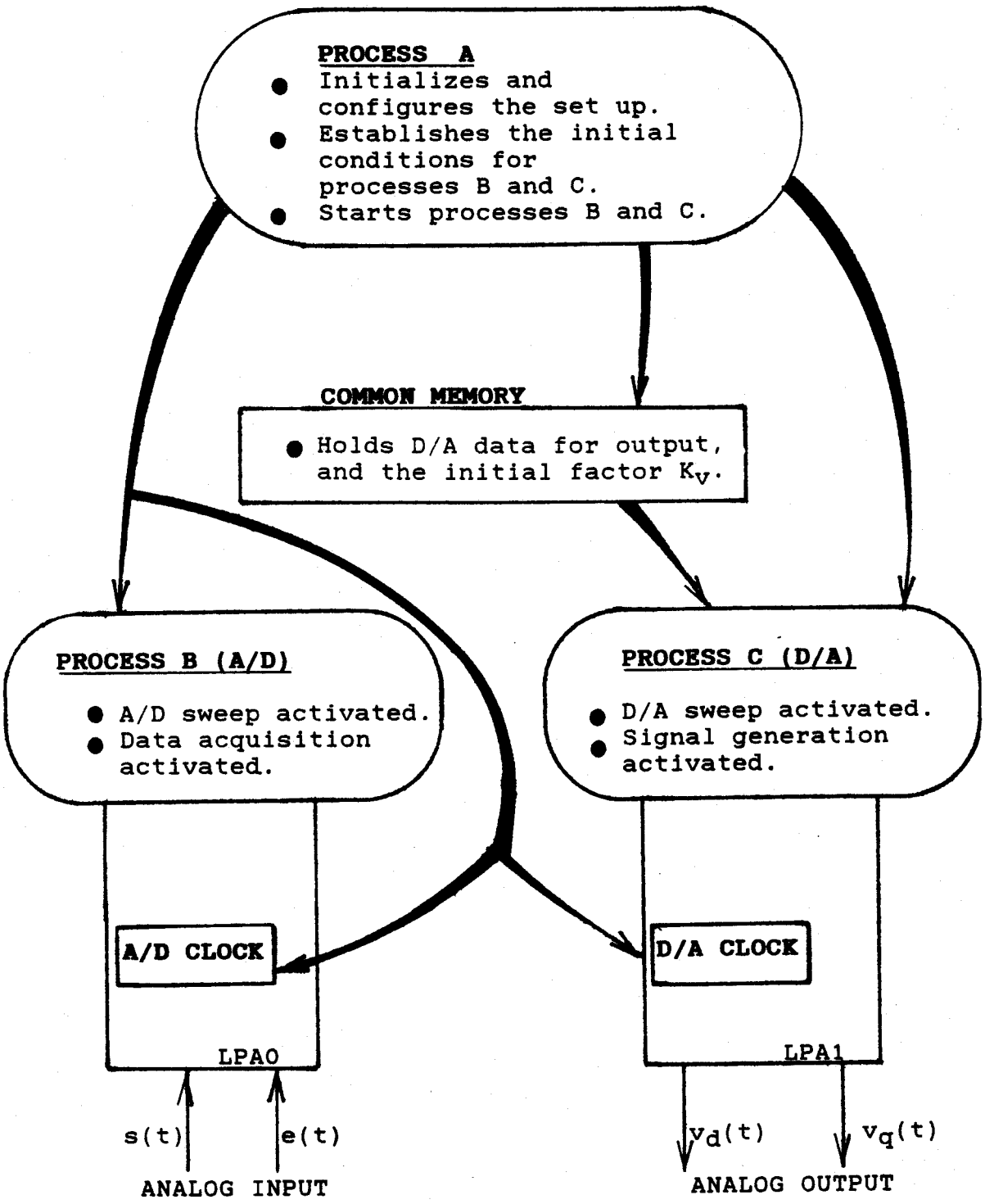



**Figure 3-3:** A flow diagram showing the flow of data during the initialization stage.

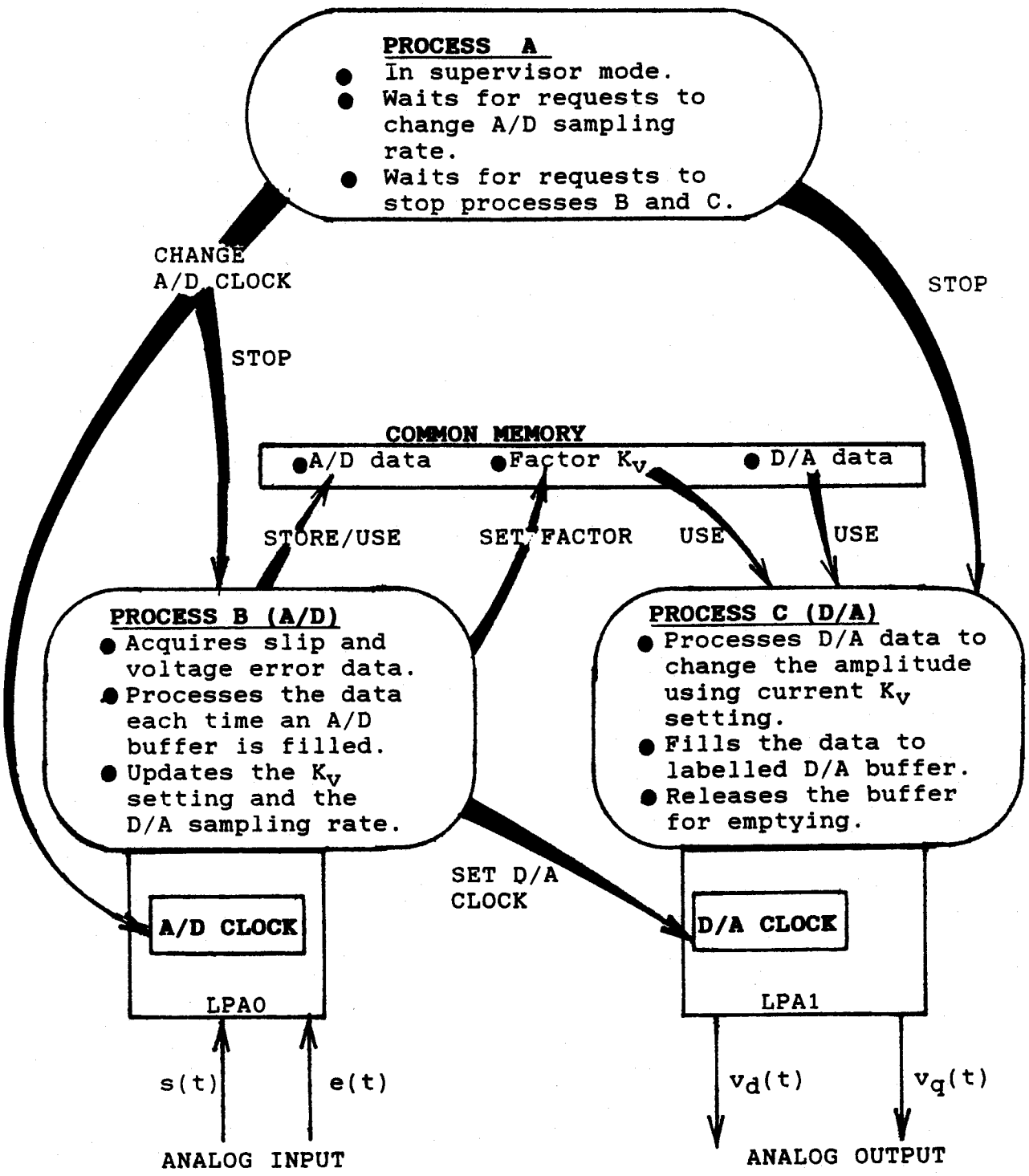



**Figure 3-4:** A flow diagram showing the flow of data during the continuation stage.

# Chapter 4

# EXPERIMENTS, RESULTS AND DISCUSSION

## 4.1. Introduction

Experiments were carried out to evaluate the validity of the signal generation methodology formulated in Chapter 2, and to investigate the performance of the digital oscillator. This chapter presents and discusses the experiments, the constraints encountered while performing the tests, and the experimental results obtained.

## 4.2. The Test Procedure

The test software is designed such that several experiments can be conducted in a single experimental session. The test procedure has one major step, that is, executing the test software. While running, the program prompts the user to make choices on what to do. It may be to test process B (A/D), process C (D/A), or test the oscillator mode (running both processes B and C).

The program is documented such that it guides the user on what to enter or change. The user responses are entered through the keyboard.

The main prompts are those requesting:

1. the clock settings,
2. the reference synchronous frequency $f_o$,
3. the length of the A/D data buffers, and
4. the length of the D/A data buffers and the manner these buffers are loaded with D/A data for output. The variation in the length of the D/A buffers and the manner in which they are filled with data varies the number of samples per cycle ($N$). Options of varying $N$ are derived in Appendix B.

The experiments were conducted in real-time. The oscillator outputs were recorded on a plotter, and at the same time displayed on a dual channel CRT operating in the X-Y mode. The X-Y mode simulates the d-q rotor windings setup in a dual-excited synchronous generator. A rotating vector whose direction of rotation is fixed by the connections to the channels (A and B) of the CRT, can be observed on the CRT screen. Reversal in the direction of rotation of the vector can be observed by interchanging the connection of one of the channels. The magnitude and frequency of the rotating vector are the visual indicators of the response of the oscillator to various types of voltage error and slip signals. The value of $K_e$ in Equation (2.11) is set to 1.0 $[\text{volt}]^{-1}$, and the value of $K_{ref}$ is set to 1.0, for all the results presented. The input signals $e(t)$ and $s(t)$ are either unidirectional or alternating with frequencies as low as 0.005Hz. The user must specify the waveforms and the frequencies of the input signals and set them on the function generators.

## 4.3. Classification of Experiments

The experiments conducted fall into three categories. The first category is of those experiments on the verification of the methodology. The second category is of those experiments on the analysis of the output signals. The third category consists of the experiments on the performance of the digital oscillator.

### 4.3.1. Experiments on The Methodology

The experiments in this group were aimed at verifying the digital methodology discussed in section 2.3. The experiments were organized specifically to study the following:

1. the type of waveforms of the D/A signals,
2. the effect of changing the D/A sampling frequency ($f_{sa}$),
3. the effect of varying the number of samples per cycle ($N$),
4. the phase shift between the output signals, and
5. the effectiveness of amplitude and frequency adjustment for both output signals.

### 4.3.2. Experiments for The Analysis of The Output Signals

The purpose of the analysis was to establish the quality of the generated excitation signals. The experiments were a series of harmonic analyses on the sampled data of the output signals. The effects studied were those caused by varying the number of samples per cycle ($N$) for each signal.

### 4.3.3. Experiments on The Performance of The Digital Oscillator

The performance of the oscillator was investigated in three stages:

1. amplitude modulation at a constant frequency,
2. frequency modulation at constant amplitude, and
3. stages (1) and (2) performed simultaneously.

A variation in these experiments was made by varying the waveforms of the modulating signals (the slip signal $s(t)$, and the voltage error signal $e(t)$).

## 4.4. Real-Time Constraints

This section points out some real-time constraints encountered while performing the experimental tests.

### 4.4.1. The Host Computer

The VAX-11/780 computer is a multi-function system. The system serves many users. Implementing a controller in such a system makes time delays unavoidable. These delays make the performance of the setup slow. Thus, the LPA11-K subsystems, while working with the VAX, can not be used to realize a practical controller for critical processes; albeit they have the ability to perform as direct-digital-controllers. The other drawback with the setup is that its performance is dependent on the software priority within the VAX computer, and as a result of this, the VAX system stops the execution of the oscillator control when programs with higher priority require the system.

### 4.4.2. The Length of The Data Buffers

All the data buffers are set to have the same size. The setup processes both A/D and D/A data in steps of buffer lengths. This buffer structure prevents access to individual samples by a pointer while the buffer is being filled with data by process B or emptied by process C. Furthermore, the cumulative buffer length can at most be 32,768.

### 4.4.3. The Clock Settings

The programmable real-time clocks in the LPAs operate such that the clock periods are quantized in units of 1$\mu$sec or 10$\mu$sec [23]. The inter-sample time settings are limited within the ranges of:

1. 100$\mu$sec - 65535$\mu$sec; for 1$\mu$sec as the quantization unit, and
2. 65536$\mu$sec - 650msec; for 10$\mu$sec as the quantization unit.

Some sampling frequencies are not obtainable, and those obtainable are not exact but approximate. The time resolution is given by the clock quantization units. The time periods of the output signals are set at the resolution of 1$\mu$sec in the first range, and at the resolution of 10$\mu$sec in the second range. Thus, higher quantization units give poor resolution in approximating the frequencies of the output signals.

### 4.4.4. The LPA Procedures

The callable LPA routines supported by the VAX/VMS operating system are used as off-the-shelf packages. They are not optimized for control purposes. The LPA programming procedures are included in reference [31].

## 4.5. Verification of The Methodology

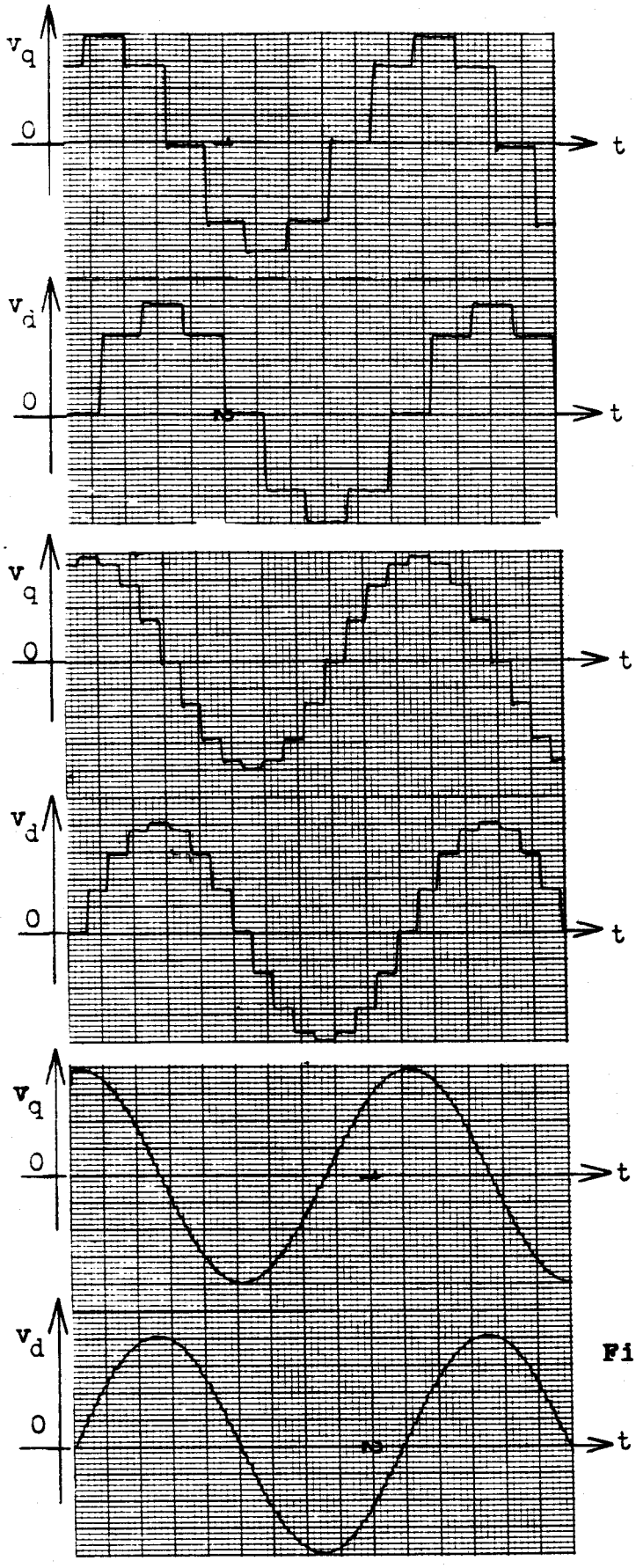
This section presents and discusses the results of the methodology verification tests.

### 4.5.1. Waveforms of the Output Signals

Figure 4-1 shows that the output signals have stepped sinusoidal waveforms. By inspecting the waveforms of Figure 4-1, it can be seen that the number of steps per cycle of each signal equals the number of samples ($N$) per cycle used to generate each signal. Moreover, Figure 4-1 shows that the size of the steps decreases as $N$ increases; and the waveforms become more smooth.

### 4.5.2. Effect of Changing The D/A sampling Frequency

Figure 4-2 displays stepped sine waveforms generated at different D/A clock settings. It can be seen that changing the sampling frequency, hence the intersample time ($T_{sa}$), changes the frequency of the output signals. For constant $N$, the output frequency increases with the D/A sampling frequency, that is, with decreasing $T_{sa}$.




(a) N = 8
$T_{sa}$ = 0.05sec
$f_{da}$ = 2.5Hz
Kv = 2.0

(b) N = 16
$T_{sa}$ = 0.025sec
$f_{da}$ = 2.5Hz
$K_v$ = 2.0

(c) N = 64
$T_{sa}$ = 0.00625sec
$f_{da}$ = 2.5Hz
$K_v$ = 2.0

**Figure 4-1:** Stepped output waveforms of the oscillator.

NOTES. Chart sensitivity:
Vertical - 100mV/div
Horizontal - 125div/sec

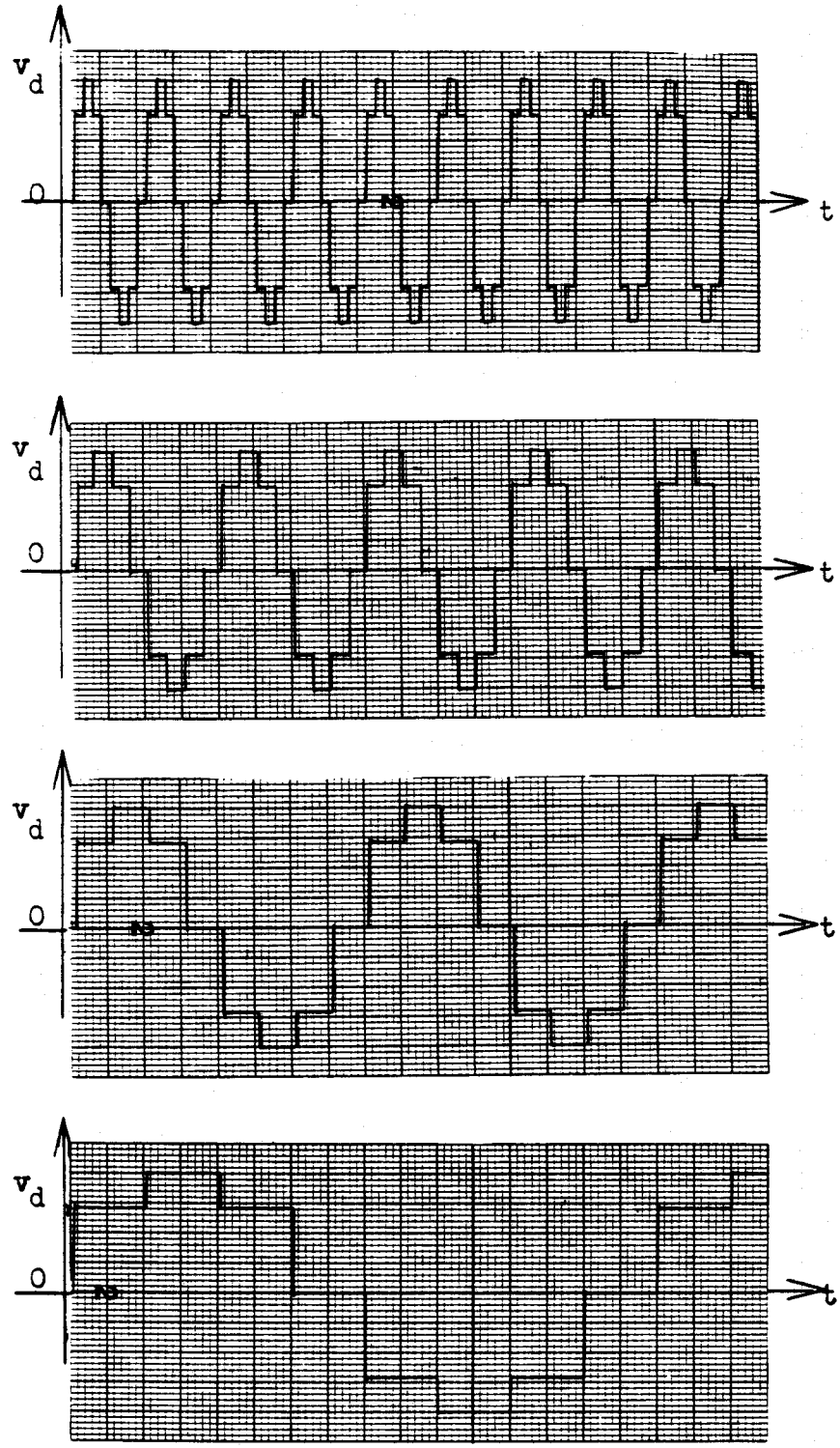



**Figure 4-2:** The effect of varying the clock setting on the output frequency for N = 8 samples/cycle.

NOTES. Chart sensitivity:
Vertical - 100mV/div
Horizontal - 25div/sec

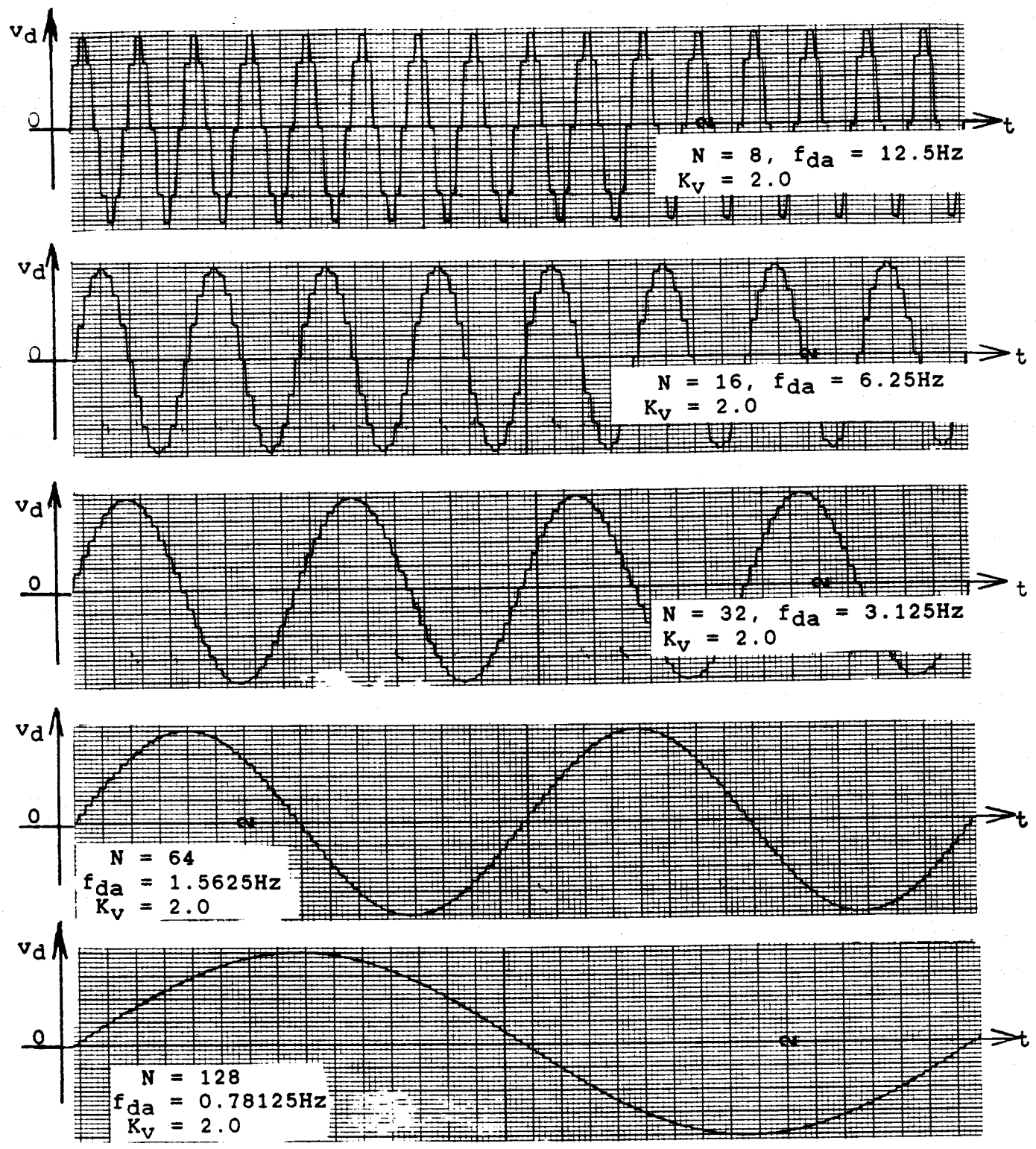
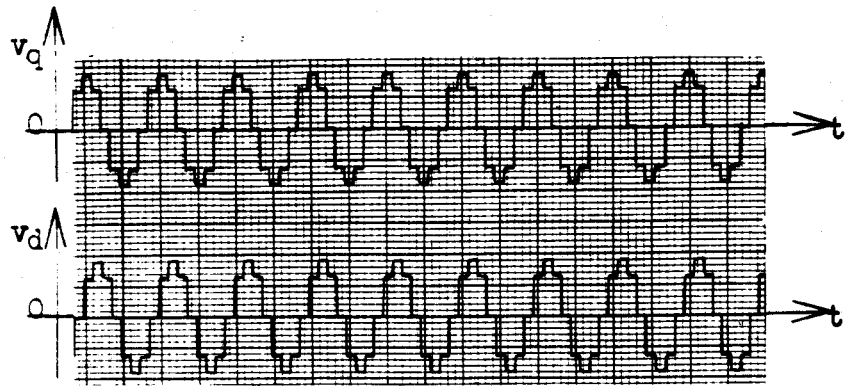
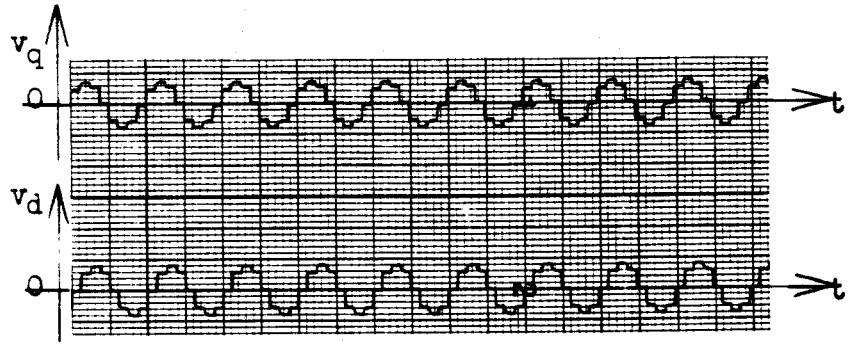



**Figure 4-3:** The effects of varying N at constant D/A sampling frequency of 100Hz.

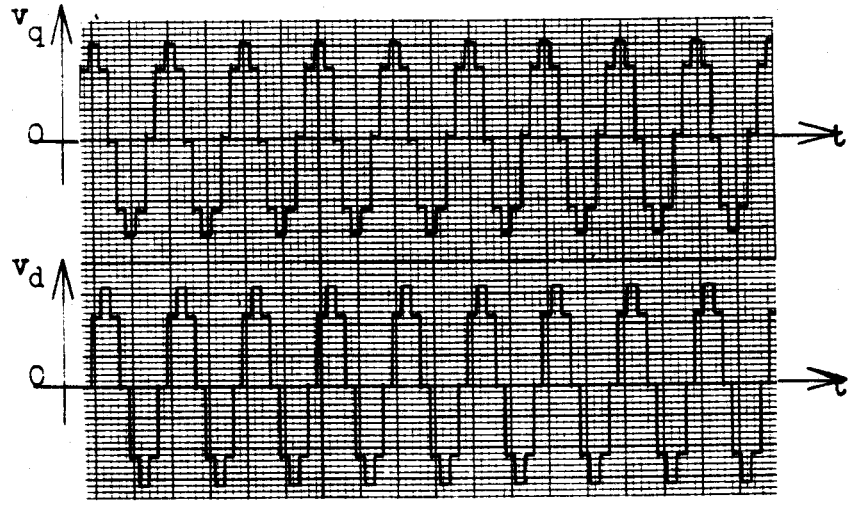
NOTES. Chart sensitivity:
Vertical - 100mV/div.
Horizontal- 125div/sec.




(a) $K_v = 0.9$




(b) $K_v = 0.4$




(c) $K_v = 1.6$

**Figure 4-4:** Oscillator outputs for different $K_v$ settings for $N = 8$, $T_{sa} = 0.01$sec, and $f_{da} = 12.5$Hz.

NOTES. Chart sensitivity:
Vertical - 100mV/div.
Horizontal - 125div/sec.

### 4.5.3. Effect of Varying The Number of Samples Per Cycle

Figure 4-3 shows the effect of changing $N$ for a constant clock setting. The period of the output signals ($=NT_{sa}$) increases with $N$, and hence the decrease in the output frequency. The value of $N$ can only be changed during the initialization process. Therefore, selecting $N$ is equivalent to selecting a frequency range for a fixed range of the clock settings.

### 4.5.4. The Phase Shift Between The Output Signals

The two output signals are approximately 90 degrees phase shifted. The accuracy of the approximation increases with $N$. This can be observed in Figure 4-1, on which a consistent time delay equal to half the intersample time can be seen. This delay is also discussed as the phase delay angle (PDA) in section 4.6. Furthermore, a circular lissajous figure is observable on a CRT (in the X-Y mode). This indicates that the 90 degrees phase shift between the output signals can be achieved even before filtering.

### 4.5.5. Amplitude Adjustment

Figure 4-4 shows that the digital oscillator, as discussed in Chapter 2, has the ability to adjust the peak amplitudes of the two output signals to be equal at any instant of time.

### 4.5.6. Frequency Adjustment

Figures 4-1 and 4-2 show that the oscillator sampling control can adjust the frequencies of the two output signals to be equal, as $N$ and $T_{sa}$ are varied.

## 4.6. Analysis of The Output Signals

Harmonic analysis by Discrete-time Fourier Transform (DFT) was performed for the quality assessment of the output signals using the data derived from normalized (unit-amplitude) output signals. Two indicators were used to assess the quality of the signals:

1. the voltage distortion factor (VDF), defined as the ratio of the power contributed by the harmonics (2nd order and higher) to the power contributed by the fundamental, and

2. the phase delay angle (PDA), defined as the phase delay of the fundamental from the actual stepped sinusoidal signal (see also section 4.6.2).

Both VDF and PDA equals zero when the number of steps per cycle of each signal is infinite.

### 4.6.1. Generation of Data for Analysis

The quality of the analog signals depends on the actual digital values in the D/A buffers, and the digital-to-analog converter hardware. Two ways can be used to obtain data for analysis. First, is by resampling the output signals. This method can introduce more noise to the data or cause aliasing; also the method is limited by the sampling rates of the analog-to-digital converter hardware.

The second method is by generating the data numerically. This method was found to be the best. The reason is that the actual digital data used to generate the signals are known and available (stored in the D/A buffers). The data for analysis was obtained from the available data by digitally representing the response of the digital-to-analog converter to each sample $v[n]$. This approach inherently avoids the data reconstruction problems [25, 26, 27, 24, 28, 29] caused by sampling at insufficient rates.

### 4.6.2. Representation of The Response of The Digital-to-Analog Converter to a Digital Word

The D/A register in Figure 4-5(a) stores the input digital word $v[n]$ in the time interval $nT_{sa} \leq t < (n+1)T_{sa}$. Within this time interval, the ports of the D/A register are held at constant levels. These levels drive the converter to output an analog step [29, 32, 33] as illustrated in Figure 4-5(b). The holding action of the register lasts for a time duration equal to the acquisition time $T_{sa}$ of each sample. The value of this time is given by the reciprocal of the D/A sampling frequency per signal, $f_{sa}$.

Figure 4-6(a) shows a digital sine sequence with 8 samples per cycle input to the D/A converter via the D/A register. Figure 4-6(b) illustrates the stepped sine output of the converter. It can be seen from Figure 4-6(b) that, for each sample $v[n]$, an infinite number of equal valued samples as $v[n]$ are required to represent the analog time step $T_{sa}$ in digital form.

The harmonic analysis [9, 28] depends on $N$, the number of samples per cycle, and is independent of the intersample time $T_{sa}$. Due to this ef-

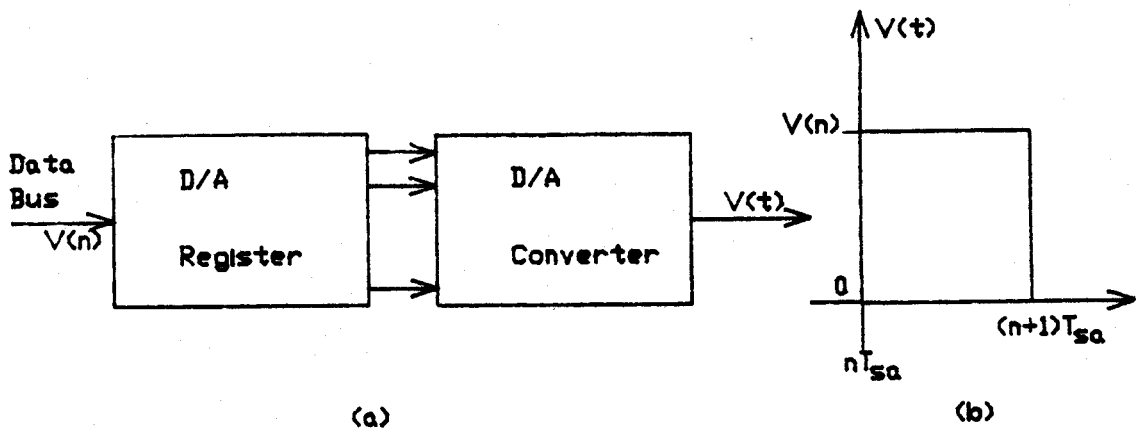
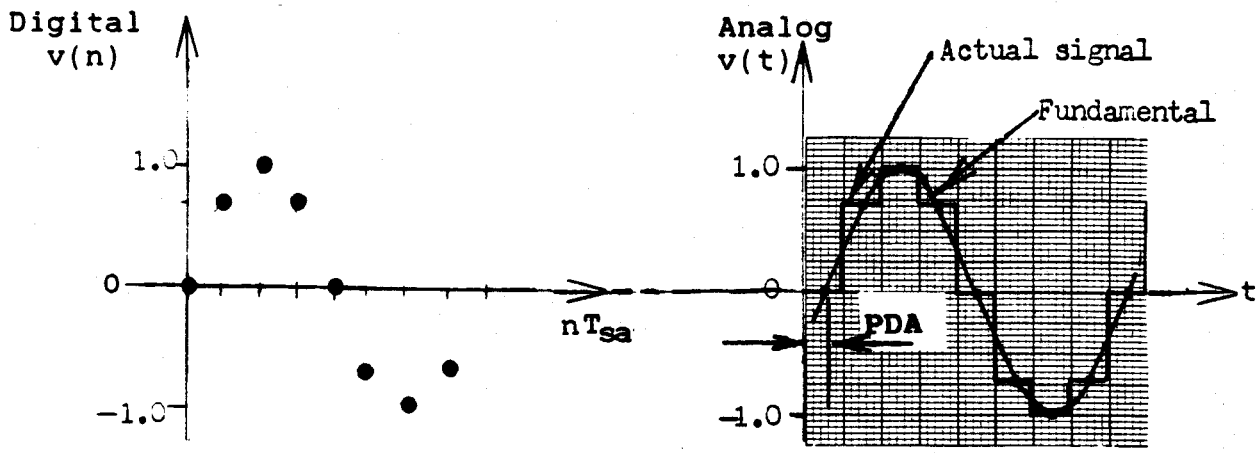



**Figure 4-5:** (a) A digital-to-analog (D/A) converter interfaced to a data bus via a parallel data port (D/A register), (b) The response of the D/A converter to a digital input $v[n]$.

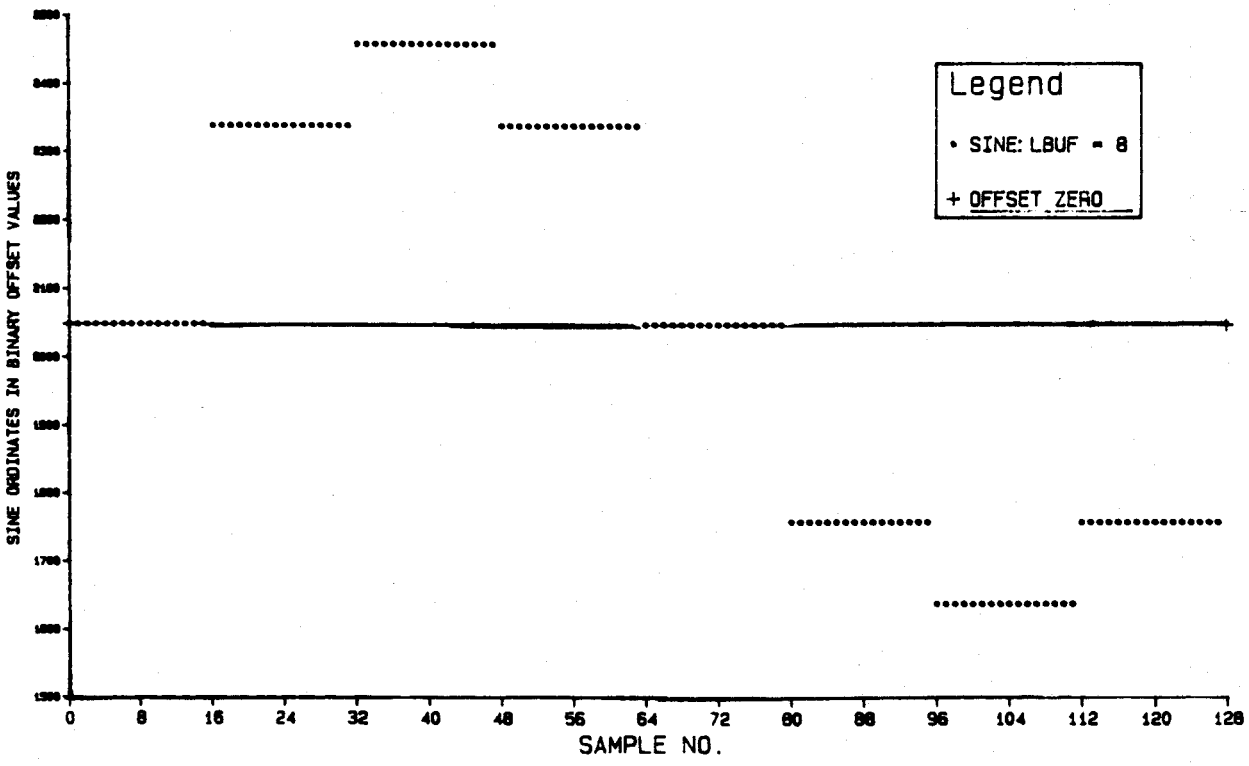
fect, the DFT formula was modified to accommodate the register holding action (details are given in Appendix C). The time step of length $T_{sa}$ was subdivided into $M_h$ substeps such that $N$ samples per cycle in a D/A buffer give $NM_h$ samples per cycle for the analysis. Figure 4-6(c) shows the representation of $T_{sa}$ using $M_h$=16 substeps for $N = 8$ ($NM_h$=128).

Figures 4-7 and 4-8 show the voltage distortion factor and the phase delay angle varied with $M_h$ for $N$ equal to 8 samples per cycle. It can be seen that, for $M_h \geq 32$, the distortion factor and the phase delay angle have approximately a constant value. This means that a sufficient representation of the holding action (or $T_{sa}$) is possible for $M_h \geq 32$.




(a) Input to the D/A converter.

(b) Output from a D/A converter.




(c) $T_{sa}$ is subdivided into $M_h$ = 16 divisions.

**Figure 4-6:** Digital representation of the response of a D/A converter to a digital sample.

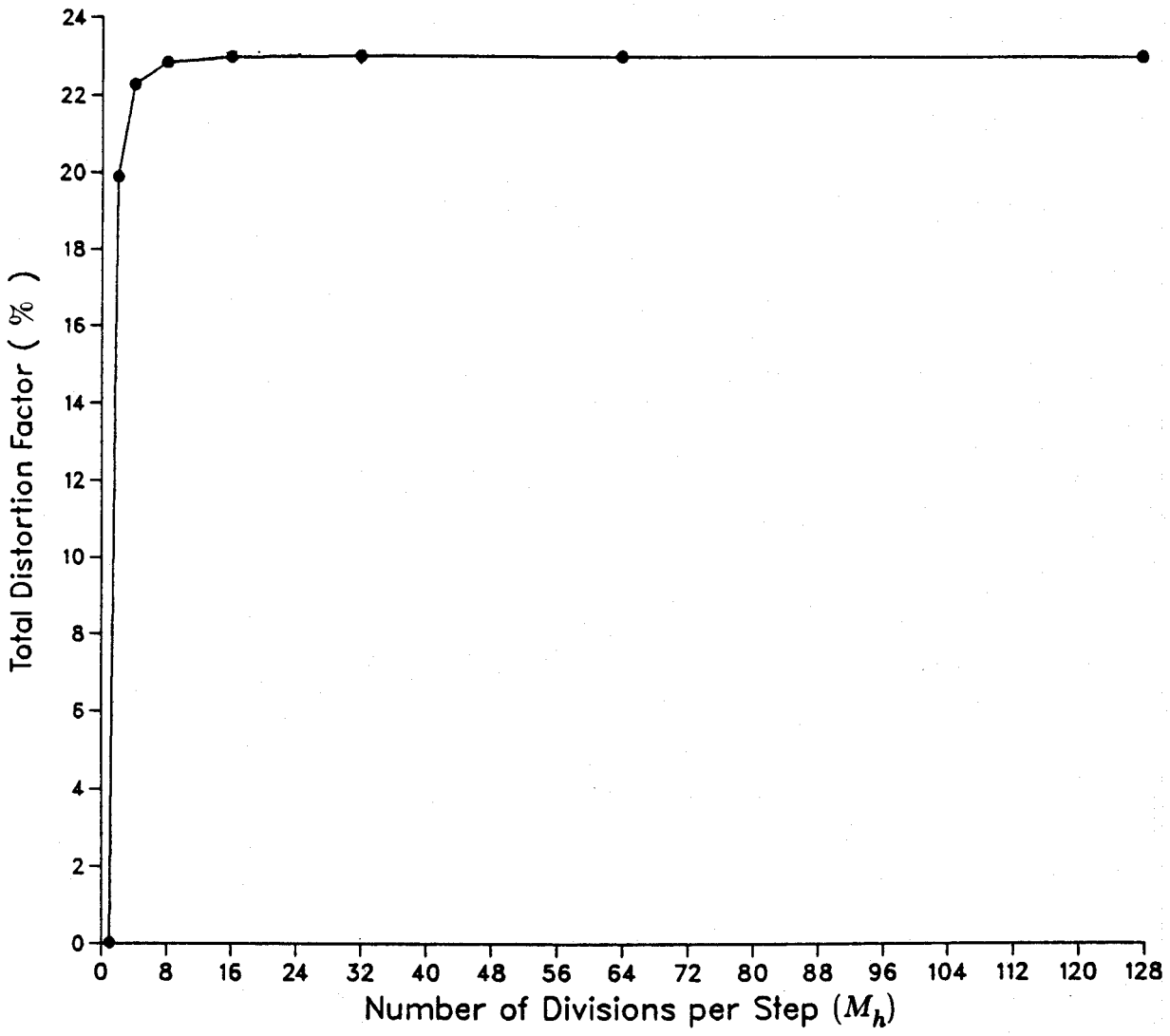



**Figure 4-7:** The total distortion of the output signals for $N = 8$ samples per cycle as a function of the number of subdivisions per step $(M_h)$.

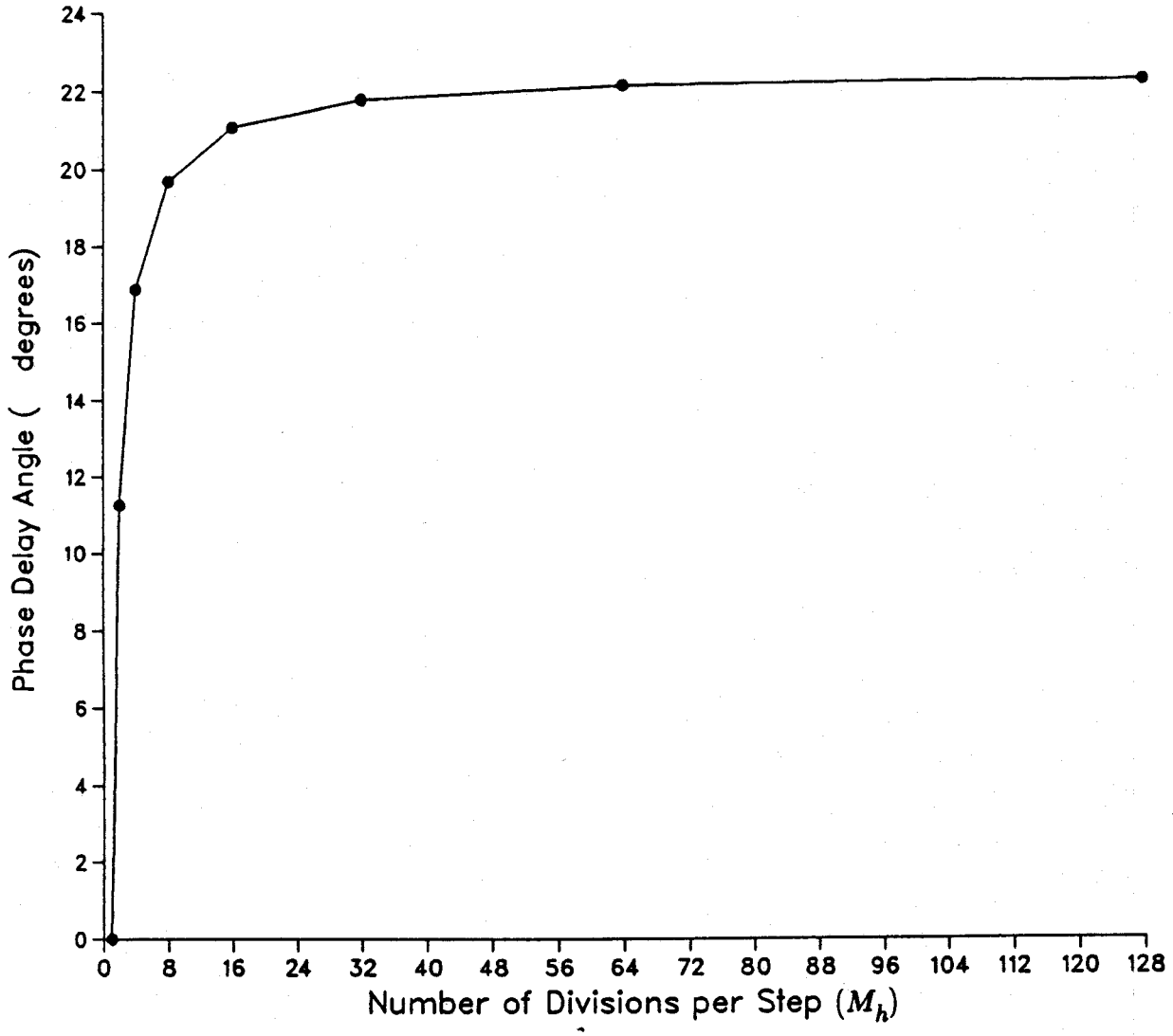



**Figure 4-8:** The phase delay angle for $N = 8$ as a function of the number of subdivisions per step ($M_h$).

The simulation value of at least 32 subdivisions per step ($T_{sa}$) implies that accurate data for analysing the output signals can be obtained by resampling the output signals at rates greater or equal to 32 times the signal frequency.

### 4.6.3. Analysis Results

This section presents the results on the indicators of the quality of the output signals at steady state. The findings can be summarized as follows.

#### 4.6.3.1. Harmonic Content

Figures 4-9 to 4-12 illustrate the harmonic content of the signals generated by using $N$ = 8, 16, 32, and 64. Besides the fundamental, harmonics present in each signal at any instant of time can be identified by the expression:

$$(mN \pm 1)f_{da} \tag{4.1}$$

where: $f_{da}$ - is the fundamental frequency of the output signals,
$N$ - is the number of digital samples/cycle of signal (loaded in the D/A buffers), and
$m$ - is a positive integer (=1,2,3, ..., )

#### 4.6.3.2. Waveform Distortion

Figures 4-13 and 4-14 display the variation of the voltage distortion factor (VDF) as a function of $N$. Figure 4-14 is plotted on a logarithmic scale. The relationship between VDF and $N$ was found to be:

$$VDF\% = \frac{180.0}{N} \tag{4.2}$$

It can be seen from Figures 4-13 and 4-14 that choosing $N \geq 200$ samples per cycle, gives a distortion factor of less than one percent.

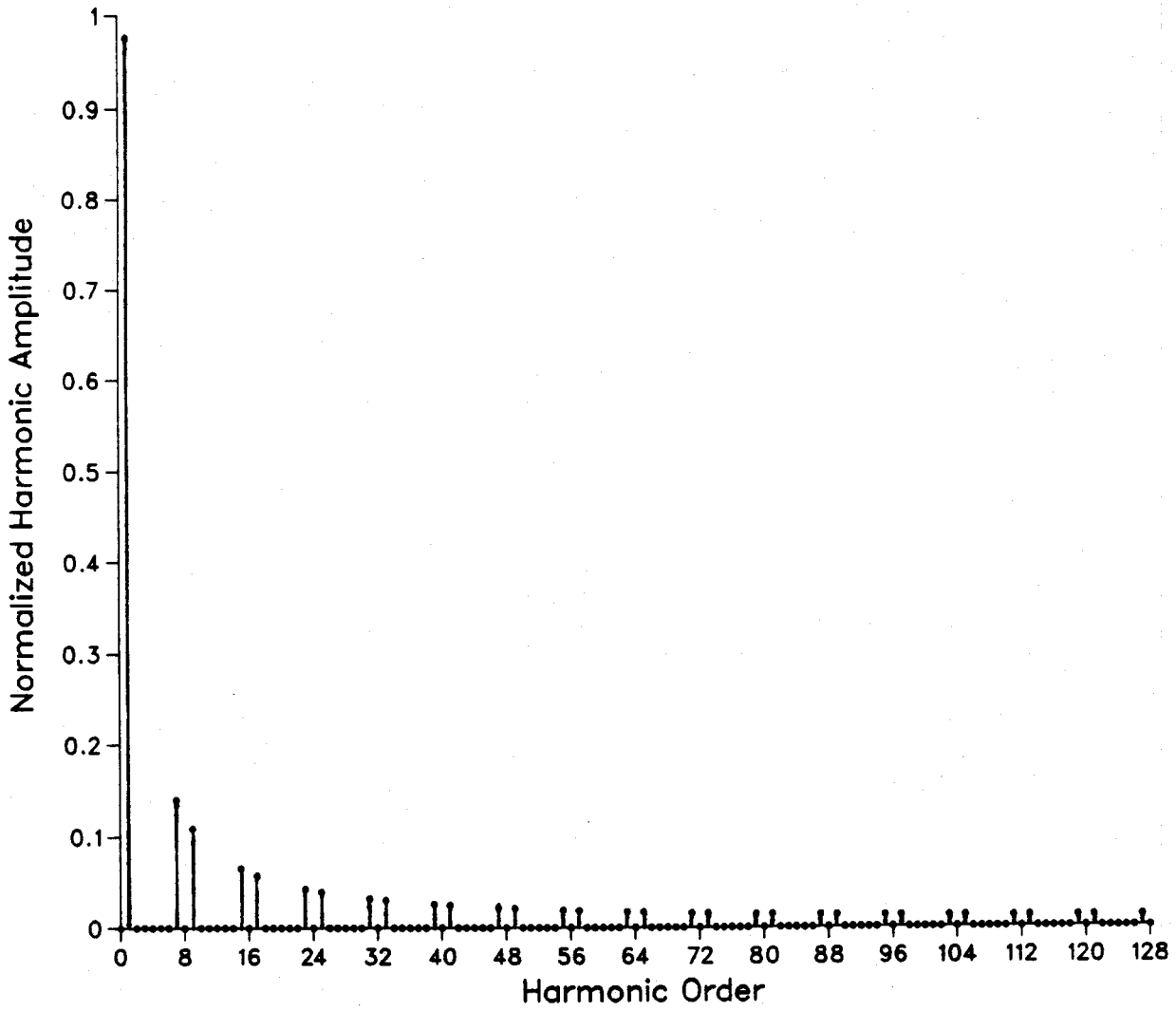



**Figure 4-9:** The harmonic spectrum of the output signals for $N = 8$, computed for $M_h = 32$ subdivisions/step.

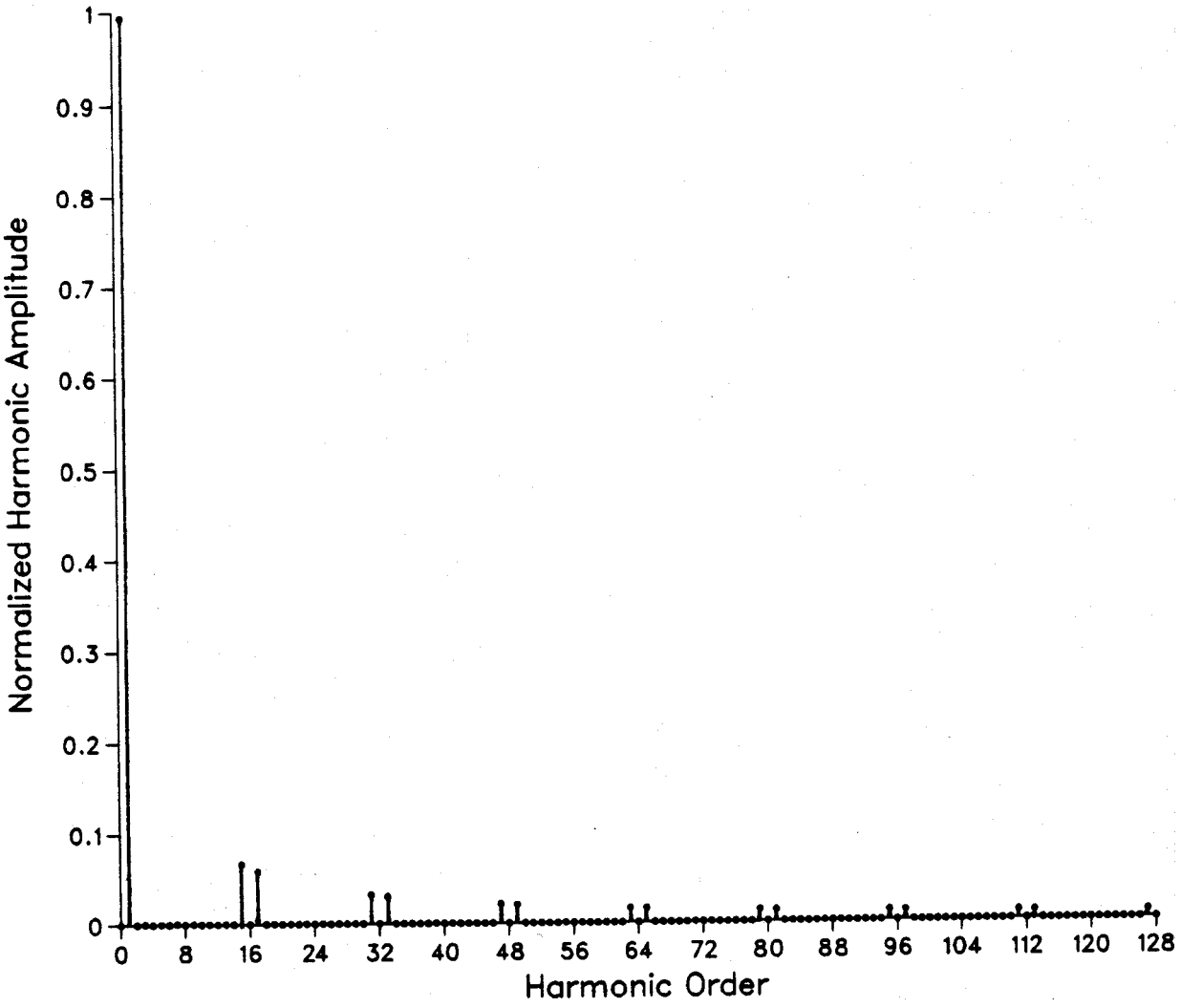



**Figure 4-10:** The harmonic spectrum of the output signals for $N = 16$, computed for $M_h = 32$ subdivisions/step.

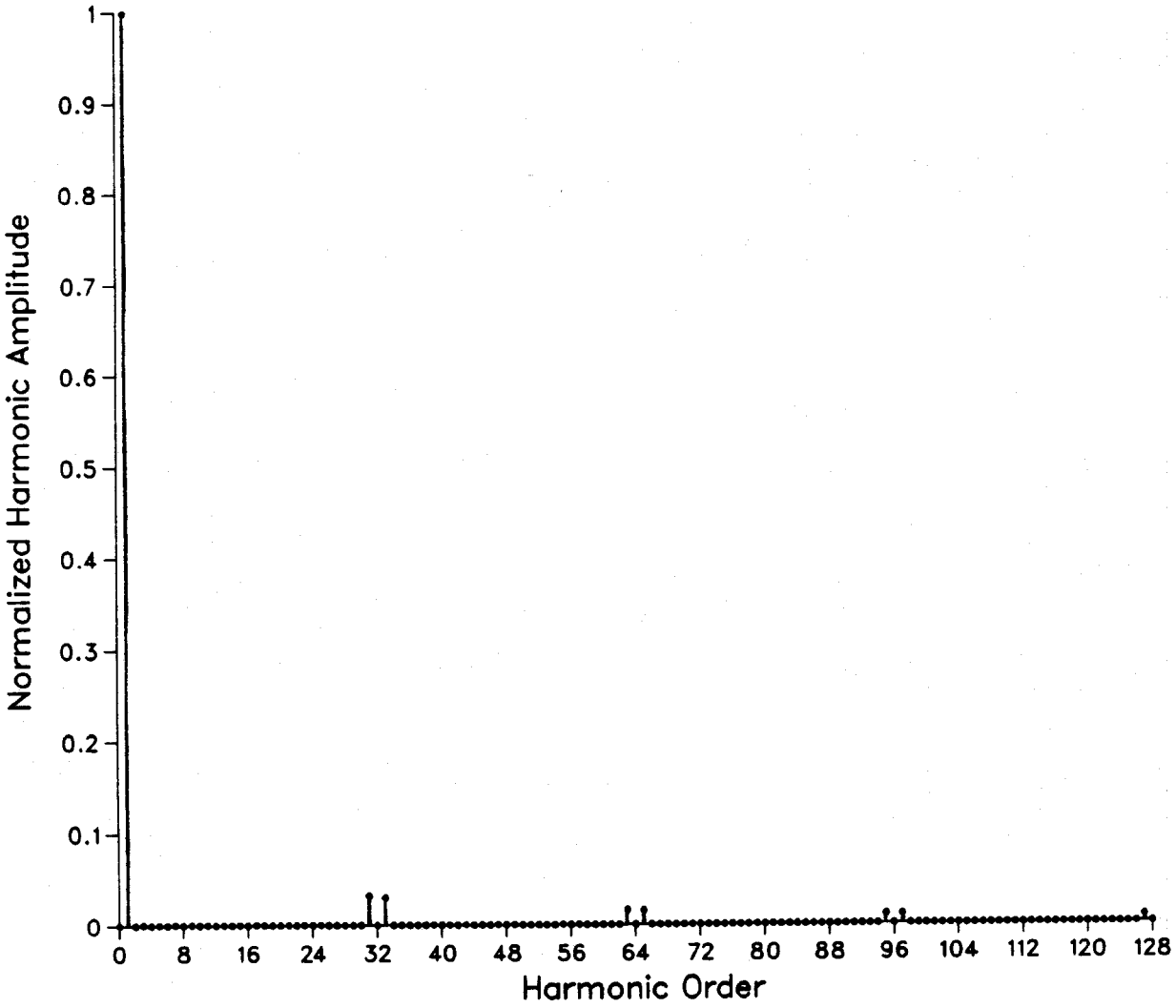



**Figure 4-11:** The harmonic spectrum of the output signals for $N = 32$, computed for $M_h = 32$ subdivisions/step.

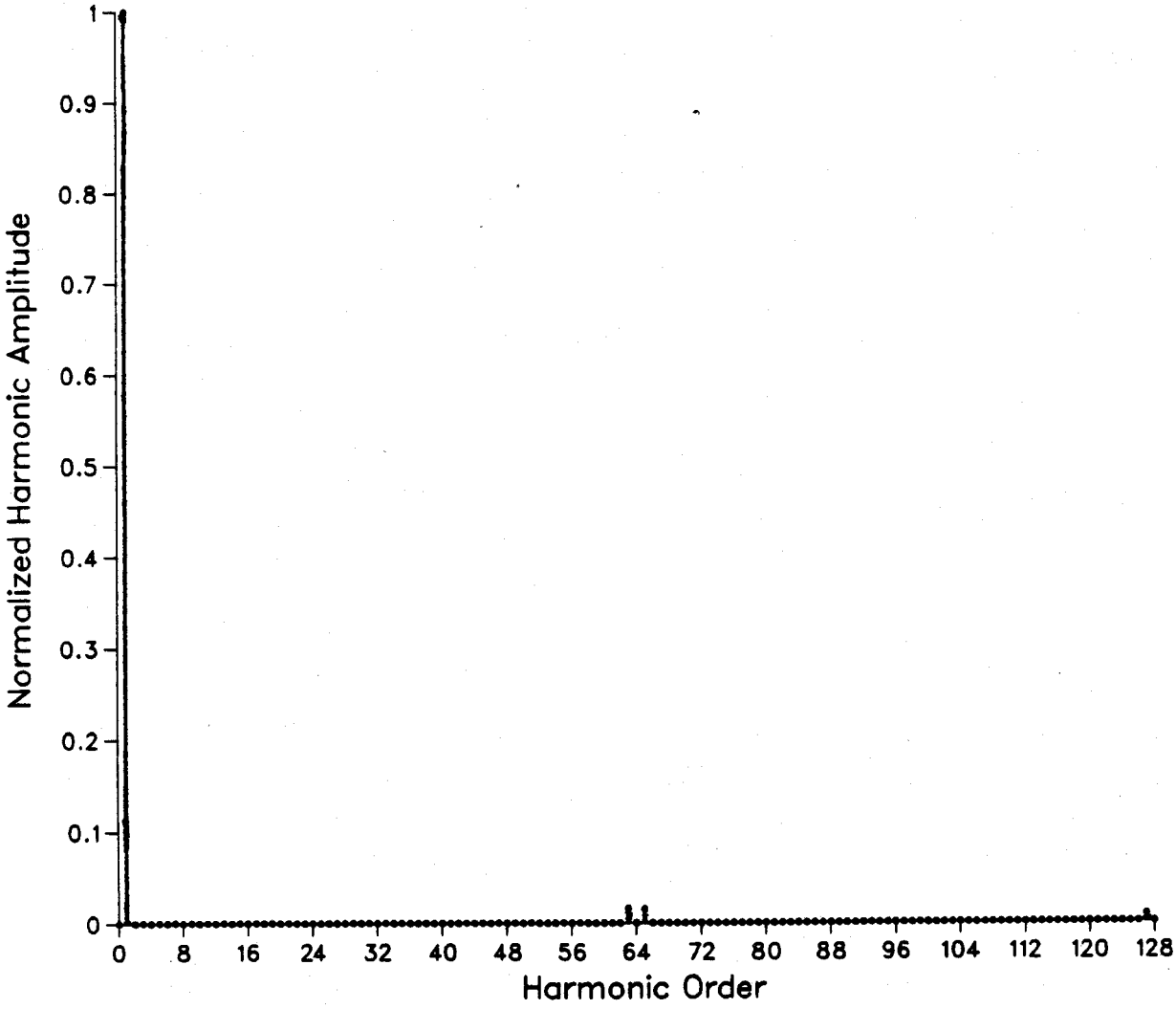



**Figure 4-12:** The harmonic spectrum of the output signals for $N = 64$, computed for $M_h = 32$ subdivisions/step.

#### 4.6.3.3. The Phase Delay Angle

The dependency of the phase delay angle (PDA) on $N$ is illustrated in Figures 4-15 and 4-16. It can be seen from the graphs that the PDA varies with $N$ in a decaying hyperbolic relation:

$$PDA\ (degrees) = \frac{180.0}{N} \tag{4.3}$$

The value of PDA is less than one degree for $N \geq 200$ samples per cycle.

#### 4.6.3.4. Selection of The Digital-to-Analog Converter

The proper size of a D/A converter can be selected on the basis of the voltage distortion factor or the phase delay angle. First, the value of $N$ is selected. Then, the size of the converter in terms of number of bits B, can be determined from the value of $N$ by the relation:

$$B = \frac{\log_{10} N}{\log_{10} 2} \tag{4.4}$$

For example an 8-bit D/A converter is adequate for $N = 200$ samples per cycle.

## 4.7. Performance of the Digital Oscillator

The performance of the oscillator is such that what happens to the sine output signal also happens to the cosine output signal. Therefore, either of these two signals represents the oscillator performance. In the following sections, the sine output signal is used to show the performance of the oscillator.

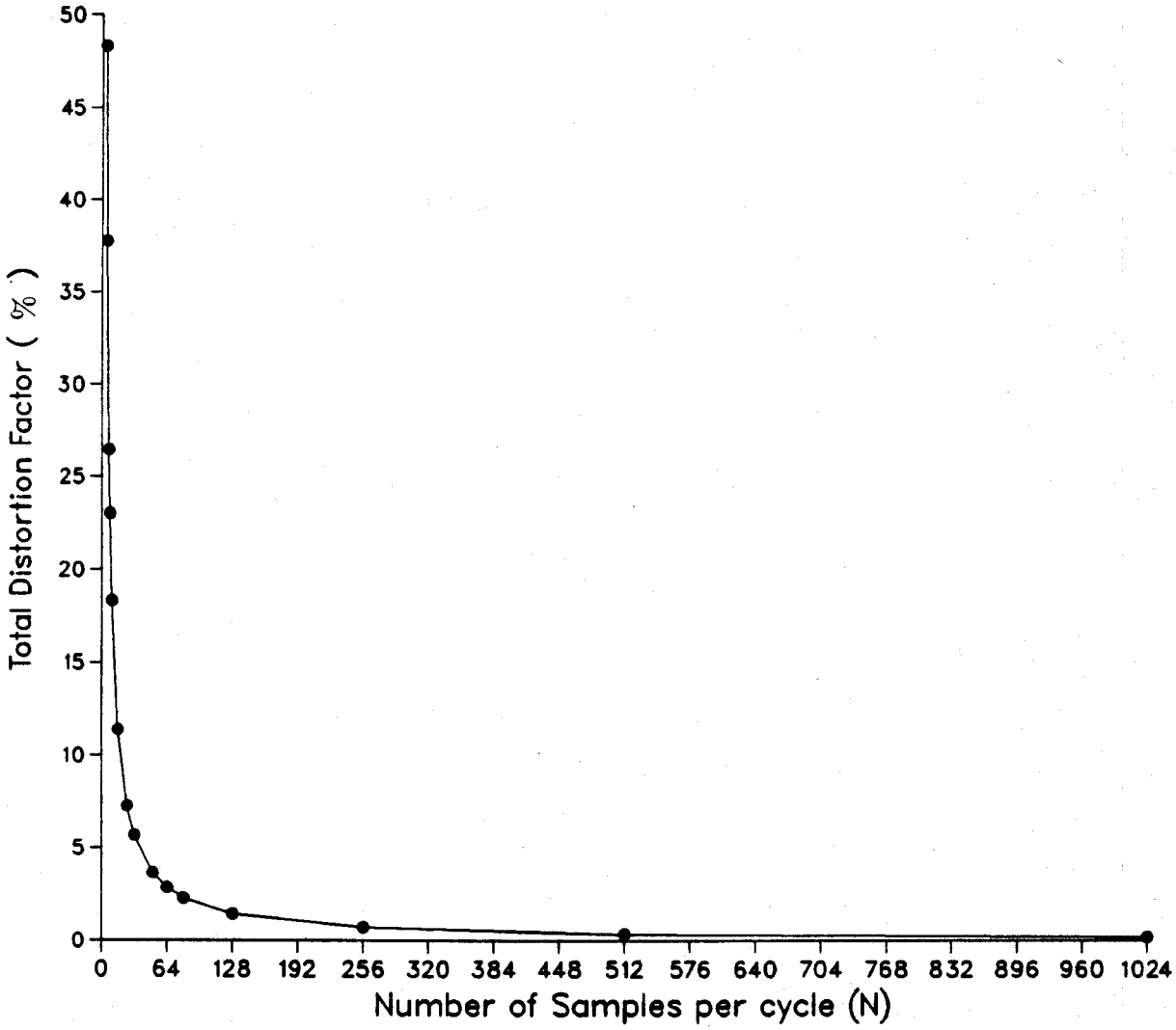



**Figure 4-13:** The variation of the total distortion factor (VDF) with the number of samples per cycle ($N$) for $M_h = 32$ subdivisions/step.

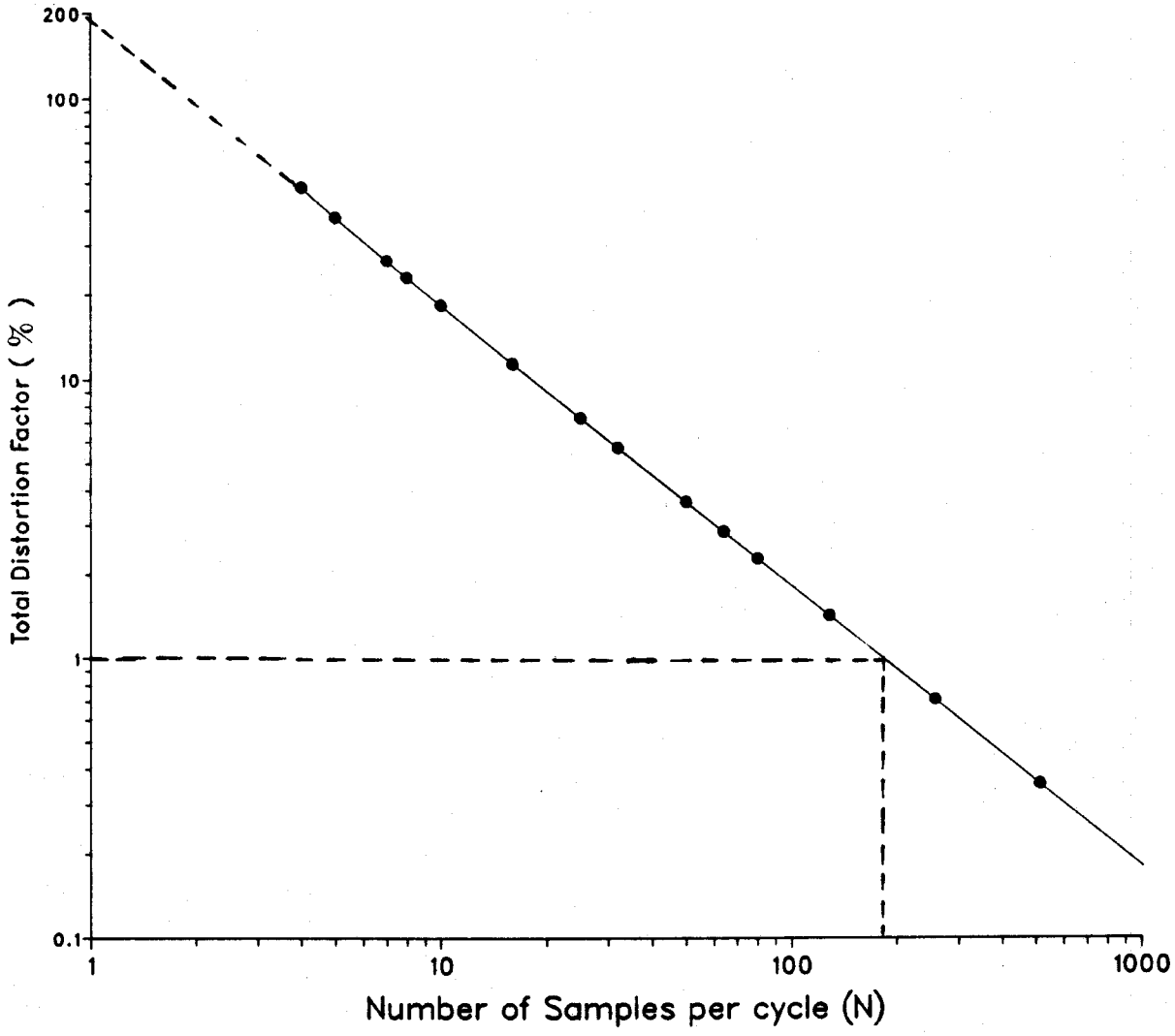



**Figure 4-14:** The variation of the total distortion factor (VDF) with the number of samples per cycle ($N$) for $M_h = 32$ subdivisions/step (on a log-log scale).

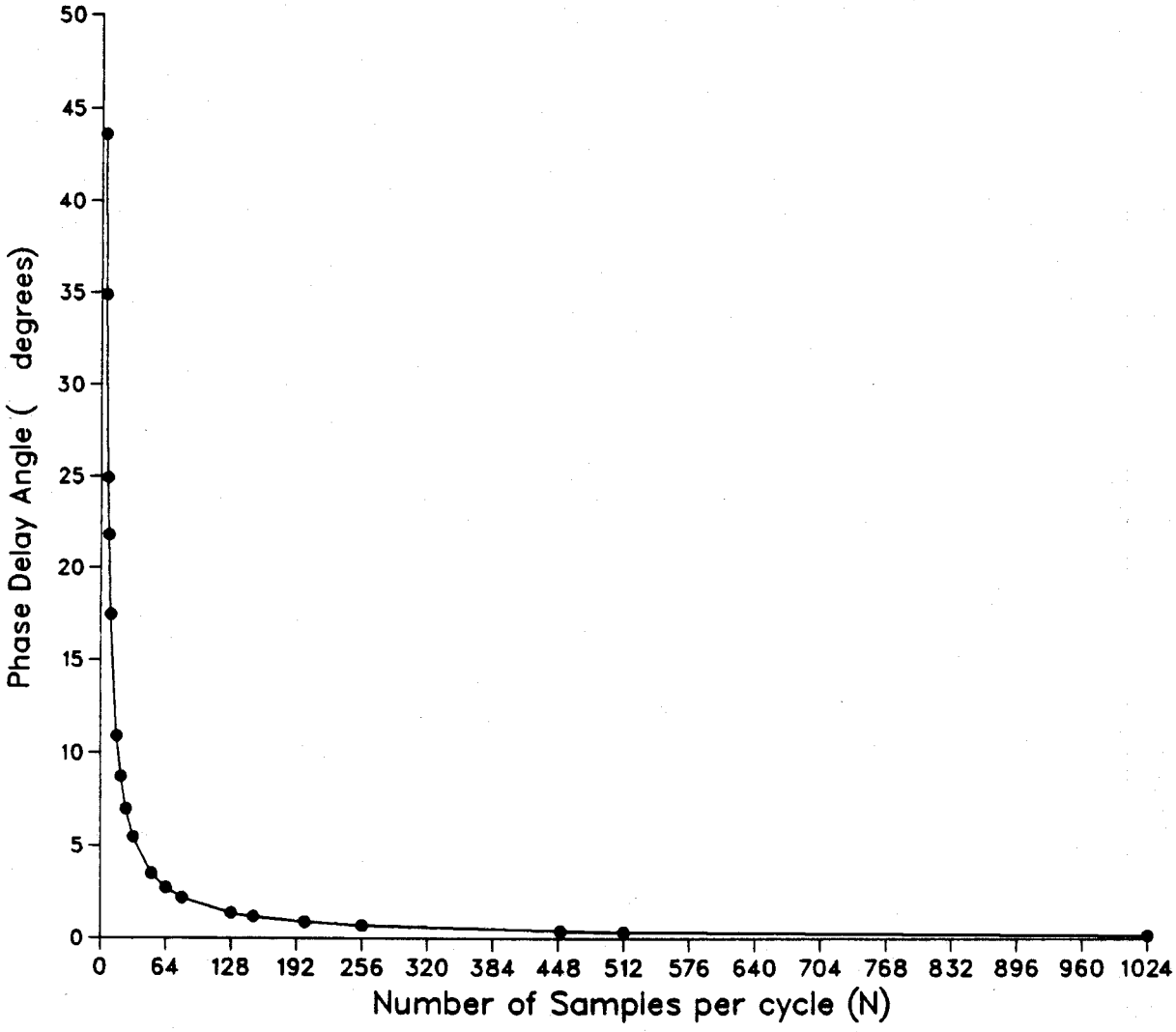



**Figure 4-15:** The variation of the phase delay angle (PDA) with the number of samples per cycle ($N$) for $M_h = 32$ subdivisions/step.

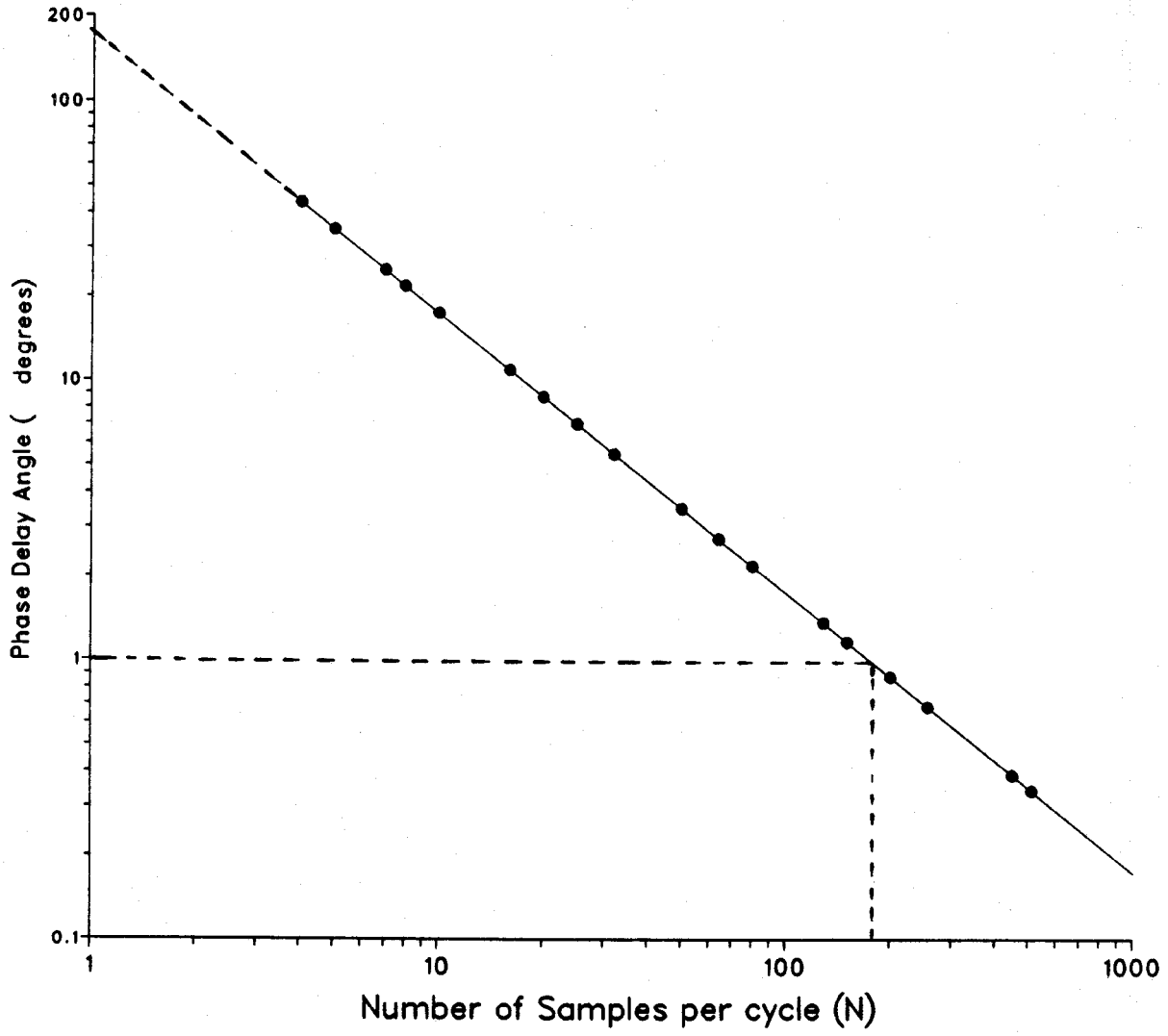



**Figure 4-16:** The variation of the phase delay angle (PDA) with the number of samples per cycle ($N$) for $M_h = 32$ subdivisions per step (on a log-log scale).

### 4.7.1. Amplitude Modulation

Figures 4-17 to 4-20 show the sine outputs of the oscillator at a constant frequency, and amplitude modulated by a voltage error signal of different waveforms. Positive-amplitude modulation is evident from Figure 4-17, and negative-amplitude modulation is shown in Figure 4-18. Figures 4-19 and 4-20 emphasize the ability of the oscillator to respond to different waveforms of the voltage error signal.

### 4.7.2. Frequency Modulation

Figures 4-21 to 4-23 depict the oscillator sine output at constant amplitude, and frequency modulated by a slip signal of different waveforms. For the inputs shown, the dynamic response of the oscillator is deemed adequate. However, it should be noted that, a high frequency input signal can not modulate a low frequency output signal [31]. Indeed, frequency modulation is difficult when the frequency of the modulating signal is comparable to that of the output.

### 4.7.3. Amplitude and Frequency Modulation

Figures 4-24 to 4-26 show that the oscillator has the ability to perform both the amplitude and the frequency modulation at the same time. This means, the oscillator generates variable-frequency variable-amplitude signals. Figures 4-19 to 4-26 show that the oscillator performs the best when relatively low frequency (0.01Hz) modulating signals are used.

However, output signals of low frequency were chosen so that they could be plotted. Figure 4-24 and 4-25 show the positive-modulation, and

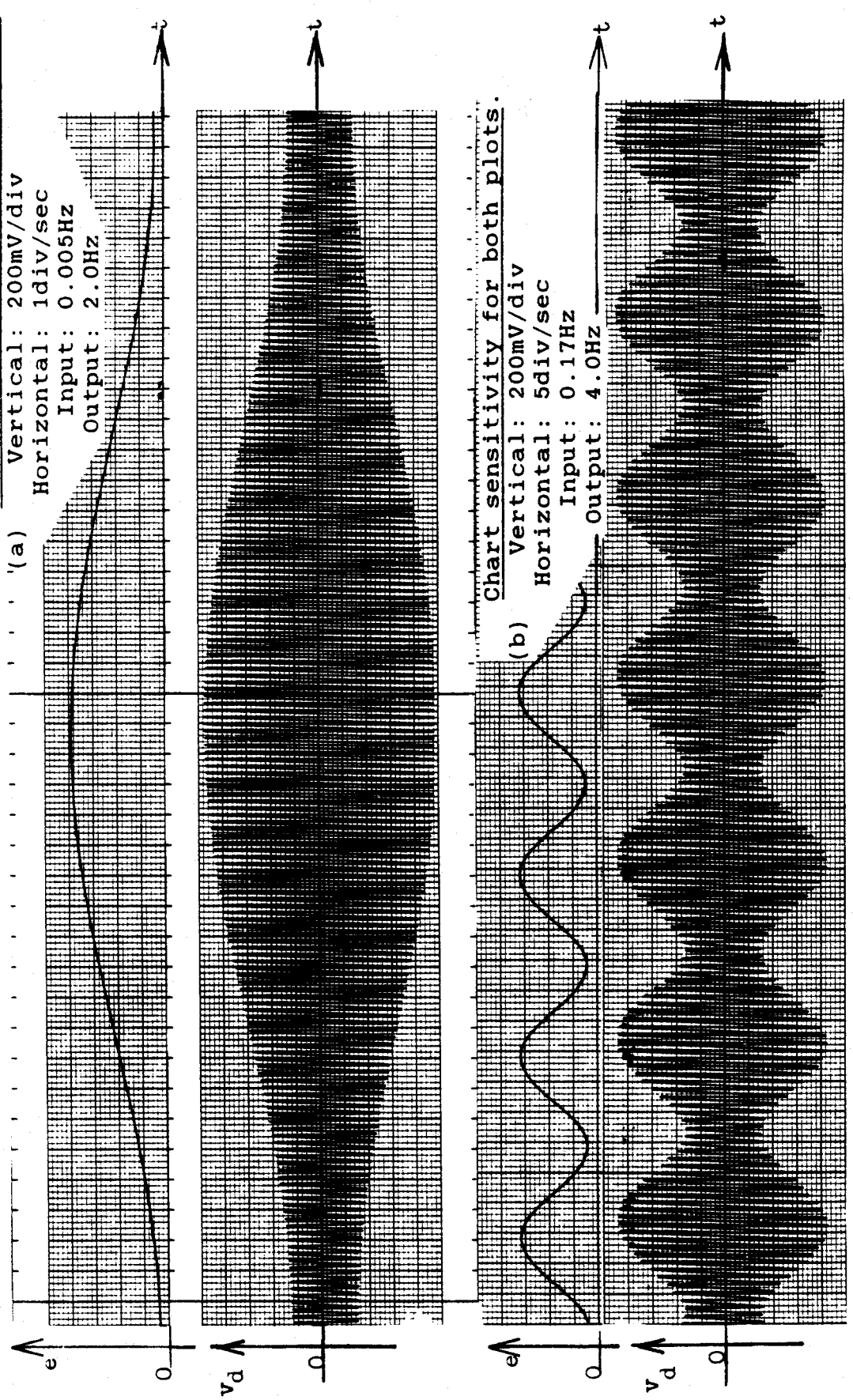



**Figure 4-17:** Positive-amplitude modulation.

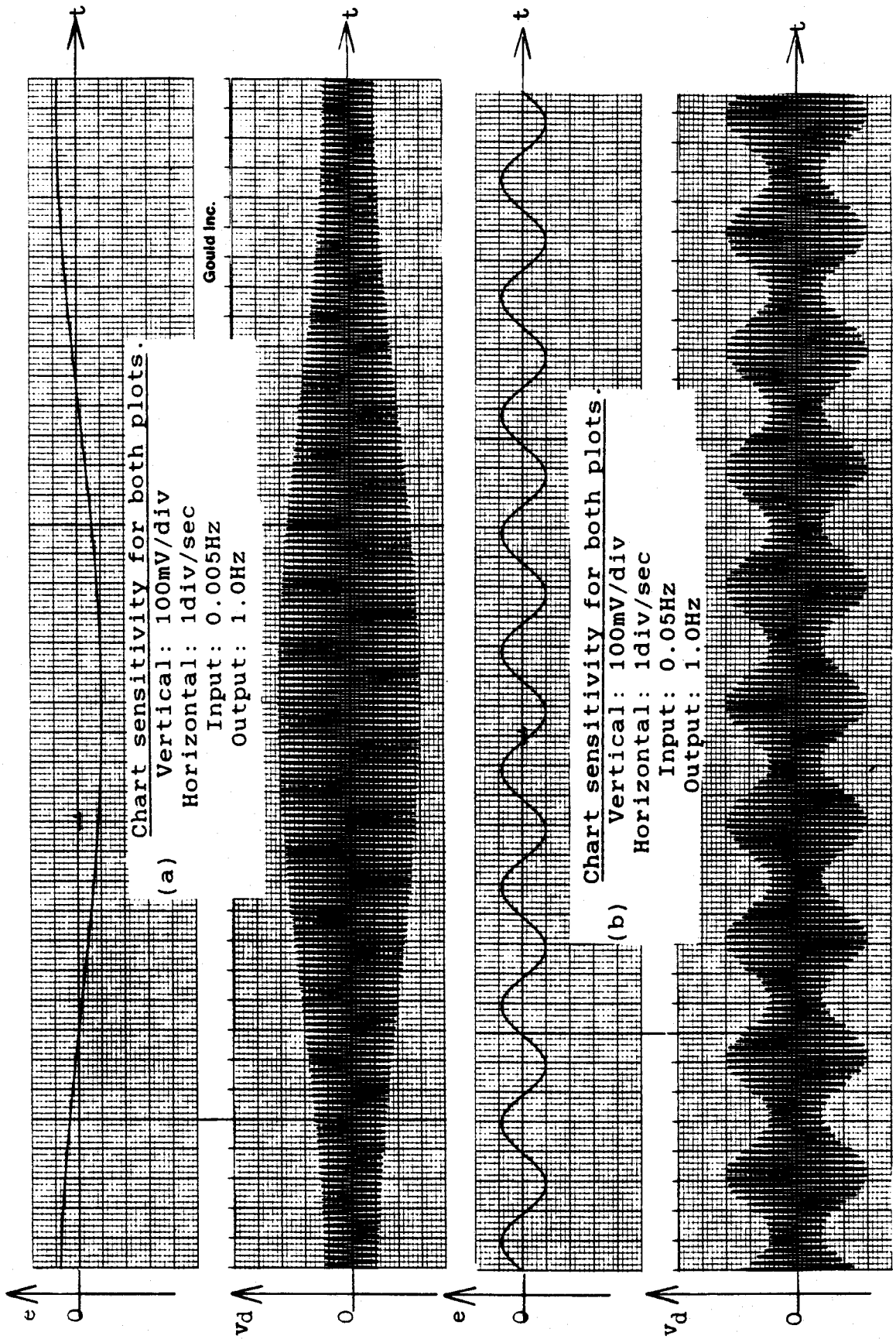
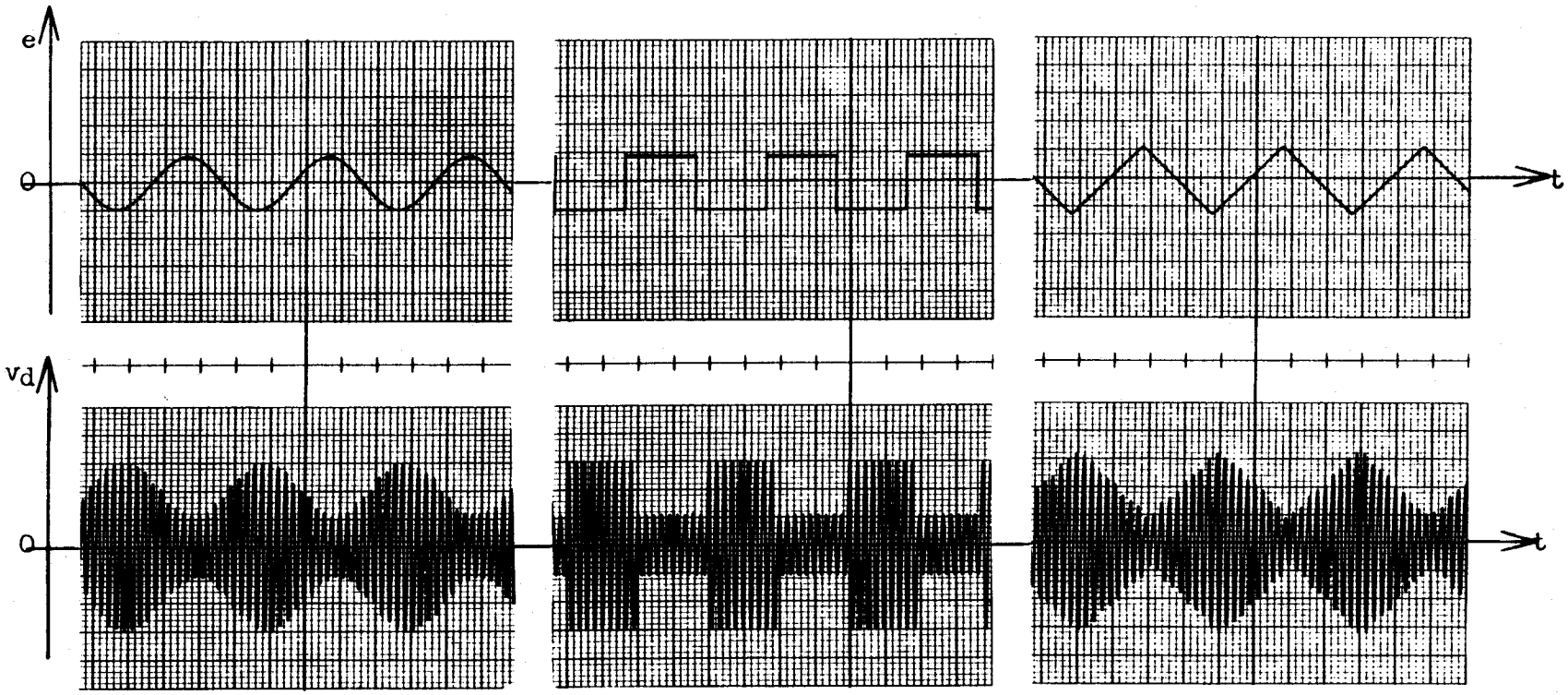



**Figure 4-18:** Negative-amplitude modulation.




(a) e(t) is a sinusoidal wave. (b) e(t) is a square wave. (c) e(t) is a triangular wave.

**Figure 4-19:** Negative-amplitude modulation for different waveforms of a 0.05Hz voltage error signal.

NOTES. Chart sensitivity for all plots:-
Vertical: 100mV/div
Horizontal: 1div/sec

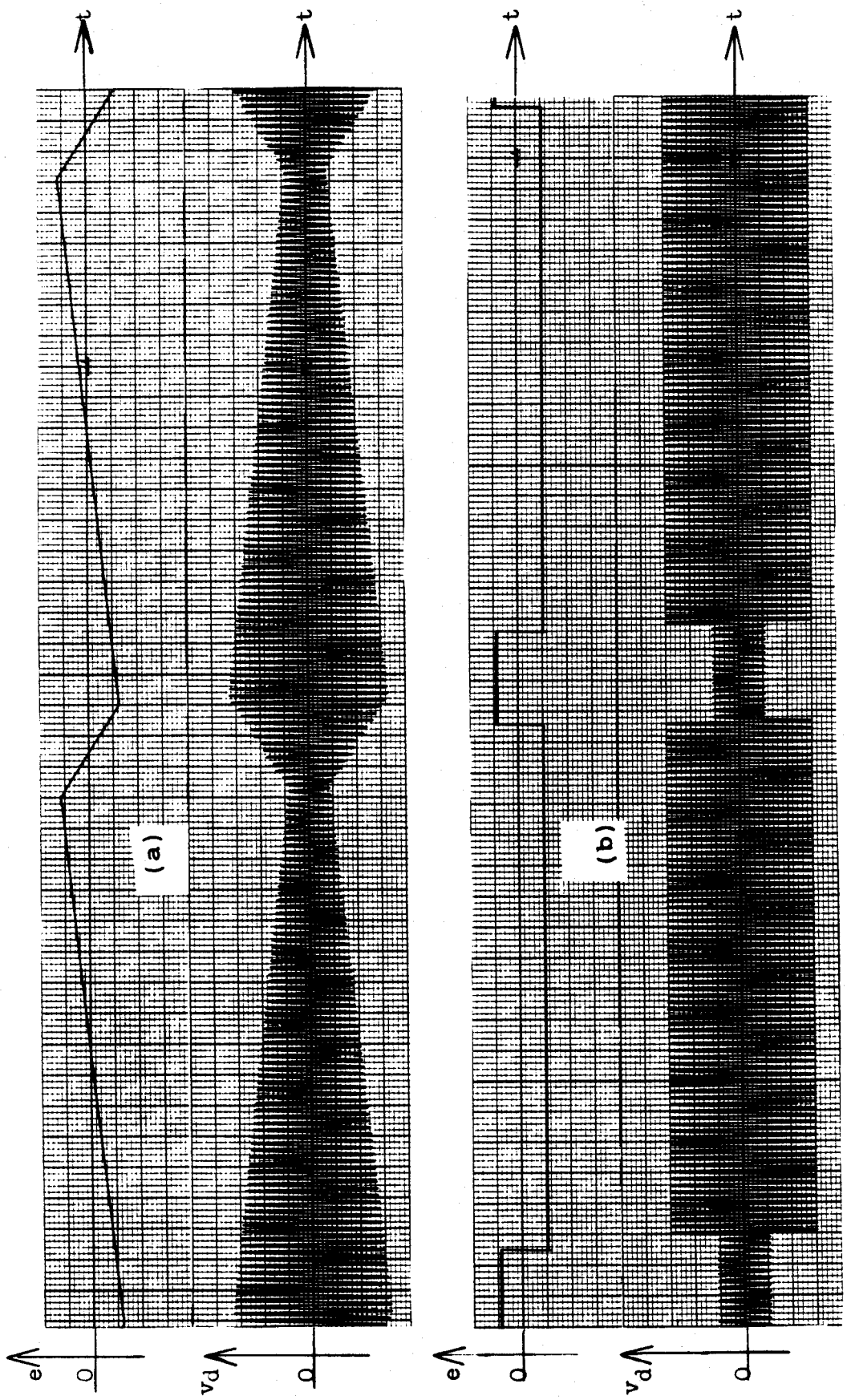



**Figure 4-20:** Negative-amplitude modulation of a 1.0Hz sine wave by a 0.01Hz voltage error signal as a (a) positive ramp, and (b) a pulse signal.

NOTES. Chart sensitivity for all plots:
Vertical - 100mV/div
Horizontal - 1 div/sec.

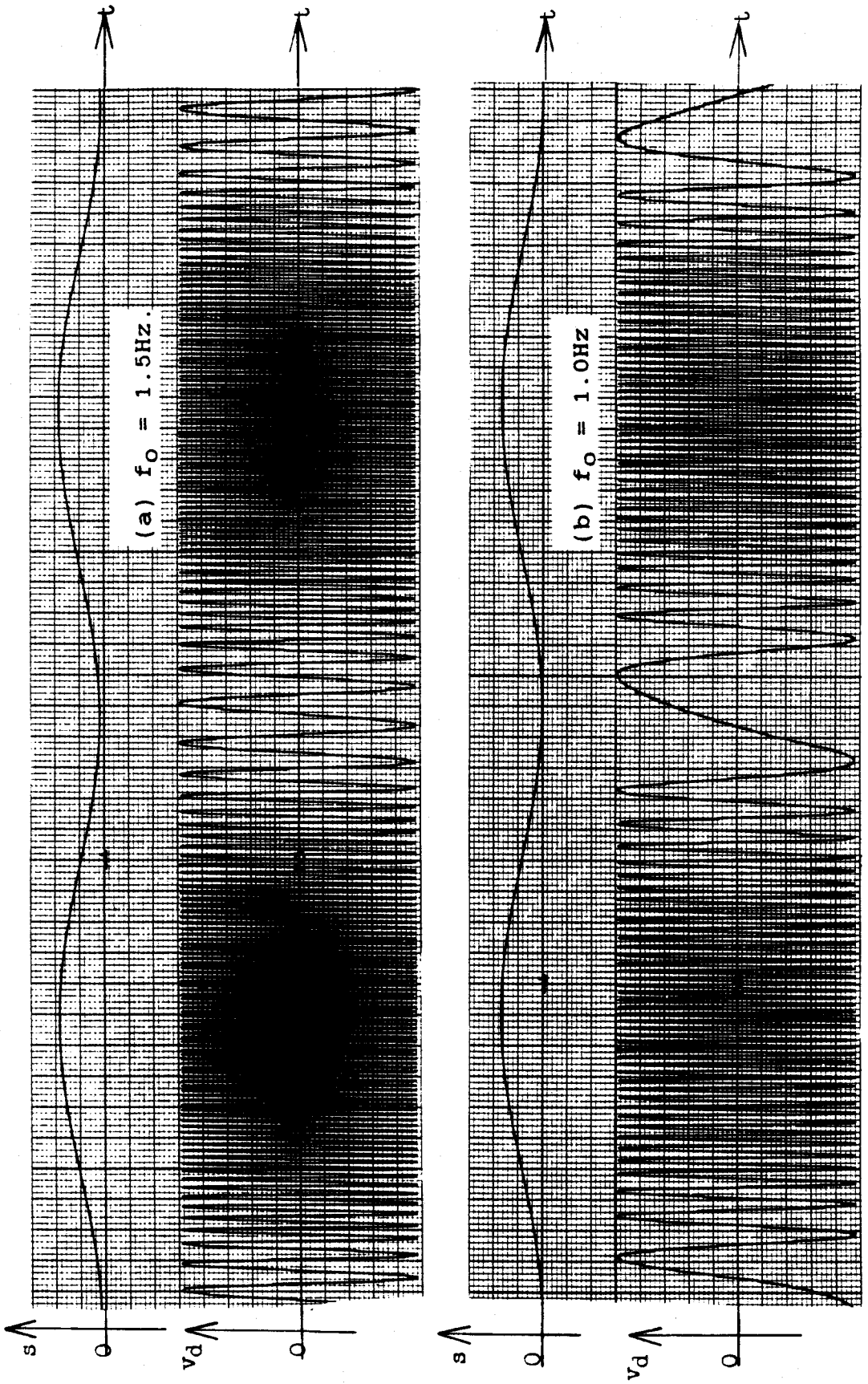
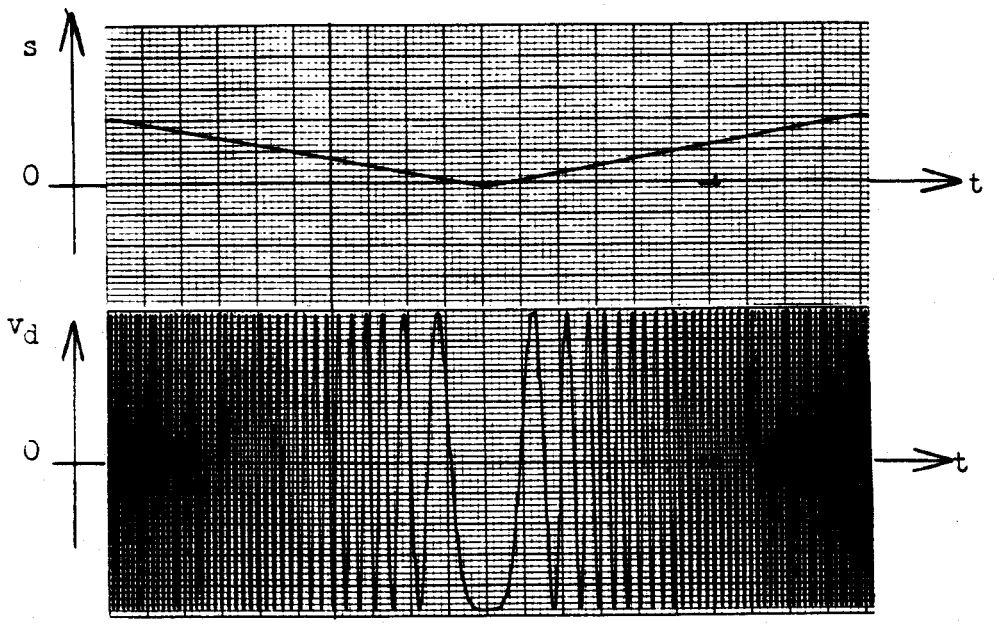
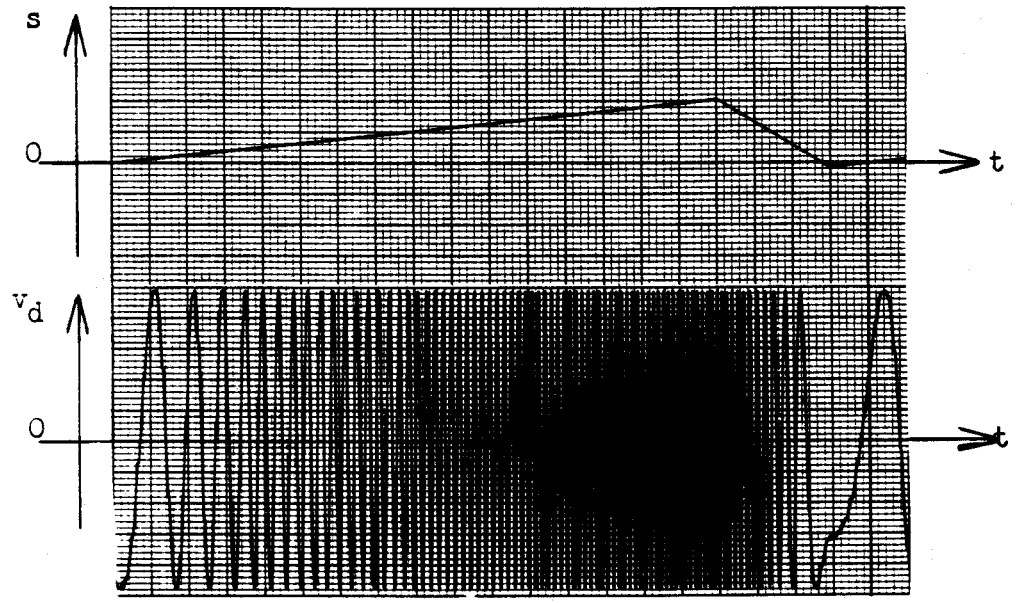



**Figure 4-21:** Frequency modulation at constant amplitude.
For both cases (a) and (b) the 0.01Hz slip signal is offset by a d.c.
Chart sensitivity for all plots:-
vertical - 100mV/div.
Horizontal - 1 div/sec.

NOTES.



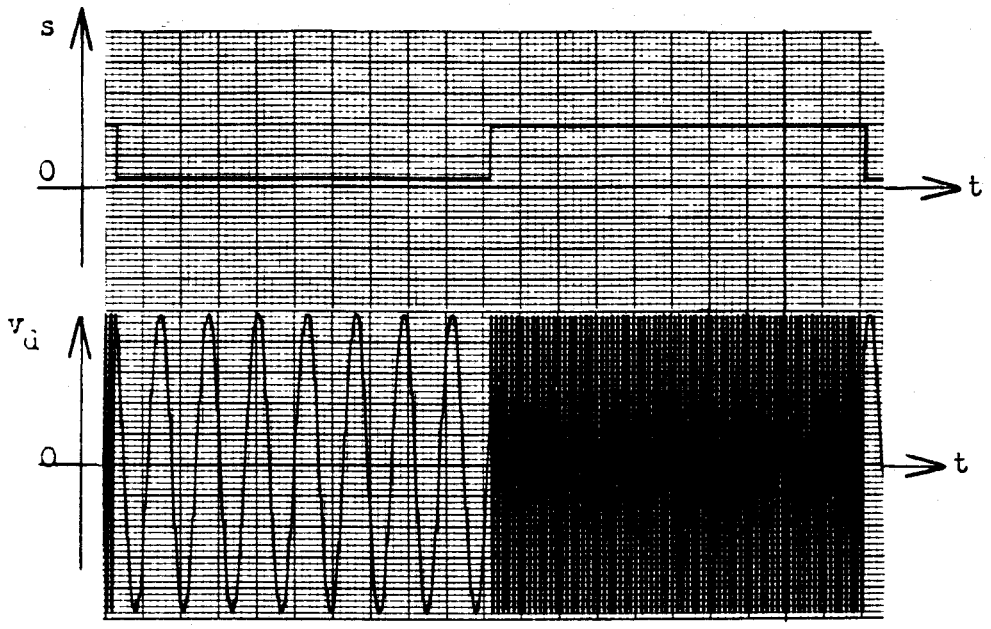

(a) The slip signal is an offset triangular wave.



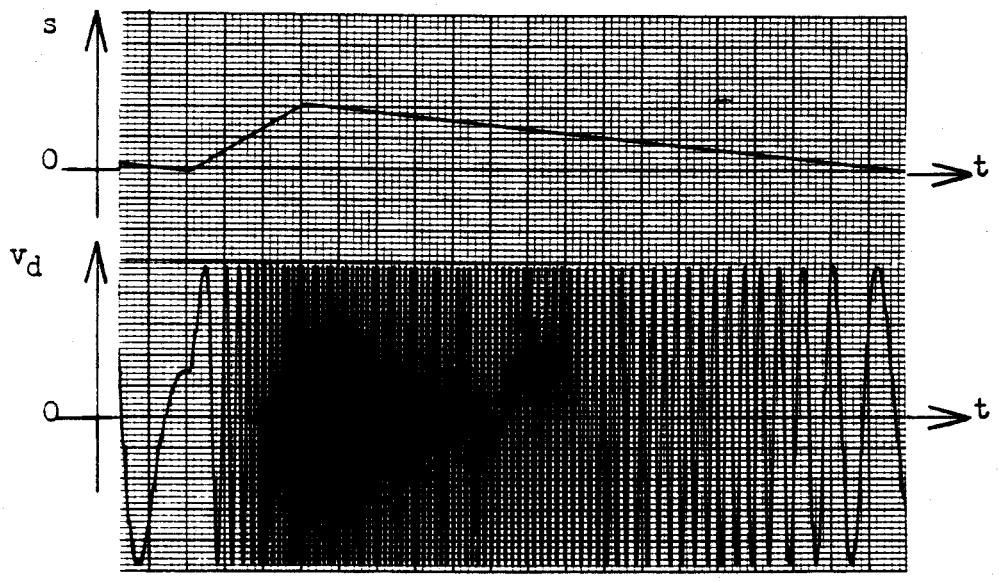

(b) The slip signal is an offset positive-ramp wave.

**Figure 4-22:** Frequency modulation for different waveforms of a 0.01Hz slip signal. The value of $f_o$ is 1.5Hz for both case (a) and (b).

NOTES. Chart sensitivity for all the plots:-
Vertical - 100mV/div.
Horizontal - 1 div/sec.




(a) The slip signal is an offset square wave.




(b) The slip signal is an offset negative-ramp wave.

**Figure 4-23:** Frequency modulation for different waveforms of a 0.01Hz slip signal. The value of $f_o$ is 1.5Hz for both case (a) and (b).

NOTES. Chart sensitivity for all the plots:-
Vertical - 100mV/div.
Horizontal - 1 div/sec.

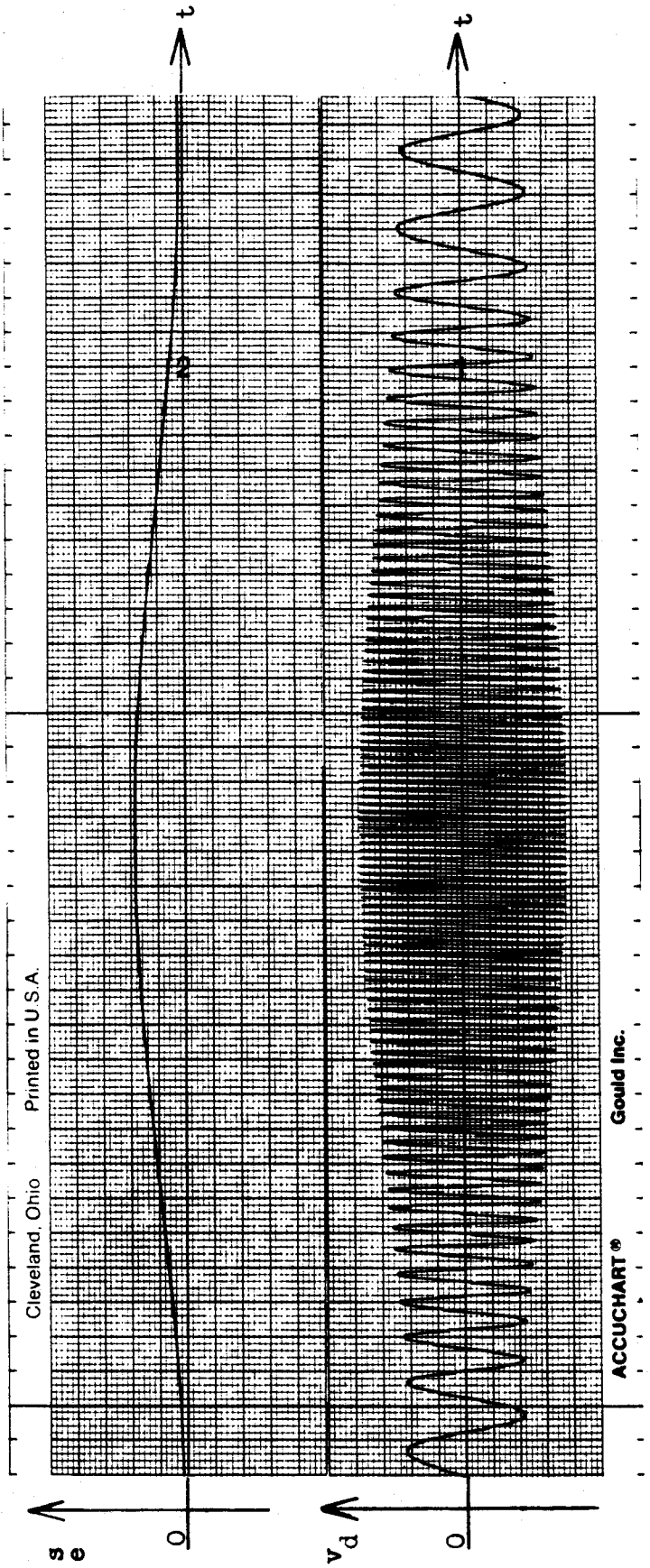



**Figure 4-24:** The oscillator sine output for the case of positive-amplitude modulation.

NOTES. $f_o$ = 1.0Hz
Input signal: a 0.005Hz offset sine signal used as e(t) as well as s(t).
Chart sensitivity for both plots:-
Vertical - 100mV/div.
Horizontal - 1 div/sec.

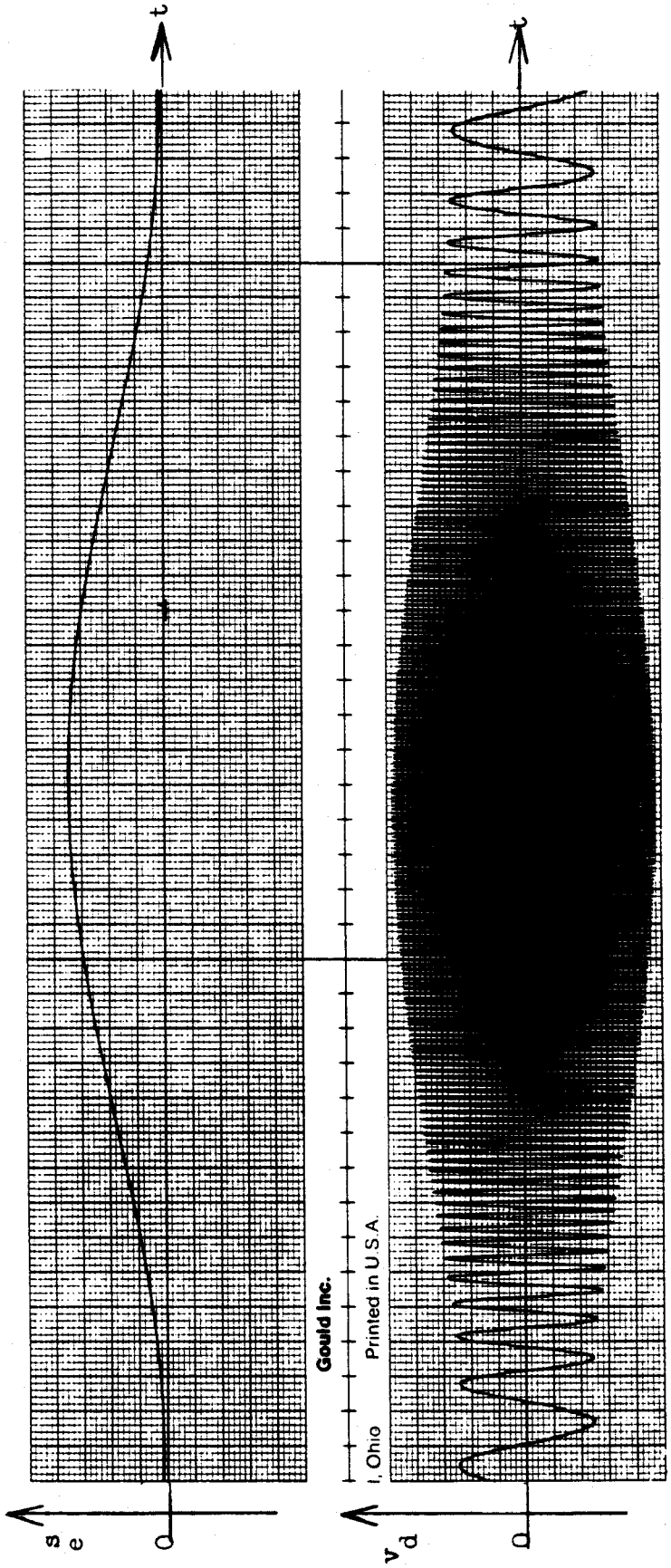



**Figure 4-25:** The oscillator sine output for the case of positive-amplitude modulation.

**NOTES.**

$f_o$ = 2.0Hz
Input signal: a 0.005Hz offset sine signal used as e(t) as well as s(t).

Chart sensitivity :-

Input: Vertical - 50mV/div. ,Horizontal- 1 div/sec.
output: Vertical - 200mV/div.,Horizontal- 1 div/sec.

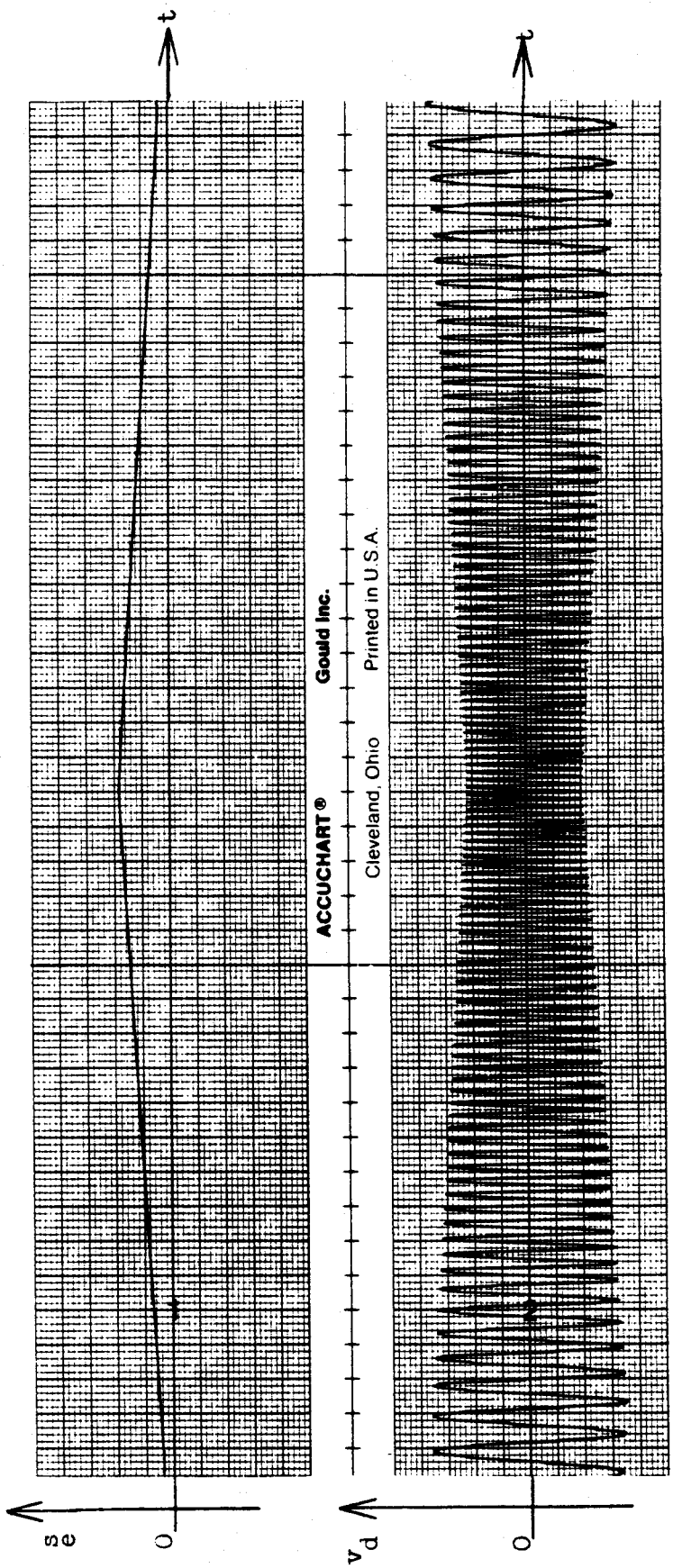



**Figure 4-26:** The oscillator sine output for the case of negative-amplitude modulation.

NOTES. $f_o$ = 2.0Hz
Input signal: a 0.005Hz offset sine signal used as e(t) as well as s(t).
Chart sensitivity for both plots:-
Vertical - 50mV/div.
Horizontal - 1 div/sec

Figure 4-26 show the negative-amplitude modulation. Figures 4-21 to 4-26 show that, the sections of the output waveforms corresponding to slip values near zero, appear to be distorted. These distortions correspond to the instants at which the D/A sampling frequency is changed. This demonstrates that the frequency modulation is more effective than amplitude modulation for values of slip close to zero. There are three D/A limitations which determine the effectiveness of amplitude modulation as explained in the following sections.

#### 4.7.3.1. Low Output Frequency

The amplitude modulation is affected when the D/A sampling frequency is low. The oscillator tries to output d.c. signals. At zero slip the sine output has to be zero. This can not be achieved due to the limitations of sampling control. Instead, the oscillator outputs a nearly steady value as demonstrated in Figure 4-27. The steady value is not unique, and it can be any value. The reason for this is that the LPAs handle data in units of buffer length. Relatively, it takes a longer time to empty a D/A data buffer at a low D/A sampling frequency. The amplitude control is therefore slowed down. This implies that, some of the $K_v$ settings are disposed of before they are used.

#### 4.7.3.2. Small Multiplication Factors

Small values of the $K_v$ settings ( $< 0.1$) distorts the output waveforms. This is caused by the rounding process during the integer conversion. Consequently, some samples ( of the $N$ samples per cycle) are set to be identical at small values of $K_v$. The effect of this limitation is more observable on a CRT. The lissajous figure becomes a rotating polygon instead of a circle.

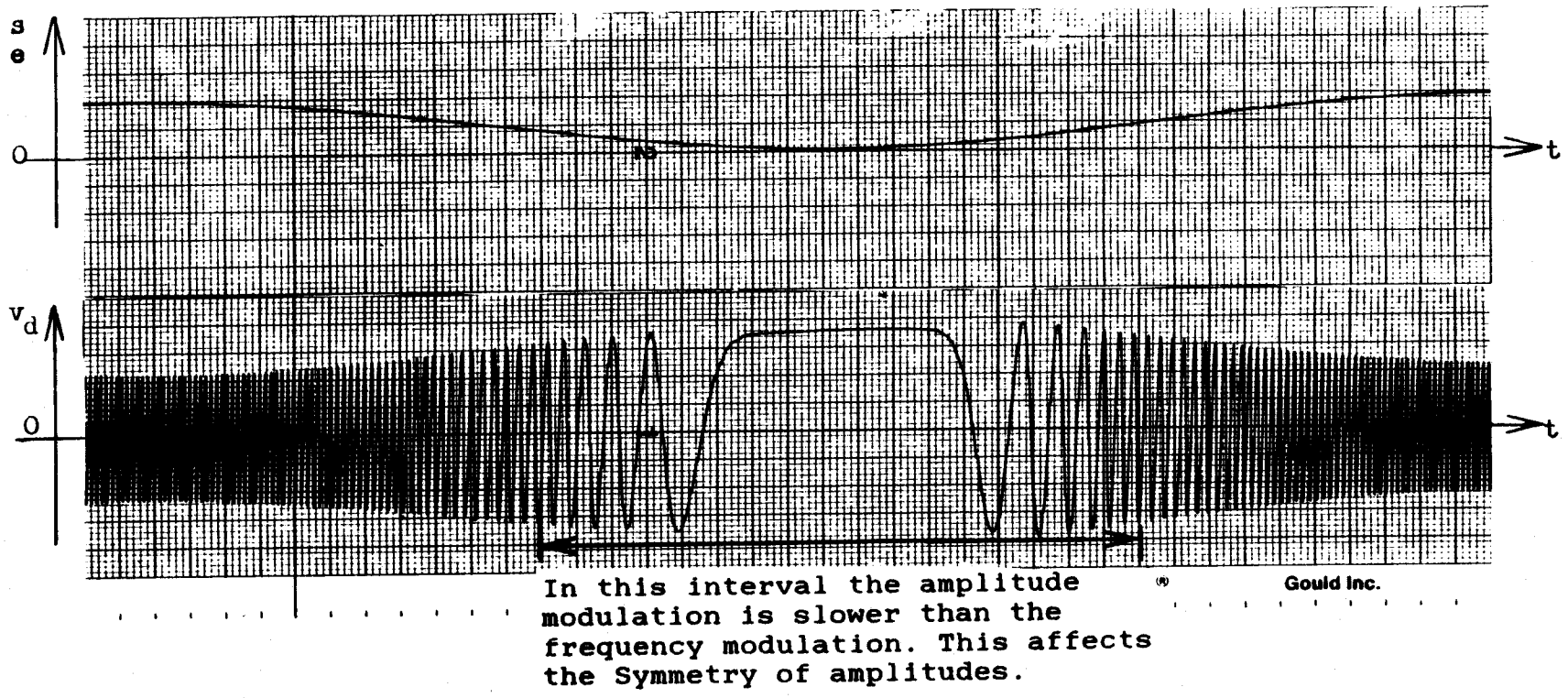



**Figure 4-27:** The effects of low output frequency (at slip values close to zero) on amplitude modulation.

NOTES. $f_o$ = 3.0Hz
Input signal: a 0.005Hz offset sine signal used as e(t) as well as s(t).
Chart sensitivity for both plots:-
Vertical - 50mV/div.
Horizontal - 1 div/sec.

#### 4.7.3.3. Insufficient A/D Sampling Rates

Sampling the input signals at insufficient rates introduces a phase shift between the input signals and the output signals. The effect is that the output is delayed relative to the input. This can be seen in Figures 4-17(b), 4-18(b) and 4-19. The explanation for this effect is again based on the multi-buffered structure of the LPAs, this time on the A/D process. When process B is active, the A/D buffers are filled with data and chained for processing one after the other. At insufficient A/D sample rates, it takes a relatively longer time to fill in a buffer with data before it is available for processing. Thus, the tracking of the input signal(s) is slowed down. The result of this is a delay in making the decision to change the amplitude.

# Chapter 5

# CONCLUSIONS AND RECOMMENDATIONS

A feasibility study on the use of a computer as a digital two-phase variable-amplitude variable-frequency oscillator has been carried out. The study was based on the excitation requirements of a dual-excited synchronous generator. The primary purposes of this research were to:

1. establish the control procedures for the oscillator,
2. identify the process variables and to develop the functional relationships between the variables, and
3. establish the limitations of the methodology.

The methodology was derived in Chapter 2. The experimental setup used to verify the methodology was described in Chapter 3. The results from the verification tests were presented and discussed in Chapter 4. This chapter summarizes the conclusions arrived at from the study. Some recommendations for further research are also included.

## 5.1. Conclusions

Based on the results of the experiments conducted, it can be concluded that the principal objectives of the thesis have been met. Collectively, the results support the following remarks.

1. It is feasible to implement a digital two-phase variable-amplitude variable-frequency oscillator by using a digital computer.

2. The technique offers a software-based way to generate good quality sinusoidal waveforms. The methodology has two options which can be used to select the frequency range of the oscillator, and also to control the harmonic distortion and the phase delay angle of the oscillator outputs. These two options are:

   a. the number of samples per cycle ($N$), and

   b. the range of the intersample setting ($T_{sa}$).

   It has been shown that the harmonic distortion of the outputs can be less than 1%, and the phase delay angle can be less than one degree, for $N \geq 200$ samples per cycle. It has been found that small time quantization units ($<10\mu$sec) are preferable for accurate approximation of the output frequencies. This suggests that the real-time D/A clock suitable for this application has to be of high rates ( > 100KHz).

3. The harmonic distortion of the output signals is independent of the output frequency. The oscillator control inherently has the capability to eliminate the low order harmonics of each possible output frequency by properly selecting the value of $N$.

4. The methodology uses numerically computed data for the signal generation, which must be recomputed each time the value of $N$ is changed. This data can be changed to generate a different set of signal waveforms. Hence, the oscillator is flexible.

5. The oscillator control is software-based. Thus, as long as the computer being used is continuously "up", the oscillator performance is independent of the effects of temperature or of component aging. This shows that the reliability of the software-based design is higher than that of analog systems such as the sine wave generator reported by Christiansen [34].

## 5.2. Recommendations for Further Research

The following are the research areas which form a basis for potential future studies related to this thesis.

### 5.2.1. On The Direction of The Field Rotation

Different multiplexing or switching techniques may be examined for a possibility to reverse the direction of the field rotation in on line mode. This implies that the power amplifier modules to be used must have the capability to transfer power both out of, and into the rotor. The multi-buffer structure of the LPAs may be organized such that three sets of reference D/A buffers are used for signal generation. The first set will be loaded with data for (say) the clockwise direction. The second set will be loaded with data for d.c. excitation, and the third set with data for anticlockwise rotation. A software control is required to decide which set should be used for signal generation at any instant of time.

### 5.2.2. On The Waveform Distortion

It is known [35] that certain schemes of waveform subdivision can reduce the distortion of the stepped output waveforms at a constant number of samples per cycle. It is therefore recommended that other schemes of waveform subdivisions be investigated in relation to this application.

### 5.2.3. On Other Applications

It may be mentioned that although this work has been concerned with the generation of a particular set of control signals, it is felt that the methodology can be applied to generate signals for other control problems. A typical application would be in the design of a variable frequency supply for an induction motor drive. The majority of induction motor speed control systems rely on varying the frequency of the supply to the motor to change the speed [36].

The digital oscillator described in this thesis can easily be modified to output balanced three-phase variable-amplitude variable-frequency control signals. This is by the addition of a third D/A channel to the output unit, and loading the three-phase sets of data in each of the reference D/A data buffers.

### 5.2.4. On The Power Amplifiers

The digital oscillator is of use only if proper power amplifiers are available to amplify the output signals to the required excitation levels of the generator. This area is only mentioned in this thesis. Therefore, extensive research on the appropriate power amplifier is recommended.

### 5.2.5. On The Implementation of The Oscillator on a Microcomputer

The methodology of the digital oscillator has been verified on a multiuser VAX-computer. The size of the VAX and its network are too large for the application advocated. The implementation of the methodology on a personal computer is expected to expose more competitive benefits of the signal generation technique. It is also expected that the amplitude control may be easier to achieve on a microcomputer. The investigation of this area is strongly recommended.

### 5.2.6. On Modelling The Oscillator

This thesis has only presented the performance of the oscillator in isolation. It is recommended that the oscillator, the prime mover, and the dual-excited synchronous generator be modelled as a system. The study of the model is expected to provide theoretical data for the design of a practical variable-speed variable-frequency generator setup.

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# Appendix A

# FREQUENCY CONTROL

## A.1. General

The time period of the output signals $T_{da}$, is given by:

$$T_{da} = NT_{sa} \tag{A.1}$$

where: $N$ - is the number of samples per cycle, and
$T_{sa}$ - is the intersample time per signal.

The frequency of the output signals fda $(=\frac{1}{T_{da}})$ can be controlled by either varying $N$ or $T_{sa}$. One value of $N$ and one range of $T_{sa}$ gives one range of frequencies. Indeed, real-time clocks have a fixed number of combinations of the clock frequency and the integer values of the preset counter. This allows only a subset of required frequencies. It was therefore expected that it would be difficult to establish very exact sampling frequencies with the LPAs. The clock settings, $T_{sa}$, were limited within the range of $100\mu sec \leq T_{sa} \leq 650msec$. This appendix describes a study on the different possibilities of varying $N$.

## A.2. Loading The D/A Data Buffers

The LPAs, as discussed in Chapter 2, are multi-buffered devices. More important is that the data transfer requests in these devices are based on sweeps. The sweeps handle the data transfers in units of buffer lengths. The excitation control problem under study requires two output signals. Hence, two D/A channels were used.

Figure B.1 illustrates how the D/A data is packed in each D/A data buffer of length $L$. These buffers are loaded with data such that the samples of both the sine and the cosine functions are in each buffer. This kind of data packing, and the use of two D/A channels introduce a doubling effect on the intersample time.

Thus, for a chosen sample time $\Delta$T, the sweep takes a duration of $2(\Delta T)$ to output consecutive samples of the same signal. Therefore, the actual intersample time for each signal is twice the clock setting. In order to maintain the clock setting value for each signal, a halving effect has to be introduced in the sweep control to cancel the doubling effect. The following derivations use the corrected intersample time $T_{sa} = 2(\Delta T)$.

## A.3. Loading D/A Buffers In terms of The Number of Full-Cycles

Figure B.2 illustrates the loading of the sine and the cosine ordinates into a D/A buffer in terms of the number of full-cycles ($N_{FC}$). In this case, each D/A buffer carries ordinates of one or more cycles of each function.

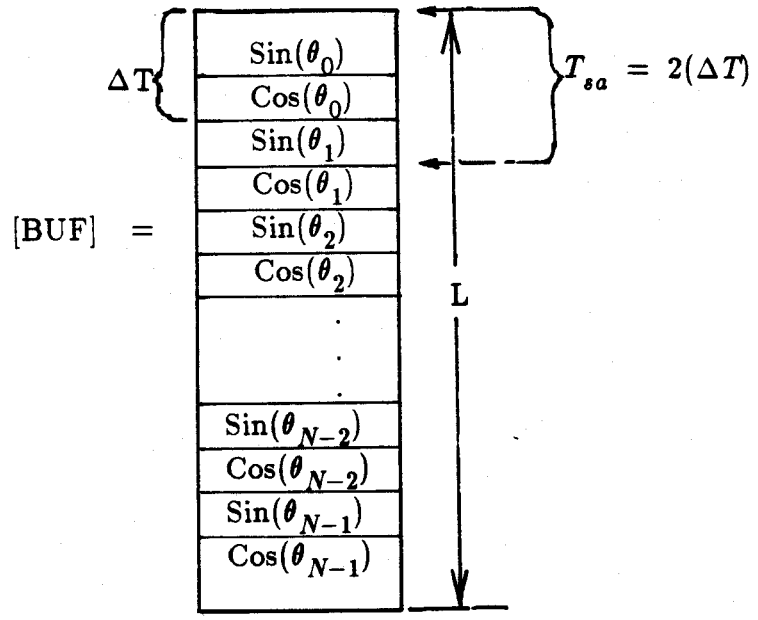


**Figure A-1:** Data packing in each D/A data buffer.

The period of the output signals sampled at a sample time $T_{sa}$ is given by

$$T_{da} = (\frac{L}{2N_{FC}})T_{sa} \qquad (B.2)$$

where: $T_{da}$ = the period of each output signal,
$L$ = the length of each D/A buffer, and
$N_{FC}$ = the number of cycles per D/A buffer.

The factor of two in the denominator of Equation (B.2) accounts for the fact that there are two sets of samples in each D/A buffer.

## A.4. Loading D/A Buffers In terms of The Number of Half-Cycles

As Shown in Figure B.3, a pair of the D/A buffers of the same length L is used to store data in terms of the number of half-cycles ($N_{HC}$). The data in one buffer is the negative of those in the other buffer. A continuous signal waveform for each signal is achieved by chaining the two buffers "head to tail". The period of the output signals is now given by:

$$T_{da} = (\frac{L}{N_{HC}})T_{sa} \qquad (A.3)$$

where: $N_{HC}$ - is the number of half-cycles in each D/A buffer.

The variable $N_{HC}$ must take odd values ($N_{HC}$=1,3,5, . . . ) to maintain a continuous waveform of each signal. In Equation (A.3), there is a scaling by a factor of two to the frequencies which can be obtained by Equation (A.2). Thus, the half-cycle option provides a new range of output frequencies.

## A.5. Loading of D/A Buffers In Terms of Quarter-Cycles

This scheme uses two pairs of D/A buffers. The four buffers are loaded as illustrated in Figure A-4. The scheme is only valid for odd values of the number of quarter-cycles ($N_{QC}$=1,3,5, . . . ). If the D/A buffers are of the same length $L$, and each containing one or more quarter cycles the period of the output signals, at a clock setting of $T_{sa}$ is given by:

$$T_{da} = (\frac{2L}{N_{QC}})T_{sa} \qquad (A.4)$$

A factor of four is introduced by the use of two pairs of buffers when compared to the full-cycle case. This causes a scaling by a factor of four to the frequencies which can be obtained by Equation (A.2). Again, this scheme opens a possibility of obtaining lower frequencies by a factor of four from those obtainable by Equation (A.2).

## A.6. Loading D/A Buffers In Terms of Cycle-Parts Multiples of Two

Each cycle of the output signals is divided into $P$ cycle parts such that:

$$P = 2b \tag{A.5}$$

where: $b$ - is the number of pairs of the D/A data buffers.

Each D/A buffer is set to have a length of $L$. While Equation (A.1) is always true, the value of $N$ is adjusted as follows:

$$N = \frac{2^{b-1}L}{N_P} \tag{A.6}$$

where: $N_P$ - is the number of cycle-parts in each D/A buffer.

The generalized expression of the period of the output signals for a clock setting of $T_{sa}$ is:

$$T_{da} = (\frac{2^{b-1}L}{N_P})T_{sa} \tag{A.7}$$

Thus, loading the D/A buffers in terms of full cycles corresponds to no pairs of buffers ($b$=0). In this case $N_P = N_{FC}$, and Equation (A.7) reduces to

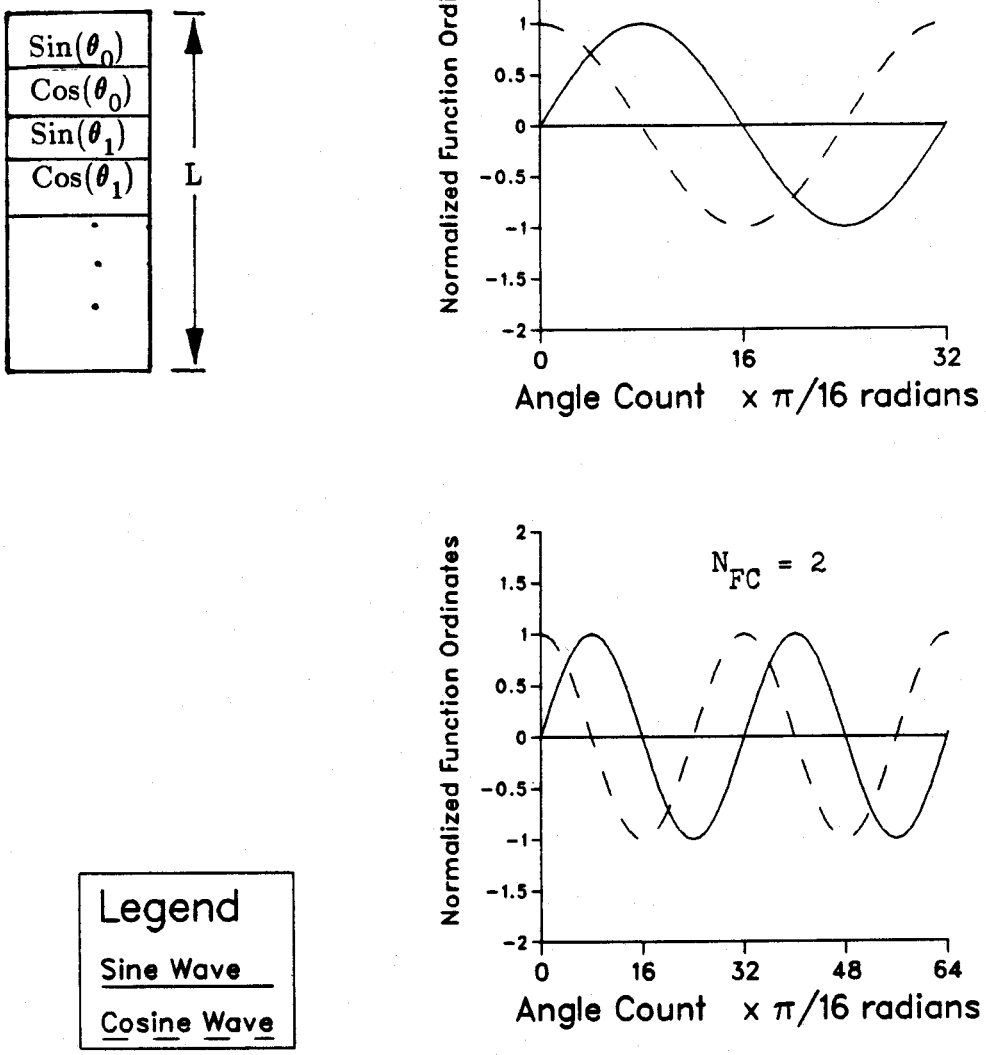


**Figure A-2:** Loading the D/A buffers in terms of the number of full-cycles ($N_{FC}$).

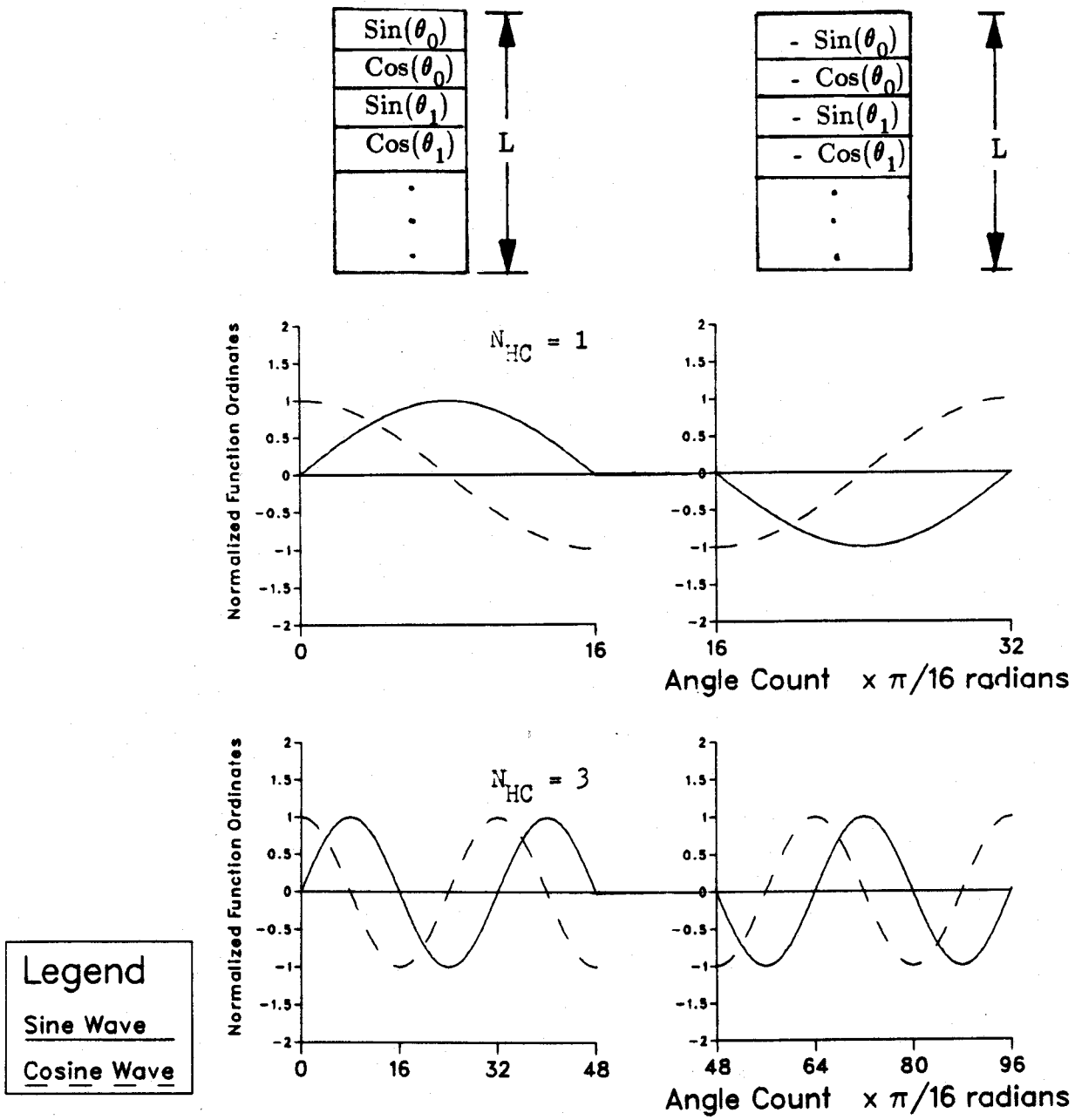


**Figure A-3:** Loading the D/A buffers in terms of the number of half-cycles ($N_{HC}$).

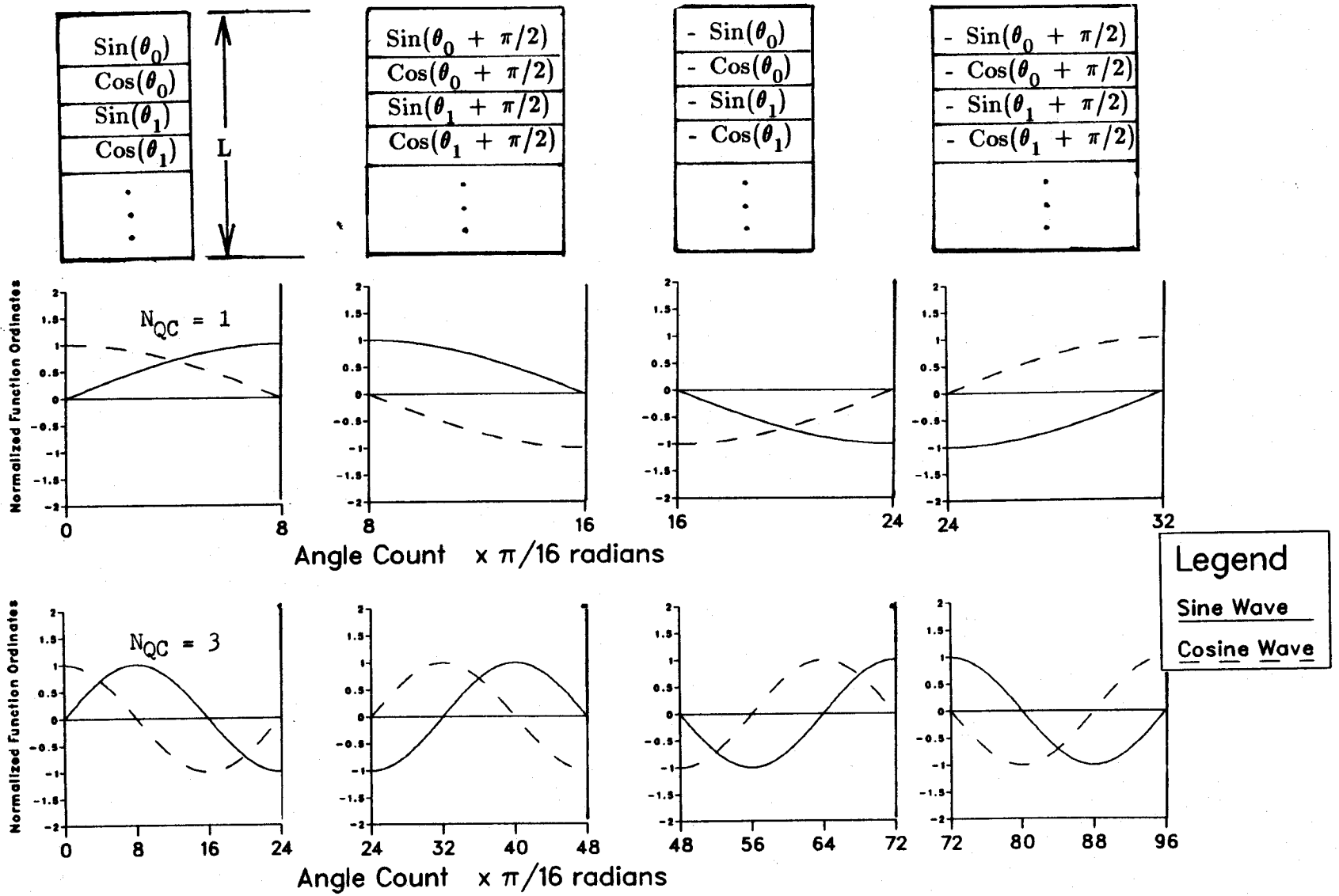


**Figure A-4:** Loading the D/A buffers in terms of the number of quarter-cycles ($N_{QC}$).

Equation (A.2). Similarly, Equations (A.3) and (A.4) can be realized by substituting $b = 1$ ($N_P = N_{HC}$) and $b = 2$ ($N_P = N_{QC}$) respectively.

However, the variation of $N$ as described by Equation (A.6) is constrained by the relation:

$$PL \leq 32768 \tag{A.8}$$

where the number 32768 is the largest word count in a 16-bit byte addressable memory.

# Appendix B

# MODULES OF THE OSCILLATOR SOFTWARE

## B.1. Introduction

A feasibility study has been carried out to investigate the use of a digital computer as a variable-amplitude variable-frequency oscillator. The application advocated is that of generating two-phase sine wave control signals for excitation control. The specifications of these control signals were the excitation requirements of a dual-excited synchronous generator when used for variable speed constant frequency schemes.

The computer used was a *VAX-11/780*, which supported two real-time peripheral devices called *Laboratory Peripheral Accelerators* [LPA11-K] [23]. This Appendix contains the description of the programs developed during the study. The listing of the programs can be found in reference [31].

## B.2. Software Description

The software is based on the modular programming technique [37]. Figure B-1 shows the action flow diagram of the test software. Each module is clearly associated with the execution of a particular task. The discussion in the following sections uses the routine names listed below.

| Routine Name | Function Description |
|---|---|
| MASTER | Supervisor program (process A). |
| MICROCODE | Loads the microcodes of the two LPAs. |
| ADPREPA | Sets, Initializes, and starts process B (A/D). |
| DAPREPA | Sets, Initializes, and starts process C (D/A). |
| AD2 | The main routine for process B. |
| DA2 | The main routine for process C. |
| ADWAIT | The waiting routine for process B. |
| DAWAIT | The waiting routine for testing process C. |
| FILDA | Data loader main routine for process C. |
| LOADER | Computes the reference data for process C. |
| FILBF0 | A/D completion routine - process B. |
| FILBF1 | D/A completion routine - process C. |
| PROC1 | Processes the slip and the voltage error data. |
| PROC2 | Estimates frequencies of two a.c. inputs. |
| AMPLITUDE | Adjusts the amplitude of the output signals. |
| ADCLOCK | Changes the A/D sampling rate when requested. |
| DACLOCK | Changes the D/A sampling rate when requested. |
| CLOCK | Changes the D/A sampling rate dynamically. |

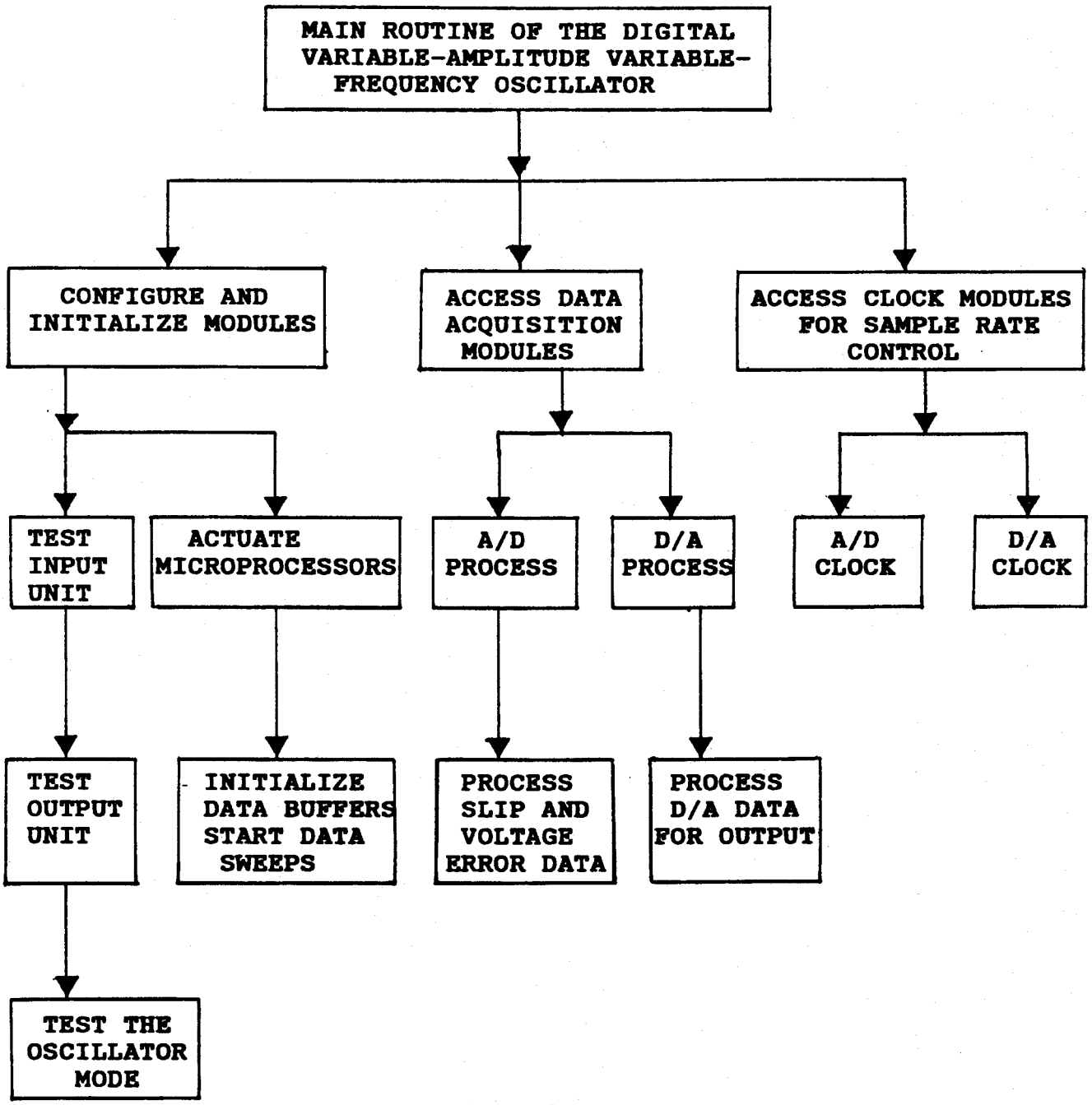


**Figure B-1:** The action flow diagram of the test software.

## B.3. Configuration and The Initialization Modules

The configuration and initialization modules are designed to load the LPAs' microcodes and start the LPAs microprocessors, and to set the initial clock rates and start the data transfer requests.

The first function is performed by the subroutine MICROCODE. The second function is performed by the routine ADPREPA for LPA0 and by the routine DAPREPA for LPA1. The supervisor program, MASTER, has a menu which allows the user to choose the system configuration to be tested. Presently, there are three main choices:

1. testing the A/D process (B) in LPA0 by calling AD2,
2. testing the D/A process (C) in LPA1 by calling DA12, and
3. running both the A/D and D/A processes simultaneously by executing AD2 and DA2.

The flow chart of the MASTER program is shown in Figure B-2. The interaction of the modules is illustrated in Figure B-3. The flow diagrams of the subroutines AD2, DA12, and DA2 are respectively shown in Figures B-4, B-5, and B-6.

## B.4. Data Acquisition Modules

Data acquisition modules are called for after establishing the predetermined initial conditions on the input and output devices. The operation of the data acquisition modules is based on the concept of the completion routines [23]. The supervisor program MASTER, allows each of the two completion routines, FILBF0 for the A/D sweep in LPA0, and FILBF1 for

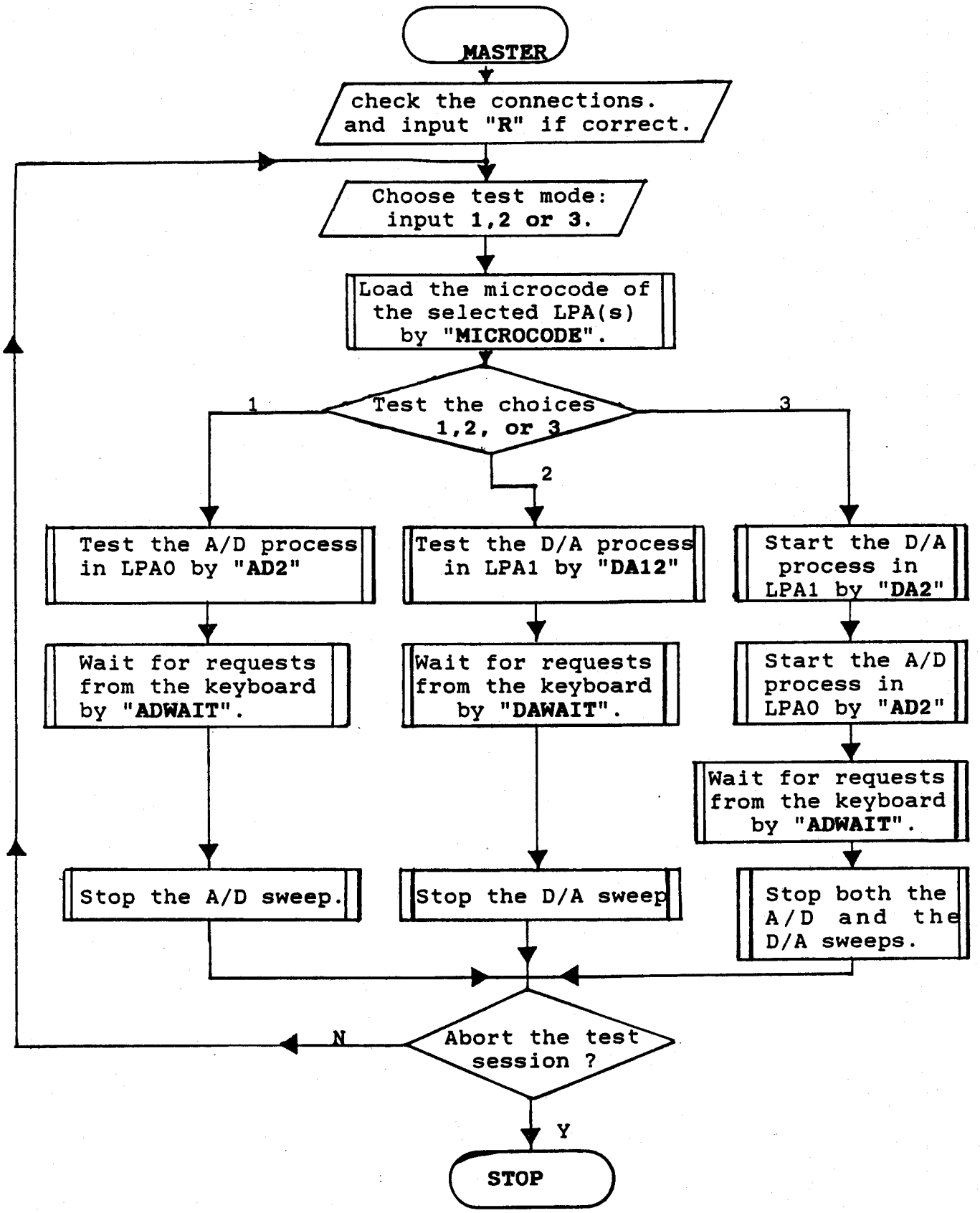


**Figure B-2:** The flow diagram of the MASTER program.

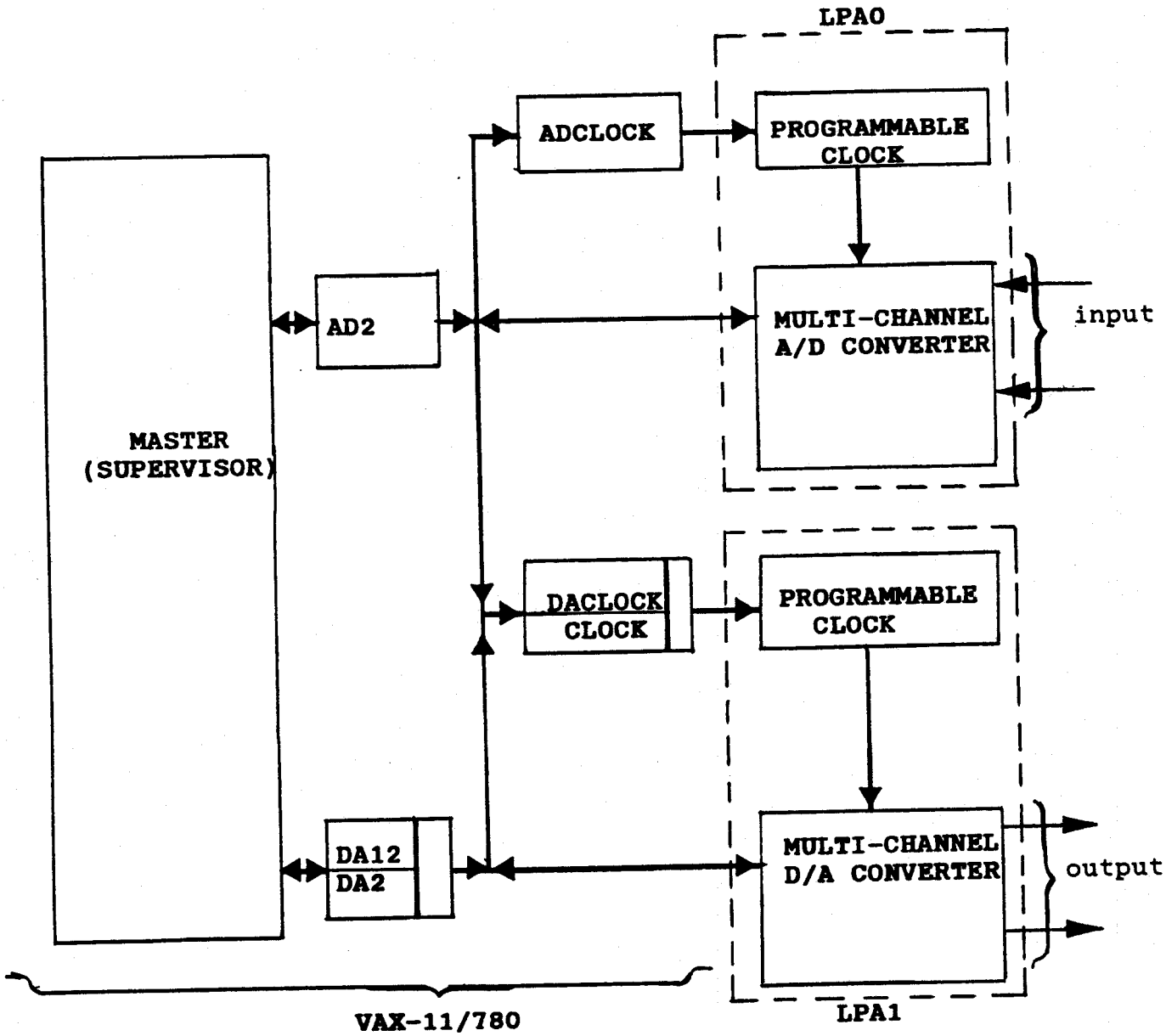


**Figure B-3:** Modules' interaction.

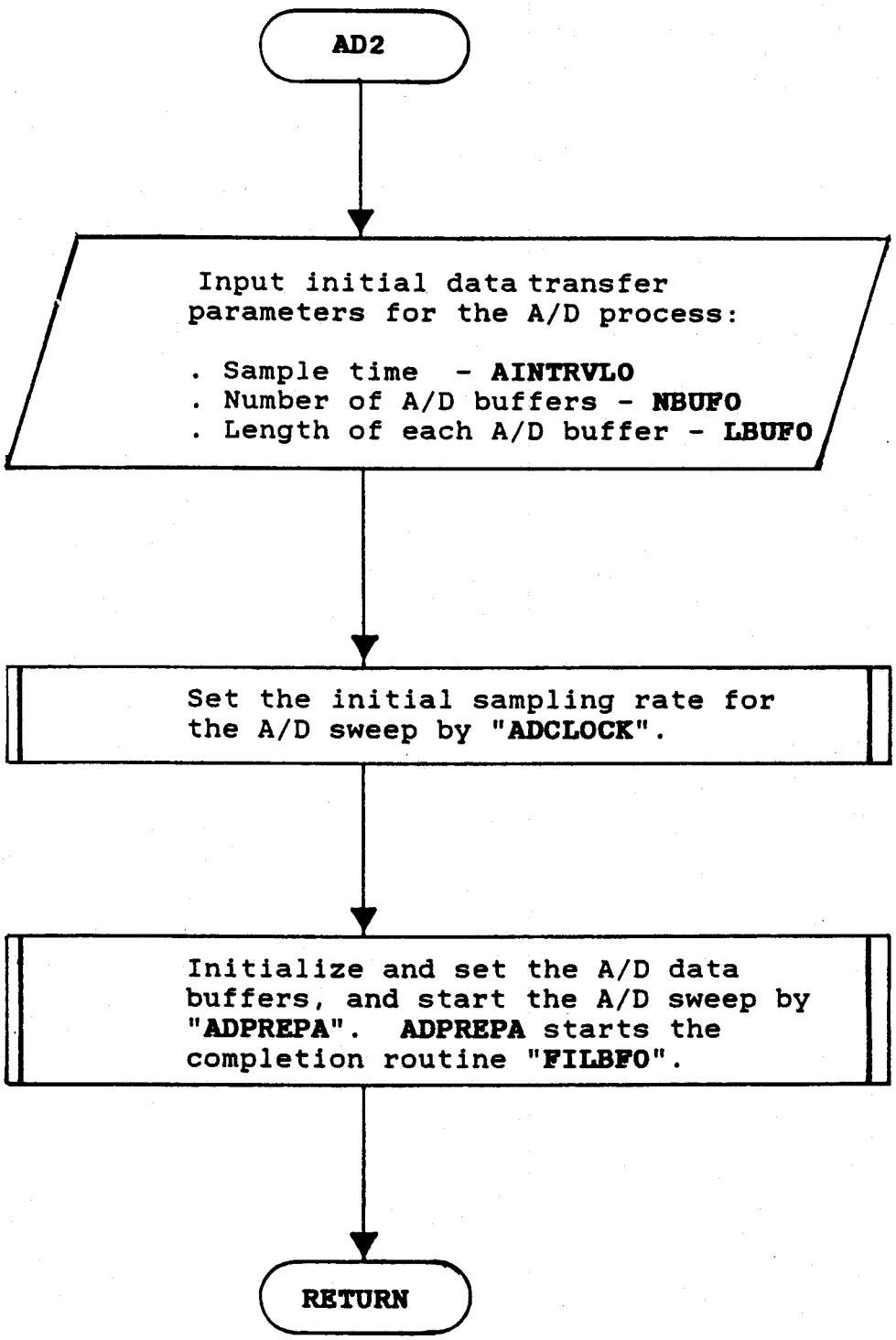


**Figure B-4:** The flow diagram of the AD2 subprogram.

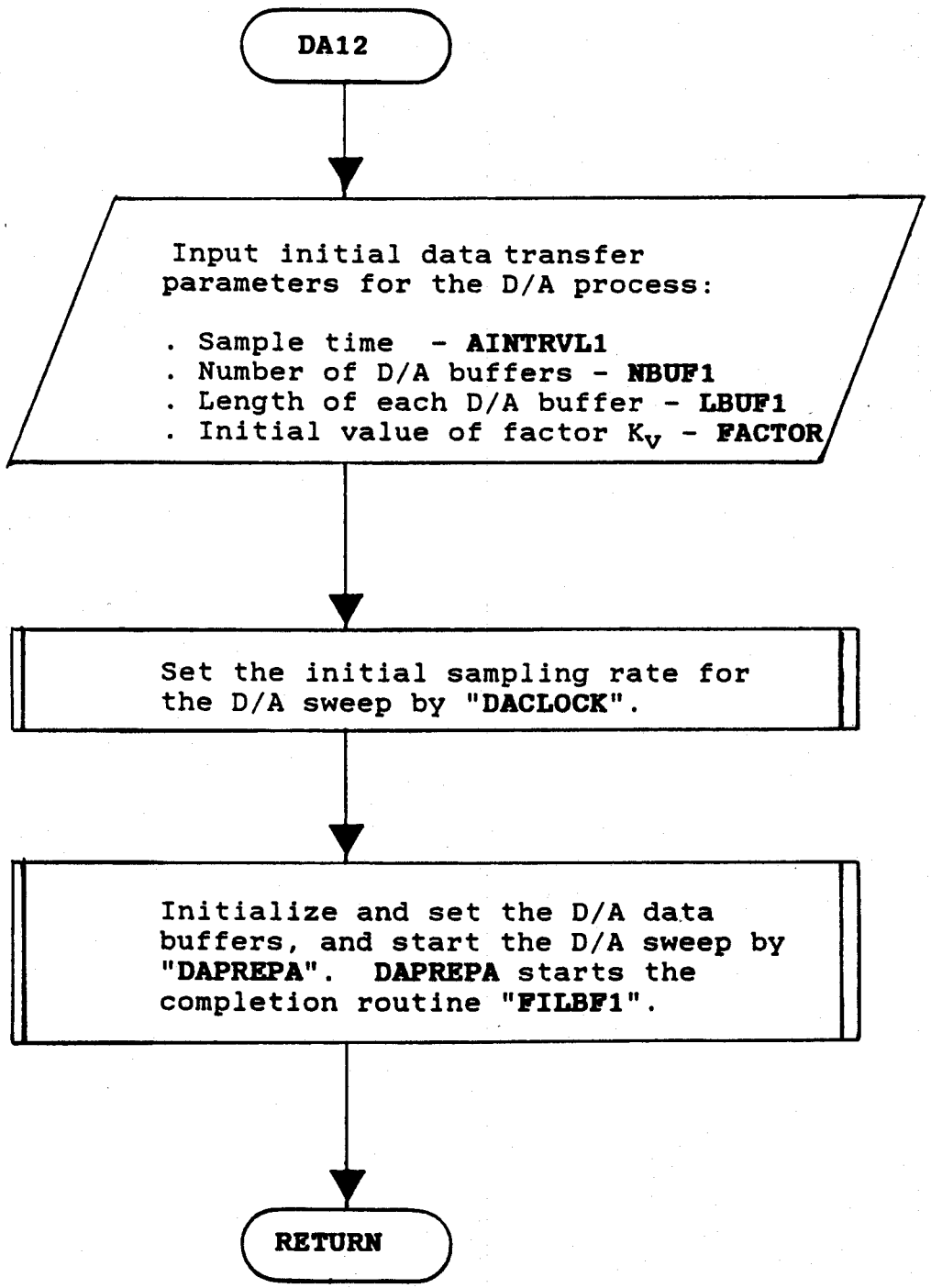


**Figure B-5:** The flow diagram of the DA12 subprogram.

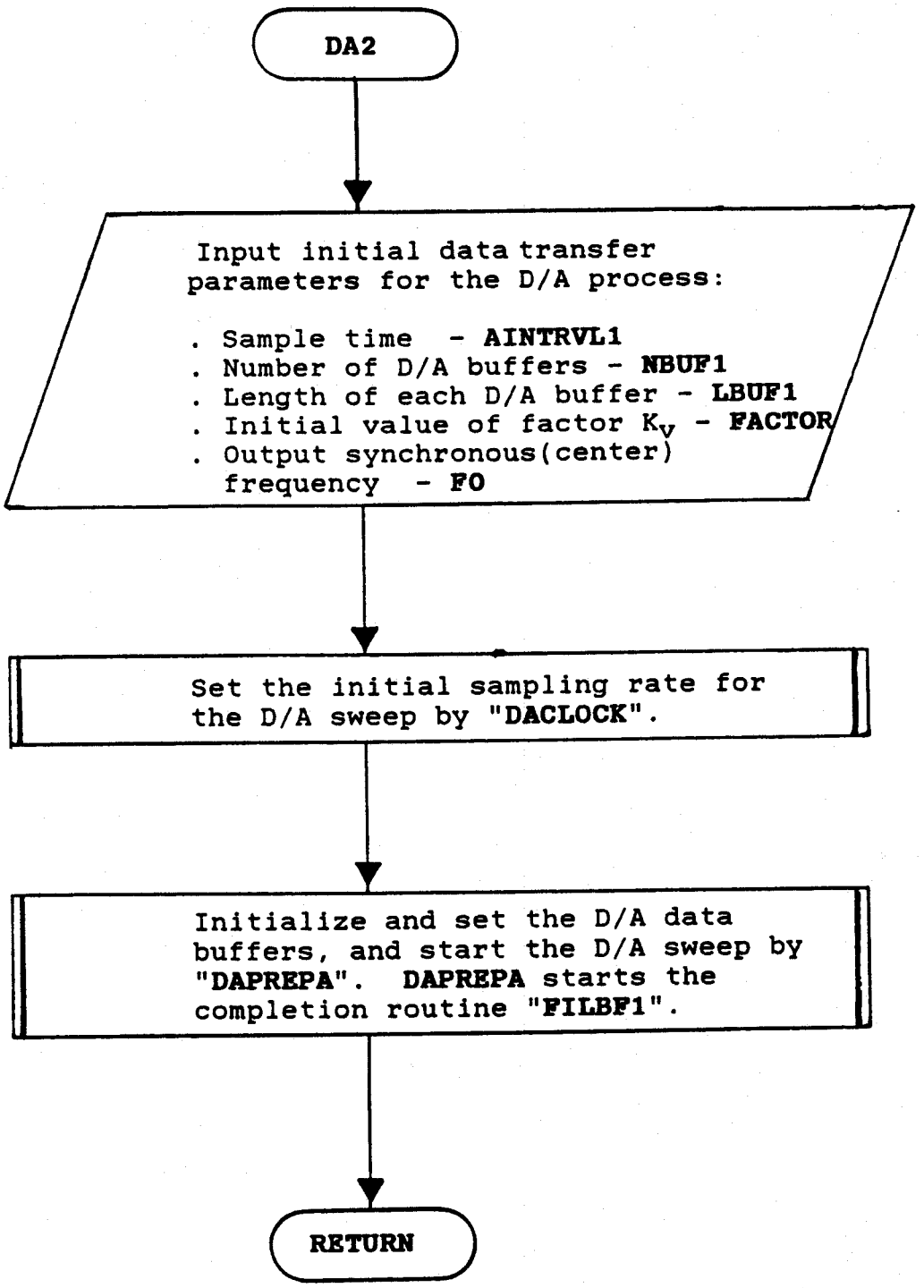


**Figure B-6:** The flow diagram of the DA2 subprogram.

the D/A sweep in LPA1, to run under continuous sampling while the main program is waiting. The waiting routine DAWAIT is executed when testing the D/A process in LPA1. The routine ADWAIT is the waiting routine both for testing the A/D process and when both processes are active. The flow diagrams of the routines ADWAIT and DAWAIT are respectively shown in Figures B-7, and B-8. For the case when both the A/D and the D/A processes are active, the two completion routines operate concurrently.

Figure B-9 elaborates the communication between the completion routines. In the present application, the A/D completion routine (FILBF0) is executed continuously to acquire the slip and the voltage error data. The acquired data is stored in temporary A/D buffers ready for processing. At the same time the D/A completion routine (FILBF1) is executed continuously to output the two variable-amplitude variable-frequency sinusoidal signals. The data for D/A process is preloaded into static memory buffers during the initialization process. The data loading is performed by the data loader routine LOADER referenced by FILDA, which is called by DAPREPA.

Eight input A/D data buffers are used to allow a sample buffer to be processed while the following buffers are being acquired. A twin buffer structure is used for the output buffers. This allows one buffer to be processed while the other is being emptied. The data buffers are chained and reused as the LPAs and the processing programs dispose of the data.

The signal processing is performed by the routines PROC1, PROC2,

and AMPLITUDE. The first two are referenced by, FILBF0, and the last one by FILBF1. The routine PROC1 computes the slip and the voltage errors corresponding to a time frame. It then sets the the D/A sampling rate and the new multiplication factor $K_v$. The routine AMPLITUDE uses the values of the factor $K_v$ to adjust the amplitude of the output signals. The routine FILBF0 calls the frequency estimator PROC2, as a processing routine, when testing the A/D process.

## B.5. The Principle of the Frequency Estimator

The frequency estimator was used to provide visual output for testing the A/D data acquisition process in LPA0. The algorithm employs the threshold crossing technique. The estimator requires both input signals (the slip and voltage error) be alternating about the threshold. Figure B-10 shows a portion of an alternating signal $y(t)$ in the neighbourhood of a threshold crossing.

First, the algorithm tests every two consecutive samples $y_{K-1}$ and $y_K$ of each signal for threshold crossing (see Figure B-10). A threshold crossing is detected when:

$$(y_{K-1} - y_{TH})(y_K - y_{TH}) \leq 0 \qquad (B.1)$$

After detecting a threshold crossing, the estimator performs an inverse linear interpolation to obtain the estimate of the time $t_{TH}$ corresponding to the threshold crossing:

$$t_{TH} \approx t_K - \frac{T_{ad}(y_K - y_{TH})}{(y_K - y_{K-1})} \qquad (B.2)$$

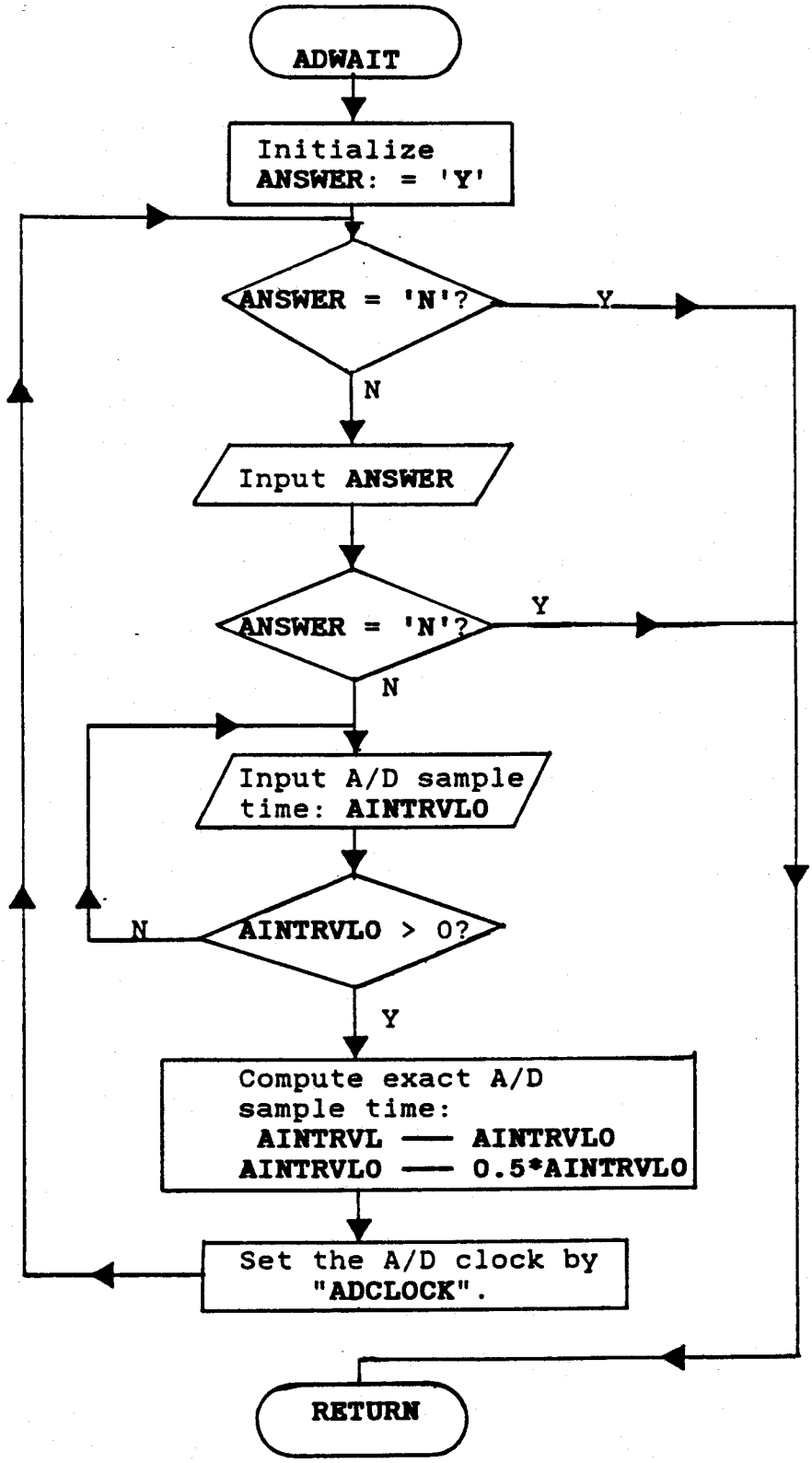


**Figure B-7:** The flow diagram of the ADWAIT routine.

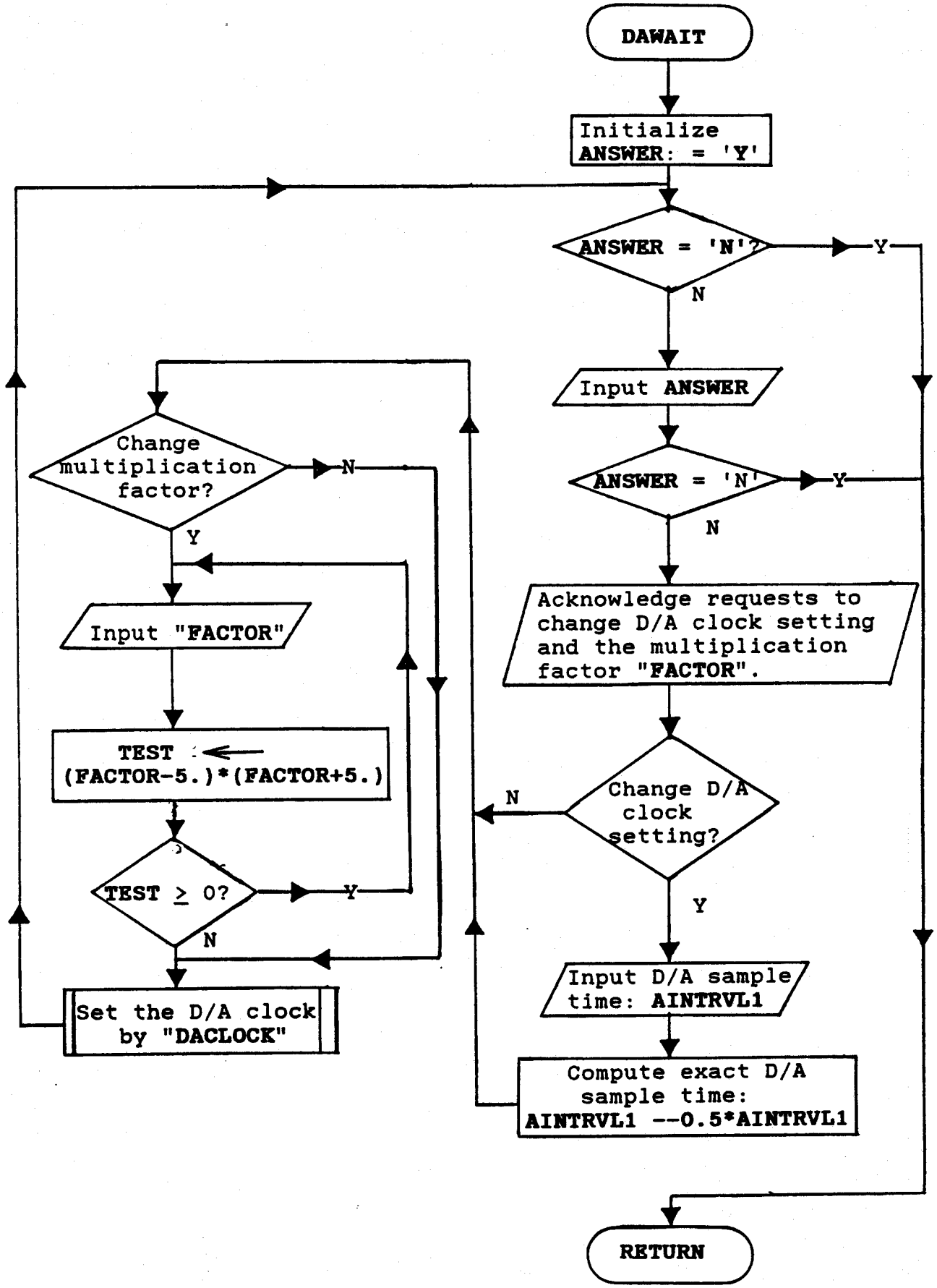


**Figure B-8:** The flow diagram of the DAWAIT routine.

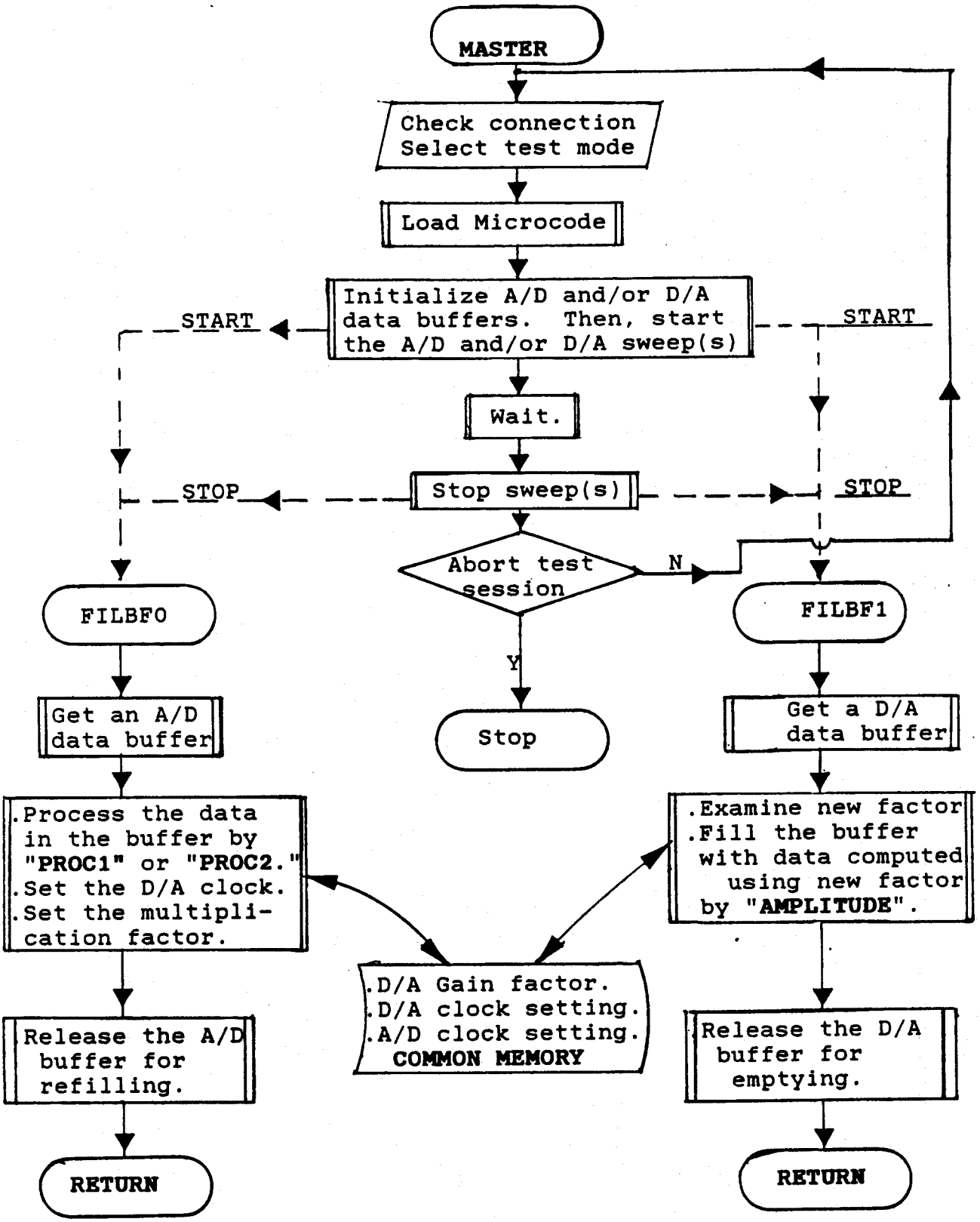


**Figure B-9:** The data flow between the completion routines.

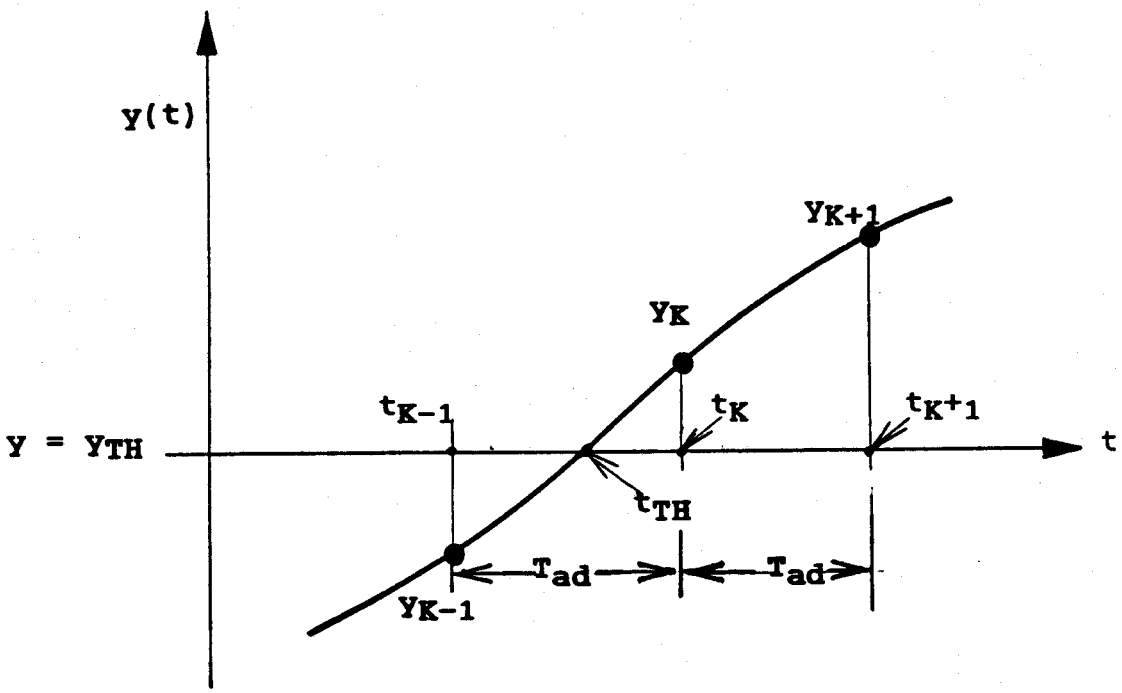


**Figure B-10:** Threshold crossing.

The difference between two consecutive values of $t_{TH}$ gives the estimate of a half period. The sum of two consecutive half periods gives the estimate of a full period. The reciprocal of the full period is the frequency estimate. The flow diagram of PROC2 is shown in Figure B-11.

## B.6. The Clock Modules

The clock subroutines ADCLOCK, DACLOCK, and CLOCK; are used to determine and set the sampling frequencies for A/D and D/A sweeps. The first two of these clock routines have interactive options for changing

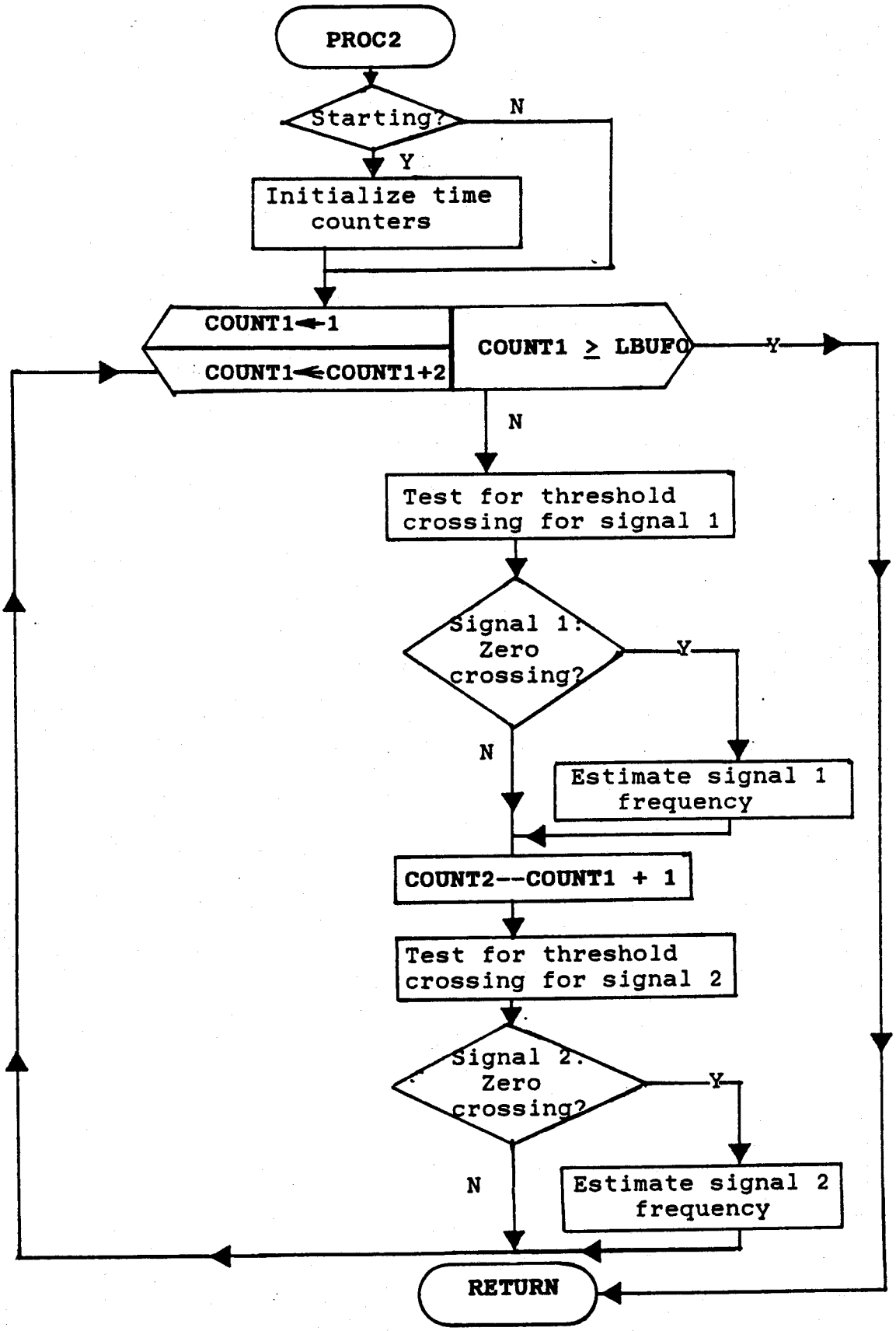


**Figure B-11:** Flow chart of the PROC2 subprogram.

the sampling rates when necessary. The routine ADCLOCK and CLOCK are referenced by PROC1. The routine ADCLOCK is for changing the A/D sampling rate from the keyboard, and the routine CLOCK is for changing the D/A sampling rate dynamically. The subroutine DACLOCK is referenced by DA12 and DA2, with which the user can change the D/A sampling rate from the keyboard.

# Appendix C

# WAVEFORM DISTORTION AND HARMONIC ANALYSIS

## C.1. Fourier Expansion

A distorted periodic voltage waveform $v(t)$, can be expanded into a Fourier Series [9, 28]. This expansion results in the description of the waveform in terms of harmonics:

$$v(t) = V_0+V_1\cos(\omega t+\beta_1)+V_2\cos(2\omega t+2\beta_2)+V_3\cos(3\omega t+3\beta_3)+\cdots \qquad (C.1)$$

where: $V_1$ - is the voltage peak value of the fundamental,
$V_n$; ($n$=1,2,3, . . . - is the voltage peak of the $n^{th}$ harmonic,
$\beta_n$ - the voltage phase of the $n^{th}$ harmonic,
and $\omega$ - is the fundamental frequency.

Knowledge of the parameters $V_n$, $\beta_n$; $n$=1,2,3, . . . along with $\omega$ completely determines the voltage waveform.

## C.2. The Indicators of Waveform Distortion

The most usual collective measure of the waveform distortion is the voltage distortion factor ($VDF$) defined as:

$$VDF = \frac{1}{V_1}\{\sqrt{\sum_{n=2}^{\infty} V_n^2}\} \qquad (C.2)$$

The other measure is called the phase delay angle ($PDA$). It is the delay

angle between the fundamental of the signal and the actual expected signal. This angle is also referred to as phase distortion [34]. Figure A.1 illustrates the interpretation of *PDA* for the sine output of the oscillator. It is evident from Equation (C.1) that *PDA* (in degrees) can be deduced from $\beta_1$ by the relation:

$$PDA\ (in\ degrees) = 270 - \beta_1 \qquad (C.3)$$

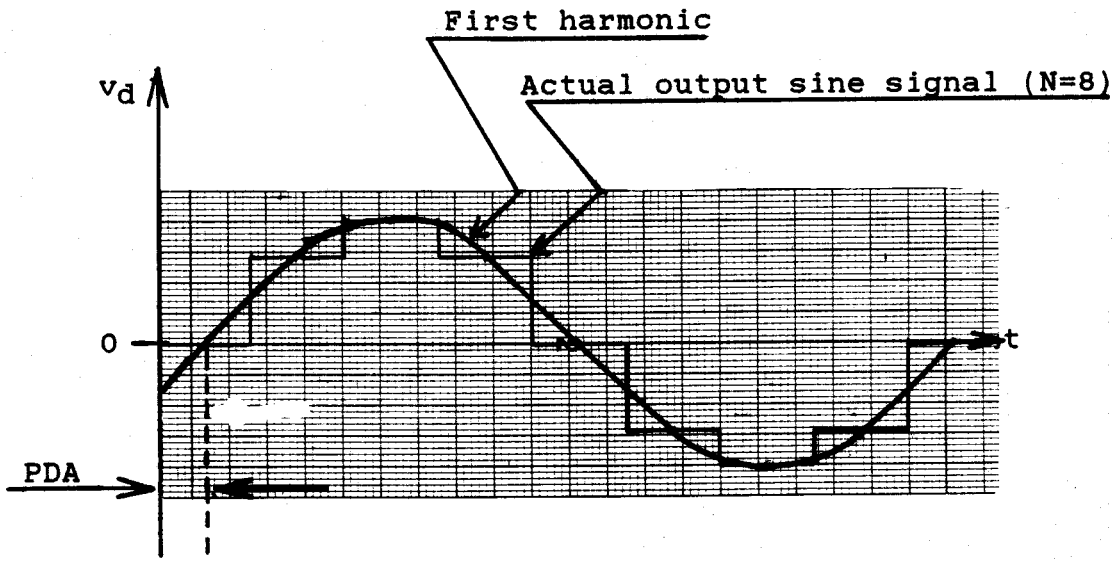


**Figure C-1:** Interpretation of phase delay angle (*PDA*) for a sine output of the oscillator.

The two measures *VDF* and *PDA* are used in this thesis as indicators for the quality of the waveforms of the generated sinusoidal signals. The oscillator stepped output sinusoidal waveform with infinite number of steps per cycle has both the values of *VDF* and *PDA* equal to zero, which means that the waveform has only the first harmonic.

## C.3. Modified Discrete-Time Fourier Expression

The discrete-time Fourier formulas for computing the real and imaginary components of each harmonic of a real periodic signal are well documented in references [9, 24, 28, 29]. In summary, the DFT coefficient of the $k^{th}$ harmonic of a real periodic signal $v(t)$ with a period $T_{da}$ and sampled such that there are $N$ samples per cycle is given by:

$$V_k = \frac{2}{N}\sum_{n=0}^{N-1} v[n]\ Exp(\frac{-j2\pi kn}{N}) \qquad (C.4)$$

where $k = 0,1,2, \ldots, \frac{N}{2} - 1$.

The time step $T_{sa}$ is subdivided into $M_h$ equal intervals of size $T_{sa}^{'}$ to simulate the holding action of the D/A register during the digital-to-analog conversion, such that:

$$T_{sa} = M_h T_{sa}^{'} \qquad (C.5)$$

This implies that, for each sample $v[n]$, there are $M_h$ samples of value equal to $v[n]$ placed between samples $v[n]$ and $v[n+1]$. Thus, the total number of

samples per cycle available for analysis will be $NM_h$ samples per cycle. As a result of this, Equation (C.4) changes to:

$$V_k = \frac{2}{NM_h} \sum_{n=0}^{NM_h-1} v[n]\ Exp(\frac{-j2\pi kn}{NM_h}) \qquad (C.6)$$

The Euler expansion of Equation (C.6) gives the real part of the $k^{\text{th}}$ harmonic as:

$$A_k = \frac{2}{NM_h} \sum_{n=0}^{NM_h-1} v[n]\cos(\frac{2\pi kn}{NM_h}) \qquad (C.7)$$

and the imaginary part as:

$$B_k = \frac{2}{NM_h} \sum_{n=0}^{NM_h-1} v[n]\sin(\frac{2\pi kn}{NM_h}) \qquad (C.8)$$

The phase angle of the $k^{\text{th}}$ harmonic is given by:

$$\beta_n = \tan^{-1}(\frac{B_k}{A_k}) \qquad (C.9)$$

At most $\frac{NM_h}{2} - 1$ harmonics can be determined. In this case the distortion factor $VDF$ is approximated as :

$$VDF \approx \frac{1}{V_1}\sqrt{\sum_{n=0}^{NM_h/2\ -\ 1} (A_k^2+B_k^2)} \qquad (C.10)$$

and the phase delay angle $PDA$ is approximated by Equation (C.3).