MODELING AND ANALYSIS OF THICK SUSPENDED DEEP X-RAY LIGA INDUCTORS ON CMOS/BICMOS SUBSTRATE

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ABSTRACT

Passive micro-scale inductors are playing an ever-increasing role in radio frequency integrated circuits (RFICs) and monolithic microwave integrated circuits (MMICs). At lower microwave frequencies, inductors on silicon (Si) substrates are a common approach, offering low process cost and possible integration with analog/digital large-scale integrated (LSI) circuits via CMOS/BiCMOS techniques. In recent years, RF MEMS (Microelectromechanical Systems) micromachinined inductors on Si substrates have received increased attention because they largely reduce not only the cost, size, and power consumption of the inductors, but also the Si conductive substrate loss and inductor metal trace resistive loss, which are two main drawbacks suffered by on chip inductors fabricated with traditional Si microelectronics processes, for instance, CMOS.

Synchrotron deep X-ray lithography (XRL, also known as LIGA) is a micromachining technique allowing the fabrication of ultra deep cavities and tall free-standing structures of arbitrary lateral shapes with high precision and high structural quality. These unique features have led to an interest in developing high performance microwave devices using LIGA. To the authors' knowledge, the LIGA microwave inductors have not been extensively explored.

This thesis presents the modeling and simulation results for two types of microwave inductors suitable for fabrication using the LIGA process. One is a suspended spiral inductor; the other is a suspended solenoid inductor. The inductors are suspended at 150 μm height. Copper is the typical metal in the CMOS/BiCMOS technique and was used for the inductor simulations. The Si substrate and Silicon Dioxide (SiO_2) isolation parameters are set up based on the TSMC 0.18 μm CMOS/BiCMOS process data.

As a simulation result, one can see the suspended MEMS inductor is a good approach to reduce the substrate parasitic loss for inductors fabricated on conductive substrates like Si. When suspended at 150 μm, a solenoid inductor can obtain a Q factor as high as 76.21 at 9.5 GHz on a simulated CMOS/BiCMOS substrate. The LIGA process is a

promising approach for fabricating such suspended structures due to its unique advantage of high aspect ratio and high quality vertical sidewall realization. By using multi-exposure LIGA and/or LIGA pattern transfer techniques, complicated 3D structures like the solenoid inductor, could potentially be fabricated on CMOS substrate with excellent performance. This result reveals the possible and promising strength of LIGA combined with CMOS for high performance inductor fabrications.

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LIST OF ABBREVIATIONS

BCB: Benzocyclobutene

BiCMOS: Bipolar Complementary Metal Oxide Semiconductor

CMOS: Complementary Metal Oxide Semiconductor

DC: Direct Current

FEM: Finite Element Method

GaAs: Gallium Arsenide

GMD: Geometric Mean Distance

GSG: Ground-Signal-Ground

HARM: High Aspect Ratio Metal

HFSS: High Frequency Structure Simulator

LIGA: German acronym for Lithography, Electroforming, and Moulding (Lithographie, Galvanoformung, and Abformung)

LSI: Large-Scale Integrated

MEMS: Micro-Electro-Mechanical Systems

MMIC: Monolithic Microwave Integrated Circuits

Ni: Nickel

NMOS: Negative-channel Metal-Oxide Semiconductor

PDMS: Polydimethyl Siloxane

PEEC: Partial-Element-Equivalent-Circuit

PMMA: Polymethyl Methacrylate

RF: Radio Frequency

RFIC: Radio Frequency Integrated Circuits

RIE: Reactive Ion Etching

SRF: Self-Resonant Frequency

TSMC: Taiwan Semiconductor Manufacturing Company

UV: Ultraviolet

VCO: Voltage Control Oscillator

1 Introduction

1.1 Motivation

The boom in wireless and satellite communications in recent years has generated strongly growing demands for radio frequency integrated circuits (RFIC's) and monolithic microwave integrated circuits (MMIC's). Micro-scale inductors are playing an ever-increasing role in these circuits. Although active devices can be synthesized into an equivalent of an inductor, they usually have higher noise, distortion, and power consumption than the passive counterpart. These limitations place a severe restriction on their application. For inductors in high performance radio frequency (RF) and microwave circuits, it is often essential to use passive realizations.

In the classical radio coil, a ferrite core was used for size reduction because it can significantly strengthen the magnetic field. However, it cannot normally be applied over 1 GHz due to the high polarization losses and low permeability [1]. Soft ferromagnetic cores may be applicable in the future at high frequencies if the eddy current losses in the conductive films can be suppressed [2], [3]. Consequently, high frequency inductors are usually built with an air core, which consumes excessive chip area.

At lower RF and/or microwave (hereinafter, RF and/or microwave will be called microwave) frequencies, (ie:< 4 GHz), the use of lumped inductors greatly reduces circuit size in contrast to distributed elements. A higher density of circuits per wafer, lower cost, and higher yield can also result. Normally, micro-scale microwave inductors are built on silicon (Si), gallium arsenide (GaAs), and alumina (Al_2O_3) substrates. Compared with GaAs and alumina technology, which are popular for higher microwave frequencies, Si/CMOS (Complementary Metal Oxide Semiconductor) technology is a popular alternative at lower microwave frequencies as it offers low process cost and

possible integration with digital large-scale integrated (LSI) circuits. Therefore, the research of micro-scale inductors on Si substrate is significant and has been extensively conducted in recent decades. Usually, on chip passive inductors are made by conventional Si microelectronics technology. But due to the Si conductive substrate loss (eddy current loss and displacement current loss) and metal resistive loss in the inductor metal trace, they typically suffer from low quality (Q) factors (generally less than 10) and low self-resonant frequencies (*SRF*). Many attempts have been explored to reduce these two drawbacks. Of them, the micromachining approach has exhibited unique advantages and has already proven to be one of the leading approaches to realize inductors on Si.

Generally, there are three kinds of micromachining techniques, surface micromachining, bulk micromachining, and LIGA. They are the same techniques used to fabricate MEMS (Micro-Electro-Mechanical Systems) except the MEMS device literally includes some moving parts. Though micromachinined structures do not necessarily have moving parts, today many of these structures are loosely categorized as MEMS. The LIGA technique, a German acronym for Lithographie (deep X-ray lithography), Galvanoformung (electroforming), and Abformung (plastic molding), was first developed at the Karlsruhe Nuclear Research Center (later Research Centre Karlsruhe) in Karlsruhe, Germany [4]. LIGA is an advanced micromachining process featuring high aspect ratio, high accuracy, excellent sidewall structural quality, and potentially low cost mass production. In contrast to surface micromachining and bulk micromachining, it has advantages for building more precise, larger aspect ratio, and smaller structures. Furthermore, suspended structures can potentially be fabricated using the LIGA process because of its high aspect ratio realization property. This provides LIGA an unique advantage to potentially overcome the Si substrate loss drawback. However, the fabrication and characterization of micro-scale inductors for microwave applications using the LIGA process has not been extensively explored.

In this research, the possible integration of LIGA fabricated inductors with the Si microelectronics process, CMOS, is also considered. If passive components with high

performance cannot be fabricated on the same chip with the rest of the circuits, they must be connected externally, for instance with bonding wires. These connections introduce parasitic loss and reduce the performance of the passive component. As well, non-integrated components enlarge the volume of the whole circuitry. Direct X-ray exposure as a post-CMOS process is likely unsuitable for many CMOS chips with active circuitry due to the potential damage produced by the hard X-rays to the dielectric components of the CMOS circuits. In these situations, polymer replication and electroplating-based LIGA approaches could be viable solutions. Recently, there is some progress reported in this field [5]. An important criterion to measure the commercial value of a technique is its potential integration and performance with leading industrial techniques, in this capacity, CMOS. Therefore, it is also worthy to do some exploration by modeling the LIGA structural inductors on the simulated CMOS/BiCMOS (Bipolar Complementary Metal Oxide Semiconductor) substrate and analyze their performance and characteristics. In doing so, one can anticipate and evaluate the advantage of LIGA in possible future industrial applications combined with CMOS.

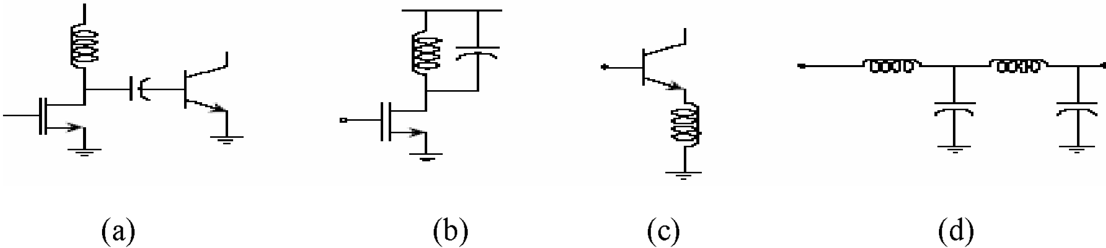
This thesis explores these issues: MEMS (Micromachining)/deep X-ray LIGA process; inductor theories and loss mechanisms; solenoid and spiral suspended inductor model designs, simulations, and performance/characteristic analysis on the simulated CMOS/BiCMOS Si substrate. Also a brief discussion of the fabrications using deep X-ray LIGA as a possible post CMOS processing step is presented.

1.2 Importance of Inductors in Communication Circuits

Inductors have extensive usage in wireless communications circuits. For example, the inductor is often used in resonant circuits. At sub-microwave frequencies, inductors can be realized by employing active devices, but passive inductors dominate in high frequency capacities. Several common applications of passive inductors used in Si ICs are shown as follows in Figure 1.1[6].

Figure 1.1 (a) is an impedance matching example. Through impedance matching, one can achieve, although not simultaneously, minimal noise, maximum gain, minimal reflections, and optimal efficiency. In the Figure, the input impedance of the second transistor is matched to an optimal impedance value desired by the driving transistor.

Figure 1.1 (b) shows a LC tuned load. A resistive load's frequency response is typically limited by its RC time constant. A tuned load can be used to obtain improved gain at high frequencies. The advantages of an LC passive is that it is less noisy than a resistor, consumes less voltage headroom, and obtains a larger impedance at high frequencies. A tuned load is also an essential part of oscillators.



(a) (b) (c) (d)

Figure 1.1: Applications of passive inductors in Si IC building blocks. (a) Impedance matching. (b) Tuned load. (c) Emitter degeneration. (d) Filtering.

In Figure 1.1(c), an inductor is used as a series-feedback element. Series feedback can, for example, increase the input impedance, stabilize the gain, or lower the non-linearity of the amplifier. A series-feedback inductor can result in less voltage headroom, and less additional noise in contrast to a resistor. The inductance can also be used to generate real input impedance at a particular frequency, thus providing a better impedance match at the input of the amplifier.

Figure 1.1 (d) exhibits a low-pass filter realized by inductors and capacitors. Compared to active filters such as gm-C [7] or MOSFET-C filters [7], passive filters can operate at higher frequencies, have higher dynamic range due to the intrinsic linearity of the passive devices, and inject less noise while requiring no DC power to operate.

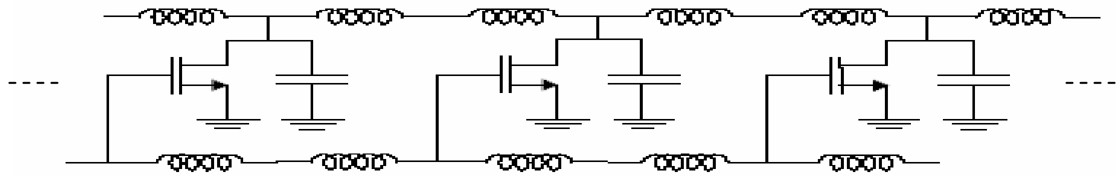


Figure 1.2: Applications of passive devices in Si IC building blocks: Distributed Amplifier

Figure 1.2 is an artificial transmission line in a section of distributed (traveling-wave) amplifier formed by inductors and capacitors. Since the LC network acts like a transmission line, it has a broadband response. A wave propagating on the gate-line is amplified and transferred onto the drain line. If the propagation velocity on the drain line matches the gate line, the signals on the drain line add in phase and the drain line delivers power to a matched load.

1.3 Si / CMOS Technology

Si technology is a competitive technology for realizing future microwave integrated circuits. Although GaAs offers superior gain, higher frequencies of operation, an insulating substrate, and higher Q factor realization, from the perspective of cost, CMOS is the clear winner. In addition, emerging advances in Si technology, for instance, SiGe, are closing the gap between Si and GaAs in performance in the 1–10 GHz frequency range. Si is also the best choice for integrating digital functionality in CMOS/BiCMOS technology. Thus, there is great value in integrating passive devices in CMOS technology.

The unity gain frequency of NMOS (Negative-channel Metal-Oxide Semiconductor) transistors and bipolar transistors is inversely proportional to the lateral channel length and vertical base width, respectively [8]. The vertical base width of a bipolar transistor W_B is determined by a diffusion process whereas the lateral channel length L of an MOS transistor is determined by lithographic processes. Traditionally, a diffusion process can make a shorter channel length than a lithographic process. In this case, it results in W_B

shorter than L. Thereby the bipolar transistors typically exhibit advantage in speed. However, the CMOS transistor channel length has been narrowed significantly with advances in lithographic technology. Within the next decade, CMOS technology is expected to be a viable and cost-effective alternative to both bipolar and GaAs.

However, in contrast to GaAs, CMOS does suffer from the conductive loss drawback. Electromagnetic energy couples to the substrate and the lossy nature of the Si substrate limits the on chip passive Q factor severely. When the substrate is heavily conductive, magnetically induced eddy currents in the substrate can be a dominant loss mechanism. Several techniques are developing to overcome this defect. Micromachining is one of the most promising.

1.4 MEMS/LIGA Techniques

MEMS mean "Micro-Electro-Mechanical Systems". They are also called "Microsystems". Literally, "Micro" describes the dimensional scale; "Electro" means electricity and/or electronics; and "Mechanical" suggests moving parts of some kind. But generally, the MEMS concept is also extended to include nonmoving parts. For instance, this dissertation considers a type of nonmoving MEMS device; MEMS inductors. In recent years, RF MEMS has become an actively developing branch in the MEMS area with focus on high frequency MEMS devices and systems for RF/Microwave communications. Various high performance RF MEMS components such as RF MEMS switches, varactors, and inductors, micromachined transmission lines, high-Q resonators, filters, and antennas have been reported [9]. The inductors presented in this thesis are also in this area and operate in the frequency band from 4 GHz to 12 GHz, considerably higher than traditional CMOS based inductors which are typically limited to only a few GHz.

Normally, MEMS devices are produced using lithography-based micro-fabrication techniques, which are borrowed from the microelectronics industry and modified with specialized techniques generally called "micromachining". MEMS techniques can

typically realize more complicated microstructures with less shape/dimension restrictions than the microelectronics techniques. In addition, batch fabrication capabilities similar to the microelectronics industry provide the cost reduction potential for high volume manufacturing.

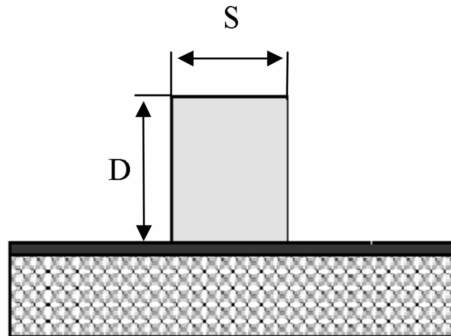


Figure 1.3: Illustration of aspect ratio

Generally speaking, there are three distinct micromachining techniques, bulk micromachining, surface micromachining, and the LIGA process. Bulk micromachining involves the removal of material from the bulk substrates, usually made of silicon, to form the desired three dimensional microstructures. In contrast, surface micromachining builds microstructure by adding materials layer by layer on top of the substrate. Both bulk micromachining and surface micromachining involve aspects borrowed from the microelectronics technology, particularly the CMOS process. In consequence, for an individual surface micromachining or bulk micromachining technique, if there is no high-temperature process involved, they can sometimes be CMOS compatible. In practice, it is sometimes advantageous for the three basic micromachining techniques to be combined together by corresponding process adjustments, and people strive for CMOS-compatible bulk micromachining or LIGA processes. The CMOS process can be regarded as a type of surface-micromaching process in essence. Thus, a CMOS compatible bulk micromachining or LIGA process implies fitting these process steps into the Si/CMOS surface micromachining process. A problem with Si based surface micromachining techniques is that they suffer from the low geometric aspect ratio limitations. Geometric aspect ratio of a microstructure is the ratio of the dimension in the depth (D) to that of the lateral surface (S), which is shown in Figure 1.3. The LIGA process overcomes this drawback.

Thanks to strong penetrating capability of X-ray radiation, deep X-ray LIGA is one of the few technologies offering high aspect ratio microstructure geometry. In contrast to UV (Ultraviolet)-LIGA, which can typically realize the vertical aspect ratios up to around 20 [10], deep X-ray LIGA can offer several hundreds [11] and with much superior sidewall structural quality. This outstanding advantage results in extremely tall and precise microstructures. Sidewall vertical slope can be better than 89.9° and with achievable sidewall roughness of 20 to 30nm, which endows the fabricated structure optical surface quality. Also the possible minimum feature size of LIGA structure can be realized as low as 0.1μm. As a result, LIGA can potentially realize RF and microwave components with high quality and high end performance. For example, several promising high aspect ratio RF MEMS devices have already been fabricated by the TRLabs/University of Saskatchewan MEMS group, including a 2mm high millimeter wave resonator [12], vertical cantilever MEMS variable capacitors [13], and broadband coupled line couplers [14]. In this research, increasing suspended structures to an unprecedented height might mean that the parasitic electromagnetic coupling to the substrate could be almost removed, providing the mechanical robustness permits.

LIGA is a low temperature polymer process. This feature provides LIGA potential compatibility with the CMOS process. Recently, several efforts were made for the integration of LIGA microstructures onto CMOS wafers/chips with the use of Polymethyl Methacrylate (PMMA) or Polydimethyl Siloxane (PDMS) pattern transfer process and molding techniques [5], [15]. One can rationally anticipate that in the near future, a mature CMOS compatible LIGA process could be a reality.

1.5 Research Objectives

The purpose of this research is to explore some advantages of deep X-ray LIGA technology to microwave passive inductor fabrication on the Si substrate. Two kinds of inductors, a square spiral type and a solenoid type, are proposed with structural features considered compatible with typical LIGA processing. The Si substrate situations are set up based on the CMOS/BiCMOS substrate characteristics, thereby exploring the

possibly CMOS compatible LIGA inductor situations. If one can verify LIGA fabricated inductors also exhibit improved RF performance in the simulated CMOS/BiCMOS environment, the value and advantage of LIGA is strengthened. The working frequency band of interest for the investigated inductors in this capacity is from 4 GHz to 12 GHz. Three key parameters of inductors, namely, quality (Q) factor, self resonant frequency (SRF), and inductance (L), are focused on. This dissertation mainly engages software designs, simulations, and analyses of the inductors using Ansoft HFSS™ (version 9.1).

In order to realize the overall goal, the following specific objectives are considered:

1. To further investigate the advantage of LIGA processing, some analysis schemes are considered: for the spiral inductor, two structures, one suspended at 150 μm height, the other touching the substrate for comparison, are developed and investigated. These architectures are particularly well suited for LIGA due to the vertical heights involved, and especially the unprecedented suspension height. For the solenoid inductor, two kinds of structures, one suspended at 150μm, the other touching the substrate are also investigated. Due to the high aspect ratios and non-ninety degree geometrics required, such structures cannot likely be built using surface or bulk micromachining techniques, but are possible using LIGA. Various geometric and physical parameter simulations are conducted for these four structures, in an attempt to reveal LIGA advantages over other MEMS techniques.

2. Optimizing the inductor characteristics, namely, optimizing the Q factors of the inductors and trying to enlarge them as big as possible, and thereby the working frequencies as high as possible. The Si substrate models are limited to one conductive case, CMOS/BiCMOS standard substrate. If one can achieve excellent performance using LIGA under this condition, the value of integrating LIGA with CMOS for these applications is further justified.

1.6 Thesis Outline

This thesis comprises the following chapters:

Chapter 2 first demonstrates general deep X-ray LIGA processes and the recent progresses in integrating the LIGA process with the CMOS technique. Then the electromagnetic mechanisms and lumped equivalent circuits of the air core spiral inductors and solenoid inductors are discussed. The discussion is focused on some key parameters, *Q* factor, Self Resonant Frequency (*SRF*), and inductance.

Chapter 3 presents various published inductor layouts. The previous works in micro-scale inductors are briefly reviewed, especially the recent progress in MEMS inductor design.

Chapter 4 describes the fundamental working principle of the high frequency simulation tool, Ansoft HFSS™. Then the basic design procedures and considerations for the simulation inductor models in terms of HFSS™ environment are explained. Finally, the potential of building LIGA structural inductor on CMOS/BiCMOS substrate are briefly discussed.

Chapter 5 gives the discussions, comparisons, and analysis of the simulation and optimization results.

Chapter 6 concludes this dissertation and describes the possible future work.

2 Principle of LIGA Process and On Silicon Inductor Theory

2.1 Principle of LIGA Fabrication Process

In Chapter 1, the LIGA technique has been briefly introduced. It is necessary to extend this topic in more detail to discuss the subsequent model designs. In the LIGA process, X-rays are used as the lithographic light source because of their short wavelength, which offers higher penetration power into the photoresist materials. The X-rays come from a synchrotron radiation source, which provides high intensity in the hard X-ray spectrum. The short wavelength also allows for high resolution in lithography, at line width of 0.2µm or even possibly lower, and high aspect ratio.

The general process steps are illustrated in Figure 2.1 for producing isolated metal structures on a substrate. The process begins from step (a) by applying a thin metal film layer on the substrate. It is called a "seed layer" and acts as the cathode attracting metal ions to the substrate during electroplating. Then, in step (b), a thick film of X-ray sensitive photoresist is deposited on the surface of the substrate. Often, the employed photoresist is polymethylmethacrylate (PMMA), but other resists are also used. After that, in step (c), the photoresist covered substrate is exposed to the high energy X-ray radiation through a patterned mask. Masking materials, for examples, SiC and Si_3N_4, are transparent to X-rays. A relatively thick film of gold is patterned on the membrane to absorb X-ray transmission and provide the contrast for patterning. X-ray absorption alters the resist chemistry and allows the exposed area to be dissolved in the subsequent development of the photoresist material (see step (d)). After photoresist development, the ensuing three-dimensional photoresist structure is filled with electroplated metal (see step (e)) and the photoresist is subsequently removed via X-ray flood irradiation followed by secondary development to generate a freestanding metal structure. Finally, the seed layer is etched away, typically with hydrofluoric acid and possibly reactive ion etching (RIE) to electrically isolate metal conductors (see step (f)). The demonstrated

processes in Figure 2.1 represent direct X-ray lithography and typically produce best structure quality. When considering mass production and cost reduction, the complete LIGA process can be used to produce structures by hot embossing, injection molding, or pattern transfer, at possibly reduced structural quality.

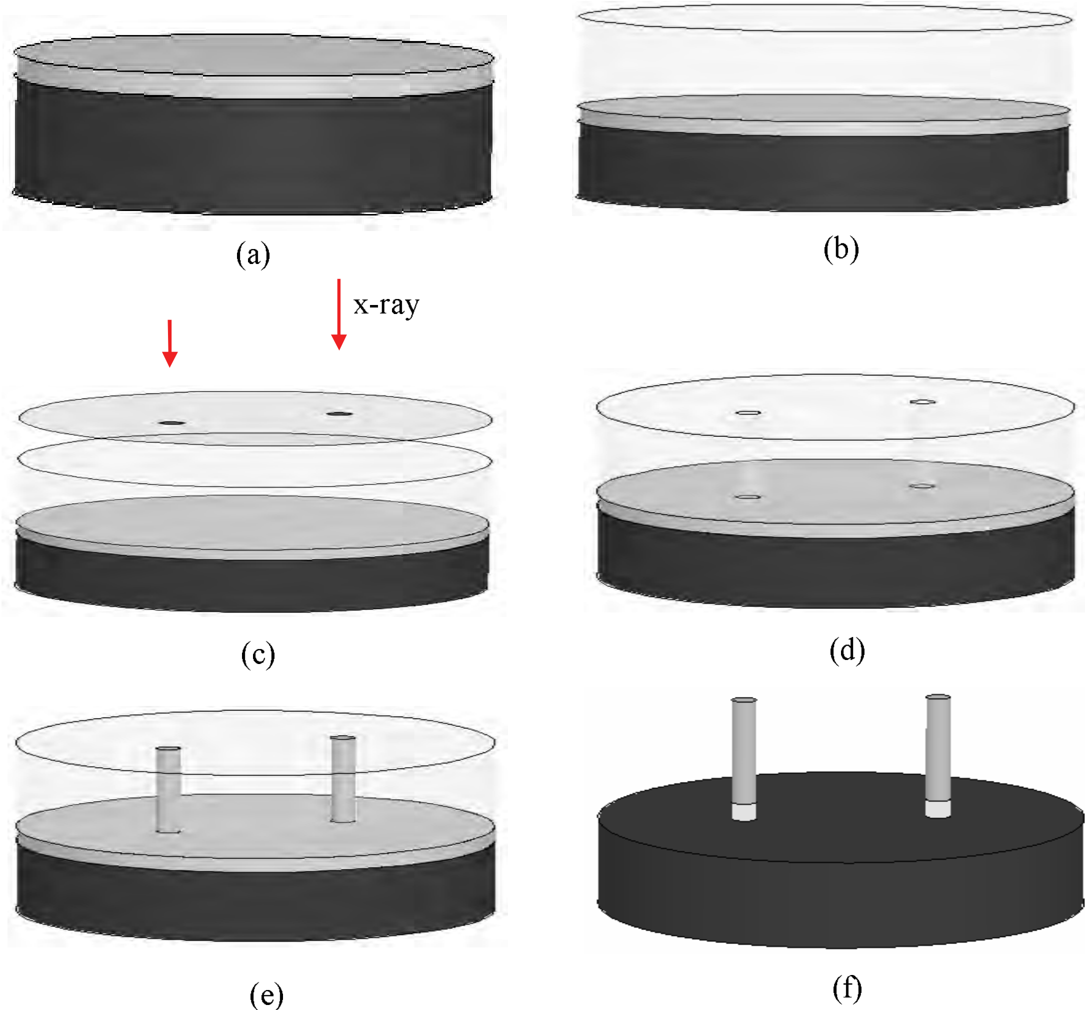


Figure 2.1: LIGA process steps (a) Application of seed layer on substrate; b) Application of photoresist; c) X-ray exposure (lithography); d) Photoresist development after lithography; e) Metal electroplating; f) Removal of photoresist and seed layer

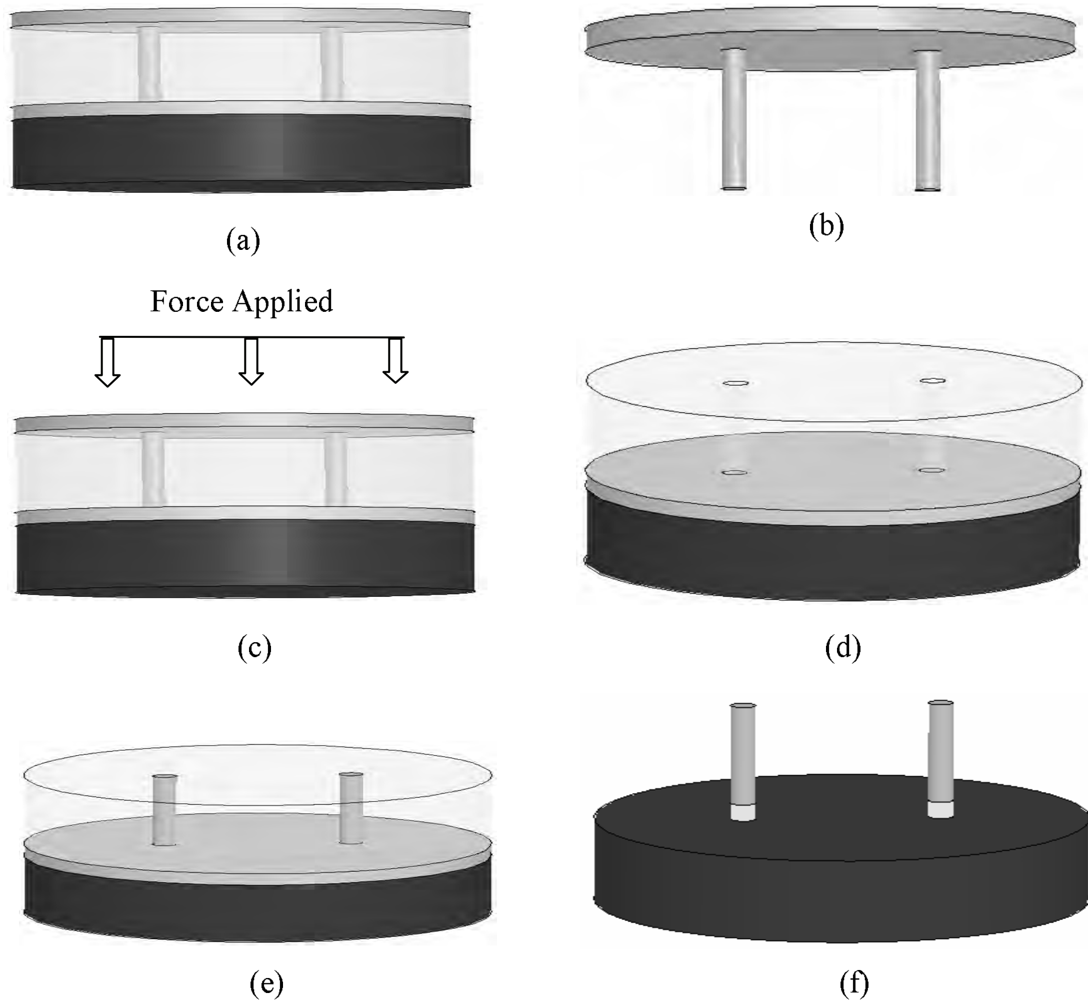


Figure 2.2: LIGA Process with Replication by Hot Embossing: a) Metal overplating into X-ray patterned photoresist; b) Release of metal mold insert; c) Hot embossing; d) Plastic mold; e) Secondary metal deposition; f) Final metal structure

Hot embossing is a mechanical technique and has been transplanted to microstructure fabrication. The summarized hot embossing procedure is illustrated in Figure 2.2 [16]. First, in step (a) and (b), a metal mould insert is created using a process similar to that shown in Figure 2.1, but during the electroplating process, the metal is deliberately overplated to form a metal bridge connecting the metal fillings. This step is called "over plating". Then in step (c), in a controlled temperature and pressure environment, an outside force applied on the metal mould insert forces it into softened plastic applied on a substrate to create the shape complimentary to the mould insert (also in this case, the

substrate has been applied with a thin layer of metal seed since final metal structures are desired). When the metal mould insert is removed, the plastic structures illustrated in step (d) result (in reality there may be a thin plastic layer on the substrate which could require further etching). Finally, a second electroplating is conducted in the created plastic mould (step (e)). This is also called “secondary metal definition”. This step is performed in the context of fabricating metal parts and may not be necessary in other cases. Finally, the plastic and seed layers are stripped to obtain the final microstructure. The LIGA replication techniques allow relatively inexpensive fabrication of parts precisely replicating the shape and size of the original X-ray-patterned part.

Currently, most developed LIGA processes use Nickel (Ni) as the metal material. Ni has good mechanical structural properties, including low internal stress during electroplating of tall structures. Copper, which is a better electrical conductor, is also being developed at for instance, Sandia National Lab, USA, but is less mature. Because copper is common in the CMOS process, in order to explore the advantage of the possible combination between LIGA and CMOS, in most of the simulation and analysis occasions, copper is used as the objective metal.

A pattern transfer technique for the post-IC integration of LIGA microstructures onto CMOS chips has been proposed [5]. Figure 2.3 shows a simplified pattern transfer process flow for the integration of a LIGA HARM (high aspect ratio metal) onto a CMOS chip using PDMS replication and CMOS-compatible electroplating techniques. The process starts with a Ni master mold, in this case, an array of cylindrical posts, on a stainless steel substrate (step (a)). Then the corresponding PDMS mold can be achieved using various techniques such as embossing and molding, which is shown in (step (b)). While the PDMS mold is being fabricated, the test chip is being attached on a Si wafer and then a metal seed layer is being deposited atop. To fasten the LIGA HARM onto the test chip, an adhesive polyamide layer at 3μm must be spin-coated between the test chip and the PDMS mold during the process. Then in step (c), the generated PDMS mold is trimmed into a smaller piece and aligned/attached to the test chip under the contact aligner. After that, the plasma etching has been continually carried out to remove the

adhesive PI layer to expose the seed layer for electroplating [17]. Subsequently, the electroplating is conducted to create metallic HARM on the testing circuit chip. Finally, after removing PDMS mold, adhesive PI layer, and the seed layer using different etching processes, the transferred metallic microstructure is generated (step (d)).

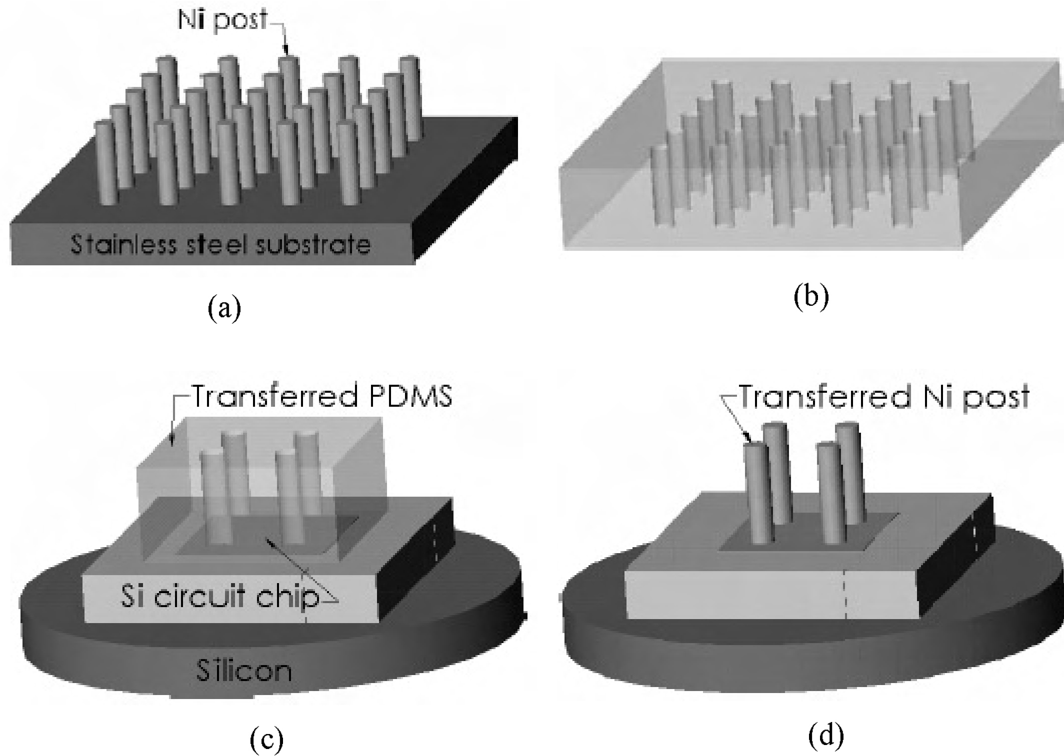


Figure 2.3: The process flow for the pattern transfer of a LIGA HARM [5]: (a) LIGA – processed metallic master mold; (b) The replicated PDMS mold; (c) PDMS mold on a Si circuit chip with metallic seed layer and adhesive PI layer; (d) The on chip transferred LIGA HARM.

This pattern transfer process has already been applied to air-suspended spiral copper inductor fabrications in the lab environment [5]. The metallic master mold in this capacity is a double-layered structure with 45μm thick coil structures at the bottom and 45μm thick via structures on top, which can be generated using multi-exposure LIGA process (see section 3.2.2). Accordingly, a double-layered PDMS mold is generated. After the replicated PDMS is attached to the test chip, two steps of electroplating are needed to be conducted. The first step is to fill up the bottom trenches for via posts.

After that, a second seed layer is deposited in the top PDMS trenches, and the unnecessary seed layer on the top PDMS surface should be removed. Then the second step electroplating is carried out to fill up the top trenches of the PDMS mold to generate the copper coil structures. The simplified process sequence is shown in Figure 2.4.

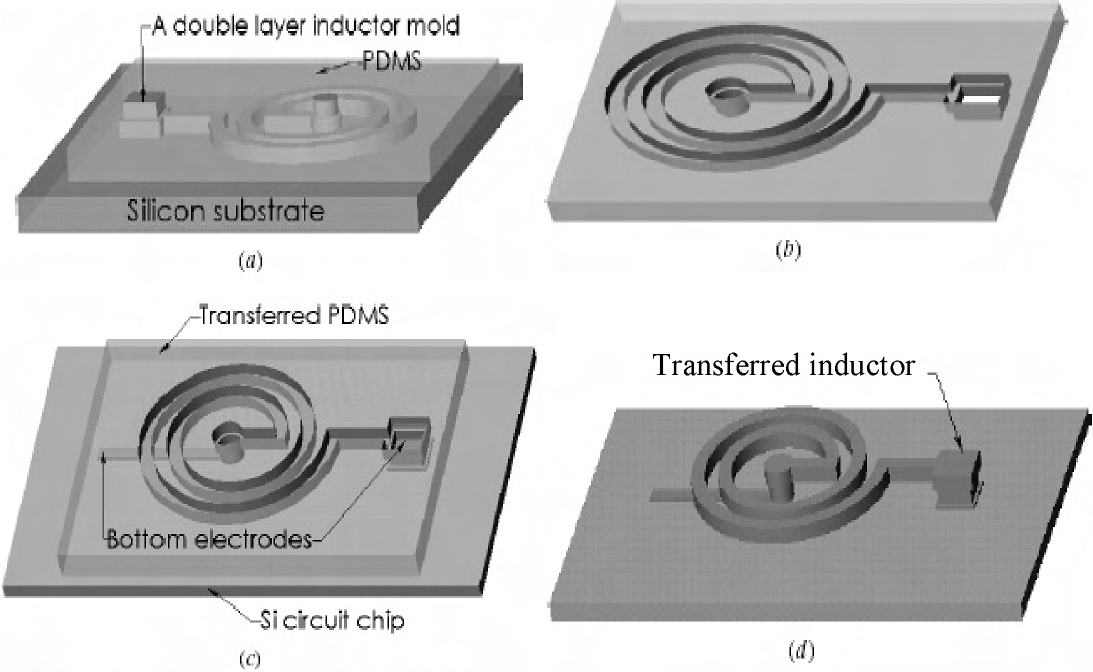


Figure 2.4. The PDMS-based pattern transfer process sequence for a spiral inductor [5]: (a) Spin-coating of PDMS; (b) Peeled-off PDMS; (c) PDMS mold on a CMOS circuit chip with bottom electrodes, metallic seed layer, and adhesive PI layer; (d) Transferred metallic inductor on a chip.

2.2 Inductor Principle

Inductors store magnetic energy. The self inductance originates from the current in the inductor. According to one of Maxwell's Equation (equation 2.1a), electrical current or changing electric field induces the magnetic field. Any change in a current also induces the change in the generated magnetic field.

$$\nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} \quad (2.1a)$$

$$\vec{D} = \varepsilon \vec{E} \quad (2.1b)$$

$$\vec{B} = \mu \vec{H} \quad (2.1c)$$

where $\vec{H}$ is the magnetic field intensity, $\vec{J}$ is the free current density, $\vec{D}$ is the electric flux density, $\vec{E}$ is the electric field intensity, $\vec{B}$ is the magnetic flux density, ε is the permittivity, and μ is the permeability. Considering an arbitrary closed-circuit formed by conductors as shown in Figure 2.5 (a), the magnetic flux of this circuit is defined as the magnetic field crossing the cross-sectional area of the circuit

$$\psi = \oint_S \vec{B} \cdot d\vec{S} \quad (2.2)$$

The origin of the magnetic field $\vec{B}$ comes from the circuit itself since there is no other current surrounding. Thus, the self-inductance of the closed conductor can be defined as

$$L = \frac{\psi}{I} \quad (2.3)$$

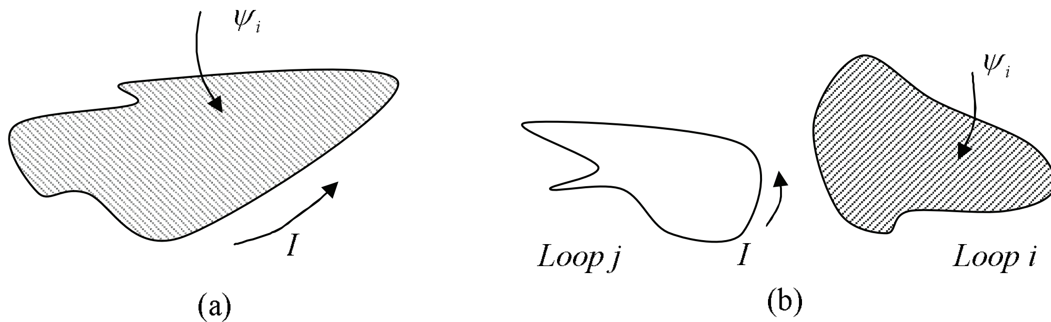


Figure 2.5: (a) An independent current loop (b) A magnetically coupled pair of loops. Current only exists in loop *j*

where I is the current flowing in the conductor. Now we consider two closed conductor loops in Figure 2.5 (b). Assuming there is current flowing in loop j and we measure the impinging flux from j to loop i, the mutual inductance can be defined as

$$M_{ij} = \frac{\psi_i}{I_j} \tag{2.4}$$

where

$$\psi_i = \oint_{S_i} \vec{B}_i \cdot d\vec{S} \tag{2.5}$$

and from Faraday's Law, the voltage induced on a loop is related to the flux

$$V = \frac{d\psi}{dt} = L\frac{dI}{dt} \; . \tag{2.6}$$

The magnetic energy stored by the inductor is given as follows

$$W_m = \frac{1}{2}LI^2 \tag{2.7}$$

and the total magnetic energy stored in a physical inductor can also be calculated as [18]

$$W_m = \frac{1}{2}\int_V \vec{B} \cdot \vec{H} dV \tag{2.8}$$

where V is the volume of interest. By equating the equation (2.7) and (2.8), one can obtain the inductance.

The general equation for an arbitrary geometry inductor can be expressed as

$$L_T = L_O + \sum M \tag{2.9}$$

Where L_O is the self inductance, and the $\sum M$ is the totaling of mutual inductances.

2.3 Quality Factor of the Inductor

Generally speaking, the complex power delivered to a conductor at the frequency ω, P, is [18]

$$P = \frac{1}{2}\oint_S \overline{E} \times \overline{H}^* \cdot d\overline{S} = P_l + 2j\omega(W_m - W_e) \tag{2.10}$$

where P_l is the average power dissipated by the conductor. As well, W_m and W_e represent the time average of the stored magnetic and electric energy, respectively. The input impedance can thus be given as follows [18]

$$Z_{in} = R + jX = \frac{V}{I} = \frac{VI^*}{|I|^2} = \frac{P}{\frac{1}{2}|I|^2} = \frac{P_l + 2j\omega(W_m - W_e)}{\frac{1}{2}|I|^2} \tag{2.11}$$

If $W_m > W_e$, the device is inductive, i.e., an inductor.

Quality factor (Q) is a key parameter to passive devices. The Q is defined as [19]

$$Q = 2\pi \cdot \frac{energy\ stored}{energy\ loss\ in\ one\ oscillation\ cycle} \tag{2.12}$$

Actually, equation (2.12) applies to all the passive devices. But the exact meanings for different devices are subtly different. For a LC tank, the energy stored is the sum of the average magnetic and electric energies. The energy stored in a (lossless) LC tank is a constant and oscillates between magnetic and electric forms. It is also equal to the peak magnetic energy, or the peak electric energy. For a lossless LC tank, Q is infinite. In contrast, for an inductor, according to its definition, only the magnetic energy is of interest. Any stored electric energy arising from the inevitable parasitic capacitances in a real inductor is counterproductive. Therefore, the inductor Q is proportional to the net magnetic energy stored, which is equal to the difference between the peak magnetic and electric energies and given as

$$Q = 2\pi \cdot \frac{peak\ magnetic\ energy - peak\ electric\ energy}{energy\ loss\ in\ one\ oscillation\ cycle} = 2 \cdot \omega \cdot \frac{(W_m - W_e)}{P_l} \tag{2.13}$$

When self-resonance occurs, the peak magnetic and electric energies are equal. At this point, Q vanishes. Above the self-resonant frequency, Q becomes negative because the net capacitive energy emerges after the balance between the peak magnetic and electric energies.

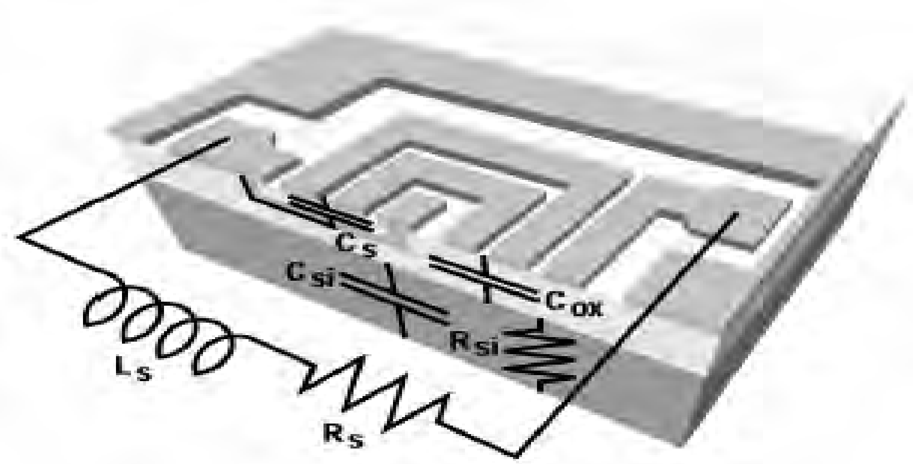
2.4 Physical Lumped Equivalent Model and Loss Mechanism

2.4.1 On Silicon Spiral Inductor Lumped Model and Loss Mechanism

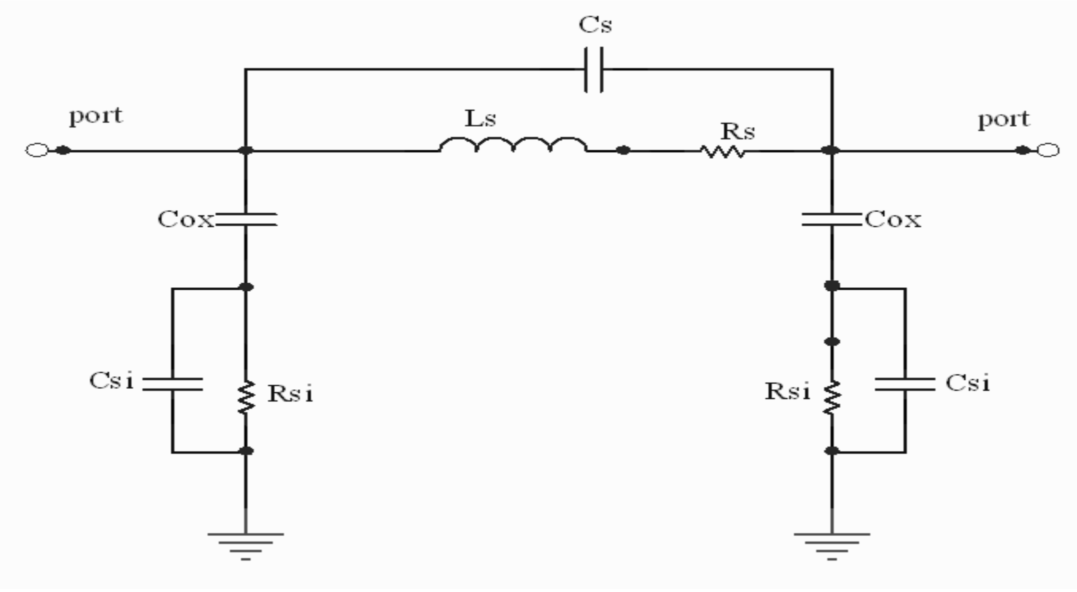
Most of the applicable spiral inductors are square inductors since the photolithographic masks for orthogonal or circular inductors are harder to generate. However, for a circular coil, the required conductor length is shorter for achieving the given inductance value. In consequence, the parasitic resistance and capacitance of the Si substrate are comparably smaller, which results in the higher $Q_{max.}$ In this dissertation, the focus is on square inductor designs due to the above practical constraint.

Since the inductor is to store magnetic energy only, the inevitable resistance and capacitance in an inductor are considered parasitics. The parasitic resistances dissipate energy through ohmic loss while the parasitic capacitances store electric energy. Compared with full electromagnetic field analysis, for instance, as performed by HFSS™ [20], or other partial-element-equivalent-circuit (PEEC) based solvers, a lumped equivalent circuit model dramatically reduces analysis complexity. The lumped-element model of a spiral inductor on silicon [21] is shown in Figure 2.6. It has been extensively used and quoted nowadays because of its simplicity and explicitness. Although from the accuracy viewpoint, it cannot replace HFSS and PEEC methods in simulations, it is more straight-forward for the qualitative theoretical analysis. The electrical characteristics of the spiral coil and the underpass are represented by the inductance L_s, the series resistance R_s, and the C_s, which is the combination of the inter-wire capacitive coupling and the overlap capacitive coupling between the spiral and the underpass. The resistance R_s is frequency–dependant due to the skin effect and the proximity effect. The skin effect depicts an increased current density near the conductor surface arising from an internal magnetic field generated by the original high frequency current. As a contrast, the proximity effect describes the changes in current density

induced by the magnetic field from neighbouring conductors. Skin effect and proximity effect are additive and cannot easily be distinguished. These two effects are also called current crowding effects. High frequency leakage current effect from the spiral to the silicon substrate is modeled by the oxide capacitance C_{ox}. The parasitic capacitance and resistance of the silicon substrate are modeled by C_{si} and R_{si} (the slight asymmetry between the two ports due to the presence of the return underpass has been neglected).



(a)



(b)

Figure 2.6: (a) 3-D view of a spiral inductor; (b) Lumped-element equivalent model of a spiral inductor [21]

Note that the substrate is assumed grounded and it is also modeled in Figure 2.6. There are eddy currents in the substrate providing the substrate resistivity is low, as in the case of Si. They create a magnetic field to weaken the original field of the inductor coil. Consequently, the inductance L_s is reduced. In the author's opinion, the lumped model in Figure 2.6 can be improved into the lumped model in Figure 2.7. The inductance L_s is weakened due to the parasitic transformer M. The substrate loss is modeled by two $R_{si'}$, two R_{sip}, and one R_{sub}. The substrate capacitive parasitics is modeled by two C_{ox}, two C_{sip}, two C_{si}, and two C_{oxp}. Among them, the C_s, L_s, and R_s represent the intrinsic inductor. The two C_{oxp}, two C_{sip}, and two R_{sip} model the port distributed effects. In contrast to other components in Figure 2.7, the port modeled components are very small due to their comparably tiny physical size and thus can be ignored. To the author's knowledge, the mechanisms of M and R_{sub} have rarely been deeply investigated to date, and moreover, the transformer effect is very weak compared with L_s. In this thesis, the model in Figure 2.6 is sufficient for qualitative analysis and understanding of the effects later demonstrated using full 3D EM simulations. The influence of R_{sub} and two $R_{si'}$ are included in the two R_{si} in the Figure 2.6 model. The individual lumped model components in Figure 2.6 are further described in the following sections.

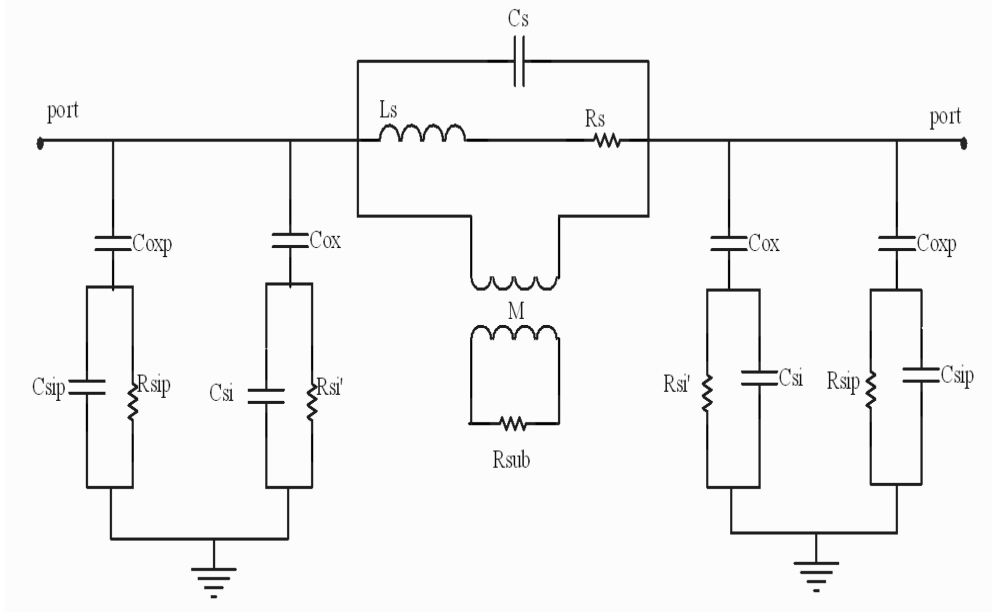


Figure 2.7: Lumped-element equivalent model of a spiral inductor with extra elements

Series Inductance L_s

As mentioned in Section 2.2, the general inductance of the inductor consists of the self inductance of the coil and all mutual inductances between pairs of conductors. The spiral inductance analysis can start from elementary single and two wire sections. The total inductance of the spiral is the sum of the self and mutual inductances of the wires that comprise it. An approximation for the DC (Direct Current) self inductance for a thin film straight conductor with rectangular cross-section is given by Greenhouse [22]

$$L = 0.002 \cdot l \cdot \left[\ln\left(\frac{2 \cdot l}{a+b}\right) + 0.50049 + \frac{(a+b)}{3 \cdot l} \right] \tag{2.14}$$

where L is the inductance in micro henries; l is the conductor length in centimetres; a and b are the rectangular dimensions of the cross-section of the conductor.

The mutual inductance between two parallel wires is a function of the length of the conductors and of the GMD (Geometric Mean Distance) between them. It can be denoted as

$$M = 2lC \tag{2.15}$$

where M is the mutual inductance in nanohenries (nH), l is the wire length in centimetres (cm), and C is the mutual inductance parameter, which is expressed as [22]

$$C = \ln\left[\frac{l}{GMD} + \sqrt{1 + \left(\frac{l}{GMD}\right)^2}\right] - \sqrt{1 + \left(\frac{GMD}{l}\right)^2} + \frac{GMD}{l}, \tag{2.16 a}$$

where GMD can be calculated using

$$\ln GMD = \ln D - \frac{W^2}{12D^2} - \frac{W^4}{60D^4} - \frac{W^6}{168D^6} - \frac{W^8}{360D^8} - \frac{W^{10}}{660D^{10}} - \cdots \tag{2.16 b}$$

and W and D are the wire width and pitch in cm, respectively. Actually, GMD can be approximated as the pitch of the inductor wires [22], which is shown in Figure 2.8. The relationship between the self and mutual inductance is given as follows [21]

$$M = k\sqrt{L_1 L_2} \quad (2.17)$$

where L_1 and L_2 are the self inductances of the two wires, and k is the mutual coupling coefficient. Narrower space enlarges the mutual inductance since the magnetic coupling is enhanced. Also the metal thickness influences the inductance value.

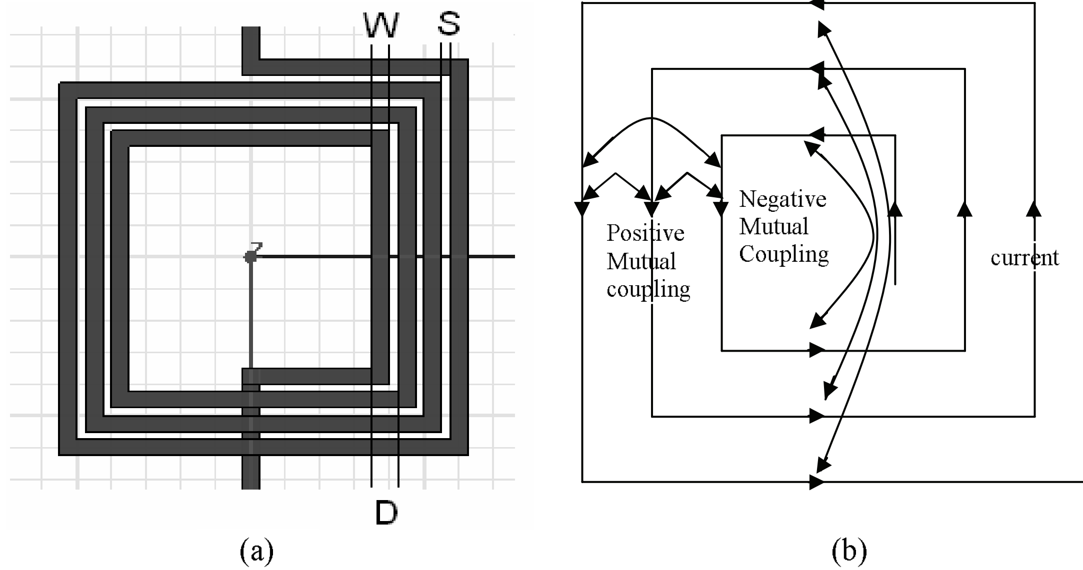


Figure 2.8: (a) Spacing S, line width W, and line pitch D=S+W of a spiral inductor; (b) Positive and negative mutual coupling illustration in a spiral inductor

Greenhouse developed a good method to estimate the planar rectangular spiral inductance [22]. The overall coil inductance is expressed in Equation (2.18) and demonstrated in Figure 2.8 (b).

$$L_S = L_O + \sum M_+ - \sum M_- \quad (2.18)$$

Briefly speaking, it is equal to the summation of self inductance of each wire segment and the positive and negative mutual inductances between all possible wire segment pairs. The mutual inductance between two wires depends on their angle of intersection, length, and separation. Two mutually perpendicular wires have no mutual inductance because of the magnetic flux uncoupling. The mutual inductance is positive if the currents in the two wires are in the same direction and negative conversely.

Series Resistance R_s

When the inductor operates at high frequencies, due to skin effect and proximity effect, the current density in its metal wire is non-uniform along the width and thickness of the conductors (see Figure 2.9). Note that Figure 2.9 is just a conceptual demonstration. The practical distribution of the eddy currents depends on the geometry of the conductor and its orientation to the actuating time-varying magnetic field. Therefore, it is not as simple as the figures shown in Figure 2.9.

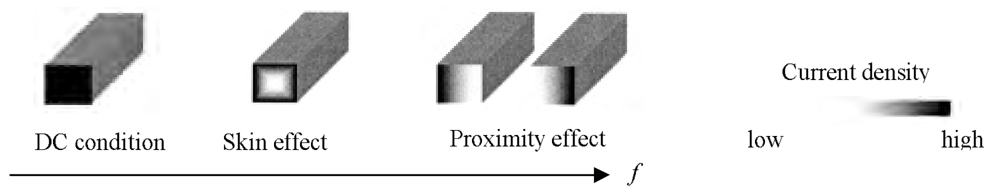


Figure 2.9: Illustration of skin effect and proximity effect in terms of straight wires with rectangular cross-section

Because the spiral inductor has a multi-conductor structure, eddy currents can potentially be caused by both proximity and skin effects. Eddy current losses contribute to the ohmic losses. Skin effect is from the magnetic field of the metal trace, whereas the proximity effect arises from the magnetic fields of nearby conductors. The proximity effect also contributes to the current distribution in a conductor, leading to the strongest magnetic field in the innermost turn of the spiral. The eddy currents resulting from the skin effect and the proximity effect induce their own magnetic field to weaken the original field. Therefore, the eddy currents reduce the net current flow in the conductor and hence increase the total resistance, pushing current to the outer layers (“skin”) of the conductors. A parameter called skin depth (δ) is crucially related to this phenomenon. It describes the “depth of penetration”, the degree of penetration by the electric current/field and magnetic flux into the surface of a conductor at high frequencies. The magnitude of the fields and the current decrease exponentially with penetration into the conductor, and δ has the significance of the depth at which the fields and current have decreased to $1/e$ (about 36.9%) of their values at the surface [18]. As well, the phases of the current and fields lag behind their surface counterparts by x/δ radian at the depth x into the conductor [18]. The severity of the eddy current effect is determined by the ratio

of skin depth to the conductor thickness. The eddy current effect is negligible only if the skin depth is much greater than the conductor thickness. Normally, the skin depth is defined as [18]

$$\delta = \sqrt{\frac{\rho}{\pi\mu f}} = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{2.19}$$

where ρ, μ, ω, σ and f denote the resistivity of the conductor in ohm·m, permeability in H/m, angular frequency of the signal in the conductor in rad/s, conductivity of the conductor in Siemens/m, and frequency in Hz, respectively.

From the above discussion, one can see the current distribution inside a spiral inductor is complicated and non-uniform, even for a single trace segment (see Figure 5.3). In contrast to skin effect, the proximity effect inside the spiral inductor is very small and is often ignored in lumped modeling [21]. Also, the wire segments can be treated as microstrip transmission lines. For the spiral inductor case, the current at high frequencies concentrates to one surface of the wire [21]. Based on these assumptions, one can see the current gradient resulting from the skin effect is in the direction away from the surface. Thus, the current density (J in A/m^2), which is simplified to attenuate as a function of the distance (x) away from the inductor metal surface, can be roughly expressed as

$$J = J_O \cdot e^{-x/\delta} \tag{2.20}$$

Where J_o is the current density on the surface. The current (I in Ampere) is equal to the integration of J over the wire cross-sectional area. Since J only changes in the x direction, I can be calculated as

$$I = \int J \cdot dA = \int_0^t J_o \cdot e^{-x/\delta} \cdot w \cdot dx = J_o \cdot w \cdot \delta \cdot (1 - e^{-t/\delta}) \tag{2.21}$$

where t denotes the thickness of the wire, and w is the wire width. From (2.21), the effective thickness, t_{eff}, can be defined as

$$t_{eff} = \delta \cdot (1 - e^{-t/\delta}) \tag{2.22}$$

In consequence, the series resistance R_s, can be approximated as

$$R_S = \frac{\rho \cdot l}{w \cdot t_{eff}} = \frac{\rho \cdot l}{w \cdot \delta \cdot (1 - e^{-t/\delta})} \tag{2.23}$$

where ρ and l represent the resistivity and length of the wire.

Parallel Capacitance C_s

The parasitic capacitive coupling between input and output ports of the inductor includes the cross-talk between adjacent turns and the overlaps between the spiral and underpass. This parasitic parallel capacitance can be modeled as C_s. it allows the signal to flow directly from the input to output port without passing the inductor wires. Since the crosstalk capacitances can be reduced by increasing the gap between the turns, and the adjacent turns are almost equi-potential, the effect of the crosstalk capacitances can be negligible. In contrast, because of the larger potential difference between the spiral and the underpass [23], [24], the C_s is mostly contributed by the overlap capacitances. Practically, in most cases, C_s can be modeled as the sum of all overlap capacitances, which is

$$C_S = n \cdot w^2 \cdot \frac{\varepsilon_{ox}}{t_{oxM1-M2}} \tag{2.24}$$

where n is the number of overlaps, w is the spiral line width, ε_{ox} is the oxide dielectric permittivity, and $t_{oxM1-M2}$ is the oxide thickness between the spiral and the underpass.

Substrate Parasitics and Losses

As shown in Figure 2.6, the characteristics of the spiral inductor structures on oxide on silicon can be modeled by a three-element network consisting of C_{ox}, R_{si}, and C_{si}. The physical origin of R_{si} is the silicon conductivity which is mainly determined by the majority carrier concentration. C_{ox} and C_{si} model the oxide capacitance and the parasitic

capacitive effects, respectively, arising from the silicon semiconductor at high frequencies. C_{ox} is the oxide capacitance between the inductor metal traces and the substrate, whereas C_{si} represents the high frequency capacitive effects inside the substrate. Usually the substrate is tied to ground through vias to metallization that is grounded externally (off-chip). Ultimately speaking, at RF and microwave frequencies, the resistance and the finite response time of the substrate to the applied fields cause the potential throughout the substrate to exhibit a non-uniform distribution relative to the external ground applied to the circuits. This results in C_{si}. The lateral dimensions of a spiral inductor are normally comparable to the silicon substrate thickness and are much larger than the oxide thickness. The substrate capacitance and resistance are approximately proportional to the area occupied by the inductor and can be roughly expressed as

$$C_{ox} = \frac{1}{2} \cdot l \cdot w \cdot \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.25}$$

$$C_{si} = \frac{1}{2} \cdot l \cdot w \cdot C_{sub} \tag{2.26}$$

$$R_{si} = \frac{2}{l \cdot w \cdot G_{sub}} \tag{2.27}$$

where C_{sub} and G_{sub} are the capacitance and conductance per unit area for the silicon substrate. The area of the spiral is equal to the product of the spiral length (l) and width (w). Because the substrate parasitics are assumed to be distributed equally at the two ends of the inductor, Equations (2.25)-(2.27) need to have a factor of two accounting for this concern. C_{sub} and G_{sub} are substrate doping dependant and extracted from measurement results. They do not vary significantly over the substrate if the substrate is uniformly doped. Therefore, the R_{si} and C_{si} only scale with l and w. ε_{ox} and t_{ox} represent the dielectric constant and thickness of the oxide layer between the inductor and the substrate, respectively.

Normally, in CMOS technologies, the silicon substrate resistivity is extremely low at around 0.015 ohm·cm for logic process, and is around 10 ohm·cm for the mix-mode process. For the bipolar process or BiCMOS processes, it is typically 10 ohm·cm to 30 ohm·cm [25]. In this research, the substrate resisitivity is universally set up as 10ohm·cm for both CMOS mix-mode and BiCMOS cases. The conductive nature of the silicon substrate leads to various losses, which convert the electromagnetic energy into heat in the substrate volume. Figure 2.10 physically illustrates the mechanisms of the substrate induced losses for a spiral inductor. Generally speaking, there are two main loss mechanisms in the substrates. First, electric energy is coupled to the substrate in terms of displacement current because of the potential difference between the inductor coil and the substrate. This current flows through C_{ox} to nearby grounds. These currents flow vertically or laterally, but are perpendicular to the spiral traces, and are curl free (unlike the eddy current, there is no circulation in this displacement current, that is, $\nabla \times I=0$). This displacement current movement is two ways: The incident currents pass through C_{ox} from some particular traces to the substrate. Also, there are reflecting currents from the substrate returning back to the inductor metal traces via the C_{ox}. This is also the nature of high frequency current. Second, induced currents circulate in the substrate due to the time-varying magnetic field $\vec{B}$ penetrating the substrate. According to Maxwell's Equation [18],

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}, \tag{2.28}$$

this magnetic field gives rise to time-varying circular electric field $\vec{E}$ which induces substrate eddy currents. These eddy currents flow parallel to the device segments.

Radiation always occurs at the frequencies where the device physical dimensions approach the wavelength at the frequencies of propagation in the medium of interest. That is why one can safely ignore the electromagnetic radiation loss into the air because even at very high frequencies, say, 100 GHz, the wavelength in free space is still 3 mm, which is considerably larger than the dimensions of the devices discussed in this thesis.

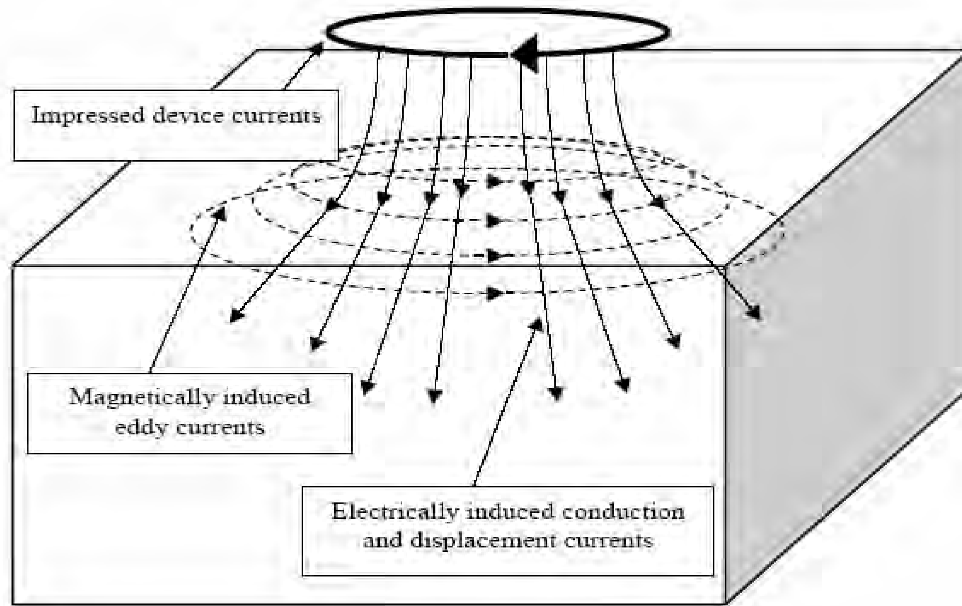


Figure 2.10: Schematic representation of substrate currents. Eddy currents and electrically induced currents are represented by the dashed lines and the solid lines, respectively [6].

2.5 Spiral Inductor Quality Factor Frequency Analysis

Although the inductor is a two port passive component, when expressing the inductor properties using simulation or measurement, a standard method is to ground one port because the measured parameters more directly relate to the inductance (L) and Q. In this way, the unnecessary complexity in the analysis is avoided and meantime the inductor characteristics is still preserved [26]. However, from Figure 2.6, one can see the grounding of one port in the circuit model, say port 2, removes the parasitic effect at port 2, namely, C_{ox}, C_{si}, and R_{si}. However in practice, grounding one port does not really short these out since the real parasitics are distributed and not lumped at the port, and therefore has little influence on the performance of the inductor. However, the one port grounding does introduce error or inaccuracy between actual measurement and the lumped model. The lumped model is still useful for qualitative analysis and understanding, but a model which represents distributed effects, is more appropriate for

simulations. HFSS™ models distributed effects, and is a more realistic analysis tool with respect to the actual measurement. If one port of the lumped equivalent model in Figure 2.6 is grounded, one can transform the model into the one in Figure 2.11 (a), and it can be simplified to Figure 2.11 (b). Based on the one port short approach and Figure 2.11 (b), the Q factor in Equation (2.13) can be further expressed in terms of admittance, Y, (or impedance, Z, parameters) as shown in Equation (2.29) [27], [28]

$$Q = 2 \cdot \omega \cdot \frac{(W_m - W_e)}{P_l} = \frac{\text{Im}(P)}{\text{Re}(P)} = -\frac{\text{Im}(Y_{11})}{\text{Re}(Y_{11})} = \frac{\text{Im}\left(\frac{1}{Y_{11}}\right)}{\text{Re}\left(\frac{1}{Y_{11}}\right)} \tag{2.29}$$

where Y11 is the input admittance at one port.

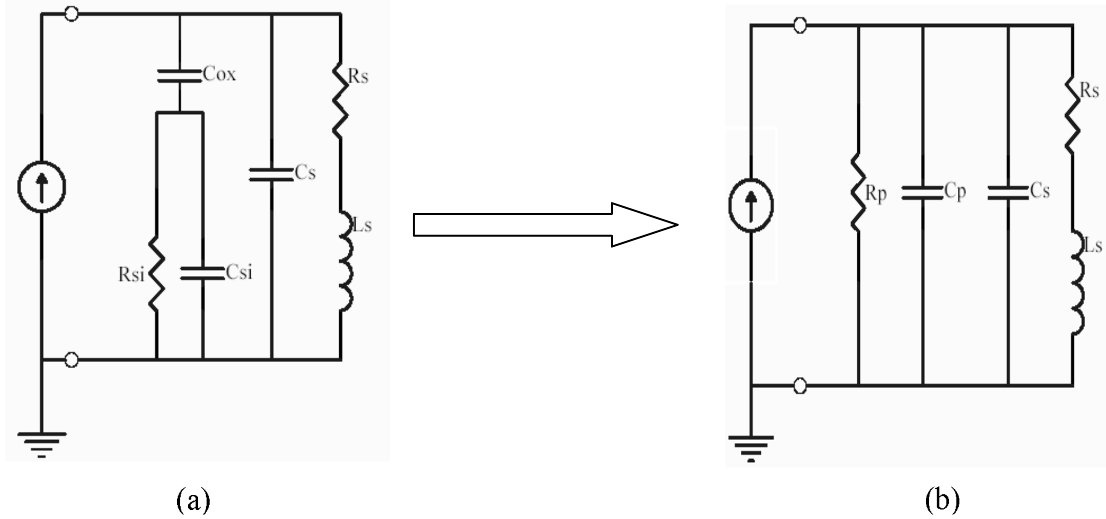


Figure 2.11 : Simplified lumped equivalent circuit models

Y11 can be determined directly from Figure 2.11 (b) as

$$Y_{11} = \left(\frac{1}{R_P} + \frac{R_S}{R_S^2 + \omega^2 L_S^2}\right) + j\omega \cdot \left(C_P + C_S - \frac{L_S}{R_S^2 + \omega^2 L_S^2}\right) \tag{2.30 a}$$

where

$$R_P = \frac{1}{\omega^2 C_{ox}^2 R_{Si}} + R_{SI} + \frac{2R_{Si}C_{Si}}{C_{ox}} + \frac{R_{Si}C_{Si}^2}{C_{ox}^2} \quad (2.30\text{b})$$

$$C_p = C_{ox} \cdot \frac{1+\omega^2(C_{ox}+C_{Si})C_{Si}R_{Si}^2}{1+\omega^2(C_{ox}+C_{Si})^2 R_{Si}^2} \quad (2.30\text{c})$$

and subsequently Q from (2.29) as:

$$Q = -\frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} = \frac{\omega \cdot [L_S R_P - R_P(R_S^2 + \omega^2 L_S^2)\cdot(C_P + C_S)]}{R_S^2 + \omega^2 L_S^2 + R_S R_P} \quad (2.30\text{d})$$

From the energy approach, the energies and resonant frequency ω_0 can be obtained as [26]

$$E_{peak\ magnetic} = \frac{V_O^2 L_S}{2\cdot[(\omega L_s)^2 + R_S^2]} \quad (2.31\text{a})$$

$$E_{peak\ electric} = \frac{V_o^2 (C_S + C_P)}{2} \quad (2.31\text{b})$$

$$E_{loss\ in\ one\ oscillation\ cycle} = \frac{2\pi}{\omega}\cdot\frac{V_O^2}{2}\cdot[\frac{1}{R_P} + \frac{R_S}{(\omega L_S)^2 + R_S^2}] \quad (2.31\text{c})$$

V_o is the peak voltage across the R_s/L_s branch or C_p branch. By substituting the (2.31a)-(2.31c) into (2.29), Q can be determined as

$$Q = \frac{\omega L_s}{R_s}\cdot\frac{R_p}{R_p + [(\frac{\omega L_s}{R_s})^2 + 1]R_s}\cdot[1 - \frac{R_s^2(C_s + C_p)}{L_s} - \omega^2 L_S(C_s + C_p)]$$

$$= \frac{\omega L_s}{R_s}\cdot substrate\ loss\ factor \cdot self-resonance\ factor \quad (2.31\text{d})$$

Which is equivalent to Equation (2.30d), showing Q can be determined directly from measurement of Y-parameter. At low frequencies, $Q \approx \omega L_s/R_s$. Forcing Q to zero, ie.,

forcing the self-resonance factor to zero, one can get the self resonance frequency (*SRF*), the frequency at which self-resonance occurs. It can be expressed as

$$\omega^2 = \frac{1}{L_s(C_s + C_p)} - \frac{R_s^2}{L_s^2} \tag{2.32}$$

For a suspended spiral inductor, the lumped model requires some modifications. First, if the Equation (2.25) is still used for C_{ox} definition, the dielectric constant should be a combination of ε_{ox} and ε_o (dielectric constant in the air). Actually, the C_{ox} in this capacity can be equivalently treated as a combination of two capacitors, C_{oxd} in series with C_{air}, which is shown in Figure 2.12. C_{oxd} models the oxide capacitance resulting from the oxide isolation and is comparable to $\frac{1}{2} \cdot l \cdot w \cdot \frac{\varepsilon_{ox}}{t_{ox}}$. C_{air} models the capacitive effect resulting from the air suspension and is comparable to $\frac{1}{2} \cdot l \cdot w \cdot \frac{\varepsilon_o}{t_{suspension}}$, where $t_{suspension}$ is equal to the defined suspension height.

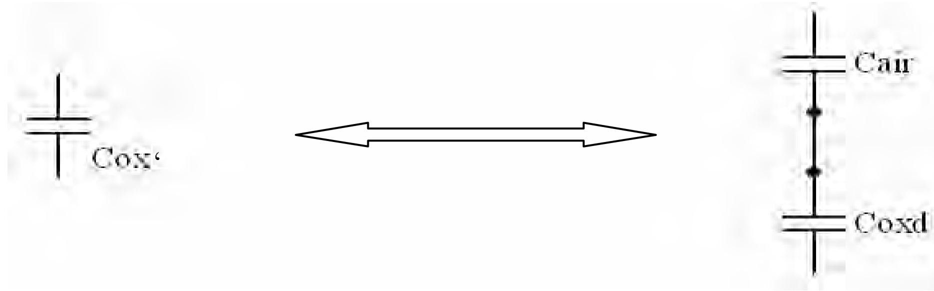


Figure 2.12: The equivalent *Cox'* of a suspended spiral inductor

The effective $C_{ox'}$ can be obtained from $\frac{1}{C_{ox'}} = \frac{1}{C_{oxd}} + \frac{1}{C_{air}}$. Therefore, the $C_{ox'}$ is greatly reduced in contrast to the substrate touching counterpart ($C_{ox'} < C_{air} << C_{oxd}$). Also, for the similar reason, the C_s in the suspended case is decreased based on Equation (2.24). Substituting $C_{ox'}$ into Equation (2.30b), one can see the R_p can be increased, possibly to a very large value if the suspension height is greater than several tens of microns. From the substrate loss factor term in Equation (2.31d), one can see the larger the R_p, the larger the substrate loss factor (closer to unity) and the less impact the substrate has on

Q. From Equation (2.30c), it is hard to judge whether the C_p goes up or not. However, Figure 2.11 shows that C_p is just a total equivalent capacitance of the simple combination of R_{si}, C_{si}, and C_{ox}. Normally, in the planar spiral coil structure, $C_{ox} >> C_s$ and C_{si} [29], that is, C_{ox} dominates in the three component combination. When C_{ox} is significantly reduced to $C_{ox'}$ due to the suspension and C_{si}/R_{si} keep intact, the total equivalent capacitance C_p will definitely decrease. Substituting this result into Equation (2.31d), one can see the self-resonance factor could also be greatly improved (closer to unity) due to the decreasing of C_p and C_s after suspension. Due to the same reason, the *SRF* is also expected to be pushed higher according to Equation (2.32). By suspension, the two loss factors are both improved. Thus, the overall high frequency property is improved.

Generally, Equation (2.31d) shows the loss mechanism of the spiral inductor at high frequencies is combination of substrate loss factor and self-resonance factor. Ultimately speaking, the self-resonance factor is also a type of substrate loss factor because in the equation, the substrate parasite capacitance C_p plays an important role. Thus, the substrate loss dominates the Q factor and thus the inductor performance at high frequencies.

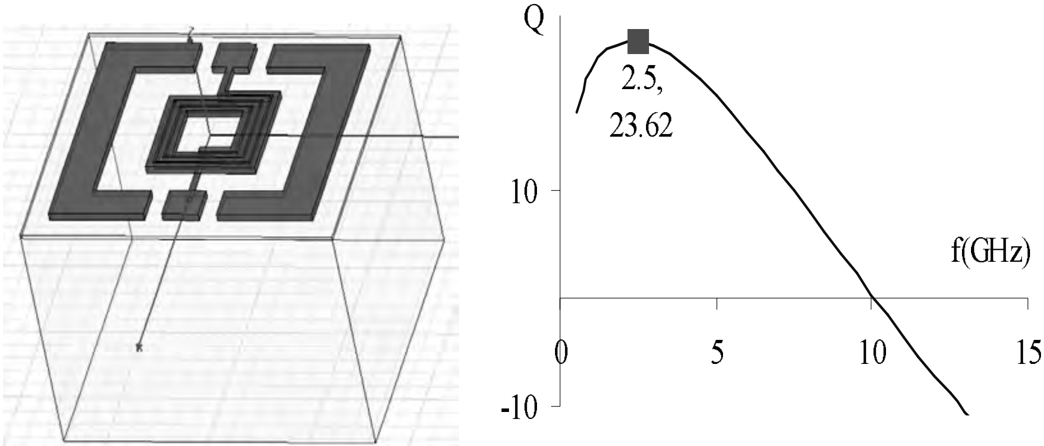


Figure 2.13: A sample spiral inductor and its Q-factor simulation result

Figure 2.13 displays a simulation curve of the Q factor of a sample inductor. The simulation was conducted with Ansoft HFSS 9.1™. From the curve displayed, one can see the Q factor exhibits a distinct maximum (Q_{max}) 23.62 at a certain frequency $f(Q_{max})$ = 2.5 GHz. This can be easily understood from the lumped-element models shown in Figure 2.6 and Figure 2.11. From the Figures, it is apparent that the substrate parasite effect is a capacitive effect, and becomes stronger with increasing frequency. Also, at any given frequency, alternating currents take the path of least impedance. When the frequency is low, the substrate effect is small (this means the substrate loss factor and self-resonance factor are close to unity in Equation (2.31d) and can even be ignored. Thus the RF signal passes through the path of L_s (the inductor coil) because ωL_s is small and $1/(\omega C_s)$ and $1/(\omega C_{ox})$ are large. And with increasing frequency, according to Equation (2.31d), Q grows initially as $\omega L_s/R_s$. Accordingly, the Q curve goes up to the peak Q point. After the peak Q point, the growing substrate loss gradually dominates the Q curve trajectory. Specifically, at frequencies between Q_{max} and the self-resonance, ωL_s is larger than $(1/\omega C_{ox} + (R_{si}//C_{si}))$ but is still smaller than $1/(\omega C_s)$. This situation arises from the mechanism $C_{ox} >> C_s$ and C_{si} [29]. Thus, the larger amount of the RF signal now passes through the substrate via C_{ox}, resulting in the Q decay with increasing frequency. At a certain high frequency (f_{srf} =10 GHz in this example), self-resonance occurs. The lumped model in Figure 2.6, Figure 2.11, and Equation (2.31d) show the possible mode of resonance: between L_s and $C_s//C_p$ (which consist of C_s, C_{ox}, and C_{si}).

2.6 Solenoid Inductor Lumped Model and Loss Mechanism

Most of the macro-scale inductors are solenoid-type. Due to the limitations of current micro fabrication techniques, most of the conventional geometries for integrated inductors have been spiral-types or even meander-types. Specifically, fabrication of a coil wrapped around a core has been more difficult using conventional IC processes than the fabrication of spiral or meander inductors. Spiral-types and meander-types suffer from some drawbacks. Meander-types suffer from low overall inductance due to the negative turn-to-turn mutual inductance. A spiral always requires a lead wire to connect from the inside most end of the coil to the outside, which introduces an unavoidable and

often dominant stray capacitance between the inductor metal trace and the lead wire [21]. Moreover, its size is larger compared with solenoid-types with the same number of turns, which normally means larger projection area on substrate. This results in stronger substrate loss effect. In addition, the direction of flux is perpendicular to the substrate, which can incur significant eddy current loss within the substrate volume. As a contrast, the magnetic field created by the solenoid inductor is parallel to the substrate and results in a significantly reduced eddy current effect. Also, if there are active circuits inside the substrate, the stronger magnetic coupling will bring more unexpected interference to the underlying circuit performance.

Figure 2.14: Suspended solenoid inductor with 150μm air gap

Advances in surface-micromachining techniques have made some solenoid-like inductors possible with IC processes. But these typically suffer from geometric limitations, for instance, no suspension possibility or low suspending height, low via structure height due to the constraint of the 2D nature of the surface micromachining, and poor planarization and over etching problems [30]. Typically, such inductors can only realize a suspension of at the most 30-50μm and the aspect ratio of the via conductor is only 1.5:1. UV (Ultra-Violet)-LIGA can also been used to fabricate suspended structures, potentially with suspensions up to 100μm [31], however, to the author's knowledge, the UV-LIGA suspended solenoid inductor has not been reported.

The 3D deep X-ray LIGA-micromachining technique is a promising tool to approach the suspended structure because of its characteristics of high aspect ratio and high resolution (accuracy). This thesis is focusing on the deep X-ray LIGA fabricated inductors (spiral-types and solenoid-types). As mentioned before, surface micromachining can realize a suspension height at 50 μm; UV-LIGA can reach 100 μm suspension. It is reasonable to believe that Deep X-ray LIGA can realize even greater heights. However, due to the mechanistic robustness concern, the suspension height for the X-ray LIGA structural inductor is tentative set up at 150 μm.

Figure 2.14 shows the simplified suspended solenoid inductor structure with a 150 μm suspension which could potentially be made by deep X-ray LIGA process. For a solenoid inductor, if we ignore the substrate and fringing effect, the inductance can be represented by

$$L = \frac{N^2 \mu A_C}{l_c} \tag{2.33}$$

where A_c is the cross section area of the core, l_c is the total length of the core, μ is the permeability of the core, and N is the number of coil turns.

As described in Section 2.4.1, the parasitics in the inductor are stray capacitances and resistances. One can employ high conductivity metals, such as copper, silver, or gold, to reduce the parasite resistance inside the metal. Meanwhile, one can control the thickness of the metal trace to reduce the heating dissipation according to the skin effect calculation.

In contrast to the parasitic resistances, the stray capacitances are more crucial in determining the self resonant frequency (*SRF*), inductor operation range, and the *Q*-factor. There are two main mechanisms for the stray capacitances, i.e., the capacitance between conductor lines (conductor to conductor) and the capacitances from the conductor to the substrate and inside the substrate. Similar to the spiral inductor case, the conductor to conductor capacitance here is much smaller than those of the substrate related, especially the one crossing the isolation layer. Hence, the substrate related

capacitances dominate the capacitive parasitics. Similar to the spiral-type case, quite a few methods, such as enlarging the thickness of the dielectric isolation layer, enlarging the resistivity of the substrate, and introducing an air gap between the substrate and the inductor metal structure, can be used to reduce these stray capacitances. Limited by the industrial process reality, one cannot change the isolation layer thickness and the conductivity of the substrate at will if the on chip inductor is compatible with IC processes, for instance, CMOS compatible. A possible way is to introduce an air gap (suspension). To analyze and further reduce the conductor to conductor capacitances inside the inductor, a simple equivalent circuit, which is shown in Figure 2.15, to model the conductor to conductor capacitances is introduced.

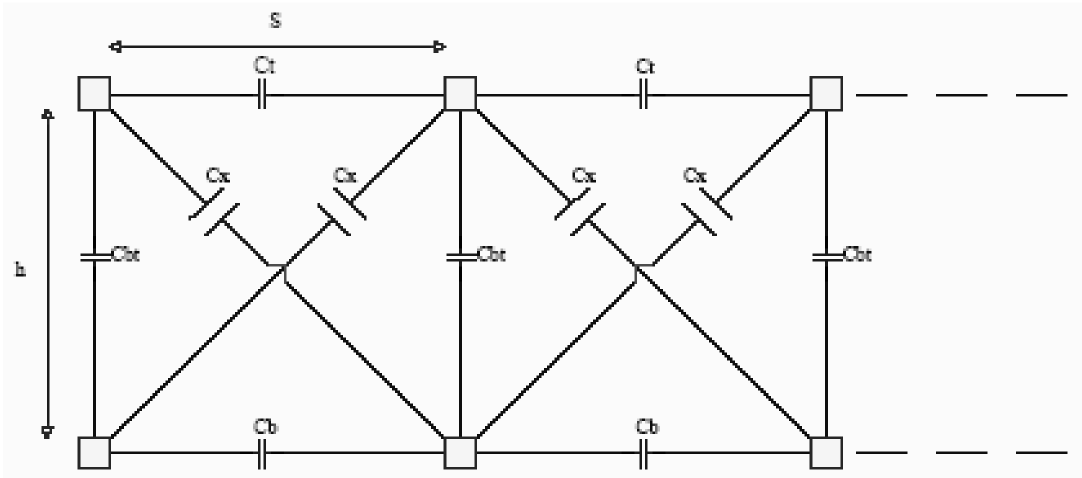


Figure 2.15: The equivalent circuit for calculating the stray capacitances between conductor lines. The side cross-sectional area of the conductor lines and the capacitances between these conductor lines are shown [30].

In this model, the inductor coil is suspended in air and the via conductors which connect the top and bottom conductors have little effect on the total stray capacitance. C_t, C_b, C_{bt}, and C_x are the capacitance between two top conductor lines, capacitance between two bottom conductor lines, capacitance between the top and the bottom conductor lines, and capacitance between two diagonally placed conductor lines, respectively. If neglecting the fringing effect, these values can be calculated as follows

$$C_t = C_b = \frac{\varepsilon A}{d} = \frac{\varepsilon (l \cdot b)}{s} \tag{2.34 a}$$

$$C_{bt} \leq \frac{\varepsilon(l \cdot a)}{h} \tag{2.34 b}$$

The equality can only be realized when the bottom and top beams are parallel.

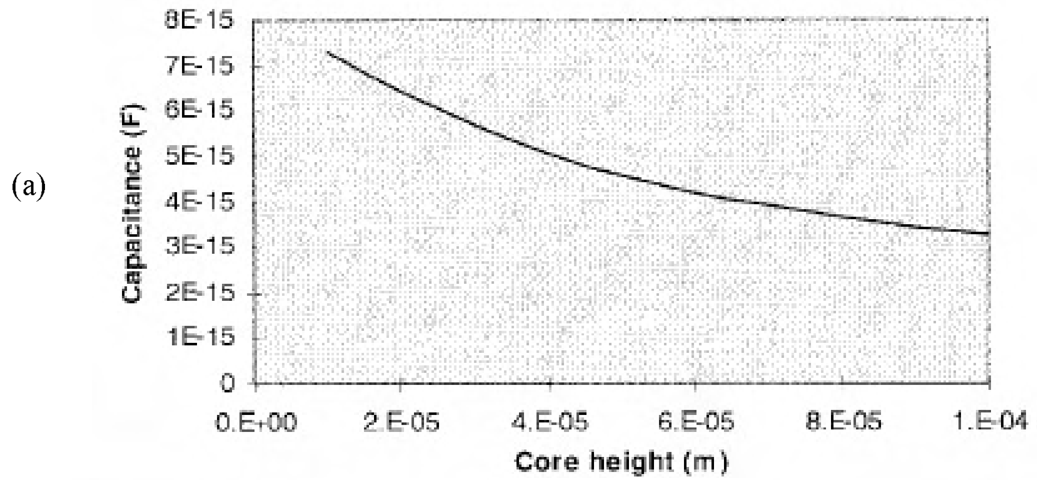
$$C_x \approx \frac{\varepsilon\left(l \cdot \sqrt{a^2 + b^2}\right)}{\sqrt{s^2 + h^2}} \tag{2.34 c}$$

where ε is the dielectric constant of air, a is the width of a conductor line, b represents the thickness of the conductor line, l is the length of each conductor line, s is the horizontal spacing between adjacent conductor lines, and h is the vertical spacing (via) between the top and the bottom conductor lines. Equation (2.34c) is just an approximation if one looks at the two diagonal beams as two plain plates facing each other.

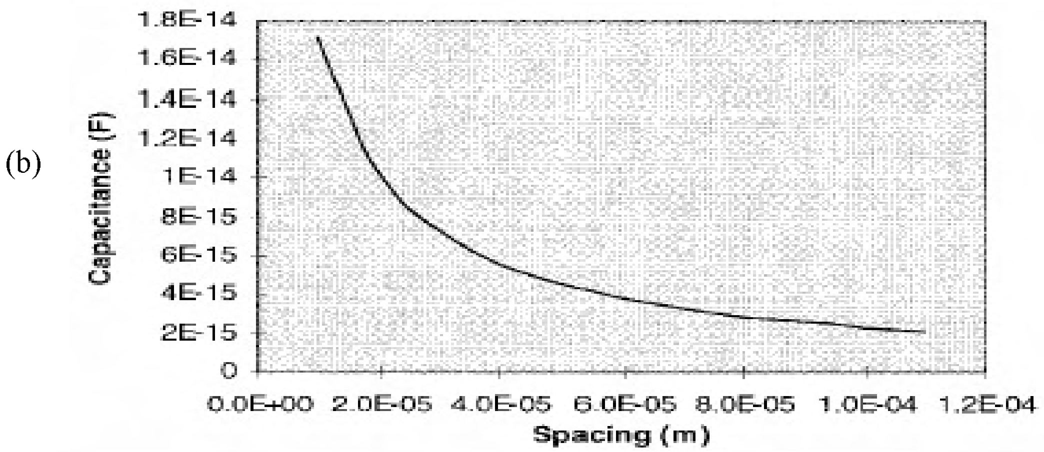
Figure 2.16 shows a capacitance simulation result [30] based on the model given by Figure 2.15. In Figure 2.16 (a), the core height (h) means the vertical spacing between the top and the bottom conductor. Obviously, the higher the h, the bigger the inductance and the lower the stray capacitance, which is desirable. From Figure 2.16 (b), one can see that the increasing line spacing helps reducing the stray capacitance. However, with the increasing of the line spacing, the total inductance also decreases. Finally, Figure 2.16 (c) shows that total stray capacitance linearly increases with regard to the conductor line thickness. From this viewpoint, one can see that excessively increasing the conductor thickness is not only unnecessary because of the skin effect, but also can bring in some negative effect due to the corresponding stray capacitance enlargement.

Unlike the spiral type inductor, which has been extensively studied, the research of the solenoid inductor in microelectronics and MEMS is far less mature. To date, there is not a well-acknowledged lumped equivalent model reported. Roughly speaking, the lumped elements modeling the substrate effect in Figure 2.6 for the spiral inductor is still loosely useful for qualitatively discussing the solenoid inductor because of the same substrate effects. But the definition and value for the individual lumped components would be different from spiral inductor case.

(a)



(b)



(c)

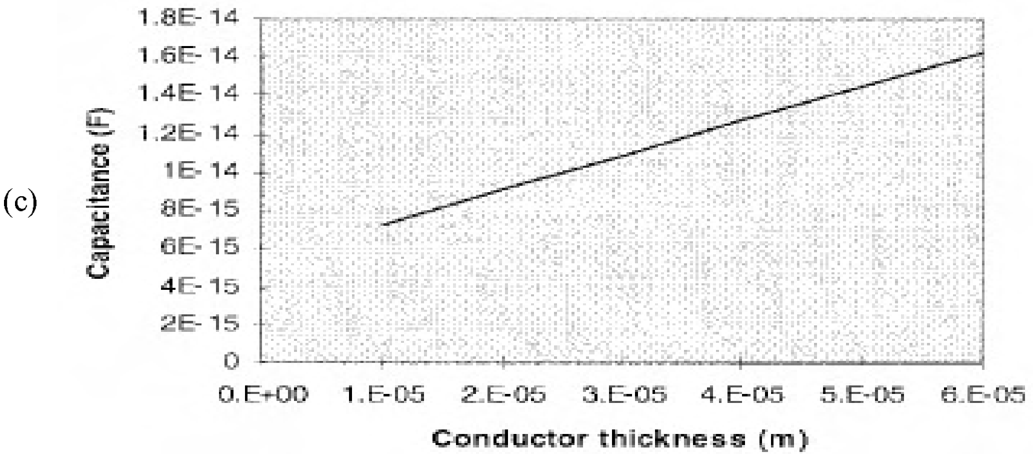


Figure 2.16 [30]: (a) The stray capacitance change with various core heights (*h*); (b) The stray capacitance change with various line spacings (*s*); (c) The stray capacitance change with various conductor line thicknesses (*b*)

3 Inductor Layout and Previous Work

3.1 Inductor Layout

In this section inductor layout issues are discussed. The magnetic energy is mostly stored in the inner core of the winding. The inductance is largely a function of the area of the loop and the number of turns.

3.1.1 Planar Inductor Structure

Due to the fabrication difficulty of more complicated geometries, planar inductors are still the mainstream of the inductor designs in MEMS and microelectronics. Since many IC processes constrain all angles to be 90°, square types of spiral inductors remain popular. Polygon spiral inductors are a compromise between circular spirals and square spirals. Figure 3.1 exhibits the simplified layouts of various types of inductors.

In a spiral, the electric fields on the outer turns tend to fringe. Therefore, the "inductive" centre does not correspond to the "capacitive" centre. Due to the non-uniform mutual magnetic coupling, the "inductive" centre also does not correspond to the "resistive" centre. To create a symmetric centre point, some researchers have proposed balanced structures as shown in Figure 3.2. These structures have a geometric center coinciding with the electrical center. This is needed in differential circuits as such points can be grounded or connected to supply without greatly disturbing the differential signals.

At low frequencies, the current in the inductor metal winding is nearly uniform. However, at high frequencies, the magnetic field is strongest in the center of the spiral. This results in the greatest strength of eddy current in the center of the inductor due to

the skin and proximity effects. The eddy current in the metal traces counteracts the

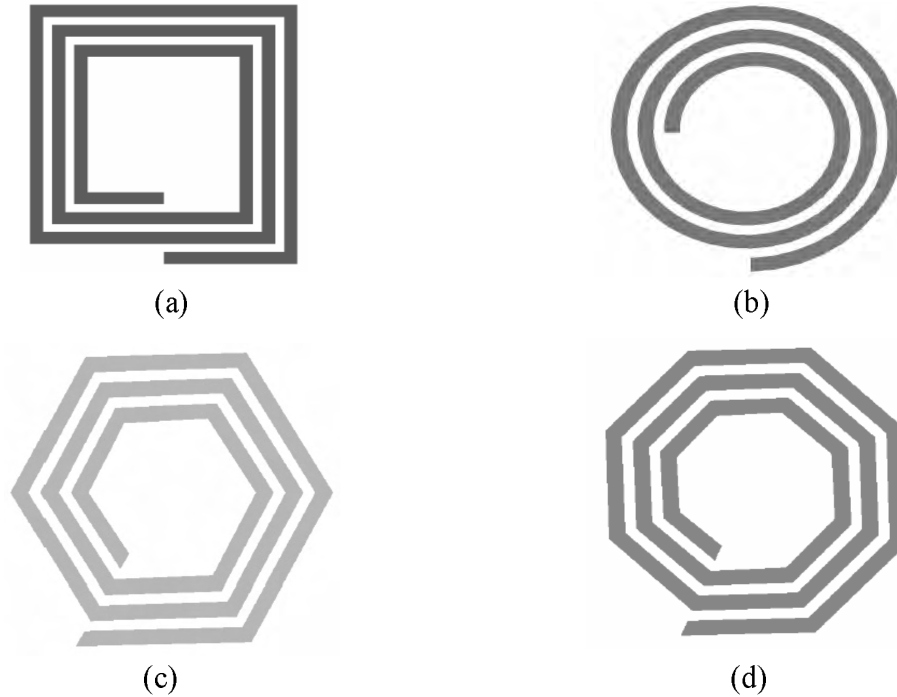
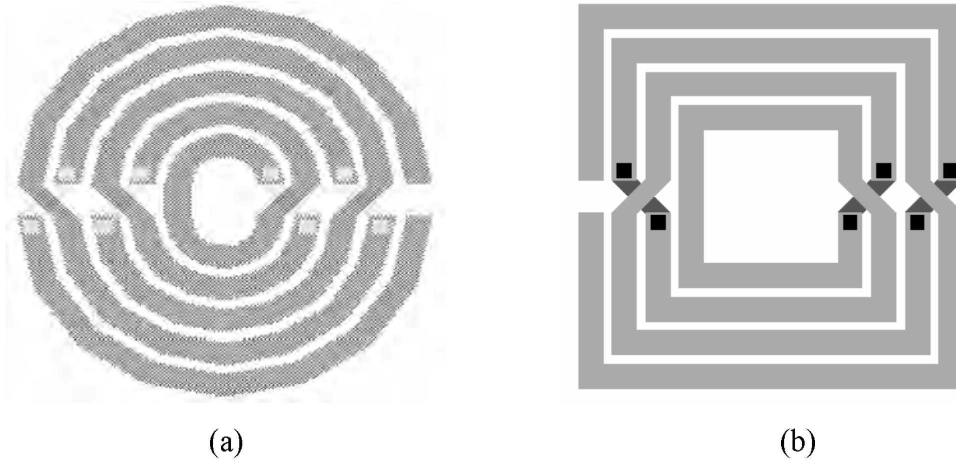


Figure 3.1: Spiral inductor layouts. (a) A square-type; (b) A circular-type; (c), (d) polygon-types

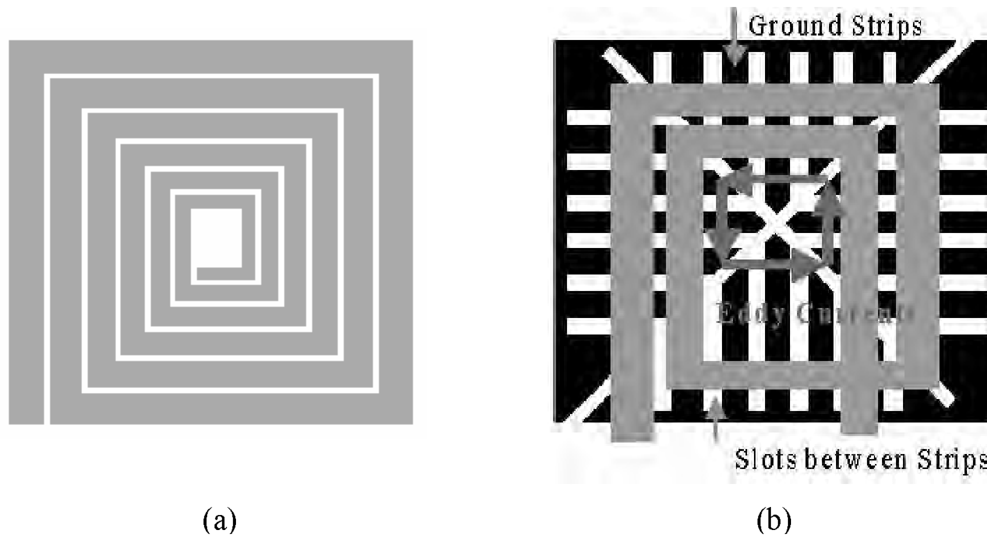
signal current. As a consequence, the balanced total current is mostly limited in the outer turns of the inductor. Thus, in the center of the inductor, the conductor width does not have as strong an influence on minimizing metal losses as at low frequencies. To take advantage of this effect, one can decrease the width of the inner turns to effectively move the turns closer to the outer edge. Also, one can remove the inner turns to produce a "hollow" spiral [32]. These realizations are illustrated in Figure 3.3. These two approaches all result in Q factor improvement.

To shield an inductor from the substrate losses, a good approach is to build a shield with lower metal layers or polysilicon layers to block electromagnetic energy from coupling to the substrate [26]. Due to the close proximity of the inductor and the shield, using solid metallization would induce "image" eddy currents inside which could generate an opposing magnetic field. This would result in inductor magnetic energy decreasing and



(a) (b)

Figure 3.2: (a) A balanced polygon spiral inductor; (b) A balanced square spiral inductor



(a) (b)

Figure 3.3: (a) A tapered spiral inductor; (b) A patterned ground shield inductor with "hollow" spiral.

the Q factor degrading. Thus, a pattern ground shield, similar to Figure 3.3 (b), is proposed. The shield currents inside can only flow perpendicular to the current path in the inductors, reducing the mutual magnetic coupling. This greatly reduces the magnetic coupling between the shield and the inductor and hence greatly reduces the eddy currents inside the shield.

3.1.2 Non-Planar Inductor Structures

There are two main advantages of non-planar structures. One is the reduction of the size which is generated by the projection of the real device size to the substrate. The projecting size reduction results in the reduction of the electromagnetic coupling between the inductor and the substrate. The other is the non-perpendicular orientation of the inductor magnetic flux to the substrate. This also reduces the magnetic coupling to the substrate. One useful approach is to build the solenoid inductors based on the conventional IC process, specifically, using the top and bottom metal layers and vias to form the inductor vertical coils, or using a combination of metal interconnection and bond wires to realize the vertical coils. However, standard IC process can not produce a coil with sufficient cross-sectional area to produce good Q [33]. Recently, with the advance of MEMS technology, self-assembled inductors and solenoid inductors, and the suspended solenoid inductors have been reported. These realizations have significantly improved the drawbacks of the solenoid inductor built with conventional IC processes. They will be discussed in more detail in Section 3.2.

3.2 Previous Work

Inductance calculation research has been carried out for some time. Grover [34], one of the early researchers, systematically proposed tables and formulas for calculating the static (DC) inductance of various structures in the 1940's. More recent work includes Greenhouse's [22], which is actually the basis for todays RF micro-scale inductor empirical calculations. Moreover, Ruehli developed the concept of Partial Element Equivalent Circuits (PEEC) [35], a technique for solving Maxwell's Equations. The PEEC method has become the core of many other numerical techniques to calculate inductance efficiently.

Various contributions to design and analysis of conventional RF IC inductors on silicon have been made in recent years [6], [8], [21], [26], [29]. These works focus on relating the various influences from the inductor coil, dielectric isolation, and Si substrate to the inductor characteristics. But the underlying problems remain: very limited inductor

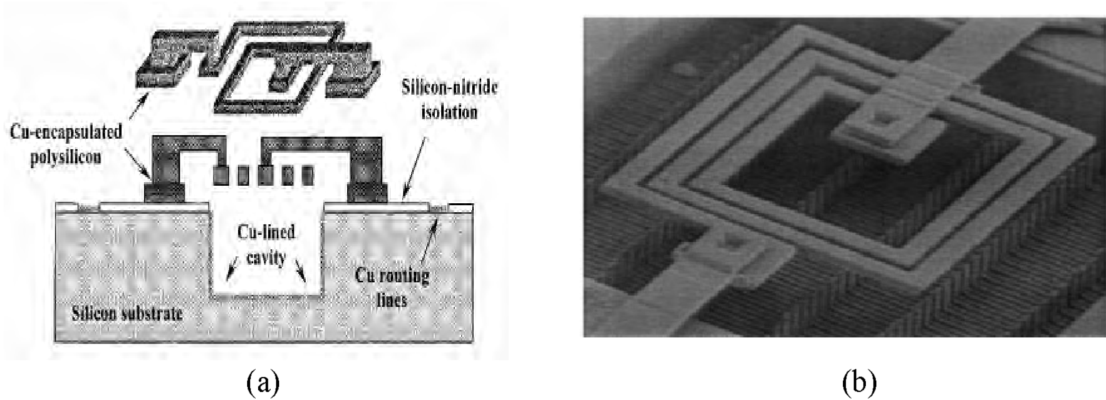
metal thickness, low geometric accuracy and coarse surface roughness, and strong substrate magnetic coupling loss. All these drawbacks limit the *Q* factors, *SRF*, and even the inductances.

3.2.1 Micromachining Inductors

The newly emerging MEMS technology has brought promising capabilities to RF and microwave inductor research, potentially improving some of these limiting factors. Some of the recent techniques are discussed below.

Thick metal traces of the inductor and the thick isolation layer between the inductor coil and the substrate can result in higher *Q* factor and also push the *SRF* upwards. The post-CMOS compatible MUMPs process uses a thick BCB layer (Benzocyclobutene) on top of a silicon substrate with a copper inductor trace of 10μm thickness. This, for instance, has resulted in a $Q > 35$, and L=1.5 nH in the band 3-6 GHz [9], which is an improvement over the counterparts fabricated with conventional CMOS technique.

Substrate Etching



(a) (b)

Figure 3.4 [38]: (a) Schematic of a copper-encapsulated polysilicon inductor suspended over a copper-lined cavity beneath; (b) SEM image of the fabricated inductor

Substrate etching is a method intended to significantly reduce the parasitic capacitance C_{si}, potentially increasing *SRF* and the *Q* at higher frequencies. However, at low

frequencies (< 2 GHz), the inductor loss is dominated by R_s, which only depends on the inductor metal structure. Thus, substrate etching does not improve the *SRF* and Q at low frequencies. Chang et al. [36] contributed one of the first example of CMOS silicon substrate anisotropic etching with KOH, underneath the inductor. The isolation is a thin layer of SiO_2. Chi and Rebeiz [37] developed a fully suspended inductor on a SiO_2 or a SiN isolation membrane with the silicon substrate etched using KOH. Jiang et al. [38] reported inductors fabricated using polysilicon and electrolessly plated with copper for low series resistance. The same plating process coats the silicon cavity, providing a good RF ground and an electromagnetic shield for the inductor from the silicon substrate. Their inductors were suspended over deep copper-lined cavities. The measured Q of a 2.7 nH inductor is 36 at 5 GHz. This device is also shown in Figure 3.4.

Self-Assembly

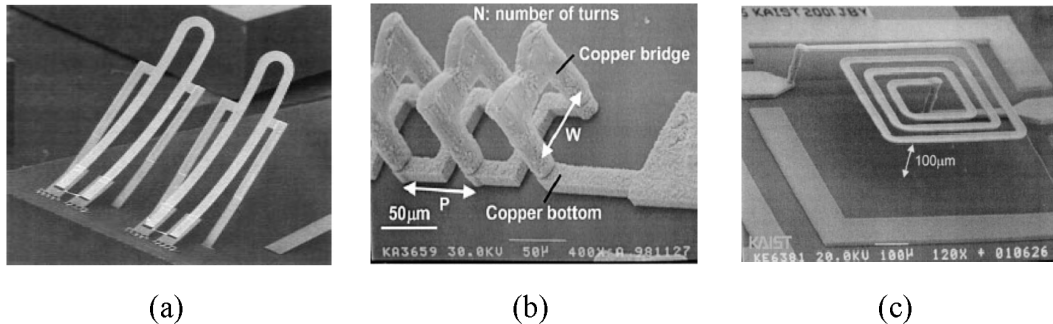


Figure 3.5: (a) The SEM image of a self-assembled inductor; (b) The SEM image of a solenoid inductor; (c) The SEM image of a suspended planar inductor

A useful micromachining approach to reduce the parasitic capacitance is self-assembly. An example was done by Lubecke et al. [39], using a 0.5 μm thick Cr-Au layer over a 1.5 μm thick polysilicon layer. The different residual stresses in the Cr-Au and polysilicon layer cause the inductor to self-assemble above the substrate. A 1 nH inductor with a Q of 13 at 9 GHz was realized and is shown in Figure 3.5 (a). Although coupling of energy into the substrate with the self-assembled inductors is greatly

reduced between inductor coils or to other circuit elements coupling due to electromagnetic radiation as well as mechanical stability could be problematic.

Solenoid and Suspended Inductors

Theoretical solenoid inductors result in a confined magnetic field inside of the solenoid, and do not couple strongly to the substrate because the flux is parallel to the substrate. In practice, on the MEMS scale, the cross-sectional area of the solenoid is quite small so that it is closer to the substrate. This leads to the generated highest intensity magnetic field closer to the substrate, more substrate coupling, and the *Q* degradation. An example done by Yoon et al [30] is shown in Figure 3.5 (b). Also, a suspended planar inductor above the silicon substrate has been reported [31]. Electromagnetic analysis indicates that substrate coupling can be reduced significantly if the inductor is placed at 30 µm or more above the substrate. A 14 nH inductor with a *Q*=38 at 1.8 GHz was obtained which is shown in Figure 3.5 (c).

3.2.2 Previous Work in CMOS Compatible MEMS Inductors

Figure 3.6: The SEM picture of the 0.18µm CMOS compatible suspended spiral inductor [40]

As mentioned in the Motivation in Chapter 1, this thesis explores the performance and characteristics of proposed LIGA structural inductors, specifically on simulated

CMOS/BiCMOS Si substrate. It is, therefore, informative to introduce some related CMOS compatible inductor cases before considering this concept for LIGA.

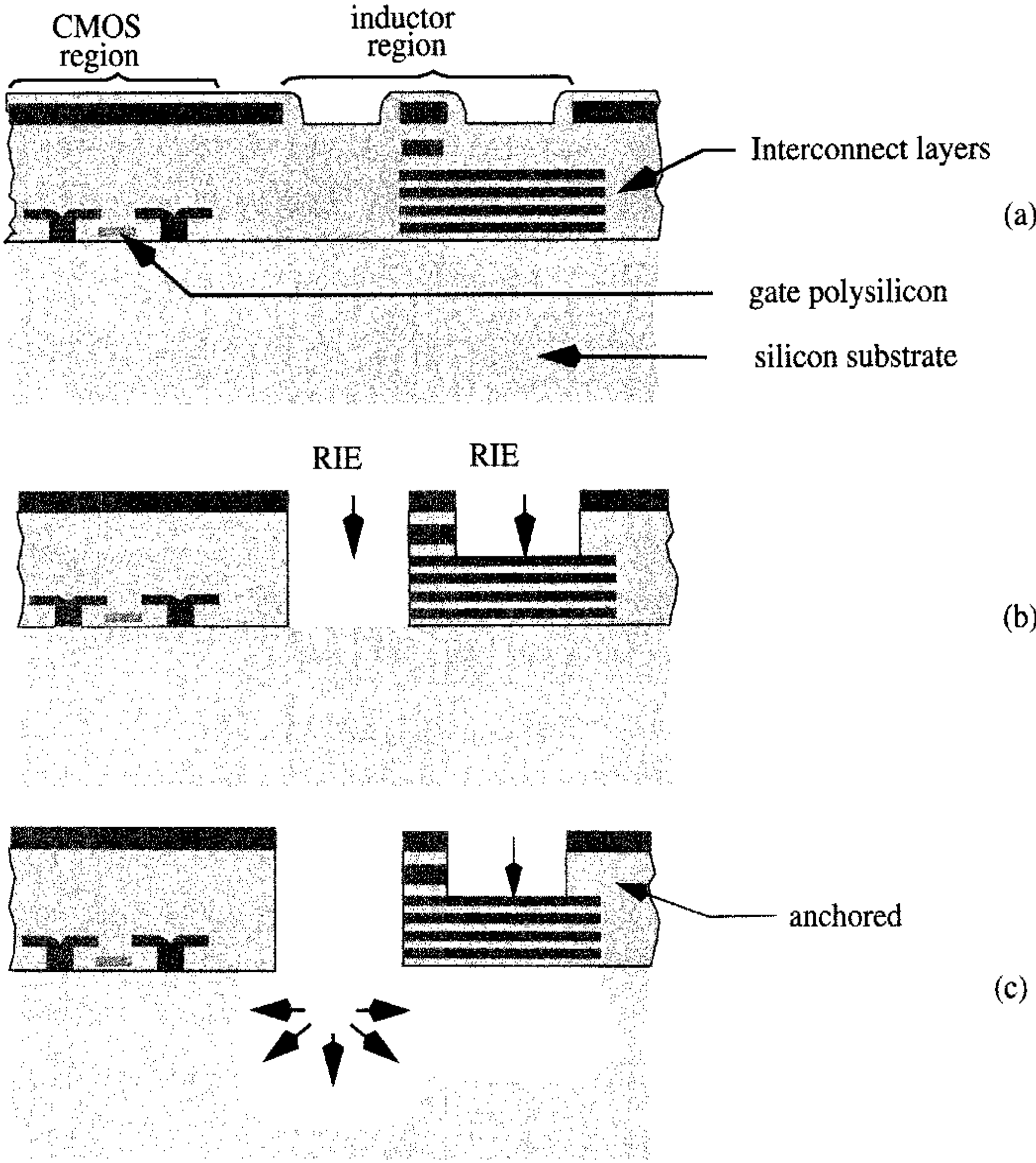


Figure 3.7 [40]: Cross sections of the CMOS compatible inductor fabrication simplified process steps (a). The conventional CMOS die from the foundry; (b). After removal of sidewall oxide; (c). After silicon substrate removal by anisotropic and isotropic etch.

Lakdawala et al. [40] proposed a suspended copper inductor single-anchored (cantilever) over the etched cavity that is compatible with 0.18 μm CMOS process. The inductor coil was designed to take advantage of the metal interconnect layers in the CMOS process.

The SEM picture of this design is shown in Figure 3.6. The simplified fabrication process is shown in Figure 3.7. Figure 3.7 (a) illustrates the CMOS region (active region) and inductor region (passive region) general layout arrangement. Figure 3.7 (b/c) show various reactive ion etching (RIE) and other etching step to remove SiO_2 not covered by any of the metal layers, and ultimately the underlying silicon to release the microstructure. Note that the active region is separated from the passive region, and protected by a metal-layer ground ring around the inductor.

Park et al. proposed a multi-exposure UV (Ultraviolet) LIGA process to fabricate 3-D inductor structures [41]. A suspended spiral inductor is built directly on top of the silicon substrate which consists of active device and circuits. The simplified fabrication process is illustrated in Figure 3.8. Figure 3.8 (a) shows a completed CMOS chip with active devices, metal interconnection lines, and a top insulation layer with reserved open pads for the subsequent suspended inductor fabrication. In Figure 3.8 (b) a metal seed layer is thermally evaporated, followed by a 20 μm thick photoresist spin-on process and first UV exposure. The bottom electrode molds are patterned inside the photoresist and completed by the Cu electroplating right on top of the reserved open pads. In Figure 3.8 (c), a second thick photoresist (about 40 μm) is spun on the wafer and the two-step UV exposure with different photo masks and exposure times follows. By photoresist development, a 3-D photoresist mold is generated. In Figure 3.8 (d), the Cu posts are electroplated. After the Cu post forming, Figure 3.8 (e) shows that a second seed metal layer is thermally deposited, followed by a mechanical polishing process to remove the topmost seed layer because only the seed metal in the upper recessed regions is useful (see Figure 3.8 (f)). Then, in Figure 3.8 (g) Cu is electroplated in the upper recessed regions. Finally, the rest of the photoresist and seed layers are etched to realize the suspended inductor in Figure 3.8 (h).

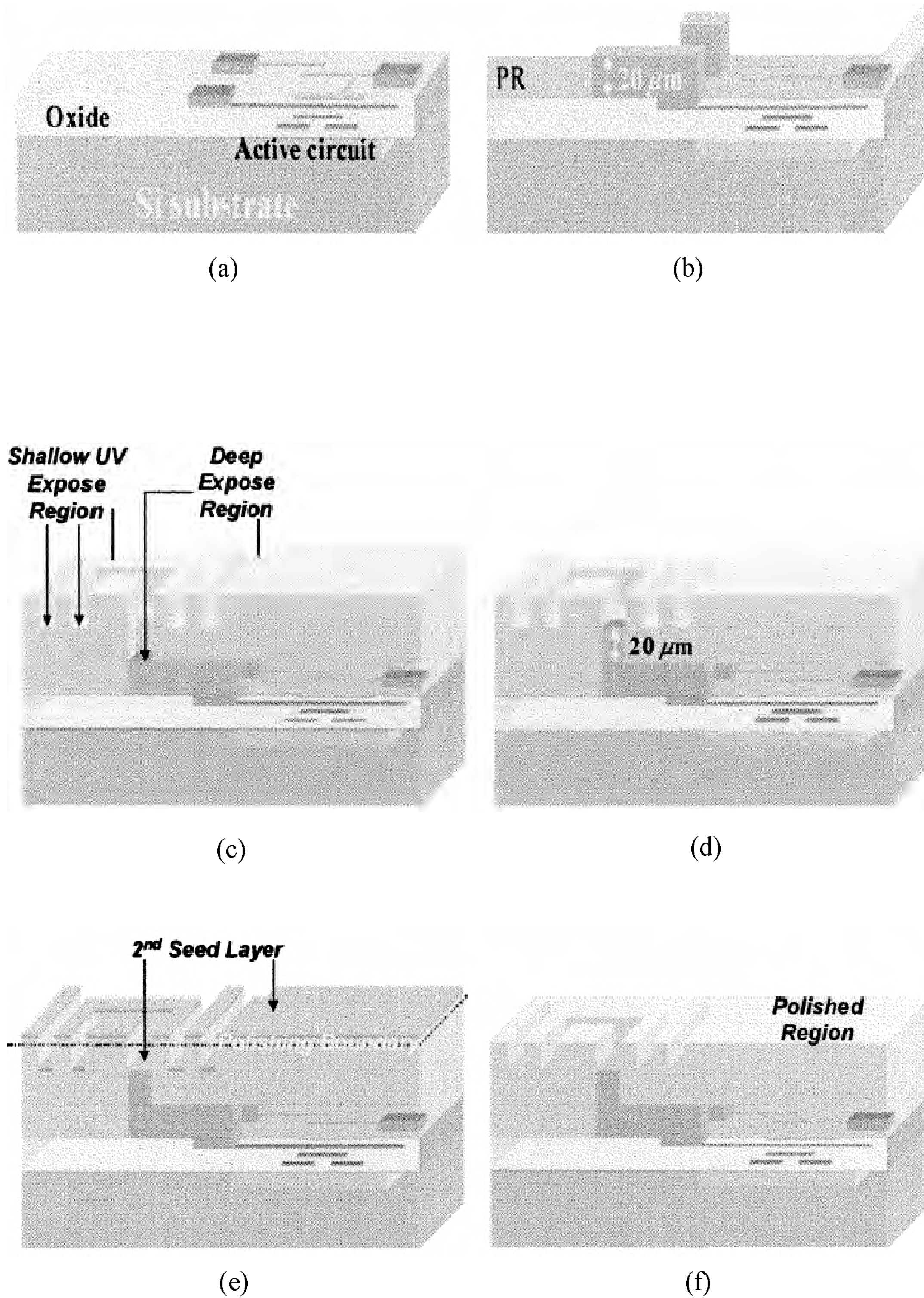
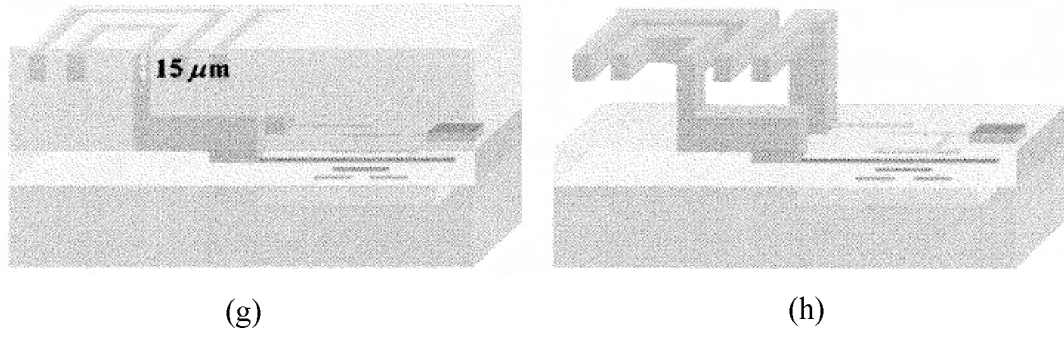


Figure 3.8: The suspended inductor simplified fabrication process [41].



(g) (h)

Figure 3.8 (continued): The suspended inductor simplified fabrication process [41].

4 Design of LIGA MEMS Air Core Inductors on CMOS

4.1 Finite Element Method and HFSS

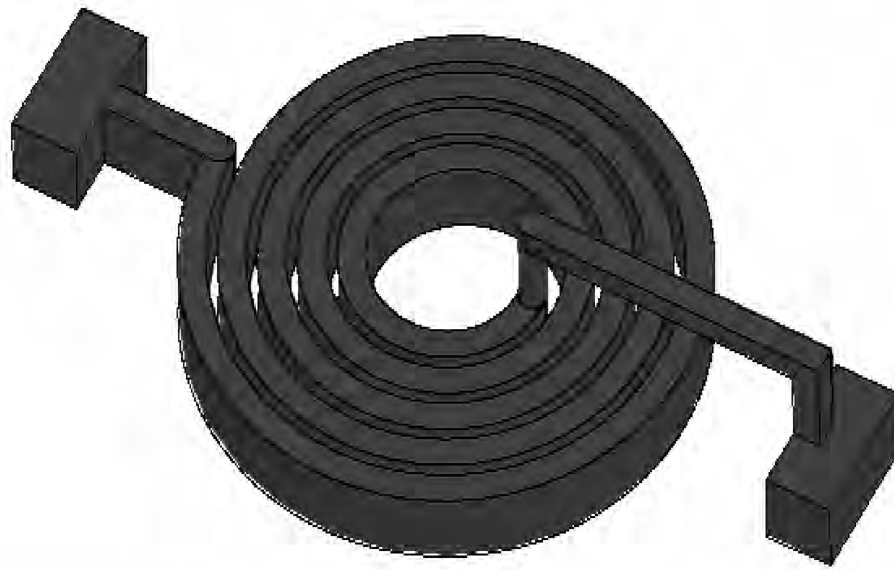
The finite element method (FEM) is a popular numerical technique for solving partial differential equation modeled physical systems. In this method, the partial differential equations are defined with three spatial variables and a temporal variable. Nowadays, the FEM has become a universal tool for solving various engineering problems such as electrical, mechanical, civil, power, heat, and aerospace. Generally, a FEM solution consists of the following principle steps [42], [43]:

Meshing of the solution region into a finite number of elements as shown in Figure 4.1;

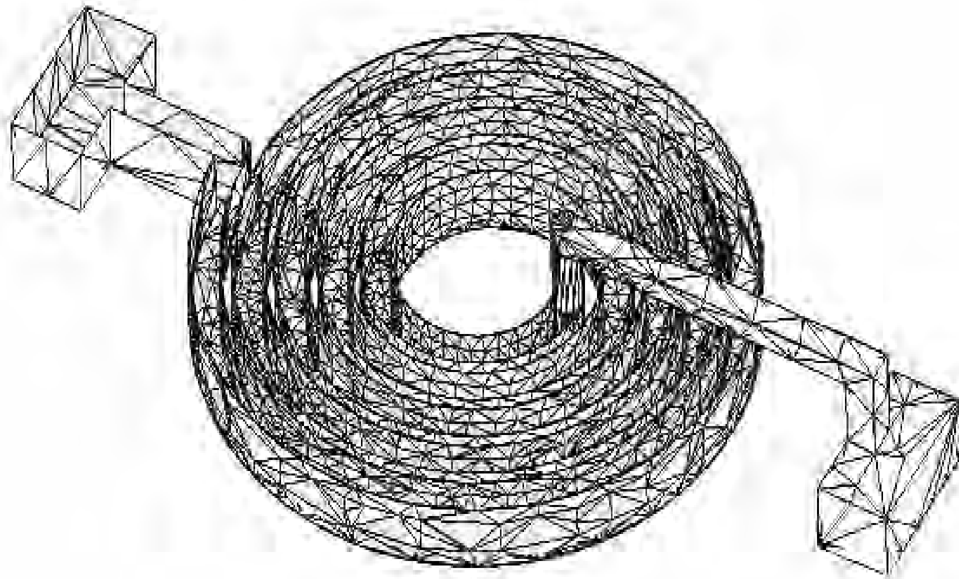
- Using a set of discrete quantities to approximately approach the continuous quantities in the finite elements which are generated in Step 1;
- Assembling all elements in the solution region;
- Solving the algebraic equations which describe the system

HFSS^{TM} (High Frequency Structure Simulator) was developed based on FEM. It is a 3-D full wave electromagnetic tool to solve the Maxwell's Equations for arbitrary shape of structures with complex material distributions. When doing the calculations, this software approximates the continuous field quantities using discrete counterparts, thus transforming the continuous Maxwell's Equations into sets of algebraic equations and solves them using conventional matrix methods. HFSS can not only solve the 3-D fields and currents, but also take into account various propagation modes and predict most of the high frequency effects such as dispersions, conversions between modes, losses, and radiations.

The main output data provided by HFSS are the [S], [Y], [Z], and [ABCD]-matrices, characteristic impedances (Z_o) at ports, VSWR, and the complex propagation constant.



(a)



(b)

Figure 4.1: Meshing of an object (a circular inductor): a) Before; b) After.

The working principle of HFSS can be briefly explained as follows. When starting a simulation, HFSS begins to divide the objective structure into a finite number of meshing elements. The meshing elements are generated in terms of tetrahedras. Then, HFSS finds the vector field quantities at the vertices and midpoint of the edges nodes,

and interpolates field quantities inside tetrahedras from the nodal values. HFSS stores at every vertex the vector field components that are tangential to the three converging edges of the tetrahedron. Moreover, it stores the vector field components at the midpoints of the edges that are also used for interpolation of the fields inside the tetrahedras. In doing so, continuous field problems are transformed to discrete problems. Normally, a finite element should be much smaller than the wavelength. The smaller the tetrahedron, the better accuracy for interpolating the fields into the element. Before the simulation, the user should manually set up the simulation iteration times. At the beginning of the simulation process, HFSS creates a coarse initial mesh and calculates the corresponding coarse field solutions. Then it refines the mesh during subsequent iterations, especially in the regions with high solution error densities. The solution error is calculated by comparing the solution results of the current iteration, namely, S-matrix, with the counterpart in the previous iteration. Such a kind of iterative process continues until the solution results converge to the defined level of accuracy or the defined total times of iterations is reached.

Note that the denser the mesh, the greater number of the finite elements, the more accurate the solution. However, the computing power limits the density of the mesh because the denser the mesh, the more nodal field values and matrix data needs to be stored in the computer memory. Thus, the user should make a right compromise between the levels of accuracy and mesh density based on the available computing resource. Figure 4.2 shows a simplified flow chart of the HFSS adaptive solution.

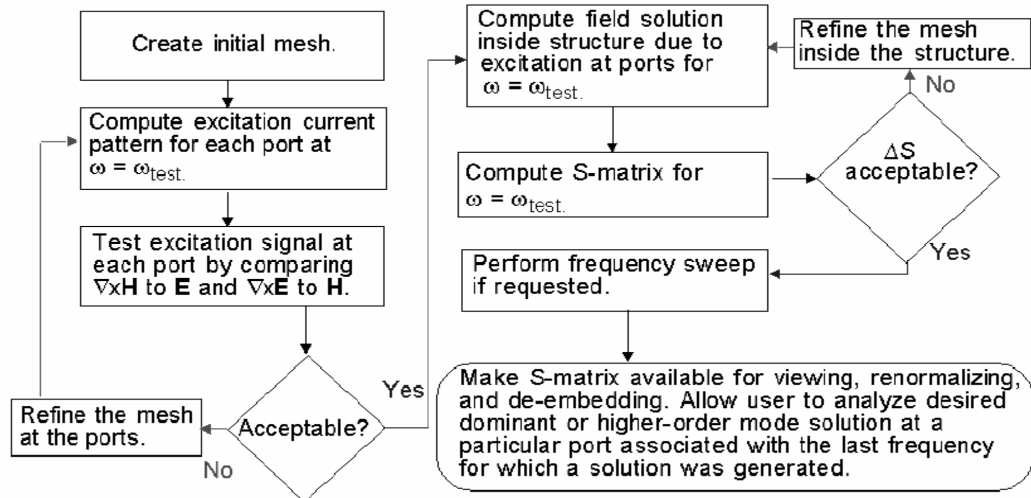
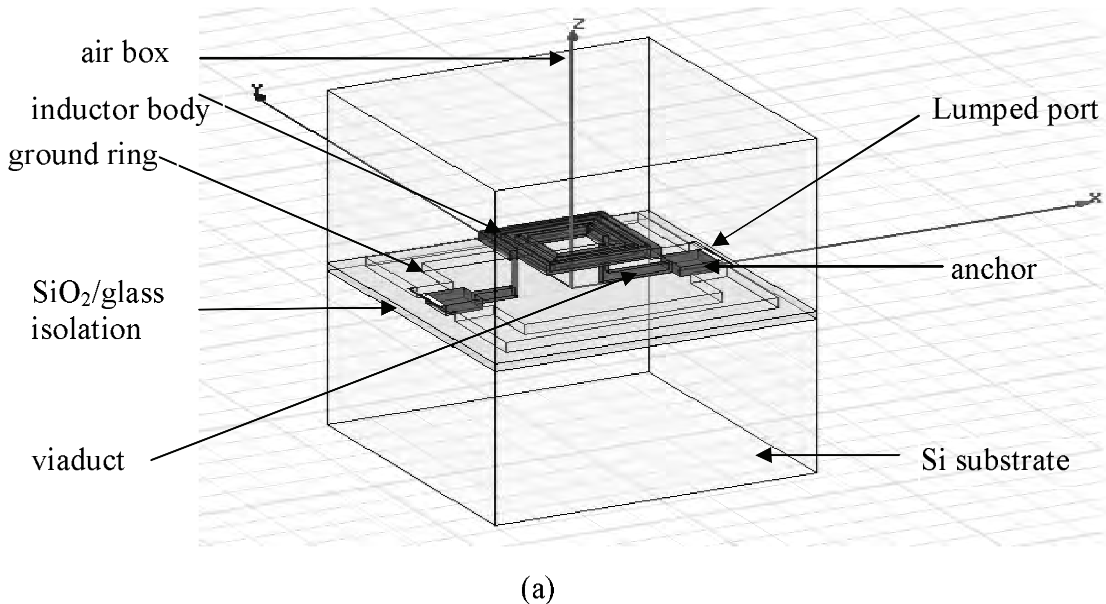


Figure 4.2: Simplified flow chart illustration of the HFSS adaptive solution

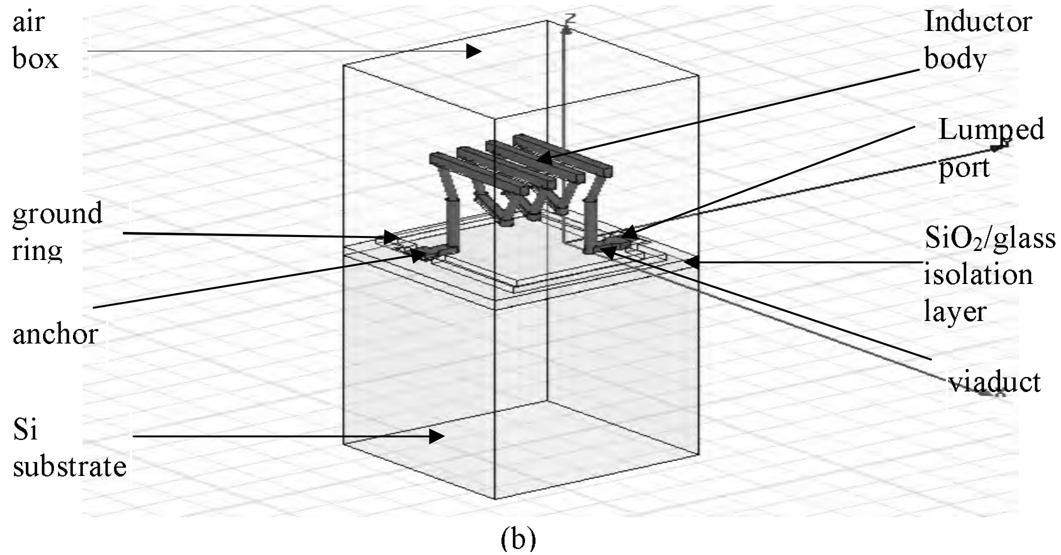
4.2 Inductor HFSS Simulation Model Designs

Figure 4.3 shows the designed HFSS models. In the figures, one can see besides the physical blocks such as inductor metal coils, ground rings, SiO_2 isolation layers, and Si substrates, there are some virtual blocks. These includes, air boxes, lumped excitation ports, and perfect-E bars. They are required by HFSS to define excitation and boundary conditions.



(a)

Figure 4.3: HFSS simulation model for a suspended square spiral inductor



(b)

Figure 4.4: HFSS simulation model for a suspended solenoid inductor

4.2.1 Virtual HFSS Block Setup

In HFSS, the outer surfaces of the model interfacing the background are assumed perfect E boundaries by default (tangential component of the electric field is zero), which do not permit any energy to enter or leave. Because of this assumption, if the investigated object surfaces touch the background, they will appear as perfect conductors where the investigated electromagnetic fields do not exist. Thus, an air box, which is a virtual block, must be put in the place where the investigated electromagnetic field exists. Of course the air box outer surfaces which touch the background are considered to be perfect conductors. In case the air box surfaces bring any significant influence to the performance and the field distributions of the model, the size of the air box should exceed the model field volume to limit interaction with the solved field of the models. In this design, the horizontal sizes of the air box and combined substrate are set 20 μm-100 μm bigger than the metal ground ring of the inductor in both $\pm x$ and $\pm y$ directions.

In HFSS^{TM}, another kind of virtual block, the port, is required to drive the passive components for the simulation. Generally speaking, a port is a 2D surface on which the fields will be solved based on Maxwell's Equations to determine appropriate RF model excitations into the 3D model volume. It usually exists where it represents a cross-

section of a stable transmission line system. The field distribution and orientation are the steady-state finite element solutions. Ports provide driven signals and the matched impedances to 50 ohm (actually, the real impedances of the ports are calculated based on their geometric and other relevant situations. Then, HFSS™ uses a built-in post processing algorithm to renormalize the real impedances to 50 ohm). There are two kinds of ports, wave ports and lumped ports. Lumped ports are more suitable to simulate the measurements gathered by Ground-Signal-Ground (GSG) probes [44], and are better for on-Silicon component and micro-strip structure simulations and analysis [44]. Normally, a lumped port connects the signal trace and the perfect E block (ground or a perfect conductor) to set up the current return path for the excitation. A ground ring is used for this purpose, and is also suitable for actual measurement using GSG probes. An equal-potential bar (a virtual block) is defined to set up an inside (air box) perfect E block to connect the two separate parts of the ground ring for building an inside (air box) perfect E boundary. The lumped ports are built between the perfect-E bars and the metal signal traces so that the return current paths can be set up. The width of the ports should not be larger than the signal trace itself [44], and the length should be electrically short. If it was too long, the port would have ignored inductive component [44]. Based on these rules, the lumped ports as shown in Figure 4.3 are constructed as in Figure 4.5. Also, an impedance line was defined on each port. It starts from the perfect E side and ends at the signal metal trace side. The matched impedance of 50 ohm at each port is thus set up. In addition, one port is excited by a signal of 1 W (P_{in}); the other port is set at zero. Note that the port cannot lie at the boundary of two different materials [45], thus the ports and the perfect-E bars are suspended in air.

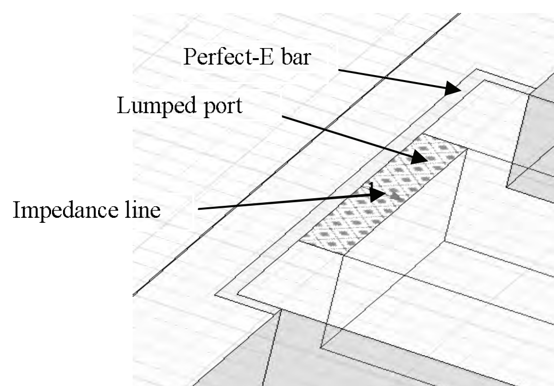


Figure 4.5: Lumped port setup

4.2.2 Combined Substrate Simulation Setup

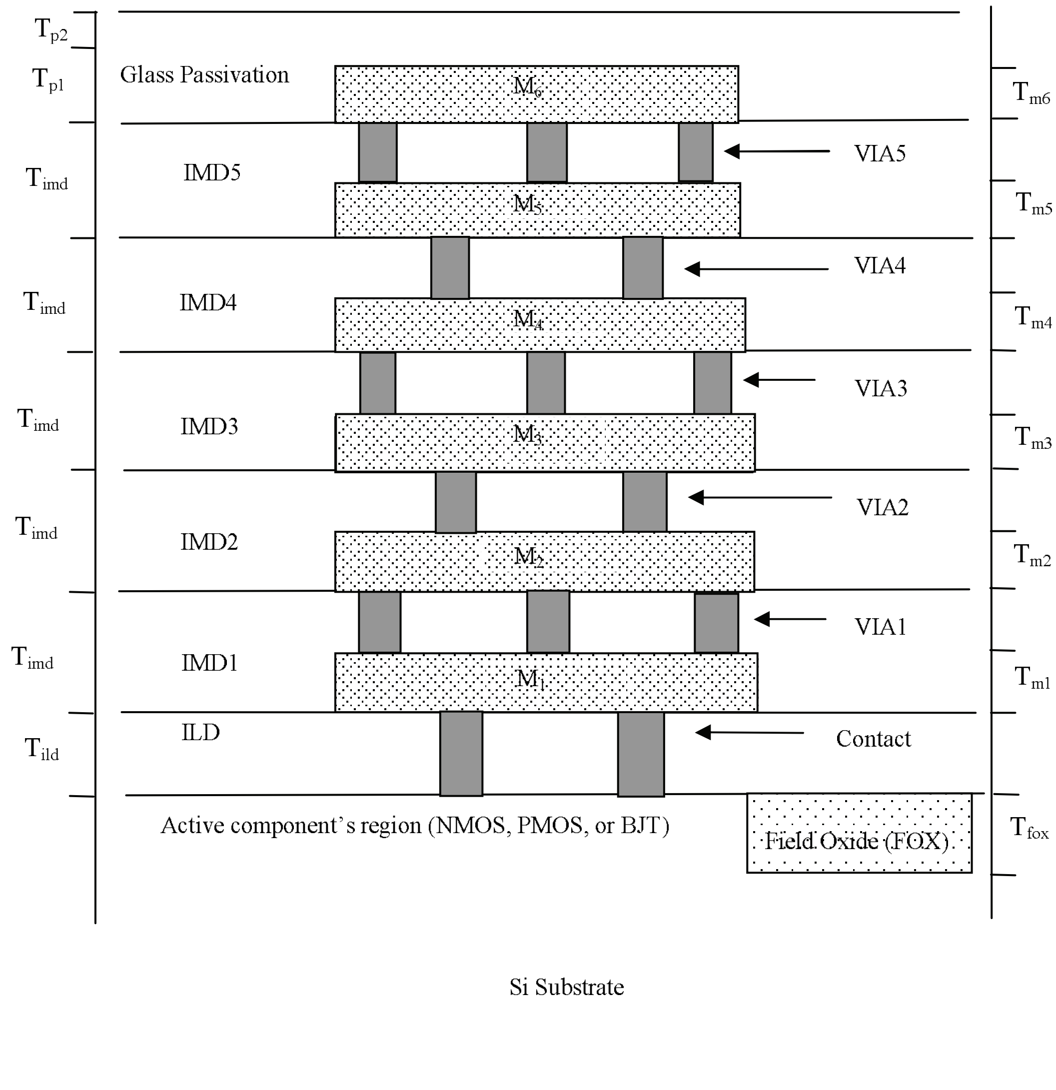


Figure 4.6: Generic cross section view of CMOS and /or BiCMOS devices fabricated with TSMC 0.18µm technique [46].

It is intended to simulate the TSMC 0.18µm CMOS / BiCMOS Si substrate. Figure 4.6 is the corresponding generic cross-sectional substrate layout. In HFSS™ simulation environment, the nominal thickness and distance values are assumed. In practice, the values have some varying range from ±3%-±20%, respectively. Due to the proprietary requirement, the exact data of the TSMC 0.18µm cannot be disclosed in this capacity. As shown in Figure 4.6, the thickness of each dielectric layer is the same and is denoted as T_{imd}, and the correspondent dielectric constant is ε_{imd}. Similarly, the thicknesses of the

passivation layer 1, layer 2, the ILD (inter layer dielectric) layer, and the FOX layer, are defined as T_{p1}, T_{p2}, T_{ild}, T_{fox}, respectively. As well, their dielectric constant are $\varepsilon_{p1}, \varepsilon_{p2}, \varepsilon_{ild},$ and $\varepsilon_{fox},$ respectively. In addition, the six layer metal interconnection thickness are defined as T_{m1}, T_{m2}, T_{m3}, T_{m4}, T_{m5}, and T_{m6}.

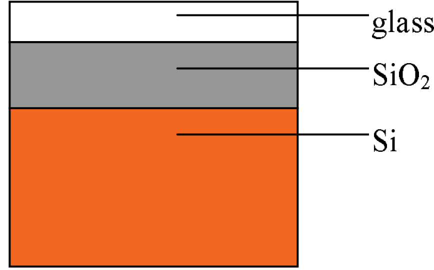


Figure 4.7: Simplified TSMC 0.18µm CMOS device substrate layers

For the simulations, the effects of these various layers are combined in a representative substrate. The combined substrate is simplified to the one shown in Figure 4.7, and includes the Si substrate, SiO_2 isolation (which is a representative combination of the FOX, IMD (inter metal dielectric), and ILD layers shown in Figure 4.6), and glass passivation. Although this simplification could introduce slight errors between simulation results and reality, they are likely small if a representative dielectric is assumed and the inductor is constructed in the reserved region on the CMOS wafer without metal interconnections beneath. For simulation convenience, effective dielectric constants and thicknesses from the data given in Figure 4.6 are calculated as:

$$t_{SiO_2} = T_{fox} + T_{ild} + 5 \times T_{imd} + T_{p1} = 8.7\ \mu\text{m} \tag{4.1}$$

$$\varepsilon_{SiO_2} = \frac{t_{SiO_2} \cdot \varepsilon_{fox} \cdot \varepsilon_{ild} \cdot \varepsilon_{imd} \cdot \varepsilon_{p1}}{T_{fox} \cdot \varepsilon_{ild} \cdot \varepsilon_{imd} \cdot \varepsilon_{p1} + T_{ild} \cdot \varepsilon_{fox} \cdot \varepsilon_{imd} \cdot \varepsilon_{p1} + 5 \cdot T_{imd} \cdot \varepsilon_{fox} \cdot \varepsilon_{ild} \cdot \varepsilon_{p1} + T_{P1} \cdot \varepsilon_{fox} \cdot \varepsilon_{ild} \cdot \varepsilon_{imd}}$$

$$= 3.84 \tag{4.2}$$

$$t_{glass} = T_{p2} = 0.7\mu\text{m}, \quad \varepsilon_{\text{glass}} = \varepsilon_{p2} = 7.9 \tag{4.3}$$

$$t_{Si} = 625\mu\text{m}, \quad \rho_{si} = 10\text{ohm}\cdot\text{cm} \tag{4.4}$$

4.2.3 Spiral Inductor Simulation Model Setup

Two types of spiral inductors were developed in the HFSS^{TM} environment. One is a substrate touching spiral inductor. The other is a suspended spiral inductor. As mentioned in Section 1.5, the suspended type is expected to have advantage in RF characteristics. These two structures are comparable, and the only difference between them is the suspended height.

As mentioned in chapter 2, the key indices of the inductor electrical characteristics are *Q* factor, inductance, and operating frequencies (mainly determined by *SRF*). All sorts of geometric and physical parameters such as trace thickness/width, spacing between traces, and dielectric constant of the isolation layer, can bring strong influences to the three key indices. Thus, various simulations are required to investigate these kinds of influences by varying their values manually or software-automatically. By performing the simulations, optimizations, and the corresponding analysis, one can also get the suitable parameter values to achieve desired RF characteristics. For these two purposes, some independent variables are defined as shown in Figure 4.8 based on the spiral inductor model in Figure 4.3.

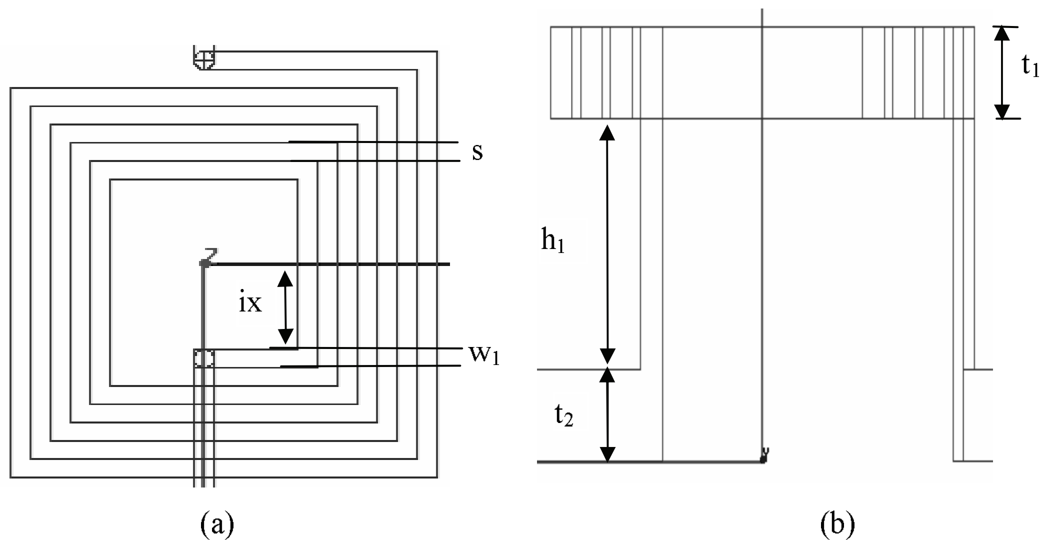


Figure 4.8: Rectangular spiral inductor model simulation variables. (a) Simplified top view; (b) Simplified side view

The distance from the innermost inductor metal trace to the inductor geometric center is defined as ix, the metal trace width is denoted as w_1, the space between adjacent parallel traces is s, and the thickness of the metal traces is t_1.

For the suspended inductor realization, two thick metal pillars are required to raise and support the suspended structure. The suspended height of the inductor coil, which means the height of the supporting pillars, is set to h_1=150μm. When h_1=0μm, the inductor is the substrate touching type and thus the supporting pillars disappear. The turn number of the inductors is denoted as n. However, the representative simulations were mainly conducted based on the n=3.5 because the dependence of Q, L, and SRF on the turn number has already been extensively investigated and well established (for instance [21], [29], and [47]).

For the substrate touching spiral inductor model, the innermost outlet has to pass through the combined substrate (the innermost outlet of the suspended type can also go through the combined substrate, but this is not necessary). Figure 4.9 shows the situation of the innermost outlet of the substrate touching spiral inductor passing through the SiO_2/glass isolation layer. In this capacity, three variables t_{SiO2}, t_{inner}, and $t_{underpass}$ are defined. Ultimately, t_{SiO2} will be fixed at 8.7μm because it simulates the thickness of the actual interconnection/isolation layer (see Figure 4.6), but making it variable allows dependant simulations to explore the influence from the thickness of SiO_2 isolation layer to the RF characteristics of the inductors. t_{inner} is the depth from the top surface of the combined substrate to the top surface of the metal outlet trace inside the SiO_2 layer. In practice, for the substrate touching spiral inductor, the innermost outlet inside the SiO_2 layer should take advantage of the interconnection metal. Thus, one cannot randomly pick the value of t_{inner}. In this design, t_{inner} is fixed at $T_{p1}+T_{p2}+T_{imd(5)}-T_{m5}$ (see Figure 4.6), which simulates the employment of M_5 metal interconnection as the outlet. Variable $t_{underpass}$ represents the thickness of the interconnecting metal.

For most other geometric dimensions, they are the functions of the defined independent unknowns. For example, for the 3.5 turn suspended spiral inductor shown in Figure 4.3

(a), the metal trace width of the inductor coil is defined as variable w_1. The distance between the ground ring (at the sides without ports) and the outside edge of the inductor coil is kept at 6 times of the metal trace width, $6 \times w_1$. In doing so, when a geometric variable changes, the whole structure (including airbox, ground ring, etc.) will change correspondingly. Thus, the simulation results from different values of the same variable are comparable. For the distance between the ground ring and the inductor coil at sides with the two ports, which is the length of the micro-strips acting as viaducts to connect the inductor coil and the anchors, it should be a fixed value. If the micro-strips were lossless, the length variation of the micro-strips would have only resulted in the phase changing of the S parameters on the Smith Chart. In practice, they are lossy. Not only the phase but also the magnitude of S parameters changes accordingly. Thus, the length variations of micro-strips should be fixed. Otherwise the simulation results are incomparable. This concern is also applied to the solenoid inductor modeling.

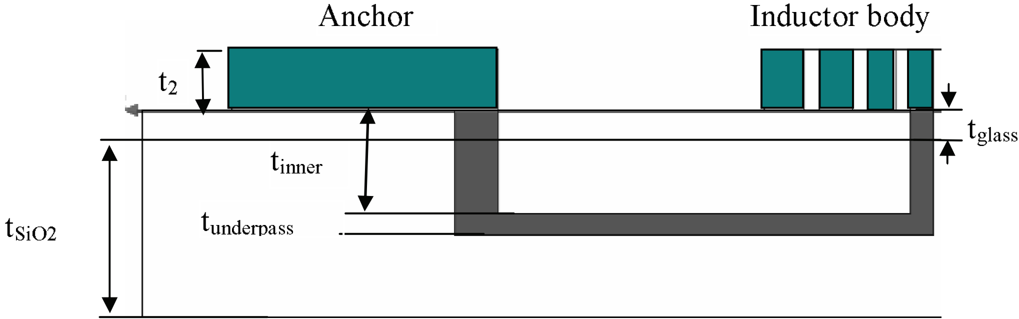


Figure 4.9: Partial cross section situation of the substrate touching spiral inductor

4.2.4 Anchors and Ground Ring Simulation Setup for Spiral Inductors

The anchors are used for the inductor outside connections. They are the physical ports of the designed inductors. When doing the measurement, the Ground-Signal-Ground probe will be put among the two ground rings and the anchor. In this sense, the anchor and the ground rings should share the same thickness. A variable t_2, which is shown in Figure 4.8 and Figure 4.9, is defined to represent the anchor and ground ring thickness. To simplify the layout, the anchors are also set to have the same width as the ground ring traces. The magnetic flux generated by the inductor not only passes through the inductor itself, but also influences the surrounding metals. As shown in Figure 4.10, this

influence incurs eddy currents in the ground ring and thus drains energy from the inductor. This parasite phenomenon results in decrease of the inductance L and the Q factor. The farther apart between the ground rings and inductor coil, the less the parasite magnetic coupling. However, constrained by the limited substrate area occupation of the MEMS devices, one cannot separate these two objects indefinitely. [47] suggested that the surrounding metallization should be placed at least five line widths from the outside edge of the outer inductor winding. In this spiral inductor design, as mentioned previously, this distance is at 6 times of the metal trace width.

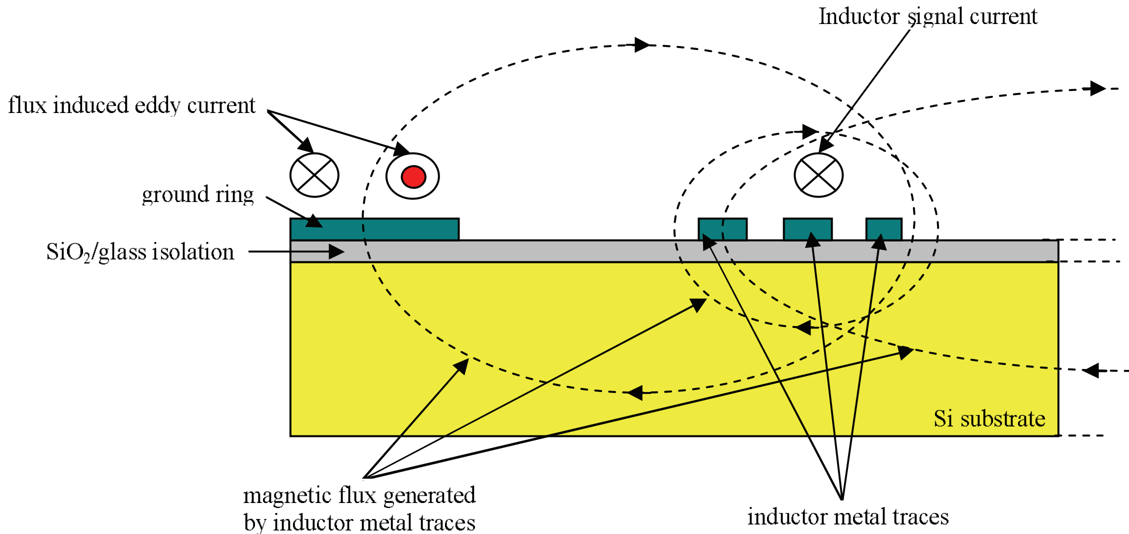


Figure 4.10: Partial cross section view of the magnetic flux and current distributions of the substrate touching spiral inductor

4.2.5 Solenoid Inductor Simulation Models Setup

Similar to the spiral inductor designs, many geometric and physical variables for the HFSS simulations and optimizations are required. The model in Figure 4.3 (b) can be simplified into 2D diagrams, which are shown in Figure 4.11, to illustrate the defined simulation variables. As shown in Figure 4.11, h represents the suspended height of the inductor coil, and also the height of the supporting pillars, in this case fixed at 150 μm. When h=0 μm, the inductor turns into a substrate touching type. h_1 is the height (distance) between upper and bottom horizontal metal traces of the solenoid inductor (vertical distance from bottom face of the upper horizontal metal trace to the upper face

of the bottom horizontal metal trace). t_1 is the thickness of the metal traces which contact the combined substrate. It is set equal to the thickness of anchors, ground rings, and viaducts between the anchors and the inductor coil. t_m is the thickness of the bottom horizontal metal traces of the inductor coil when the inductor is suspended. Obviously, when h=0 μm (substrate touching type), t_m should be set equal to t_1 for the fabrication convenience. t_2 is the thickness of top horizontal metal traces. For the suspended situation, $t_2=t_m$. $2\times ix$ is the horizontal bottom span distance ($\pm x$ direction) between the two slanting (non-horizontal) metal beams in the same turn of the inductor coil. r_b is the radius of the supporting pillars. y_g is the horizontal span distance between the adjacent turns. Evidently, the varying range of y_g must be greater than $2\times r_b$. Otherwise, the bottom sides of the two adjacent turns would have contacted each other. For convenience, an interim variable $y_{gvari}=y_g-2\times r_b-20$ μm was defined. It is equivalent to simulate the variation of y_{gvari} instead of y_g because of the linear relationship between them.

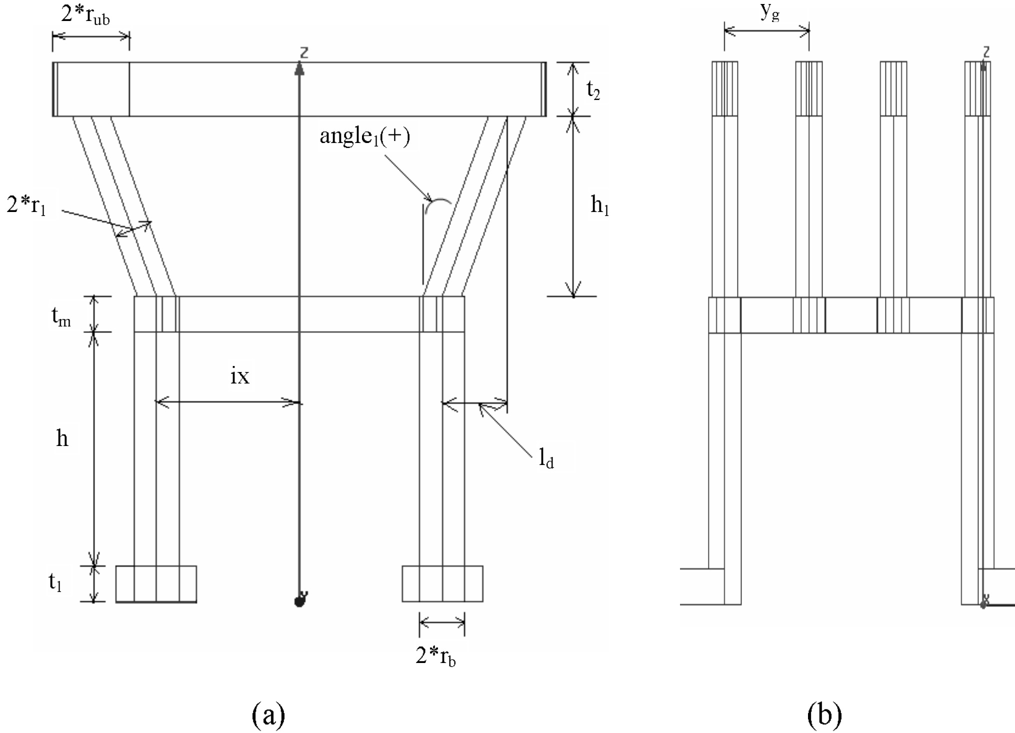


Figure 4.11: Simplified view and simulation variable illustration of the solenoid inductor model (a) Side view; (b) Front view

To correctly simulate the LIGA structural inductors, various fabrication issues should also be considered and taken advantage of in the model designs. For example, deep X-ray beams in the LIGA process cannot only be projected perpendicularly, but can be incident at a slanting angle using inclined exposure. Therefore, the side metal beams of the solenoid inductor can be slanted to a non-perpendicular position, and new geometric flexibility can potentially provide improvements to the inductor characteristics. Variable $angle_1$ is thus defined. Figure 4.11 (a) shows a positive $angle_1$ case. If $angle_1$ is negative, the bottom horizontal traces should be longer than the top counterparts. The two supporting pillars could be built using the pattern transfer technique introduced in Section 2.1. Once the two pillars are fulfilled, the suspended inductor coil could be fabricated with direct X-ray exposure. If the fabrication goes with direct X-ray exposure, the multi-exposure technique introduced in Section 3.2.2 should be used. The slanting beams of the inductor coil could be fabricated using slanting X-ray exposure. For the inductor coil shown in Figure 4.12, the bottom horizontal metal trace comprises two cylinders and one rectangular bar to connect them. To properly build the slanting

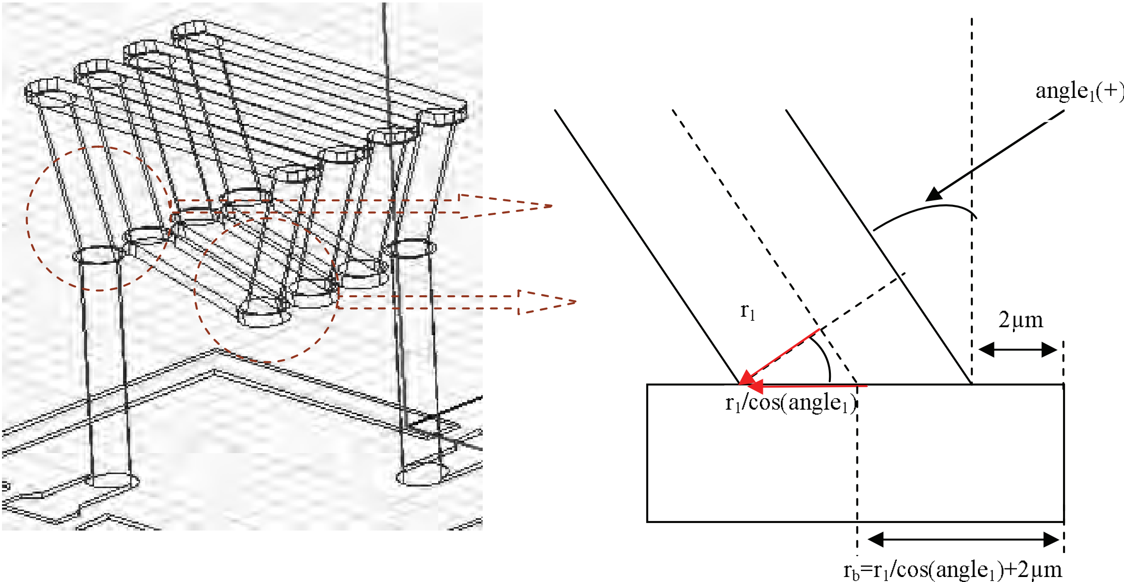


Figure 4.12: The relationship between variable r_1 and r_b in model design

beams on top of them, the projected X-rays must be aligned with the centers of the top circular surfaces of the supporting pillars and the thin cylinders at the two sides of the

bottom horizontal trace. In practice, with the slanting X-ray projection it is difficult to align precisely for the centres. Therefore, one can set up the radius of the slanting beams r_1, and also the radius of the X-ray, to be $(r_b\text{-}2\mu m)*cos(angle_1)$, which is shown in Figure 4.12. In doing so, when the X-ray projection misses the centers of the circular surfaces, the generated slanting metal beams can be still limited in the circular surface area (the reported LIGA lateral resolution is 0.2 µm). Thereby, this set up prevents some unwanted structure from happening. As well, the thicker pillars (2 µm thicker than r_1) help strengthen the robustness of the suspended structure. As for the top horizontal trace setup, similar to the bottom counterpart, it is also made up of two thin cylinders and one rectangular bar to connect them.

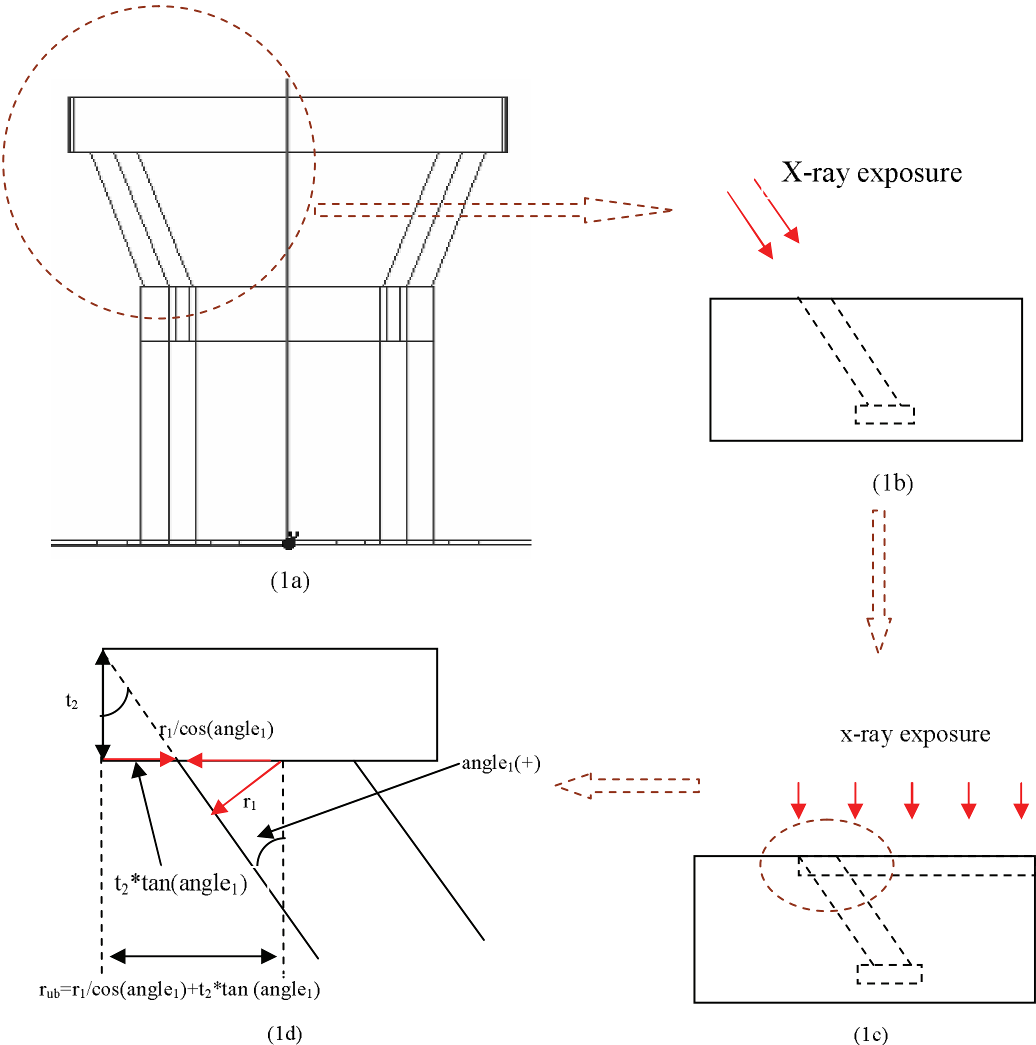


Figure 4.13: Variable r_{ub} set up when $angle_1$ is positive

As mentioned before, slanting side beams are built with slanting X-ray exposure, the top horizontal traces are built with perpendicular X-ray exposure. This results in some constraint between the radius of the top cylinder rub and the radius of the slanting beam r_1 in practice. Specifically, when the X-ray beam projects into the photoresist at a positive angle, the radius of the top cylinder r_{ub} should be $r_1/cos(angle_1)+t2\times tan(angle_1)$, which is shown in Figure 4.13; when the X-ray beam

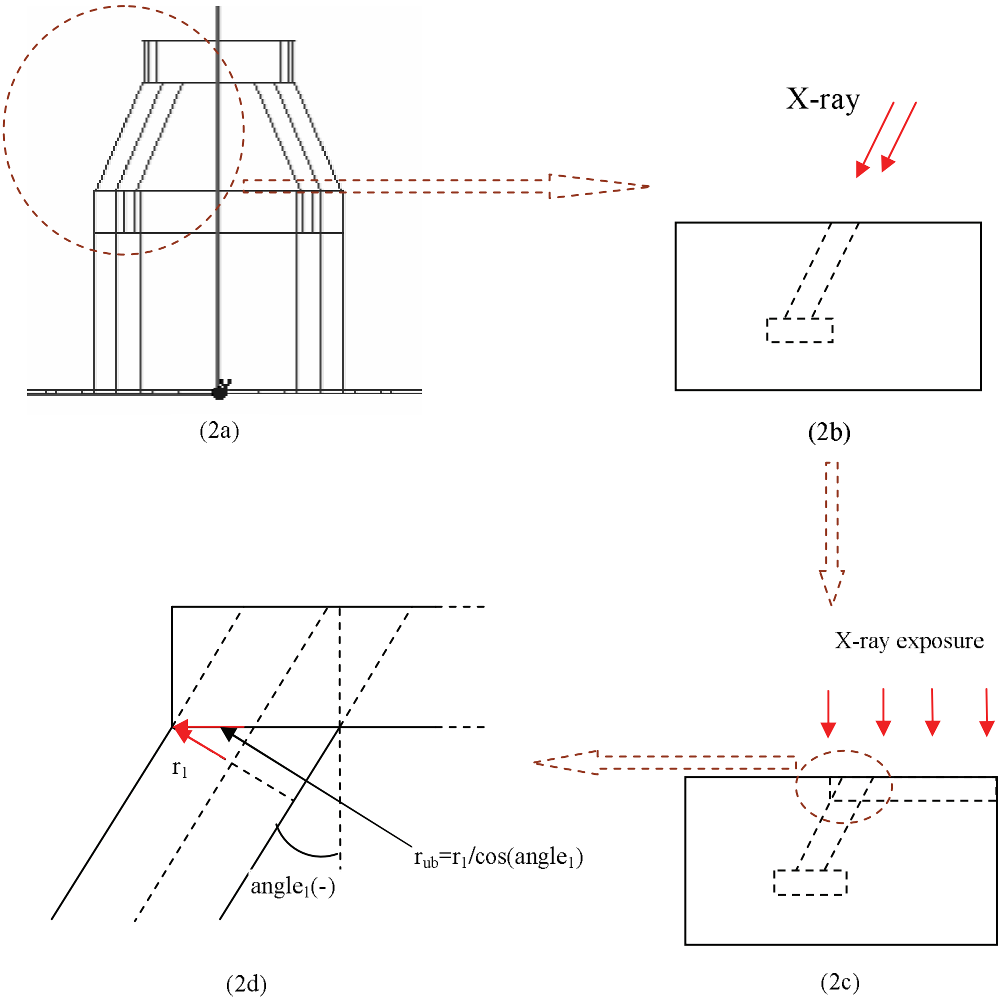


Figure 4.14: Variable r_{ub} set up when $angle_1$ is negative

projects at a negative angle, which is illustrated in Figure 4.14, r_{ub} should be $r_1/cos(angle_1)$. Because one needs to build a universal model to do the simulations and optimizations, it is necessary to combine these two situations together. The ultimate definition of $r_{ub} = r_1/cos\ (angle_1)\ +t_2\times(abs\ (tan\ (angle_1))\ +tan\ (angle_1))/2$. Finally,

similar to the spiral inductor modeling, most other geometric parameters (dimensions) in this solenoid inductor modeling are set to be functions of defined independent unknowns. For example, in this design, as shown in Figure 4.15, the ground ring is placed at the distance $2\times(l_d+r_{ub}+ix)$ from the central geometric point (this is for the ground ring at the sides without physical ports, for those at the port including sides, the distance is fixed), where $l_d = (h_1\times tan\ (angle_1)\ +h_1\times abs\ (tan\ (angle_1)))/2$. When the $angle_1$ is positive, the ground ring distance from the central geometric point is two times of $ix+r_{ub}+h_1\times tan\ (angle_1)$. When it is negative, the ground ring distance is $ix+r_{ub}$. Considering the geometric difference between the $+angle_1$ situation and the $-angle_1$ situation, this setup makes the ground ring have almost the same electromagnetic influences when $angle_1$ changes. As a result, the simulation results for different $angle_1$ cases are comparable.

In all modeling, the metal seed layers are ignored and considered consistent with the inductor material for electrical performance. Deviation from this assumption (especially thick seed layer) may impact the results.

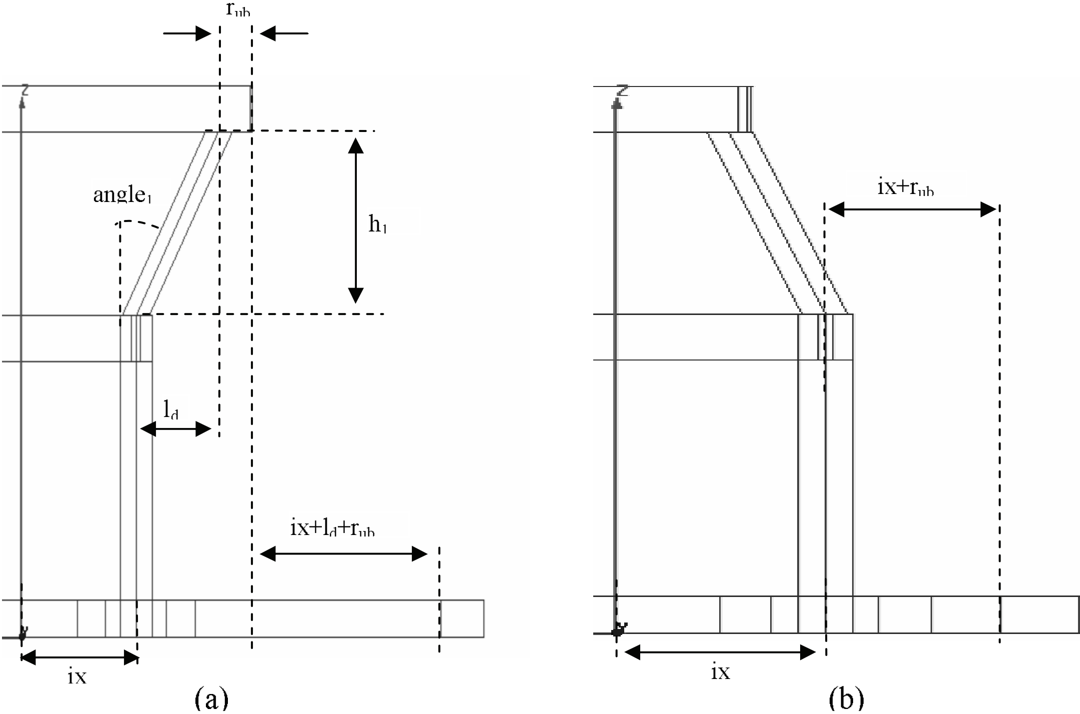


Figure 4.15: Some detail in ground ring set up. (a) angle1 is positive; (b) angle1 is negative

4.3 Brief Discussions of the Proposed Combination with CMOS

Although the focus here is not on fabrication process designing, but the modeling and characteristics analysis of LIGA structural inductors, it is necessary to briefly discuss the possible fabrication processes to make sure that simulation modeling and simulation results are practically meaningful. Strictly speaking, CMOS compatible post processing with the LIGA technique has not been formally developed. However, recent progress in this and relative research field has made some individual situations and cases practically realizable. The fabrication discussion is based on these reported successful cases.

Figure 4.3 illustrates the prototype modeling for testing. The anchors, and microstrips (viaducts), which connect the anchors and the inductor coil/suspending pillars are all for prototype measurement purpose. In real on-chip integration, they do not exist. However, a ground ring is probably necessary to realize the electromagnetic isolation from surrounding circuits. Section 3.2.2 gave a good approach of taking advantage of the top interconnection metal layer M_6 (see Figure 4.6 and Figure 3.7) as the ground of the inductor. Therefore, in practical applications, only the suspending pillars and inductor coil are necessarily needed to be fabricated using the post CMOS LIGA processing. The suspended pillars can be connected with other circuits or components via the open pads which are fabricated during the preceding chip fabrication process and reserved for the post-CMOS LIGA processing (please refer to Section 3.2.2).

As for the designed suspended spiral inductors, one can see the same pattern transfer technique reported by [5] in its example inductor fabrication can be suggested for the inductor designed in this dissertation. For the suspended solenoid inductors, the two suspended pillars can be built using pattern transfer process. After the suspended pillars are fulfilled, to build the suspended inductor coil, a polymer layer at the thickness of the suspended pillar will cover the substrate and will not be etched away until the inductor coil is built up. Because of this thick polymer layer isolation, the direct X-ray exposure process can be employed without damage to the substrate.

5 Simulation, Analysis, and Optimization for the LIGA Air Core Inductors on CMOS/BiCMOS Substrate

In chapter 4, the model design was discussed. This chapter presents the high frequency simulations using Ansoft HFSS™. As mentioned in the previous chapters, Q factor, inductance, and Self Resonant Frequency (SRF) are three key performance indices. Two types of simulations are conducted based on S, Z, and Y parameter measurements, those versus frequency and also versus various geometric parameters. Based on the simulation generating Y parameters, two key indexes, Q and inductance are defined as follows:

$$Q = -\frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} = \frac{\mathrm{Im}(\frac{1}{Y_{11}})}{\mathrm{Re}(\frac{1}{Y_{11}})} \tag{5.1}$$

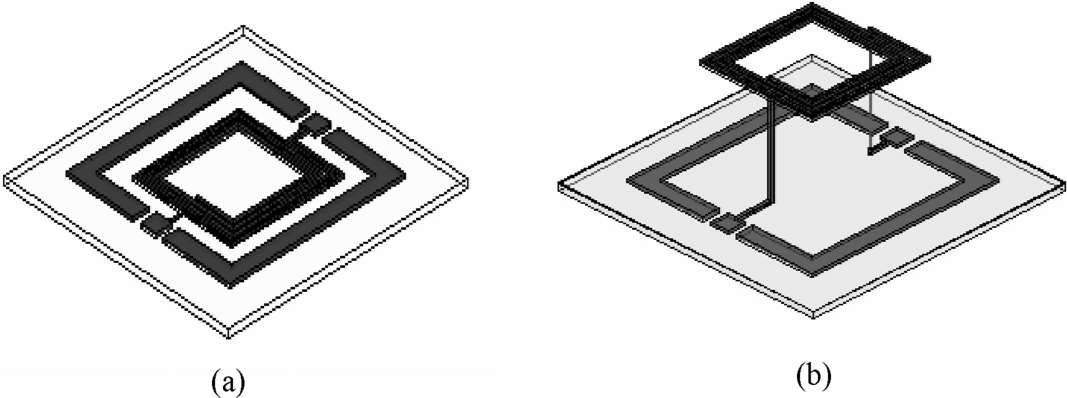
$$L(nH) = \frac{10^9\,\mathrm{Im}(\frac{1}{Y_{11}})}{2\pi f} \tag{5.2}$$

From Equation 5.2, one can see the inductance is actually defined as the general susceptance of the inductor model (including the inductor wire and the substrate parasitics), not the pure inductance of L_s (see the lumped model in Figure 2.6). This is because the L_s is submerged by the capacitive parasitics and cannot be seen by current HFSS simulator. On the other hand, the capacitive parasitics is always attached to L_s. For only investigating the general inductor performance, the general suspeptance analysis is practical and good enough. However, in the future work, if there is some suitable tool available, it is worthy doing some individual investigation for L_s and relevant capacitive/resistive parasitics to further reveal their individual and combined influence to the inductor performance.

The simulation scheme is to build an incipient model at first, then to vary various geometric parameters specified in chapter 4 and to do the corresponding frequency sweeping based on them. In doing so, their dedicated influences to the *Q*, inductance, and *SRF* can be revealed. In practice, at certain frequency points, geometric or physical parameter variation can bring contradictory influences to the inductor characteristic. The comprehensive influences from all the parameters are really a tradeoff. The goal for the various parameter simulations is to analyze their influences on the inductor characteristic and then find the suitable starting values for the subsequent optimizations. Also, the simulation results between the substrate touching types and the suspended types will be compared. In doing so, the advantages of the suspended approaches for the inductor designs can be further revealed.

Rigorous electromagnetic field distribution analysis inside the inductor structures versus frequency is difficult, particularly for the solenoid types. There are reported papers providing incomplete analysis from the field perspective for the substrate touching spiral inductors, and no well-acknowledged analysis for the solenoid types has been reported. On the other hand, the inductor lumped model discussed in chapter 2 is comparatively easy to understand and the simulation results, although electromagnetically based, are more conceptually meaningful to discuss in the context of the lumped model parameters.

5.1 Simulation Analysis of the Square Spiral Inductors



(a) (b)

Figure 5.1: Simplified incipient models of spiral inductor. (a) Substrate touching type; (b) Suspended type

Table 5.1: Square spiral inductor model incipient data

Variable	Incipient value	Unit	Comments
ix	70	μm	See Figure 4.8
h_1	0, 150	μm	0μm is for substrate touching type, 150μm is for suspended type. See Figure 4.8
w_1	15	μm	See Figure 4.8
t_1	5	μm	See Figure 4.8
s	5	μm	See Figure 4.8
t_{inner}	2.5	μm	$T_{p1}+T_{p2}+T_{imd(5)}-t_{m5}$, see Figure 4.9 and Figure 4.6
$t_{underpass}$	0.53	μm	t_{m5}, see Figure 4.9
t_2	t_1	μm	see Figure 4.9
t_{SiO2}	8.7	μm	see Figure 4.9 and Equation (4.1)
t_{glass}	0.7	μm	see Figure 4.9 and Equation (4.3)
ρ_{si}	10	ohm·cm	see Equation (4.4)
ε_{glass}	7.9		see Equation (4.3)
ε_{SiO_2}	3.84		See Equation (4.2)

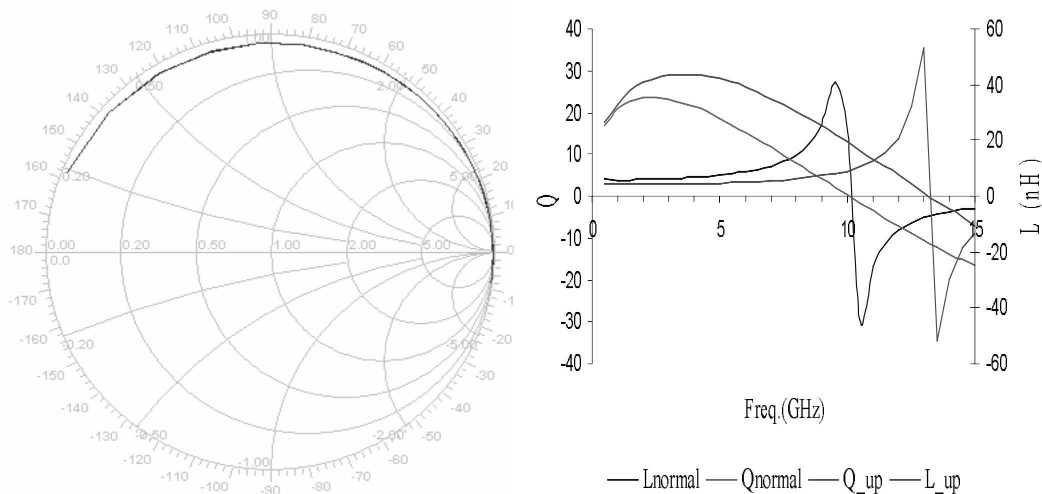


Figure 5.2: (a) Simulated S parameters. (b) Q and L curves of the spiral startup models

For comparison purpose, two incipient models whose simplified layouts are shown in Figure 5.1 were built. One is a substrate touching type; the other is a suspended type. They are only different in variable h_1. The data for both incipient models are listed in Table 5.1, and correspond to variables discussed in Section 4.2. Simulation results for these two types of inductors are shown in Figure 5.2. As mentioned in Section 2.5, one port is shorted as defined by its Y-parameters, which reduces the inductor to a one port device.

The simulated S parameters for the suspended spiral inductor are shown in Figure 5.2 (a). There are two S parameters, S_{11} and S_{22} in the figure. One can see the S parameters are inductive in most of the curve because they are not only located in the upper part of Smith Chart, but also very close to the pure imaginary circle, r=0. When frequency goes up, after a certain frequency point, the curves turn to the lower part of the Smith Chart, indicating the component is capacitive. At the point crossing the horizontal axis, the curve reaches the *SRF*. As mentioned previously, the simulated inductor has only one port. Thus, in practice, S_{11} and S_{22} are obtained in two separate simulations. When simulating S_{11}, port 2 is shorted. When simulating S_{22}, port 1 is shorted. The two outlet metal traces of the inductor are not symmetric. One outlet connects the outermost turn of the coil, while the other connects the innermost turn of the inductor. This imbalance should have brought a slight difference between the curves of S_{11} and S_{22}. However, because these two curves are so reactive that they both are really close to the pure imaginary circle in this figure, it is difficult to tell the difference.

In Figure 5.2 (b), the Q factor and inductance of the substrate touching inductor are denoted as Q_{normal} and L_{normal}, and those for the suspended type as $Q_{_up}$ and $L_{_up}$. One can see both types of curve trajectories are similar to the one exhibited in Figure 2.13. Figure 5.2 (b) can also be interpreted with the frequency domain analysis in Section 2.5. From the curve trajectories, one can see the property of the suspended model is much better than the substrate touching counterpart. This improvement mechanism has been discussed in Section 2.5. By suspension, the peak Q point and the *SRF* are all pushed to the higher frequencies, and the peak Q value also rises. On the other hand, as mentioned

in Section 2.4.1, at low frequencies, the substrate loss effect can be ignored, and $Q \approx \omega L_s/R_s$ (see Equation 2.31) because it is very weak. From this viewpoint, at low frequencies, the suspended structure does not have too much advantage over the substrate touching type. That is why at low frequencies, the Q and L trajectories for both suspended and substrate touching types are very close, which means at low frequencies, suspension has little influence to the inductor property.

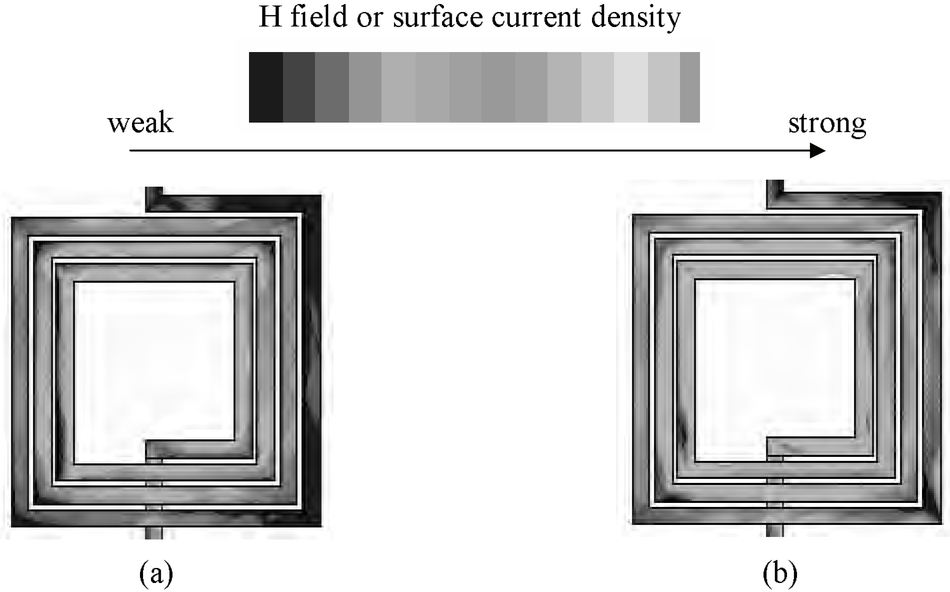


Figure 5.3: Top view of the spiral inductor (a) Surface current distribution (b) Magnitude H field distribution

Figure 5.3 exhibits the surface current and magnetic field distributions of the substrate touching type inductor (the suspended type has the similar situation). The lighter the color, the stronger the magnetic field and the surface current. One can see that the magnetic field reaches a peak in the center of the spiral inductor, then it fades gradually when the metal coil winds outwards. Accordingly, the surface current has the similar situation and tread to the magnetic field. Note that in Figure 5.3, the displayed field and current are the summation of the excitation field and current plus the parasite counterparts. Specifically, excitation current generates the excitation magnetic field. The excitation magnetic field then creates eddy current due to skin and proximity effects as discussed in chapter 2. Eddy current offsets the excitation current as well as produces

parasite magnetic field to oppose the original excitation field. The distributions of eddy current and thus the eddy current generated parasite magnetic field are complicated. Normally, eddy current flows on the two sides of the metal trace [25]. That is why some places on the outer edge of the innermost turn looks very dark and even darker than the outer turns. This is because strong eddy current and parasite magnetic field are there and they largely offset the original current and field. Eventually, the total field and current are also largely weakened.

5.1.1 Varying t_1

Various simulations based on the incipient models were done by varying geometric parameters. The first simulations vary t_1, the thickness of the metal trace of the inductors, from 1 µm, 3 µm, 5 µm, to 10 µm, for both the substrate touching and suspended types. From the simulation results illustrated in Figure 5.4, an interesting phenomenon can be found. When t_1 changes from 1 µm to 3 µm, the Q factors improve significantly to higher frequencies. As well, the *SRF* is also largely pushed to a higher frequency. However, when t_1 continues to increase after 3 µm, there is no significant difference in the Q and L simulation results for both suspended and substrate touching cases. This mainly arises from the more severe skin effect in the thicker spiral. According to the skin depth definition in equation (2.19), the skin depth of copper at 2.5 GHz and 12 GHz is 1.32 µm and 0.6 µm respectively. At the depth more than skin depth inside the metal trace, the field attenuates to the $1/e$ of the surface field strength. That means most of field and current are limited the surface of the metal trace. When the thickness is more than 3 µm, for example 5 µm, the added 2 µm thickness contributes little to the field and current distribution. From the lumped model perspective, it is easy to see that varying t_1 mainly influences R_s (see Section 2.4.1). Due to skin effect, after a few skin depths, enlarging the metal thickness cannot effectively lower the R_s. That is why the Q and L simulation results for t_1=3 µm, 5 µm, and 10 µm do not have evident difference. The effective thickness, t_{eff}, of the metal trace based on Equation (2.22) are shown in Table 5.2. From the table, one can see, after 3 µm, the effective thickness changes very slowly and slightly.

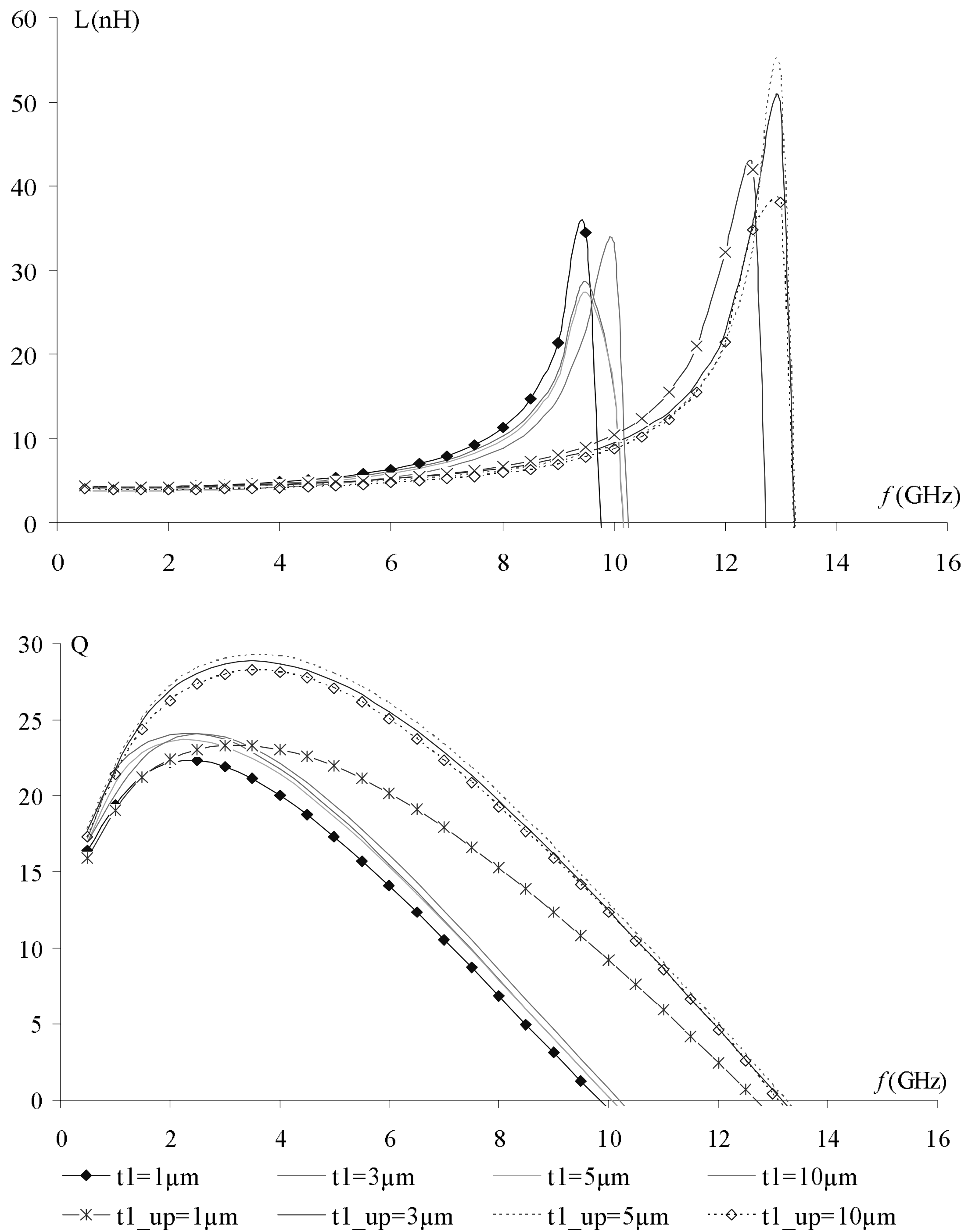


Figure 5.4: Comparison of the simulation results for the t_1 variations. (a) Inductance comparisons; (b) *Q* factor comparisons

Table 5.2: The effective thickness of inductor metal trace when the metal traces are 1 μm, 3 μm, 5 μm, and 10 μm

			metal thickness (μm)			
t_{eff}	frequency(GHz)	skin depth(μm)	1	3	5	10
	2.5	1.32	0.7	1.18	1.28	1.31
	12	0.6	0.49	0.596	0.5998	0.5999

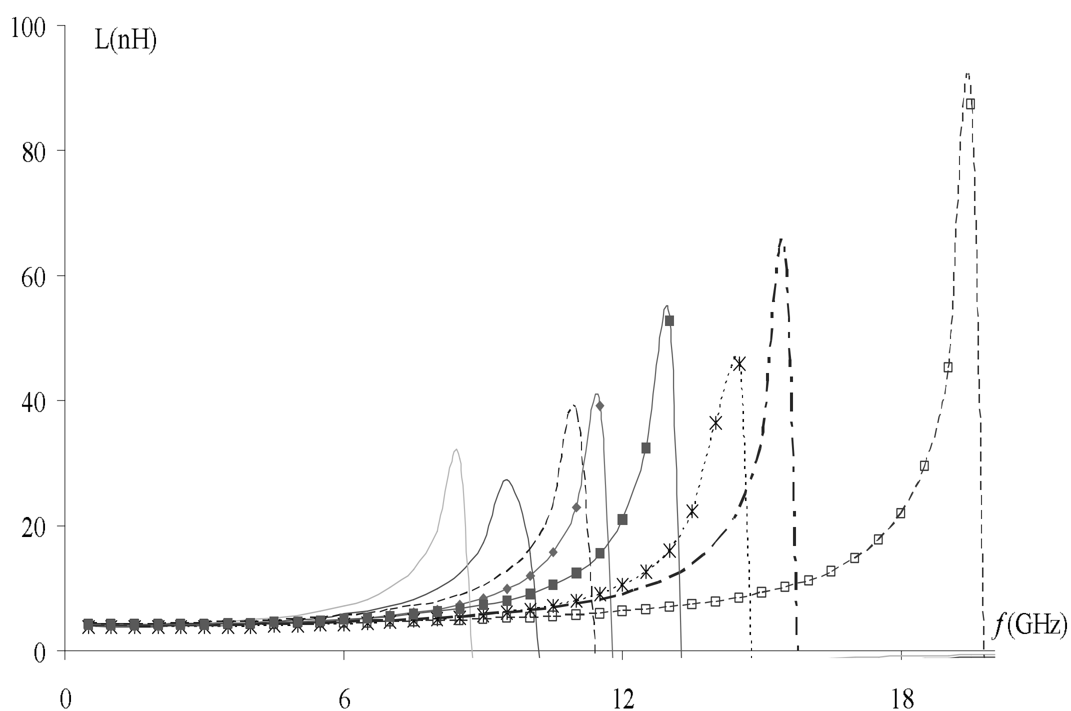
As said in the beginning of this chapter, this kind of frequency and parameter sweep simulations are also used for setting up the initial value for the subsequent optimizations. For the variable t_1 at CMOS situation, the initial value of 10 μm, which is a few times of the skin depth at 2.5 GHz, is chosen. As mentioned in Section 2.4.1, for spiral inductors, the eddy current concentrates on one surface of the metal trace. However, for solenoid inductors , the current distribution is more complicated and the t_{eff} can not directly use equation (2.22) to calculate. The corresponding simulation results are shown in Figure B6-7 in the appendix.

5.1.2 Varying w_1

Figure 5.5 and Figure 5.6 show the simulation results of varying variable w_1, the width of the metal trace of the inductor. Frequency domain simulations were done at individual values of 5 μm, 10 μm, 15 μm, and 20 μm for both substrate touching and suspended types, respectively. From the simulation results, one can see at low frequencies, the substrate parasitic effects are not significant because they are capacitive and thus can be neglected. Thus, larger w_1 results in less ohm loss. On the other hand, w_1 variation brings increase in metal trace circumference, which is the dominating factor for inductance at low frequencies in this capacity. It thus results in inductance increase. However, the enlarging w_1 is relatively equivalent to decrease the inter wire air gap. From magnetic field flux distribution analysis, the inductance is primarily determined by the magnetic flux external to the wires. In general, the wires with smaller cross-section area have a slightly larger inductance because they generate more magnetic flux external to the wires. Thus, the relatively decreasing inter wire air gap downturns the inductance. The comprehensive influence from above two factors makes the corresponding L

variation at low frequencies very small as shown in Figure 5.5. Specifically, for substrate touching case, at 0.5 GHz, when w_1 varies from 5 μm to 20 μm at an increasing step of 5 μm, the resulting L variation is only around 0.4 nH. For the suspended case, the L variation at 0.5 GHz is much smaller and is only around 0.1 nH. And the variation is not a strictly increasing function versus w_1. An explanation for this is because in this occasion, the inductance downturn mentioned above is comparable to the inductance increase resulting from the circumference enlargement. The comprehensive influence is complex. This brings the complexity of the curve tendency. An explanation for the smaller variation of the suspended case is that the two suspended pillars contribute significantly to L. And they are constants when w_1 changes, which further constrains the L variation range. The very small L variation when the w_1 changes gives advantage to investigate the substrate effects. That is, in some sense, the L influence can be ignored or at least can be considered as a secondary factor for the inductor characteristics. According to Equation (2.31d), at low frequencies, $Q \approx \omega L_s/R_s$, $L_s \approx L$, at the situation that R_s decreases significantly while L_s varies much less, one can see the Q increases.

However, larger w_1 inductor has larger occupation area. According to Equation (2.25) to (2.27), it results in larger C_{ox}, C_{si}, and R_{si}, which means stronger substrate loss. At high frequencies, the substrate loss effects become more significant and eventually dominate. Therefore, an inductor with smaller w_1 pushes the Q peak to a higher value and a higher frequency as shown in Figure 5.6. And the *SRF* of the smaller w_1 inductor has also been pushed higher as shown in Figure 5.5. As a result, the starting value for the optimization is w_1=5 μm. As well, the similar simulations based on variations of ix, s, the isolation layer thickness t_{SiO_2}, and the inductor metal trace material were performed respectively. The corresponding results are shown in the Appendix. The analyses are similar to the varying w_1 and t_1 situations.



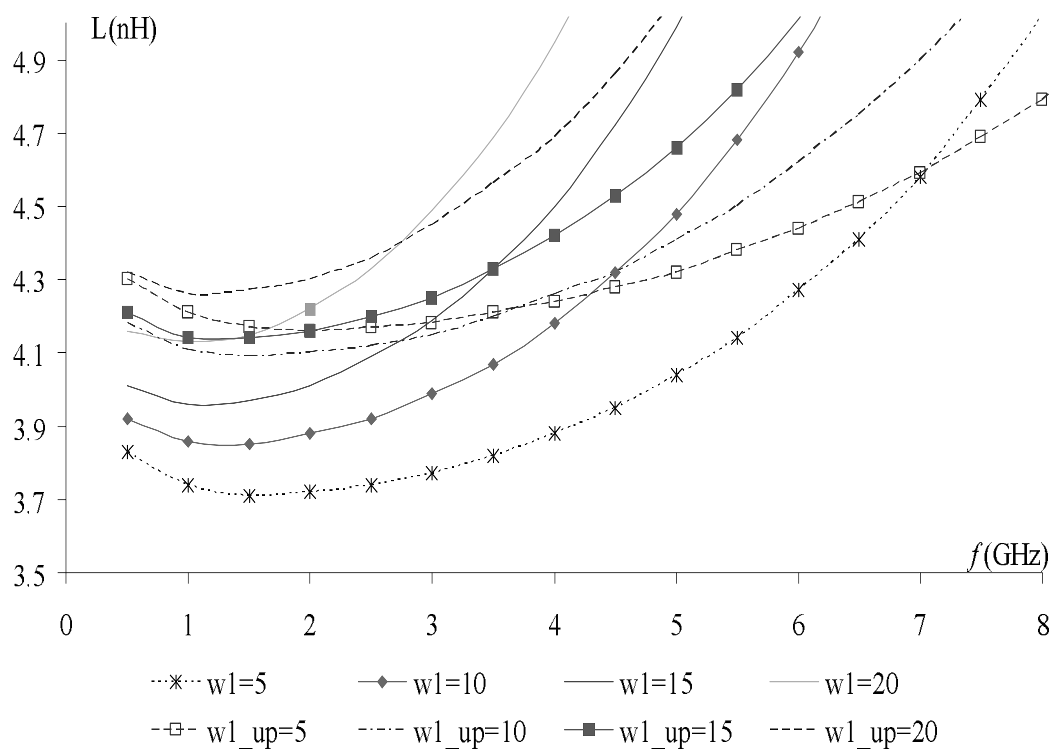
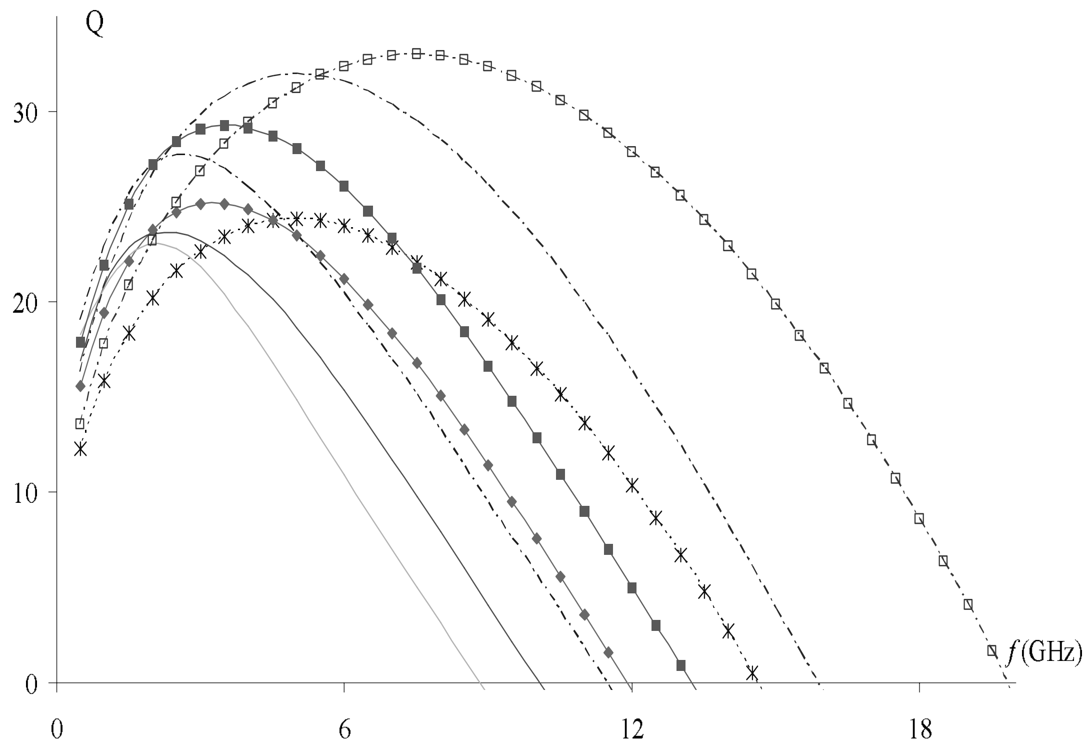


Figure 5.5: Comparison of inductance simulation results for w_1 (in unit of μm) variations.



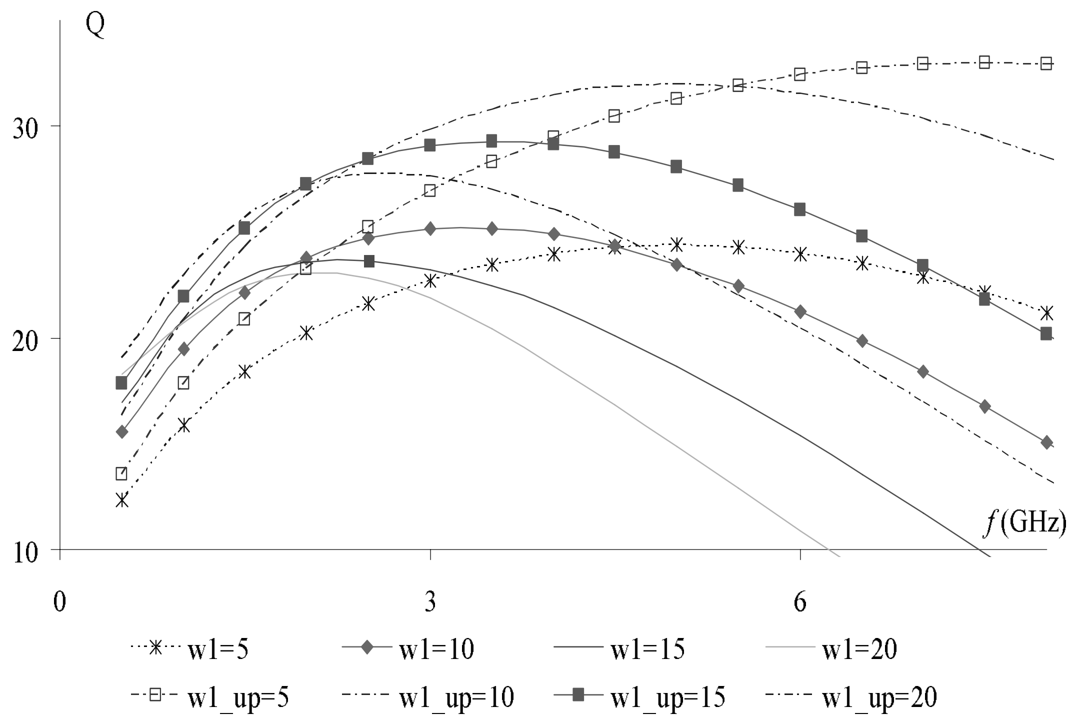


Figure 5.6: Comparison of Q simulation results for w_1 (in unit of µm) variations.

5.2 Simulation Analysis of the Solenoid Inductors

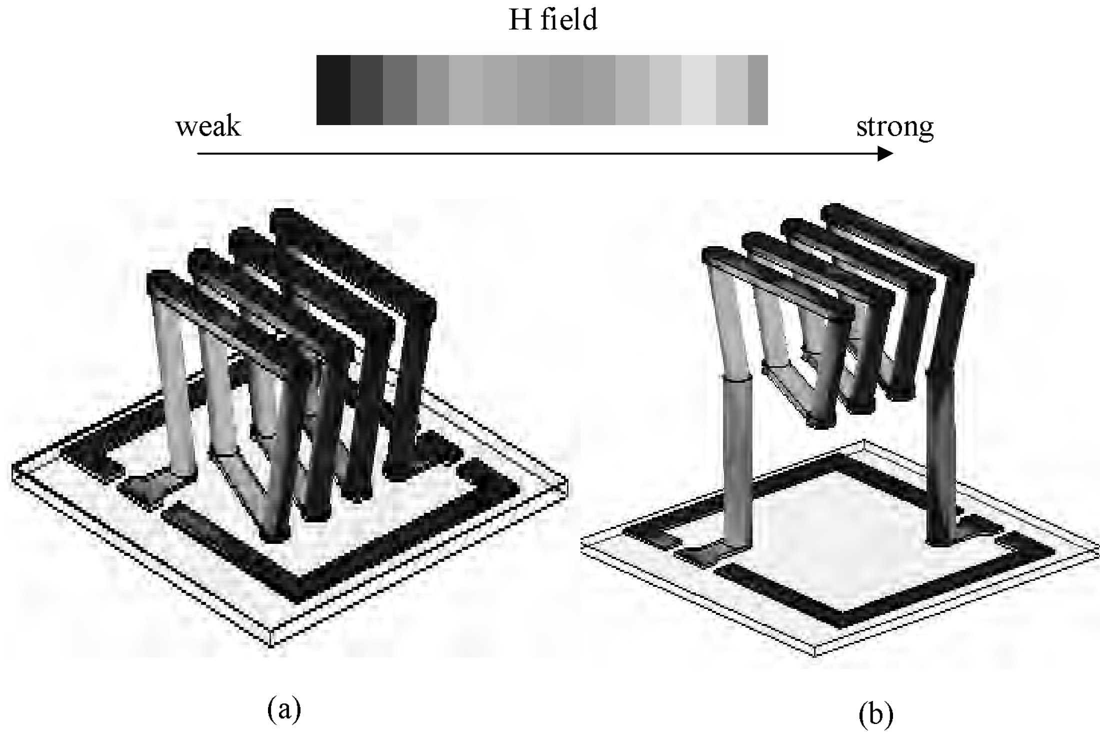


Figure 5.7: Simplified startup models of solenoid inductor. (a) Substrate touching type; (b) Suspended type

Similar to the spiral case, two solenoid startup models are illustrated in the simplified models in Figure 5.7. They are different in the suspended height, variable h_1. This figure also shows the magnetic fields distributions. Actually, the corresponding current distributions are quite similar to the magnetic field counterparts. One can see the magnetic fields concentrate on the inside edges of the solenoid turns. Similar to the spiral case, the shown field and current are the summations of the original excitations and the induced parasites. The data for these two startup models is listed in Table 5.3. This data corresponds to variables discussed in Section 4.2.5, and is displayed from Figure 4.11 to Figure 4.15. The simulation results for these two startup models are shown in Figure 5.8. Similar to the spiral case, the Q factor and inductance for the substrate touching model is denoted as Q_{normal} and L_{normal}, whereas the counterparts for the suspended type are $Q_{_up}$ and $L_{_up}$, respectively. The simulation characteristics in Figure 5.8 as with the spiral ones, demonstrate the advantage of the suspended type.

This advantage can also be found in Figure 5.7, where the color at the inner side of each turn in the suspended type is far brighter than the substrate touching counterpart. This means the magnetic field inside the suspended type is much stronger.

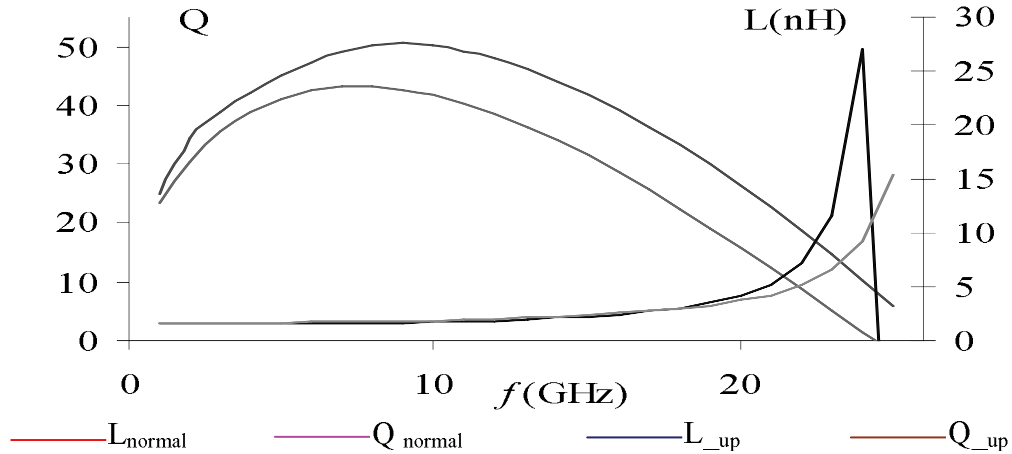


Figure 5.8: Q and L curves of the solenoid start up models

Table 5.3: Solenoid inductor startup model data

Variable	Startup value	Unit	Comments
h_1	100	μm	See Figure 4.11
$angle_1$	20	degree	See Figure 4.11
r_1	15	μm	See Figure 4.11
t_2	8	μm	See Figure 4.11
ix	80	μm	See Figure 4.11
y_g	$2\times r_b+10$	μm	See Figure 4.11
t_{glass}	0.7	μm	See Equation (4.3)
t_{SiO_2}	8.7	μm	See Equation (4.1)
t_1	3	μm	See Figure 4.11
h	0, 150	μm	See Figure 4.11
ρ_{si}	10	ohm·cm	see Equation (4.4)
ε_{glass}	7.9		see Equation (4.3)
ε_{SiO_2}	3.84		See Equation (4.2)

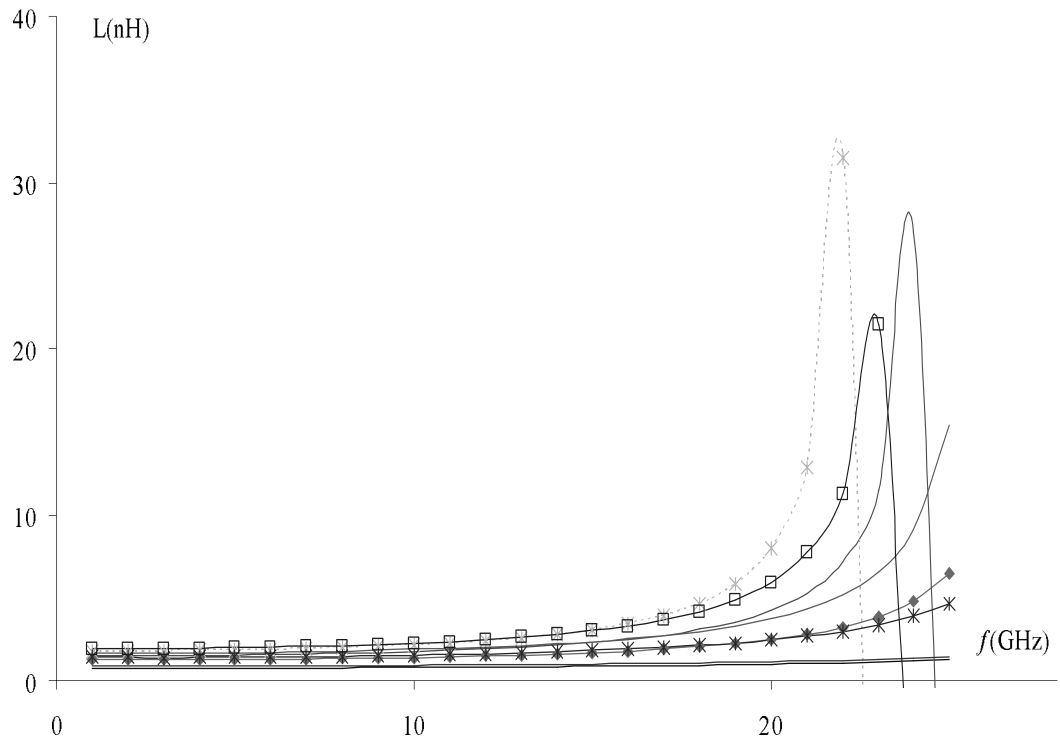
5.2.1 Varying h_1

Similar to the spiral case, various parameter simulations to find suitable start points (values) for the subsequent optimizations were performed. Figure 5.7 shows that the top and bottom horizontal conductors are not parallel. Thus the stray parasite C_{bt} in Figure 2.15 has been decreased. Also because the vertical conductors are cylindrical, not flat, the stray capacitance between them is comparatively small. As the lumped model in Figure 2.15 anticipated, this kind of capacitance can be ignored. First the vertical distance (h_1, see Figure 4.11) between the top and bottom horizontal metal traces of the solenoid inductor is varied and its influence on the inductor property is investigated. The simulation results are illustrated in Figure 5.9-Figure 5.11. With the increasing of h_1, the circumference/cross-section of one inductor turn is enlarged, and the total length of the inductor metal trace extends. This results in the inductance going up accordingly. This can be seen in Figure 5.9. As mentioned in Equation (2.31d) and Section 5.1.2, at low frequencies, $L \approx L_s$ and L dominates. This leads to the Q improvement and also the peak Q value improvement at low frequencies, which is shown in Figure 5.10. Figure 5.11 illustrates the h_1 parameter sweep simulation results. It shows at 9 GHz, with the growing of h_1, the Q and L values both increase.

However, when h_1 grows, the *SRF* backs off to a lower frequency. As mentioned in Section 2.6, the lumped model shown in Figure 2.6 can also be roughly used for solenoid inductor analysis. Therefore, from Equation (2.32), h_1 increasing enlarges both L_s and R_s. At high frequencies, because of the more significant skin effect (thinner skin depth), R_s further turns up sharply. Therefore, the second term in Equation (2.32) can be roughly looked as increasing versus frequency or at least a constant. On the other hand, besides L_s increasing, there are stronger and stronger capacitive parasite effects when the frequency goes up. In this capacity, they are C_s and C_p. The increasing L_s, C_s, and C_p at the denominator of the first term in Equation (2.32) makes the first term go down. Totally, the *SRF* goes down when h_1 increases. Note that the *SRF* for some cases shown in Figure 5.10 are well in excess of 20 GHz and difficult to obtain due to the resolution

of the FEM mesh required and finite computer resources. However, from the treads in the curves, these look to be approaching 30 GHz. As for the optimization startup value of h_1, h_1=80 μm is chosen considering the tradeoff between the high working frequency (depends on *SRF*) and high *Q* factor value and the robustness of the suspending structure (large h_1 results in structure fragility).

In addition, the influences from the variable *ix*, y_g (y_{gvari}), and r_1, $angle_1$, etc. to the RF performances are also be investigated by simulations. The simulations results are shown in the Appendix. The analyses are pretty much the similar to the varying h_1 case.



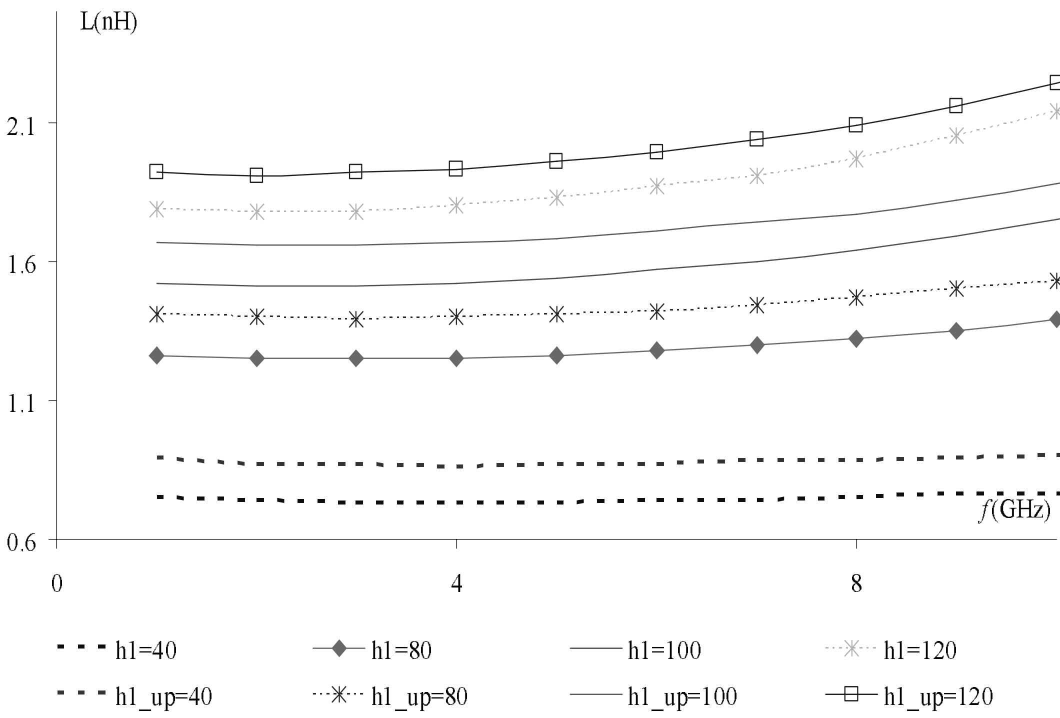
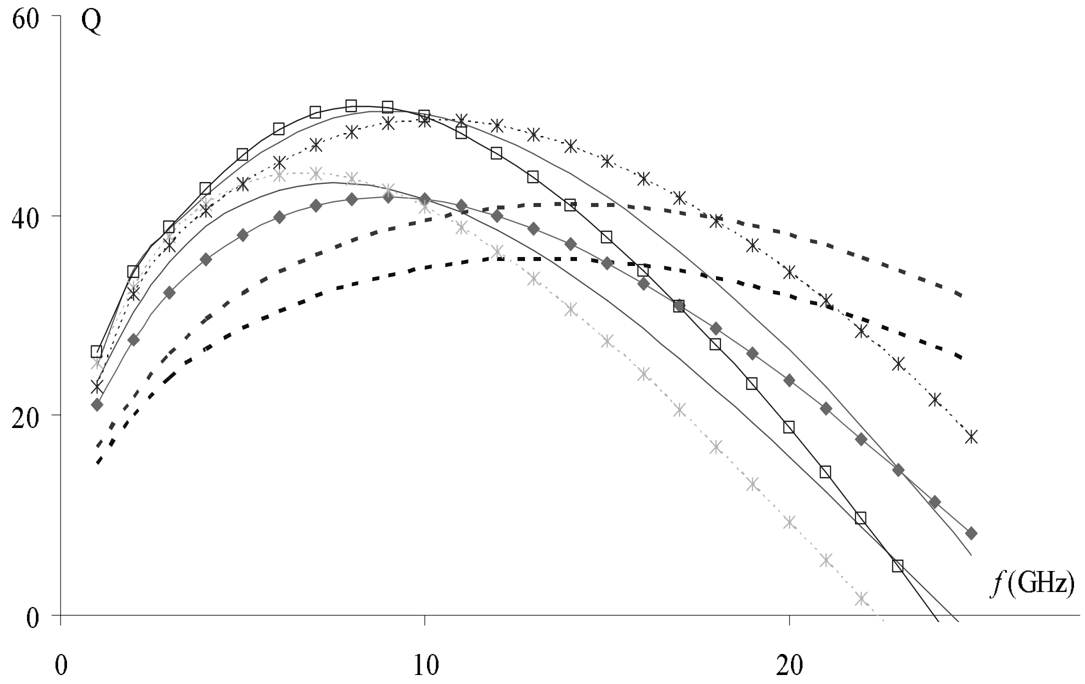


Figure 5.9: Comparison of the inductance simulation results for h_1 (in the unit of μm) variation of solenoid inductors



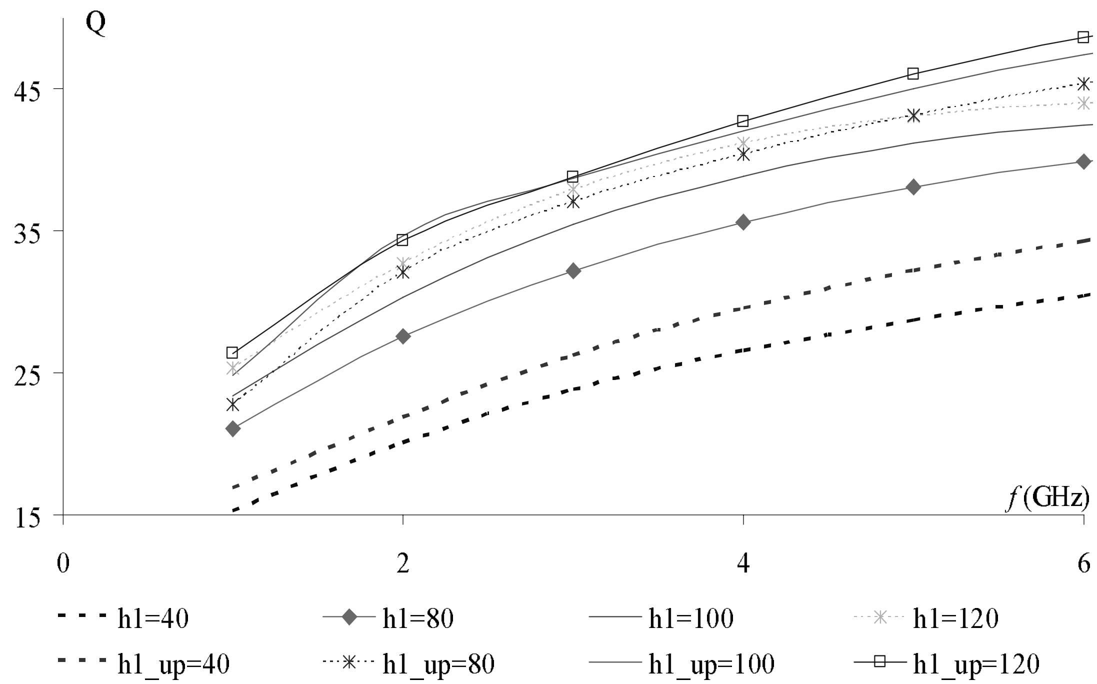


Figure 5.10: Comparison of the Q factor simulation results for h_1 (in the unit of μm) variation of solenoid inductors

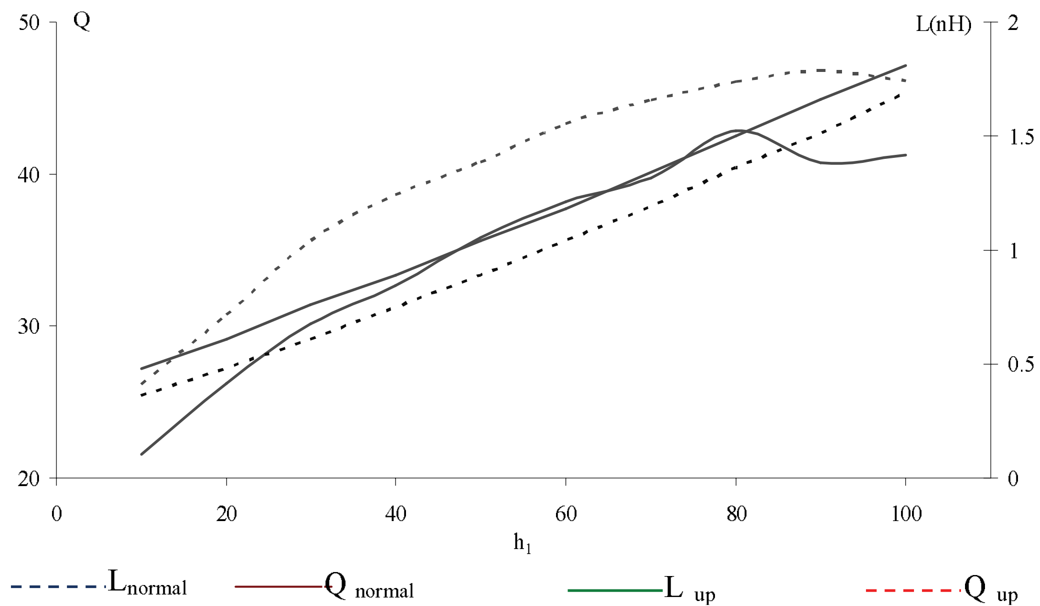


Figure 5.11: h_1 parameter sweep at 9 GHz

5.3 Summary of The Inductor Simulations

The previous simulations not only obtained some useful data for the subsequent optimizations, but also verified the theoretical discussions in Chapter 2 and further investigated and determined the characteristics of the LIGA structural inductors.

Loss mechanism is a key constraint issue for the inductor performance. Normally, two loss mechanisms need to be considered. One is the inductor metal resistive loss. It plays an important role in determining the *Q* factor and inductance at the low frequency region below the peak *Q* point. Low-resistivity metal is preferred accordingly. As well, simulations results show thicker metal trace can reduce the metal ohmic loss at low frequencies. However, due to the current crowding effects, when the metal trace thickness surpasses a certain few skin depths, the *Q* factor starts to saturate and there is little increment in *Q* if the thickness is further enlarged. In this thesis, copper and nickel are employed as the designing metal materials, respectively. The other key loss mechanism is the substrate parasite effect loss. This loss is caused by the electromagnetic coupling from the inductor coil to the Si substrate. It dominates the inductor property at high frequencies between the *Q* peak and the *SRF*. This substrate

coupling loss can be significantly reduced by suspending the inductor metal structure from the substrate. In this dissertation, a suspending height of 150μm was chosen because of the high aspect ratio advantage of LIGA process. To be consistent with post-CMOS 0.18μm fabrication, the variable t_{SiO2} is fixed at 8.7μm (see Section 3.4). Meanwhile the resistivities of the Si substrate are set up at 10 ohm·cm (for both the BiCMOS case and mix-mode CMOS case).

5.4 Optimization

Through the parameter sweeps and simulations, the suitable startup values are obtained for the characteristic optimizations. HFSS Optimetrics™ is used for the optimizations. HFSS Optimetrics™ is not a global operation covering the whole parameter optimization range which the user defines. Instead, it is local because during the optimization, if there is a local peak by chance caused by a parameter close to the startup value, the optimization will not run to the real maximum in the variation range, but stops at the local peak regardless if the targeted error requirement has been realized. With so many parameters influencing the inductor characteristics this is highly likely. To overcome this drawback, it is better to associate the parameter sweep with the parameter optimizations to try and limit the variations to small enough ranges that convergence to a solution can obtained.

Under the Ansoft HFSS environment, a combined manual adjustment and software optimization approach for optimizing the parameters was developed. From the previous parameter sweeps and simulations, the parameter variation ranges during the optimizations have been reasonably narrow down. Based on the optimization startup values obtained in Section 5.1, 5.2, and the Appendix, the corresponding parameter variation ranges were set up close to the startup values and varied mainly in the directions that improve Q. For example, in this research, for spiral inductor on the CMOS substrate, the variation ranges of variables t_1, ix, w_1, and s were set within (9 μm, 30 μm), (45 μm, 100 μm), (5 μm, 25 μm), and (7 μm, 25 μm), respectively. Then a series parameter arrays were randomly picked up from the above variation ranges, for instance, (t_1, ix, w_1, s) can be set as (20 μm, 55 μm, 10 μm, 12 μm). The corresponding

simulation was then performed. From Equation (2.29) to Equation (2.32), varying geometric parameters brings variation in L. And L variation influences the Q and SRF. Practically, the desired L value must be chosen before the optimizations. To simulate the practical situations and remove the L influences to the Q and SRF, L values also need to be fixed during the optimizations. Based on pre-optimization simulation results, for the spiral inductor on CMOS/BiCMOS substrate, the fixed L value is empirically set to be 5.92 nH. However, L and Q peaks are output of the HFSS simulations and cannot be accurately anticipated before simulations. It is really hard and practically unnecessary to fix the L at an exact fixed value when varying the parameter values. Thus, in this optimization capacity, instead of fixing L exactly at a fixed value, for example, 5.92 nH, the L values are strictly limited within a narrow domain 5.92±5% nH. Any simulated result whose L beyond this domain was abandoned. After setting up the narrow L variation range, quite a few simulations, say 30, were performed by manually adjusting the geometric parameters. Their Q factor results were compared. Normally, close to the parameter array which generates a larger Q value, a regional peak Q exists. Thus, a corresponding parameter sweep and optimization is carried out close to the above parameter array. Specifically, each parameter only varies at a few values close to value which was achieved in the randomly manually sampling. As a result, the total simultaneous parameter sweep and optimization times are at the most a few hundreds, which is acceptable under HFSS environment. This kind of small range simultaneous sweeps and optimizations are performed regarding every bigger Q factor obtained in previous manual sampling. Their optimization results are compared together and the parameter array which makes the largest Q is regarded as the final optimized parameter array.

This approach does have some drawbacks, for example, the chance for the random manual sampling to find a good parameter array which generates a higher enough Q is really a random probability. Moreover, the frequency point of the Q peak can not be anticipated and controlled accurately. However, under HFSS environment, to the author's competence, this is the most applicable approach currently. As for the final results, for the suspended spiral inductor, the Q peak is 48.33 for a L of 5.92 nH. As

mentioned previously, normally, the conventional spiral inductors built on standard CMOS/BiCMOS substrate can only realize the Q factor at 10 or so. Thus, the optimization results are much better. However, the Q peak occurs at 4.5 GHz, which results in an impedance of 167 ohm. It is not in the well-acknowledged ideal impedance range, roughly from 50 ohm to 75 ohm. From this perspective, this is a drawback. However, in some capacities, the most important pursuits are not impedance, but high Q at high frequencies. In this sense, this optimization and simulation result does have some unique advantages. The similar approaches also apply to solenoid on CMOS/BiCMOS substrate situations. The final result is Q = 76.21 at 9.5 GHz while L is 1.05 nH. This result is much better than the spiral counterpart, and its impedance, 62.7 ohm, is also inside the well-acknowledged ideal impedance range. The optimization results are illustrated in Figure 5.12 and Figure 5.13. The peak Q point values and its frequency as well as the corresponding L values at this point were marked. Note that for most solenoid inductors, we set up the $angle_1$=0. This will make the possible future fabrications much easier. Table 5.5 lists the dimensions of the optimized inductors.

Table 5.4: List and Comparison of inductor key parameters

Inductor	Operational frequency (GHz)	Nominal Inductance (nH)	Q factor
Spiral in this thesis	4.5	5.92	48.33
Conventional spiral	1~2	varied	≈ 10
Solenoid in this thesis	9.5	1.05	76.21
Solenoid with 20 µm suspension [30]	approx. 8	approx. 1.8	approx.60

Table 5.5: Dimensions of the optimized inductors (in unit of µm)

Inductor type	Dimensions (µm)					
Spiral	ix	w_1	t_1	s	n	h_1
	44	11	25	36	3.5	150
Solenoid	ix	$ygvari$	t_2	r_1	n	h_1
	35	40	25	10	4	150

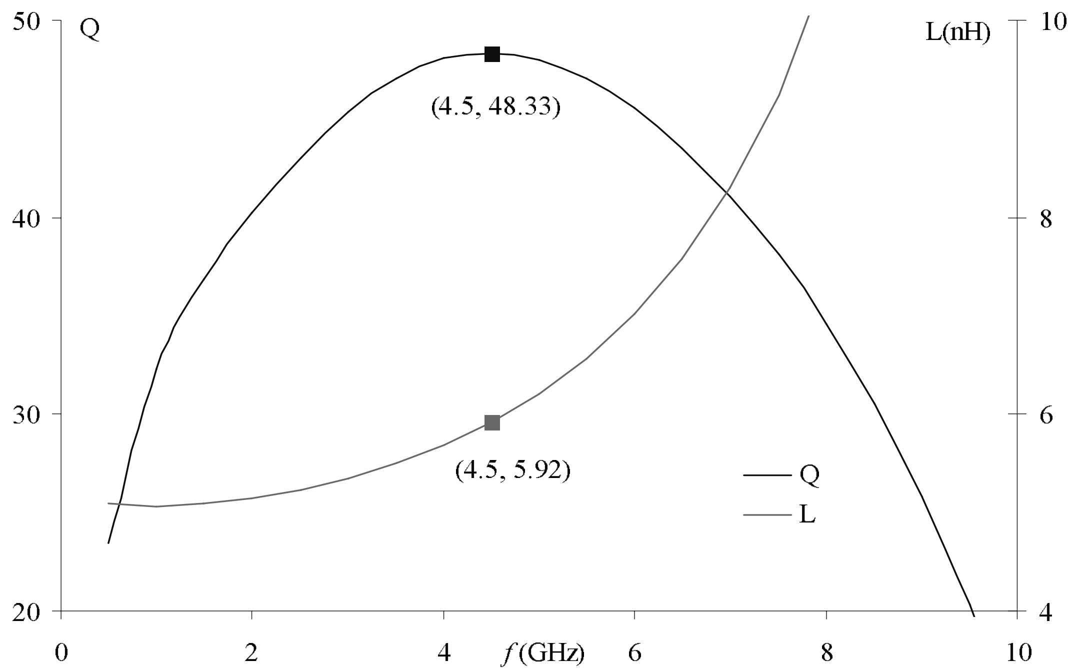


Figure 5.12: Optimization results of designed spiral suspended inductors on simulated CMOS/BiCMOS substrate

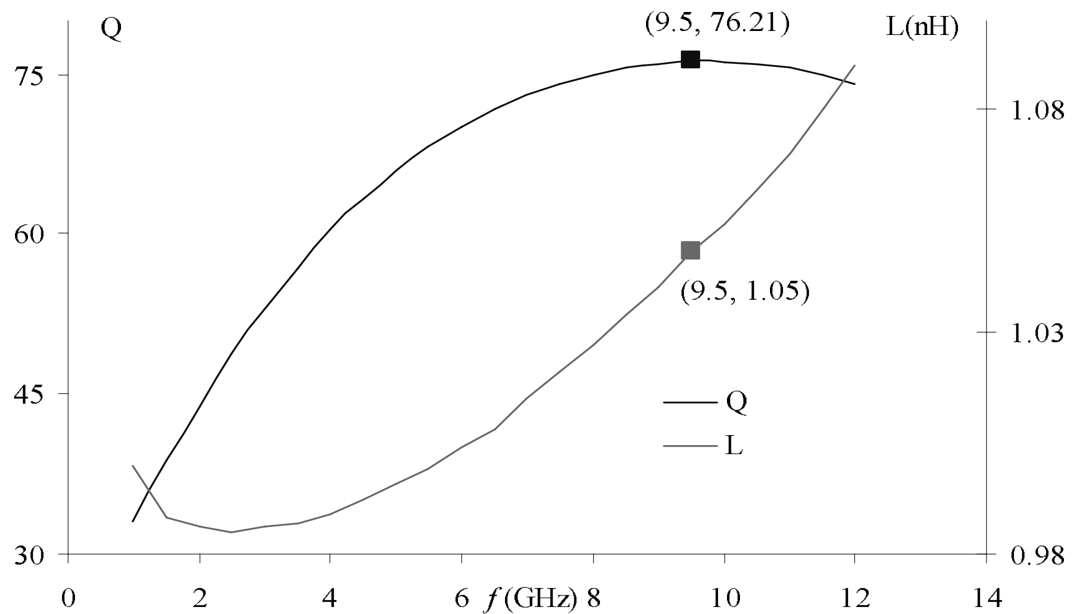


Figure 5.13: Optimization results of designed solenoid inductors on simulated CMOS/BiCMOS substrate

6 Conclusions

6.1 Summary

The main goal of this thesis is to explore the characteristics of the LIGA structural inductors on Si substrate, particularly those on the Si CMOS/BiCMOS substrate. The other theme briefly discussed was the possible post-CMOS LIGA processing. This approach has the advantage of integrating the high aspect ratio structure with the leading microelectronics technique, CMOS.

A brief introduction of relevant air core inductor theory was presented. This included basic air core inductor theory, micro-scale inductor lumped equivalent model introductions, and loss mechanisms for the micro-scale inductors. As well, a brief introduction of LIGA micromachining process and its recent progress in possible CMOS compatible post processing was presented.

Two types of inductors, namely, spiral inductors and solenoid inductors, were designed on the simulated TSMC 0.18 μm CMOS and BiCMOS substrate, respectively using Ansoft HFSS [20]. For each type of inductors, a substrate touching subtype of structure and a 150 μm height air suspended subtype of structure were built for comparison. Recent advance in the CMOS compatible LIGA processing and corresponding research were also briefly introduced.

Using HFSS [20], a series of simulations based on the geometric and physical parameter variations were performed for each type (subtype) of inductor. The simulation results were put together for characteristics analysis and comparison. The advantage of LIGA process in inductor fabrications and the possible advantage of integrating LIGA with

CMOS process were explored by analyzing the simulation results. Finally, the suspended inductors were optimized for the future fabrication purpose.

6.2 Conclusions

The following main conclusions were drawn from analysis of the simulation and optimization results.

1. The LIGA technique has the unique advantage to build high profile inductors due to its high aspect ratio and high side wall realization. Increased metal thickness improves inductor *Q* up to a point, but is constrained by the skin effect at high frequencies, so there appears to be advantage only up to frequencies of about 6 GHz. Another advantage of LIGA is in 3-D vertical and suspended structures. The HFSS simulation results reveal that the RF characteristics of suspended inductors are universally better than the substrate touching counterparts. For conductive or semi-conductive substrate, for example, Si substrate, suspended structures can largely decrease the electromagnetic coupling between the inductor coil and the substrate. LIGA also has the advantage to potentially build 3-D non-planar structures, for example, solenoid inductors. These can be used to change the dominating magnetic flux direction and further reduce the coupling between the inductor and the substrate. Because electromagnetic coupling is largely suppressed by structure suspension and magnetic flux orientation change, the energy drainage from the inductor to the substrate is largely suppressed and thus the inductor *Q* factor, the frequency at the maximum *Q* factor value, and the *SRF* are greatly improved. It is easy to see this improvement from the comparison between Figure 5.12 and Figure 5.13.

2. Recent advance in the exploration of CMOS compatible LIGA processing makes the integration between CMOS and LIGA possible. The reported CMOS and BiCMOS substrate resistivities are fairly conductive, on the order of 10 ohm·cm. However, under this circumstance, the LIGA structural solenoid copper

inductors in this research can still achieve the Q factor of 76.21 and L (inductance) of 1.05 nH at 9.5 GHz (simulated CMOS/BiCMOS substrate, suspended structure). The LIGA structural spiral copper inductor can also obtain the Q factor of 48.33 and L of 5.92 nH at 4.5 GHz (simulated CMOS/BiCMOS substrate, suspended structure). From the listed simulation results above, one can see LIGA structural inductors still have very good performance even on conductive substrate. In addition, a highly suspended inductor reduces the substrate noise, which is mainly generated by active devices on the substrate, to be coupled into the inductor. On the other hand, the highly suspended structures reduce the influence to the surrounding circuitry from the internally induced electromagnetic field. Because of these advantages, LIGA structural inductors have promising commercial future if they can be integrated with one of the leading microelectronics technique, CMOS.

6.3 Future research directives

Some suggested research directions to further explore the RF characteristics and the significance of the approaches presented here might include:

1. The electromagnetic mechanisms of influence from the variation of some geometric or physical inductor parameters to the inductor RF characteristics need further investigation.

2. For prototype testing convenience, this research includes the ground ring and other auxiliary structures into the inductor models. It is worthy to further explore the inductor characteristics after de-embedding these kinds of surrounding structures.

3. Different optimization approaches could be explored to possibly obtain simpler methods for maximizing a better geometry and for a better simulation results.

4. The software designed, simulated, and optimized inductors need to be put through fabrications and subsequent testing for verifications.

5. Normally, in the micro-scale domain, the influence from the gravity to the structure robustness is negligible. Instead, the internal stress of the metal structure becomes the dominating mechanical force affecting the structure robustness. However, strictly speaking, considering the external shocks and temperature changes, it is better to do the mechanical robustness analysis for the designed inductors. Furthermore, due to lack of mechanical analysis, the aspect ratio of the suspended pillars is conservatively set to around 10:1. It is reasonable to anticipate that with the assistance of mechanical analysis, the aspect ratio can be further enlarged. Accordingly, the electromagnetic coupling can be further reduced and the Q factor and SRF can be further improved.

6. The LIGA structural inductor performance/characteristics investigated in this thesis are the limited to the stand-alone (unloaded) situation. To fully investigate the overall performance, the designed inductors need to be integrated into a circuit, for example, a VCO, to further investigate the characteristics in the integrated situations. Thus, if possible, the inductor needs to be fabricated with a circuit chip using the suitable CMOS compatible LIGA process to form a VCO and then to be put into testing for verifications.

Reference:

[1] G. P. Podrigue, "A Generation of Microwave Ferrite Devices," Proc. IEEE, vol. 76, pp. 121–137, Feb. 1988.

[2] M. Munakata, M. Yagi, M. Motoyama, Y. Shimada, M. Baba, M.Yamaguchi, and K. Arai, "Thickness Effect on 1 GHz Permeability of (CoFeB)-(SiO_2) Films with High Electrical Resistivity," IEEE Trans. Magnetics, vol. 37, pp. 2258–2260, 2001.

[3] Y. Zhuang, M. Vroubel, B. Rejaei, and J. N. Burghartz, "Ferromagnetic RF Inductors and Transformers in Standard CMOS/BiCMOS," IEDM Tech. Digest, pp. 475–478, 2002.

[4] E.W. Becker, W. Ehrfeld, P. Hagmann, A. Maner, and D. Münchmeyer, "Fabrication of Microstructures with High Aspect Ratios and GreatStructural Heights by Synchrotron Radiation Lithography, Galvanoforming, and Plastic Moulding (LIGA process)," Microelectronic Engineering, vol. 4, pp. 35-56, 1986.

[5] Daniel S. Park, K. S. Kim, B. Pillans, and J.-B. Lee, "PDMS-based Pattern Transfer Process for the Post-IC Integration of MEMS Onto CMOS Chips," Journal of Micromechanics and Microengineering, vol. 14, no. 3, pp. 335–340, 2004.

[6] Ali M. Niknejad, "Analysis, Simulation, and Applications of Passive Devices on Conductive Substrates," Ph.D. thesis, Electrical Engineering and Computer Science, University of California at Berkely, Spring 2000.

[7] David A. Johns and Ken Martin, Analog Integrated Circuit Design, Wiley, 1997.

[8] Paul R. Gray and Robert G. Meyer, Analysis and design of Analog Integrated Circuits, 3rd edition, Wiley, 1993.

[9] Gabriel M. Rebeiz, RF MEMS: Theory, Design, and Technology, John Wiley & Sons, 2003.

[10] M. J. Madou, Fundamentals of Microfabrication: The Science of Miniaturiza- tion, CRC Press, 2002.

[11] Mohamed Gad-el-Hak, The MEMS Handbook, CRC Press, 2002.

[12] Z. Ma, D.M. Klymyshyn, S. Achenbach, and J. Mohr, "LIGA Cavity Resonator for K-band Applications," pp. 106-109, International Conference on MEMS, NANO, and Smart Systems (ICMENS-05), Banff, Canada, 2005.

[13] D. T. Haluzan and D. M. Klymyshyn, "High-Q LIGA-MEMS Vertical Cantilever Variable Capacitors for Upper Microwave Frequencies," Microwave and Optical Technology Letters, vol. 42, no. 6, pp. 507-512, September 2004.

[14] A. A. Kachayev, D. M. Klymyshyn, "High Vertical Aspect Ratio LIGA Micro-wave 3-dB Coupler," International Conference on MEMS, NANO, and Smart Systems (ICMENS-03), pp. 38-43, 2003.

[15] W. Menz, W. Bacher, W. Bier, O. F. Hagena, J. Mohr, and D. Seidel, "Combination of LIGA with Other Microstructure Technologies," Microsystem Technology, vol. 2, pp. 162–166, 1996.

[16] Anton Kachayev, "LIGA-Micromachined Tight Microwave Couplers," M. Sc. thesis, Department of Electrical Engineering, University of Saskatchewan, 2004.

[17] S. W. Park, K. S. Kim, and J.-B. Lee, "A Novel CMOS-compatible Polymeric Pattern Transfer Technique for Integrated MEMS," Proceedings of the ICMAT 2001

Symposium J: Packaging Materials and Processes for Microelectronics, Optoelectronics, MEMS and Displays, Singapore, Jul. 2001.

[18] D. M. Pozar, Microwave Engineering, 2nd edition, Wiley, New York, NY, 1997.

[19] H. G. Booker, Energy in Electromagnetism, Peter Peregrinus (on behalf of the IEE), London/New York, 1982.

[20] internet resource: http://www.ansoft.com/products/hf/hfss/

[21] C. P. Yue, S. S. Wong, "Physical Modeling of Spiral Inductors on Silicon," Electron Devices, IEEE Transactions on, vol. 47, issue 3, pp. 560–568, March 2000.

[22] H. M. Greenhouse, "Design of Planar Rectangular Microelectronic Inductors," IEEE Transactions on Parts, Hybrids, and Packaging, vol. PHP-10, no.2, June 1974.

[23] R. H. Jansen, et al., "Theoretical and Experimental Broadband Characterization of Multiturn Square Spiral Inductors in Sandwich Type GaAs MMIC," Proc. 15th Eur. Microwave Conf., pp. 946–951, 1985.

[24] L.Wiemer and R. H. Jansen, "Determination of Coupling Capacitance of Under-passes, Air bridges and Crossings in MICs and MMICs," Electron. Lett., vol. 23, pp. 344–346, Mar. 1987.

[25] W. B. Kuhn and N. M. Ibrahim, "Analysis of Current Crowding Effects in Multiturn Spiral Inductors," IEEE Transactions on Microwave Theory and Techniques, vol. 49, no. 1, January 2001.

[26] C. P. Yue, S. S. Wong. "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," IEEE Journal of Solid-State Circuits, vol. 33, no. 5, May 1998.

[27] T. S. Horng, K.C. Peng, et al, "S-Parameter Formulation of Quality Factor for a Spiral Inductor in Generalized Two-Port Configuration," IEEE Transactions on Microwave Theory and Techniques, vol. 51, no. 11, November 2003.

[28] Kenneth O, "Estimation Methods for Quality Factors of Inductors Fabricated in Silicon Integrated Circuit Process Technologies," IEEE Journal of Solid-State Circuits, vol.33, no.8, August 1998.

[29] J. N. Burghartz and B. Rejaei, "On the Design of RF Spiral Inductors on Silicon," IEEE Transactions on Electron Devices, vol. 50, no. 3, March 2003.

[30] Yong-Jun Kim and M. G. Allen, "Surface Micromachined Solenoid Inductors for High Frequency Applications," Components, Packaging, and Manufacturing Technology, Part C, IEEE Transactions on [see also Components, Hybrids, and Manufacturing Technology, IEEE Transactions on], vol. 21 , issue 1, pp. 26 – 33, Jan. 1998.

[31] Jun-Bo Yoon, Byeong-Il Kim, Yun-Seok Choi, and Euisik Yoon, "3-D Construction of Monolithic Passive Components for RF and Microwave ICs Using Thick-metal Surface Micromachining Technology," Microwave Theory and Techniques, IEEE Transactions on , vol. 51 , issue 1 , pp. 279–288, Jan. 2003.

[32] J. Craninckx and M. S. J. Steyaert. "A 1.8-GHz Low-phase-noise CMOS VCO Using Optimized Hollow Spiral Inductors," IEEE J. Solid-State Circuits, vol. 32, pp. 736–744, May 1997.

[33] D. J. Young, V. Malba, Jia-Jiunn Ou, A. F. Bernhardt, and B. E. Boser, "A Low-noise RF Voltage-controlled Oscillator Using On-chip High-Q Three-dimensional Coil Inductor and Micromachined Variable Capacitor," International Electron Devices Meeting, pp. 128–131, 1997.

[34] F. W. Grover, Inductance Calculations, Van Nostrand, Princeton, N.J., 1946.

[35] A.E. Ruehli. “Equivalent Circuit Models for Three-dimensional Multi-conductor Systems,” IEEE Transactions on Microwave Theory and Techniques, MTT-22, pp. 216–221, March 1974.

[36] J. Y. –C. Chang, A. A. Abidi, and M. Gaitan, “Large Suspended Inductors and Their Use in a 2μm CMOS RF Amplifier,” IEEE Electron Device Lett., vol. 14, pp. 246-248, May 1993.

[37] C.-Y. Chi and G. M. Rebeiz, “Planar Microwave and Millimeter-wave Lumped Elements and Coupled-line Filters Using Micro-machining Techniques,” IEEE Trans. Microwave Theory Tech., vol.43, no.4, pp.730-738, April 1995.

[38] H. Jiang, Y. Wang, J.-L. A. Yeh, and N. C. Tien, “On-chip Spiral Inductors Suspended Over Deep Copper-lined Cavities,” IEEE Trans. Microwave Theory Tech., vol. 48, no. 12, pp. 2415-2423, December 2000.

[39] V. M. Lubecke, B. Barber, E. Chan, D. Lopez, M. E. Gross, and P. Gammel, “Self-Assembling MEMS Variable and Fixed RF Inductors,” IEEE Trans. Microwave Theory Tech., vol. 49, no. 11, pp. 2093-2098, Nov. 2001.

[40] H. Lakdawala, X. Zhu, H. Luo, S. Santhanam, L. R. Carley, G. K. Fedder, “Micromachined High-Q Inductors in a 0.18-μm Copper Interconnect Low-K Dielectric CMOS Process,” IEEE Journal of Solid-State Circuits, ,vol. 37 , issue 3 , pp. 394–403, March 2002.

[41] Eun-Chul Park, Yun-Seok Choi, Jun-Bo Yoon, Songcheol Hong, and Euisik Yoon, “Fully Integrated Low Phase-Noise VCOs With On-Chip MEMS Inductors,” IEEE Transactions on Microwave Theory and Techniques, vol. 51, no.1, January 2003.

[42] T. Itoh, Numerical Techniques for Microwave and Millimeter-Wave Passive Structures, John Wiley & Sons, 1989.

[43] K. J. Binns and P. J. Lawrenson, Analysis and Computation of Electric and Magnetic Field Problems, Pergamon Press, Oxford, 1973.

[44] internet resource: Port Tutorial Series: Coplanar Waveguide (CPW), www. ansoft.com.

[45] internet resource: Advanced Training "Boundary and Excitation Training," http://www.ansoft.com/workshops/hfworkshop03/Steve_Rouselle.pdf

[46] TSMC 0.18 μm CMOS/BiCMOS chip designing manuals, TSMC Document No.: TA-10A5-6001 (T-018-LO-SP-001)

[47] J. R. Long and M. A. Copland, "The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's," IEEE Journal of Solid-State Circuits, vol. 32, no. 3, pp. 357-369, March 1997.

APPENDIX

A. Some Simulations Results for Spiral Inductor

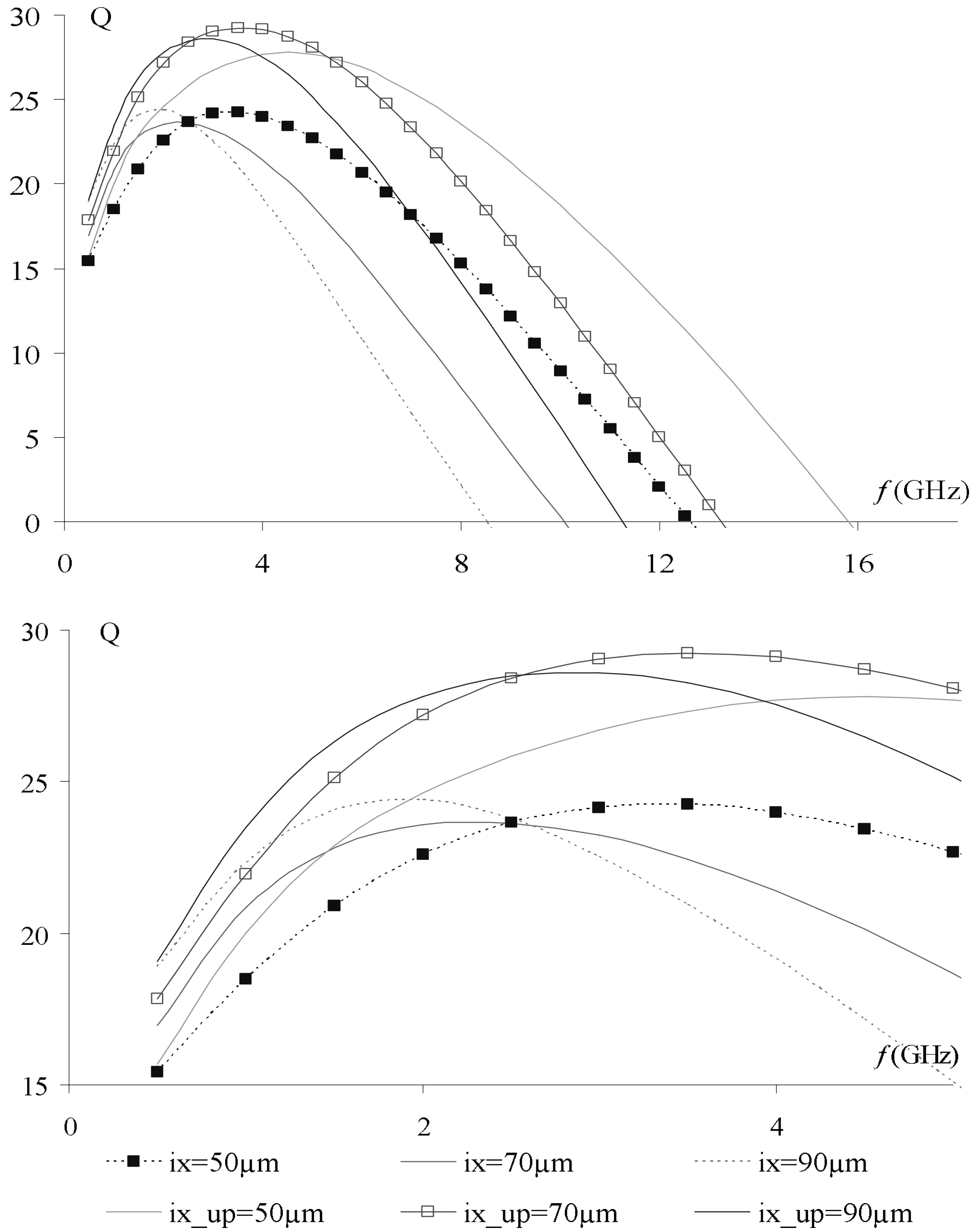
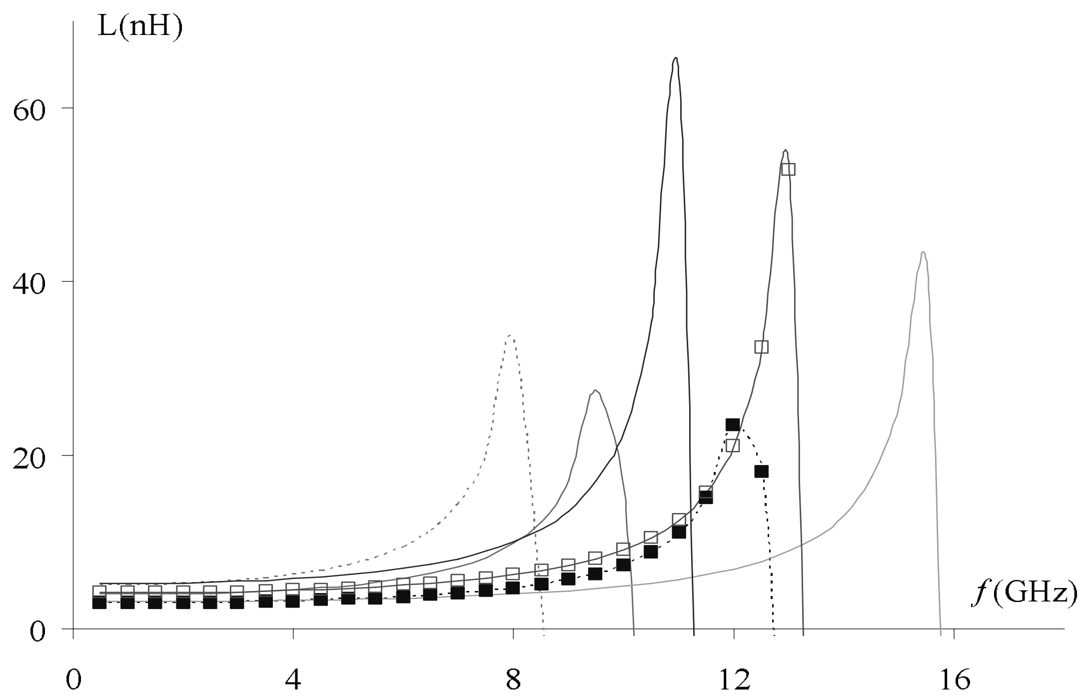


Figure A. 1: Comparison of *Q* factor simulation results for *ix* variations.



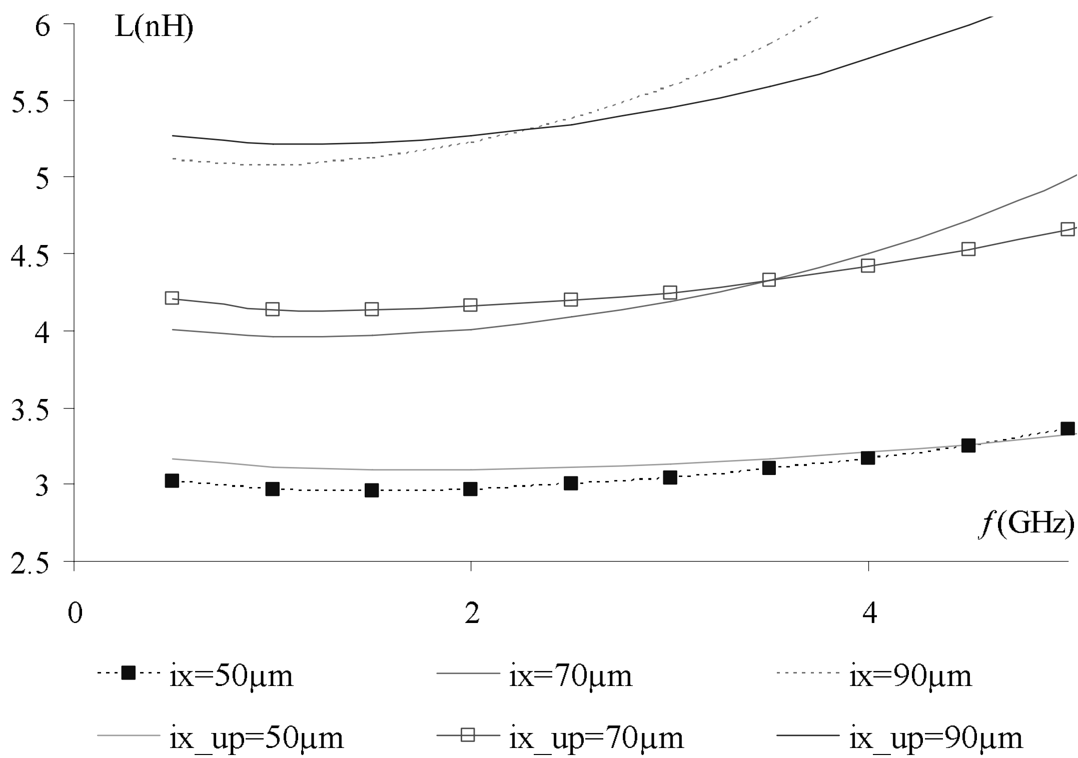


Figure A. 2: Comparison of inductance simulation results for *ix* variations.

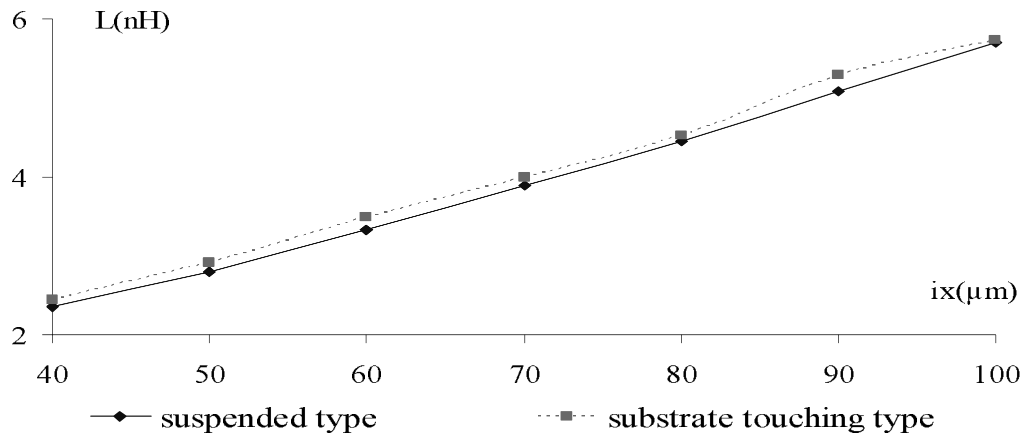
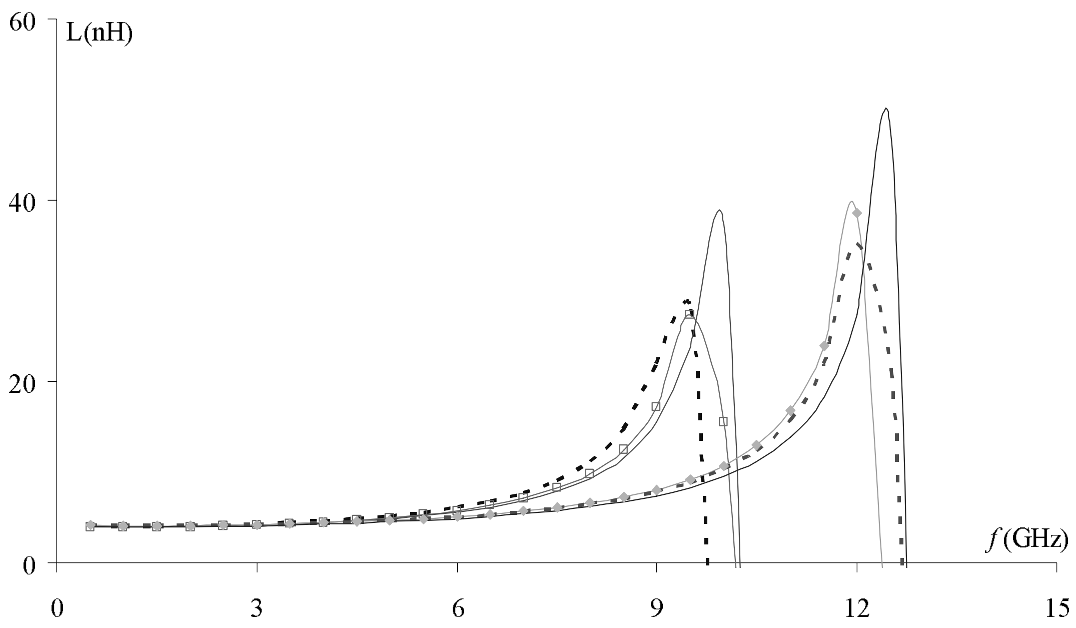
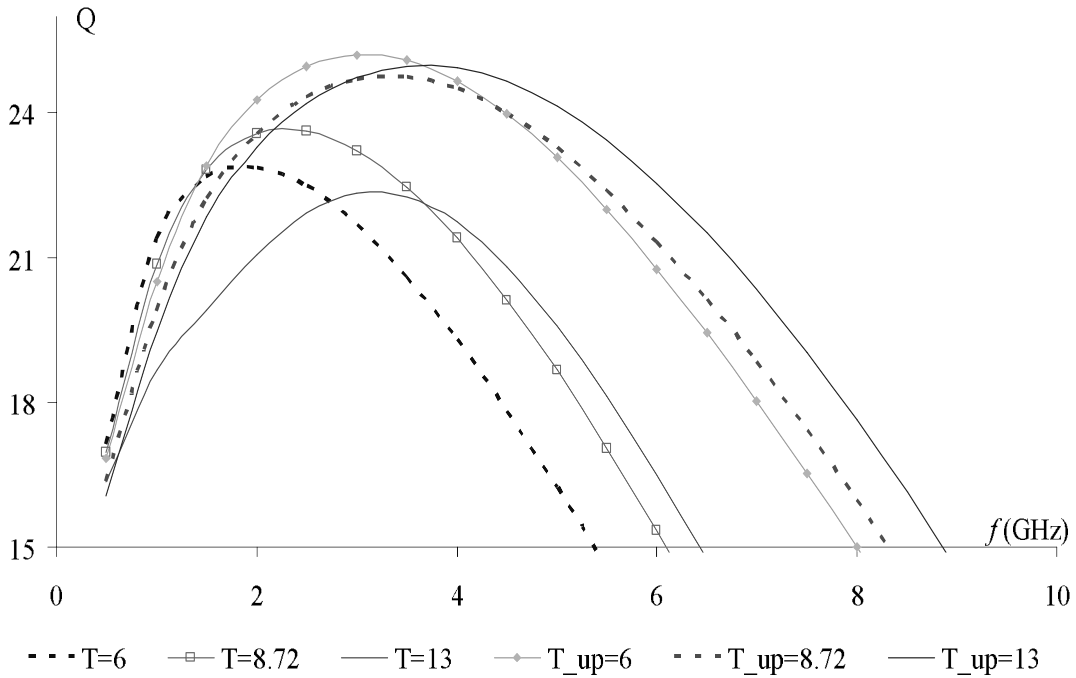


Figure A. 3: Parameter sweep of *ix* at 2 GHz.



(a)



(b)

Figure A. 4: Comparison of simulation results for T= t_{SiO2} (in the unit of μm) variations. (a) Comparisons of inductance; (b) Comparisons of Q factor

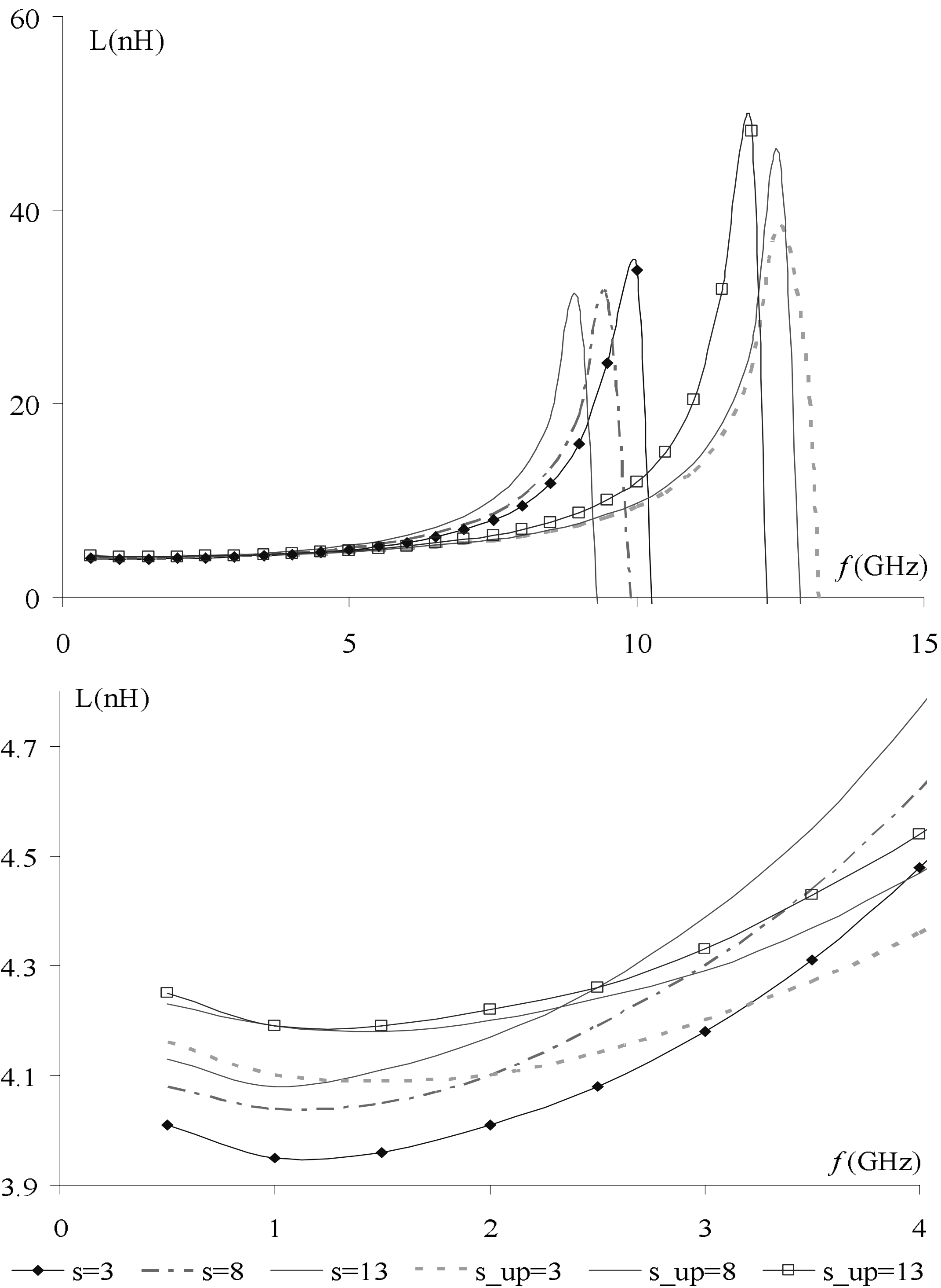


Figure A. 5: Comparison of inductance simulation results for *s* (in the unit of μm) variations.

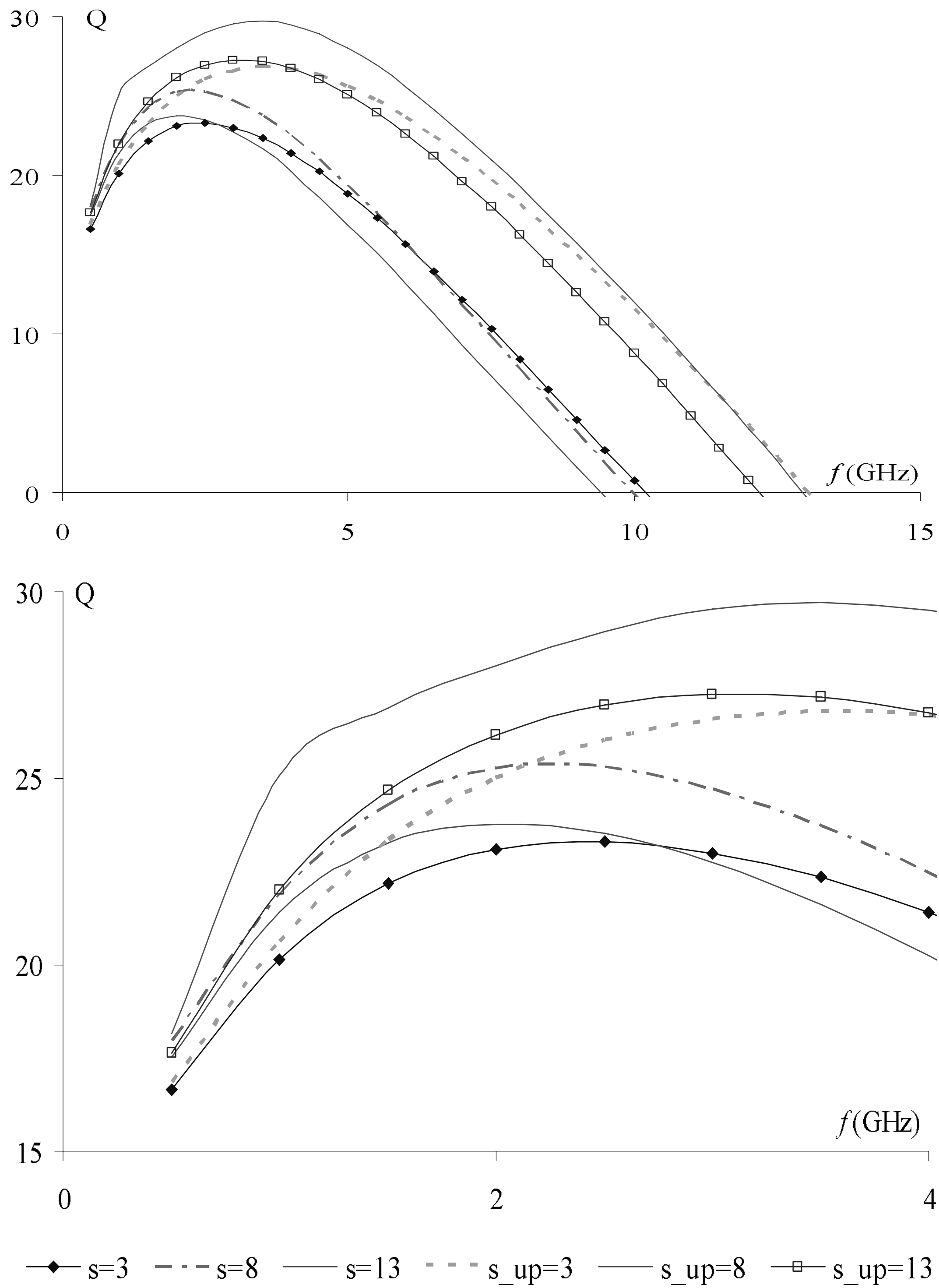


Figure A. 6: Comparison of Q factor simulation results for s (in the unit of μm) variations.

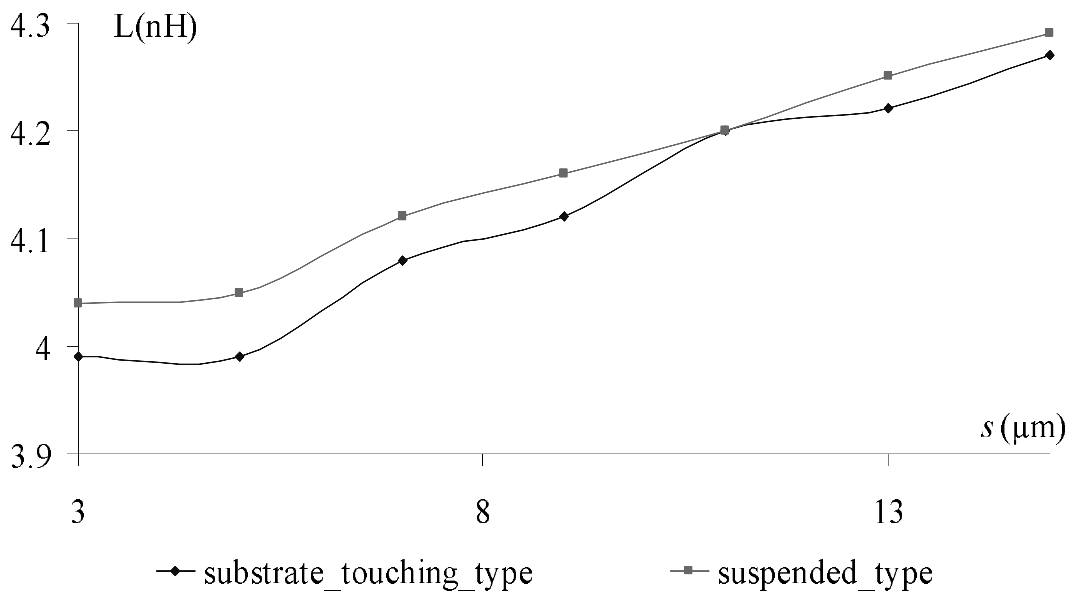


Figure A. 7: S parameter sweep at 2.5 GHz

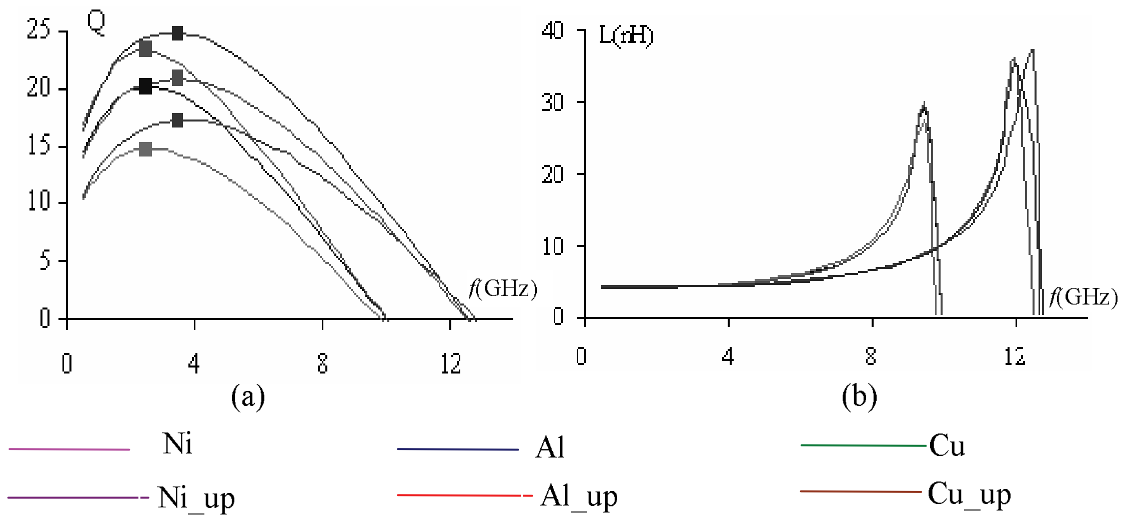


Figure A. 8: Comparison of the simulation results for spiral inductors made of different metals. (a) Q comparison (b) Inductance comparison

B. Some Simulations Results for Solenoid Inductor

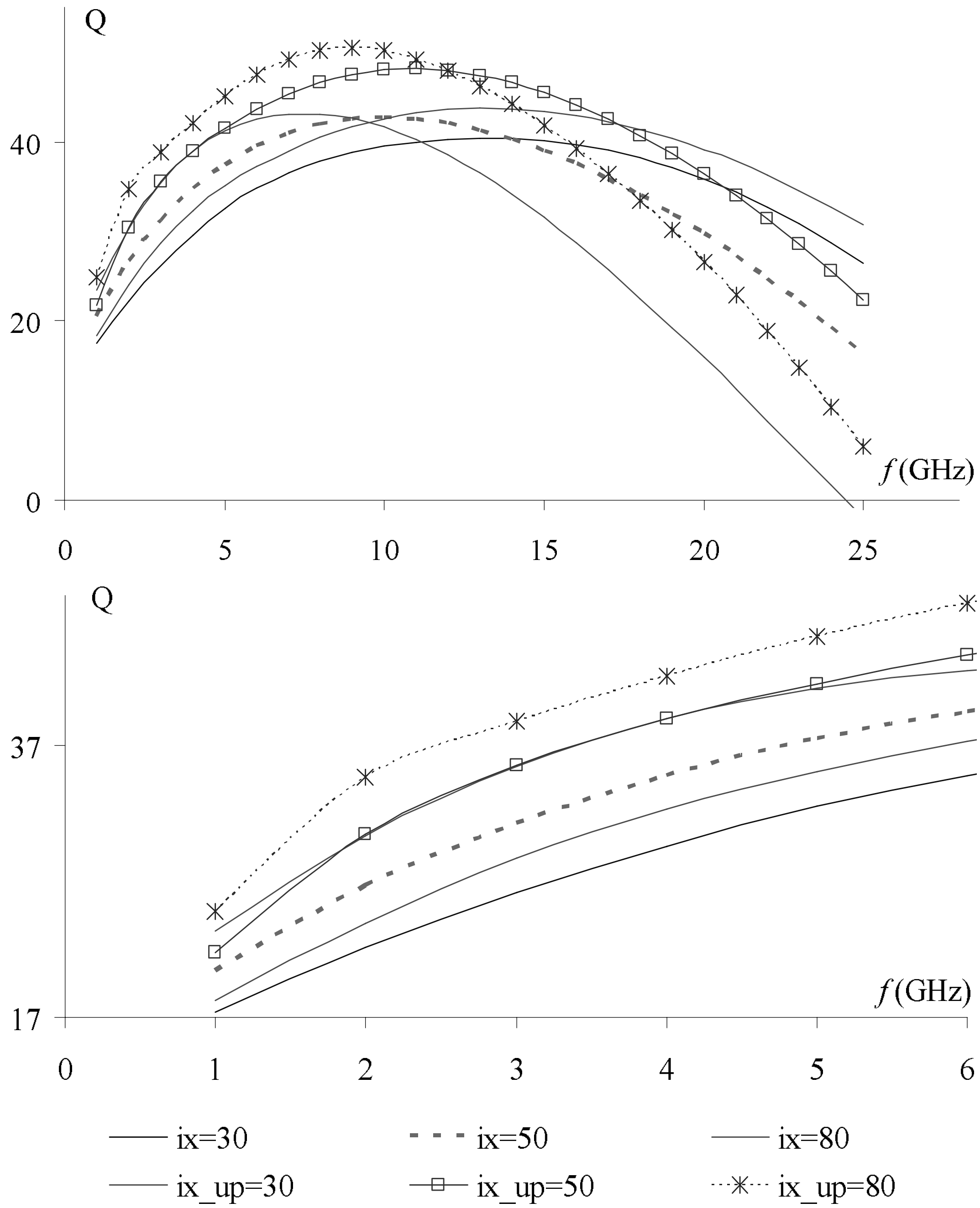
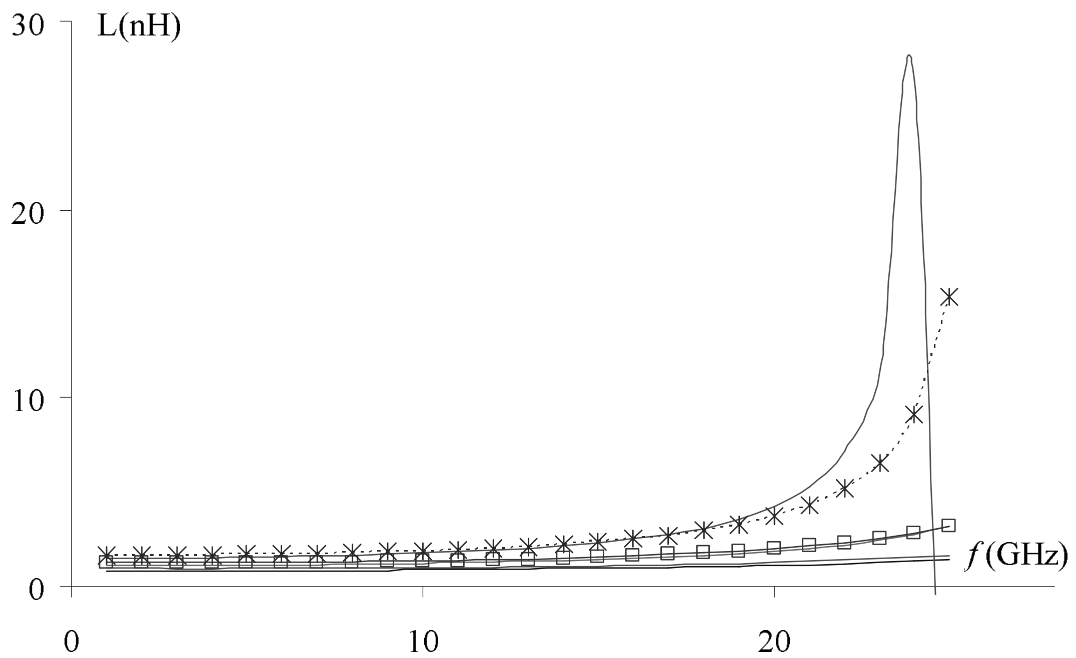


Figure B. 1: Comparison of Q factor simulation results for ix (in the unit of μm) variations of the solenoid inductors.



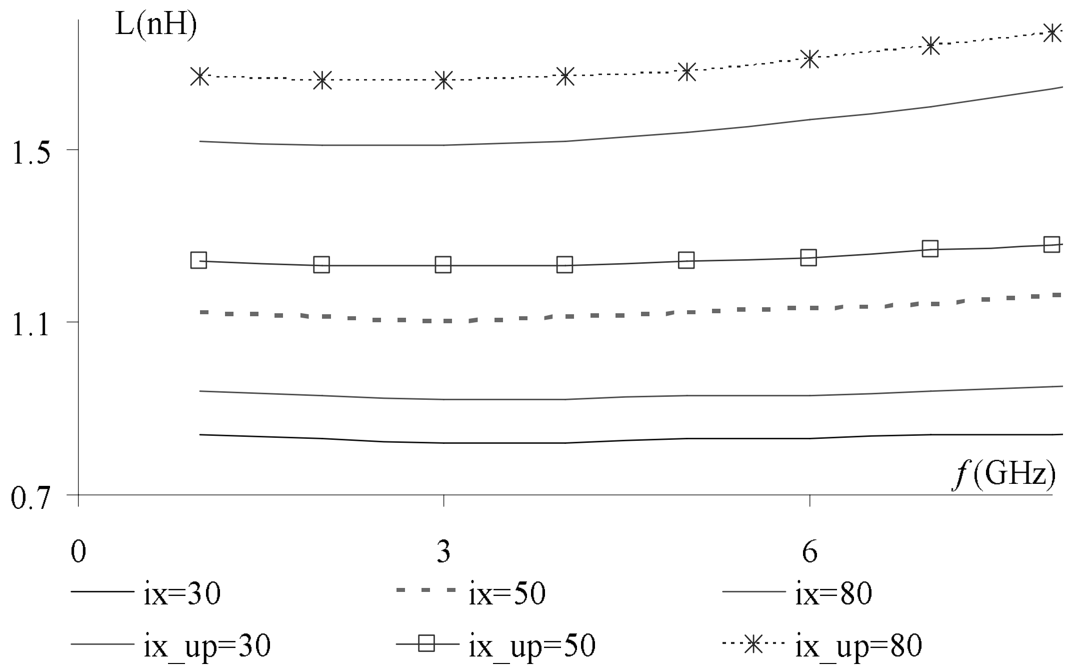


Figure B. 2: Comparison of inductance simulation results for *ix* (in the unit of µm) variations of the solenoid inductors.

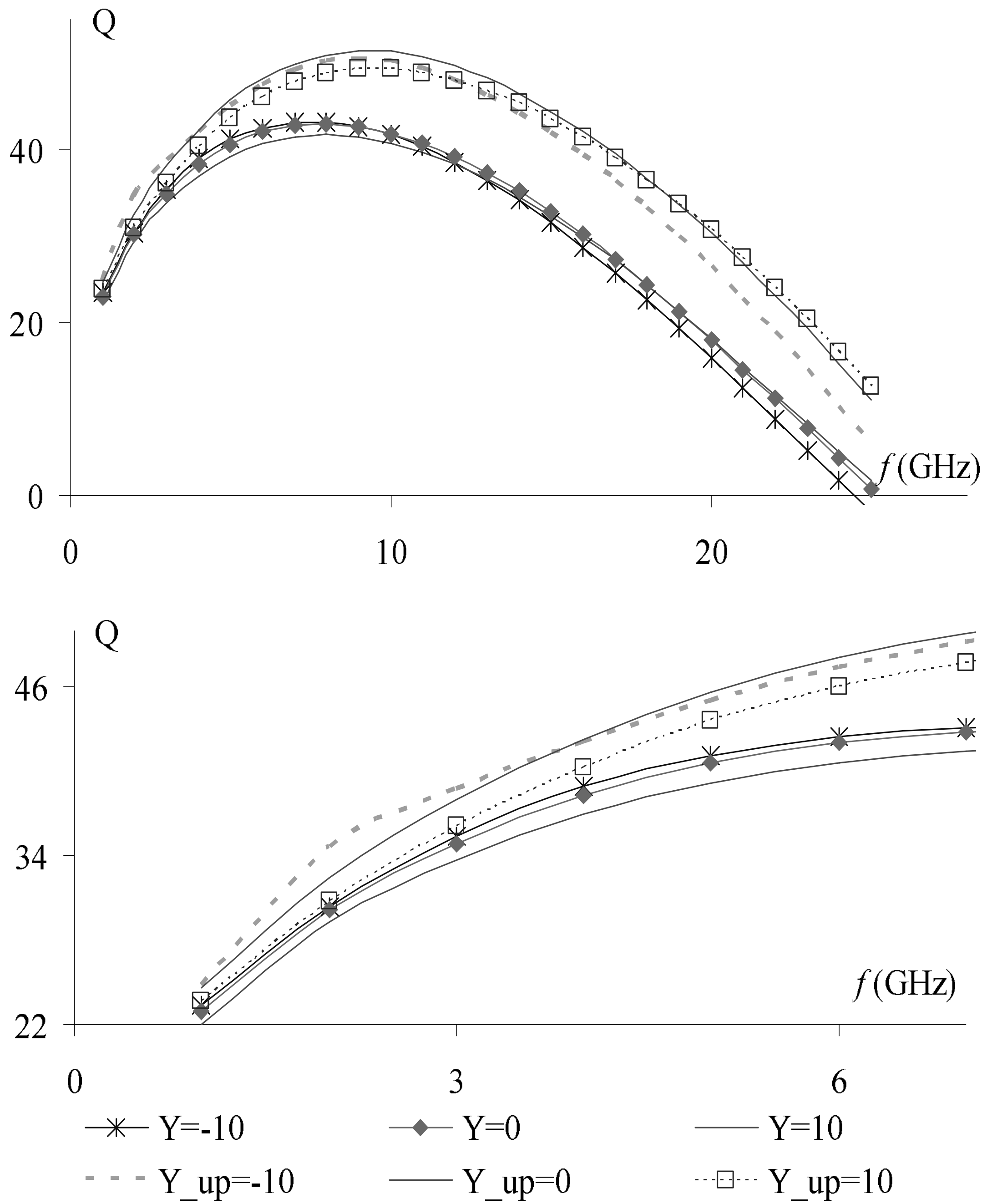


Figure B. 3: Comparison of *Q* factor simulation results for Y=y_{gvari} (in unit of μm) variations of the solenoid inductors.

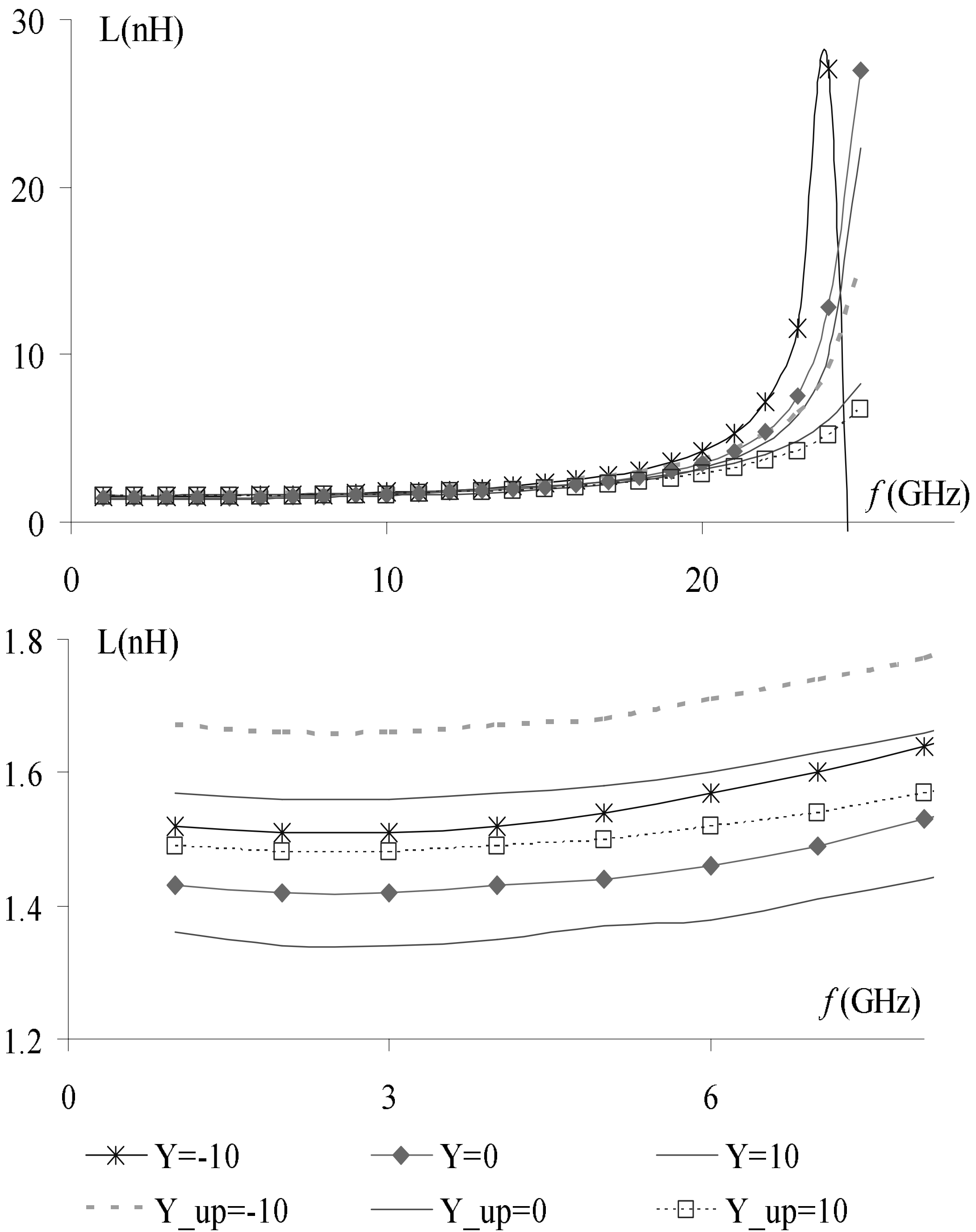


Figure B. 4: Comparison of inductance simulation results for Y=y_{gvari} (in the unit of µm) variations of the solenoid inductors.

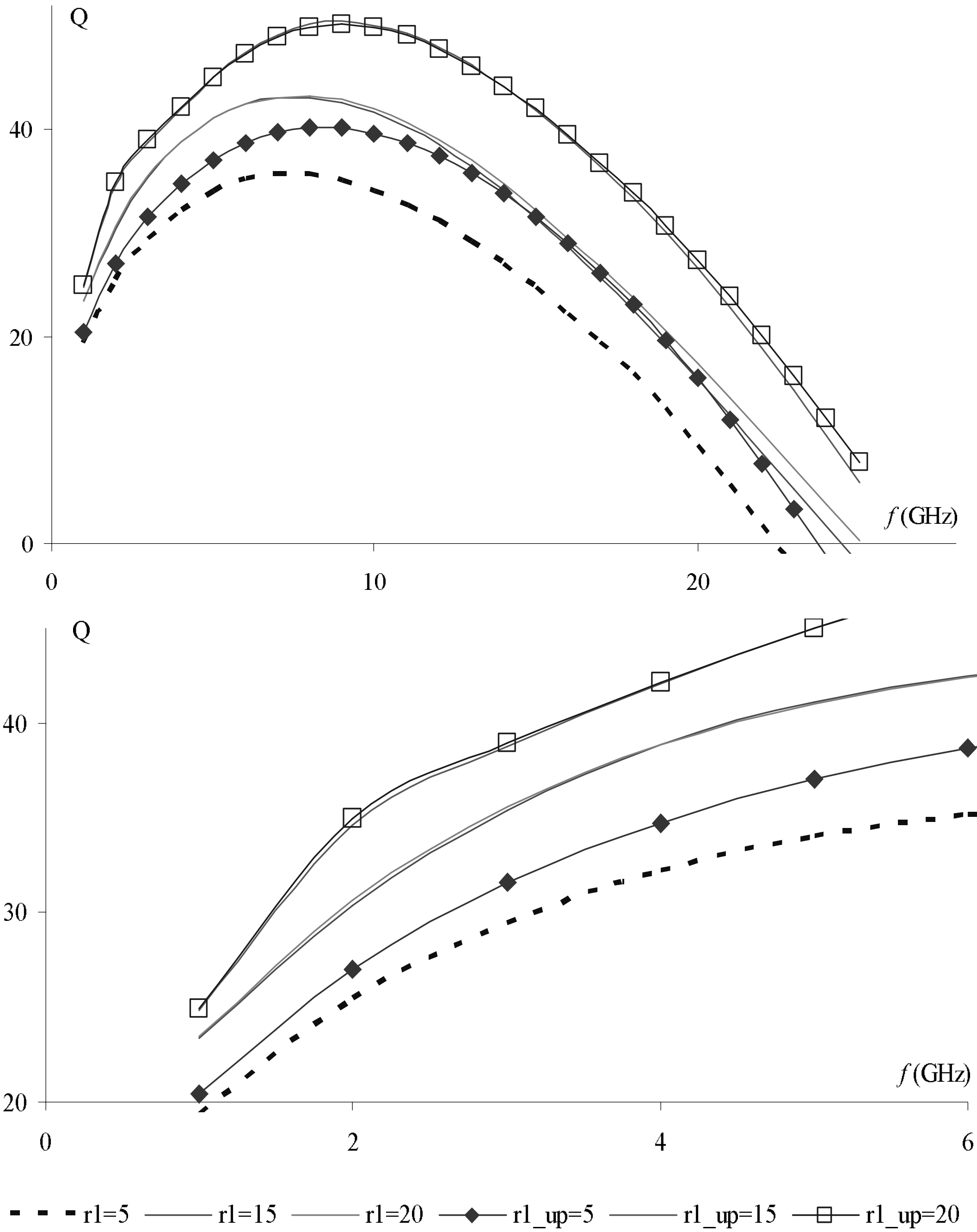


Figure B. 5: Comparison of Q factor simulation results for r_1 (in the unit of μm) variations of the solenoid inductors.

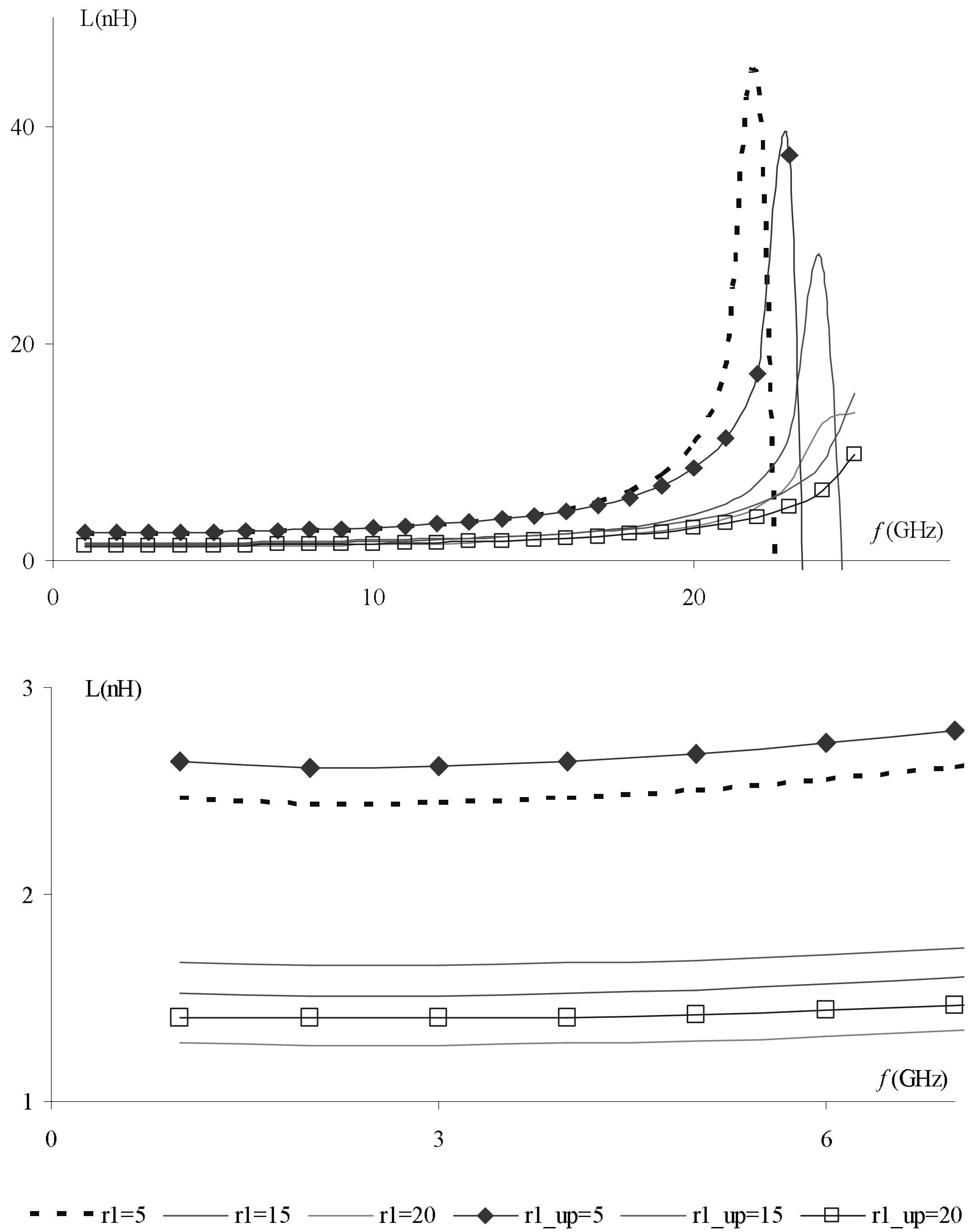


Figure B. 6: Comparison of inductance simulation results for r_1 (in the unit of μm) variations of the solenoid inductors.

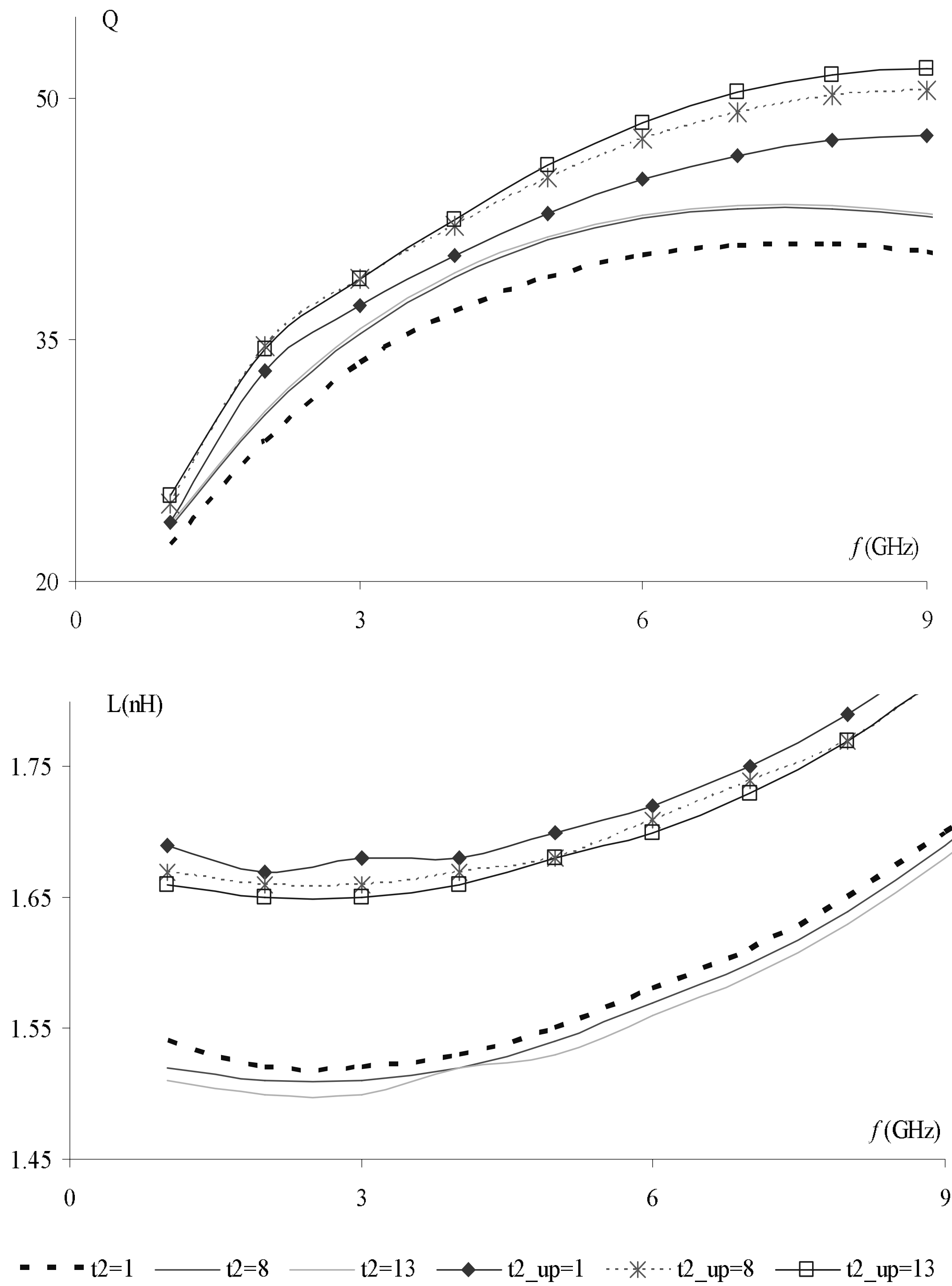
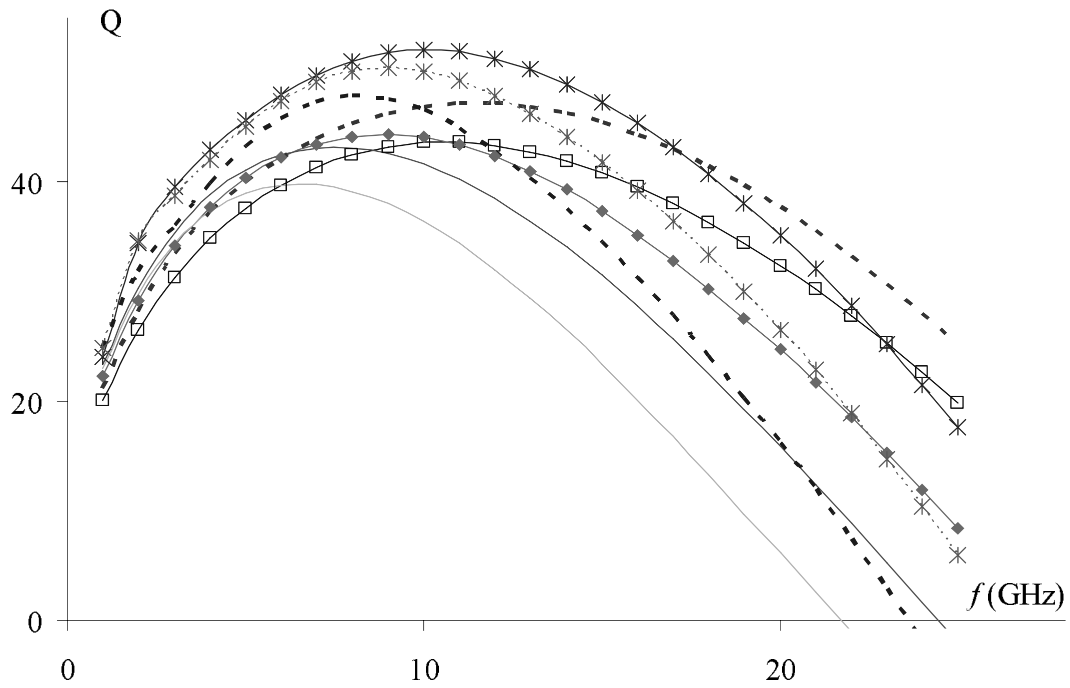


Figure B. 7: Comparison of the simulation results for the t_2 (in the unit of μm) variations of the solenoid inductors. (a) Q factor comparisons; (b) Inductance comparisons



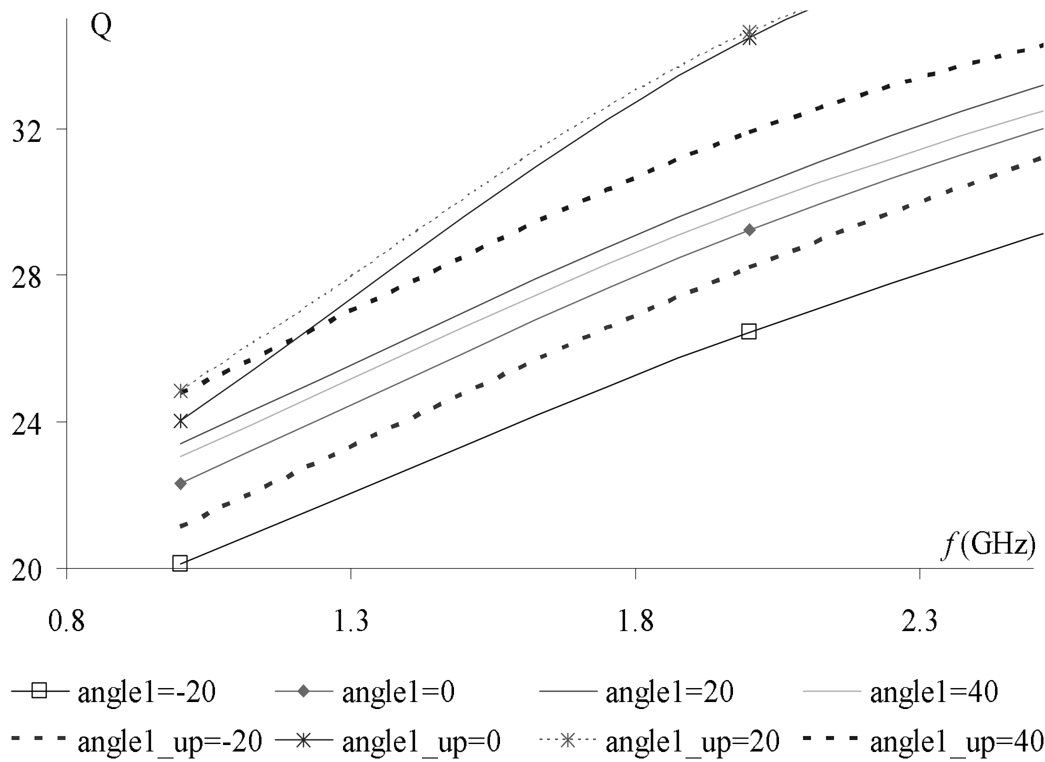


Figure B. 8: Comparison of the Q simulation results for angle1 (in the unit of degree) variation of solenoid inductors.

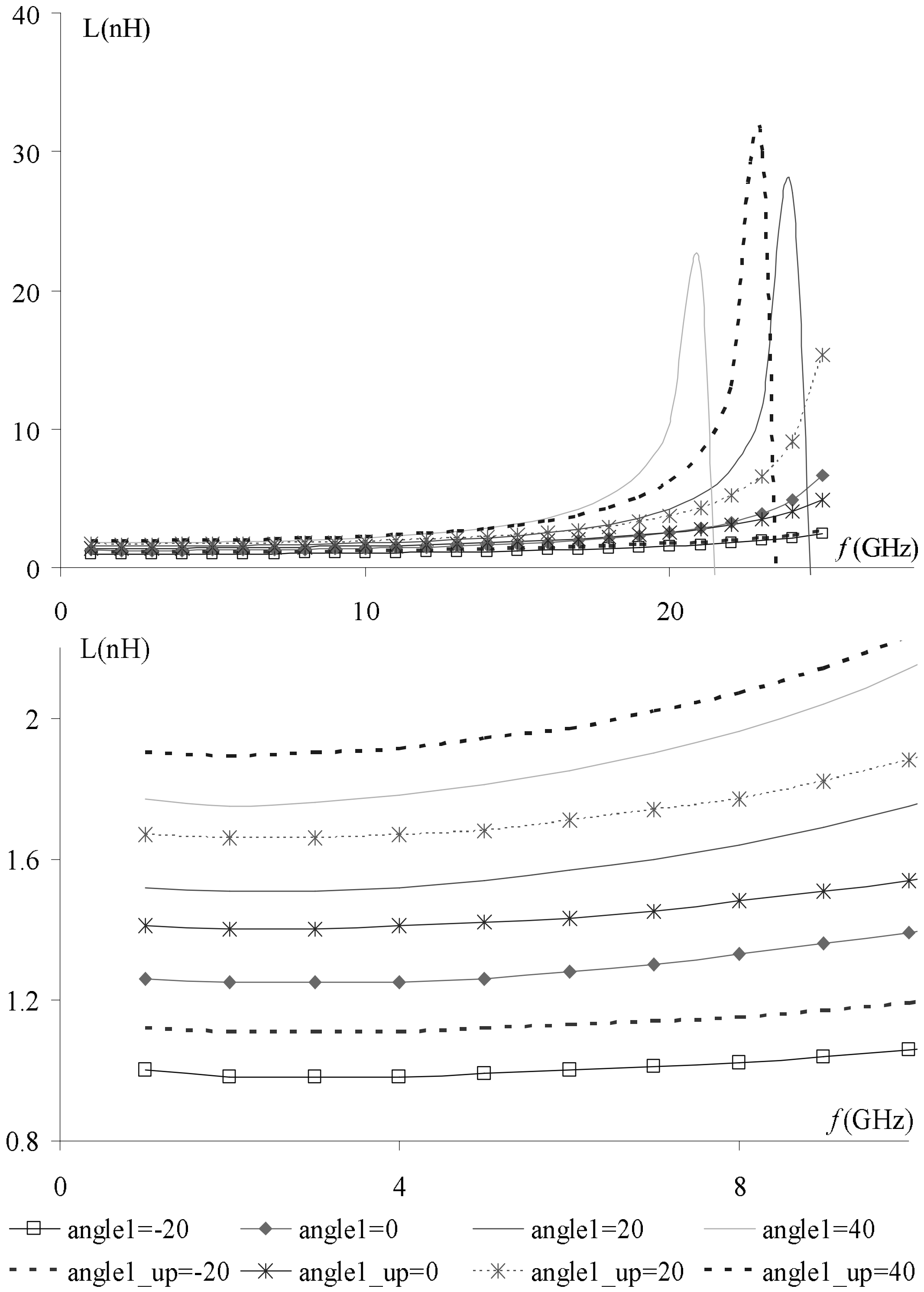


Figure B. 9: Comparison of the inductance simulation results for $angle_1$ (in the unit of degree) variation of solenoid inductors.