Transparent semiconducting oxides for active multi-electrode arrays

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Referat Die vorliegende Arbeit befasst sich mit der Anwendbarkeit von transparenter Elektronik basierend auf oxidischen Halbleitern in Multielektrodenarrays zur Messung von neuronalen Signalen. Im ersten experimentellen Kapitel werden auf Zinkoxid basierende Bauelemente untersucht. Verschiedene Varianten von Feldeffekttransistoren (FETs) werden charakterisiert und ihre Eignung zur Detektion von Zellsignalen überprüft. Die Anwendbarkeit physikalischer Modelle zur Beschreibung von ZnO-basierten Metal-Halbleiter-FETs (MESFETs) wird behandelt. Weiterhin wird die Eignung von einfachen Inverterschaltungen zur Spannungsverstärkung diskutiert. Das zweite Kapitel thematisiert Rauschmessungen an unterschiedlichen ZnO-basierten Proben, darunter Dünnfilme, Mikronadeln, MESFETs und Inverter. Darauf aufbauend wird die Auswirkung des gemessenen Stromrauschens auf die Sensitivität der Bauelemente nachvollzogen und theoretisch modelliert. Im dritten Kapitel wird das Verhalten der Bauelemente im Kontakt mit Elektolyt beschrieben. Die Signalübertragung von Spannungsänderungen im Elektrolyt auf die Chipelektronik wird mit verschiedenen Messmethoden charakterisiert. Dabei kommt teilweise ein selbstgebauter Vorverstärker zum Einsatz, dessen Aufbau ebenfalls beschrieben wird. Die Stabilität der verwendeten Materialien in physiologischen Salzlösungen und ihre Biokompatibilität wird überprüft. Darüber hinaus werden FETs mit Elektrolytgate und Zinkzinnoxid-Kanal vorgestellt.

Contents

1. Introduction

"Transparent electronics" is an expression, which has emerged in the last 10 to 15 years, maybe starting with the article "invisible circuits" of Thomas [1] in 1997. It describes the realization of electronic circuits on transparent substrates like glass, sapphire, or plastic foil, where all components are fabricated from optically transparent materials. This includes semiconductors, conductors, and insulating layers. Transparent insulators like SiO_2 and Si_3N_4 belong to the standard repertoire of research and industry. Also transparent conductive oxides (TCOs) like indium tin oxide (ITO) or aluminum doped zinc oxide can be found in a broad range of applications, in some cases since decades. Examples are window defrosters, electrochromic coatings, or the front electrodes of solar cells [2]. Transparent *n*-type semiconductors like ZnO or SnO_2 were subject of research since the early 20th century (e.g. [3]). However, it was not before 2003 that all these components were put together with the declared aim to fabricate transparent thin film transistors (TFTs) [4]. A major driving force for the progress of oxide semiconductor based TFTs in the last decade was the need of the TFT display industry for a faster alternative to the amorphous silicon circuits used as pixel drivers. Only recently, the technology was implemented in the mass production of large flatscreen displays [5], using TFTs based on amorphous InGaZnO channels. For this application, the use of glass as substrate together with the high electron mobility of InGaZnO compared to amorphous silicon was decisive. The transparency of the channel material is not exploited so far, likely because the long term stability of such devices is not sufficient under illumination [6]. The fabrication of transparent OLED displays with zinc tin oxide based driver circuits has been demonstrated [7], but the technology is not implemented up to now in commercial applications. Nevertheless, it can be expected that the successful integration of oxide semiconductor based TFTs in an industrial process will boost the introduction of the technology in other fields.

An application, where transparent electronics might be especially useful, are multi-electrode arrays (MEAs). MEAs are used to measure electric potential variations caused by biological tissue or single nerve cells. These devices emerged at the end of the 1970s, when measurement electrodes were integrated in the substrate of culture vessels instead of placing them on or into the examined tissue [8, 9]. Passive electrode chips are usually facricated on glass wafers. The conduction paths connecting the electrode sites with the external amplifiers are either metallic (typically gold or titanium/gold layers) or made up of TCOs (usually ITO). The chips are encapsulated by insulators, which can consist

of organic substances like polyimide or of anorganic materials, often layers of SiO_2 and Si_3N_4 [10, 11, 12]. Passive MEAs are widely used in basic research and commercial applications, e.g. for pharmaceutical screenings [11].

In 1968 Bergveld [13] proposed to place a field-effect transistor (FET) as buffer amplifier close to the test subjects, namely brain slices or single nerve cells. Wise and Angell [14] presented a similar approach using JFETs for electrophysiological recordings from brain samples. The common idea presented by these papers was, that the voltage signals are applied at the transistor gate, while source and drain are connected by low impedance conduction paths to an external amplifier. This was supposed to lead to a reduction of crosstalk between the conduction paths and to a minimization of the coupling of unwanted signals into the leads. Using silicon MISFETs, electrophysical measurements on locust muscles were performed in 1975 [15]. In 1981 Jobling *et al.* [16] were able to measure the extracellular potential of nerve cells from rat hippocampus *in vitro*. They also demonstrated signal multiplexing to display the signals of multiple measurement sites on a single oscilloscope. In the last decade the progress in silicon technology allowed the development of arrays with several thousand electrodes and electrode distances down to 8 μm [17, 18]. Silicon based MEAs are being commercialized in the last years, as reviewed 2011 by Graham *et al.* [19]. Different material systems and transistor realizations were tested in recent years, usually with the aim to improve the signal-to-noise ratio of active MEAs. Examples include transistors based on AlGaN/GaN [20], silicon nanowires [21], diamond [22], graphene [23], and organic semiconductors [24]. In the reported proof-of-principle experiments, these approaches were not able to outperform silicon devices in a way, which would lead to a change of technology. Hence, silicon chips will remain state of the art for active MEAs in the years to come.

While silicon based chips achieve unmatched electrode numbers and densities, the optical opacity of silicon prevents the use of inverted microscopes for the assessment of the biological samples on the chip. Optical microscopy can still be applied from above, but is restricted by the need to look through the cell medium. Culture vessel and additional electrodes in the electrolyte must be designed to allow microscope access from above. The resolution of thin nerve fibers can be difficult on silicon chips (see e.g. [25]), while inverted microcopes together with optically transparent MEAs allow comparably easy evaluation of nerve cell networks. The development of active MEAs similar to silicon chips, but based on transparent materials, could bring together the advantages of both approaches. The current state of transparent electronics at the brink between basic research and industrial application marks an excellent time to evaluate such new field of application. Nevertheless, it should be noted, that the technological knowledge for the fabrication of transparent devices is by no means comparable to silicon technology after decades of unprecedented technological advancement.

In recent years a variety of transistors based on oxide semiconductors has been demonstrated. This includes various channel materials, such as ZnO, InGaZnO, SnO, as well as

different field-effect transistor types, i.e. MESFETs, MISFETs, and JFETs. For many of those devices only static characteristics have been published. Especially noise has not been in the focus in this research area, yet. Dynamic properties were examined for MISFETs only, usually by realization of ring oscillators. Depending on the fabrication details, oscillation frequencies from the low kilohertz regime up to several megahertz were reported [26, 27]. Thus, a comparative study was necessary and conducted in the framework of this thesis, to shed light on the respective strengths of the different devices and to find the most suitable approach for the application in MEAs.

Up to now, zinc oxide is the only oxide semiconductor, where the fabrication of JFETs, MESFETs, as well as MISFETs has been demonstrated [28, 29, 30]. Therefore, this material was used as starting point for the comparison of device types. Crucial parameters for the application of a transistor in a MEA are the transconductance, determining the signal transmission, the cutoff frequency, below which signals are transmitted without damping, and the current noise generated by the device, limiting the sensitivity. Lambacher *et al.* [31] state for the extracellular recording of action potentials from mammalian neuron networks a required maximal input noise level of 100 μV and a minimum sampling frequency of 5 kHz. These requirements are not covered by many publications, where the transconductance as well as quantities like ON/OFF-ratio and subthreshold swing are discussed. A "good" transistor according to those figures of merit is not necessarily suitable for application in MEAs.

In this work, the requirements for the desired application as well as other customary FET properties were investigated. The applicability of theoretical models was evaluated, since in the diverse field of oxide semiconductors often no standard device models exist. This is especially true for JFETs and MESFETs, while possible theoretical descriptions for oxide based MISFETs are discussed in [2]. Special attention was paid to noise measurements, as up to now no systematic survey on noise sources in oxide semiconductors exists to the best knowledge of the author. To evaluate the applicability of ZnO based devices in MEAs, the operation under cell culture conditions had to be tested and proof-of-principle measurements with living cells performed. This included the development of a stable passivation and encapsulation for the chips and the assembling of a suitable measurement setup.

2. Measurement Setup and Sample Fabrication

2.1. Device Fabrication

2.1.1. Pulsed lased deposition

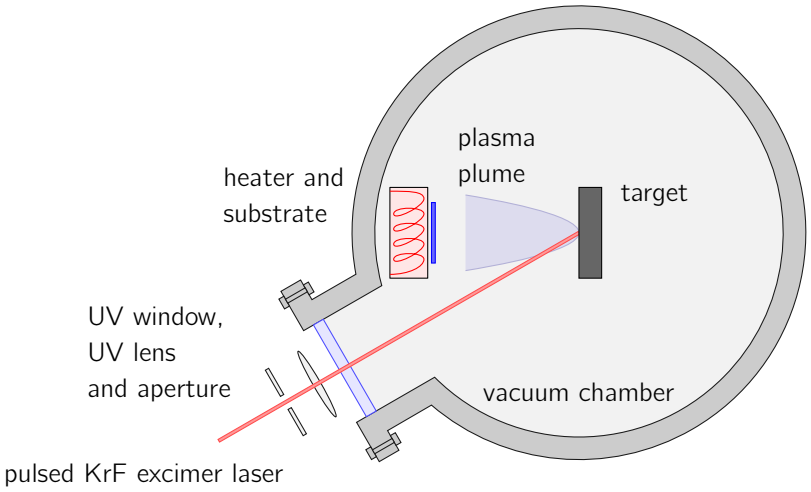

Figure 2.1.: Schematic view of a PLD system. Not shown are the vacuum pump and the inlet for the background gas. Compare [32].

Oxide materials used in this work were grown by pulsed laser deposition (PLD). The PLD process takes place in a vacuum chamber, where a ceramic target is irradiated by high energy laser pulses. A schematic view of a PLD chamber is shown in Fig. 2.1. For this work, a Lambda Physik LPX 300 excimer laser operating at 248 nm with a laser pulse energy of 600 mJ was used. The laser pulse width is in the nanosecond range and the repetition range in the range between 1 Hz and 50 Hz. Most depositions for this work were conducted at 3 Hz. Several processes are involved in the process of material ablation from the target and deposition on the substrate. The ablation of material from the target is based on thermal evaporation, photoinduced electronic sputtering,

and indirect sputtering by secondary ions and electrons from the plasma. This plasma forms due to the partial absorption of laser energy in the ablated material and expands in the direction of the substrate. The film growth mechanisms are comparable to other deposition methods, and depend on material system, substrate temperature and the energy of the incident particles. The latter is controlled mostly by the laser energy and the background gas pressure in the chamber. The deposition of oxides always took place in a pure oxygen atmosphere, with a pressure depending on target material and desired thin film properties. Advantages of PLD are the wide range of materials, that can be grown, and good conservation of the target stoichiometry in the thin films. In some cases the formation of droplets, larger particles emitted from the target, can complicate the processing of devices, expecially when droplets break through the vertical stacking of multiple material layers due to their size. Further information on PLD in general and the system used here can be found in [32, 33]. For this work, all PLD targets were prepared by G. Ramm and the deposition of thin films was conducted by H. Hochmuth and P. Schlupp (all from Universität Leipzig).

2.1.2. Sputtering

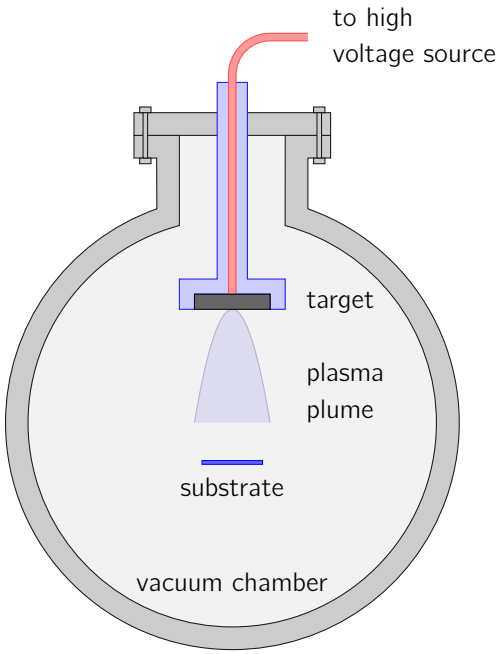

Figure 2.2.: Schematic view of a dc sputtering chamber. Not shown are the vacuum pump and the inlet for the background gas. Vacuum chamber and substrate holder are grounded.

The sputtering deposition method uses a plasma, which is created by impact ionization of the background gas due to a high externally applied voltage. The electric field accelerates the ions towards the target, where material is ablated and accelerated mostly perpendicular to the target surface. The largely neutral particles emitted from the target subsequently condensate on the substrate. The process is schematically depicted in Fig. 2.2. For the fabrication of metallic contacts dc magnetron sputtering was used, i.e. sputtering with a constant voltage and additional magnetic fields at the target to enhance the sputtering rate. No substrate heating was applied. The process for metallic thin films usually took place in a pure argon atmosphere at 0.02 mbar. However, for the fabrication of highly rectifying Schottky contacts on oxide semiconductors it has been shown beneficial to use a mixed atmosphere of oxygen and argon [34]. This process is called reactive sputtering and was applied for all Schottky contacts in this work. It should be noted, that reactively sputtered metal films will be denoted only by the metal names in the following chapters, although they are partially oxidized. Due to the unknown fraction of oxidization, it seemed more clear to speak of reactively sputtered Au, Pt, etc., instead of using terms like AuO_x, PtO_y and so forth.

2.1.3. Photolithography

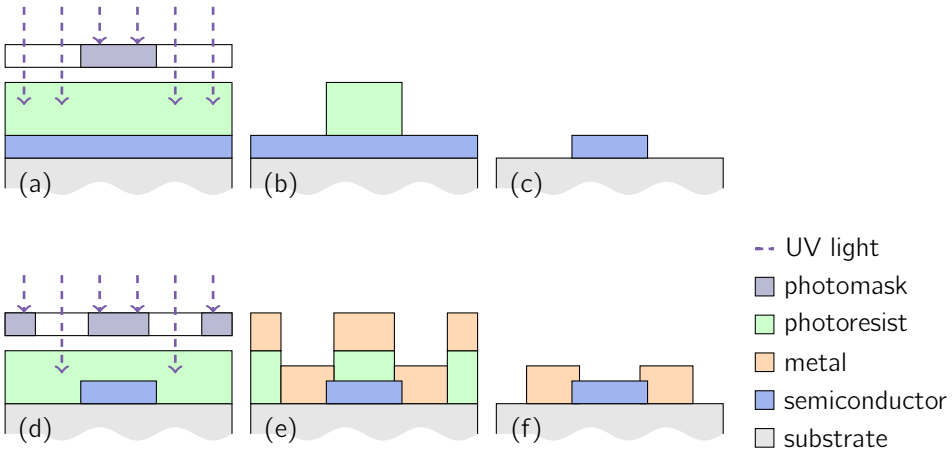

Figure 2.3.: Schematic depiction of the photolithographic structuring of semiconductor devices. (a) Illumination of the photoresist by UV light through a photomask. (b) Development of the resist. (c) Etching of the semiconductor and subsequent removal of the resist using organic solvents. (d) Illumination of a new resist layer. (e) Development of the resist and deposition of a metal layer. (f) Removal of the resist together with the capping metal parts.

Most deposition methods, including PLD and sputtering, cover the whole sample area with the desired material. For the fabrication of devices, these layers must be structured

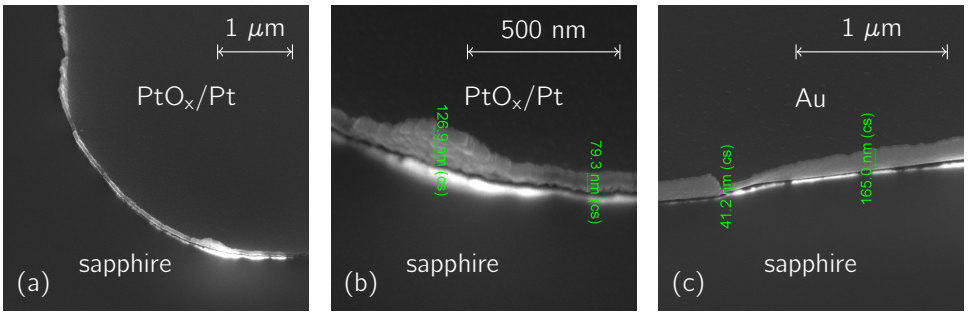

Figure 2.4.: Edge bending of sputtered metal layers on a-sapphire substrate due to lift-off with the AZ 1415H photoresist. The SEM images are recorded at an angle of 52° to the sample surface. (a),(b) PtO_x layer (thickness ≈ 40 nm) with Pt capping (thickness ≈ 10 nm) (c) Au layer (thickness ≈ 18 nm).

laterally, usually by the application of photolithography. This technique is depicted schematically in Fig. 2.3. A photo sensitive resist is spreaded over the sample using spin coating. The resist thickness is controlled by the resist viscosity and the applied angular velocity. Consequently, a photomask is placed over the sample and illuminated with UV light. The following bath in the developer patterns the photoresist. For so-called positive resists, the illuminated parts dissolve in the developer, while for negative resists the shadowed parts are removed. Subsequently different etching techniques can be used to pattern the underlying material layers. It is also possible to deposit a new material layer on top of the resist. By using an organic solvent and ultrasonic cleaning the resist is stripped from the sample, leaving the new material only where the resist had been dissolved beforehand. Such a lift-off process can be advantageous compared to etching, if suitable etchants are not available or if the etch rate is slow, e.g. for noble metals. However, deposition at high temperature is not possible, as most resists degrade at temperatures above 150°C. Another drawback can be the upbending of metal edges as depicted in Fig. 2.4. This happens especially for multi-purpose resists like the AZ 1415H resist used for this work, as the resist edges are not very steep. The metal layer has to break during lift-off along the resist edges, which needs a certain force that also pulls the metal layers up. A possiblity to avoid this effect is the usage of special negative photo resists for lift-off.

2.1.4. SU-8 Resist

SU-8 is an epoxy based negative photoresist. It is used for passivation and encapsulation of electronic devices and has also been reportedly used with oxide semiconductor devices [35, 36]. Due to its excellent biocompatibility it is also used as capping layer for MEAs, e.g. in diamond based transistor arrays [22] and silicon nanowire transistor arrays [21].

After illumination and annealing at temperatures around 100°C, the polymer layer is very resistant against most kinds of organic solvents, e.g. isopropanol and acetone. Actually, no solvent for easy stripping of properly annealed SU-8 is available. In this work the resist GM 1040 from Gersteltec Sarl, Switzerland, was used, with a layer thickness of approximately 1 μm.

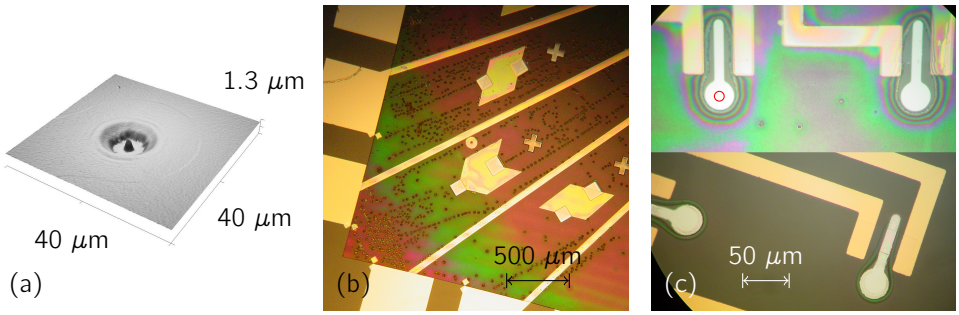

Figure 2.5.: SU-8 processing issues: (a) Overexposure when using a circular mask with a diameter of 10 μm, here an AFM topography image of the SU-8 surface. (b) Bubble-like disturbances in the SU-8 layer, probably due to underexposure. (c) Coverage avoidance for gates capped with sputtered TiO_2 (above) and Pt (below). The desired hole size in the SU-8 layer is depicted by the red circle.

Being a negative resist, SU-8 is cured by UV radiation. Thus, areas, which should be free of resist after development, must be covered by the photomask during illumination. For small holes in the polymer layer this can be challenging, as stray light cures supposedly covered parts of the resist. Fig. 2.5(a) demonstrates, that a circular mask might also concentrate stray light in the center, leaving a cone of SU-8 in the middle of the planned hole. Reduction of the UV exposure dose below a certain threshold is not possible, however, as the layer becomes unstable without proper curing. Typical signs of underexposure observed in our experiments were bubble-like disturbances in the resist (Fig. 2.5(b)), which appeared after development. Proper optimization of the exposure dose proved to be challenging for samples with transparent substrates, as UV light penetrates the substrate and is either absorbed or scattered at the sample holder. On the other hand, metallized regions on the sample reflect the radiation at least partially, leading to an additional irradiation dose. To reduce this difference in the exposure dose on different sample areas, the samples were placed on a mirror during exposure, as depicted in Fig. 2.6(a). Nevertheless, after development the SU-8 layer on transparent regions often extends several microns into areas which were shadowed by the photomask during exposure, due to stray light from the substrate.

Several material surfaces were often not covered by SU-8 after development, as depicted by Fig. 2.5(c). This concerned especially sputtered platinum, titanium oxide, and PLD grown zinc tin oxide, in some cases also sputtered gold. Typically gate contacts were

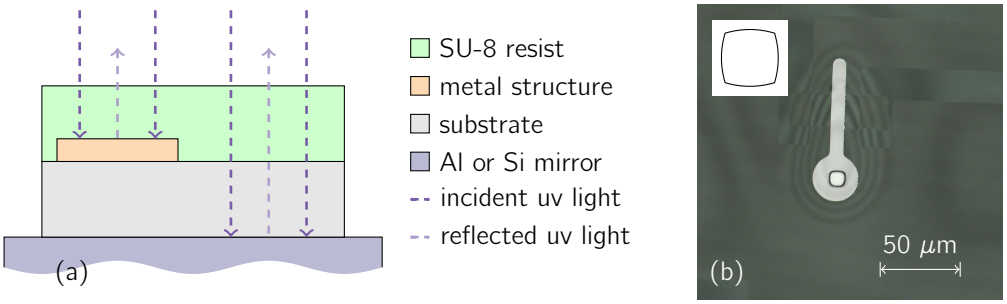

Figure 2.6.: Techniques applied for improving the SU-8 processing: (a) Improved homogeneity of UV illumination by using a mirror. (b) Diminishing stray light effects by substituting circular shapes with a rounded square (depicted in the inset), in contrast to the electrode opening shown in Fig 2.5(a).

affected, where only a small hole in the SU-8 layer, situated in the middle of the electrodes, was desired. If the cause would be a wetting problem only, the effect should appear directly after spin coating, however it was not visible before illumination. With samples completely covered by these materials good lithography results were achieved. In the case of gold contacts, good results were achieved with adjusted illumination conditions. The exposure time was increased by 30% and the back reflection was reduced by exchanging the aluminum coated mirror beneath the substrate with a polished silicon substrate. This indicates, that the SU-8 layer on the transparent parts of the chip exhibits stronger strain during polymerization than on the metallized parts, when the total irradiation dose during exposure is larger on the transparent areas. This would be the case, when the back reflection from the mirror is more intense than the back reflection from the metallized parts. The strain in the layer around the metal gate structures pulls the less crosslinked SU-8 from the gate contact, supported by the non-illuminated hole in the middle of the gate electrode. This underlines, that the exposure conditions for SU-8 resist must be very carefully controlled for samples with inhomogenous UV reflectivity. This is especially relevant for structures on transparent substrates, where the back reflection through the substrate must be considered. Despite strict control of the processing parameters, occasional recalibration is neccesary, due to the narrow window of feasible exposure conditions.

2.2. Measurement Methods

Sample preparation For electrical measurements, it is essential to establish stable conducting contacts to the sample. With a wafer prober, metal needles are placed directly on the sample, enabling flexible selection of the measurement position. In some cases the wafer prober does not provide the necessary conditions for the measurement. E.g. for

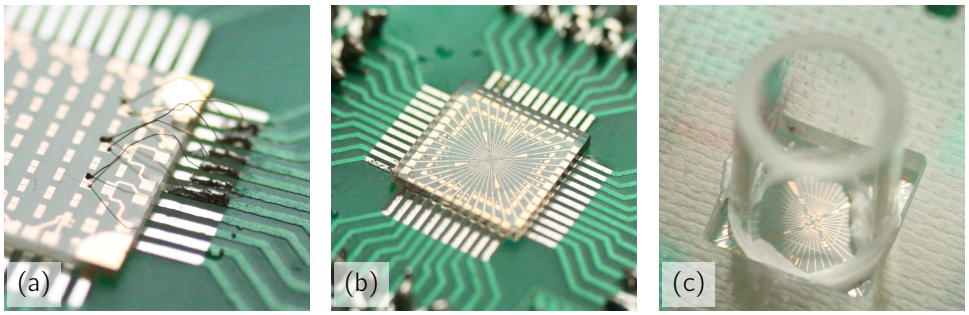

Figure 2.7.: Sample mounting techniques. The sample size is 10×10 mm^2. (a) Bonding with gold wires. (b) Flip-chip contacting, sample is mounted face-down on the PCB. (c) Glass ring with outer diameter of 8 mm mounted on a flip-chip contacted sample. In contrast to (b) the PCB is turned face-down.

accurate noise characterization the shieldings of the prober and the feed cables are not sufficient. Another example are measurements with living cells, where sufficient control over the environmental conditions must be guaranteed. For stable electrical contacts outside the wafer prober, the samples were mounted on printed circuit boards (PCBs) with Epotek H20E conducting epoxy glue, either using gold wires soldered to the PCB or flip chip contacting, where the contacts of the face-down sample are fixed directly to the board [37]. The contacting methods are depiced in Fig. 2.7. For measurements on chips in contact to electrolyte, the samples were mounted by the flip-chip technique on a PCB with opening in the center. Through this opening a glass ring was attached to the sample surface with silicon rubber (RTV162Q, Momentive Performance Materials Inc.), as shown in Fig. 2.7(c). The electrical contacts to the PCB are outside of the glass ring, so that only a defined area in the middle of the sample is exposed to the electrolyte.

Electrical Measurements Electrical characterization was conducted with an Agilent 4155C semiconductor parameter analyzer with pulse generator expander 41501B. The samples could be measured in a Suss MicroTec PA200 wafer prober or in an Agilent 16442A test fixture. With this setup, current-voltage measurements (I-V) and quasi-static capacitance-voltage measurements (QSCV) were performed. Time-resolved sampling measurements with rectangular voltage pulses are possible, but with a maximum sampling frequency of 12.5 kHz. Hence, for the recording of time traces and the determination of cutoff frequencies, a TiePie HS3 oscilloscope and signal generator was used. Capacitance-voltage measurements (C-V) were performed with an Agilent 4294A precision impedance analyzer. All measurements presented in this work were conducted in the dark, when not otherwise stated.

Imaging methods High resolution topography images were recorded with a Park Systems XE-150 atomic force microscope (AFM). Optical microscope images as well as topography images were taken with an Keyence VK-X200K laser scanning microscope (LSM). Scanning electron microscopy (SEM) was conducted with a NovaLab 200 dual beam system, which combines the electron microscopy setup with a focussed beam of Ga^+ ions (FIB). The ion beam was used to mill trenches in the sample surface, in order to obtain SEM cross section images. SEM and FIB were operated by J. Lenzner (Universität Leipzig).

2.3. Current Amplifier with Offset Compensation

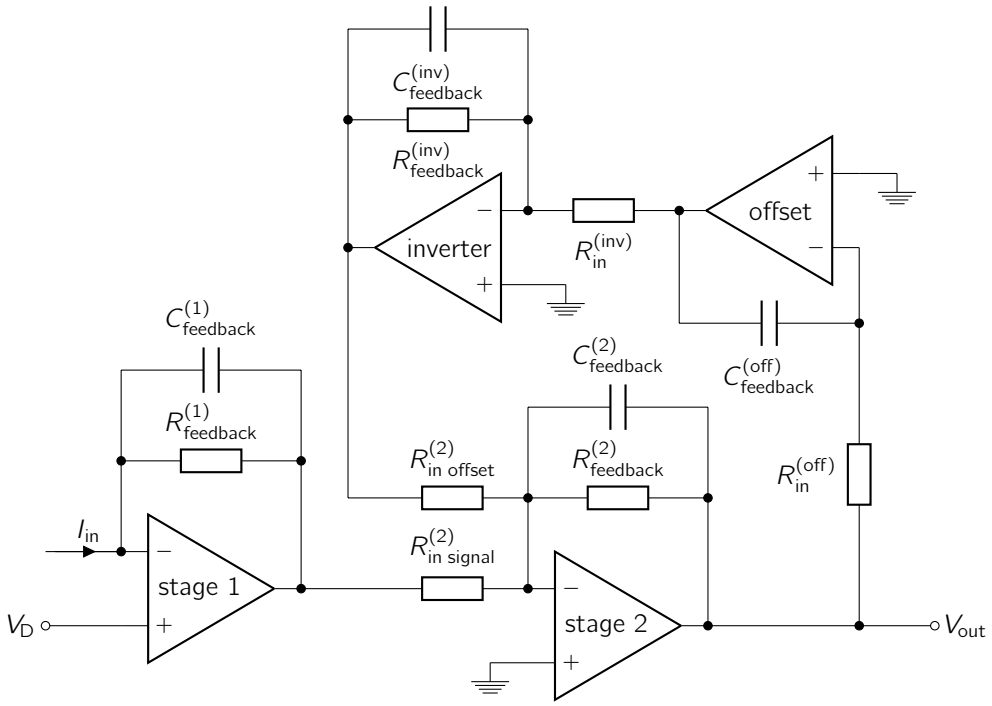

Figure 2.8.: Circuit diagram of a current amplifier with offset compensation, adopted from [10] for this work.

The measurement of small current signals with comparably large offset, as necessary for the analysis of MEA signals in this work, is not directly possible with usual oscilloscopes. The Agilent 4155C used for I-V characterization of devices has a rather low maximum measurement frequency of 12.5 kHz, and offers no possibility for offset compensation. Thus, for this work a preamplifier was built, which is able to amplify signals in the nanoampere range, while automatically cancelling offsets up to the microampere range.

The amplifier layout has been adopted from Ecken *et al.* [10] and is shown in Fig. 2.8. The output voltage is given by

$$\Delta V_{\text{out}} = \Delta I_{\text{in}} \cdot R^{(1)}_{\text{feedback}} \cdot \frac{R^{(2)}_{\text{feedback}}}{R^{(2)}_{\text{in signal}}}. \tag{2.1}$$

The circuit has been optimized to increase the signal-to-noise ratio (SNR). Stage 1 and 2 work as low-pass filters, in order to surpress high frequency noise in the amplification chain as soon as possible. In [38], amplification ratios of $R^{(2)}_{\text{feedback}}/R^{(2)}_{\text{in signal}} = 10$ for the signal and $R^{(2)}_{\text{feedback}}/R^{(2)}_{\text{in offset}} = 100$ for the offset were used. In the device built for this work, the offset compensation stage was dominating the amplifier noise, when similar ratios were used. By reducing the offset amplification ratio to 22, the input transimpedance amplifier (stage 1 in Fig. 2.8) became the limiting noise source. A main noise contribution in the relevant frequency range is the thermal noise of resistor $R^{(1)}_{\text{feedback}}$, which is given by $\text{Var}(V) = 4k_{\text{B}}TR\Delta f$. As the output voltage ΔV_{out} depends linearly on $R^{(1)}_{\text{feedback}}$, the SNR is proportional to $(R^{(1)}_{\text{feedback}})^{0.5}$, thus a large resistance is favorable. The upper boundary for ΔV_{out} is the maximum output voltage $V^{(1)}_{\text{out,max}}$ of the stage 1 op-amp, as the current through the feedback resistor matches always the input current:

$$I_{\text{in,max}} \leq \frac{(V^{(1)}_{\text{out,max}} - V_{\text{D}})}{R^{(1)}_{\text{feedback}}} \tag{2.2}$$

The signal transmission in dependance on the the frequency was evaluated by the application of sinusoidal signals at the input, using a metal film resistor as device-under-test (DUT). The transfer function shown in Fig. 2.9 is constant in the range between 3 Hz and 10 kHz, where it adopts the amplification rate given by Eqn. 2.1. The lower cutoff is given by the offset correction circuit and can be described as a first-order high-pass filter with

$$f_{\text{c}} = \frac{R^{(2)}_{\text{feedback}}}{R^{(2)}_{\text{in offset}}} \frac{1}{2\pi R^{(\text{off})}_{\text{in}} C^{(\text{off})}_{\text{feedback}}}. \tag{2.3}$$

The first term is the amplification of the offset signal in stage 2, which influences the cutoff frequency through the feedback loop used for offset cancelling. The upper cutoff is determined by the two low-pass filters of stages 1 and 2. The simple multiplication of the transfer functions for both stages leads to a certain overestimation of the bandwidth,

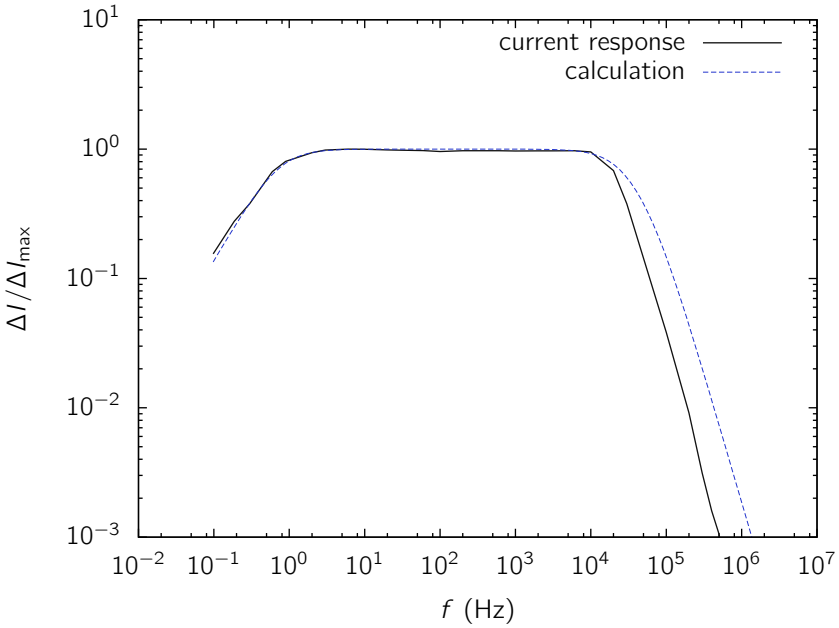

Figure 2.9.: Frequency response of the MEA amplifier, measured with an input amplitude of 0.02 V and 1 MΩ input resistance. The calculation includes the two low-pass filters of stage 1 and 2 and the offset compensation. The measurement is normalized by its maximum value.

as shown in Fig. 2.9, but gives an estimate good enough for the proper dimensioning of the components.

Two amplifiers have been designed and built for this work. The first one has a single amplifier channel and is depicted in Fig. 2.10(a). The amplifier is powered by two 9 V batteries and placed together with the sample in an aluminum box, which serves as shielding. The MEA is plugged into a socket consisting of standard PCB connectors. Insertion and removal of MEAs must be carefully handled, as twisting can lead to a break of the flip-chip contacts between PCB and MEA. The measured MEA channel is manually selected by a jumper. In addition to the layout presented in Fig. 2.8 a third amplification stage was implemented, using a Linear Technology LT1167 instrumentation amplifier, whose amplification can be adjusted by a trimming resistor. Thus, the final output voltage can be optimized for the ocilloscope, which is used for data recording. The voltage V_D can be applied externally or supplied from the batteries, fixed at 2 V by a voltage divider. The overall amplification used for the recordings in this work was 10^8 V/A. A list with the components used for the device can be found in Appendix A. A second amplifier with ten identical measurement channels was intended for actual recordings from nerve cells. The main PCB was designed for the use of SMD components and produced by the Fritzing Fab Service, Potsdam. For connection with the MEAs, spring contacts have been implemented. This should prevent the degradation of the

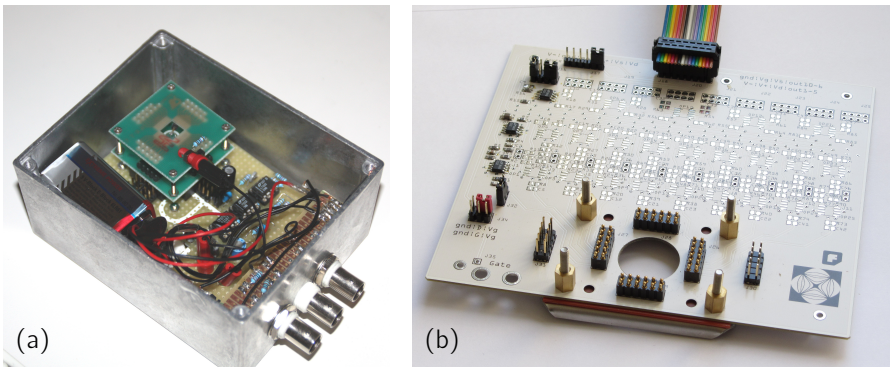

Figure 2.10.: Amplifiers built for the transmision of MEA signals to an external oscilloscope or analog to digital converter. (a) Single channel amplifier in aluminum casing. The MEA is mounted on the lower green PCB, which has an edge length of 40 nm. The upper green PCB holds the Ag/AgCl electrode, which applies the reference voltage to the electrolyte. (b) Main PCB of amplifier with ten identical channels. Only the first channel to the right is fitted with components. The width of the PCB is 140 mm.

flip-chip contacts, due to twisting of the MEA PCBs when using plug-in contacts. The main PCB of the amplifier is shown in Fig. 2.10(b). One channel has been finished and successfully tested, however the development was suspended in favor of further MEA evaluation and improvement.

3. Oxide Semiconductor Based Devices

3.1. Theoretical Description

3.1.1. Schottky Barrier Contacts

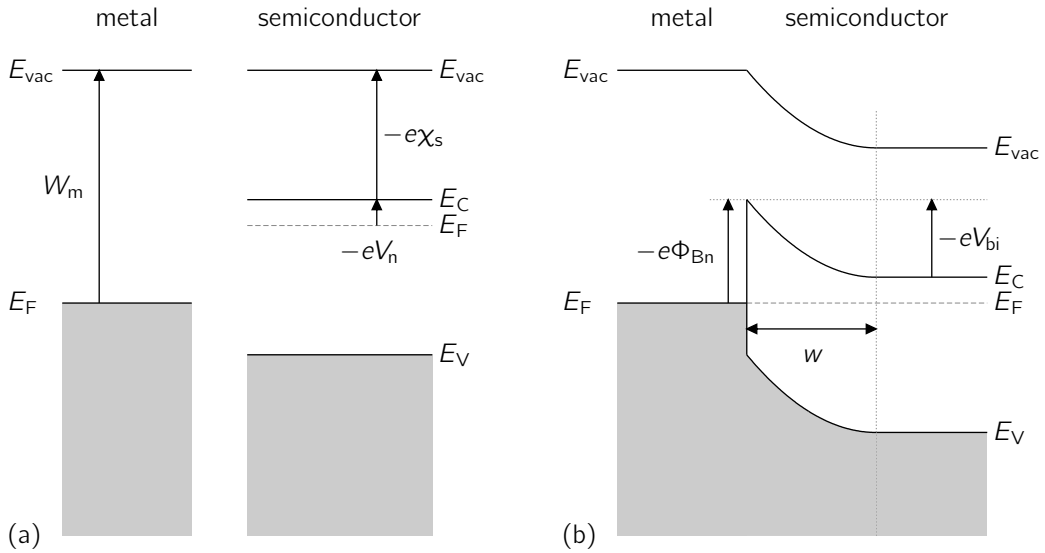

Figure 3.1.: Simplified band diagramm of a metal and a n-type semiconductor (a) seperate and (b) in contact with each other, for the case that surface states can be neglected. According to [39].

The contact between a metal and a semiconductor is not neccessarly ohmic, which would be indicated by a linear current-voltage characteristic. In a metal the Fermi energy with respect to the vacuum energy is determined by the work function $W_m = -e\Phi_m = E_{vac} - E_F$. In a semiconductor the electron affinity χ_s is the difference between vacuum energy and conduction band edge, while the difference between conduction band and Fermi energy is denoted $-eV_n$. Using these quantities the Fermi energy in the semiconductor is $E_F = E_{vac} + e(\chi_s + V_n)$. When metal and semiconductor come into contact, charges will flow until the Fermi energy is constant throughout the sample (in

equilibrium, i.e. no external potentials applied). Far from the interface the equilibrium conditions as described before prevail, but at both sides of the interface space charge regions with opposite sign are formed. In the metal these charges are located directly at the interface, due to the high density of states. At the interface the Schottky barrier $\Phi_{\mathrm{Bn}} = \Phi_{\mathrm{m}} - \chi_{\mathrm{s}}$ is formed. On the semiconductor side the energy bands are bent within a region of width w by the built-in potential $V_{\mathrm{bi}} = \Phi_{\mathrm{Bn}} - V_{\mathrm{n}}$. For a n-type semiconductor with donor density N_{D}, as depicted in Fig. 3.1, this increases the energetic difference between Fermi level and conduction band close to the interface. Within the so-called abrupt approximation all donors in the space charge region are assumed to be ionized, which results in a space charge density of $\rho_{\mathrm{sc}} = -eN_{\mathrm{D}}$. The solution for the one-dimensional Poisson's equation with constant charge density is a electrostatic potential with quadratic dependence on the position x. With the boundary conditions outlined in Fig. 3.1 the depletion layer width w is given as

$$w = \left[\frac{2\epsilon_{\mathrm{s}}}{eN_{\mathrm{D}}}\left(V_{\mathrm{bi}} - V_{\mathrm{ext}}\right)\right]^{1/2}. \tag{3.1}$$

This equation also considers an external potential V_{ext} applied at the metal side in reference to the semiconductor. Using a simple parallel-plate capacitor model, the diode capacitance is given by $C = \epsilon_{\mathrm{s}} A_0 / w(V_{\mathrm{ext}})$, where A_0 is the diode area. Measuring the capacitance in dependence on V_{ext} can be used to determine N_{D}, using the relation

$$\frac{\mathrm{d}}{\mathrm{d}V_{\mathrm{ext}}}\left(\frac{1}{C^2}\right) = -\frac{2}{e\epsilon_{\mathrm{s}} A_0^2 N_{\mathrm{D}}}. \tag{3.2}$$

Electrons can cross the Schottky barrier by their thermal energy, due to diffusion, by tunneling through the barrier, or by any combination of these processes. For nominally undoped ZnO thin films with thickness around 1 μm it was shown, that thermionic emission is the dominant current transport process [40]. The cited paper demonstrates, that only for low net doping densities or low mobilities diffusion must be considered. The thin films used for this work usually had charge carrier densities above 10^{18} cm^{-3}, so that diffusion was not relevant to describe the transport across the Schottky barrier. However, due to the decreased barrier width at high doping densities, tunneling assisted transport cannot be neglected.

The transport of hot electrons over the top of the barrier is called thermionic emission (TE). By taking into account the barrier height Φ_{Bn} and a Boltzmann distribution for the electrons, the current density from the semiconductor to the metal is described by [39]

$$j_{\mathrm{s}\to\mathrm{m}} = A^* T^2 \exp\left(-\frac{e\Phi_{\mathrm{Bn}}}{k_{\mathrm{B}}T}\right)\exp\left(\frac{eV}{k_{\mathrm{B}}T}\right), \tag{3.3}$$

with the Richardson constant A^* defined by

$$A^* = \frac{4\pi e m^* k_\mathrm{B}^2}{h^3}. \tag{3.4}$$

The condition $j = 0$ for $V = 0$ gives the total current density [39]

$$j_\mathrm{TE} = j_\mathrm{s} \left[\exp\left(\frac{eV}{\eta k_\mathrm{B} T} \right) - 1 \right], \tag{3.5}$$

where j_s is the saturation current densisty defined as

$$j_\mathrm{s} = A^* T^2 \exp\left(-\frac{e\Phi_\mathrm{Bn}}{k_\mathrm{B} T} \right). \tag{3.6}$$

η is called ideality factor. For an ideal diode it equals one, but is often larger for actual devices. The image force lowering of the barrier, called Schottky effect, causes an increased η, but results only in values smaller than 1.03 [39]. Larger values can be caused by inhomogenous barriers, which exhibit a bias dependeny in the effective barrier height [41, 42].

At low temperatures or at high carrier densities there is a high probability for electrons to tunnel through the barrier at an energy E_m between the bulk Fermi level and the top of the Schottky barrier. This thermally assisted tunneling process is called thermionic field emission (TFE).

The current density arising from this process has been derived by Padovani and Stratton [43]. For an intermediate temperature range and forward bias they give

$$j_\mathrm{TFE,for} = j_\mathrm{s,for} \exp\left(\frac{eV}{E_0} \right), \tag{3.7}$$

with the saturation current density

$$j_\mathrm{s,for} = \frac{A_\mathrm{s}^* \sqrt{\pi E_{00}(E_\mathrm{B} - eV + \xi_2)}}{k_\mathrm{B} T \cosh(E_{00}/k_\mathrm{B} T)} \times \exp\left(-\frac{E_\mathrm{B}}{E_0} + \xi_2 \left(\frac{1}{k_\mathrm{B} T} - \frac{1}{E_0} \right) \right). \tag{3.8}$$

The reverse current density is

$$j_{\mathrm{TFE,rev}} = j_{\mathrm{s,rev}} \exp\left(-\frac{eV}{E_0} \times \left(\frac{E_0}{k_{\mathrm{B}}T} - 1\right)\right), \tag{3.9}$$

with

$$j_{\mathrm{s,rev}} = \frac{A^*_{\mathrm{m}}\sqrt{\pi E_{00}(E_{\mathrm{B}} - eV\cosh^2(E_{00}/k_{\mathrm{B}}T))}}{k_{\mathrm{B}}T\cosh(E_{00}/k_{\mathrm{B}}T)} \times \exp\left(-\frac{E_{\mathrm{B}}}{E_0}\right). \tag{3.10}$$

Here the Richardson constants of the semiconductor A^*_{s} and the metal A^*_{m} must be distinguished. ξ_2 is the difference between conduction band edge and Fermi level of the bulk semiconductor. This quantity is negligible for reverse bias, as the band bending will be large compared to ξ_2. The characteristic energy E_{00} is defined by

$$E_{00} = \frac{e\hbar\sqrt{N_{\mathrm{D}}}}{2\sqrt{\epsilon_{\mathrm{s}} m^*}}, \tag{3.11}$$

and the constant E_0 by

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{k_{\mathrm{B}}T}\right). \tag{3.12}$$

3.1.2. Field-Effect Transistors

A field-effect transistor (FET) is a semiconductor device with three terminals, which are called source, drain, and gate. The conductivity of the channel between source and drain is controlled by the voltage at the gate contact, in the ideal case without power consumption. In a real transistor the gate capacitance makes a certain input power neccessary for switching the device, while the gate leakage current causes a permanent power consumption at the gate [44]. The control of the channel conductivity is based on the extension of a depletion layer, which is controlled by the gate voltage. The gate is either a Schottky-diode, a *pn*-junction or a metal-insulator-semiconductor diode. The resulting devices are called metal-semiconductor field-effect transistor (MESFET), junction field-effect transistor (JFET), and metal-insulator-semiconductor field-effect transistor (MISFET), respectively.

A MISFET uses an insulating layer and a metallic electrode to form the gate contact on the semiconductor channel. If the source and drain contacts are semiconducting with

opposite sign of carrier charge than in the channel, inversion must be induced before charge can flow through the channel. These devices are called "normally off", while transistors with ohmic source and drain contacts to the channel are called "normally on". For MISFETs with oxide insulators also the term MOSFET is used.

A MESFET has a metallic gate in direct contact to the channel to form a Schottky diode, while in a JFET the gate consists of a semiconductor with opposite majority carrier type. If the doping density of the JFET's gate material is significantly higher than the channel doping density, the current characteristic through the channel of both JFET and MESFET can be described by the same formalism. The following considerations are presented for n-type channels, as these were exclusively used within this work. However, the equations can be easily adjusted for p-type materials, when charges, charge carrier densities, and doping densities are exchanged accordingly.

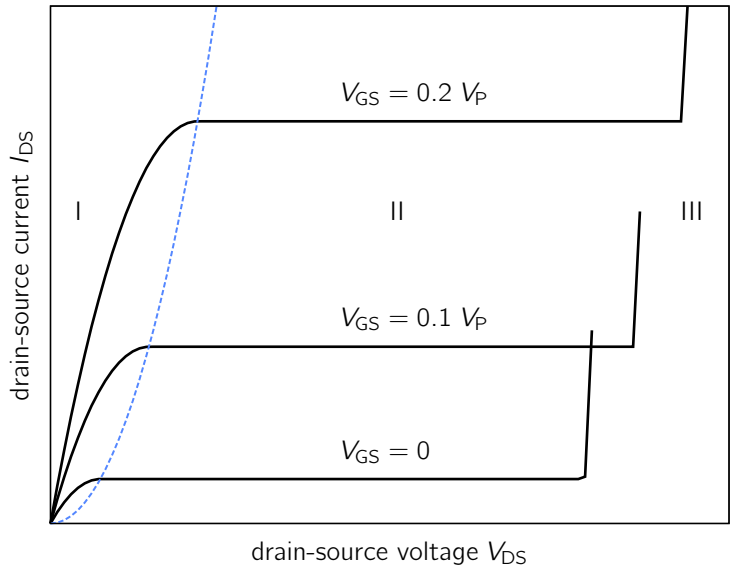

Figure 3.2.: Ideal output characteristics of a MESFET. Based on [45, 39].

Assuming a large gate length L compared to the channel thickness a and neglecting thermal effects, the depletion layer width w in dependence on the position x between source and drain can be calculated according to Eq. 3.1:

$$w(x) = \left[\frac{2\epsilon_s}{eN_D}\left(V_{bi} - V_{GS} + V(x)\right)\right]^{1/2}. \tag{3.13}$$

The depletion layer width at source ($x = 0$) and drain ($x = L$) is therefore given by

$$\begin{aligned} w(0) &= \left[\tfrac{2\epsilon_s}{eN_D}\left(V_{bi} - V_{GS}\right)\right]^{1/2}, \\ w(L) &= \left[\tfrac{2\epsilon_s}{eN_D}\left(V_{bi} - V_{GS} + V_{DS}\right)\right]^{1/2}. \end{aligned} \tag{3.14}$$

The width of the depletion layer $w(x)$ equals the channel width a for $V_{\mathrm{bi}} - V_{\mathrm{GS}} + V_{\mathrm{DS}} = V_{\mathrm{P}}$, with the pinch-off voltage V_{P} defined by

$$V_{\mathrm{P}} = \frac{ea^2 N_{\mathrm{D}}}{2\epsilon_{\mathrm{s}}}. \tag{3.15}$$

The pinch-off voltage denotes the potential difference between the top of the barrier and the substrate/channel interface, when the channel is totally depleted. Assuming $V_{\mathrm{DS}} > 0$, in order to deplete the entire channel the threshold voltage, or turn-on voltage,

$$V_{\mathrm{T}} = V_{\mathrm{bi}} - V_{\mathrm{P}} \tag{3.16}$$

must be applied at the gate. One should be aware, that V_{P} is sometimes defined equally to V_{T} (e.g. Sedra and Smith [46]), while both denote different quantities in this work. The current flowing from source to drain can be calculated by integrating the channel conductance along x, as derived first by Shockley [45]. It should be noted, that current conservation along the channel is assumed, which implies a negligible gate current compared to the source-drain current. For both JFET and MESFET this assumption is reasonable for typical operating conditions, but clearly violated for sufficently high gate voltages.

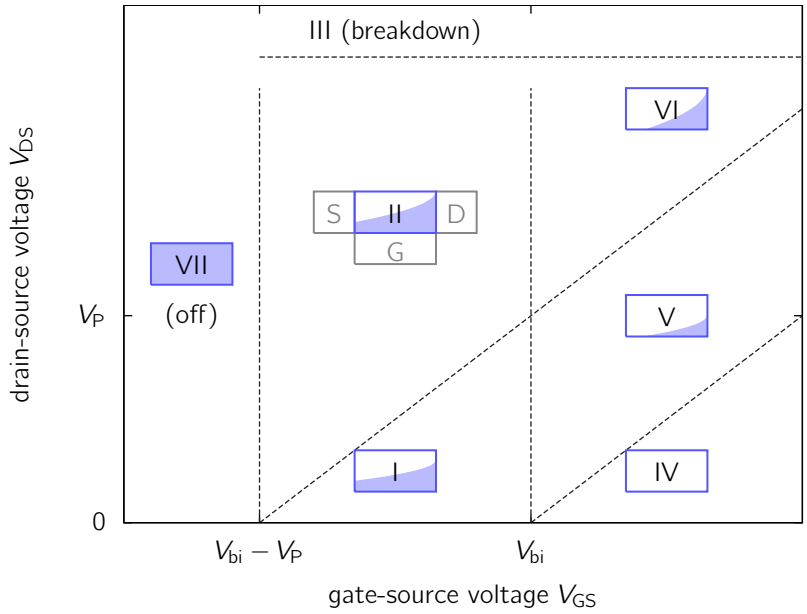

Figure 3.3.: Different regimes for the current-voltage characteristics of a MESFET. I-III correspond to the numbers in Fig. 3.2. The pictograms show schematically the expansion of the depletion layer.

The current is then given by

$$I_{\mathrm{D}} = I_{\mathrm{P}} \left[\frac{3V_{\mathrm{DS}}}{V_{\mathrm{P}}} - 2\left(\frac{V_{\mathrm{bi}} - V_{\mathrm{GS}} + V_{\mathrm{DS}}}{V_{\mathrm{P}}} \right)^{3/2} + 2\left(\frac{V_{\mathrm{bi}} - V_{\mathrm{GS}}}{V_{\mathrm{P}}} \right)^{3/2} \right] \tag{3.17}$$

for the voltage range designated in Fig. 3.3 with the roman number I. The saturation current

$$I_{\mathrm{P}} = \frac{e^2 \mu_{\mathrm{n}} N_{\mathrm{D}}^2 W a^3}{6 \epsilon_{\mathrm{s}} L} \tag{3.18}$$

is a constant depending on material and geometrical properties. When the depletion layer near the drain contact reaches the semiconductor-substrate interface, the current saturates and becomes independent of V_{DS}. This corresponds to case II in Fig. 3.3, given by $V_{\mathrm{bi}} - V_{\mathrm{GS}} + V_{\mathrm{DS}} \geq V_{\mathrm{P}}$. The channel current in saturation is

$$I_{\mathrm{D,sat}} = I_{\mathrm{P}} \left[1 - 3 \frac{V_{\mathrm{bi}} - V_{\mathrm{GS}}}{V_{\mathrm{P}}} + 2 \left(\frac{V_{\mathrm{bi}} - V_{\mathrm{GS}}}{V_{\mathrm{P}}} \right)^{3/2} \right]. \tag{3.19}$$

For sufficiently high source-drain voltage the device will break down, which will result in an uncontrolled increase of the current and probably irreversible damage of the device. Fig. 3.2 shows the output characteristics which results from Eqns. 3.17 and 3.19. For $V_{\mathrm{GS}} = V_{\mathrm{bi}} - V_{\mathrm{P}}$ Eqn. 3.19 equals zero, as the channel is completely depleted and no current can flow. $V_{\mathrm{GS}} \leq V_{\mathrm{bi}} - V_{\mathrm{P}}$ is called the OFF-regime, designated by VII in Fig. 3.3.

Especially in electrial engineering simplified equations are in use, to which empirical terms are added in order to describe real devices. For the saturation regime, Eqn. 3.19 can be expanded around $V_{\mathrm{GS}} = V_{\mathrm{T}}$, which yields

$$I_{\mathrm{D,sat}} \approx \frac{3 I_{\mathrm{P}}}{4 V_{\mathrm{P}}^2} (V_{\mathrm{GS}} - V_{\mathrm{T}})^2. \tag{3.20}$$

This equation is found in many electrical engineering textbooks as starting point for more involved device models [46, 44].

When V_{GS} exceeds V_{bi}, the depletion layer at the source contact vanishes and Eqns. 3.17 and 3.19 are not defined. Thus, from source to the location in the channel where a potential of $V(x) = V_{\mathrm{GS}} - V_{\mathrm{bi}}$ is reached, ohmic conduction occurs. The rest of the channel forms a transistor with reduced gate length, gate voltage and source-drain voltage. Using current conservation for the charge transport through these two regions the source-drain current can be calculated, giving

$$I_{\mathrm{D,V}} = I_{\mathrm{P}} \left[3 \frac{V_{\mathrm{bi}} - V_{\mathrm{GS}} + V_{\mathrm{DS}}}{V_{\mathrm{P}}} - 2 \left(\frac{V_{\mathrm{bi}} - V_{\mathrm{GS}} + V_{\mathrm{DS}}}{V_{\mathrm{P}}} \right)^{3/2} \right] + \frac{e \mu_{\mathrm{n}} N_{\mathrm{D}} W a}{L} (V_{\mathrm{GS}} - V_{\mathrm{bi}}) \tag{3.21}$$

for the non-saturated case (region V in Fig. 3.3), and

$$I_{\mathrm{D,VI}} = I_{\mathrm{P}} + \frac{e \mu_{\mathrm{n}} N_{\mathrm{D}} W a}{L} (V_{\mathrm{GS}} - V_{\mathrm{bi}}) \tag{3.22}$$

for saturation (region VI in Fig. 3.3). When the depletion layer vanishes completely, the channel can be treated as an simple ohmic conductor:

$$I_{\mathrm{D,IV}} = \frac{e \mu_{\mathrm{n}} N_{\mathrm{D}} W a}{L} V_{\mathrm{DS}}. \tag{3.23}$$

The forward transconductance g_m of the transistor, often called only transconductance, is in the linear regime given by

$$g_\mathrm{m} = \frac{\partial I_\mathrm{D}}{\partial V_\mathrm{GS}} = g_\mathrm{max} \left[\left(\frac{V_\mathrm{bi} - V_\mathrm{GS}}{V_\mathrm{P}} \right)^{1/2} - \left(\frac{V_\mathrm{bi} - V_\mathrm{GS} + V_\mathrm{DS}}{V_\mathrm{P}} \right)^{1/2} \right] \tag{3.24}$$

and in saturation by

$$g_\mathrm{m,sat} = \frac{\partial I_\mathrm{D,sat}}{\partial V_\mathrm{GS}} = g_\mathrm{max} \left[1 - \left(\frac{V_\mathrm{bi} - V_\mathrm{GS}}{V_\mathrm{P}} \right)^{1/2} \right], \tag{3.25}$$

with

$$g_\mathrm{max} = \frac{3 I_\mathrm{P}}{V_\mathrm{P}} = \frac{e N_\mathrm{D} a \mu W}{L}. \tag{3.26}$$

g_max is the theoretical maximum of the transconductance and equal to the conductance of the channel. If the maximum transconductance of a measured FET characteristic is compared to g_max, a value for μ can be determined when N_D is known. This value is called field-effect mobility μ_FE. Often the theoretical maximum of the transconductance is not reached, due to the influence of the gate current at positive V_GS. Then, μ_FE underestimates the actual carrier mobility μ.

The reason for the reduced transconductance in the presence of high gate current is depicted in Fig. 3.4. For small gate current densities j_G, the current along the channel can be considered constant. When the contribution of j_G to the channel current becomes comparable to the drain current, the potential distribution in the channel will become more flat near drain and more steep near source, as the additional current is connected to an additional potential drop by Ohm's law. This reduces I_D and eventually reverses the current flow at the drain contact. In this case, a potential barrier exists in the channel, and no current can flow between drain and source. In the FET's output characteristic, this leads to a zero-crossing of the drain current for high gate voltages.

For the ideal MESFET characteristics derived above, at gate voltages below V_T the channel is completly depleted of charge carriers, and no current flow is possible. However, the electron quasi-Fermi level F_n extends into the depletion layer from both contacts, leading to a non-zero charge carrier density given by

$$n \approx N_\mathrm{C} \exp\left(\frac{F_\mathrm{n} - E_\mathrm{C}}{k_\mathrm{B} T} \right) \tag{3.27}$$

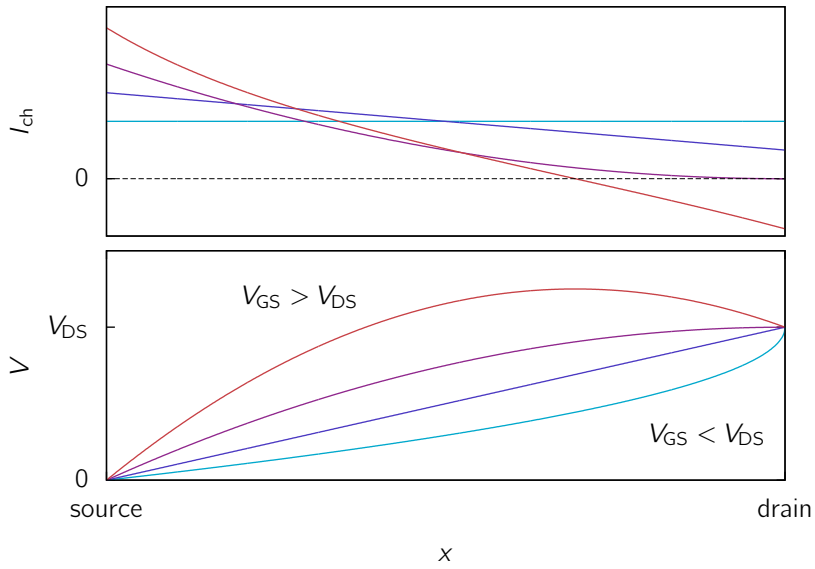

Figure 3.4.: Schematic dependency of channel current $I_{ch}(x)$ and channel potential $V(x)$ on the gate voltage. I_{ch} is approximately constant for small gate currents (blue line), but for $V_{GS} > V_{DS}$ the gate current dominates the potential distribution in the channel (red line).

in the Boltzmann approximation. Underneath the gate the band edges are at constant energy in the OFF-regime. Due to the different voltage levels at source and drain, the quasi-Fermi level at source is closer to E_C than at drain, which causes a gradient of the free carrier concentration n in the depletion layer. This leads to a diffusion current with expontential dependence on V_{GS}, which is called subthreshold current. Liang *et al.* [47] give the resulting drain current as

$$I_{D,ss} = \beta \frac{\epsilon_s Z}{a L_{eff}} \frac{k_B T}{e} D_n \exp\left[\frac{e}{k_B T}(V_{GS} - V_T)\right] \times \left[1 - \exp\left(-\frac{e}{k_B T} V_{DS}\right)\right], \tag{3.28}$$

where D_n is the electron diffusion constant and β a constant due to mathematical approximations. β satisfies $2 \geq \beta \geq 1$ and is usually close to unity. L_{eff} is the effective gate length, smaller than L due to edge effects close to the contacts, and given by

$$L_{eff} = L - \sqrt{\frac{2\epsilon_s}{e N_D}} \left[(V_{DS} + V_T - V_{GS})^{1/2} + (V_T - V_{GS})^{1/2})\right]. \tag{3.29}$$

The slope of the subthreshold current provides a lower limit for the voltage, that is

necessary to switch the device between OFF- and ON-state. It is usually characterized by the subthreshold swing S, which is defined as the inverse of the slope of the logarithmic transfer characteristic. Its theoretical mimimum can be calculated from Eqn. 3.28, and is given by

$$S_{\mathrm{min}} = \left(\frac{\mathrm{d} \log_{10}(I_{\mathrm{D,ss}})}{\mathrm{d}V_{\mathrm{GS}}} \right)^{-1} = \ln(10) \frac{k_{\mathrm{B}} T}{e}. \tag{3.30}$$

At room temperature this yields $S_{\mathrm{min}} \approx 60$ mV/dec.

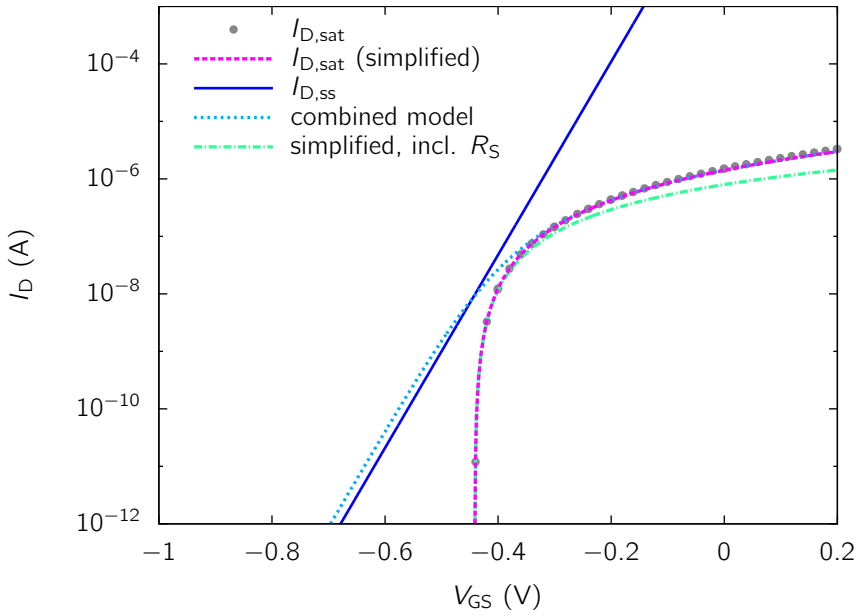

Figure 3.5.: Calculated transfer characteristic of a MESFET, using $V_{\mathrm{DS}} = 2$ V and FET parameters typical for devices in this work. $I_{\mathrm{D,sat}}$ is shown according to Eqn. 3.19 and for the simplified Eqn. 3.20. The subthreshold current as described by Eqn. 3.28 is shown for $\beta = 1$. The combined solution is according to Eqn. 3.32. The saturation current including the series resistance is given by Eqn. 3.33.

To obtain a continuous model including both saturation current and subthreshold current, the voltage term $(V_{\mathrm{GS}} - V_{\mathrm{T}})$ in the simplified equation for the saturation current (Eqn. 3.20) can be replaced by

$$V_{\mathrm{GS}} - V_{\mathrm{T}} = \frac{2 k_{\mathrm{B}} T}{e} \ln \left(1 + \exp \left(\frac{e(V'_{\mathrm{GS}} - V_{\mathrm{T}})}{2 k_{\mathrm{B}} T} \right) \right) \tag{3.31}$$

as proposed by Parker and Skellern [48]. This results in the equation

$$I_{\mathrm{D,com}} = \frac{3I_{\mathrm{P}}}{4V_{\mathrm{P}}^2}\left[\frac{2k_{\mathrm{B}}T}{e}\ln\left(1+\exp\left(\frac{e(V_{\mathrm{GS}}-V_{\mathrm{T}})}{2k_{\mathrm{B}}T}\right)\right)\right]^2, \tag{3.32}$$

using the assumptions $L_{\mathrm{eff}} \approx L$ and $V_{\mathrm{DS}} \gg k_{\mathrm{B}}T/e$. The diffusion constant was calculated with the Einstein relation $D_{\mathrm{q}} = \mu_{\mathrm{q}}k_{\mathrm{B}}T/q$. As illustrated in Fig. 3.5, the combined equation connects Eqn. 3.20 and Eqn. 3.28 smoothly. The subthreshold current has a slight offset, as the combined solution can only be formulated for $\beta = 2$. This is because Eqn. 3.32 has a common prefactor for both subtreshold and ON-regime. When the equation is adjusted for $V_{\mathrm{GS}} \gg V_{\mathrm{T}}$, the factor $\beta = 2$ arises automatically for $V_{\mathrm{GS}} \ll V_{\mathrm{T}}$. Although to the best knowledge of the author the formalism for the combined solution is rather empirical, Eqn. 3.32 can be seen as physical model, as both limits are backed by equations derived from basic physical concepts, and no empirical parameters are added.

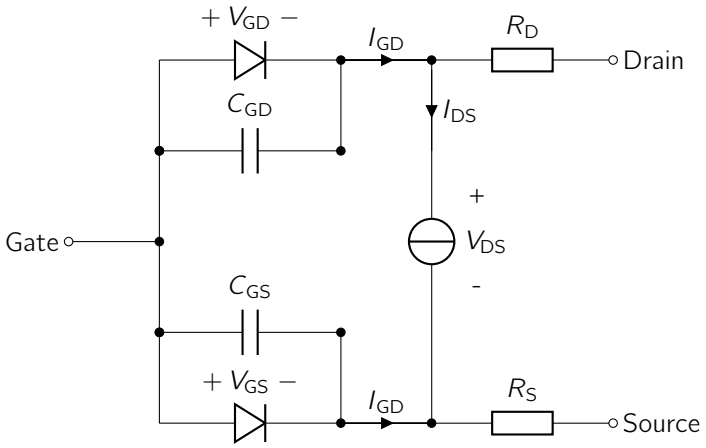

Figure 3.6.: Equivalent circuit for a MESFET model as described in [48].

So far only the channel current from drain to source has been discussed, under the assumption that source and drain voltage are applied directly next to the gate. In a real device, between the ohmic contacts and the channel the series resistances R_{S} and R_{D} must be considered. For thin film devices, these consist usually of the channel parts, that are not covered by the gate. When the channel conductivity is known, the resistances can be directly calculated. Fig. 3.6 shows an equivalent circuit, that can be applied for the description of real devices. The current source in the circuit represents the channel current as described previously. The voltage drop across R_{S} and R_{D} reduces the effective V_{DS}, and the voltage drop across R_{S} reduces V_{GS}. These effects must be included especially for high gate voltages, when the transconductance is close to the

maximum. Otherwise the model would overestimate the channel current. The simplified equation for the saturation current, Eqn. 3.20, can be solved analytically when including R_S, which yields

$$I_{D,sat} = \frac{V_{GS} - V_T}{R_S} - \frac{2V_P^2}{3I_P R_S^2}\left[1 - \sqrt{\frac{3I_P R_S}{V_P^2}(V_{GS} - V_T) + 1}\right]. \tag{3.33}$$

This solution is depicted in Fig. 3.5. For the other equations which describe the FET characteristics in this section, numerical methods must be applied in order to include the series resistances.

The circuit model presented in Fig. 3.6 makes it possible to describe the influence of gate capacitance and leakage current on the FET characteristics. The gate can be described more accurately, when more than two diodes are considered, that attach at different positions of the channel. For this, the potential distribution in the channel must be calculated, which can be done using Eqn. 3.13 and the condition for current conservation in the channel.

The equations summarized in this section have been implemented in a MATLAB script, allowing the calculation of static FET characteristics for arbitrary operation voltages, if necessary under consideration of gate current, series resistances and subthreshold current. This script was used for several calculations presented in the following sections, where the complexity exceeded the evaluation of simple analytical expressions. The source code is listed in Appendix D.

3.1.3. Simple Inverter

A simple inverter is a device consisting of two FETs in series, as depicted in the inset of Fig. 3.7. The gate voltage of the input FET is the input voltage V_{in}. The voltage V_{GS} of the load FET is fixed at zero by a short between source and gate. At the drain of the load FET the constant voltage V_{DD} is applied. Drain of the input FET and source of the load FET are connected and the potential at the connection is called output voltage V_{out}, which can have values between 0 V and V_{DD}. At negative input voltages the channel of the input FET is depleted and has a large resistance compared to the load FET, resulting in $V_{out} \approx V_{DD}$. At positive V_{in} the depletion layer in the input channel vanishes and V_{out} is close to zero. Thus, the device gives a high output for a low input voltage and vice versa. In contrast to a full inverter one cannot find two voltage levels which are exchanged by the device, as a positive input voltage always gives an output close to zero, which is an undefined input level. More details about inverters can be found in [46].

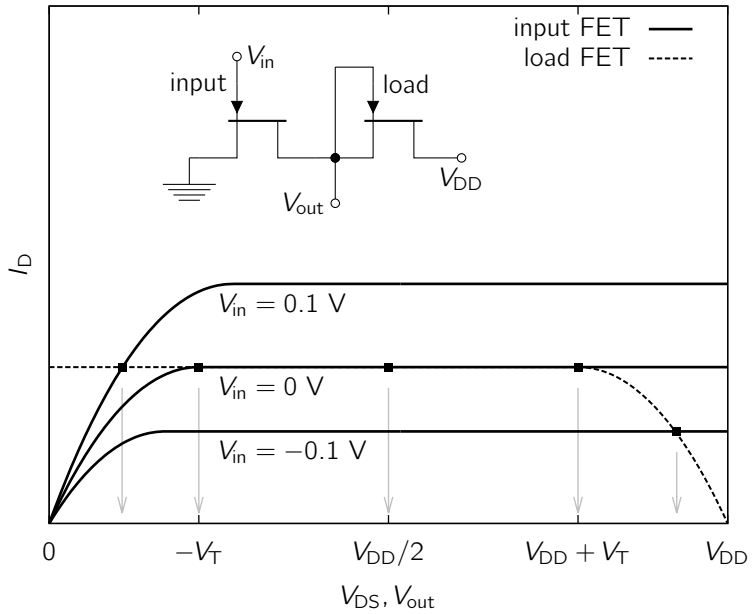

Figure 3.7.: Construction of the inverter characteristic from the FET output characteristics. The inset depicts the build-up of a simple inverter from two FETs.

The characteristic of the inverter is given by $V_{\text{out}} = V_{\text{DS}}^{\text{input}} = V_{\text{DD}} - V_{\text{DS}}^{\text{load}}$ and the current conservation equation

$$I_{\text{D}}^{\text{input}}(V_{\text{in}}, V_{\text{DS}}^{\text{input}}) = I_{\text{D}}^{\text{load}}(0, V_{\text{DS}}^{\text{load}}), \tag{3.34}$$

when gate currents are neglected. Fig. 3.7 illustrates, how the relation between V_{in} and V_{out} can be constructed geometrically. The output characteristic of the input FET is plotted as usual, but the characteristic of the load FET, fixed at $V_{\text{GS}} = 0$ V, is drawn mirrored at $V_{\text{DS}} = V_{\text{DD}}/2$. This way, all crossings between the curves of input and load FETs fullfill the conditions for voltage and current stated above. The output voltage is equal to the V_{DS} value where the crossing occurs, depicted by the grey arrows in Fig. 3.7. It can be seen, that for $V_{\text{in}} = 0$ V the solution is not unique. Thus, a discontinuity occurs between $V_{\text{out}} = -V_{\text{T}}$ and $V_{\text{DD}} + V_{\text{T}}$ ($V_{\text{T}} < 0$ by definition!). By numerical interpolation of the line crossings for FET characteristics calculated according to the FET model presented in the previous section, the inverter characteristic shown in Fig. 3.8(a) has been calculated. The gain g of the device is defined as

$$g = -\frac{\mathrm{d}V_{\text{out}}}{\mathrm{d}V_{\text{in}}} \tag{3.35}$$

and shown in Fig. 3.8(b). For small input signals around $V_{\text{in}} = 0$ V a high amplification of the signal can be obtained, although with strong nonlinearity. This makes the simple inverter interesting for sensor applications, where more complicated amplifier circuits are not feasable due to area limitations.

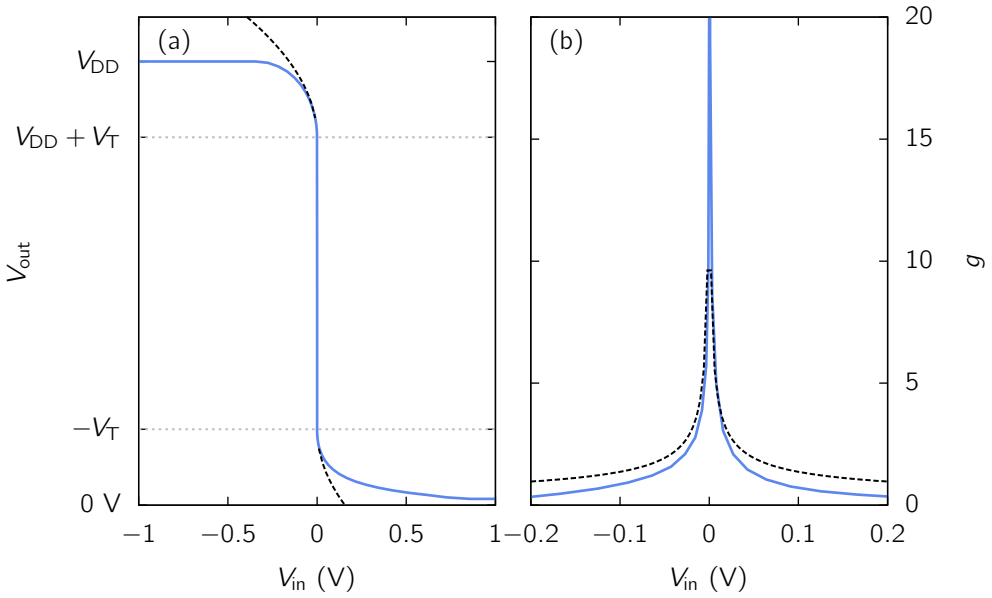

Figure 3.8.: Ideal inverter characteristic, numerically interpolated from calculated FET characteristics. The dashed lines show the analytical expressions obtained by Taylor expansion.

Although an analytical solutions is not accessible for the complete inverter characteristics, Taylor expansion can be used to solve Eqn. 3.34 in vicinity to $V_{\mathrm{in}} = 0$ V. This was done for this work, in order to assess the amplification properties of simple inverters in dependence on the transistor properties. Measurements are suitable to evaluate certain device configurations, but without theoretical backing it is challenging to analyze which transistor or material parameters are decisive for the inverter performance. For $V_{\mathrm{in}} < 0$, the expansion was performed around $V_{\mathrm{in}} = 0$ V up to linear order and around $V_{\mathrm{out}} = V_{\mathrm{DD}} + V_{\mathrm{T}}$ up to quadratic order. This yields

$$V_{\mathrm{out},-} = V_{\mathrm{DD}} + V_{\mathrm{T}} + \sqrt{-4V_{\mathrm{P}}(1 - \sqrt{V_{\mathrm{bi}}/V_{\mathrm{P}}})V_{\mathrm{in}}}. \tag{3.36}$$

A similar expansion was used for $V_{\mathrm{in}} > 0$, but around $V_{\mathrm{out}} = -V_{\mathrm{T}}$, resulting in

$$V_{\mathrm{out},+} = -V_{\mathrm{T}} - \sqrt{4V_{\mathrm{P}}(1 - \sqrt{V_{\mathrm{bi}}/V_{\mathrm{P}}})V_{\mathrm{in}}}. \tag{3.37}$$

The gain is given by

$$g = \sqrt{\frac{V_{\mathrm{P}}(1 - \sqrt{V_{\mathrm{bi}}/V_{\mathrm{P}}})}{|V_{\mathrm{in}}|}}. \tag{3.38}$$

These expressions are depicted in Fig. 3.8 by dashed black lines. The curve shape is indeed reproduced close to $V_{\mathrm{in}} = 0$ V, but quantitatively well described only for input voltages in a range of a few 10 mV.

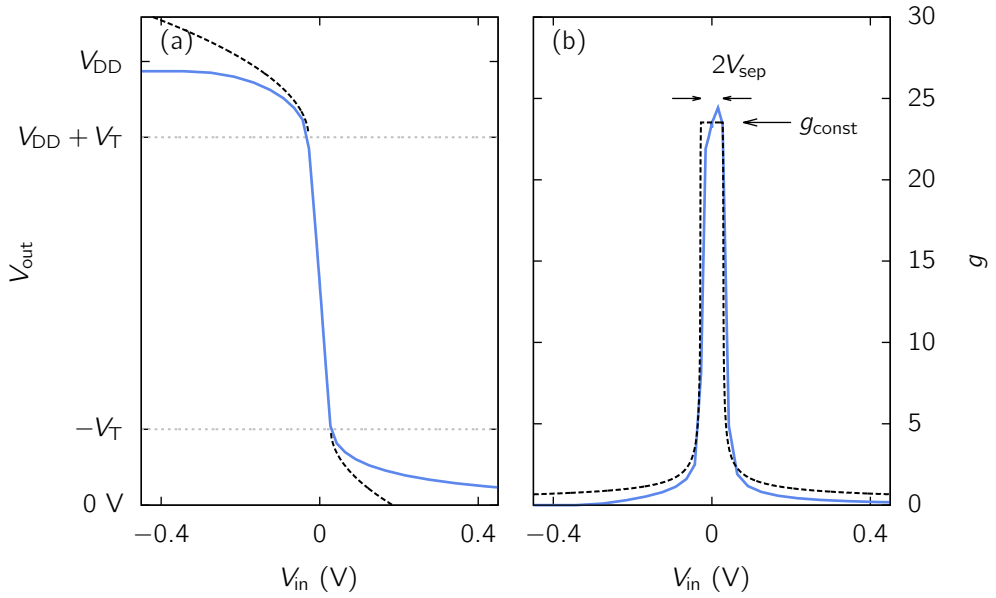

Figure 3.9.: Calculated inverter characteristic for FETs with non-constant saturation current ($\alpha = 0.01 I_P$ A^{-1}V^{-1}). The dashed lines show the analytical expressions obtained by Taylor expansion.

For a non-ideal FET the saturation current is not constant, but depends on V_{DS}. In a simple way this can be expressed by $I^{ni}_{D,sat}(V_{GS}, V_{DS}) = I_{D,sat}(V_{GS}) + \alpha(V_{DS} + V_T)$, where $I_{D,sat}$ is the ideal and $I^{ni}_{D,sat}$ the non-ideal saturation current. The transfer characteristic of an inverter built from such transistors will have a finite slope at $V_{in} = 0$ V. The characteristic is again defined by the current conservation equation, now stating

$$I^{input}_{D,sat}(V_{in}) + \alpha(V_{out} + V_T) = I^{load}_{D,sat}(0) + \alpha(V_{DD} - V_{out} + V_T) \tag{3.39}$$

for $-V_T < V_{out} < V_{DD} + V_T$, the range where the gain is maximal. Taylor expansion around $V_{in} = 0$ V yields

$$V_{out} = \frac{V_{DD}}{2} - g_{const} V_{in}, \tag{3.40}$$

with constant gain

$$g_{const} = \frac{3 I_P}{2 \alpha V_P} (1 - \sqrt{V_{bi}/V_P}). \tag{3.41}$$

The numerical calculation presented in Fig. 3.9 shows, that the gain is actually increasing slightly with V_{in}, but is well approximated by the constant value g_{const}. The conditions $V_{out} = -V_T$ and $V_{out} = V_{DD} + V_T$ mark the transition between the range with constant gain and gain decreasing proportional to $|V_{in}|^{-1/2}$, as given by Eqn. 3.38 for the ideal case. This transition occurs at the input voltages

$$\pm V_{sep} = \pm \frac{\alpha V_P}{3 I_P} \frac{V_{DD} + 2 V_T}{1 - \sqrt{V_{bi}/V_P}}. \tag{3.42}$$

The gain outside of this range is then given by

$$g_{\mathrm{sep}} = \sqrt{\frac{V_{\mathrm{P}}(1-\sqrt{V_{\mathrm{bi}}/V_{\mathrm{P}}})}{|V_{\mathrm{in}}| - V_{\mathrm{sep}}}} \tag{3.43}$$

in the expansion around $V_{\mathrm{in}} = 0$ V. Fig. 3.9 demonstrates, that for V_{in} close to zero the approximations follow the numerically calculated characteristics well, providing a method to derive the maximal achievable amplification of simple inverters from FET properties. Notably, the non-ideality described by the parameter α enhances the usability of the device as an amplifier, as the divergence in the gain at zero input voltage is replaced by a region with nearly constant gain. However, while increasing α increases the voltage range $2V_{\mathrm{sep}}$, in which the constant gain occurs, the absolute value g_{const} of the gain decreases.

3.2. Thin Films

3.2.1. Structural Properties and Chemical Composition

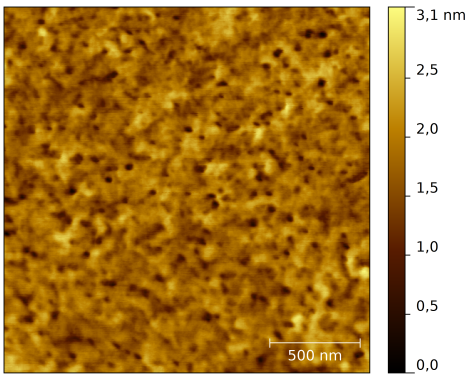

Figure 3.10.: AFM topography image of a ZnO thin film with thickness of about 20 nm. The sample was grown by PLD at 650°C and 0.02 mbar oxygen pressure, using a ZnO target with 0.25wt-% MgO. The root mean square roughness was 0.3 nm.

ZnO thin films have been studied extensively, regarding their electrical and optical properties and for multiple deposition methods. On a-plane sapphire substrates thin films deposited by PLD grow with the c-axis perpendicular to the surface. The films are crytalline but textured, which means that rotational domains with different in-plane orientations exist. Structural analyses including XRD spectra and TEM cross sections of PLD grown ZnO films can be found in [32]. FETs based on PLD grown thin films

have been reported on sapphire [49] and glass substrates [50]. While FETs on glass exhibit channel mobilities around 1 cm^2/Vs, mobilities on sapphire can exceed 20 cm^2/Vs. Thus, solely sapphire was chosen as substrate for this work. Frenzel *et al.* [28] reported, that MESFET gates on pure ZnO channels degraded during 60 days after fabrication, before a stable state was reached. The introduction of a small fraction of Mg (0.3%) into the channel decreased the mobility to about 10 cm^2/Vs, but resulted in stable contacts during a period of 250 days or more. For the thin films grown for this work a ZnO target with 0.25wt-% MgO was used. An AFM topography map of a 20 nm thick layer on a-sapphire is shown in Fig. 3.10. The roughness, as determined by the root mean square value, was well below 1 nm.

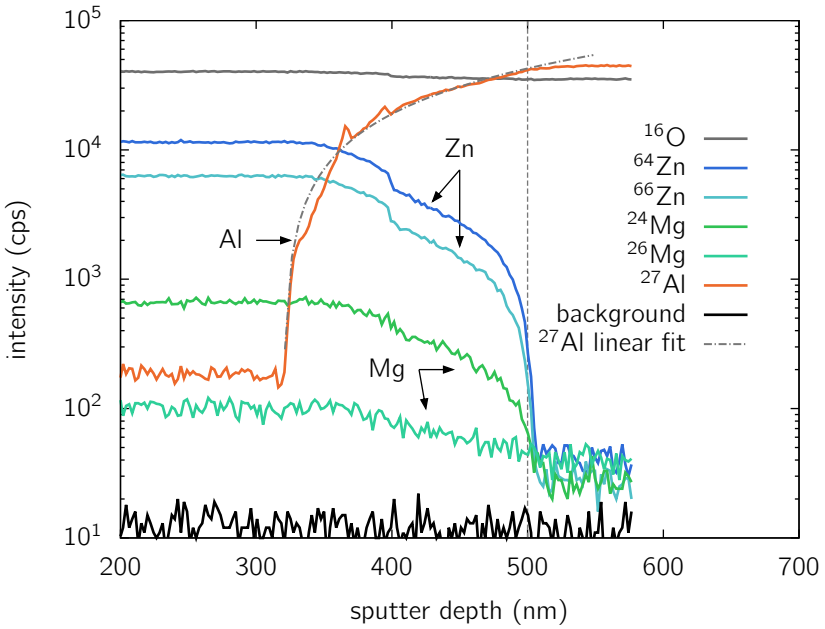

Figure 3.11.: SNMS depth profile of a 500 nm thick ZnO thin film on a-plane sapphire (Al_2O_3). The PLD target contained 0.25wt-% MgO. The intensity is given in counts per second (cps) and is not corrected for the varying sensitivity of the measurement process to different isotopes. The sputter depth refers to the distance from the film surface. The vertical dashed line marks the nominal position of the thin film/substrate interface.

Usually published results on transport properties and defects of ZnO thin film are either based on single crystals or on layers with a thickness of several hundred nanometers up to few microns [51]. For the fabrication of thin film transistors channel thicknesses from few nanometes up to about 100 nm thickness have been reported (compare e.g. [52, 49, 53, 54, 55]). Especially on sapphire substrates the thickness is a crucial parameter for the electrical properties, as the carrier density is determined by Al diffusion from the substrate during the deposition process (see e.g. [33]). At deposition temperatures around 650°C the indiffusion of aluminum from the substrate into the thin film is in-

evitable. The depth resolved chemical composition of a thin film can be measured by secondary neutrals mass spectrometry (SNMS). Fig. 3.11 shows the intensity signals for several isotopes recorded with a SPECS INA-3 SNMS system. The examined thin film on a-sapphire was PLD grown with 0.25wt-% MgO in the target and had a thickness of 500 nm. The substrate consists of pure Al_2O_3 within the measurement accuracy, but also the thin film contains a relatively high fraction of Al. The Al content decreases nearly linearly for about 180 nm from the thin film/substrate interface and is in the remaining film constant at about 1/200 of the concentration in the substrate. As a linear distribution of Al in the thin film due to diffusion is very improbable, the transition between 320 nm and 500 nm depth is most likely due to a nonuniform depth during sputtering. This means, that a transient in the Al content of the film should be visible for depths lower than 320 nm. However, the Al content is constant in this region, indicating that Al is distributed uniformly in the thin film. Thus, also for the thin films used for devices a uniform doping density can be assumed.

3.2.2. Hall Effect Measurements

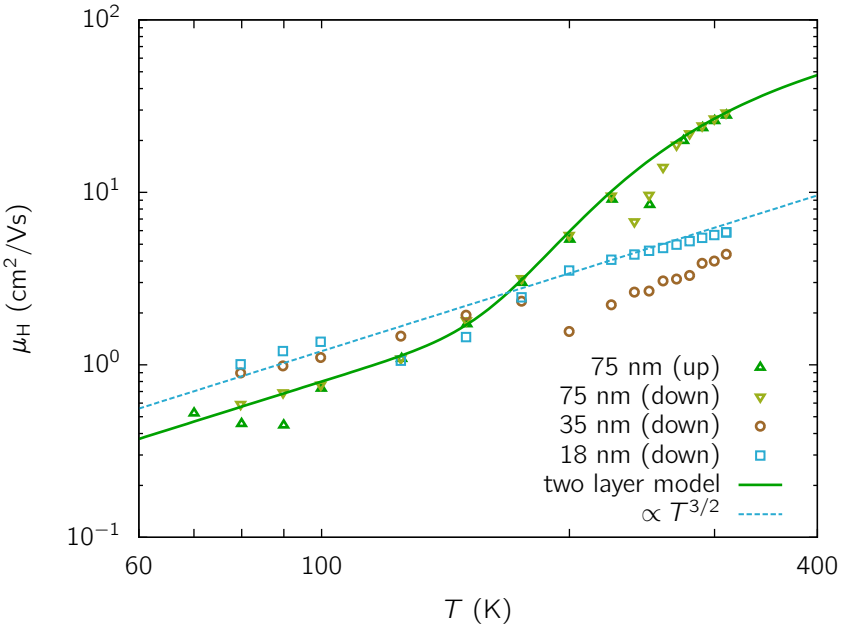

Figure 3.12.: Hall mobility for ZnO thin films with different thicknesses. The measurement results are depicted by the symbols, the lines are fits to the data. For the thickest layer two measurement series are shown, measured from cold to hot (up) and from hot to cold (down).

The electrical properties of ZnO thin films have been examined by Hall effect measurements in van der Pauw geometry. To clarify the prevalent conduction mechanism, these

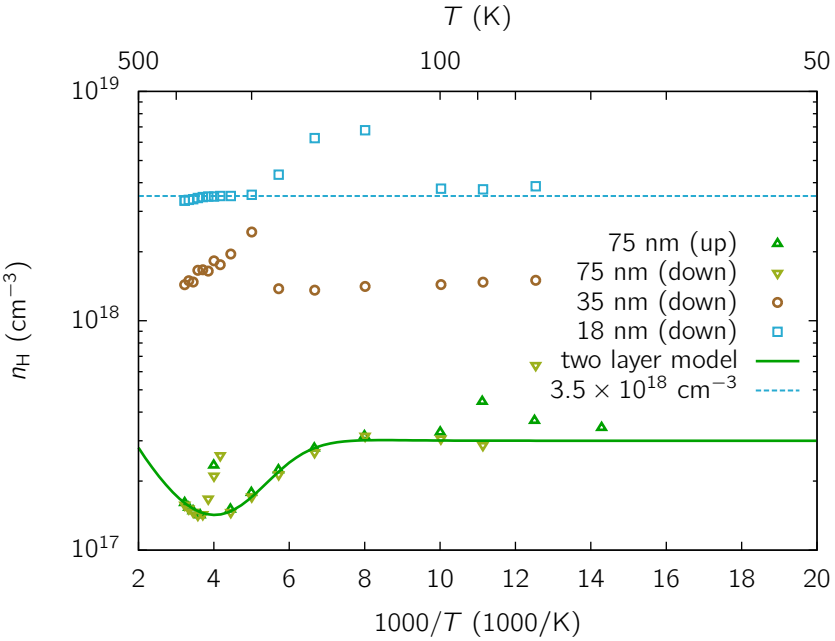

Figure 3.13.: Hall charge carrier density for ZnO thin films with different thicknesses. The measurement results are depicted by the symbols, the lines are fits to the data. For the thickest layer two measurement series are shown, measured from cold to hot (up) and from hot to cold (down).

measurements were performed temperature dependently. The films were n-type and their resistance decreased monotonously with decreasing temperature. The determined Hall mobility μ_H and charge carrier density n_H for three films with thicknesses a between 18 nm and 75 nm are depicted in Fig. 3.12 and Fig. 3.13, respectively. The displayed temperature range is from 70 K to 330 K. Lower temperatures down to 40 K have been applied, but did not yield reliable results due to the very high sample resistances at these temperatures.

For all samples the otherwise monotonous μ_H is interrupted by a dent, which is accompanied by a peak in n_H at the same temperature (∼250 K for 75 nm, ∼200 K for 35 nm, ∼125 K for 18 nm). The respective temperature and also the broadening of the peaks shift with the thickness, but no correlation to another quantity like the applied current could be found, which could explain this as a measurement artifact. By repeating several measurements it was verified, that no random disturbance is responsible. To illustrate the reproducibility, two measurement series for 75 nm thickness are shown in Fig. 3.12 and Fig. 3.13. Peaks in μ_H as well as dents n_H can be reproduced when using multi-layer models to describe the measured quantities. However, no parameters were found to describe the simultaneous behavior observed here. In the following, the overall trend of the curves is evaluated, ignoring this feature. Not because of its insignificance, but because so far no explanation was found.

For the thinnest layers the carrier density is nearly constant. This is typical for a degenerate semiconductor, with E_F close to or within an energy band. The conduction band edge density calculated for ZnO at room temperature is

$$N_{C,ZnO} = 2\left(\frac{m_e^* k_B T}{2\pi\hbar^2}\right)^{3/2} = 3.5 \times 10^{18}\ \mathrm{cm}^{-3} \tag{3.44}$$

For $N_D > N_C$ the Fermi energy is located within the conduction band. This condition is satisfied for the thinnest layer. At very high impurity densities, the impurity wavefunctions will overlap and an impurity band forms. An estimate for the critical density N_c is given by

$$\frac{4}{3}\pi(2\epsilon_r \frac{m_0}{m_e^*} a_B)^3 = \frac{1}{N_c}. \tag{3.45}$$

It is based on the condition, that the distance between the randomly distributed impurities is similar to twice their Bohr radius. For ZnO this evaluates to $N_c = 7.4\times10^{18}$ cm^{-3}. n_H measured on ZnO thin films for this work was always below that value, but up to 6×10^{18} cm^{-3} for $a \approx 15$ nm. If a certain amount of compensation is present, the Al donor density may indeed be high enough to form an impurity band. The mobility for $a = 18$ nm is dependent on $T^{3/2}$ over the displayed temperature range. This indicates, that ionized impurity scattering as described by Conwell and Weisskopf [56] is the dominant scattering mechanism for this sample in the temperature range investigated. As discussed by Chattopadhyay and Queisser [57], the validity of this approach is questionable for high doping densities, where the impurities form rather a smooth energy landscape instead of individual scattering centers. A strong influence of impurities and grain boundaries on the mobility is nevertheless probable, due to the structural properties of this thin films.

The thickest film with $a = 75$ nm exhibits a T-dependency in both μ_H and n_H, which cannot be described by a single band or layer of charge carriers. This could either mean a model with seperate layers, that contribute differently to the total sheet conductivity, or different species of carriers in the same layer. Both cases are described by the same formalism, for two carrier species given by [58]

$$n_H = \frac{(\mu_1 n_1 + \mu_2 n_2)^2}{\mu_1^2 n_1 + \mu_2^2 n_2}, \tag{3.46}$$

$$\mu_H = \frac{\mu_1^2 n_1 + \mu_2^2 n_2}{\mu_1 n_1 + \mu_2 n_2}. \tag{3.47}$$

For the fit shown in Fig. 3.12 and Fig. 3.13 two carrier bands within the total layer thickness a were assumed. This does not limit the generality, as the carrier density n_i of species i can be easily transformed to a reduced layer thickness a_i using $n_{i,\mathrm{red}} = n_i a/a_i$. For one carrier species, a constant carrier density and a mobility with $T^{3/2}$ dependency was chosen. This is in agreement with the formalism used by Look [59] to describe the degenerate surface conduction layer of ZnO single crystals, under the assumption that ionized impurity scattering is the dominant scattering mechanism. The second carrier density was described by a Boltzmann term

$$n = N_\mathrm{D} \exp\left(-\frac{E_\mathrm{D}^\mathrm{b}}{k_\mathrm{B}T}\right). \tag{3.48}$$

Such a term is valid, when $k_\mathrm{B}T \ll E_\mathrm{D}^\mathrm{b}$ and the Fermi energy E_F is fixed close to the conduction band minimum E_C, giving $E_\mathrm{D}^\mathrm{b} = E_\mathrm{C} - E_\mathrm{D} \approx E_\mathrm{F} - E_\mathrm{D}$. For high temperatures the mobility for $a = 75$ nm has no $T^{3/2}$ dependency, but can be well described by grain-boundary scattering according to [60], given by

$$\mu_\mathrm{eff} = qL_\mathrm{G}\left(\frac{1}{2\pi m_\mathrm{e}^* k_\mathrm{B}T}\right)^{1/2} \exp\left(-\frac{E_\mathrm{B}}{k_\mathrm{B}T}\right) \tag{3.49}$$

with grain size L_G and barrier height E_B. The fit results for the first species were $n_1 = 3 \times 10^{17}$ cm^{-3} and $\mu_1 = 8 \times 10^{-4} T^{3/2}$ cm^2/Vs. For the second species n_2 is determined by $N_\mathrm{D} = 8.5 \times 10^{17}$ cm^{-3} and $E_\mathrm{D}^\mathrm{b} = 61$ meV. The binding energy agrees roughly with the 65 meV which have been attributed to the $\mathrm{Al_{Zn}}$ donor in ZnO [33]. It is also close to $E_\mathrm{D}^\mathrm{b} = 56$ meV calculated from the hydrogen model for a shallow donor in ZnO, given by [39]

$$E_\mathrm{D}^\mathrm{b} = \frac{m_\mathrm{e}^*}{m_0}\frac{\epsilon_0^2}{\epsilon_\mathrm{s}^2}\frac{m_0 e^4}{2(4\pi\epsilon_0\hbar)^2}. \tag{3.50}$$

The fit parameters for μ_2 are $L_\mathrm{G} = 20$ nm and $E_\mathrm{B} = 62$ meV. For a PLD-grown ZnO film on a-sapphire with thickness in the range of 1 μm von Wenckstern [33] reports $L_\mathrm{G} = 40$ nm and $E_\mathrm{B} = 13$ meV. Considering the higher defect density close to the substrate, the value for L_G determined for $a = 75$ nm is well in line with these results. The barrier height is significantly higher, but due to the much higher free carrier density still transparent for the charge carriers.

3.3. Field-Effect Transistors

3.3.1. Modelling of Experimental Data

Before analyzing the properties of various types of FETs, the applicability of the aforementioned device models should be discussed. Exemplarily a ZnO based MESFET with Pt gate is used for comparison with the theroretical descriptions, as this was the FET type most frequently used for this work.

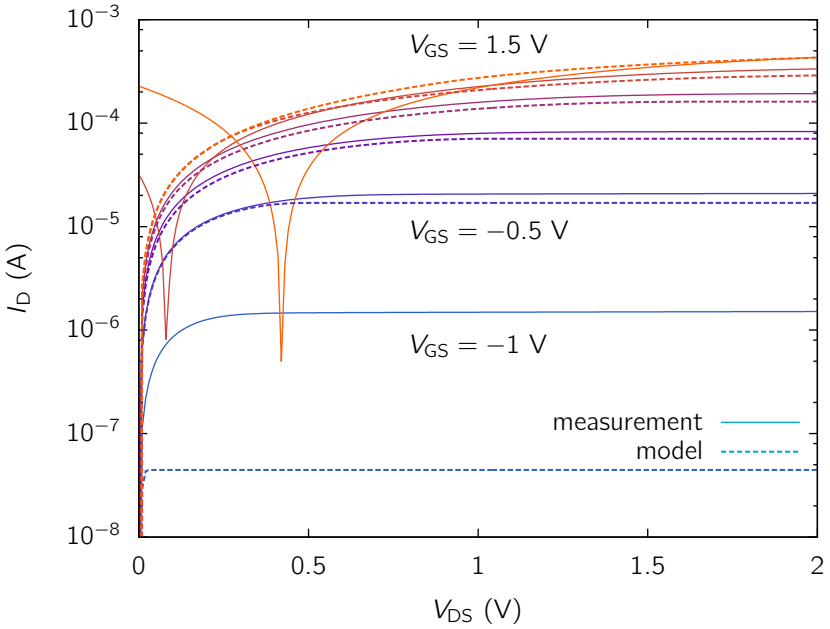

Figure 3.14.: Output characteristics of a ZnO based MESFET with Pt gates, compared to a calculation including subthreshold current and series resistances. The gate voltage was varied in steps of 0.5 V.

The charge carrier density and mobility for this device were obtained by Hall effect measurements, and the thin film thickness by spectroscopic ellipsometry. V_{bi} for reactively sputtered Pt on ZnO is usually between 0.8 V and 0.9 V [61, 49]. Here, in agreement with a fit of the gate diode I-V curve with TE, $V_{bi} = 0.8$ V was used. Together with the lateral dimensions defined by the photomasks, this is sufficient information to calculate the drain current by Eqns. 3.17, 3.19, 3.23, 3.21, and 3.22 for the different voltage regimes. For regarding the subthreshold current, a substitution of the gate voltage according to Eq. 3.31 was conducted. A numerical procedure was necessary to account for the series resistances. The channel current was first calculated without series resistances and then varied until current conservation through R_S, R_D and transistor channel was given. The resulting output characteristics is shown in Fig. 3.14 in comparison to experiment. The transfer characteristic obtained from this model is denoted in Fig. 3.15 by model 1. It is

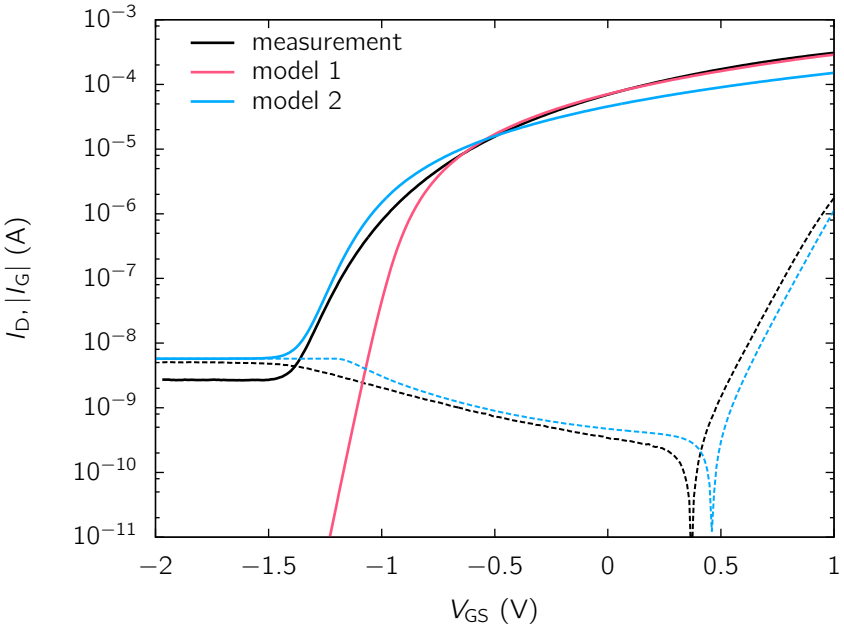

Figure 3.15.: Transfer characteristics of a ZnO based MESFET with Pt gates. Model 1 is similar to the calculations shown in Fig. 3.14. Model 2 includes the gate current, and scales V_{GS} by the ideality factor η obtained from fitting the gate diode current with TFE. V_{DS} was 2 V. The drain currents are depicted by solid lines and the gate currents by dashed lines.

demonstrated, that the description matches best with the experiment for intermediate gate voltages. The agreement is also good for high gate voltages, when $V_{DS} > V_{GS}$ is satisfied. For $V_{DS} < V_{GS}$ the channel potential is dominated by the gate current, which is not included in the model. For gate voltages below -0.5 V the calculated drain current drops much faster than the experimental values. While the model includes an ideal subthreshold current with a slope of 60 mV/dec, the measurement yields $S = 120$ mV/dec. This difference will be discussed later in this chapter. Comparison between different device types indicates strongly, that a connection to the gate structure exists.

In Fig. 3.16 the I-V characteristic of the gate diode is shown. The forward current can be fitted using thermionic emission theory. For diodes fabricated on thick ZnO films ($a \approx 1$ μm) this is the established theoretical approach [40]. The fit depicted in Fig. 3.16 yields $V_{bi} = 0.81$ V and $\eta = 2$. The barrier height is typical for reactively sputtered Pt on ZnO, but η is rather high, even when considering an inhomogenous barrier. The reverse current is not fitted at all by the thermionic emission model. Introducing an appropriate shunt resistance would also affect the forward current. Hence, this is not a suitable explanation for the high reverse current. By using thermionic field emission a far better agreement can be reached. However, similar to TE an ideality factor must be introduced. This was done by exchanging the bias voltage V in Eqns. 3.7 and 3.9 with V/η. Also

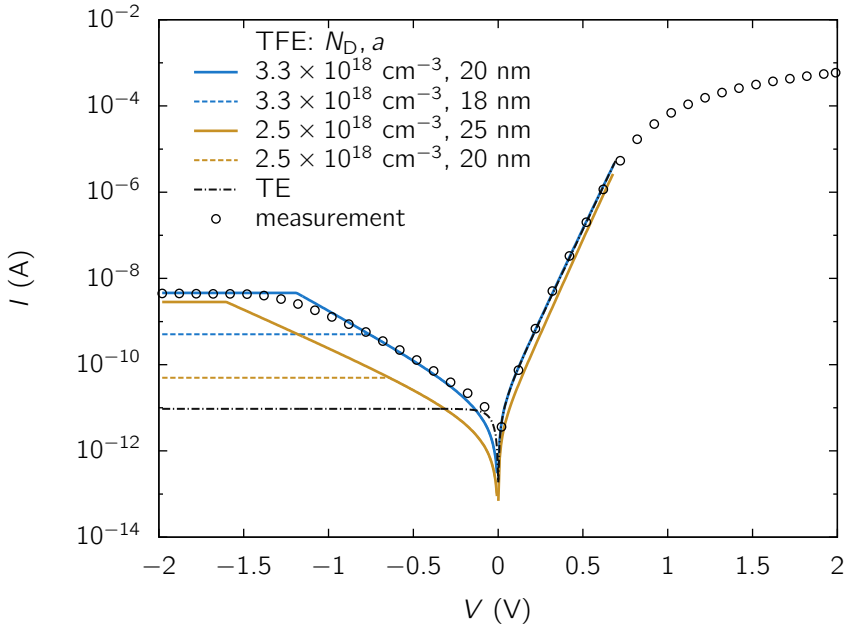

Figure 3.16.: Schottky characteristics of a MESFET with Pt gate, measured between gate and source. The measurement data was fitted using thermionic emission (TE) and thermionic field emission (TFE). For TFE the impact of variations in a and N_D is demonstrated. The fitting constants for TE were $V_{bi} = 0.81$ V and $\eta = 2$, and for TFE $V_{bi} = 0.69$ V and $\eta = 1.55$.

voltage dependent quantities used by these equations were changed accordingly. The finite channel thickness is taken into account by holding the bias voltage constant for $V/\eta < V_T$. For more negative gate voltages, the excess voltage will drop along the series resistance, while the potential below the gate remains unchanged. This is true for $L \gg a$, when the potential in the OFF-regime does not change in direction of the channel length. Then the potential drop between the top of barrier and the substrate/channel interface is fixed at V_P, as the potential curvature is determined by N_D, and the electric field must become zero at the substrate. With these considerations the Schottky characteristics were fitted using $V_{bi} = 0.69$ V, $\eta = 1.55$, and $N_D = 3.3 \times 10^{18}$ cm^{-3}. N_D had to be slightly adjusted, as the reverse current described by TFE is very sensitive to variations of N_D and a. The calculations depicted in Fig. 3.16 demonstrate, that decreasing N_D by 25% leads to a decrease of the reverse current by two orders of magnitude. Decreasing a by 10%, which is approximately the relative error of the measured thickness, leads to a decrease of the reverse current by one order of magnitude. The relative error of N_D is likely higher, probably around 20%, as a is used for its calculation and adds an additional uncertainty to the Hall effect measurements. Thus, it is reasonable to allow a certain adjustment of N_D and a when fitting the Schottky characteristics with TFE.

Using the results from the Schottky diode fit with TFE, the gate current can be included

into the FET model. The potential distribution $V(x)$ in the channel has been solved, and a parallel arrangement of 20 diodes at different positions x was considered. N_D and V_{bi} from the fit were also adapted for the calculation of the channel current. Taking the diode's ideality factor η into account is more difficult. The kink in the reverse current of the diode must match the threshold voltage of the FET, as both features give notice of the same situation, the complete depletion of the channel below the gate. For a first attempt, the gate voltage for the calculation of the channel current was substituted by V_{GS}/η, similar to the calculation of the gate current. The resulting transfer characteristic is denoted in Fig. 3.15 by model 2. The gate current is described well by the model, with a small offset to positive gate voltages. The drain current fits the experiment close to the threshold better than model 1, and also the OFF-current is roughly matched. The similar slope for the subthreshold current raises the question, whether a physical relation between S and η exists. An interesting feature resulting from the theory is, that the kink of the gate current occurs at the connection between subthreshold current and normal channel current. In the experiment the drain current and the gate current become constant at the same gate voltage. This means, that the potential below the gate is not competely constant in the subthreshold regime, as was assumed in the derivation of the model. Besides the subthreshold current, the drain current is not well described by model 2. This is due to the stretching with η and due to the reduced N_D, which results in a lower ON-current. The change in V_{bi} has a minor impact on the characteristic, which was demonstrated by further calculations (not shown).

3.3.2. Comparison of Different Gate Structures

Using ZnO as channel material the fabrication of JFETs [30], MESFETs [28] and MISFETs [4, 52, 29] has been reported. For MESFETs and MISFETs various subtypes concerning the gate structure exist. In the cited papers, mostly static electrical characteristics were published. Such measurements reveal the transconductance, and thereby the amplification of the transistors. For the integration into biosensors, further electrical properties like cutoff frequency and noise as well as processing issues like degradation temperature and passivation are important. For the applicability in a MEA, the device capabilities must be compared to the properties of neuronal action potentials. A typical bandwith used for recording such signals is 10 kHz (see e.g. [62, 63]). Below this frequency the transistors must not damp an applied voltage signal. The expected magnitude of the signals is discussed in Chapter 5 and must be compared to the ratio of FET transconductance and noise, which is examined in Chapter 4. In this section the static and dynamic electric properties of different transistor types are compared, to facilitate the preselection of suitable devices within the multitude of options.

All devices had ZnO channels deposited by PLD with 0.25wt-% MgO in the target on a-sapphire substrates at temperatures between 650°C and 700°C and at 0.02 mbar

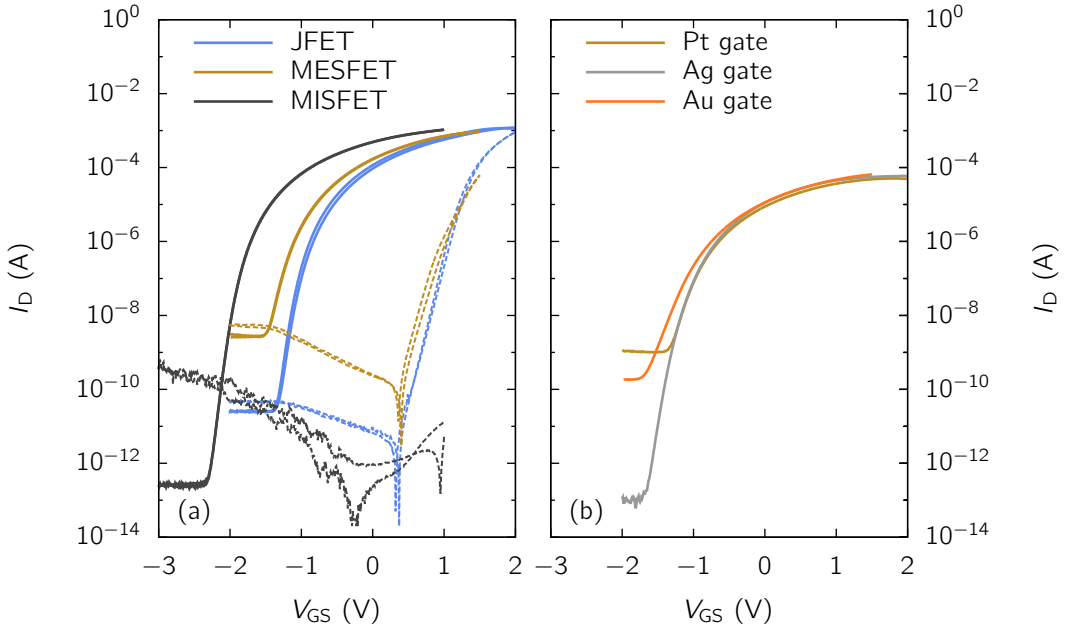

Figure 3.17.: Transfer characteristics of ZnO based transistors. (a) JFET with $ZnCo_2O_4$ gate, MESFET with Pt gate, MISFET with WO_3/ZnO:Ga gate structure, dashed is the gate current. (b) MESFETs with different gate metals.

device type	gate structure	ON/OFF-ratio	g_{max}/W (μS/μm)	μ_{FE} (cm^2/Vs)	I_{off} (A)	S (mV/dec)
JFET	$ZnCo_2O_4$/Au	3×10^7	2.0	14	2×10^{-11}	73
MESFET	PtO_y/Pt	1×10^5	1.5	10	3×10^{-9}	120
MISFET	WO_3/ZnO:Ga	8×10^9	1.4	10	1×10^{-13}	64

Table 3.1.: Properties of the ZnO based FETs at room temperature (20°C).

oxygen atmosphere. Ohmic contacts were obtained by dc magnetron sputtering of gold in argon atmosphere. For the JFETs $ZnCo_2O_4$ gates were grown by PLD at room temperature and 0.05 mbar oxygen atmosphere. MESFET gates were fabricated by sputtering of platinum, silver or gold in a mixed atmosphere of oxygen and argon, with a capping of platinum or gold sputtered in a pure argon atmosphere. The MISFETs had PLD-grown WO_3 as gate insulator, which was deposited at room temperature and 0.02 mbar oxygen pressure. On the insulator GaZnO (ZnO with 4wt-% Ga_2O_3 in the target) was deposited by PLD as contact material. For best comparability the FETs presented in Fig. 3.17(a) were fabricated from the same sample, which was cleaved prior to gate deposition. The channels of the MESFETs shown in Fig. 3.17(b) were not from the same substrate, but deposited simultaneously in one PLD process.

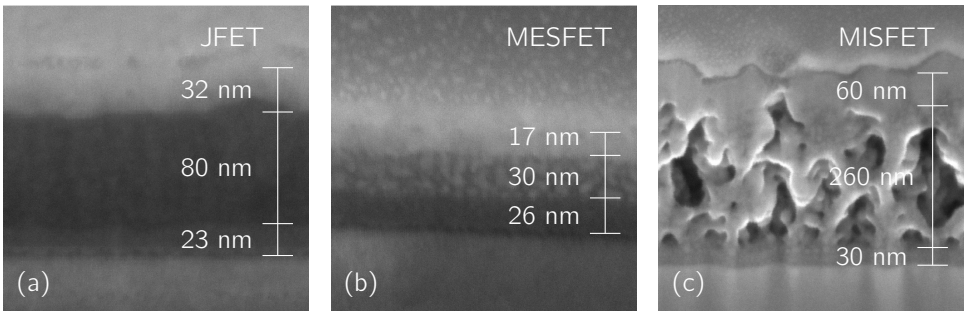

Figure 3.18.: Scanning electron micrograph of transistor cross sections prepared by focussed ion beam. The lowest layer with thickness label is always the ZnO channel. The two layers of the respective gate structure are described in Tab. 3.1.

In the following, the FETs with different gate types (JFET, MESFET, and MISFET) are compared. Some of these results have been published in [64] and were obtained in collaboration with Friedrich-Leonhard Schein and Michael Lorenz. The room temperature transfer characteristics are shown in Fig. 3.17(a). Key quantities extracted from the measurements are summarized in Tab. 3.1. The ZnO thin film had a thickness of 20 nm determined by AFM at the channel edges. $\mu = 20$ cm^2/Vs and $n = 4 \times 10^{18}$ cm^{-3} were obtained by Hall effect measurements. In Fig. 3.18 cross sections of the gate structures are presented, which were prepared by focussed ion beam and recorded by scanning electron microscopy. The thickness of the channels measured by SEM deviates somewhat from the 20 nm determined with AFM, indicating an uncertainty of about 30% for the dimensions given in Fig. 3.18.

The JFET exhibits the largest V_T, which probably corresponds to a high built-in voltage. As the band alignment of $ZnCo_2O_4$ and ZnO is not known yet, the calculation of V_bi from the *pn*-diode's *I*-*V* characteristic is not possible. The transfer characteristic also exhibits a small hysteresis, that is not present for MESFET and MISFET. Schein *et al.* [30] attribute this effect to slow trap states at the interface between the amorphous $ZnCo_2O_4$ and the crystalline ZnO.

The MESFET with Pt gate exhibits the highest OFF-current among the three devices, which traces back to a high gate leakage current. Also the subthreshold slope of $S = 120$ mV/dec is comparably high. This is connected to the high OFF-current, as the maximum S is only obtained for small channel currents, which are in this case obscured by the large leakage current. Frenzel *et al.* [65] report similarly fabricated devices with $S = 83$ mV/dec and two orders of magnitude lower I_off. Their samples exhibited carrier densities between 1.5×10^{18} cm^{-3} and 2.8×10^{18} cm^{-3}. The difference in the leakage current between the different MESFET samples was explained in section 3.3.1 by the high sensitivity of the diode reverse current on N_D, as described by TFE.

The highest ON/OFF ratio of more than 9 orders of magnitude was found for the MISFET, due to the low leakage current of a MIS diode compared to Schottky contact and *pn*-junction. V_T is the most negative among the examined FETs, explained by the voltage drop across the insulator. The subthreshold slope of 64 mV/dec is very close to the theoretical minimum of 60 mV/dec at room temperature. The gate capacitance was $C_i = 8 \times 10^{-7}$ F/cm^2, determined by QSCV measurement.

MESFETs with different gate metals on ZnO thin films were first compared by Frenzel *et al.* [49]. The ON/OFF-ratios reported for their FETs were around 10^8 with Ag gates, more than 10^6 with Pt gates, and about 10^3 with Au gates. The high rectification ratios of reactively sputtered Ag contacts were first reported by Allen *et al.* [34], and are due to high barrier heights around 1 V. The measurements shown in Fig. 3.17(b) demonstrate, that also with Au gates ON/OFF-ratios $> 10^5$ can be achieved. The previous section demonstrated, that small variations in a and N_D lead to large changes in the Schottky diode's reverse current, and thus the transitor's OFF-current. As the barrier height of reactively sputtered Au on ZnO is typically smaller than for Pt contacts (0.69 V compared to 0.84 V reported by Lajn *et al.* [61]), a higher OFF-current for Au must be expected. When comparing different samples with Au gates, it turns out that the OFF-current shows a stronger variation than for Pt gates, and the ON/OFF-ratio is indeed often lower than 10^5.

The temperature stability of the FETs has been tested up to 150°C. Fig. 3.19(a-c) show the transfer characteristics for JFET, MESFET and MISFET, respectively. All devices stay functional within the examined temperature range, but several changes can be observed. It is notable, that the current decreases for all devices with increasing temperature. For TFTs in literature usually the opposite behavior is reported, explained by temperature activated trap states [66, 67, 68]. For ZnO based FETs a decreasing current with increasing temperature has been reported before, and attributed to traps in the channel or at the channel/oxide interface [69, 29, 30]. For the MESFET examined here, the current decrease is mostly due to an increase in V_T, as illustrated by Fig. 3.20(a). The effective barrier height of the gate diode increases with increasing temperature, which is shown by the decreasing reverse current in Fig. 3.19(d). The change of the barrier height is depicted by the dashed line in Fig. 3.20(a) and is in agreement with the model of a laterally inhomogenous barrier height [70]. According to Eqn. 3.16 changes in V_{bi} are directly affecting V_T. An additional process with exponential dependence on the temperature is neccessary to explain the total V_T shift. This process must be introduced by the Pt gate deposition, as it is not observed with the other FET types. After cooling down to room temperature, this part of the shift remains permanent. Thus, curing of trap states at the interface might be responsible. Also the OFF-current is permanently lowered by the temperature cycle, which might be caused by the same process. The MESFET ON-current decreases to a third of its initial value when the temperature is increased to 150°C. After cooling down to 20°C a permanent decrease of 50% compared to the previous room temperature value is observed. The current decrease

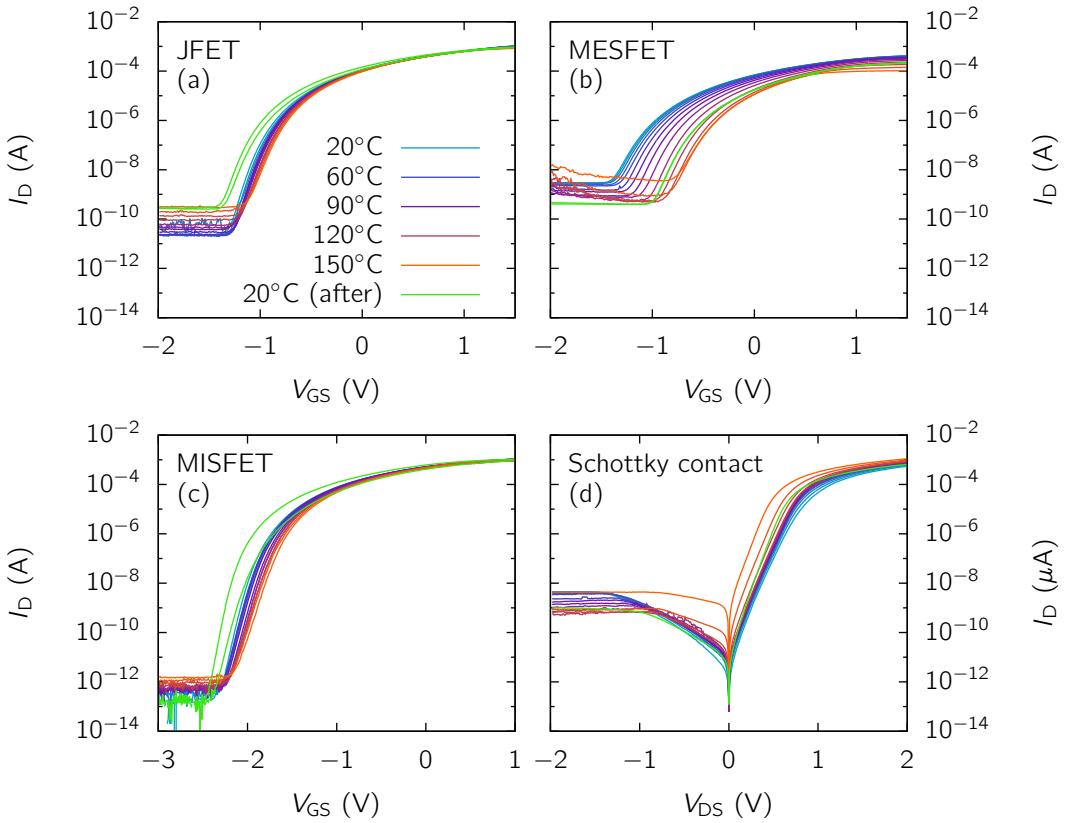

Figure 3.19.: FET characteristics measured from 20°C up to 150°C. The transfer characteristics at 20°C after the temperature cycle are depicted as double measurements (measured in both directions), in order to show changes in the hysteresis compared to Fig. 3.17. For a clearer view all other traces are single measurements.

is also responsible for the decrease of the field-effect mobility depicted in Fig. 3.20(c), which is calculated from the maximum transconductance. At $T > 120$°C the OFF-current increases, which could be a sign for degradation of the Schottky contact, which has been reported for Pt MESFETs to occur at temperatures above 75°C [49]. However, in contrast to the results presented in the cited paper, the device examined here showed no permanent degradation of OFF-current or barrier height. As mentioned above for room temperature measurements, the subthreshold slope S of the MESFET is comparably large at room temperature, due to the high OFF-current. For higher temperatures, S approaches the theoretical minimum, but increases strongly for $T > 120$°C. This corresponds to changes in the OFF-current, which has its minimum around 120°C.

The JFET's V_T exhibits a small shift compared to the MESFET, which might be according to an inhomogenous barrier. The subthreshold slope does not reach the theoretical minimum, but follows with an offset smaller than 20 mV/dec. The field-effect mobility

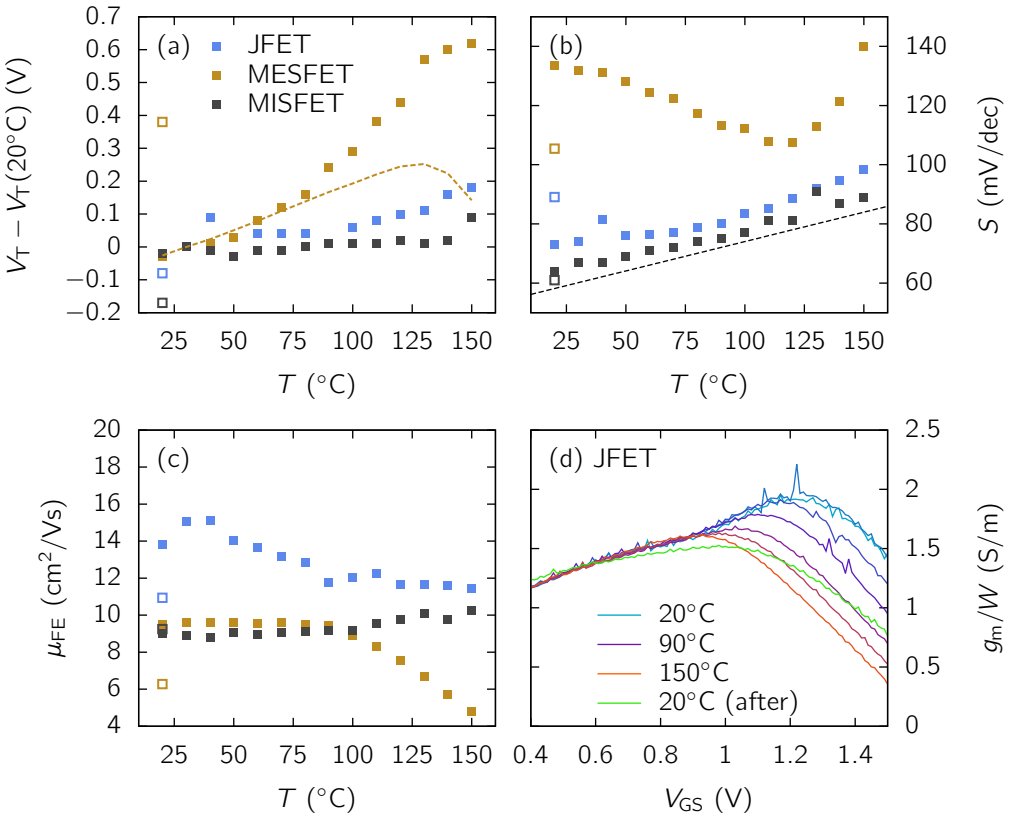

Figure 3.20.: Transistor properties at temperatures from 20°C up to 150°C. Values for the measurements at 20°C after the temperature cycle are depicted with open symbols. (a) Change in the threshold voltage compared to 20°C. The dashed line shows the change of the MESFET's Schottky barrier height. (b) Subthreshold slope, dashed is the theoretical minimum. (c) Field-effect mobility. (d) Transconductance of the JFET in dependence of the gate voltage.

is larger compared to the other FET types at room temperature, but decreases permanently when heated to 150°C. The transconductance depicted in Fig 3.20(d) reveals, that an additional maximum is responsible for the increased μ_{FE}, which disappears after heating. As the additional maximum appears at a gate voltage larger than the usual maximum, the origin could be an elevated carrier density close to the channel/gate interface, maybe caused by interface states introduced by the amorphous $ZnCo_2O_4$. This states could be healed out at increased temperatures, resulting in a carrier density comparable to the other FET types.

The MISFET is the most stable device in the examined temperature range. V_T and μ_{FE} exhibit only minor changes, and S follows closely the theoretical minimum depicted by the dashed line in Fig 3.20(b). However, after the temperature cycle the transfer

characteristic shows a distinct hysteresis, and V_T shifts about -150 mV. The reason could be temperature activated trap states in the porous insulator material.

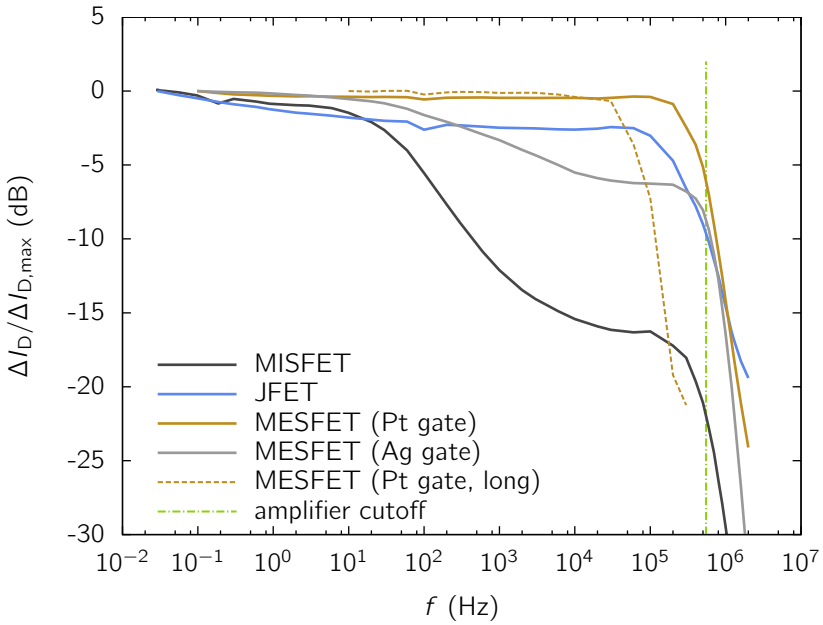

Figure 3.21.: Frequency dependent response of I_D on a sinusoidal gate voltage. The devices were switched between ON- and OFF-regime. The gate length for all devices was $L = 10$ μm, except the FET denoted long, which had $L = 120$ μm.

The cutoff frequency for a signal transmission from the gate voltage to drain current has been determined by appying sinusoidal voltages at the transistor gates. In series to the drain a resistor of 100 kΩ or 220 kΩ was used, where the voltage drop proportional to the drain current was measured using an self built instrumentation amplifier and an oscilloscope. In Fig. 3.21 it can be seen, that for MESFETs with Pt gates and short gate length ($L = 10$ μm) no drop in the signal occurs up to the cutoff of the preamplifier at 550 kHz. The same is observed for MESFETs with Au gates (not shown in the figure). MESFETs with Ag gates exhibit a decreasing current signal for f>10 Hz. This can be attributed to the indiffusion of Ag in the channel during fabrication, which has been reported to increase the contact capacitance [71]. There are also reports, that Ag acts as an acceptor in ZnO [72, 73]. As for Pt and Au no indiffusion into ZnO has been reported, this is most probably the origin of the differing frequency response. The switching behavior of ZnO based MESFETs has been published more detailed in [74].

As additional proof for the impact of Ag acceptors on the switching speed, samples with Ag doping in the channel have been fabricated. The sintering of PLD targets consisting of ZnO and 1wt-% Ag_2O_3 proved to be challenging, as demixing and clustering of the silver in the target took place. Therefore, the samples had inhomogenous silver content.

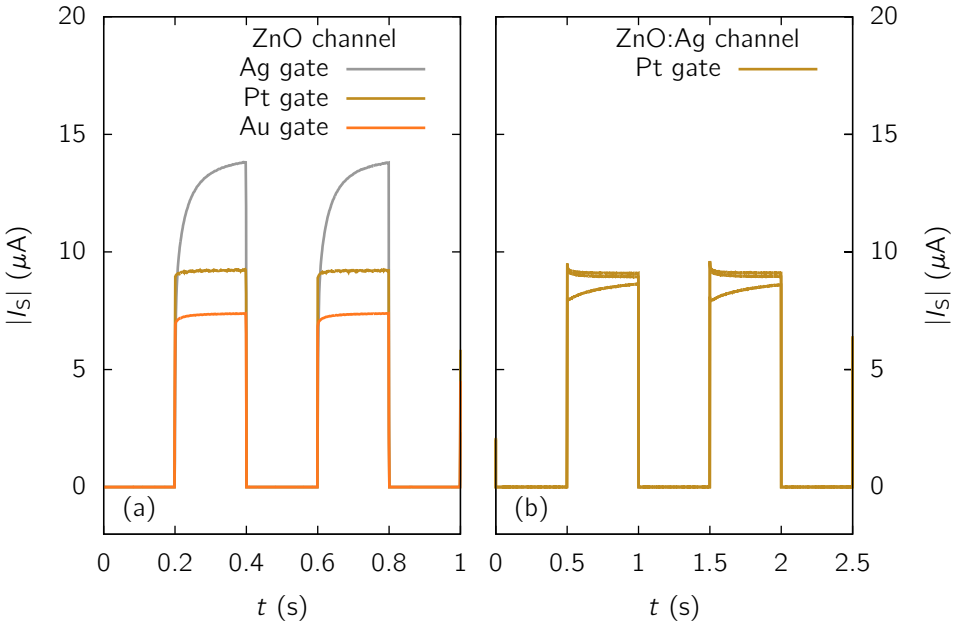

Figure 3.22.: Gate lag measurements on ZnO-based MESFETs. (a) With ZnO channels. (b) With ZnO:Ag channels, measurements on three different FETs from the same sample are shown. V_{GS} was switched between -2 V and 0 V, V_{DS} was constant at 2 V.

Nevertheless, a qualitative analysis of the Ag doped samples has been conducted. In Fig. 3.22 gate lag measurements for MESFETs are presented. At the gate contact rectangular voltage pulses were applied, which switched the devices between OFF- and ON-regime. For FETs with Au and Pt gate on ZnO channel I_D switches immediately within the time resolution of 1.4 ms, while the device with Ag gate approaches the steady state value with an average time constant of around 30 ms, determined by fitting the transient with a stretched exponential function. FETs with Pt gate on ZnO:Ag channel exhibited various transient types, due to the inhomogenous distribution of Ag in the target. Fig. 3.22(b) shows, however, that larger transients are observed than without Ag doping. Many devices exhibited current overshoot instead of a slow approach of the steady state value. Temperature dependent gate lag measurements (not shown) indicated, that in all devices at least two processes with opposite transient behavior contribute, but with varying and temperature-dependent ratio. It can not be excluded at this point, that the integration of Ag in the thin films causes additional structural defects, that contribute to the lag effects. Nevertheless, an impact of Ag doping on the current response is strongly indicated.

MESFETs with Pt gates and larger gate length of $L = 120$ μm show a cutoff at about 60 kHz. With the maximum transconductance $g_m = 8$ μS obtained from the transfer characteristics and a calculated gate capacitance $C_G = 60$ pF in the ON-region, one can

estimate an upper boundary for the cutoff frequency $f_{c,est} \approx 1/(2\pi C_G/g_m) = 15$ kHz. This value underestimates the actual f_c, but gives an idea where to expect it. Scaling the calulated value for MESFETs with $L = 10$ μm gives $f_{c,est} \approx 2$ MHz. In collaboration with Gregor Keller (Solid-State Electronics Departement, University of Duisburg-Essen) high frequency measurements have been attempted, in order to measure the actual cutoff frequency. The lower frequency limit of the measurement setup was 45 MHz. The results indicated, that this was considerably higher than the FET's cutoff frequency, prohibiting a meaningful analysis. Thus, together with the measurements on MESFETs with long gates and the associated calculations, a cutoff frequency around 5 MHz for MESFETs with Pt gates and $L = 10$ μm is considered a reliable estimate. This agrees with the value calculated by Klüpfel *et al.* [64] from transconductance and QSCV measurements.

The drain current response of the JFET shown in Fig. 3.21 decreases at low frequencies between 0.1 and 100 Hz, but for higher frequencies a constant signal up to the limit of the measurement range is observed. The low frequency loss might correspond to the hysteresis oberved in the transfer characteristics, which was attributed to interface traps.

The MISFETs with WO_3 gate insulator suffer from continuous signal loss already at low frequencies. This is probably due to slow surface states in the porous insulator (see cross section in Fig. 3.18(c)). The slow switching is not a general property of MISFETs, and faster ZnO based TFTs have been reported, up to frequencies in the MHz range [26, 27]. When using PLD for the insulator deposition, one must pay attention to the danger of droplets from the target, that can create shorts between gate and channel. With WO_3 this can be avoided by using a large insulator thickness, made possible by the high dielectric constant $\epsilon_r \approx 70$ [29]. For other insulators different deposition methods like atomic layer deposition (ALD) or rf sputtering need to be employed. Also eclipse PLD could be beneficial to the insulator homogeneity. The difference of this method to standard PLD is a shadow mask introduced between target and sample, so that only small particles scattered around the mask can reach the substrate. Higher temperature deposition of the insulating material would also be beneficial to the material quality. However, in that case lift-off can not be used for structuring the insulating layer, as typical photoresists degrade at temperatures above 150°C. Finding a selective etching process is very challenging, as ZnO is etched by very dilute acids, while insulating metal oxides like Al_2O_3 or HfO_2 are only etched by concentrated acids at high temperatures. Only recently a selective etching process of Al_2O_3 has been reported, that does not affect ZnO [75]. Alternatively plasma etching could be facilitated to structure the insulator. Due to these challenges, which reach beyond the scope of this work, it was decided to limit the further examinations to JFETs with $ZnCo_2O_4$ and MESFETs with Pt and Au gates.

3.3.3. Passivation

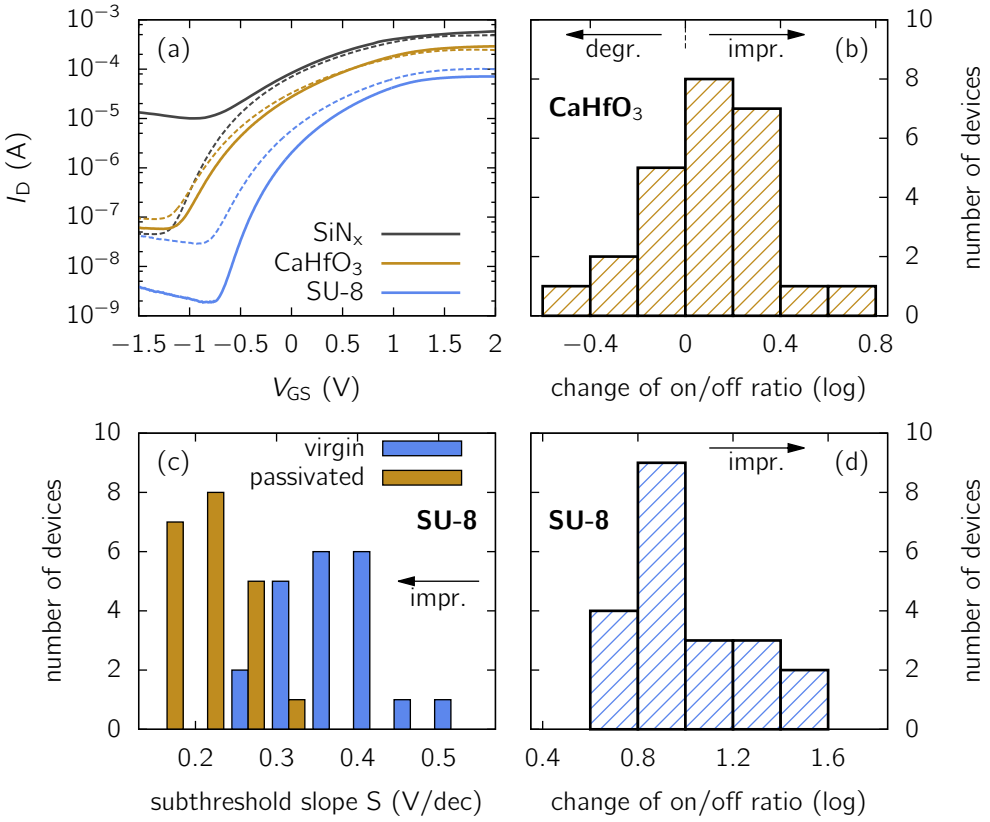

Figure 3.23.: Results for the passivation of ZnO based MESFETs with Pt gates. The dashed lines in (a) depict the transfer characteristics before and the solid lines after passivation.

In the previous section measurements on devices exposed to ambient air were presented. The integration of devices in an application usually requires an encapsulation, that protects the electronics from potentially harmful environmental conditions. This is especially true for MEA applications, as living cells are cultivated in electrolytic solutions. Such liquid would not only lead to shortcuts, but also dissolve the channels of ZnO-based FETs. A further reason for covering of the devices is the passivation of surface effects. The ZnO/electrolyte interface has been proposed for the use in pH sensors [76, 77], and ZnO nanorod arrays in contact to air for the sensing of various gases, including H_2, NH_3, and CO [78]. At low pressures the formation of a surface conduction path has been observed, which would short the gate with the ohmic contacts in a FET [79]. In an application, where the FETs are not directly involved in the sensing of evironmental conditions, stable operation regardless of the surrounding conditions must be ensured by a suitable protecting layer. The successful suppression of surface conduction by passivation of Au Schottky contacts with $CaHfO_3$ was achieved by von Wenckstern *et al.* [80].

For ZnO based FETs the passivation with Al_2O_3 has been reported [75]. For GaInZnO based FETs many passivation materials have been evaluated, including SiO_2, Ta_2O_5, Al_2O_3, Y_2O_3, and HfO_2 [35, 6]. Olziersky *et al.* [36] passivated GaInZnO based TFTs with SU-8 resist, which lowered the OFF-current by two orders of magnitudes under specific fabrication conditions.

For this work, $CaHfO_3$ was singled out as PLD-grown insulator, due to its successful application for the passivation of Schottky diodes. SU-8 was investigated due to the widespread use in biotechnological applications. Additionally SiO_x and SiN_y grown by plama-enhanced chemical vapor deposition (PECVD) were included in the study, which have also been reported for the passivation of MEAs (e.g. [10, 63]). All processes were conducted at room temperature or up to a maximum of 90°C. In Fig. 3.23(a) the impact of passivation on the transfer characteristics of MESFETs with Pt gate is demonstrated. $CaHfO_3$ does not change the device properties by much. Fig. 3.23(b) shows, that the ON/OFF-ratio changes up to a factor 5 for individual devices, but the average stays basically constant. Passivation with SU-8 tends to improve both the individual FET characteristics and the homogeneity of devices on the same sample. Most prominently the OFF-current decreases, which increases the ON/OFF-ratio in average about tenfold. The subthreshold slope S decreases and becomes more homogeneous, as shown in Fig. 3.23(c). It should be noted, that also the ON-current decreases. This effect is unwanted, as it also lowers the transconductance and thus the amplification potential of the FET. The results for passivation with PECVD grown insulators were similar among SiO_x and SiN_y and are exemplarily shown for nitride. MESFETs with Pt gate degraded strongly, resulting in ON/OFF-ratios less than 100. Au Schottky contacts were competely ohmic after the PECVD process. This degradation has not been investigated further, but is probably connected to the deposition process rather than the used materials. Otherwise at least somewhat different results for SiO_x and SiN_y would be expected.

The examinations yield PLD grown $CaHfO_3$ and SU-8 resist as suitable passivation materials, which do not degrade the FET characteristics and actually improve some of the device properties. No conclusion about the protective effects of these materials can be drawn at this point. The material stability under cell culture conditions will be discussed in chapter 5.

3.3.4. Influence of Geometrical Parameters

Besides the choice of the most suitable materials, the dimensions of transistors have a crucial influence on the performance. This is impressively demonstrated by the ongoing development of silicon technology, where the gradual shrinking of the structures ensures further improvements in terms of energy efficiency, operation frequency and cost. The inverse proportionality between gate length L and cutoff frequency is universal for FETs

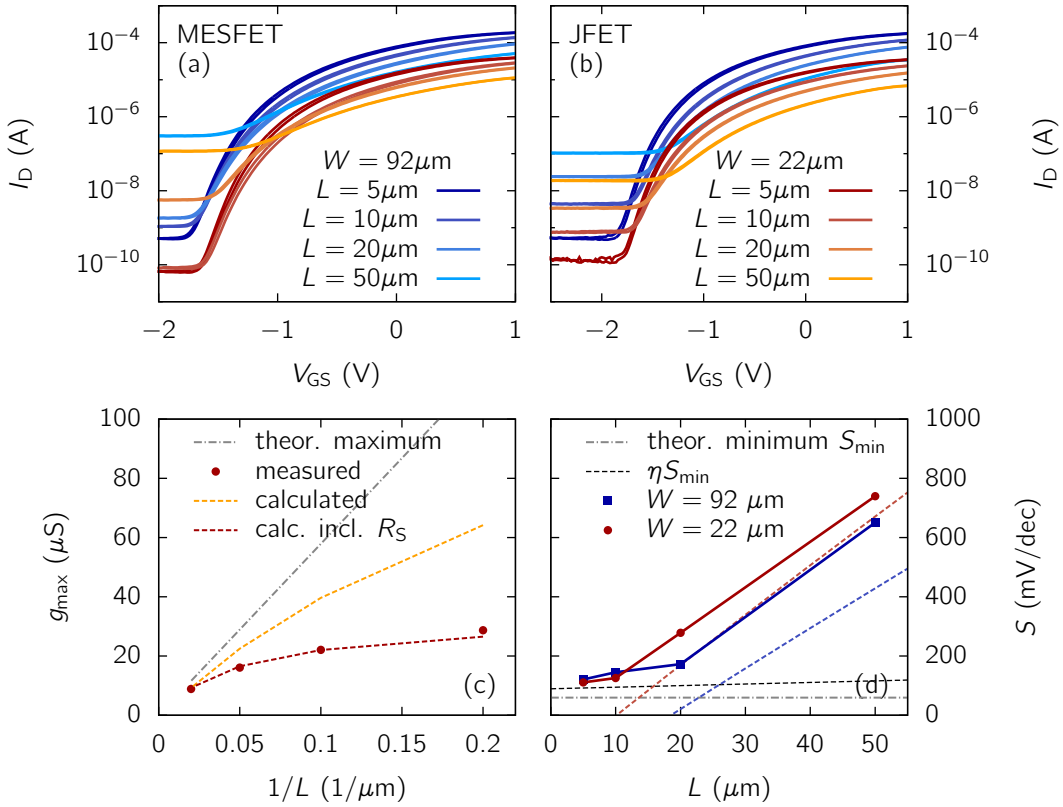

Figure 3.24.: Influence of lateral dimensions on FET characteristics. (a,b) MESFETs with Pt gate and JFETs with $ZnCo_2O_4$ gates, respectively. The keys are valid for both subimages. (c) Maximum transconductance of MESFETs with $W = 22\ \mu m$. Theoretical maximum according to Eqn. 3.26 and calculation according to Eqn. 3.25. (d) Subthreshold slope of the MESFETs. The red and blue dashed lines correspond to the transconductance calculated from FET theory, evaluated at the V_{GS} where S was measured.

and was demonstrated in this work for MESFETs with Pt gates. The gate width W can be considered as scaling factor for the currents flowing through the device. Thereby, it is directly proportional to the transconductance of the device. For logic circuits it is desirable to keep the currents small, in order to avoid unnecessary power consumption. In analog amplifiers, larger currents might be desirable for a better signal-to-noise ratio. In the theoretical description for FETs described in section 3.1, W/L appears as factor for the drain current, and no other dependency on the gate dimensions is present. However, the gate current is proportional to the gate area WL. Hence, the FET characteristics for different gate sizes with equal W/L will only be similar where the gate current is negligible.

In Fig. 3.24 the transfer characteristics of FETs with different lateral dimensions are

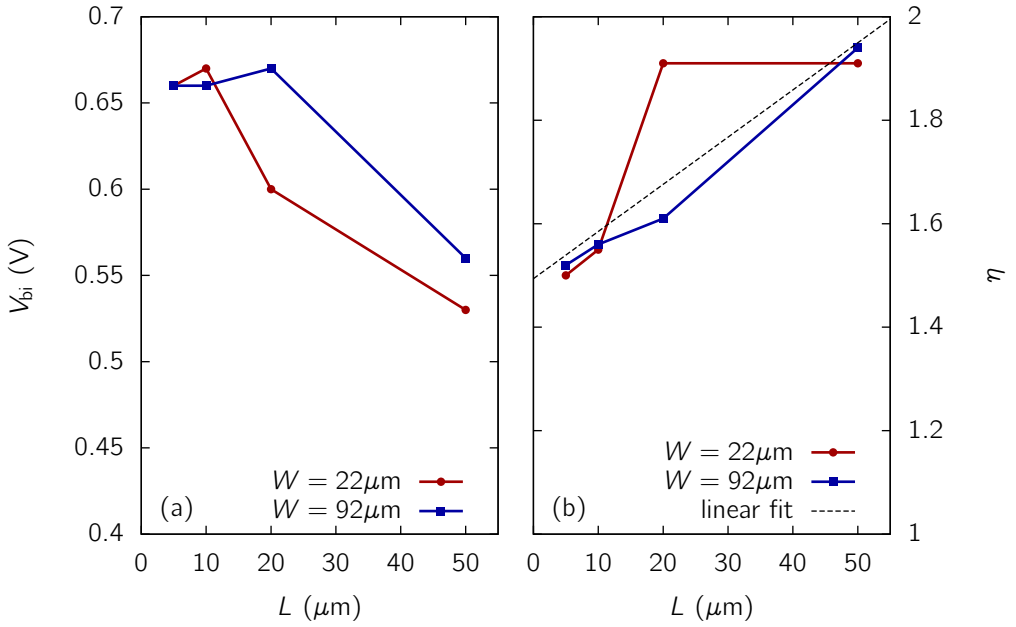

Figure 3.25.: Fit parameters for MESFET gate contacts with varying gate length, described by TFE. Only the forward current was fitted, because of the unsystematically changing reverse current. The straight line in (b) is given by $\eta = 1.5 + L \cdot 0.009\ \mu\text{m}^{-1}$.

shown. Both ON- and OFF-current follow the respective proportionality on L. For the JFETs the dependency is more regular than for the MESFETs, due to the more pronounced inhomogeneity of the Pt Schottky contacts. The JFETs ON-current exhibits a direct dependency on $1/L$, according to theory. In the gate voltage range between -1 V and 0 V, where the gate currents are small, the curves with W/L of 92 μm/50 μm and 22 μm/10 μm overlap, as expected for similar W/L. The OFF-current varies over more than 2 orders of magnitudes, for a change in L of a factor 10. This is surprising, as the diode reverse current is expected to change with linear proportionality to the area, at least when a one-dimensional diode model is considered. Also for the MESFET this overproportional change in the OFF-current is observed, although the current changes less systematically. Most likely a two-dimensional model of the device must be applied in order to explain this behavior. The limited applicability of the one-dimensional diode model is confirmed by fitting the MESFET gate Schottky contacts with TFE. The parameters obtained from fitting the forward current are shown in Fig. 3.25. As all contacts were on the same sample, the channel material and also the gate contacts should have similar properties. However, V_{bi} decreases about 0.1 V when changing the gate length from 5 μm to 50 μm. η increases from 1.5 at small gate lengths to nearly 2. This raises the question, whether the deviation of η from one is generally caused by geometrical constraints. Diodes on thick, highly doped ZnO films with ohmic bottom contact could help to clarify this matter. It would be useful, if the more regular

JFET characterisics could be analyzed accordingly. However, without knowledge of the band alignment in the *pn*-diode, an exact description is not possible. Thus, further considerations will be focused on the MESFETs.

The transconductance g_m of the FETs can be described according to Eqn. 3.25, when the series resistance R_S is considered by $g_\mathrm{m}^{-1} = g_\mathrm{m,sat}^{-1} + R_\mathrm{S}$. R_S is determined by the part of the channel between the gate and the ohmic contacts and easily calculated. The theoretical maximum g_max, given by the channel conductance, is not reached due to the increasing gate current for positive V_GS. Thus, for the calculation shown in Fig. 3.24(c) the measured voltage V_gmax, where the maximum transconductance was observed, was plugged into Eqn. 3.25. For the calculation of V_gmax a MESFET model is needed, that includes the gate current. Besides mathematical difficulties, the unclear origin of the ideality factor η and its dependence on the gate length hinder the development of such a model so far.

As described before, the subtreshold slope is determined by taking the inverse of the maximum slope of the logarithmic transfer curve. The actual subthreshold current is observed for $V_\mathrm{GS} < V_\mathrm{T} = V_\mathrm{bi} - V_\mathrm{P}$ (as indicated by the name), and in the ideal case $\propto \exp(eV_\mathrm{GS}/(k_\mathrm{B}T))$. This leads to the theoretical minimum $S_\mathrm{min} = 60$ mV/dec at room temperature. Fig. 3.24(d) shows a strong increase of S at large L. When the gate current in the OFF-region is large, it crosses the ideal drain current at higher gate voltages, resulting in a higher apparent threshold voltage $V_\mathrm{T,app} > V_\mathrm{bi} - V_\mathrm{P}$. In this case, the method for determining S actually gives an apparent subthreshold slope

$$S_\mathrm{app} = \left(\frac{\mathrm{d}\log_{10}(I_\mathrm{D})}{\mathrm{d}V_\mathrm{GS}}\right)^{-1} = \frac{\ln(10) I_\mathrm{D}}{g_\mathrm{m}}. \tag{3.51}$$

For the calculation of S_app, one must know the gate voltage $V_\mathrm{S,app}$, at which S is minimal. It is close to $V_\mathrm{T,app}$, which is determined by the gate leakage voltage. As the gate voltage is not easily described theoretically, $V_\mathrm{S,app}$ was taken from the transfer characteristics and the dependency on L extracted by a linear fit. This values were plugged into Eqn. 3.51, yielding the results depicted in Fig. 3.24(d) as blue and red dashed lines. Especially for $W = 22$ μm the agreement with the experimental values is good. The difference between experimental S and calculation is due to the gradual transition between the constant OFF-current and the ideal drain current, resulting in a reduced slope of the transfer characteristics close to $V_\mathrm{T,app}$. In summary, the measured values for S show, that only for $L \lesssim 15$ μm the actual subthreshold slope is determined. For larger L the apparent S is a measure of the transconductance g_m close to $V_\mathrm{T,app}$.

It can be speculated, that a connection exists between the ideality factor η of the Schottky diodes and the deviation of S from the theoretical minimum. Here, the actual S for $L < 15$ μm is addressed. The Schottky diode reverse current exhibits a kink for the

voltage at which the channel is completely depleted. This voltage is naturally the same as the measured V_T (compare Fig. 3.17 and Fig. 3.16). When the Schottky I-V curve is fitted with TFE, the ideal diode characteristic is stretched by η, which also shifts the MESFET's V_T to more negative values compared to the ideal device. The middle part of the MESFET transfer characteristics is usually well described by the ideal characteristics, indicating that the stretching of the transfer curve, necessary for the consistence between diode and FET characteristics, takes place close to V_T. If this stretching also applies to the subthreshold current, it would result in $S = \eta S_{min}$. This relation is shown Fig. 3.24(d) by the black dashed line, and describes the right dependency on L. However, without a better understanding of η, the relation between S and η is hard to prove.

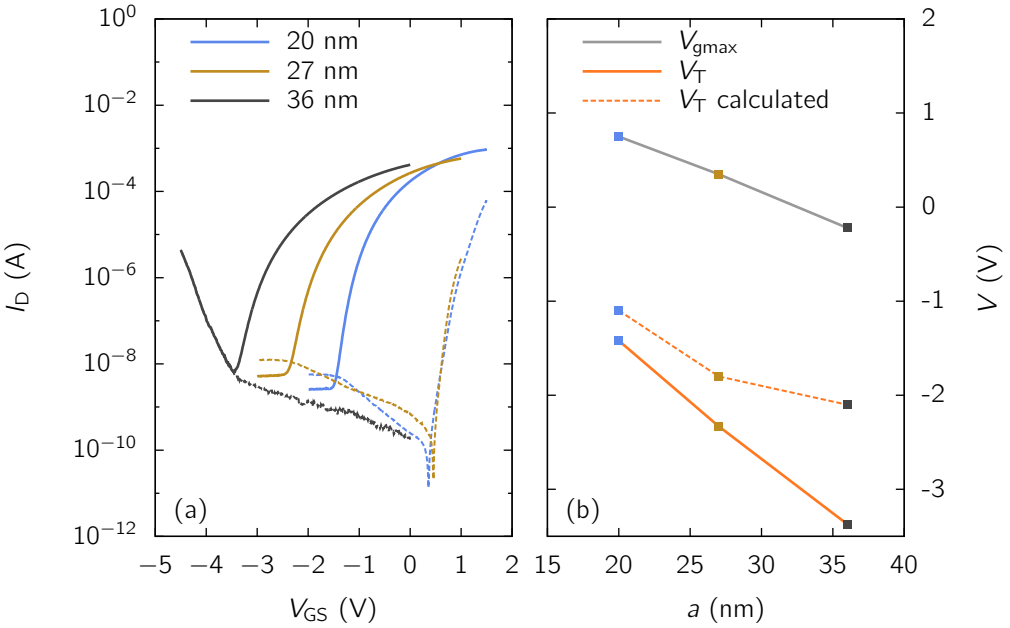

Figure 3.26.: Influence of channel thickness on FET characteristics. (a) Transfer characteristics. (b) Turn-on voltage and voltage of maximum transconductance. The calculation was according to Eqn. 3.16, using the Hall carrier density for N_D.

a (nm)	n_H (cm^{-3})	g_{max}/W ($\mu S/\mu m$)	S (mV/dec)
20	4.3×10^{18}	1.5	120
27	3.2×10^{18}	0.78	170
36	2.0×10^{18}	0.62	180

Table 3.2.: Variation of thickness

The thin film thickness a has a major influence on the FET properties, especially on V_T and the voltage V_{gmax} where the maximum transconductance occurs. Also the absolute

value of the channel current and the transconductance depend on a. Due to the dependence of the channel transport properties on a, the situation is more involved with ZnO based devices on a-sapphire, than the usual equations for I_D suggest. For that reason, the examination presented here is more qualitative than for the dependence on W and L. Fig. 3.26 illustrates several properties, that are influenced by a. Most clearly the threshold voltage shifts to negative values with increasing a. In Fig. 3.26(b) a calculation of V_T is shown, using the charge carrier density obtained from Hall effect measurements before FET fabrication. Due to the neglected subthreshold current, the measured values are some 100 mV more negative. For the largest a the difference between measurement and calculation increases to more than 1 V. Most likely this is due to a change in the electronic transport properties during FET fabrication, which can be observed for $a \gtrsim 30$ nm. This leads to underestimation of N_D, and therefor less negative V_T. In the next chapter, some more details on the change of n_H and μ_H during lithographic processing are given. The shift of V_T also affects the OFF-current, because at some bias voltage the diode breaks down. This can be observed for the sample with $a = 36$ nm, where the OFF-current is not constant but strongly increasing with decreasing V_{GS}. Fig. 3.26(b) shows, that V_{gmax} shifts roughly linearly with a. If the transistor is supposed to work close to the maximum transconductance in an application, a can be used to control the working point. For example, it might be desirable to minimize the gate current, which is zero around $V_{SG} = 0.4$ V for all thicknesses. In Tab. 3.2 the changes of g_{max} and S with varying a are summarized. Although g_{max} is defined linearly dependent on a by Eqn. 3.26, the actual g_{max} decreases with increasing a. On the one hand, the carrier density n decreases with increasing a, on the other hand V_P depends quadratically on a and scales the voltage dependent part of g_m, as described by Eqn. 3.25.

In summary, many features of ZnO based MESFETs on a-sapphire can be theoretically well described, when non-idealities like the series resistance are kept in mind. For modelling the devices, the dependence of the electronic transport properties on a, that is caused by the indiffusion of Al from the substrate during PLD, must be considered. The I-V characteristic of the gate diodes can be described with TFE, when an ideality factor η is introduced. This factor is the weakest point in the model, as its origin is unclear so far. However, measurements on FETs with varying gate length indicate, that geometrical constraints contribute at least partially to η. An inhomogenous barrier height, as often used to explain large ideality factors with TE, might also increase η. Directly depending on the diode characteristic, and thus on η, are the FET properties V_T and I_{off}. The diode forward current determines, at which voltage g_{max} is observed, and thus its absolute value, too. Furthermore, a direct dependency of S on η might exist. For use in an application, L should be small for high transconductance and high cutoff frequency. W scales the absolute value of currents and transconductance, but also increases the gate capacity. This might be undesirable, as the necessary power for switching the device increases accordingly. a can be used to shift the voltages V_T and V_{gmax}, but has an influence on g_m and the channel current as well.

3.4. Simple Inverter

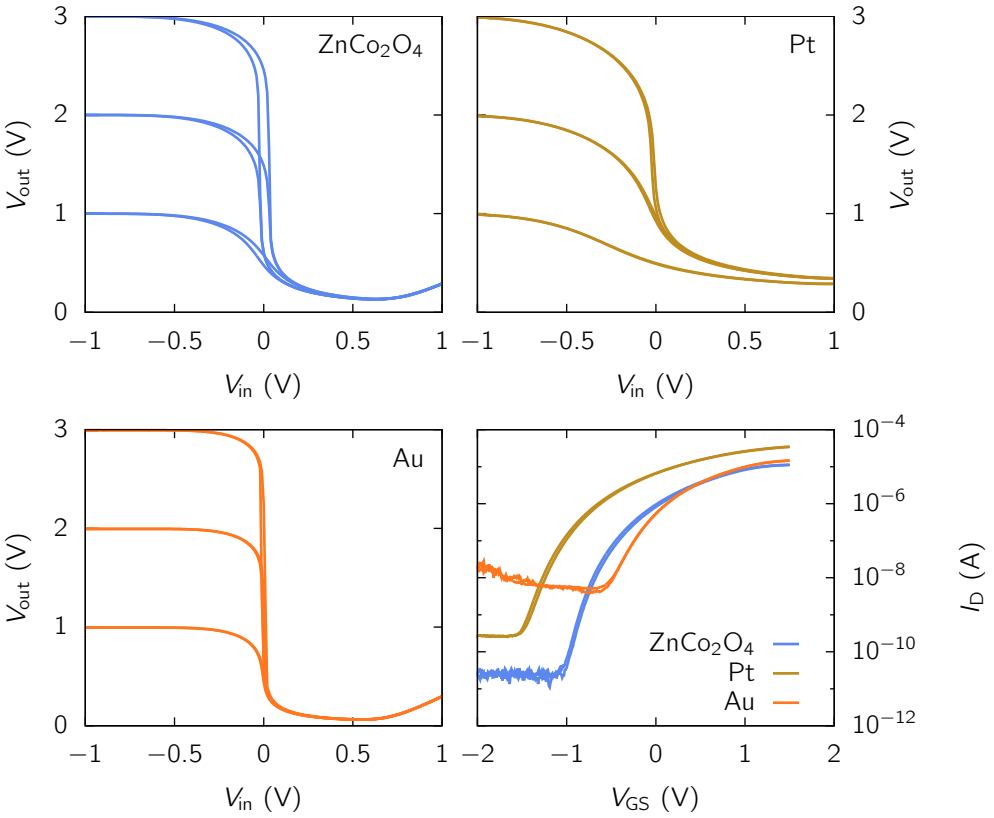

Figure 3.27.: Characteristics of simple inverters with different gate realizations, measured for the supply voltages V_{DD} of 1 V, 2 V, and 3 V.

Simple inverter consisting of MESFETs with gates based on reactively sputtered Ag Schottky contacts have been reported [28], also as fully transparent devices with ultra-thin metal gates [81]. Due to the low cutoff frequency of such transistors discussed in the previous section, simple inverter structures for this work have been realized with MESFETs incorporating Au and Pt gates and with JFETs using $ZnCo_2O_4$ gates. The inverter characteristics are displayed in Fig. 3.27, together with the transfer curves of the input transistors. The gain of the inverters is presented in Fig. 3.28. A comparison of inverter and transistor transfer characteristics reveals, that the ON/OFF-ratio of the transistors, and hence the gate leakage current, has no decisive influence on the steepness of the inverter characteristic. Although the FET with Au gate presented here had an ON/OFF-ratio of barely 1000, the corresponding inverter exhibited the highest gain with basically no shift of the gain maximum from $V_{in} = 0$ V. The Pt MESFETs had a typical ON/OFF-ratio of about 5 orders of magnitudes, and a threshold voltage of about -1.5 V, compared to -0.5 V for MESFETs with Au gates. The difference in V_T between the MESFETs is unexpected, as the channel layers were simultaneously deposited and

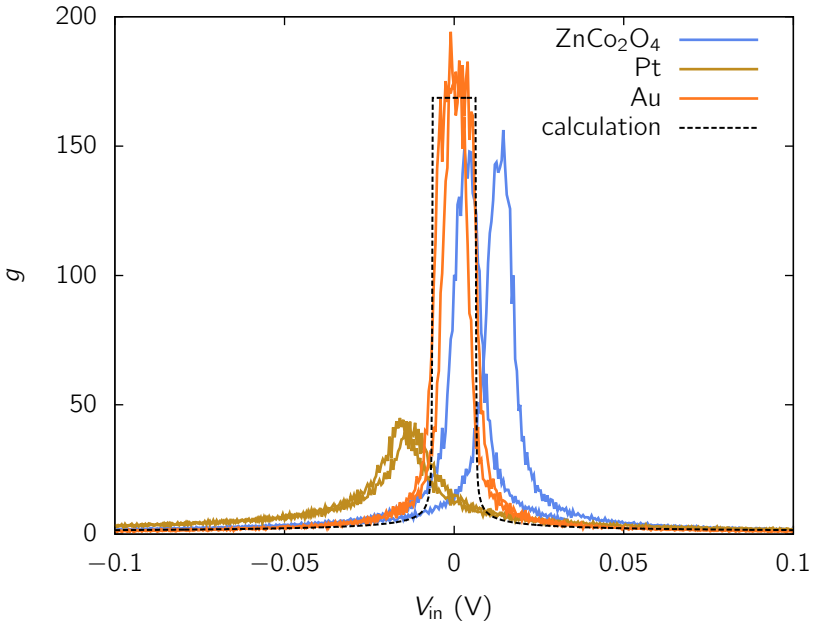

Figure 3.28.: Gain of inverters with different gate materials. The calculation for the inverter with Au gates was based on Eqns. 3.41 and 3.43.

are thus nominally identical. The transistor ON-currents indicate either a difference in the film thickness or the conductivity, however both Hall-effect and ellipsometry measurements conducted after deposition yielded similar properties. Thus, the difference was most probably introduced during sample processing. The larger threshold voltage for the Pt MESFET explains the small gain and the more rounded curve shape of the Pt inverter characteristic compared to the other devices. As illustrated by Fig. 3.7 V_{DD} must be larger than $2|V_T|$ to reach the maximum gain, which is then only determined by the saturation currents of both input and load transistor. Thus, threshold voltages close to zero are favorable to reach high gain values. Fig. 3.28 demonstrates, that the slope of a real inverter is successfully described by Eqns. 3.41 and 3.43. The parameter $\alpha \approx 10^{-8}$ S was determined by a linear fit of the MESFET's output characteristic in saturation at $V_{GS} = 0$ V.

The input voltage at which the highest gain occurs can be shifted by using different gate widths for input and load transistors. For an estimation of the shift, the current conservation equation must be solved. It is not feasible to use Taylor expansions as performed in section 3.1, as the validity would be limited to input voltages very close to zero. For a rough approximation the simplified equation for the FET saturation current, Eqn. 3.20, can be used. Then, the saturation current for both FETs is equal for the input voltage

$$V_{in} = V_T \left(1 - \sqrt{\frac{W_{load}}{W_{input}}}\right). \tag{3.52}$$

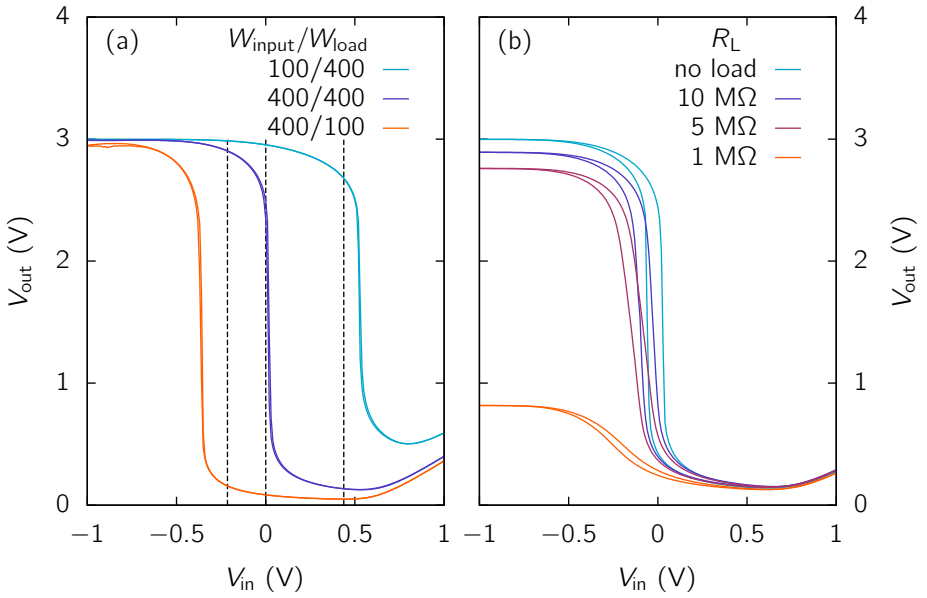

Figure 3.29.: (a) Characteristics of simple inverters with varying gate widths. V_{DD} was 3 V. The black dashed lines show the estimation of the voltage shift according to Eqn. 3.52. (b) Characteristics of a simple inverter with load at the output. R_L connected the output contact and ground. V_{DD} was 3 V. The saturation current of the load transistor was 0.6 μA.

The experimental verification is presented in Fig. 3.29(a). Eqn. 3.52 underestimates the shift of the input voltage, but exhibits a qualitative agreement with the measurements.

All inverter characteristics so far were recorded by a voltage measurement unit with high input impedance ($\geq$ 10 GΩ according to Agilent 4155C users guide). If a load with input resistance R_L in the range of $V_{DD}/I_{D,sat}^{load}$ or below is attached at the inverter output, the current conservation through input and load FET does not hold anymore. For low input voltages the maximum output voltage will be less than V_{DD}, due to the current through R_L. Also the maximum gain will decrease. The inverter characteristics for an inverter with $V_{DD}/I_{D,sat}^{load}$ = 5 MΩ and varying load resistances is shown in Fig. 3.29(b). The sensitivity of the inverters to load resistances must be considered when measuring the output voltage with oscilloscopes, which often have input impedances in the MΩ range. For measuring the undisturbed inverter output an impedance converter must be applied between inverter and oscilloscope.

With impedance converter and oscilloscope the response of V_{out} to sinusoidal input voltages at different frequencies was determined. Fig. 3.30(a) illustrates, that the cutoff frequency f_c is inversely proportional to the maximum gain reached for the respective gate material. The inverter with Au and $ZnCo_2O_4$ gates, both exhibiting a maximum

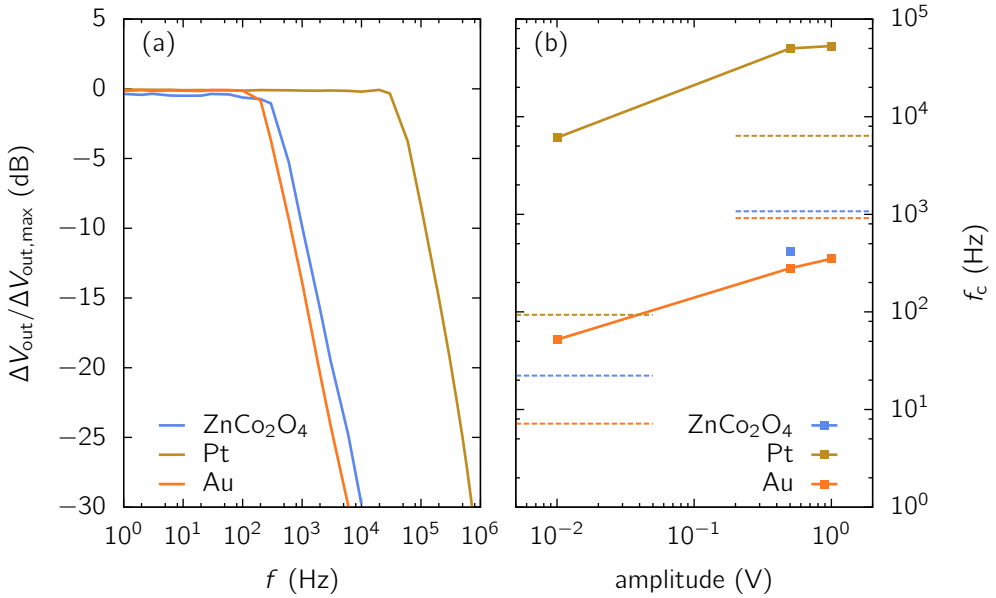

Figure 3.30.: Response of the output voltage to sinusoidal input voltages. (a) V_{out} response depending on the frequency, measured around $V_{in,0} = 0$ V with an amplitude of 0.5 V. (b) Cutoff frequency f_c in relation to the amplitude of the input signal. The solid lines are a guide for the eyes. The dashed lines are estimations for the small and large signal cases according to Eqns. 3.53 and 3.54. Both estimations are based on linear fits of the FET output characteristics, in saturation and close to $V_{DS} = 0$, respectively

gain around 150, have a cutoff frequency below 1 kHz for an amplitude of 0.5 V. The Pt inverter with gain below 50 reaches a cutoff frequency in the range of 50 kHz for the same amplitude. Fig. 3.30(b) shows f_c for different amplitudes. For the smallest amplitude of 0.01 V f_c is about 10 times smaller than for 1 V. An important paramter for the frequency behavior is probably the capacitance between the input and output contacts, which must be recharged through the transistor currents on each change of the input voltage. QSCV measurements yielded for all gate materials a capacitance $C_{in/out} \approx 400$ pF. This is significantly higher than the gate capacitance measured for single transistors, usually in the range of 10-20 pF for FETs of similar size. For small amplitudes both FETs in the inverter are in saturation, and their differential resistance is given by $1/\alpha$. This leads to small signal limit of

$$f_{c,ss} = \frac{2\alpha}{2\pi C_{in/out}}. \tag{3.53}$$

For input voltages far away from zero, one of the FETs is in saturation and the other in the linear regime. The FET in the linear regime should dominate the recharging of $C_{in/out}$, because of its much smaller differential resistance. The derivation of I_D for V_{DS}

close to zero is equal to $g_{\max}$ (see Eqn. 3.17), which gives an estimate for the large signal cutoff frequency

$$f_{\mathrm{c,ls}} = \frac{g_{\max}}{2\pi C_{\mathrm{in/out}}}. \tag{3.54}$$

These estimates are depicted in Fig. 3.30(b) by dashed lines. For Pt and $ZnCo_2O_4$ gates the calculated limits envelope the measured values. f_c of the inverter with Pt gates is underestimated by a factor of about 10. Nevertheless, the calculations predict correctly a significantly higher cutoff frequency. So far, the reason for the low f_c compared to the single transistors is not clear, especially concerning the difference between $C_{\mathrm{in/out}}$ and the FET's gate capacitance. Further examinations will be neccesary to determine other capacitances in the circuit and simulations would be desirable to obtain better estimations for the frequency behavior.

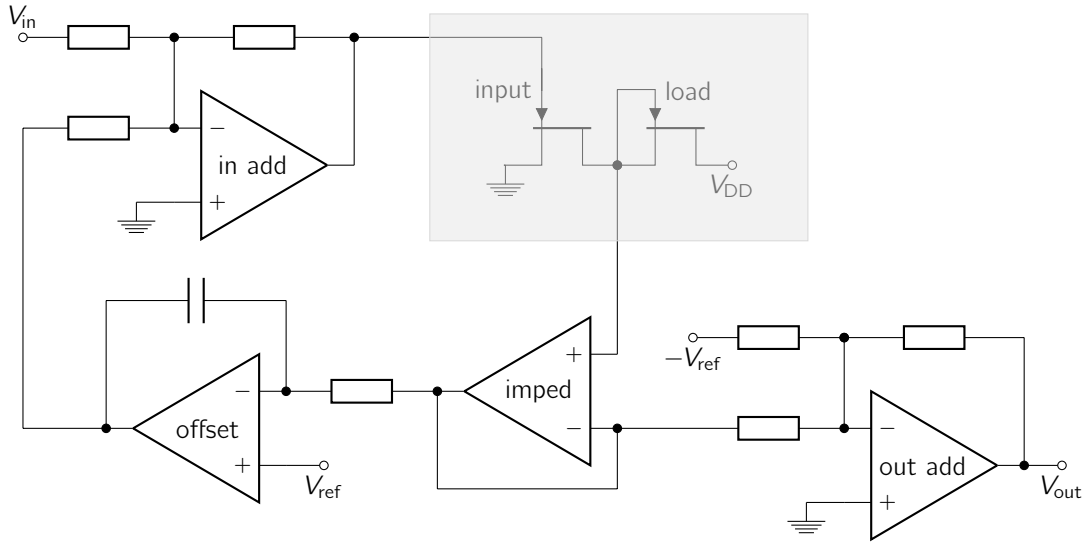

Figure 3.31.: Measurement circuit for small signal measurements with simple inverters (gray box). The input voltage is shifted by the offset correction circuit, so that the inverter's average output voltage is always at V_{ref}. The last stage subtracts V_{ref} from the output, yielding a signal around 0 V which can be measured with an oscilloscope. All resistors in the actual circuit had a value of 10 kΩ, the capacitance was 22 μF. Two Linear Technology LT1112 dual op-amps were used for the circuit.

The use of simple inverters as amplifying circuits for small signals is complicated by the narrow input voltage range where high gain is obtained. The point of maximum gain is usually close to $V_{\mathrm{in}} = 0$ V, but has often an offset of several ten millivolts. To facilitate the adjustment of the input voltage, an electronic circuit was developed, which shifts the offset voltage of any applied signal until the ouput voltage of the inverter equals a given reference voltage V_{ref}. For $V_{\mathrm{ref}} = V_{\mathrm{DD}}/2$ this is very close to the working point of

maximum gain. The circuit is depicted in Fig. 3.31 and comprises four op-amps. The first op-amp works as analog adder ('in add'), which adds the input voltage V_{in} and the offset correction voltage, and gives the inverted signal as input for the simple inverter (in the gray box). The output of the simple inverter is fed into an impedance converter ('imped'), to avoid an alteration of the inverter characteristic by a too large output current. The offset correction circuit ('offset') compares the inverter's output voltage to V_{ref} and outputs a correction voltage, which will shift the inverter's input voltage until the output voltage equals V_{ref}. The large capacitance at the offset op-amp works as low-pass filter, so that only the dc part and very slow voltage changes are corrected. Signals with $f > 10\ Hz$ will pass unaltered from V_{in} to V_{out}, only modulated by the inverters transfer characteristic. The ouput adder ('out add') subtracts V_{ref} from the inverter's output voltage, in order to obtain a final output voltage V_{out} around zero volt, which allows a better resolution when measuring with an oscilloscope. The circuit was built by Agnes Holtz in the framework of her master's thesis and successfully tested. The usage of an Agilent 4155C for providing the dc voltages V_{DD}, V_{ref}, and $-V_{\mathrm{ref}}$ and a TiePie HS3 oscilloscope for the voltage measurements resulted however in strong 50 Hz oscillations of the output, which made the evaluation of input signals with amplitudes below 1 mV impossible. With suitable decoupling of the voltage sources, this circuit could be a valuable tool for the examination of inverters at the working point of maximum gain.

3.5. Test Circuit for Active Matrix Configurations

The integration of amplifying circuits on a MEA chip would be beneficial, when further signal processing steps are performed on the chip. As every electronic component adds to the noise of the signal, amplification directly at the electrode would be desirable to sustain the best possible signal-to-noise ratio. An important example for on-chip signal processing is the multiplexing of several input signals to a common measurement line. This way, higher electrode numbers and densities can be achieved. The electrodes can be organized in a matrix, where the columns are connected by common measurement lines, and the rows by the selector lines, which control whether the input signals of the row are connected to the measurement line. As the electrodes are not connected by individual lines, the number of neccessary conduction paths scales with $\sqrt{N}$ instead of N for directly connected electrodes, where N is the total number of electrodes. However, only electrodes from single rows can be measured simultanously. For quasi-simultanous measurements, fast scanning through the rows must be employed, with demultiplexers at the measurement lines to recover the individual electrode signals.

For a proof-of-principle of this concept for ZnO MESFET based devices, the test circuit presented by Fig. 3.32 was realized. Two identical cells, each representing a measurement site on the chip, are connected to a common measurement line (V_{meas}), and can be

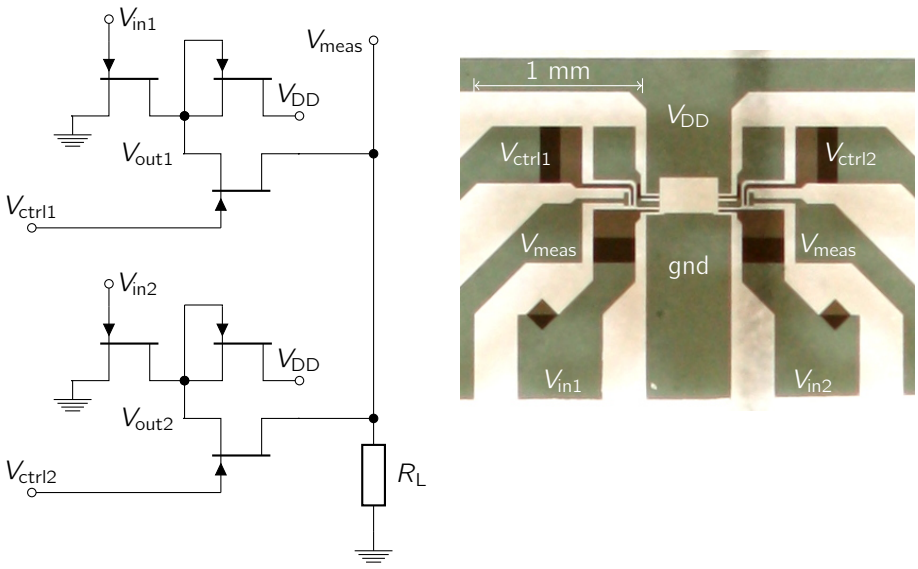

Figure 3.32.: Test circuit for an active matrix configuration of simple amplifiers with row adressing. On the right side an optical micrograph of the circuit is shown, where dark areas are metallized. The 3-transistor cells have an area of about 32000 μm^2. In the actual circuit the V_{meas} contacts and the resistor R_L must be connected externally.

controlled individually by selector lines (V_{ctrl1},V_{ctrl2}). A cell consists of a simple inverter, working as on-site amplifier, and a transistor for the signal selection. Fig. 3.33(a) shows the transfer characteristics of one cell for different selector voltages V_{ctrl}. For high V_{ctrl} the inverter characteristic with high gain at $V_{in} = 0$ V is reproduced. At negative voltages a linear dependence of the measured voltage on V_{in} is observed, instead of the intended constant output. With only a high ohmic measurement device at the measurement line the selection transistor has no defined source voltage, and no proper OFF-state can be reached. Thus, an additional load resistor R_L was introduced between the measurement line and ground. The characteristics for $R_L = 1$ MΩ are shown in Fig. 3.33(b). Due to the load the gain is dimished, as described in the previous section. However, the input signal is now properly separated from the measurement line, when negative V_{ctrl} are applied. In this configuration a test with both cells was performed. At the inputs two sinusoidal signals with different frequencies were applied. At the selector lines, rectangular pulses with a higher frequency connected the cells alternately to the measurement line, separated by phases where both signals were turned off. The measured voltage is presented in Fig. 3.34. The signals from the individual inputs can be clearly separated, which demonstrates the correct operation of the circuit. However, the gain for both signals is less than 2, due to the load introduced by R_L. By increasing R_L it should be possible to find a configuration, where both high gain and proper separation

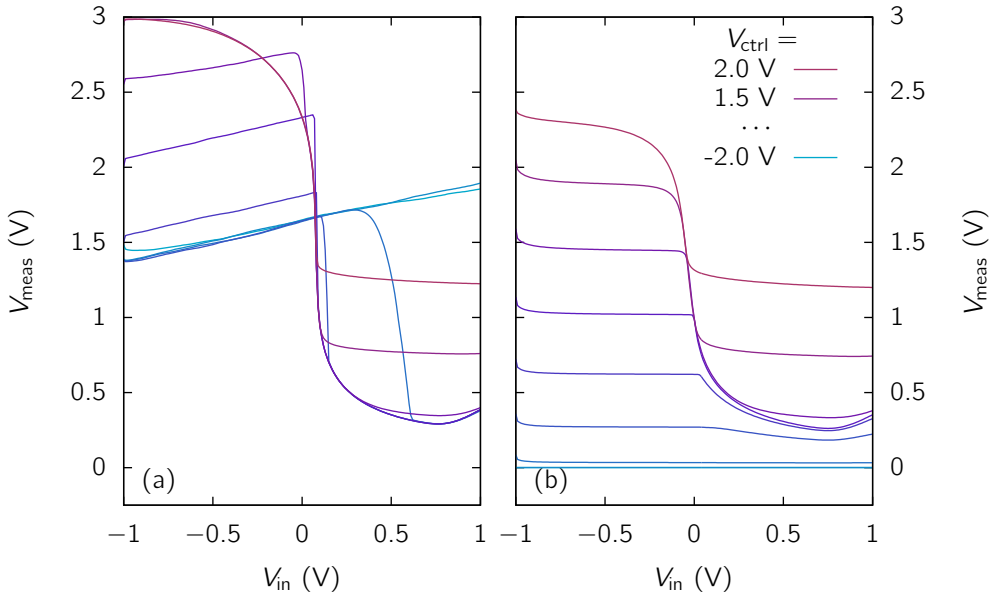

Figure 3.33.: Measurement of the inverter characteristics at V_{DD} = 3 V, including a control transistor at the output. The load resistor R_L at the measurement line was not present in (a) and 1 MΩ in (b).

from the measurement line are realized. The comparably low switching speed of the inverters as described in the previous section must also be increased for the application of the concept presented here. These issues were not addressed further within this work. Proof-of-principle measurements with MEAs based on single ZnO transistors must be successfully conducted before more involved on-chip circuits are implemented.

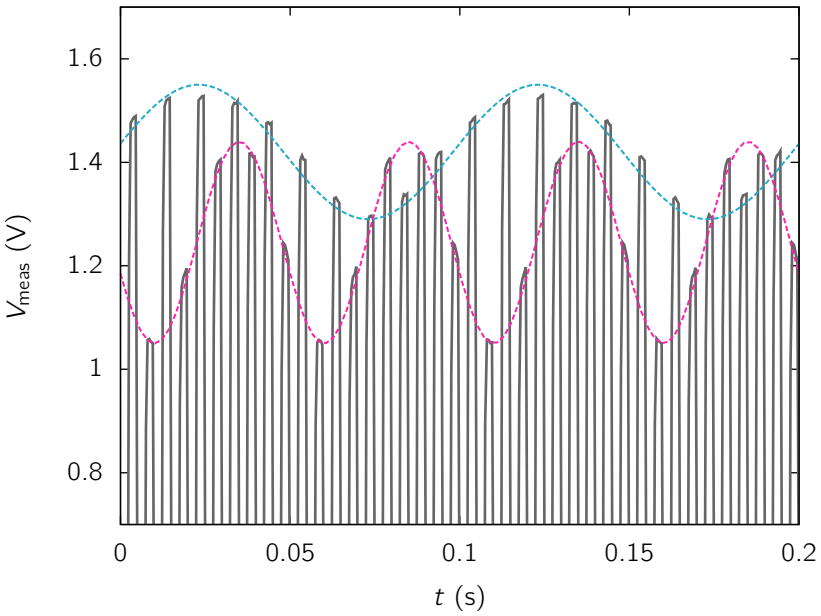

Figure 3.34.: Proof-of-principle measurement for the active matrix test circuit. At both inputs sinusoidal signals with peak-to-peak amplitude of 100 mV were applied, with 10 Hz and 20 Hz respectively. The control transistors were switched with a frequency of 100 Hz, alternating between 2.5 ms in the ON-state and 7.5 ms in the OFF-state. Note, that the output was measured with a single oscilloscope channel. The dashed lines are a guide for the eyes, representing the reconstructed output signals of the two cells.

4. Noise

4.1. Noise Sources

Statistical fluctuations of measured quantities are generally called noise. Typical reasons for such fluctuations when measuring voltage or current are the thermal motion of charge carriers or trapping and detrapping effects in semiconductors. Also the finite size of the elementary charge can lead to noise, revealing the "granular" nature of electrical currents.

The course of fluctuations due to a random process cannot be described by a function dependent on time. However, by statistical examination of the process information about correlations between an event to a time t and a time $t + \tau$ can be attained. This is decribed by the autocorrelation function

$$\rho(\tau) = \overline{a(t)a(t+\tau)} = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{+T} a(t)a(t+\tau)\mathrm{d}t \tag{4.1}$$

for a quantity $a(t)$ fluctuating around zero, i.e. $\overline{a} = 0$.

The autocorrelation function can be used to calculate the power spectral density

$$S(f) = \int_{-\infty}^{+\infty} \rho(\tau)\mathrm{e}^{-2\pi i f\tau}\mathrm{d}\tau. \tag{4.2}$$

The power spectrum for different noise sources can have discriminative frequency dependence or magnitude, and hence be used for an analysis of the measured noise. In this section the most important noise sources for semiconductors are outlined, generally based on Müller [82] and Hooge [83].

4.1.1. Thermal Noise

The thermal energy of charge carriers results in a noise contribution which is even present in equilibrium conditions. The thermal motion of the carriers leads to randomly fluctuating currents in a conductor and to potential fluctuations at the surface. Under

the assumption that the thermal energy of $k_{\mathrm{B}}T/2$ per degree of freedom of each particle is totally contained in kinetic energy, the current power spectral density of a conductor with conductance G can be calculated using Drude's model to be (see e.g. [84, 85])

$$S_I(f) = 4k_{\mathrm{B}}TG. \tag{4.3}$$

It should be noted, that in equilibrium only thermal noise can be measured directly, regardless of other noise sources present in the device. A method to observe conductance fluctuations under equilibrium conditions, which often cause 1/f noise in non-equilibrium, is the analysis of fluctuations in the current noise spectrum S_I, which could be expressed by S_{S_I}.

4.1.2. Shot Noise

Electric current consists of carriers with the electric charge q. Thus, when measuring the charge flow through a certain area, fluctuations due to the statistical crossing of the single carriers will be observed. The resulting noise density is called shot noise and given by

$$S_I(f) = 2qI. \tag{4.4}$$

In a semiconductor shot noise is typically oberved at potential barriers, as in a bulk semiconductor injected charge carriers usually recombine before reaching the second electrode [82]. This can be expressed by an effective charge $q_{\mathrm{eff}} = e\overline{v}\tau_{\mathrm{m}}/L$, where $\overline{v}$ is the average velocity, τ_{m} the majority carrier lifetime, and L the distance between the electrodes. q_{eff} is typically much smaller than e, hence the shot noise contribution becomes very small.

4.1.3. Generation-Recombination Noise

In a semiconductor the number of charge carriers N may fluctuate due to transitions between energy bands and trap states, which lead to fluctuations in the conductance G. The spectral noise density is given by a so called Lorentzian power spectrum [86, 83]

$$\frac{S_I}{I^2} = \frac{S_G}{G^2} = \frac{S_N}{N^2} = \frac{\overline{\Delta N^2}}{N^2}\frac{4\tau}{1+(2\pi f\tau)^2}, \tag{4.5}$$

where $\overline{\Delta N^2}$ is the variance of the carrier number and τ a characteristic relaxation time of the trap. The spectrum is constant for $f \ll 1/(2\pi\tau)$ and proportional to f^{-2} for $f \gg 1/(2\pi\tau)$.

4.1.4. Flicker Noise

At low frequencies noise with a power spectral density proportional to $1/f$ is frequently observed, often called flicker noise. Especially in semiconductor based devices this is usually the dominant noise contribution at sufficently low frequencies, where it exceeds the thermal noise. It has been shown, that many parameters like surface and interface properties or crystal quality may influence $1/f$ noise [87, 82]. This leads to the conclusion, that several mechanisms cause $1/f$ noise. Consequently, one has to be careful when applying theoretical models to experimental results, as very different processes might lead to similar behavior.

An often cited model was developed by McWhorter [88], where traps in an insulating layer lead to carrier density fluctuations in an adjacent semiconductor. Under the assumption, that the time constant for the trapping process increases exponentially with the distance from the interface, integration over the insulator thickness leads to $1/f$ noise in the carrier density. It is basically generation-recombination noise for interface traps with a certain distribution of time constants. The frequency range, where the $1/f$ proportionality holds, corresponds to the range of trapping time constants. The McWhorther model is often applied to noise in MISFETs, where channel carriers might interact with traps within the gate insulator, e.g. by quantum mechanical tunneling or more involved processes [87]. The island model by Pellegrini [89] can be understood as generalization of the McWhorter model to arbitrary traps in bulk or surface of a semiconductor. It is based on localized states with discrete energy levels, which exchange charge carriers with the surrounding medium by tunneling or thermally activated processes. Variations in size and nature of these so-called islands cause the wide range of time constants, which is neccessary to produce $1/f$ noise. However, the approach has been criticized by van Vliet and Mehta [90] by general theoretical considerations, reducing its validity to surface states.

In many cases $1/f$ noise in semiconductors can be described by the empirical relation introduced by Hooge [91]

$$\frac{S_I}{I^2} = \frac{S_V}{V^2} = \frac{S_R}{R^2} = \frac{\alpha_{\mathrm{H}}}{Nf}, \tag{4.6}$$

where $N = nV_0$ is the total number of carriers in a volume V_0 with the charge carrier density n. For the dimensionless constant α_{H}, often called Hooge constant, values between 10^{-4} and 2×10^{-3} were found in a group of about 20 semiconductors [83]. The narrow range of observed α_{H} values was often interpreted as indication for an universal process underlying the measured $1/f$ noise. In an extensive review by Hooge *et al.* [87], experimental evidence for $1/f$ noise in the electron mobility is presented, in contrast to the carrier fluctuations caused by trapping effects. The proposed source of $1/f$ noise is the lattice scattering of electrons, as other scattering processes seemed not to contribute.

The presented experiments follow the relation

$$\alpha_{\mathrm{H,meas}} = \left(\frac{\mu}{\mu_{\mathrm{lattice}}}\right)^2 \alpha_{\mathrm{H,lattice}}, \tag{4.7}$$

where μ is the electron mobility, μ_{lattice} the hypothetical mobility in case only lattice scattering was present, and $\alpha_{\mathrm{H,lattice}}$ a value around 2×10^{-3}. However, the question about the microscopic origin of the $1/f$ noise caused by lattice scattering was not answered. It should be noted here, that $\mu < \mu_{\mathrm{lattice}}$ leads to small values for $\alpha_{\mathrm{H,meas}}$ when Eq. 4.7 is applied. Therefore small $\alpha_{\mathrm{H,meas}}$ values are not automatically a sign for good material quality, as often stated. For comparison the scattering mechanisms in the examined material should be taken into account.

Handel [92] derived $1/f$ noise from the interaction of scattered charges with the vacuum electromagnetic field in the infrared, which leads to corrections in the scattering cross sections. This approach is called quantum $1/f$ noise. Comparison of noise measurements with calculations based on this work seemed promising [93]. However, the derivation of the quantum $1/f$ noise has been severely criticized. Van Vliet [94] stated several major problems in the original calculation, but presented an own derivation based on quantum electrodynamics. It confirms the generation of $1/f$ noise, but predicts very low α_{H} around $10^{-6} - 10^{-9}$. Such values have been found in small and high quality semiconductor devices. Higher α_{H} are very likely not based on quantum $1/f$ noise.

For metals the scattering at mobile impurities [95] or the diffusion of atoms at grain boundaries [96] have been suspected to cause 1/f noise. For semiconductors these effects are probably not relevant at room temperature, only one possible case has been reported for GaAs at low temperatures [83].

Summing up, for several experiments the origin of $1/f$ noise could be identified, and in many other cases theoretical models have been proposed. However, to test the applicability of such a model a thorough knowledge of the sample properties, and the ability to vary parameters like mobility or doping density independently and in controlled fashion, are neccessary. Even then it can be challenging to reach the required accuracy for acceptance or rejection of a model. Hooge [83] reports, that even with high quality n-GaAs samples from the same wafer a spread in α_{H} of a factor 5 was found. For samples from different wafers or even different research groups the spread is even higher. This demonstrates, that often only an agreement in the order of magnitude can be aimed for when comparing experimental results with each other or with theory.

4.2. Contributions from Measurement Setup

4.2.1. Operational Amplifier Noise

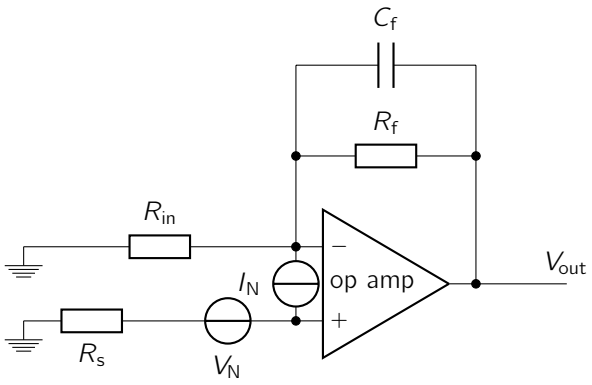

Figure 4.1.: Equivalent circuit for the noise calculation of an op-amp amplifier with low-pass filter.

An operational amplifier (op-amp) is a four-terminal device, so two independent noise sources are needed to describe the characteristics in an equivalent circuit. Techncial datasheets often give an input noise current I_N and an input noise voltage V_N for the noise characterization. The equivalent circuit for an inverted amplifier with those quantities is depicted in Fig. 4.1. Additionally the resistors contribute thermal noise. Feedback capacitor and resistor form a lowpass filter with cutoff frequency $f_c = 1/(2\pi R_f C_f)$, which has also an impact on the output noise. It must be considered, that noise at the positive input of the op-amp will be amplified according to a noninverting amplifier. This leads to an amplification $G = 1$ for noise at frequencies $f \gg f_c$, while the amplification of a signal at the negative input goes to zero.

The total output voltage noise density in V^2/Hz is:

$$S_V = [V_N^2 + 4k_B T R_{eq} + (R_{eq} I_N)^2] \, (1 + \frac{R_{ff}}{R_{in}})^2, \tag{4.8}$$

with

$$R_{ff}(f) = \frac{R_f}{\sqrt{1 + (f/f_c)^2}} \tag{4.9}$$

and

$$R_{eq}(f) = R_s + \frac{R_{in} R_{ff}(f)}{R_{in} + R_{ff}(f)}. \tag{4.10}$$

4.2.2. Characteristics of the MEA Amplifier

The measurement of current noise can be challenging as it is often modulated on a comparably high offset current. This offset must be cancelled out to record the noise with a sufficient resolution. The amplifier setup described in section 2.3 for measurements with electrolyte and living cells on MEA chips performs such an offset cancellation and thus was used also for noise characterization of semiconductor materials and devices.

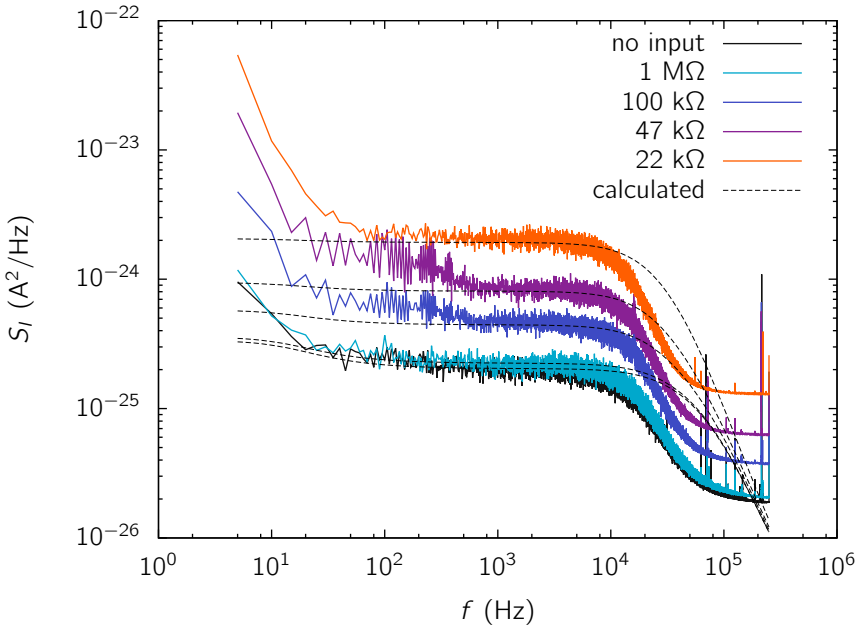

Figure 4.2.: Noise characterization of the MEA amplifier using metal film resistors as test devices and zero bias voltage. The oscilloscope output was divided by the overall amplification to get the equivalent input current noise. For the calculations the noise from the input resistors and from stage 1, stage 2, and inverter stage as denoted in Fig. 2.8 was taken into account.

The noise contribution of the amplifier circuit has been modeled using Eqn. 4.8 for each of the amplifier parts denoted in Fig. 2.8 (i.e. stage 1, stage 2 and the inverter circuit). The input resistance R_{in} of stage 1 is determined by the device under test (DUT). The ratio $R_{\mathrm{f}}/R_{\mathrm{in}}$ determines the amplification of the op-amp noise quantities V_{N} and I_{N} as well as noise coupling into the positive input of the op-amp, e.g. from a voltage source. For that reason the noise contributions of stage 1 are not fixed in their absolute value, but depend on the conductance of the DUT. The noise contributions of stage 2 and the inverter stage do not depend on the DUT.

The power density spectra of metal film resistors as DUT are presented in Fig. 4.2. The voltage noise measured with an oscilloscope was divided by the amplification factor

$(R^{(1)}_{\mathrm{feedback}} R^{(2)}_{\mathrm{feedback}} / R^{(2)}_{\mathrm{in,signal}})^2$ in order to scale it to the level of the input current noise. The dashed lines show the calculated noise spectra, which match the measurements very well in the constant part. The increase in the measured spectra below 20 Hz originates from the signal generator used to set the bias voltage V_d. A second order lowpass filter has been added between voltage source and amplifier to suppress this noise contribution, but the shoulder of the filter is still visible. A lower edge frequency of the lowpass filter would lead to stronger damping, but would increase the waiting time, before the steady state is achieved after a voltage change, to several minutes.

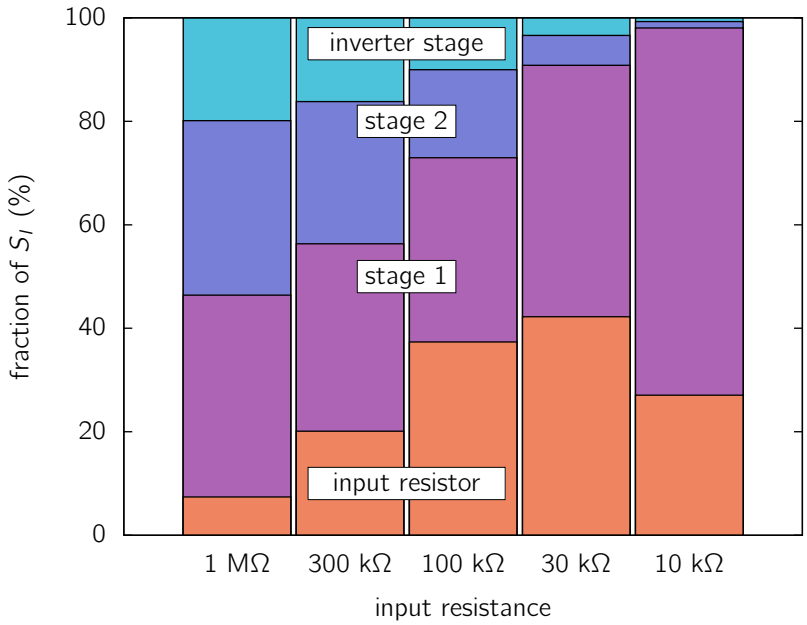

Figure 4.3.: Contributions to the total noise output of the MEA amplifier around 1 kHz, depending on the input resistance. Metal film resistors were used as DUT. The absolute values of S_I contributed by stage 2 and inverter stage are constant.

The composition of the total noise level in the constant regime around 1 kHz is illustrated by Fig. 4.3. As mentioned before, stage 2 and inverter stage contribute a noise level that is constant in absolute numbers. The thermal current noise of the DUT increases with decreasing resistance, but also the other noise sources of stage 1 gain power due to increasing amplification. The ratio between the current noise of the DUT and the other noise contributions from stage 1 can be calculated from the op-amp noise equations presented above. It exhibits a maximum at

$$R_{\mathrm{in,max}} = \sqrt{\frac{R_\mathrm{f}^2 V_\mathrm{N}^2}{V_\mathrm{N}^2 + 4 k_\mathrm{B} T R_\mathrm{f}}}. \tag{4.11}$$

Using the amplifier specifications implemented for this work yields $R_{\mathrm{in,max}} = 53$ kΩ. This input resistance would lead to a minimal influence of the amplifier noise on the signal-to-noise ratio when considering thermal noise. The ZnO channels used for the fabrications of MEAs had in most cases resistances between 50 kΩ and 100 kΩ, close to $R_{\mathrm{in,max}}$. The results presented in the following sections show, that the $1/f$ noise of ZnO-based devices usually exceeds both thermal and amplifier noise by far, rendering these mostly negligible. Nevertheless, it should be kept in mind, that the amplifier sets a lower limit for the signal-to-noise ratio.

4.3. Homogenous ZnO Samples

4.3.1. Literature on Noise in ZnO-based Samples

The first time noise in ZnO samples has been mentioned in literature (to the best of our knowledge) was in 1967 by Anderson and van Vliet [97]. They examined rod-like single crystals with diameters between 70 μm and 250 μm and observed $1/f$ noise for undoped samples in the observed range between 1 Hz and 100 kHz. They attributed it to surface traps according to the McWhorter model, but without clear arguments against an origin from the bulk. More results from lithium doped samples are presented, but difficult to compare with other samples, as additional features in the noise spectra are introduced and the doping densitiy is not known. From the 1980s on reports on conduction mechanisms and low frequency $1/f$ noise in ZnO varistors have been published [98, 99, 100]. In this polycrystalline samples the grains are seperated by double Schottky barriers, which cause the non-ohmic behavior. The first of the cited papers argues, that the noise stems from the forward biased diodes, but makes no further assumptions concerning the actual origin. The second paper assumes mobility fluctuations as suggested by Hooge *et al.* [87], without further experimental evidence. The third uses the island model by Pellegrini [89] to explain the observed noise spectra, whose validity has been doubted (see section 4.1.4).

In the last decade many results on ZnO thin films and nanostructures have been published, which include noise measurements in some cases. Always $1/f^{\gamma}$ noise with $\gamma \approx 1$ has been observed as dominant noise source at low frequencies. For sputtered ZnO thin films on glass and Pt/Si substrates a decrease in the noise level with increasing substrate temperature during deposition was observed, attributed to improving crystal quality [101, 102]. Ke *et al.* [103] measured $1/f$ noise on e-beam evaporated ZnO films on Si as function of the annealing temperature and determined extremely low values for α_{H} between 4×10^{-9} (400°C) and 2×10^{-5} (700°C). However, it seems they used a formula for resistance noise for the evaluation of the voltage noise measured, which would explain the unrealistic results and casts doubt on their conclusions. MBE grown films on

a-sapphire were fabricated by Chang *et al.* [104] at 430°C growth temperature. After annealing at 700°C in oxygen atmosphere ohmic Ni/Au contacts were deposited for the use as photoconductive sensor. They report $1/f$ noise below 100 Hz with $\alpha_{\mathrm{H}} = 2 \times 10^{-3}$.

For thin film transistors based on amorphous IGZO [105] and polycrystalline ZnO [106] noise characterizations have been reported. The values for α_{H} range between 0.1 and 2 and seem to decrease with increasing annealing temperatures, explained by improved crystal quality. The measurements are always presented for the complete transistor structure, making a seperation of effects from the bulk channel material and from interface or insulator traps difficult.

4.3.2. Thin Films

Before studying the noise characteristics of actual devices, ZnO samples with ohmic contacts were investigated. A constant cross section along the direction of current flow is important to achieve homogenous current densities. Only for such samples Eqn. 4.5 for generation-recombination noise and Hooge's formula for $1/f$ noise (Eqn. 4.6) can be applied directly, at least when material constants independent of the geometrical constraints are to be determined. Channels were etched from ZnO thin films on a-sapphire, grown by PLD at 650°C and 0.02 mbar O_2 using ZnO targets with 0.25wt-% MgO. The film thickness a ranged between 15 nm and 80 nm, similar to those used for FETs. The channels had cuboid shape with width/length ratios W/L of 400 μm/50 μm, 100 μm/50 μm, 30 μm/50 μm, and 30 μm/230 μm. This makes it possible to distinguish between a dependency of the current noise on the channel resistivity, which is proportional to L/W, and on the volume of the semiconductor, proportional to WL. A variation of the film thickness must be considered more carefully, as mobility and carrier density depend strongly on a. This is due to improving crystal quality with increasing distance from the substrate/ZnO interface and due to the doping caused by Al indiffusion from the substrate during growth. The film growth and properties were described more detailed in section 3.2. Ohmic contacts were deposited along two edges of each channel by dc magnetron sputtering of gold.

For the examination of the W and L dependence of the current noise, samples with thickness $a = 27$ nm (determined by spectroscopic ellipsometry), charge carrier density $n = 4 \times 10^{18}$ cm^{-3}, and mobility $\mu = 10$ cm^2/Vs (determined by Hall effect measurements) were fabricated, similar to those used for FETs. The current noise power spectral density for a channel with $W = 30$ μm and $L = 50$ μm is shown in Fig. 4.4, for bias voltages between 0 V and 2.5 V. For 0 V the spectrum is similar to the resistor spectra presented in Fig. 4.2. By fitting with the relation for thermal noise together with the corrections for the setup described in the previous section, a resistance of 87 kΩ is obtained, which is close to the 84 kΩ measured with a multimeter. For non-zero bias

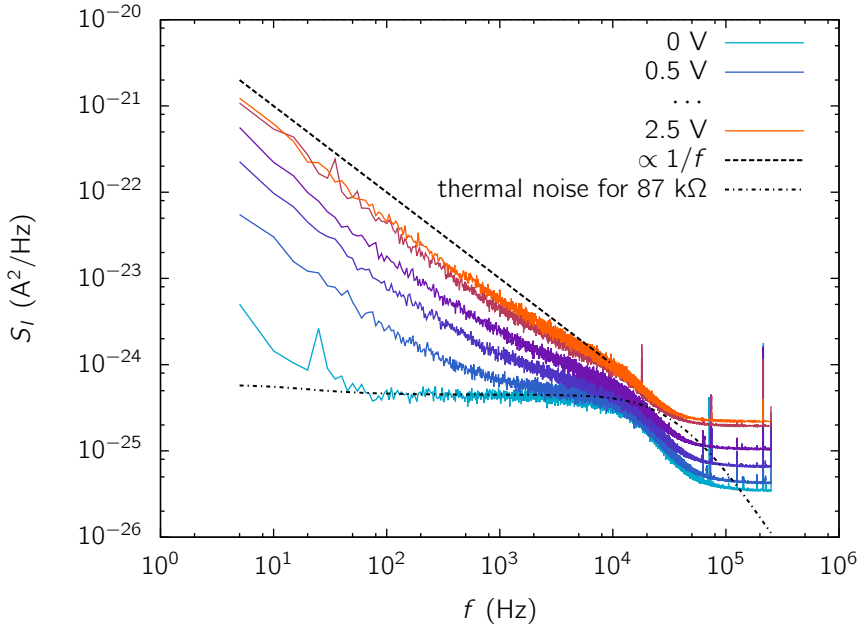

Figure 4.4.: Noise power density spectra of a ZnO channel with a width of 30 μm, length of 50 μm and a layer thickness of 25 nm for bias voltages from 0 V to 2.5 V.

voltage a noise contribution with $1/f$ proportionality becomes dominant. By plotting the power spectral density for a single frequency against the voltage, as shown in Fig. 4.5, the quadratic dependency $S_{I,1/f} \propto I^2$ can be verified. Thus, the complete voltage series can be fitted by the sum of thermal noise $4k_\mathrm{B}T/R$ and $1/f$ noise according to Hooge's formula (Eqn. 4.6), using R and α_H as fit constants. The resistances were also measured by multimeter or I-V measurements. Generally these values agree very well within the accuracy limits.

The Hooge constants α_H determined by fitting the power spectral densities for ZnO channels under bias with Eqn. 4.6 are shown in Fig. 4.6. Regardless of the strongly differing dimensions, nearly all values are around 6×10^{-4}, and no trend concerning resistivity or edge length was observed. One outlier with a 100 times higher constant was measured. Similar behavior was observed with other samples, where arbitrary channels exhibited higher noise levels. Still, always a lower limit for α_H close to 1×10^{-3} was observed. Renewing the contacts from the gold pads to the measurement setup yielded unchanged results. Fig. 4.6 shows, that different contacting methods have no influence on the noise level. Hence, such outliers are most likely caused by disturbances in the bulk material or at the surface of the channels.

Between 1 kHz and 10 kHz the spectral densities at high bias voltages show a flattening, which is not completely described by the addition of the $1/f$ contribution and the constant thermal noise. The evaluation of this deviation is difficult, as it blends with the

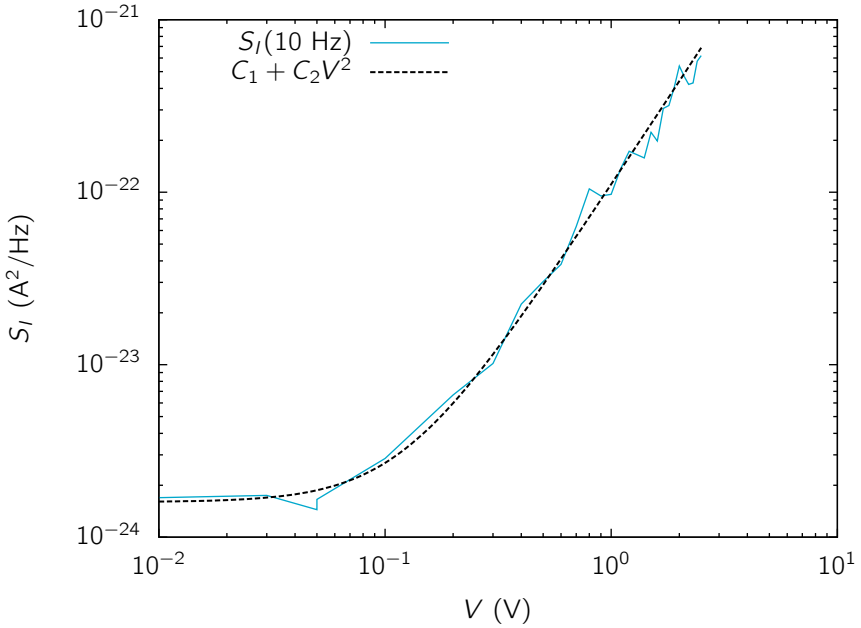

Figure 4.5.: Dependency of the noise power density spectrum of a ZnO channel on the bias voltage. Presented here are the values at 15 Hz for the measurements shown in Fig.4.4.

amplifier cutoff at about 10 kHz. It should be kept in mind, however, as the microwire presented in the next subsection exhibits a similar but more pronounced feature in the same frequency range.

The dependency of the current noise in ZnO channels on the film thickness has been investigated on a series of four samples. After deposition of the thin films, the thicknesses were determined by spectroscopic ellipsometry to be 17 nm, 32 nm, 53 nm, and 71 nm. The electronic transport properties were investigated by Hall effect measurements at room temperature. Results for a similar series of samples were described in section 3.2. After lithographic patterning of the thin films, the resistivity was checked again using a multimeter. By fitting of the thermal noise an additional measure of the resistivity was obtained. Fig. 4.8(a) demonstrates, that the resistivity before and after lithography differs with increasing thickness. Below 30 nm, and hence also for the samples described beforehand in this section, the change is small and can be neglected. For thicker layers, the electronic transport properties change substantially during lithographic patterning. It seems, that the change is dependent on the degree of degeneration of the thin film. For the analysis of $1/f$ noise the knowledge of the carrier density is neccessary. Thus, it was attempted to access this quantity after lithography by using CV measurements. Schottky diodes were fabricated using silver conducting glue, because lithographic methods were not applicable after contacting of the samples with gold wires. For thin layers this method is inaccurate, as the equation used for the evaluation (Eqn. 3.2) is based on an

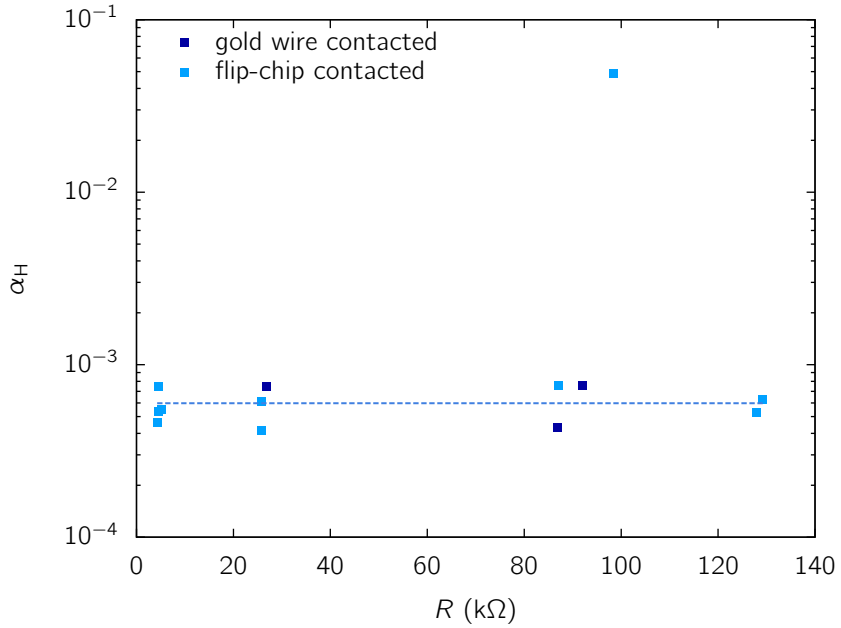

Figure 4.6.: Hooge parameter for current noise in ZnO channels etched from thin films. Shown are results from two samples contacted by different methods. The difference in resistance results from different W/L ratios. The mean value indicated by the dashed line is 6×10^{-4} and does not include the outlier in the upper part of the figure.

one-dimensional model. When both ohmic and Schottky contact are on top of the thin film, the expansion of the depletion layer will be distorted when its width approaches the thickness a. Meaningful results were only obtained for the thickest sample. Depicted in Fig. 4.8(b) is N_D calculated from C, in dependence on the distance d from the surface. d has been calculated from the applied bias voltage using Eqn. 3.1 and the doping density $N_{D,CV} = 8 \times 10^{17}$ cm^{-3}, which is also shown in the graph. Compared to $n_H = 1 \times 10^{17}$ cm^{-3} measured before lithography, the carrier density has increased strongly. The eightfold increase in n explains only half of the change in ρ, which means that also the carrier mobility must have increased.

Fig. 4.8 shows the Hooge constants for the ZnO channels with varying thickness. Most notably, the value for the thinnest and the thickest thin films are very similar, when the carrier density obtained by CV measurement is used. This could indicate an a_H independent on the film thickness a. The values for the intermediate samples are uncertain, because of the unknown transport properties after lithography. Considering the decrease of resistivity, an increase in n and thus also in a_H is probable. This would lead to a maximum of a_H around 50 nm. In any case, the results show, that for thin ZnO layers with $a < 50$ nm the $1/f$ noise is no surface effect. Otherwise it would strongly increase with decreasing a. For layers with $a > 50$ nm the decrease in a_H is most likely due to im-

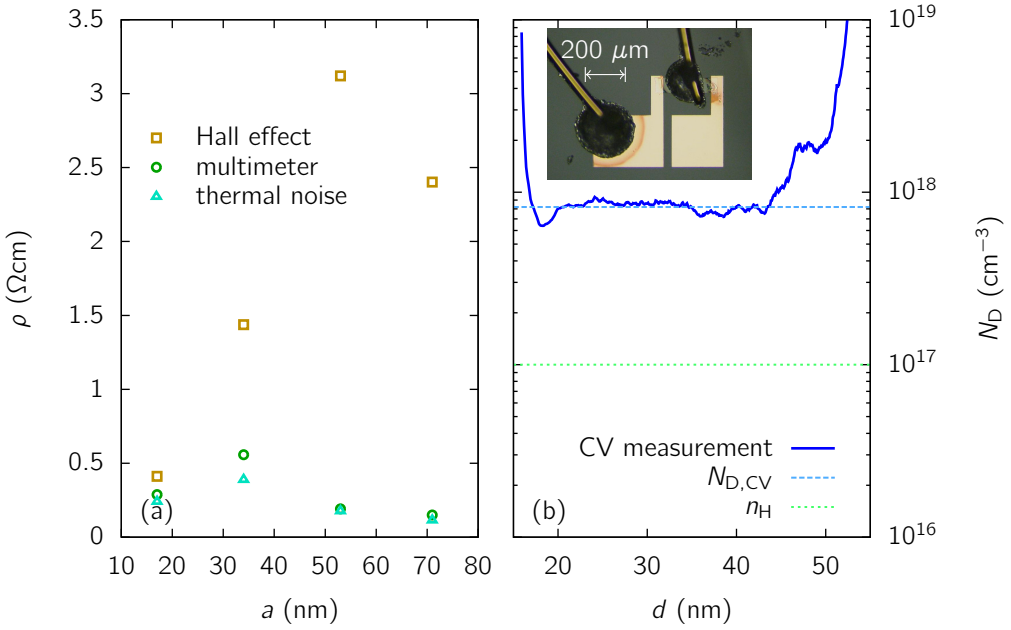

Figure 4.7.: Resistivity of ZnO channels with varying thickness a. (a) Comparison of thin film resistivity (Hall effect) with channel resistivity (multimeter and thermal noise). (b) Charge carrier density for the sample with $a = 71$ nm in dependency on the distance d from the surface. The inset shows the diode for the CV measurement.

proving crystal quality, although surface effects cannot be excluded. As demonstrated in section 3.2, very thin ZnO layers are degenerate, but the room temperature conduction for $a > 50$ nm is not dominated by the degenerate region close to the substrate. This difference could also result in a different coupling of the charge carriers with surface states.

For further examinations a series of sample with better control over μ and n would be desirable. A good choice might be ZnO thin films on glass, as reported by Frenzel *et al.* [50]. The crystalline quality of such films is not as good as on a-sapphire, resulting in lower electron mobility. However, the doping density is not determined by the substrate, and should therefore not be connected to the film thickness a. A series of samples with varying growth temperature could clarify, if a dependence of the noise on the crystal quality exists. Samples with different doping density could be grown by using PLD targets with different concentrations of Al or Ga. An interesting field for examinations would be the transition between the degenerated and non-degenerated regimes. For thin films on a-sapphire this is more involved, as a degenerate layer always exists close to the substrate.

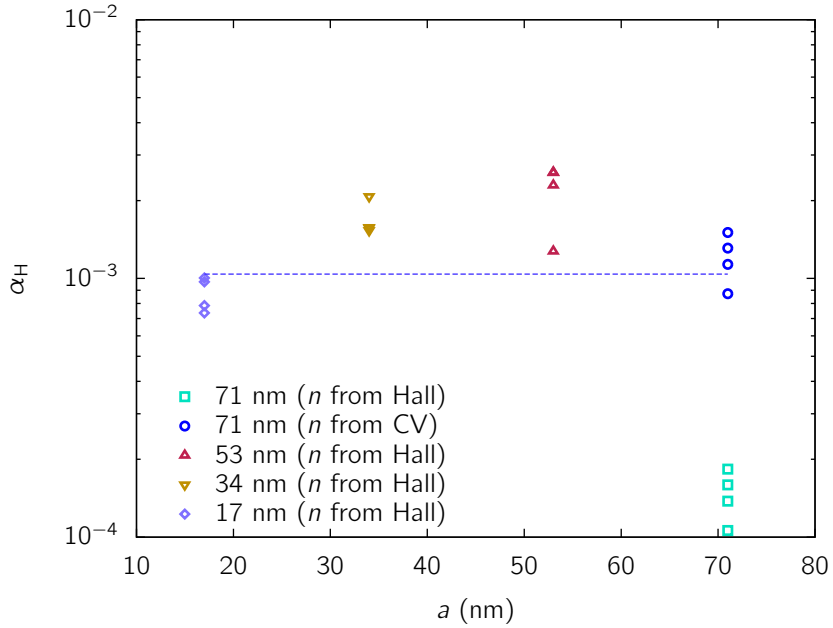

Figure 4.8.: Hooge parameter for current noise in ZnO channels etched from thin films with varying thickness. The dashed line indicates the mean of the values for the thinnest and the thickest sample (n from CV for the thick sample).

4.3.3. Microwires

Heteroepitaxial ZnO thin films always suffer from a high density of structural defects, especially near the susbtrate. Thus, the investigation of single crystals or homoepitaxial films would be useful to seperate the influence of grain boundaries and extended defects on the current noise from impurity and lattice induced mechanisms. As 1/f noise is inversely proportional to the total number of charge carriers, the examined sample must be sufficiently small. The preparation of such samples with defined geometry from bulk ZnO substrates would be challenging. Hence, ZnO microwires were investigated, being experimentally easily accessible samples of high crystal quality and precisely measureable dimensions. A drawback is the difficulty to determine μ and n seperately, as the contacts neccessary for Hall effect measurements require considerable experimental effort. We used nominally undoped ZnO microwires grown by carbothermal vapor-phase transport, as reported by Dietrich *et al.* [107]. In this paper Hall effect measurements on an undoped wire with diameter $d = 16$ μm yielded $n \approx 3 \times 10^{16}$ cm^{-3}, $\mu \approx 4$ cm^2/Vs, and $\sigma \approx 2$ S/m at room temperature. The low mobility is surprising, as in the same work a phosphorus doped microwire showed an electron mobility above 200 cm^2/Vs. C-V measurements on a similarly fabricated microwire gave an estimate of $n \approx 1 \times 10^{16}$ cm^{-3} [108]. Another possibility to determine the mobility in ZnO wires was exploited by Wang *et al.* [109], using a FET based on a carbothermal grown nanowire with $d = 0.14$ μm. The electrical properties were $n \approx 3 \times 10^{17}$ cm^{-3} and $\mu \approx 53$ cm^2/Vs at room temperature, which

gives $\sigma \approx 300$ S/m.

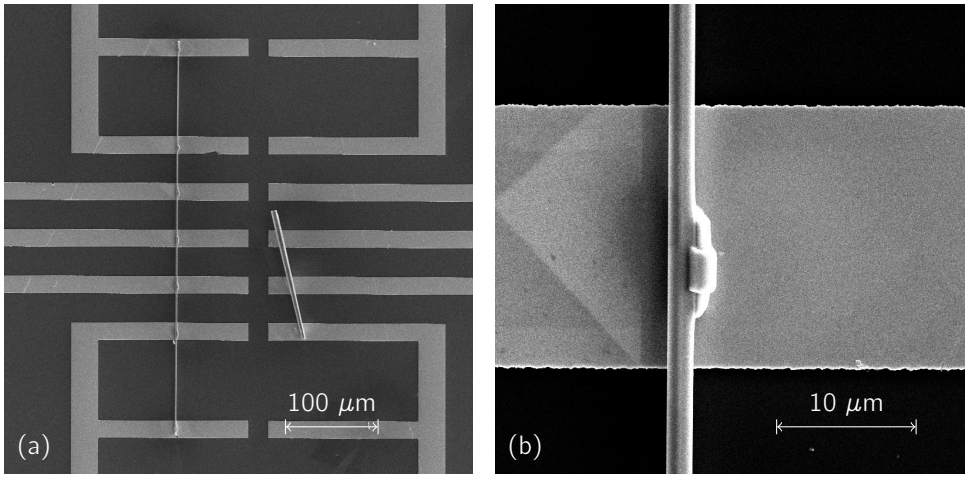

Figure 4.9.: SEM image of contacted ZnO microwires. (a) Overview, the measurements presented below were conducted on the left wire. (b) FIB deposited platinum contact between the left wire and a gold conducting path.

For this work a microwire with $d = 1.5$ μm was placed on a Si substrate with SiO_2 layer and prefabricated Au conducting paths. Pt deposited by a focused ion beam (FIB) was used to ensure good electrical contacts (depicted in Fig. 4.9). Microwire growth and contacting was performed by M. Wille (Universität Leipzig). *I-V* measurements confirmed perfectly ohmic behavior of the contacts and determined a conductivity of $\sigma \approx 150$ S/m. This is much higher than the value stated above for the wire investigated by Hall effect measurement. If a higher mobility would completely account for this difference, it would have to be around 300 cm^2/Vs. As all reported values for μ are lower, the carrier density in our sample was most likely higher than $n \approx 3 \times 10^{16}$.

The sections between the contacts had a length of 30 μm, a surface of 140 μm^2 and a volume of about 50 μm^3. For comparison, the smallest ZnO thin film channels investigated in the previous section had a surface to the air of 1100 μm^2 and a volume of 26 μm^3. If the noise would be dominated by surface traps, the 15 times lower surface/volume ratio of the wire should result in a distinct reduction of the noise level compared to thin films. Similarly, grain boundaries and extended defects as noise sources should affect the microwire much less compared to the textured thin films.

The power density spectra displayed in Fig. 4.10 for $V > 0$ V show $1/f$ dependence at low frequencies, but exhibit a flattening between 100 Hz and 1 kHz. The increasingly negative slope for $f > 1$ kHz is not completely due to the amplifier cutoff, which sets in at about 10 kHz. Thus, the data cannot be described by the addition of two $1/f^\gamma$ contributions with different, but frequency independent, exponent γ. A reasonable fit

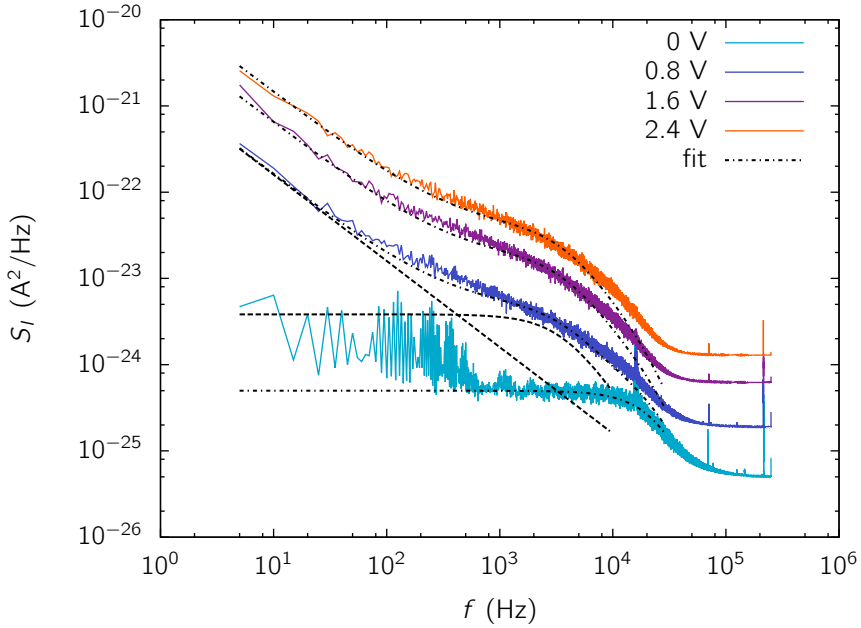

Figure 4.10.: Current noise power density spectra of a ZnO microwire. The fit consists of the current independent part visible for $V = 0$ V, a 1/f contribution and a Lorentzian with characterisic time constant of 42 μs. The current dependent contributions are depicted for $V = 0.8$ V by dashed lines.

was obtained by a Lorentzian according to Eq. 4.5 with a characteristic time constant $\tau = 42$ μs in addition to the $1/f$ contribution. A flattening of the spectrum in the same frequency range was also observed for the thin film samples investigated in the previous subsection. Hence, this might be a general feature of ZnO. Unfortunately most spectra shown in literature end around 1 kHz, so that no further inquiry on this matter was possible. In Fig. 4.11 the fit results for the flicker noise are presented. α_{H} is between 2×10^{-4} and 2×10^{-3}, calculated for charge carrier densities of 3×10^{16} cm^{-3} and 3×10^{17} cm^{-3}, respectively. This is very close to the values obtained for the thin film samples. Unless additional noise sources are introduced in the microwires due to the different growth technique, the $1/f$ noise observed in our measurements is very likely neither caused by grain boundaries nor surface traps.

If the $1/f$ noise source in wires and thin films is assumed to be identical, also the assignment of mobility fluctuations as origin of the measured noise runs into problems. In microwires, lattice scattering (e.g. polar optical scattering) is most likely the dominant scattering mechanism at room temperature, similar to high quality thin films and single crystals [51]. In the thin films used for this work, grain boundary scattering or impurity scattering are probably dominant at room temperature (see section 3.2). If Matthiesen's rule holds, the fluctuations induced by different scattering paths enter the fluctuations of the total mobility μ via [83]

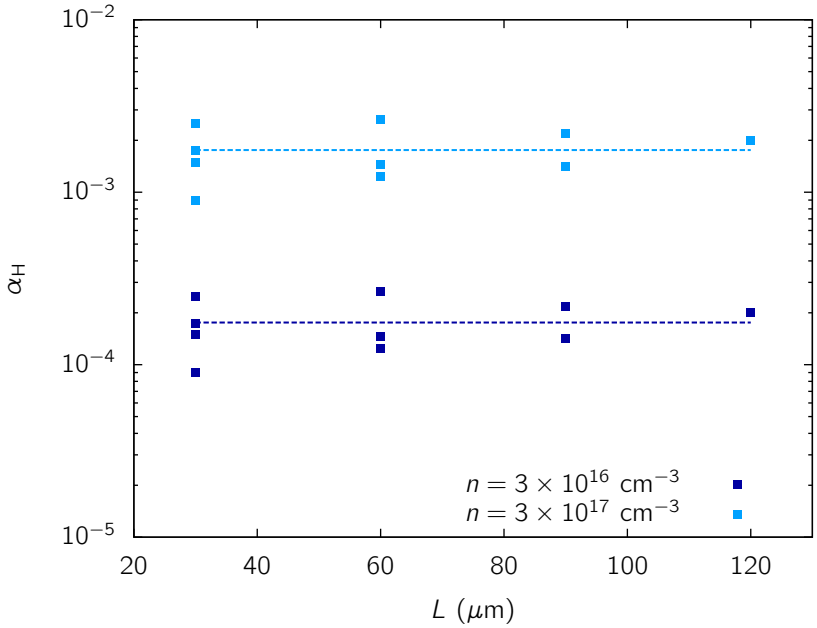

Figure 4.11.: Hooge parameter for current noise in a ZnO microwire, calculated from measurement assuming different charge carrier densities. All measurements are from the same wire, measured between different contact points. The average values are 1.75×10^{-3} and 1.75×10^{-4}.

$$\alpha_\mathrm{H} = \sum_i \frac{\mu^2}{\mu_\mathrm{i}^2} \alpha_{\mathrm{H,i}}. \tag{4.12}$$

μ_i are the mobilities due to the various scattering paths and $\alpha_{\mathrm{H,i}}$ the respective Hooge constants, assuming $1/f$ noise for all contributions. If a scattering mechanism, e.g. grain boundary scattering, becomes insignificant, the factor μ^2/μ_i^2 decreases. To keep α_H constant, $\alpha_{\mathrm{H,i}}$ would have to increase accordingly. However, with fewer grain boundaries present, $\alpha_{\mathrm{H,i}}$ should rather decrease. In this way, similar Hooge constants for samples with different scattering mechanisms are hardly compatible with the model for mobility fluctuations represented by Eqn 4.12.

Summing up, the flicker noise stems most likely from the ZnO bulk and has a similar magnitude in all examined samples, apart from some unsystematical outliers. As the most likely candidates for the origin of $1/f$ noise are disfavored by the experiments presented here, no model for the noise is proposed. Unless further experimental data is available, the assignment of theoretical models for the explanation seems premature.

4.4. ZnO Based Devices

4.4.1. Transistors

Noise produced by a semiconductor, as described in the previous section, will also be present in transistors based on the material. The gate insulator in MISFETs is often a major source of noise, as described by the McWhorter model. The gate/channel interface of MESFETs and JFETs is conducting, which prevents such $1/f$ noise caused by tunneling into isolated traps. Under most operating conditions there will be a depletion layer below the gate, which keeps the channel current away from the gate/channel interface. Hence, the interface is expected to have minor influence on the current noise. However, the gate current can be an additional source of noise in MESFETs and JFETs.

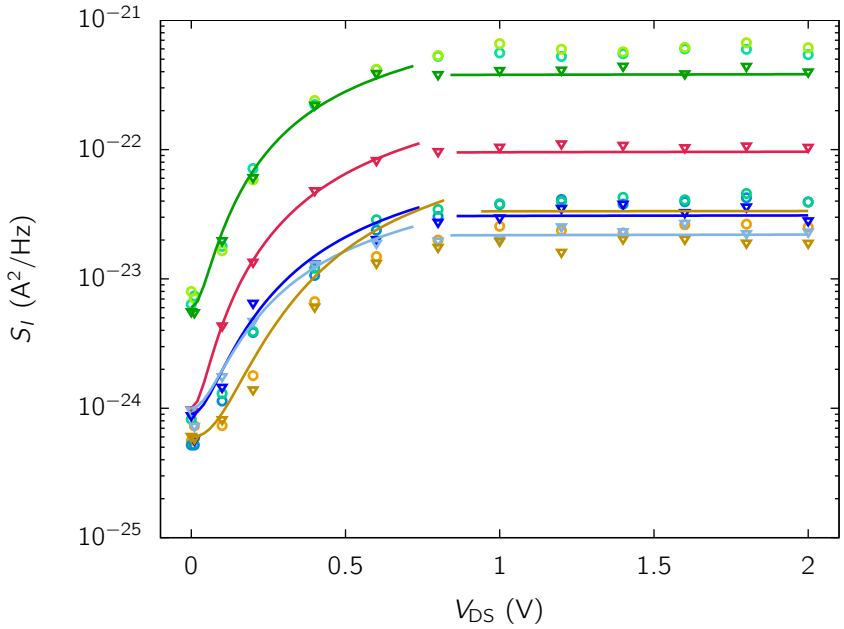

Figure 4.12.: Power spectral density of the MESFET drain current noise at 15 Hz and $V_{GS} = 0$ V (symbols), dependent on the drain-source voltage. For five FETs the noise has been calculated using the output characteristics and $\alpha_H = 1.5 \times 10^{-3}$ (solid lines). The transistors had the same gate length $L = 10$ μm, but varying gate width W and source/drain-gate distance L_s: $W = 392$ μm, $L_s = 20$ μm (green), $W = 72$ μm, $L_s = 20$ μm (red), $W = 22$ μm, $L_s = 20$ μm (blue), $W = 72$ μm, $L_s = 110$ μm (orange/brown).

The drain current noise of ZnO-based MESFETs with Pt gate and JFETs with $ZnCo_2O_4$ gate (as described in detail in Chapter 3) showed a dominating 1/f contribution at low frequencies, similar to the spectra shown previously for ZnO channels without gates. The measured power spectral density at 15 Hz and $V_{GS} = 0$ V for MESFETs is shown

in Fig. 4.12. To compare these measurements with the Hooge paramters α_{H} determined from ZnO samples in the previous sections, one must consider the inhomogenous current density in a transistor. Near the drain contact the channel cross section is smaller than near source, due to the wider depletion layer. Thus, this part of the channel has a major influence on the total current flowing and also on the current noise. The total noise can be calculated by integrating over the channel length, as has been demonstrated for generation-recombination noise by van der Ziel [110] and by van Vliet and Hiatt [111]. The same procedure can be applied for 1/f noise, which gives

$$S_I(f) = \frac{e\mu V_{\mathrm{DS}} I_{\mathrm{D}}}{L^2} \frac{\alpha_{\mathrm{H}}}{f}. \tag{4.13}$$

For an ohmic resistance with length L, cross section $A_0 = V_0/L$ and conductivity $en\mu$ this expression becomes equivalent to Hooge's formula (Eqn. 4.6). In the saturation regime the voltage V_{DS} must be substituted by $V_{\mathrm{DS,sat}} = V_{\mathrm{GS}} - V_{\mathrm{T}}$. Also the effective channel length changes in saturation, but is close to L for high L/a ratios. Using I_{D} from the FET's output characteristics, the measured noise can be fitted. In Fig. 4.12 the calculations for $\alpha_H = 1.5 \times 10^{-3}$ are shown by solid lines, separately for linear and saturation regime. The constant thermal contribution measured for $V_{\mathrm{DS}} = 0$ V has been added to improve the fit at small voltages. Also the series resistance caused by the distance L_{S} between gate and the ohmic contacts has to be taken into account, which is made clear by the difference between the red and orange symbols in Fig. 4.12. These correspond to FETs with the same gate dimensions, but different series resistances. For the calculations shown here it was assumed, that the noise contributions from the series resistances are negligible, due to the higher current density below the gate. However, the voltage drop $V_{\mathrm{S}} = R_{\mathrm{S}} I_{\mathrm{D}}$ across the series resistances was taken into account, reducing V_{DS} by $2V_{\mathrm{S}}$. The pinch-off condition changes to $V_{\mathrm{bi}} - (V_{\mathrm{GS}} - V_{\mathrm{S}}) + (V_{\mathrm{DS}} - 2V_{\mathrm{S}}) = V_{\mathrm{P}}$, leading to $V_{\mathrm{DS,sat}} = V_{\mathrm{GS}} - V_{\mathrm{T}} - V_{\mathrm{S}}$. Whether this is sufficient to cover the effects of the series resistances remains unclear, as attempts to include the parts of the channel not covered by the gate in a calculation similar to Eqn. 4.13 led to results strongly deviating from experiment. The relatively good match of measurements and calculations shown in Fig. 4.12 suggest, that the assumed assumptions are reasonable. The conformity of a_{H} with the values obtained from measurements at homogenous ZnO samples demonstrates, that in FETs the same noise process is dominant and the influence of the gate/channel interface and the gate leakage current is negligible at intermediate gate voltages.

The current noise density of a JFET and a MESFET at $V_{\mathrm{DS}} = 2$ V in dependence on the gate voltage is shown in Fig. 4.13(a). In an intermediate V_{GS} range from -0.5 V to about 1 V S_{I} is well described by calculations based on Eqn. 4.13 and the measured transfer characteristics (Fig. 4.13(b)). Below $V_{\mathrm{GS}} = -0.5$ V the power spectral density is constant. It is probably dominated by the gate leakage current, whose noise has not been modelled within this work, due its negligible contribution under the desired operation conditions. To test the long term stability, the measurements were repeated after several weeks. The transfer characteristics are stable within at least 1 month for

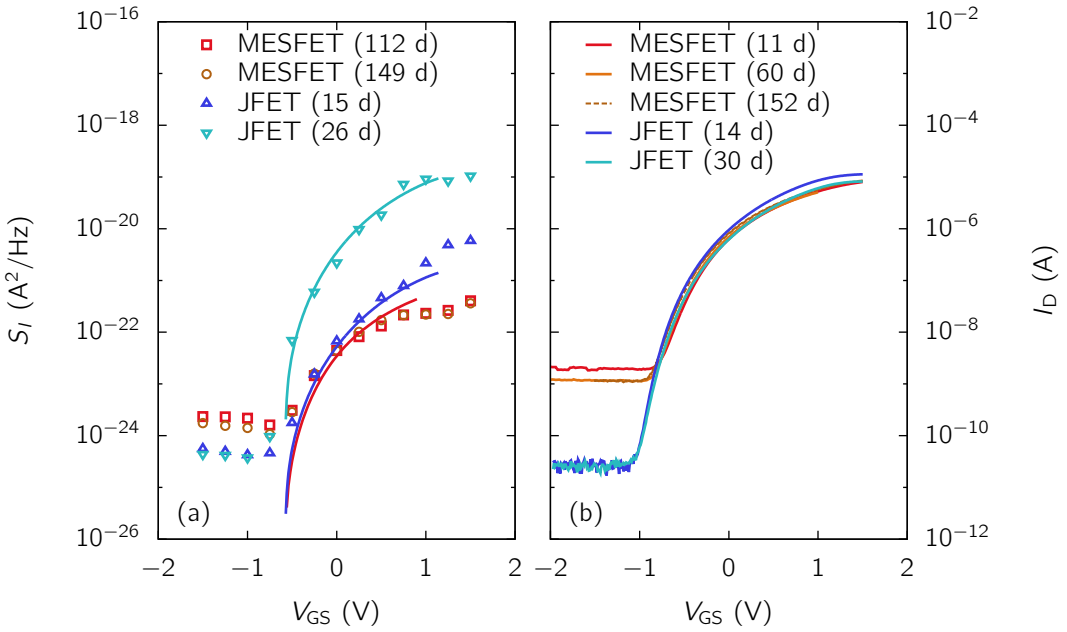

Figure 4.13.: (a) Power spectral density of MESFET and JFET at 15 Hz and V_{DS} = 2 V (symbols), dependent on the gate-source voltage. The solid lines are calculations based on the measured transfer characteristics. For the blue and red curves $\alpha_H = 1.5 \times 10^{-3}$ was used, for the cyan curve $\alpha_H = 0.1$. (b) Transfer characteristics of the same MESFET and JFET, measured at different time after the fabrication.

the JFET and 5 months for the MESFET. The noise of the JFET was similar to the MESFET after 2 weeks, but significantly increased after 4 weeks. This degradation is indicated in the transfer characteristics only by a slight decrease in the ON-current, but more prominently by a less constant saturation current in the output characteristics. Such degradation would be a serious drawback for the use of the JFETs in a sensor application, as the sensitivity is reduced by one order of magnitude. More sophisticated long term experiments would be desirable, to reassure these findings and possibly develop a strategy to prevent the degradation. It should be noted, that the MESFET shown here was contacted by the flip-chip method, while the JFET was contacted by gold wires. Experiments on one MESFET sample contacted with gold wires exhibited also elevated noise figures, but already directly after the contacting and not after a certain elapsed time. Thus, the contacts might under certain (unknown) conditions be involved in the origin of the $1/f$ noise. The change of the JFETs' output characteristics during one month, however, was veryfied independently from the gold wire contacting by wafer prober measurements.

Based on the ascertained agreements between theoretical descriptions and measurements, the signal-to-noise ratio (SNR) of the devices can be modelled. For this work,

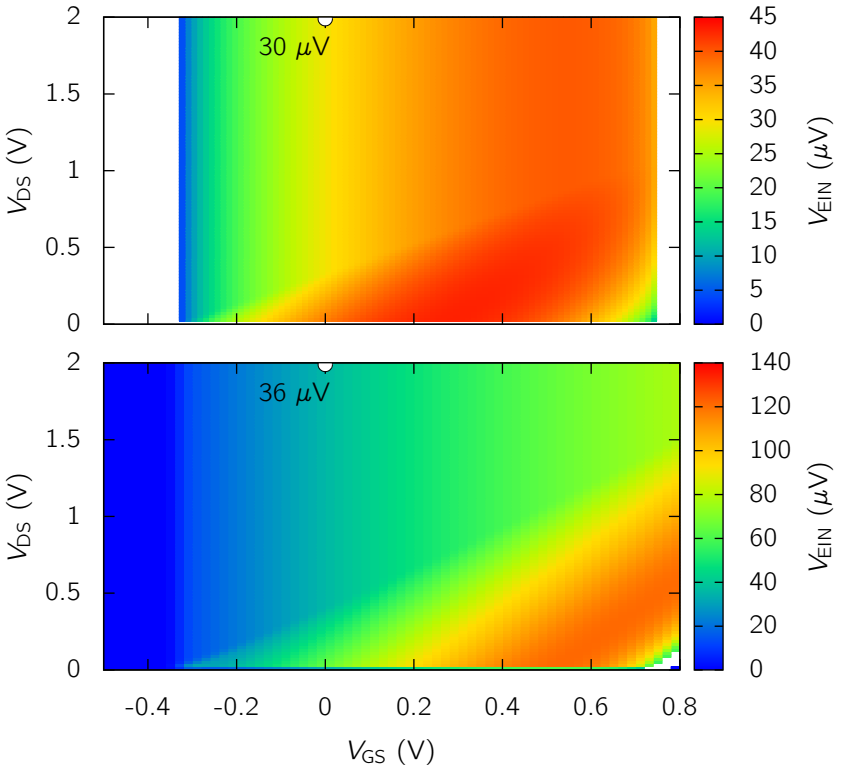

Figure 4.14.: Theoretical dependency of the equivalent input noise on the transistor working point. The noise level was calculated for a frequency range between 10 Hz and 10 kHz, using twice the standard deviation caused by 1/f noise according to Eqn. 4.13. For the upper plot the transconductance was calculated using Eqns. 3.24 and 3.25. For the lower plot the more involved model including R_S and subthreshold current was used.

the noise level for a recorded time series is defined by twice the standard deviation. This is a suitable measure for the noise in the sense, that signals with this magnitude cannot be seperated from the noise, while signals with an amplitude larger than twice this level should be detectable. The *SNR* of a transistor for a voltage signal with amplitude ΔV_{GS} at the gate is then defined by

$$SNR_{FET} = \frac{\Delta I_D}{2\sigma(I_D)} \approx \frac{g_m(V_{GS}, V_{DS})\Delta V_{GS}}{2\sigma(I_D)}, \tag{4.14}$$

using the transconductance $g_m(V_{GS}, V_{DS})$ of the FET. As the *SNR* must always be defined for a specific signal strength ΔV_{GS}, a useful quantity for characterizing the FET is the equivalent input noise voltage V_{EIN}, given by

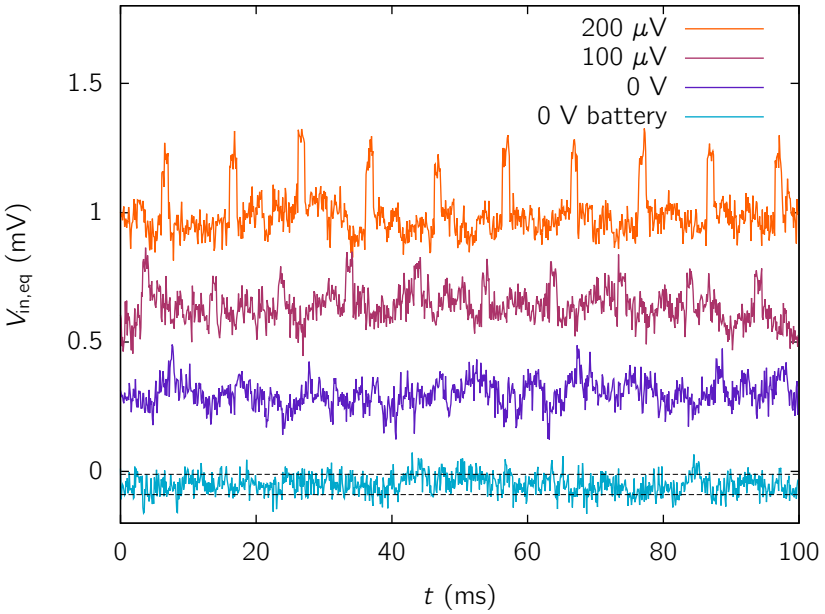

Figure 4.15.: Current response of FET to rectangular voltage pulses at the gate. The output was normalized by the transconductance to obtain equivalent input values, and shifted by an offset voltage to obtain the stacked layout. The operation point was $V_{\mathrm{DS}} = 2$ V and $V_{\mathrm{GS}} = 0$ V, and the sampling frequency 10 kHz. The distance between the black lines is $2\sigma = 80$ μV.

$$V_{\mathrm{EIN}} = \frac{\Delta V_{\mathrm{GS}}}{SNR} = \frac{2\sigma(I_{\mathrm{D}})}{g_{\mathrm{m}}(V_{\mathrm{GS}}, V_{\mathrm{DS}})} = \frac{2\sqrt{\int_{\Delta f} S_I(f)\,\mathrm{d}f}}{g_{\mathrm{m}}(V_{\mathrm{GS}}, V_{\mathrm{DS}})}. \tag{4.15}$$

This is the inverse *SNR*, normalized by the signal amplitude. It describes a hypothetical noise level at the input, which would lead to the oberved noise at the output for an ideal noise-free device, and gives the lower limit of detectable signals. V_{EIN} does not depend on the specific properties of an input signal, but through $\sigma(I_{\mathrm{D}})$ on the frequency range Δf in which the measurement takes place. Besides the sampling parameters only transistor properties enter the quantity.

The calculated equivalent input noise in dependence on V_{GS} and V_{DS} is presented in Fig. 4.14. In the upper part of the figure the transconductance was calculated according to Eqns. 3.24 and 3.25. For $V_{\mathrm{GS}} > 0$ V V_{EIN} assumes values between 30 μV and 45 μV. This calculation can be considered as limit for an ideal device. In the lower part of Fig. 4.14, a device model including series resistances and subthreshold current was applied. For high drain voltages, V_{EIN} increases only little compared to the ideal case, as in the saturation regime a large part of V_{DS} drops across the series resistances anyway. In the linear regime V_{EIN} can increase to more than 100 μV, because of the

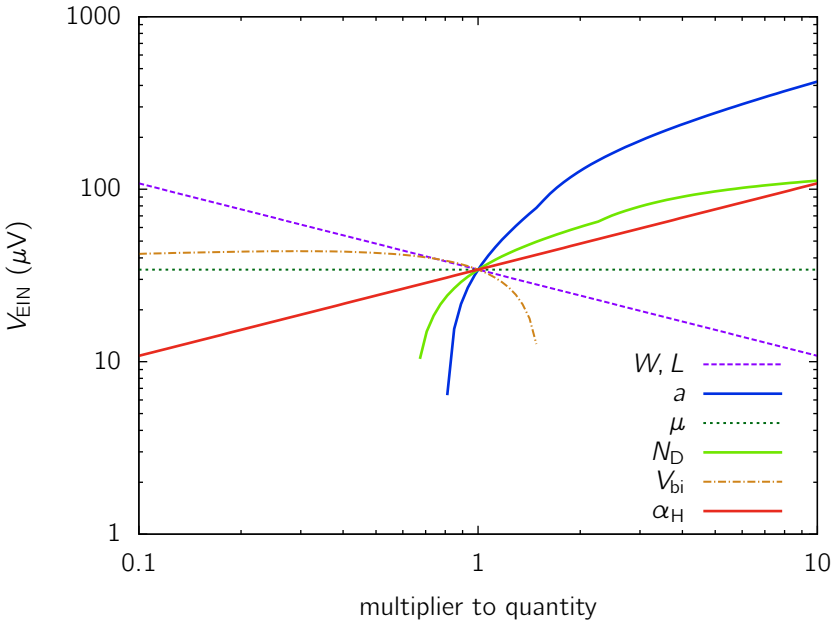

Figure 4.16.: Calculated dependency of the equivalent input noise voltage on variations in device and material properties. The quantites were varied between 10% and 1000% around the values given for Fig. 4.14.

reduced transconductance. The quantites used for both calculations were $W = 22\ \mu$m, $L = 10\ \mu$m, $L_S = 20\ \mu$m, $a = 14$ nm, $\mu = 10\ \mathrm{cm}^2/\mathrm{Vs}$, $N_D = 5 \times 10^{18}\ \mathrm{cm}^{-3}$, $V_{bi} = 0.75$ V, $\alpha_H = 2 \times 10^{-3}$, typical values for devices in this work.

At $V_{DS} = 2$ V and $V_{GS} = 0$ V the equivalent input noise and the detectability of voltage signals applied at the gate were experimentally ascertained. The expected values for V_{EIN} at this working point are marked in Fig. 4.14. The measurements are presented in Fig. 4.15. Additional noise from the voltage generator must be considered here. For that reason, a measurement with constant gate voltage was conducted, where the voltage was determined by the internal ground of the battery supplied amplifier instead of the signal generator. Statistical analysis of the signal yields $2\sigma = 80\ \mu$V for the equivalent input voltage. This is roughly twice the calculated value of 36 μV. The difference is due to the systematic overestimation of the transconductance close to the threshold by the FET model. Fig. 4.14 shows, that the signal with amplitude 100 μV can be distinguished from the noise, but partly only because the periodicity is known. For the reliable detection of a random signal an amplitude of about 200 μV is necessary.

To investigate the influence of material properties and device dimensions on V_{EIN}, the calculations shown in Fig. 4.16 have been performed. The influence of gate length L and width W is explained by the inverse dependence of S_I on the total number of carriers. Hence, the noise level decreases with $1/\sqrt{WL}$. The mobility μ does not influence the

equivalent input noise at all, under the assumption that the conductivity fluctuations in the channel are independent of μ. This might not be true, as indicated by Eqn. 4.7, but cannot be judged using the measurements on hand. A carefully prepared series of samples with varying mobility, but otherwise very similar properties, would be neccesary to investigate this further. The channel thickness a and the doping density N_D have a qualitative similar proportionality to V_{EIN}. They do not enter S_I directly, but I_D and g_m through the definitions of V_P and I_P. Decreasing a and N_D results in decreasing equivalent input noise, but the change is less for N_D due to the inverse dependence of the 1/f noise on the total carrier number. For ZnO channels on a-sapphire it has been demonstrated in section 3.2, that a reduction in the channel thickness causes the carrier density to increase and vice verso. This means, that variations in a and N_D cannot be fully exploited to decrease the equivalent input noise. The use of glass substrates, as reported by Frenzel *et al.* [50], would make it possible to change these quantities independently and to check the effect on V_{EIN}. For completeness also the dependency on the built-in potential V_{bi} has been calculated. Increasing the barrier height increases the transconductance, due to a more efficient control of the depletion layer in the channel, hence decreasing the equivalent input noise. However, the barrier height is determined by the gate material and not easily changed. Usually the highest possible barrier is used anyways, if not connected to a serious drawbacks like the low cutoff frequency observed with Ag gate contacts on ZnO channels.

4.4.2. Transistors with Floating Gate

A transistor gate that is not fixed at a given potential is called a floating gate. In case of an ideal MISFET the gate metal contact is totally isolated, and the charge on the contact determines the conduction properties of the channel under floating gate conditions. MESFET and JFET gate contacts are always electrically contacted via the gate diode. Thus, under floating gate conditions a clearly defined gate voltage will arise for every given source-drain voltage. This gate voltage V_{GS} is determined by the condition $I_G = 0$. This does not mean, that no current flows between channel and gate. V_{GS} will adopt a value between 0 V and V_{DS}, so that the forward diode current close to source equals the reverse diode current close to drain. Fig. 4.17(a) shows the output characteristics of a MESFET for V_{GS} between 0 V and 0.5 V, together with the current measured under floating gate conditions. The floating gate voltage in dependence on V_{DS} can be determined by the crossings of the currents in Fig. 4.17(a), or measured directly with a voltage measurement unit at the gate. The result of this measurement is shown in Fig. 4.17(b). V_{GS} does not stay close to 0 V, but increases to nearly 0.6 V at $V_{DS} = 2$ V. For small V_{DS} the measurement is not very accurate and exhibits a large hysteresis, as the input capacitance of the measurement unit must be charged via the gate diode, which has a very high impedance.

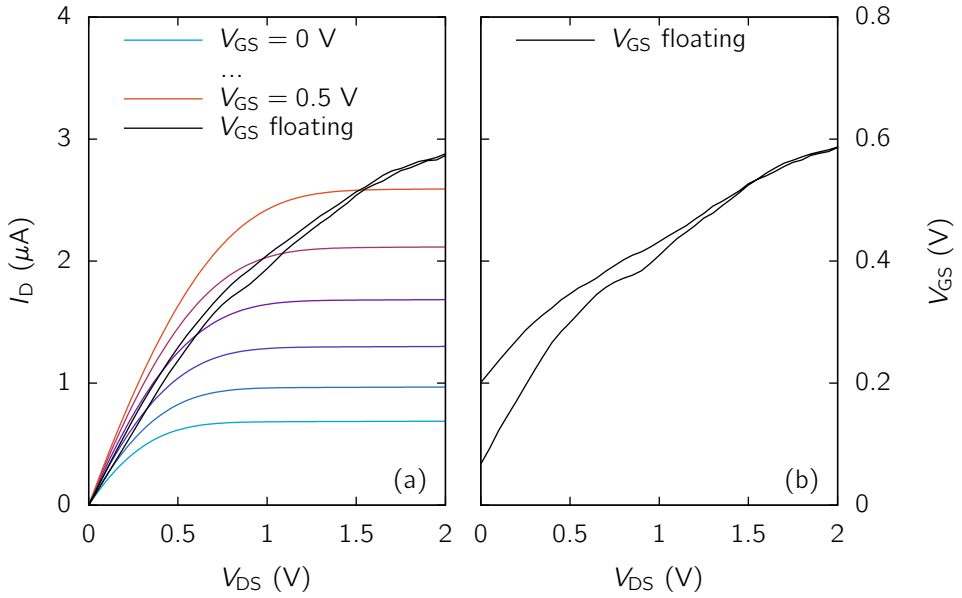

Figure 4.17.: (a) Output characteristic of a MESFET with Pt gate for different gate voltages and with floating gate. (b) Measured gate voltage under floating gate condition.

Typical noise power density spectra of the drain current under floating gate conditions are shown in Fig. 4.18(a). A peak at the power line frequency of 50 Hz is visible, indicating that the floating gate acts as antenna for stray noise due to the gate diode's high impedance. In contrast to measurements with fixed gate voltage, S_I is only at very low frequencies proportional to $1/f^\beta$ with $\beta \approx 1$, while in an intermediate range around 100 Hz rather $\beta \approx 3$ holds. The transition frequency f_0 between these regimes shifts with V_{DS}. Thus, for $V_{DS} < 1$ V only the $1/f^3$ part is visible in our measurements, which have a minimal frequency of 5 Hz. The spectra can be fitted with the empirical relation

$$S_I = \frac{A}{f} \frac{1}{1 + (f/f_0)^2}, \tag{4.16}$$

where the first term with the fit paramter A decribes the $1/f$ part and the second term a first order low-pass filter with cutoff frequency f_0. Very likely this filtering behavior is caused by the gate capacitance C_G together with the gate diode impedance. The transition frequency can be estimated by

$$f_0 \approx \frac{1}{2\pi R_G C_G}, \tag{4.17}$$

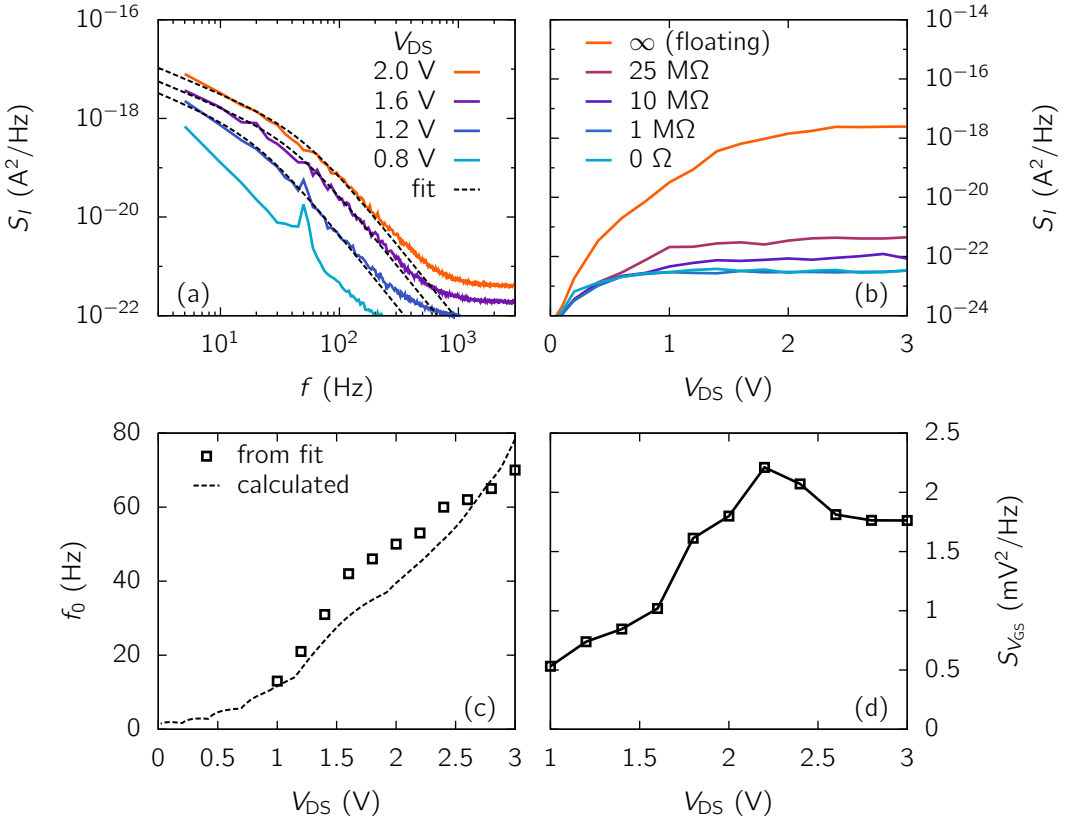

Figure 4.18.: Drain current noise under floating gate condition. (a) Power spectral density of I_D. (b) S_I at 15 Hz, dependent on the drain voltage. (c) Transition frequency f_0 between $1/f$ and $1/f^3$ regime, dependent on V_{DS}. (d) Power spectral density of the gate voltage at 15 Hz, calculated from S_I and the FET transconductance g_m.

where R_G is the differential resistance of the gate diode at the specific working point. C_G can be calculated according to the FET model proposed in the previous section, while R_G is given by

$$\frac{1}{R_G} = \int_0^L W \left.\frac{\mathrm{d}j_G}{\mathrm{d}V}\right|_{V_{GS}-V(x)} \mathrm{d}x. \tag{4.18}$$

The integral has been solved numerically, using the gate current density $j_G(V)$ obtained from a measured Schottky diode characteristic. V_{GS} was obtained by the measured relation presented in Fig. 4.17(b). The results from this calculation together with the f_0 values from the fits are displayed in Fig. 4.18(c). The agreement between calculation and fit is good (at least concerning the order of magnitude), providing evidence that the gate capacitance is indeed responsible for the filtering behavior.

The absolute magnitude of the noise under floating gate conditions is discussed in Fig. 4.18(b), exemplarily displayed for 15 Hz. Different resistances R_G were introduced between the gate contact and the voltage source that provides the gate voltage V_{GS}. $R_G = \infty$ denotes a fully floating gate, while $R_G = 0\ \Omega$ represents the usual operation conditions, as used in the previous section. It can be seen, that the noise with floating gate is nearly 5 orders of magnitude larger than with a fixed gate voltage. When R_G is in the range of a few ten MΩ a transition between both limits can be reached.

Using the transconductance of the FET the fluctuations of the gate voltage, which produce the observed drain current noise under floating gate conditions, can be calculated. $S_{V_{GS}}$ is shown in Fig. 4.17(d), again for $f = 15$ Hz. The integral over the noise power density gives the variance of the respective quantity. Using $S_{V_{GS}}(15\ Hz) \approx 1\ \mathrm{mV}^2/\mathrm{Hz}$, $f_0 \approx 45$ Hz and a frequency range from 10 Hz to 10 kHz, the standard deviation of the gate voltage is about 7 mV. The origin of these relatively large voltage fluctuations is not clear, yet. Possibly the conductivity fluctuations in the channel couple into the gate, as local fluctuations in the channel potential have an impact on the local gate current density. The gate currents determine V_{GS} under floating gate conditions, and V_{GS} again controls the channel current. However, attempts to derive a theoretical dependency, that would directly relate the channel conductivity fluctuations with the gate voltage fluctuations, were not successful within this work. Therefore, other noise contributions like gate current fluctuations cannot be excluded.

4.4.3. Simple Inverter

The output voltage fluctuations of ZnO-based simple inverters were evaluated, in order to judge whether the SNR can be improved by the inverter gain. The power spectral density of V_{out} for a ZnO based inverter with Au gates at different input voltages is shown in Fig. 4.19. The low frequency noise has again $1/f$ dependency, above 1 kHz superimposed by the low-pass behavior caused by the inverter cutoff (compare Fig. 3.30). The values of $S_{V_{out}}$ at 15 Hz are displayed in Fig. 4.20. It can be seen, that $S_{V_{out}}$ rises for several orders of magnitudes close to $V_{in} = 0$. The shape of the curve is comparable to the square of the inverter gain g, which is also displayed. The peak of $S_{V_{out}}$ is shifted slightly to positive voltages and less sharp compared to g^2. This is either due to degradation effects or due to the different measurement setups used for I-V and noise measurements. In any case, the similar curve shapes indicate, that the SNR of V_{out} does not depend strongly on the offset of V_{in}. Similar to Eqn. 4.15 for FETs the equivalent input noise V_{EIN} for inverters can be defined as

$$V_{EIN} = \frac{2\sqrt{\int_{\Delta f} S_{V_{out}}(f)\,\mathrm{d}f}}{g}. \tag{4.19}$$

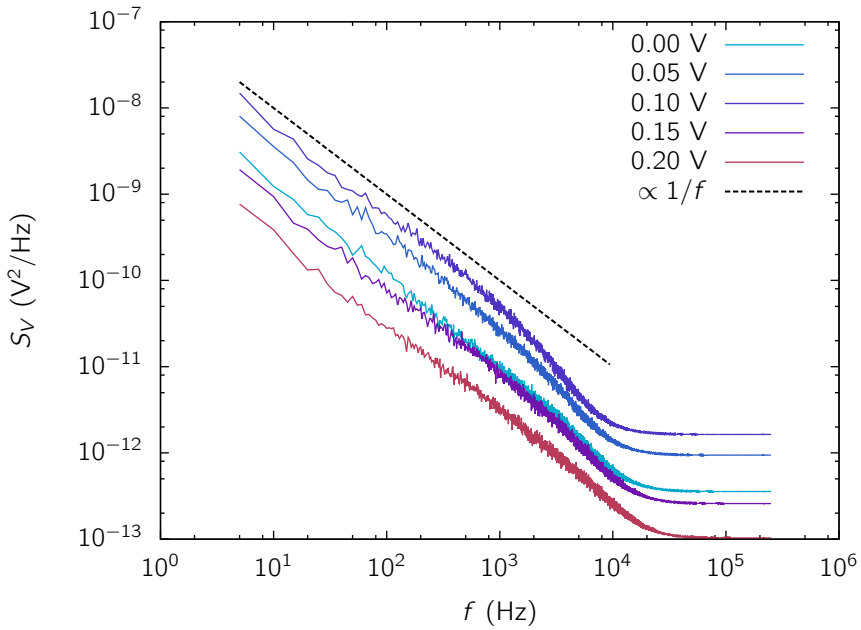

Figure 4.19.: Power spectral density of the output voltage of a ZnO based simple inverter with Au gates. The input voltage was varied, while V_{DD} was constant at 2 V.

The maximum values of $S_{V_{\mathrm{out}}}$ and g from the data presented in Fig. 4.20 yield a value of $V_{\mathrm{EIN}} = 67$ mV for the frequency range between 10 Hz and 10 kHz. This is twice the value calculated for FETs, as shown in Fig. 4.14, due to the fact that both transistors in the inverter contribute to the current noise.

The equivalence of the inverter's V_{EIN} with twice the value calculated for FETs can also be reproduced theoretically. In the previous chapter an expression for the inverter gain close to $V_{\mathrm{in}} = 0$ V was derived from the current conservation equation (Eqn. 3.34) using Taylor expansion. When only the left-hand side of the equation is evaluated, the dependency of V_{out} on the load transistor's drain current $I_{\mathrm{D}}^{\mathrm{load}}$ can be examined. For $V_{\mathrm{in}} > 0$ this leads to

$$\frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}I_{\mathrm{D,sat}}^{\mathrm{load}}} = -\sqrt{\frac{V_{\mathrm{p}}^3}{9I_{\mathrm{p}}^2(1-\sqrt{V_{\mathrm{bi}}/V_{\mathrm{p}}})V_{\mathrm{in}}}}. \tag{4.20}$$

If $I_{\mathrm{D,sat}}^{\mathrm{load}}$ exhibits current noise according to Eqn. 4.13, the noise density of the output voltage close to $V_{\mathrm{in}} = 0$ V is

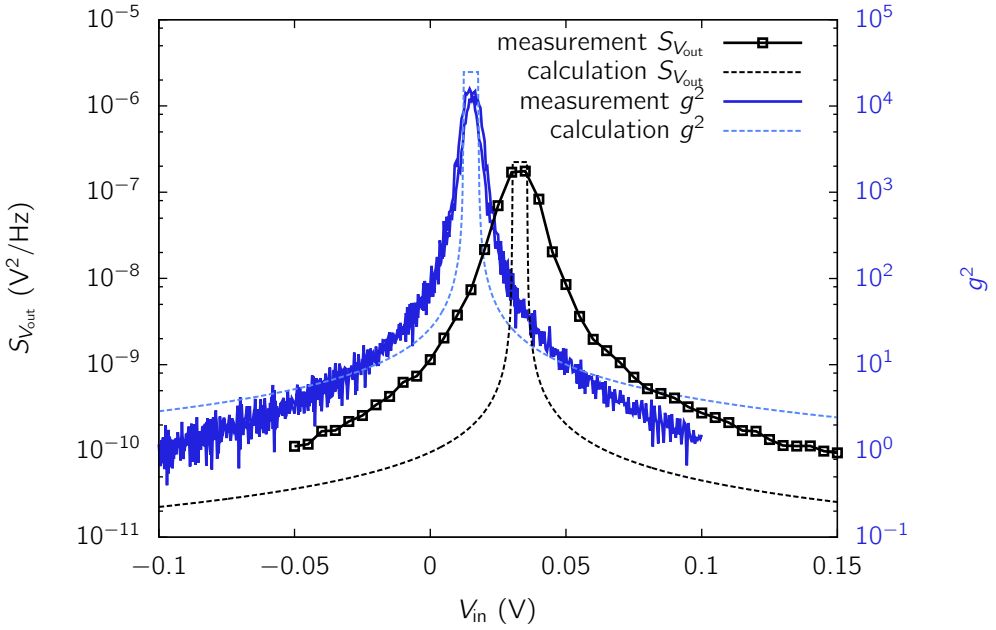

Figure 4.20.: $S_{V_{out}}$ at 15 Hz of a ZnO based simple inverter with Au gates in dependence on V_{in}. For comparison the square of the inverter gain, obtained from the transfer characteristics, is displayed.

$$S_{V_{out}} = \frac{V_p^3}{9I_p^2(1-\sqrt{V_{bi}/V_p})V_{in}} \frac{e\mu(V_p - V_{bi})I_{D,sat}^{load}}{L^2} \frac{\alpha_H}{f}. \tag{4.21}$$

Using Eqn. 3.20 for the description of the FET saturation current, this can be written as

$$S_{V_{out}} = \frac{e\mu V_p(V_p - V_{bi})^3}{12L^2 I_p(1-\sqrt{V_{bi}/V_p})V_{in}} \frac{\alpha_H}{f}. \tag{4.22}$$

In section 3.1.3 it was discussed, how non-ideal FETs with a saturation current proportional to αV_{DS} result in inverters that exhibit a nearly constant gain g_{const} close to $V_{in} = 0$ V. The value of g_{const} is given by Eqn. 3.41. If the influence of the FET's non-ideality on the output noise is evaluated, a constant value for $S_{V_{out}}$ close to $V_{in} = 0$ V is found. It is given by

$$S_{V_{out},max} = \frac{1}{4\alpha^2} \frac{3e\mu(V_p - V_{bi})^3 I_p}{4V_P^2 L^2} \frac{\alpha_H}{f}. \tag{4.23}$$

In Fig. 4.20 calculations for g (based on Eqns. 3.41 and 3.43) and for $S_{V_{\mathrm{out}}}$ (based on Eqns. 4.22 and 4.23 with $\alpha_{\mathrm{H}} = 2 \times 10^{-3}$) are shown. The offset value of V_{in} was in both cases fitted to the respective measurement. Although the width of the $S_{V_{\mathrm{out}}}$ peak is underestimated by the calculation, the height is matched very well. Thus, the equations derived for this work give good estimates for both gain and the low frequency noise magnitude close to the point of maximum gain.

If Eqn. 4.23 for the noise and Eqn. 3.41 for the gain are inserted in Eqn. 4.19 for the inverter V_{EIN}, the expression of the transistor V_{EIN} is exactly reproduced. This illustrates again, that the amplification of the inverters cannot overcome the sensitivity limit determined by the FETs. The usage of an amplifying stage would still be reasonable, if further data processing steps are performed on-chip. Then the amplification of the signal directly at the input transistor would reduce the relative contribution of these steps to the total noise.

5. Experiments in Electrolyte and with Cells

5.1. Cell-Transistor Coupling

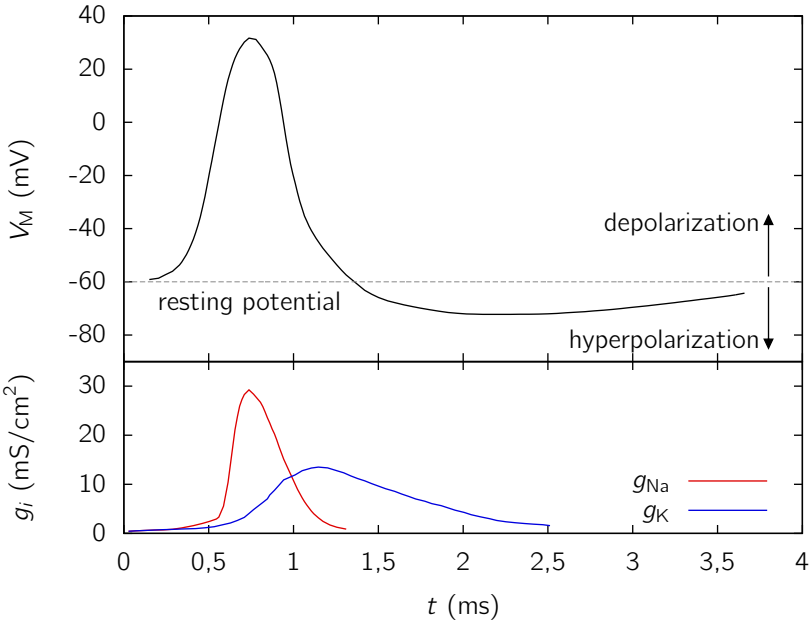

Figure 5.1.: Schematic course of an neuron action potential, based on [112]. The lower graph depicts the membrane conductivity for Na^+ and K^+ ions.

The concentration of ions in the interior of animal cells differs from that in the extracellular medium. Typically, ion concentrations of Na^+, Cl^-, and Ca^{2+} in the cell interior are lower and that of K^+ higher than in the surrounding electrolytic solution. The ion gradients are maintained by so-called ion pumps, proteins in the cell membrane that transport ions actively and selectively through the membrane, with energy usually provided by the hydrolysis of ATP [114]. The gradients are also supported by the selective permeability of the cell membrane to different ion species. Ion gradients without active transport emerge especially from the presence of negativly charged organic ions inside the cell, which cannot pass the membrane. The excess of negative ions inside the cell leads to a potential difference V_M between cell exterior and interior. The resting potential of neurons is usually between -55 mV and -75 mV, differing not only between animal

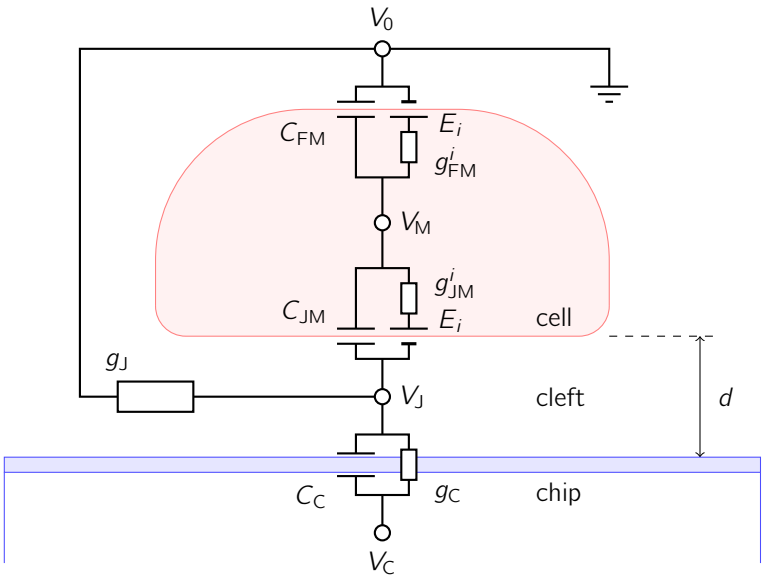

Figure 5.2.: Schematic illustration of the electrical contact between cell and electrode chip, based on [113].

species but also between different neuron types of the same animal [115]. Nerve cells have the capability to change their membrane potential in response to external stimuli, some neuron types even exhibit spontaneous potential changes without external excitation. As described and experimentally verified by Hodgkin and Huxley [116] such an action potential is started by rapid influx of Na^+ into the cell, due to opening of specific ion channels and driven by both diffusion and drift. This leads to the so-called depolarisation, a change of the membrane potential to positive voltages, typically in the range of few 10 mV. K^+ channels will open with a certain delay, countering the Na^+ flow and returning the potential eventually to negative voltages. The voltage peak lasts about 1-2 ms, as depicted in Fig. 5.1. After spiking, a certain time is necessary to return the cell to the excitable state, which limits the firing rate of the neuron. This time depends on the neuron species and is typically in the range of several milliseconds. The actual course of an action potential involves more ion species and a multitude of different ion channels in the membrane, which will not be discussed in detail here.

It should be noticed, that the relative change of the ion concentrations during an action potential is less than one per mill [115]. The situation in the cell interior as well as in the exterior space is basically not altered, restricting the effect of the potential change to the membrane. Hence, for extracellular recordings of action potentials from single cells the neurons must be very close the electrodes. The coupling of a neuron with an electrode, that is completely covered by the cell, can be described by the point-contact model illustrated in Fig. 5.2 [113, 117]. The cell membrane is divided into a

part which forms the junction with the chip and a free part in contact with the bulk of the surrounding medium. The first part is characterized by the capacitance C_{JM} and the ion conductivities g^i_{JM}, the latter by C_{FM} and g^i_{FM}. The batteries in the equivalent circuit represent the equilibrium potentials E_i for each ion species, determined by the Nernst equation (see e.g. [114]). Due to proteins embedded in the cell membrane and protein coating of the chip a cleft between cell and electrode emerges, which is filled with electrolyte. The sealing conductance g_{J}, which represents the electrical connection of the cleft with the surrounding cell medium, is determined by the conductivity of the electrolyte, the distance between cell and chip, and the circumference of the area covered by the cell.

If the influence of the chip is negligible, the charge conservation equation for the cleft is given by

$$g_{\mathrm{J}} V_{\mathrm{J}}(t) = C_{\mathrm{JM}} \frac{\mathrm{d}(V_{\mathrm{M}}(t) - V_{\mathrm{J}}(t))}{\mathrm{d}t} + \sum_i g^i_{\mathrm{JM}} (V_{\mathrm{M}}(t) - V_{\mathrm{J}}(t) - E_i). \tag{5.1}$$

When the junction voltage $V_{\mathrm{J}}(t)$ is small compared to the membrane potential V_{M}, $V_{\mathrm{J}}(t)$ is approximated by

$$V_{\mathrm{J}}(t) \approx \frac{1}{g_{\mathrm{J}}} \left(C_{\mathrm{JM}} \frac{\mathrm{d}V_{\mathrm{M}}(t)}{\mathrm{d}t} + \sum_i g^i_{\mathrm{JM}} (V_{\mathrm{M}}(t) - E_i) \right). \tag{5.2}$$

This is the quantity, that can actually be measured by a MEA chip. However, the shape of the transmitted signal is not necessarily identical to V_{J}, as it depends also on the properties of the electrode and how the cell is placed on the electrode.

With neurons from invertebrates like *Lymnaea stagnalis* (great pond snail) or *Hirudo medicinalis* (european medicinal leech) signal amplitudes up to several millivolts were measured with silicon based MEAs [25, 118, 119]. Experiments with mammalian neurons are often conducted with embryonal or fetal rat hippocampus cells. Action potential amplitudes measured with silicon chips are in the range of few 100 μV [18, 31, 63]. Lambacher *et al.* [31] feature a histogram of roughly 1000 measured spikes, where about 50% are in the range between 250 mV and 500 mV, and about 5% above 1 mV. Comparably strong signals are achieved with cardiac myocytes. A confluent layer of such cells exhibits local contractions, which provide optical control over the cell activity. A cell line based on mouse cardiomyocytes is HL-1, derived by Claycomb *et al.* [120]. Signal amplitudes up to 1 mV have been reported for HL-1 cells and cardiomyocytes [22, 23, 121].

Noise figures reported for active MEAs are quite diverse, and differently defined. Often the root mean square (rms) of the noise is given, which is in this context identical to the standard deviation of the measured signal. Another frequently reported quantity is the peak-to-peak noise level. This is an intuitive quantity, but statistically difficult to define, as for usual theoretical noise distributions arbitrary large values are possible. If estimated by the eye, the peak-to-peak noise is typically 3 to 5 times larger than the rms noise. For a normally distributed random quantity this corresponds to a confidence interval between 87% and 99%. Usually all measured signals and noise quantities are divided by the gain of the system, in order to obtain the signal strength at the input and equivalent input noise figures, respectively.

The rms noise level of highly integrated silicon chips is reported at 11 μV by [18] and 40-80 μV by [31]. In some cases, especially for new experimental systems, low noise for the actual devices is claimed, while measurements with cells exhibit comparably high noise levels. This is usually attributed to the measurement setup. E.g. Steinhoff *et al.* [20] calculate for their AlGaN/GaN transistors peak-to-peak noise of 15 μV (due to $1/f$ noise with $a_{\mathrm{H}} = 5 \times 10^{-3}$), while the measured noise is about 200 μV peak-to-peak, attributed to the analog-to-digital converter (consider the erratum published for this paper!). Hess *et al.* [23] report for graphene solution-gated FETs a minimal rms noise of 11 μV, while observing 50 μV rms noise during measurements with HL-1 cells.

The MESFETs with Pt gates examined in the previous chapter exhibited rms noise in the range of 40 μV at a sampling frequency of 10 kHz (see Fig. 4.15). Compared to the noise levels for active MEAs based on silicon and other material systems reported in literature, this is sufficient for proof-of-principle measurements with ZnO based MEAs. However, one must keep in mind, that other components in the setup might contribute to the total noise. Only when the system is fully understood, the sensitivity of the MEAs can be correctly evaluated.

5.2. Materials in Electrolytical and Biological Environment

5.2.1. Material Stability in Electrolytical Environment

The surface of a MEA during cell culture is exposed to an aqueous electrolytic solution. Thus, the stability of the materials in contact to the electrolyte must be guaranteed for at least one week. Furthermore, the protection of sensitive parts of the chip must be assured. Noble metal electrodes can be expected to withstand the conditions during cell culture, but the stability of alternative materials like transparent conducting oxides must be evaluated. This applies also to semiconducting materials, in order to determine the grade of protection necessary for the electronic structures on the chip. For semiconduc-

tors unaffected by the electrolyte the fabrication of solution-gated transistors is possible, where the gate contact is simply formed by the electrolyte/semiconductor interface.

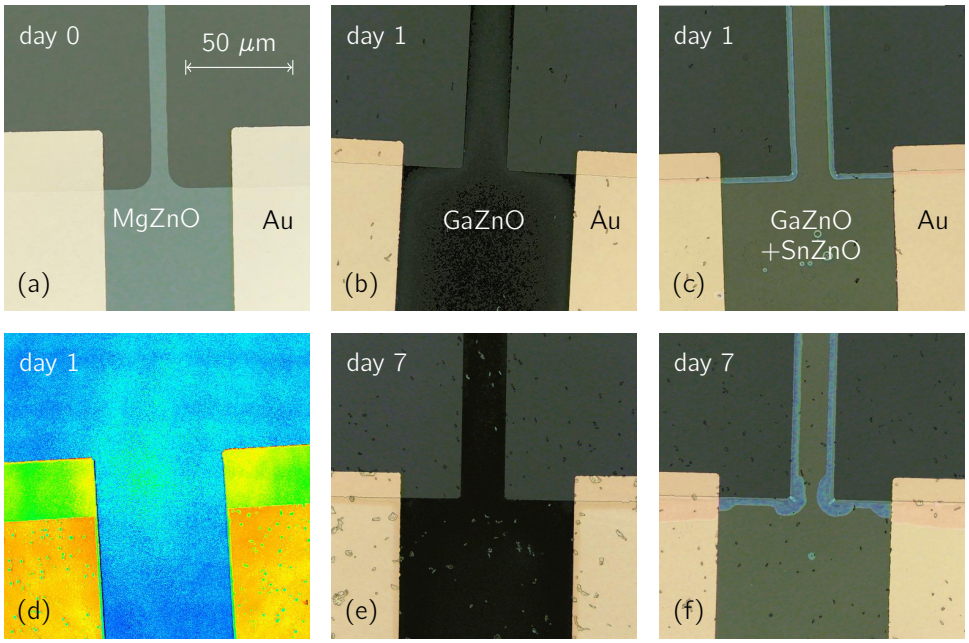

Figure 5.3.: Stability of conducting and semiconducting materials deposited by PLD exposed to PBS. (a-c,e-f) are optical micrographs, (d) is a height map recorded by laser scanning microscopy.

The stability of several conducting and semiconducting materials deposited by PLD was tested by exposure to phosphate buffered saline (PBS) for several days. PBS contains several anorganic ion species in physiological concentration, comparable to the aqueous solutions used for cell culture. The material layers were structured by photolithography and partially covered by ohmic gold contacts, similar to a transistor without gate contact. The Au contacts were deposited by dc sputtering and had a thickness of about 30 nm. Several times during one week the samples were taken out of the electrolyte and characterized by optical microscopy, laser scanning microscopy, and I-V measurements. Fig 5.3 shows microscope images for three materials. ZnO with 0.25wt-% MgO in the target, as used for FET channels in this work, has completely dissolved after one day in electrolyte. The height image Fig 5.3(d) reveals, that even the gold contacts provide no suitable protection, as circular holes appear in the ZnO layer below the contacts. This indicates, that sputtered metal contacts contain pinholes and cannot be used to shield underlying materials from liquids without further optimization. Thus, FETs with ZnO channels must be well protected from the electrolyte, and also the metal gate contacts provide no sufficient cover for the channel material.

ZnO with 4wt-% Ga_2O_3 in the target is a transparent conductor and a material candidate

for conducting paths and electrodes. Thin films deposited at room temperature with a thickness of 100 nm and an initial resistivity of 2×10^{-5} Ωm were examined. Fig 5.3(b) shows, that the initially smooth and homogenous material exhibits dark spots after one day in electrolyte, which are a sign for roughening of the surface. After 7 days, the layer appears completely black in the optical micrograph. The average film thickness remains approximately constant, but the resistivity increases after one day to 5×10^4 Ωm, which is basically insulating. By covering the GaZnO layer with 20 nm of SnZnO the degradation of the material in electrolyte can be prevented. While the bulk of the material remains unaffected, the edges of the GaZnO are underetched several microns after one day. *I-V* measurements revealed no change in the conductance of the GaZnO layer, when the underetching is negligible compared to the width of the conduction path.

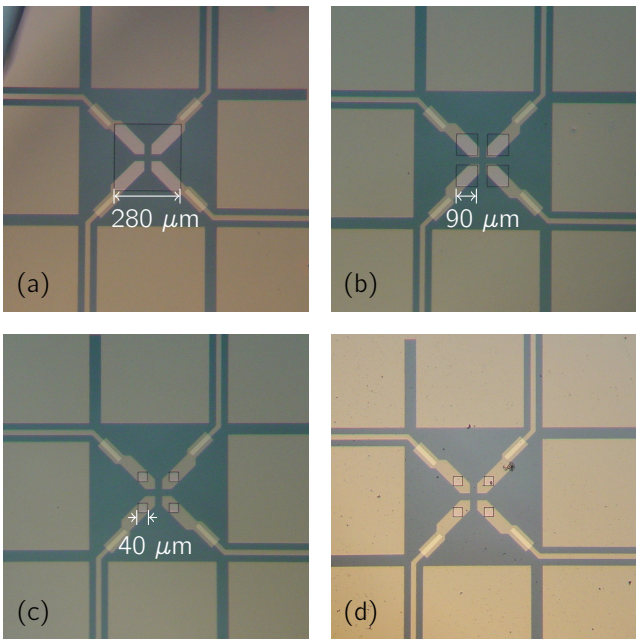

Figure 5.4.: Optical micrographs of a test chip for measuring the SU-8 stability in electrolyte (deionized water with 150 mmol NaCl). (a)-(c) Different electrode sizes, images taken before measurement series. (d) Small electrodes after 7 days in solution.

Besides the conductive materials in contact with the electrolyte, which are used for the signal transmission, an insulation layer must cover the remaining parts of the chip. The suitability of various materials under cell culture conditions was evaluated by Faßbender *et al.* [122]. They found, that the insulating properties of single layers of SiO_2 and Si_3N_4 fail after few hours of cell culture. Better results were obtained with epoxy based organic layers and polyimide, which failed after about 500 hours. The best results were obtained by multiple layers of SiO_2 and Si_3N_4, which were annealed at several hundred degree Celsius.

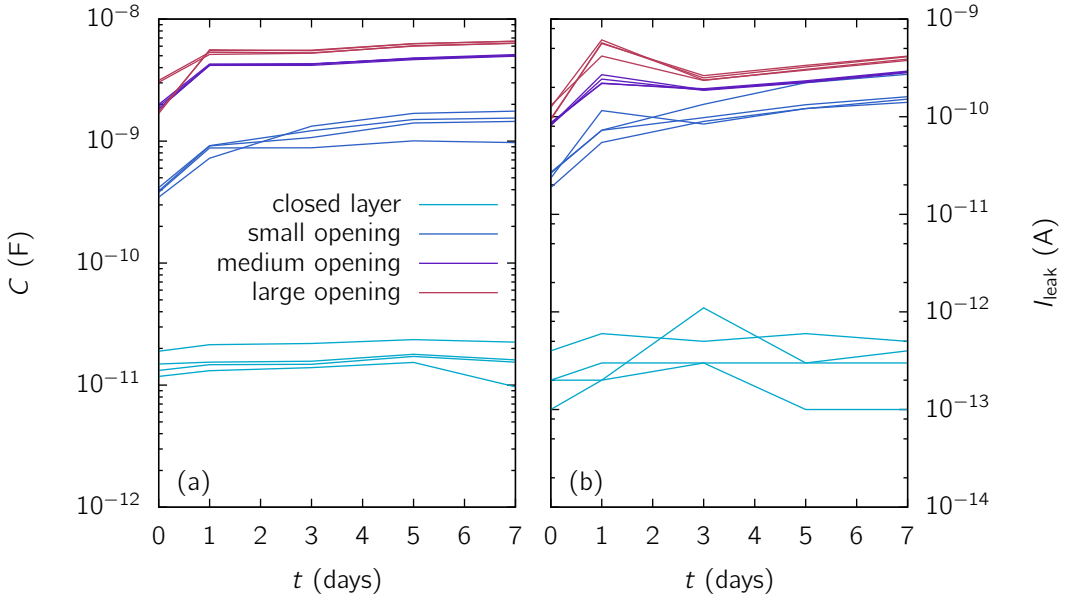

Figure 5.5.: Capacitance (a) and leakage current (b) of partially SU-8 covered electrodes in contact to electrolyte (deionized water with 150 mmol NaCl) during one week, measured by QSCV.

Experiments presented in section 3.3.3 of this work revealed, that the passivation of ZnO-based MESFETs with PECVD grown SiO_2 and Si_3N_4 lead to a serious degradation of the devices. Furthermore, annealing of the insulation layers is not feasible, due to the limited temperature stability of the ZnO based transistors. Experiments with insulators like $CaHfO_3$ and Al_2O_3 grown by PLD at room temperature showed, that the electrical insulation is often locally penetrated by droplets, particles with diameter in the range of the film thickness originating from the PLD targets. Thus, for the insulation of ZnO based MEAs with inorganic materials a multistep approach would be necessary. $CaHfO_3$ could be facilitated for device passivation, followed by multiple layers of SiO_2 and Si_3N_4 for protection from the electrolytic cell medium.

Alternatively organic materials can be used for insulating layers. Requirements are the possibility to structure these materials by photolithographic methods, as well as resistance against organic solvents used for cleaning. These criteria are met by the SU-8 resist, an epoxy based negative photoresist. The good passivation properties of SU-8 for ZnO based MESFETs were already demonstrated in section 3.3.3. After exposure, development, and an additional annealing step at 90°C the material is also resistant against most organic solvents like isopropanol or acetone. The processing of the SU-8 resist on transparent substrates can be challenging, but is possible with suitable optimizations as described in section 2.1.4.

The stability of a SU-8 capping layer was tested with an electrode chip in a 150 mmol NaCl solution by measuring capacitance (Fig. 5.5(a)) and leakage current (Fig. 5.5(b)) of the electrodes via QSCV. The gold electrodes had each the same size, but different sized openings in the SU-8 layer to the electrolyte. Fig. 5.4 show optical micrographs of the electrode areas. The openings are classified as large (8400 μm^2), medium (5000 μm^2), small (1600 μm^2), and closed (no opening). Both capacitance and leakage current show clear difference between the fully covered electrodes and electrodes in contact with the electrolyte. The covered electrodes exhibit a constant capacitance between 10 and 20 pF for the whole week. The leakage current was below 1 pA, at the resolution limit of the measurement unit. The average capacitance per area of the electrodes exposed to electrolyte changed from about 0.3 pF/μm^2 at the first day to 1 pF/μm^2 after one week. Also the leakage current increased by a factor of roughly 3. The capacitance increases actually about 2 times for the large and 4 times for the small openings, indicating that the change might be related to the edge of the openings. Thus, a certain security distance between openings and sensitive structures below the SU-8 layer should be considered. Otherwise SU-8 provides stable insulation during one week. Optical micrographs of the chip after one week in electrolyte showed no visible degradation of the SU8 edges (see Fig.5.4(c)). Crosstalk from capacitive coupling between electrolyte and insulated conduction paths should be negligible, due to the low capacitance of the covered electrodes.

5.2.2. Biocompatibility

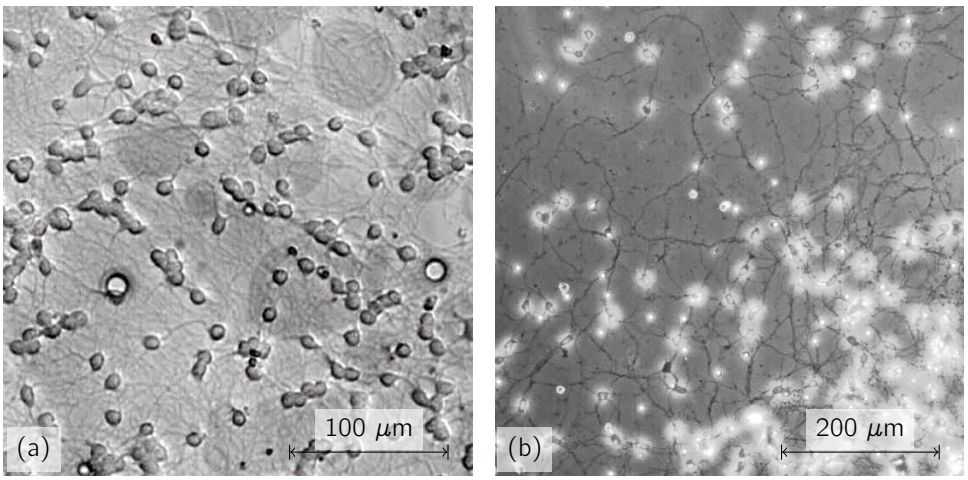

Figure 5.6.: Optical micrographs of primary neurons from mouse cerebellum on test chips. (a) On a SU-8 insulating layer after 3 days, and (b) on PECVD grown Si_3N_4 after 4 days in culture. Both images were recorded by inverted microscopes (view from below).

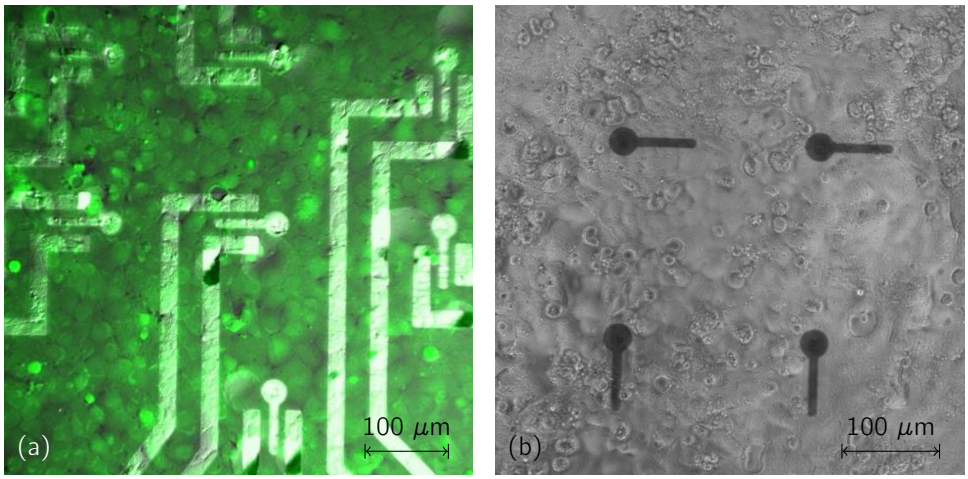

Figure 5.7.: Optical micrographs of cultures of the HL-1 cardiac muscle cell line on ZnO based MEAs. (a) Cultured in the FZ Jülich with calcein staining to prove the cell viability, on a chip with Au conduction paths. The image was taken in top view. (b) Cultured in the BBZ Leizig on a chip with GaZnO conduction paths. The image was recorded in bottom view (inverted microscope).

The compatibility of the ZnO based MEAs with cell culture has been examined with the cardiac muscle cell line HL-1 as well as with primary neurons from mouse cerebellum. For cell culture, glass rings were mounted on the chips with silcon rubber, providing vessels with an inner diameter of 6 mm and with a height of about 8 mm. For the HL-1 cultures the chips were coated with fibronectin and gelatine, for the primary neurons with poly-d-lysine and laminin.

Primary neurons from mouse cerebellum were kindly provided by Prof. Dr. Thomas Claudepierre (Faculty of Medicine, Universität Leipzig) and cultivated in collaboration with Sebastian Schmidt (Soft Matter Physics Group, Universität Leipzig), using the cell culture protocol attached in Appendix C. Images of the primary cells on test structures are shown in Fig. 5.6. HL-1 cell culture tests were performed by Astrid Müller and Heinz-Georg Jahnke from the group of Prof. Dr. Andrea A. Robitzki (Division of Molecular biological-biochemical Processing Technology (BBZ), Universität Leipzig) as well as by Jan Schnitker from the group of Prof. Dr. Andreas Offenhäusser (Peter Grünberg Institute (PGI-8), Forschungszentrum Jülich). Images of HL-1 cells on SU-8 covered MEAs are shown in Fig. 5.7.

The images demonstrate, that the SU-8 and SiN insulating layers provide suitable substrates for cell culture and none of the used materials exhibit signficant neurotoxic effects. The presence of action potentials in the primary neuron networks could not be confirmed, due to the lack of equipment for patch-clamp or similar methods at Leipzig's

Physics Institutes. The electrical activity of HL-1 cells was proven by optically visible contractions of the cell layers.

5.3. Electrode Arrays with Field-Effect Transistors

5.3.1. Layout and Fabrication

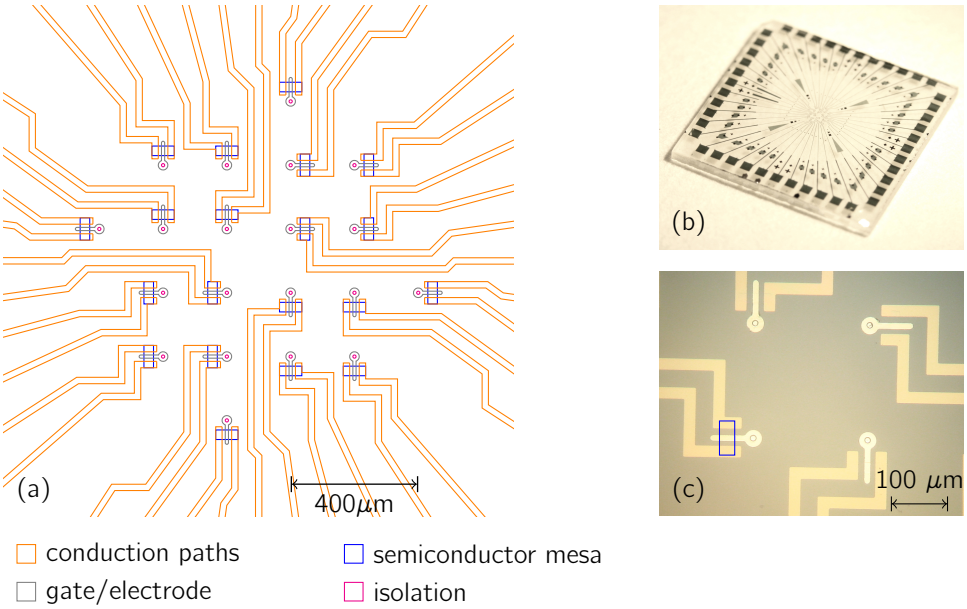

Figure 5.8.: Layout of a MEA with 20 FETs. (a) Schematic drawing of the electrode area. (b) Photograph of a chip with a total size of 10×10 mm^2. (c) Optical micrograph of the inner electrodes. The position of one of the optically transparent ZnO channels is marked by a blue rectangle.

For the fabrication of ZnO based MEAs a layout with 20 transistors in a rectangular grid with a distance of 200 μm between the electrode sites was designed. The layout is illustrated in Fig. 5.8. Due to the high solubility of ZnO the electrode sites were placed beside the actual transistor gate area, as pinholes in the metal could otherwise lead to damages in the transistor channel. The FETs have a nominal gate width of 30 μm, which is reduced to an actual width of about 22 μm due to underetching. The openings in the insulation layer have a diameter of 10 μm.

The fabrication of the devices is in detail described in Appendix B. The first step is the deposition the ZnO channel layer. Then, metal alignment markers are fabricated, which

are used for the orientation of the subsequent steps. The etching of the ZnO layer is done in two steps. First the actual channels are structured with a short UV illumination time, in order to obtain a good optical projection from the photomask on the resist. In the second step, with very long exposure time, ZnO is removed around the chip edges, where the resist has a higher thickness due to the so-called edge bead formation. The conducting paths for source and drain in the center of the chip are fabricated separately from the paths close to the chip edges, since the inner conductors must be optimized for cell culture conditions and the outer parts for high electrical conductance and robust contacting. The last steps are the fabrication of the gate contacts and the deposition of the insulationg layer. Further steps included in the design were an additional electrode mask, which would enable the selection of the material in contact to the electrolyte independently of the gate material, and a passivation layer deposited before the final insulation. Experiments conducted with these additional two steps showed no decisive improvements of MEA properties, and were thus omitted in the fabrication of most chips. Altogether, seven lithography steps were necessary for a typical fabrication process.

The MEAs presented in the following had reactively sputtered Pt gates on a ZnO channel with small Mg content, as described in the previous chapters. The Pt gates were capped with few nanometers of gold, which improved the processing of the SU-8 insulation layer. The outer conduction paths consisted of Au with a thickness of 30 nm. The inner conduction paths were either made from Au with a thickness of 20 nm or from 100 nm thick GaZnO.

5.3.2. Electrical Characterization and Stability Issues

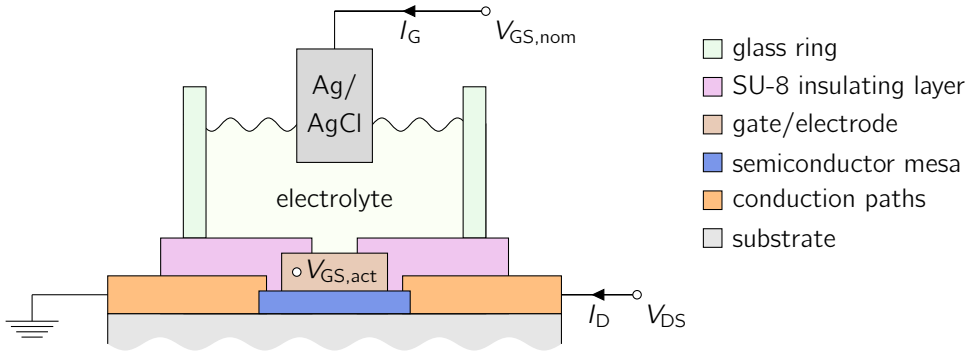

Figure 5.9.: Measurement principle for electrical characterization of MEAs with electrolyte, simplified for this schematical 2d drawing (compare Fig. 5.8). The actual gate voltage $V_{GS,act}$ is not applied externally, but arises according to the external voltages $V_{GS,nom}$ and V_D.

When using the term "measured in/with electrolyte", the transistor channels are insu-

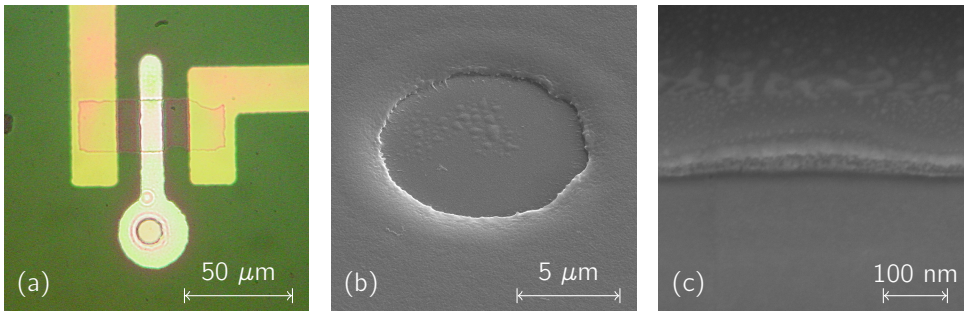

Figure 5.10.: MEA electrode after a single transfer measurement with V_{GS} between 2 V and -3 V. (a) Optical micrograph. (b) SEM image of the electrode. (c) SEM cross section image of one of the bumps in the electrode area.

lated from the liquid by the SU-8 layer. The gate voltage is applied via an Ag/AgCl-electrode at the electrolyte and couples to the transistor gate through openings in the SU-8 layer, where gate electrode and electrolyte are in direct contact (in the following called electrode/electroyte interface). The measurement principle is illustrated in Fig. 5.9. The electrolyte used for characterization of the MEAs was phosphate buffered saline (PBS). PBS is available from many vendors, who specify the conductivity in the range of 14 to 18 mS/cm. Taking a distance between chip and Ag/AgCl electrode of 5 mm, an Ag/AgCl electrode diameter of 1 mm and an electrode diameter on the chip of 10 μm, the electric resistivity of the electrolyte between chip and Ag/AgCl electrode can be estimated to be around 40 kΩ, when the current is assumed to flow through the volume of a truncated cone with the circular electrodes as side facets. Even for large gate leakage currents in the 10 nA range the voltage drop across the electrolyte is in the millivolt range, and thus negligible. Hence, deviations from the device characteristics measured without electrolyte originate from the electrode/electrolyte interfaces, assuming the FETs are sufficiently insulated by the SU-8 layer and retain their actual characteristics. The deviations can be described by the nominal gate voltage $V_{GS,nom}$, which is applied externally at the Ag/AgCl electrode, in relation to the actual gate voltage $V_{GS,act}$, which appears directly at the transistor gate. If the term V_{GS} is used in the following, always the voltage applied at the Ag/AgCl-electrode is addressed.

Transfer characteristics of the devices in electrolyte were recorded by applying the gate voltage at the Ag/AgCl-electrode. It has been found, that the appliance of positive voltages somewhat larger than 0.5 V at the Ag/AgCl-electrode leads to rapid degradation of the MEA electrodes, as depicted in Fig. 5.11. The SEM image gives the impression of a metal layer, that is cracked and bent upwards. This indicates, that the capping Pt layer sputtered at Ar atmosphere is less affected, but the reactively sputtered PtO_x below is taking part in an electrochemical reaction. If the chip potential is sufficiently negative compared to the electrolyte, H_2 is produced at the chip electrodes and also PtO_x might be reduced to elemetary Pt under the formation of OH^-. Fig. 5.10 shows

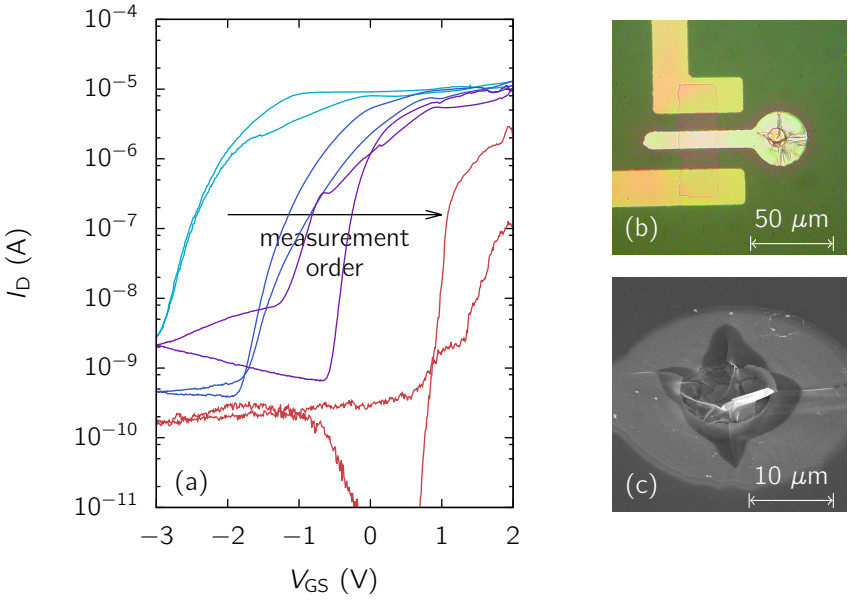

Figure 5.11.: Destroyed MEA electrode due to positive electrolyte voltages. (a) Series of transfer measurements on the same FET, causing rapid degradation. (b) Optical micrograph after the measurement series. (c) SEM image after measurement.

an electrode after only one transfer measurement, which exhibits several bubble-like features. The electrolyte probably reaches the PtO_x layer locally through pinholes in the Pt layer. Due to gas production the Pt capping layer will eventually burst open, leading to the destruction of the electrode as shown in 5.11(c). The microscopic images gave no hint of a destruction of the FET channel, which is likely due to the reduced current in Fig. 5.11(a). Possibly the decomposition of PtO_x allows the electrolyte to spread beneath the Pt capping layer, reaching the ZnO channel and dissolving it gradually. The intact Pt top layer makes it diffcult to monitor this process.

MEAs fabricated with gold conducting paths suffered from a very high grade of variations in the FET properties when measured with electrolyte (Fig. 5.12(a)), especially concerning threshold voltage and ON/OFF-ratio. Good homogeneity of the actual transistor properties was verified by *I-V* measurements without electrolyte and using a wafer prober. The reason for the apparent changes of the FETs when measured with electrolyte was found to be the upbending of metal at the edges of the conducting paths, as described in section 2.1. This seems to disturb the spread of the SU-8 insulating layer and leads to shortcuts to the electrolyte. The delamination of conducting paths during one week of cell culture, as shown in Fig. 5.13(a), is also attributed to an incomplete SU-8 coverage at the edges of the Au structures. Partly responsible is the weak adhesion strength of gold on sapphire [123]. Also the positive photo resist AZ 1514H used for

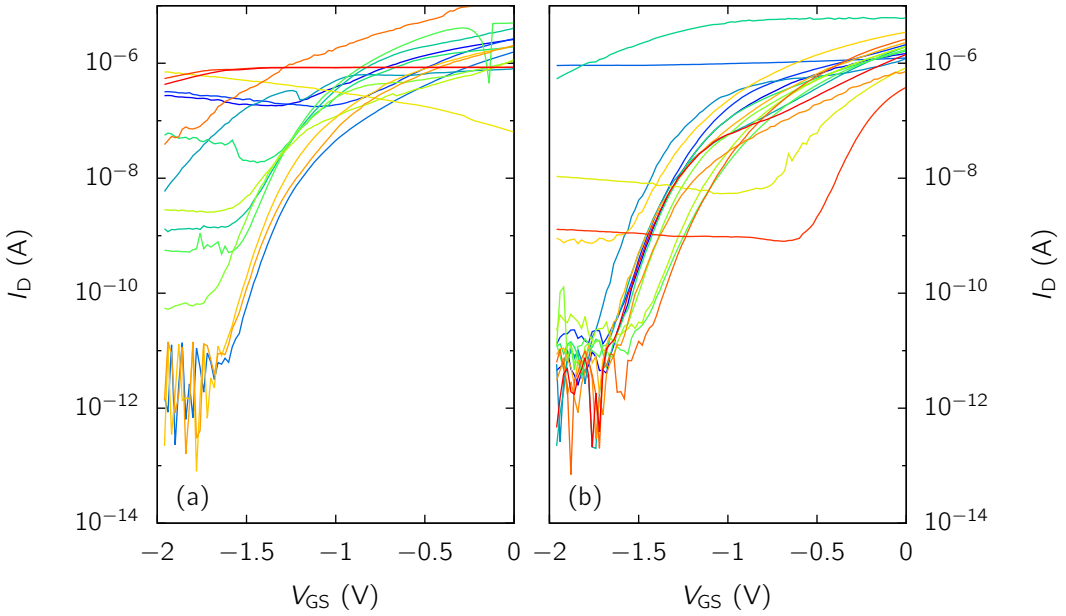

Figure 5.12.: Comparison of two MEA chip with Pt gates and conduction paths made of (a) Au and (b) GaZnO. Shown are the transfer characteristics of all FETs on each chip, measured in electrolyte.

this work is not the best choice for lift-off processing. Probably better results could be obtained with a negative photo resist specially designed for lift-off.

An alternative conducting path material is gallium doped zinc oxide (GaZnO). This material was grown by PLD at room temperature and 0.002 mbar oxygen pressure, using a ZnO target with 4wt-% Ga_2O_3. The film thickness was about 100 nm. GaZnO is more brittle than gold and breaks without upbending at the edges during lift-off. This was verified by SEM images of FIB prepared cross sections. MEAs with such conduction paths had a much better homogeneity concerning the FET characteristics measured with electrolyte, as shown in Fig. 5.12(b). Although 5 of the 17 transistors shown seem to be damaged, the remaining 12 devices exhibit very similar characteristics. For the chip with Au paths presented in Fig. 5.12(a) only 3 of the 15 transistors shown had comparable characteristics. In cell culture experiments the GaZnO paths degraded after several days in electrolyte, so that no current was measurable between the source and drain contacts. Due to the optical transparency of GaZnO, the degradation was not directly observable in optical micrographs. However, bubbles with diameters around 10 μm were lining the conduction paths. In SEM images a change of contrast of the GaZnO around this bubbles is visible (Fig 5.13(b)). Cross section images verified, that indeed hollows were formed beneath the SU-8 layer at the conduction path edges, partially filled with crystallites (Fig 5.13(c)). Liquid from the electrolyte must have reached and dissolved the GaZnO layer, forming crystallites after the cell culture during drying. It had been

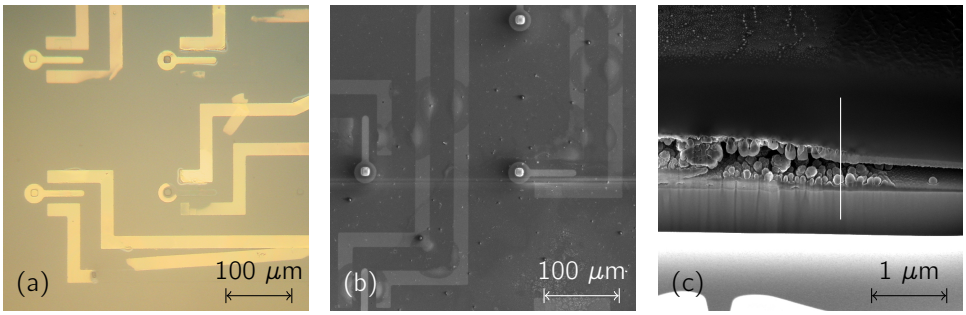

Figure 5.13.: Degradation of conduction paths during cell culture. (a) Optical micrograph, showing delamination and dissolution of gold conduction paths. (b) SEM image revealing the dissolution of GaZnO paths. (c) SEM cross section through a dissolved GaZnO conduction path, which was originally left of the white line. Below the cleft is the sapphire substrate, above the SU-8 insulation.

shown in a previous section, that GaZnO layers directly exposed to PBS degrade within few days. It is surprising, however, that this degradation occurs also beneath a SU-8 layer, that exhibits no openings visible by SEM. While ZnO is even more sensitive to PBS exposure, the transistor channels do not exhibit any degradation when covered by SU-8. Possibly the SU-8 polymer layer is saturated by water to some degree. While the crystalline ZnO layers are rather smooth and compact, the room temperature grown GaZnO might offer more surface features like crevices where the liquid can attack the material. The degradation of GaZnO can be prevented by covering it with about 20 nm of room temperature deposited SnZnO. While this double layer exhibited underetching when directly exposed to PBS, no degradation is observed beneath a SU-8 layer. The double layer of 100 nm GaZnO and 20 nm SnZnO was used for the conducting paths of MEAs used in the following measurements.

Repeated measurements of the transfer characteristic with the gate voltage applied at the electrolyte exhibit often significant changes between the first runs, but stable characteristics after about 3 measurements. This is demonstrated by Fig. 5.14. The threshold voltage and the transconductance increase gradually during measurement, until stable conditions are reached. In some cases, here represented by Fig. 5.14(c), the transfer characteristic is initially completely flat, which means that no signal can be transmitted from the electrolyte to the drain current. In many cases repeated measurements down to large negative gate voltages (<-1 V) will lead to a sudden decrease in the current, after which a transfer characteristic with an ON/OFF-ratio of several orders of magnitude is obtained. Some FETs, however, will retain the constant transfer curves and are not sensible to any signals applied at the electrolyte. One can speculate, that some physical obstacle must block the signals, like an insulating layer covering the electrodes or a disruption of the metal path between electrode and transistor gate. However, neither

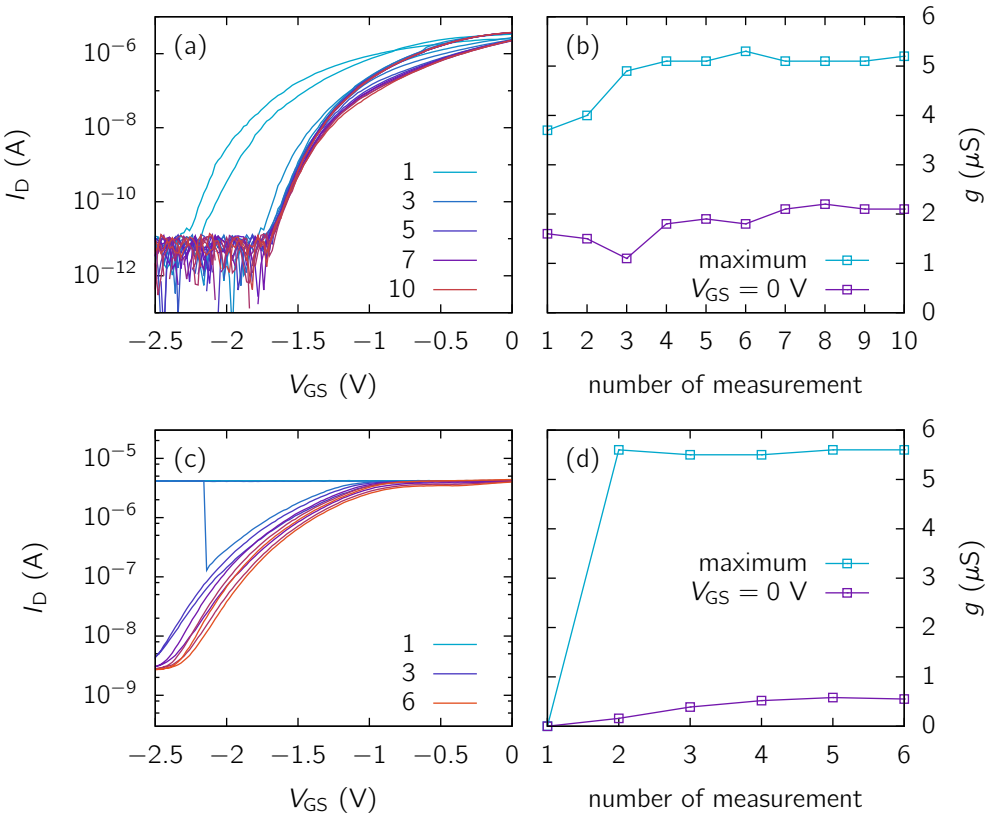

Figure 5.14.: Repeated transfer measurement on FETs in electrolyte. (a) and (b) as well as (c) and (d) refer to the same FET, respectively.

optical micrographs nor electron microscopy images showed significant differences between sensitive and non-sensitive electrodes. Leaving the chips immersed in isopropanol for several hours can induce signal sensitivity for some transistors. Interestingly also the opposite behavior has been observed few times, where previously sensitive FETs obtained flat transfer characteristics after isopropanol cleaning without any mechanical damage. Generally such a long cleaning step is beneficial to the overal chip performance. An example for the sensitivity of a chip before and after cleaning is presented in the next section. It was not possible during this work to clarify the reason for the changing sensitivity of the electrodes. It is assumed, that the origin is most probably at the electrode/electrolyte interface. Changes at the actual transistor site would most likely lead to a change of the FET's ON-current, which is not observed. Changes at the Ag/AgCl-electrode or in the electrolyte would affect all FETs equally. It was suspected, whether air residues in the electrode holes could be responsible, however drying and refilling of the electrolyte vessel preserves the measured characteristics in nearly all cases. Thus, it can only be concluded, that several hours of immersion in an organic solvent and transfer measurements to gate voltages <-1 V are recommendable before further use of such chips. The clarification of this issue is vital, however, if one aims for the application of

ZnO based MEAs.

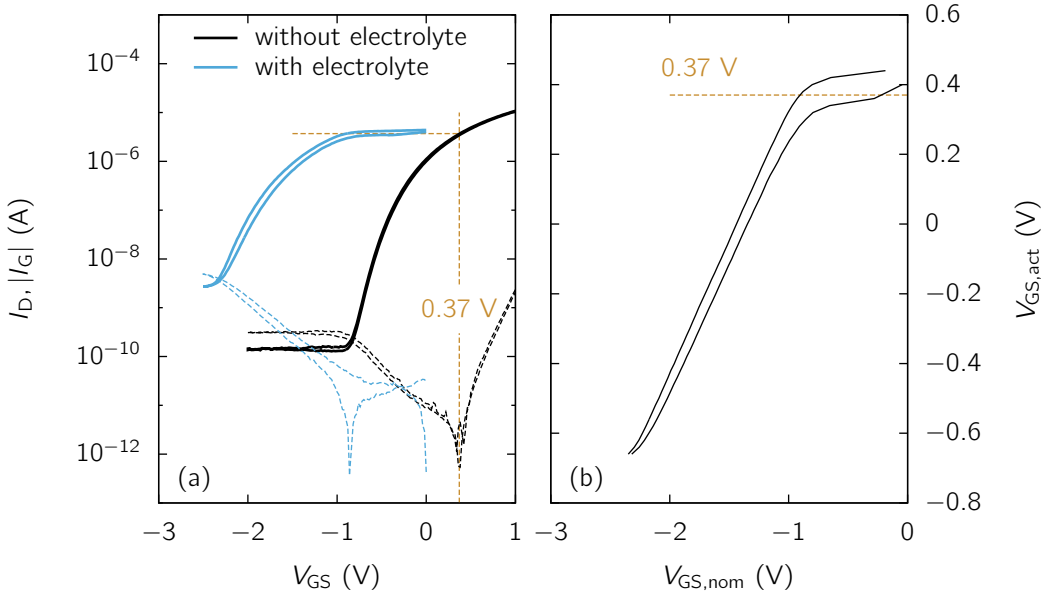

Figure 5.15.: (a) Comparison of transfer characteristics of the same MESFET measured without electrolyte (before SU-8 deposition) and with electrolyte. The drain currents are depicted by solid lines, the gate currents dashed. The vertical dashed line marks the voltage $V_{GS} = 0.37$ V, where the gate current is zero. (b) Relation between the nominal and the actual gate voltage ($V_{GS,nom}$ and $V_{GS,act}$, respectively), calculated from the transfer characteristics shown in the left part of the figure.

The measurement of the transfer characteristics from the MEA transistors without electrolyte is challenging, as the gate contacts are quite small compared to usual needle size of a wafer prober. Thus, the measurement is time consuming and electrode or FET can be easily damaged. After SU-8 application, contacting of gate electrodes is not possible without mechanical removal of the SU-8 layer covering the electrodes. Nevertheless, few FETs of each chip were usually characterized before SU-8 coating, to compare the characteristics with and without electrolyte. Exemplarily this is shown in Fig. 5.15(a). With electrolyte the threshold voltage is shifted to more negative values and the curve is flattened close to $V_{GS} = 0$ V. Comparison with the characteristic recorded without electrolyte shows, that in this voltage range the FET assumes an operation condition where the gate current is nearly zero. In Fig. 5.15 this is illustrated by the brown dashed lines. This means, that the gate is essentially electrically insulated from the electrolyte and the FET operates under floating gate conditions, where the actual gate voltage $V_{GS,act}$ is only determined by V_{DS} and not by the electrolyte potential. Under the assumption, that the FET properties were not substantially altered by the SU-8 layer and further contacting and encapsulation steps, the dependency of $V_{GS,act}$ on the voltage $V_{GS,nom}$ applied at the

Ag/AgCl-electrode can be calculated from both transfer characteristics. Value pairs at the same drain current connect the gate voltage from the measurement with electrolyte, which equals $V_{\mathrm{GS,nom}}$, with the gate voltage from the measurement without electrolyte, which equals $V_{\mathrm{GS,act}}$. The result is displayed in Fig. 5.15(b) and demonstrates, that between $V_{\mathrm{GS,nom}} = 0$ V and $V_{\mathrm{GS,nom}} \approx -1$ V the actual gate voltage is nearly constant. For more negative voltages the electrode/electrolyte interface becomes conductive, enabeling the control of the channel current by the electrolyte potential. This increase in conductivity is probably due to the electrolysis of water.

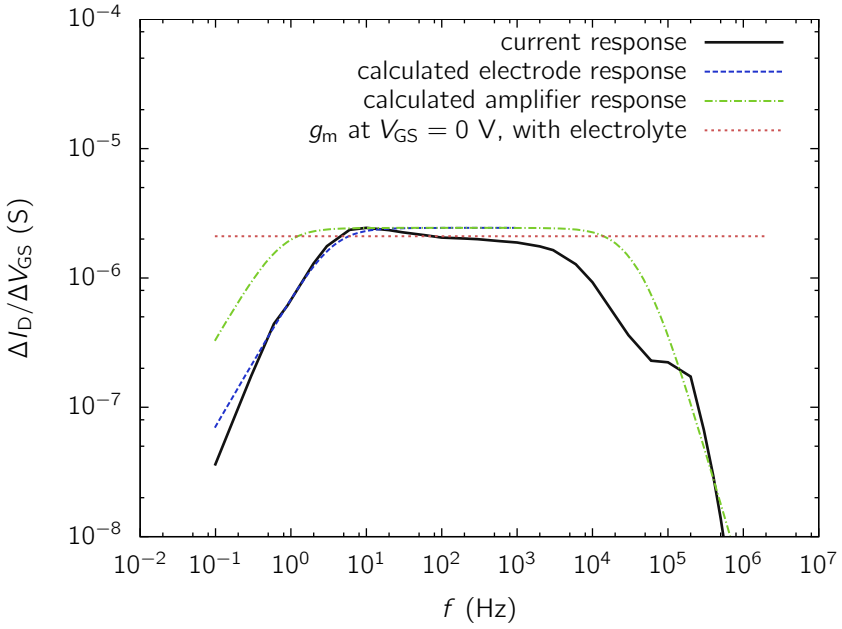

Figure 5.16.: Response of the transistor drain current on sinusoidal voltages applied at the Ag/AgCl electrode in PBS, determined in dependence on the stimulation frequency. The signal amplitude was 20 mV, the offset voltage 0 V. The transfer characteristic of the FET used for this measurement is shown in Fig. 5.14(a).

The very low slopes exhibited by the transfer characteristics measured with electrolyte close to $V_{\mathrm{GS}} = 0$ V, as shown in Fig 5.15, can be related to the comparably long recording time of such measurements. Although the integration time is selected below 1 ms, the adjustment of the correct measurement range for each sample extends the total measurement time to many seconds. This raises the question, whether the transconductance obtained from the transfer characteristic is a good measure for the transmission of signals at higher frequencies. For a better evaluation of the sensitivity with electrolyte, the response of the FETs drain current on sinusoidal voltage signals with varying frequency applied at the Ag/AgCl electrode was measured. The result shown in Fig. 5.16 demonstrates, that the signal is damped below a cutoff frequency of about 7 Hz. However, the lack of dc current conductivity across the interface between MEA electrode and elec-

trolyte does not hinder the transfer of ac signals. The cutoff frequency can be modelled by a simple RC high-pass filter, when the FET's gate capacitance of about 1 pF and the differential resistance of the gate diode close to the zero crossing of the gate current are used. It is interesting, that the limit seems to be determined by the gate capacitance, and not by the capacitance of the electrode interface, which is at 15 pF. Probably the equivalent circuit of two capacitors in series can be applied here, where the lowest capacitance dominates the total capacitance of the system. In Fig. 5.16 the transconductance g_m obtained from the FET's transfer characteristic measurements with electrolyte at $V_\mathrm{GS} = 0$ V is depicted. g_m matches well with the frequency dependent measurement in the range between 10 Hz and 1000 Hz. Thus, for this device the transfer characteristics gave the right magnitude for the transmission of signals up to the kHz range. However, due to the diverse characteristics observed for different MEAs in this work, the frequency dependent characterization should not be omitted.

5.3.3. Noise and Sensitivity

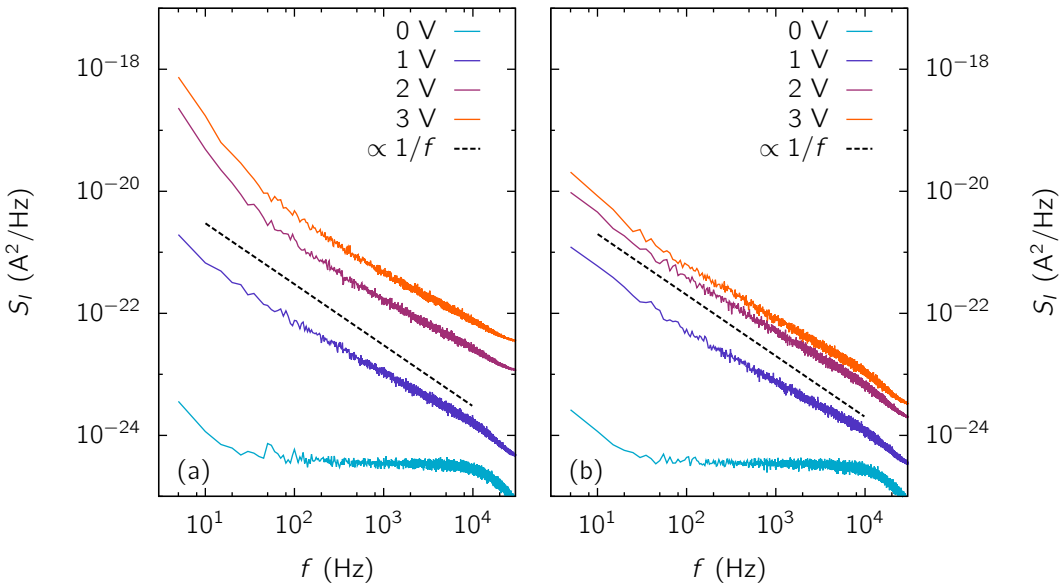

Figure 5.17.: Power spectral density of the drain current noise of a MEA with ZnO based MESFETs with Pt gate. (a) Without electrolyte (floating gate). (b) With PBS and 0 V applied at the Ag/AgCl-electrode.

The sensitivity of the devices is limited by the noise observed in the drain current of the transistors. Without electroyte the FETs have a floating gate, as described in section 4.4.2. The corresponding noise spectrum is shown in Fig. 5.17(a). The FET noise examined in section 4.4.2 for floating gate conditions was dominated by gate voltage

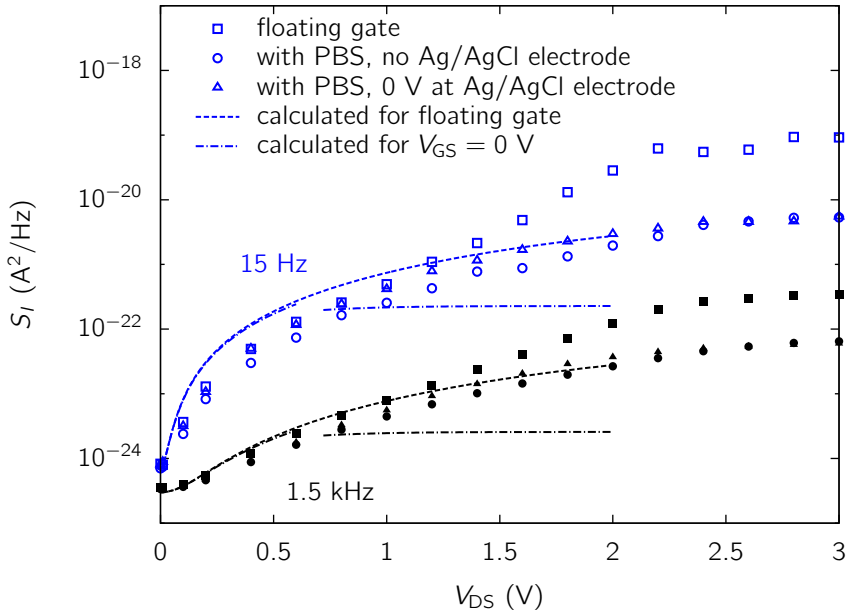

Figure 5.18.: Power spectral density of the drain current noise at two different frequencies. Shown are the measured values with floating gate, with PBS but no applied voltage, and with PBS and 0 V applied at the Ag/AgCl-electrode. The calculations are based on the measured output characteristics with floating gate and with $V_{GS} = 0$ V, according to Eqn. 4.13.

fluctuations, which were superimposed by a low-pass filter formed by gate capacitance and resistance. This caused a $1/f$ trend for low frequencies and $1/f^3$ behavior for most of the measured frequency range (see Fig. 4.18). Here, this seems reversed, with most of the spectra close to $1/f^{0.9}$ and for high bias voltages and low frequencies a proportionality to $1/f^2$. This can be explained by the assumption, that the cutoff frequency f_0 of the gate low-pass filter is at very low frequencies, below the lower limit of the measurement range. f_0 is proportional to the bias voltage, thus the shoulder of the filter is only visible for high bias voltages. The origin of the remaining noise with near $1/f$ proportionality becomes clear in Fig. 5.18, where the power spectral density at two selected frequencies is shown. Up to about 1.2 V the measurement follows closely the calculation according to Eqn. 4.13, which is based on the measured drain current with floating gate. This means, that in this range only current noise as described for FETs with fixed gate potential is observed. However, in contrast to fixed V_{GS} the saturation regime is not reached with floating gate, which is demonstrated by both calculations in Fig. 5.18. For bias voltage larger than 1.2 V an additional noise contribution arises, which is attributed to the gate potential fluctuations mentioned before.

When PBS is filled into the culture vessel, a significant reduction of the noise is observed. Fig. 5.17(b) shows, that the proportionality is close to $1/f$ in the entire frequency range

for non-zero bias voltages. Fig. 5.18 reveals, that S_I is now also for higher bias voltages dominated by the current noise, and gate voltage fluctuations seem to be negligible. However, the device is still in floating gate mode, as no saturation is oberved. This is due to largely capacitive coupling at the electrode/electrolyte interface. The electrolyte potential does not influence the dc gate potential, but can damp the fluctuations of the gate voltage at higher frequencies. Interestingly it does not matter, whether the electrolyte is grounded by the Ag/AgCl electrode or not. Probably the adjacent FETs, whose source contact is always connected to ground, provide the reference potential to the electrolyte.

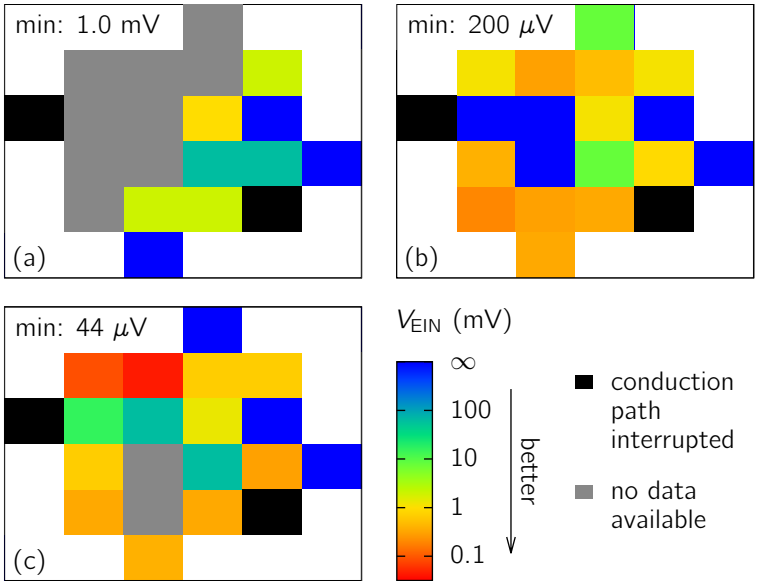

Figure 5.19.: Equivalent input noise of a MEA chip in electrolyte with Pt gates and GaZnO conducting paths, measured (a) before transfer measurements, (b) after transfer measurements, (c) after one day in isopropanol. Each colored rectangle represents one of the 20 FETs on the chip. Dark blue color indicates, that no signal was transduced by the FET. The mimimum values observed for V_{EIN} are given inside each graph.

The resulting sensitivity of the ZnO-based MEAs to variations of the electrolyte potential is represented by the equivalent input noise V_{EIN}, which can be understood as lower limit for the amplitude of detectable signals. It was determined by recordings of the drain current at 50 kHz for the duration of 40 ms, either with constant electrolyte potential or with rectangular voltage pulses applied at the Ag/AgCl electrode. The pulses had amplitudes of few millivolts and a period of 1 ms. The measurements at constant potential were used to obtain the noise level, the voltage pulses to calculate the actual transconductance of the electrolyte/FET system at 1 kHz. The measurements are presented in Fig. 5.19 for a ZnO based MEA with Pt gates and GaZnO conduction

paths. Measurements were conducted directly after the first filling with PBS and again after transfer measurements from $V_{GS} = 0$ V to -2.5 V. A third series of measurements was performed after immersion in isopropanol over night (about 24 hours).

The measurements demonstrate, that the sensitivity of the electrodes are subject to significant variations. After each series of measurements more FETs are sensitive to the voltage signals and the minimum V_{EIN} observed decreases strongly, however the variance remains large even after immersion in isopropanol. In the last measurement series, only 6 transistors exhibited a V_{EIN} below 500 μV, and only 2 FETs below 100 μV. It is clear, that only strong cell signals in the range of several hundred microvolts can be detected with sufficient confidence. Especially signals from primary neurons, with expected signal amplitudes of maximum few 100 μV, are beyond the achievable sensitivity range of the ZnO based MEAs in the present configuration.

5.3.4. Electrical Measurements on HL-1 Cells

Several attempts to measure electrical signals from HL-1 cells were made. Altogether about 20-30 times HL-1 cells were cultivated on MEAs with ZnO based MESFETs. Generally, not every culture yields a confluent cell layer with strong contractions, and such contractions occur sometimes only locally. Nevertheless, on several occasions contractions at electrode sites could be observed, indicating the existance of measureable electrical activity. Still, no signal was measured, which could be definitely attributed to a cell's action potential. Most likely the inhomogenous sensitivity of the chips plays a major role. When only few transistors exhibit a sufficient signal-to-noise ratio, the probability is low, that a group of strongly signaling cells is close to the respective electrodes. Besides, for the signal strength measureable by the transistor it is critical, whether a cell is completely sealing the electrode or whether it is covering the electrode only partly. This degree of freedom reduces the probability even more, that a sufficiently strong signal occurs at same place as a sufficiently sensitive transistor. A proof-of-principle measurement of cell signals with the MEAs presented here might still be possible. However, a better understanding of the electrolyte/electrode coupling and an improvement of the sensitivity and its homogeneity should be achieved, in order to obtain reliable results from measurements with living cells.

5.4. Electrode Arrays with Simple Inverters

The application of simple inverters as amplifying elements was discussed in section 3.4. The integration of simple inverters in MEA chips was examined together with Agnes Holtz in the framework of her master's thesis. The MEA layout from the previous

section was modified, in order to place two transistors with a common channel next to each measurement electrode. The layout is illustrated in Fig. 5.20. The ground connections of all inverters are connected at the chip center to reduce the total number of conduction paths. Each inverter has individual conduction paths for V_{DD} and the output voltage. Besides the different photomasks, the fabrication steps are similar to the MEAs with single transistors.

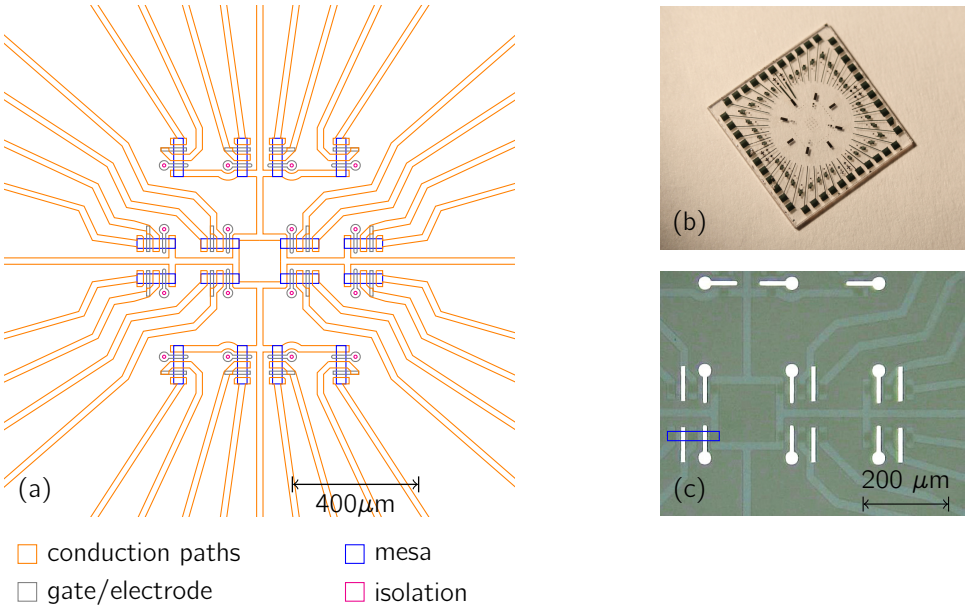

Figure 5.20.: Layout of a MEA with 16 simple inverters. (a) Schematic drawing of the electrode area. (b) Photograph of a chip with a total size of 10×10 mm^2. (c) Optical micrograph of the inner electrodes. The position of one of the optically transparent ZnO channels is marked by a blue rectangle.

Inverter transfer characteristics measured with electrolyte for different gate materials are depicted in Fig. 5.21. The general shape of the curves compared to measurements without electrolyte is reproduced, however with a very large hysteresis for Au and $ZnCo_2O_4$ gates. The inverters with Au gates reach high gain values even with electrolyte. For the presented device $g = 36$ for measurement from positive to negative V_{in} and $g = 56$ in the opposite direction was obtained. The device with Pt gates exhibits a large offset shift to positive voltages. For application of invertes in a MEA, strategies to fix the working point of each inverter at the point of maximum gain must be developed. The offset correction circuit proposed in Fig. 3.31 demonstrates, that this is basically possible. In order to control the offset for each inverter on a MEA individually, individual ground connections instead of individual V_{DD} conduction paths could be used. As the ground contact provides the reference for the input voltage, a small shift in the ground potential would lead to an effective shift of the input voltage of the inverter. As long as the offset

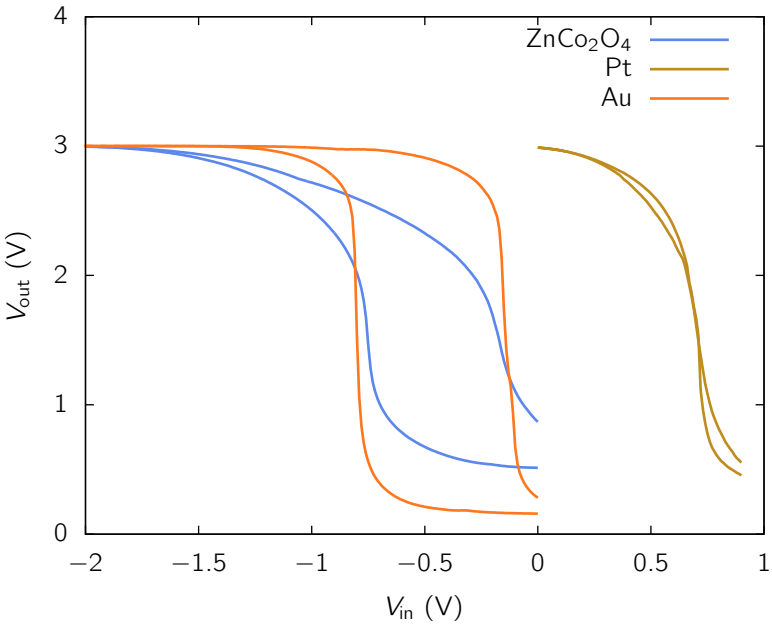

Figure 5.21.: Inverter characteristics measured with electrolyte for different gate materials.

is small compared to V_{DD}, this would not change the inverter characteristics by much.

The hysteresis exhibited by the devices in Fig. 5.21 indicates, that the cutoff frequency of the inverters is lowered even more compared to the measurements presented in section 3.4, when the input voltage is applied at the electrolyte. Furthermore, the low reproducability and homogeneity of the electrolyte/electrode coupling, as discussed in the previous section, affects the MEAs with ZnO based invertes in a similar fashion. This is to be expected, as the MEA layout is similar apart from the additional load transistor, which does not affect the signal transmission from Ag/AgCl electrode to the input transistor. Hence, before the amplification properties of simple inverters can be exploited for cell signal measurements, the coupling between electrolyte and chip electronics must be improved, and the origin of the low cutoff frequencies of the inverters must be clarified.

5.5. Electrode Arrays with Solution Gated Transistors

If the transistor channel material is stable under cell culture conditions, the fabrication of solution-gated FETs (SGFETs, also called electrolyte-gated FETs (EGFETs)) can be aspired. In this case the electrolyte is in direct contact with the semiconductor and the gate is formed by the electrolyte/semiconductor interface. This approach has

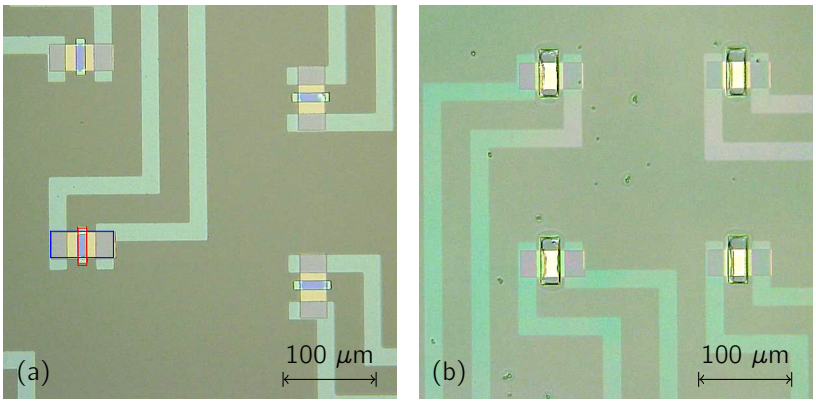

Figure 5.22.: Optical micrograph of a MEA with SGFETs based on ZTO channels. (a) Before SU-8 deposition, showing the ZTO mesa structures (blue rectangle), GaZnO conduction paths, and the ZnO sacrificial structures (red rectangle). (b) Finished SGFETs after SU-8 processing and removal of ZnO.

been successfull reported for AlGaN/GaN heterostructures [20] and for graphene based SGFETs [23]. Similar concepts were tested with wire-like structures, e.g. Si nanowires [21] and carbon nanotubes [124].

As shown previously, ZnO is not a suitable material, as it is not stable in contact with aqueous solutions. Oxide semiconductors with very good resistivity against liquids are zin tin oxide (ZTO) and gallium oxide, which are also resistant against many acids used for wet chemical etching. ZTO is amorphous and can be deposited by PLD at room temperature [125]. Thus, it can be structured with a standard lift-off process. β-Ga_2O_3 is grown by PLD at temperatures above 500°C, if good conductivity is desired [126], making the structuring of such thin films difficult. A method successfully applied is the use of a sacrificial ZnO layer as lift-off mask, which is stable at these temperatures. Because of the more straightforward processibility, ZTO was used in the experiments for this work. Both materials have reduced conductivity for films with thicknesses around 100 nm, when grown by PLD. For ZTO deposited at 0.025 mbar oxygen pressure with thickness between 500 nm and 1 μm resistivities as low as 3×10^{-4} Ωm were reported [125], while for a thin film with 60 nm thickness grown at the same conditions about 10 Ωm were measured. Hall effect measurements yielded $n_H = 2.6 \times 10^{17}$ cm^{-3} and $\mu_H = 2.5$ cm^2/Vs for this film.

The processing of SGFETs seems straightforward when compared to the fabrication of MEAs with MESFETs, as the gate is just substituted by a larger hole in the SU-8 layer above the channel. However, several challenges arose during the implementation of this concept. The adhesion of ZTO is low on glass and also on sapphire substrates, which lead to delamination of the channels during further processing steps. This was

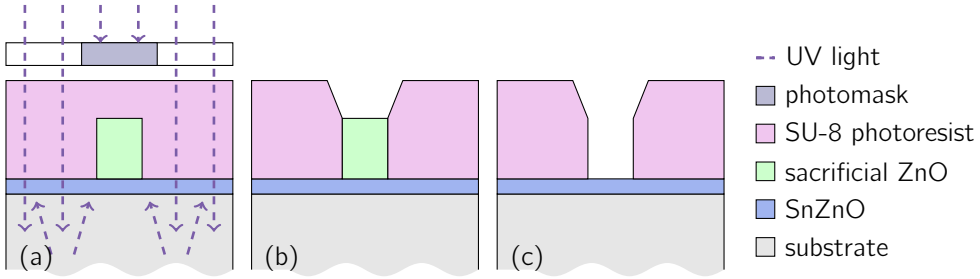

Figure 5.23.: Schematic depiction of the structuring of the SGFET insulation layer. (a) After deposition and structuring of the sacrificial ZnO, the SU-8 layer is applied on the sample and illuminated through the photomask. Stray light from below is absorbed by the ZnO. (b) Development of the SU-8 layer. (c) Removal of ZnO by dilute phosphorous acid.

solved by depositon of few nanometers ZnO below the ZTO thin film. No delamination occured with this material stack, however the ZnO layer might alter the total conduction properties of the channel, when ZTO has a comparably low conductivity. The processing of the SU-8 layer was an additional difficulty, as the resist protected by the photomask during illumination was cured by stray light from beneath. Thus, no openings in the insulation layer were obtained. To prevent the backside illumination, sacrificial ZnO structures were fabricated prior to the SU-8 processing. The procedure is illustrated by Fig. 5.23. The ZnO layer with a thickness in the range of several 100 nm was deposited by room temperature PLD and structured by lift-off, leaving bar-like structures where the openings in the SU-8 layer were planned (see Fig. 5.22(a)). During UV exposure of the SU-8 resist these structures absorb the backscattered radiation, so that the SU-8 layer is protected from both beneath and above. After SU-8 development, the ZnO layer was removed by diluted phosphorous acid, leaving the desired openings in the SU-8 layer. The size of the ZnO bars was chosen slightly smaller than the size of the openings, to facilitate the alignment of the photomasks. The ZnO bars act not only as UV absorber, but take also remaining SU-8 with them, similar to an additional lift-off step. A micrograph of the finished structure is shown in Fig. 5.22(b). The ZTO thin films for the devices presented here were optimized and deposited by P. Schlupp (Universität Leipzig), while the SGFET concept was implemented by Agnes Holtz for her master's thesis.

Transfer measurements were performed similar to experiments with MESFETs. Measurements on 5 different SGFETs from the same sample are shown in Fig. 5.24(a). The characterisics prove, that a field-effect is present and the channel current can be controlled by the electrolyte potential. However, due to the low forward current, caused by the low conductivity of the ZTO thin film, only an ON/OFF-ratio of 10 is observed. The ON-voltage is for all devices around $V_{GS} = 0$ V. The gate potential was increased

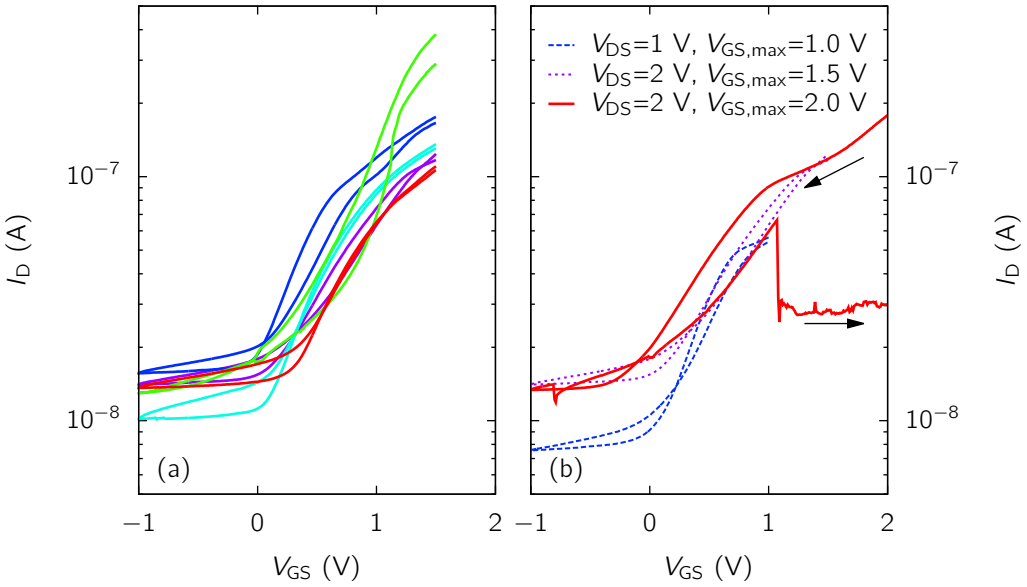

Figure 5.24.: Transfer measurements on ZTO based SGFETs. (a) Five different SGFETs at $V_{DS} = 2$ V. (b) The same SGFET at different operating conditions.

gradually, in order to investigate the maximum operation conditions. For $V_{GS} > 1$ V a non-reversible breakdown occured (Fig. 5.24(b)), probably due to electrochemical degradation of the channel material.

For a better understanding of the coupling between electrolyte and ZTO channel, the signal transmission was investigated frequency dependent. The response of the drain current on sinusoidal electrolyte voltages with an amplitude of 50 mV is shown in Fig. 5.25. The low and high frequency limits observed for all measurements are determined by the MEA amplifier. This is different from the measurements on MESFETs with electrolyte, where the gate capacitance was involved in the low frequency limit. In contrast to the measurements on ZnO based MESFETs, the transmission between these limits is only constant at low frequencies, but exhibits a peak around 10 kHz. The high frequency slope of this peak is determined by the MEA amplifier, while the low frequency slope can be described by a first-order high-pass with a cutoff frequency f_{cap}. It can be attributed to direct capacitive coupling between electrolyte and drain contact, due to the electrolyte/ZTO interface capacitance. With the amplifier gain $G_{amp}(f)$, as described in section 2.3, the gain function for the complete system is given by

$$G(f) = G_{amp}(f) \left(g_{FET}(V_{GS}) + \frac{g_{cap}}{\sqrt{1 + (f_{cap}/f)^2}} \right). \tag{5.3}$$

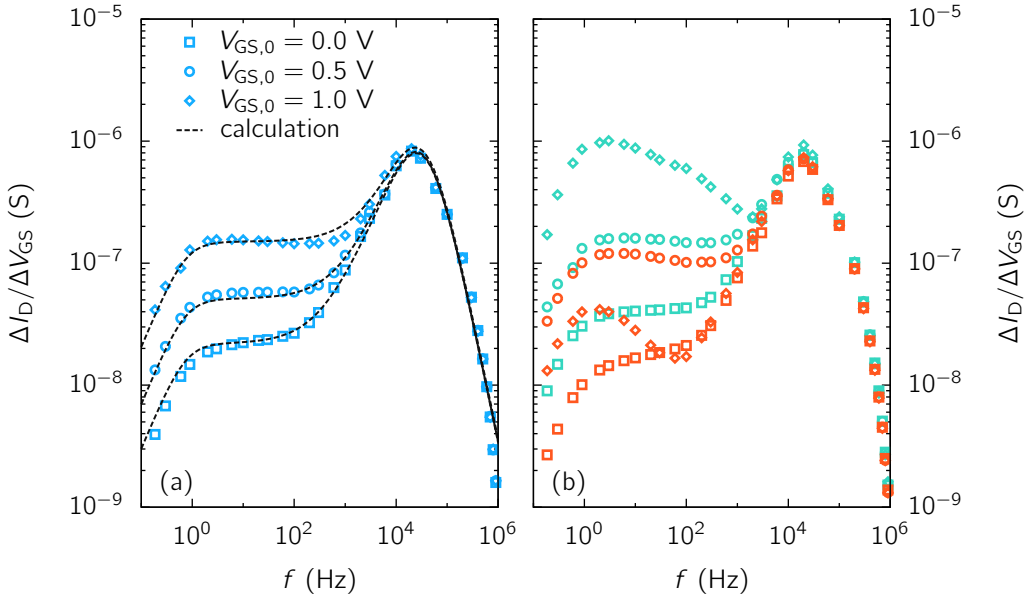

Figure 5.25.: Response of the drain current on sinusoidal electrolyte potential with an amplitude of 50 mV at different offset voltages $V_{GS,0}$. (a) Measurement on a single SGFET, together with a calculation based on a FET-like part together with direct capacitive coupling at high frequencies. (b) Measurements on two more SGFETs, showing similar behavior for 0 V and 0.5 V, but strongly deviating curves for 1 V.

The FET transconductance g_{FET} and the capacitive coupling are summed up, becaused they arise from parallel conduction paths (compare FET equivalent circuit in Fig. 3.6). Fig. 5.25(a) shows for one SGFET, that this function gives a good description for the observed relation between input and output amplitudes. g_{FET} is used as individual fitting parameter for each FET and each V_{GS}. The high frequency transconductance $g_{cap} = 1.8$ μS and $f_{cap} = 30$ kHz are constant for all FETs and electrolyte potentials. For $V_{GS,0} = 1.0$ V a peak arises around 3 Hz, which is not considered in the model. For the FET presented in Fig. 5.25(a) this feature is barely visible, but for other devices, as those shown in Fig. 5.25(b), this peak becomes very prominent at high gate voltages. It might be due to electrochemical reactions at the electrolyte/ZTO interface. Whether this is a reversible process or due to channel degradation was not investigated, yet.

For the FET presented in Fig. 5.25(a), measurements with rectangular voltage pulses at 100 Hz are shown in Fig. 5.26, with a sampling rate of 5 kHz. The pulse height expected from the fitted transconductance g_{FET} is marked with dashed black lines. The agreement is good for the lower gate voltages, while for $V_{GS,0} = 1.0$ V the actual amplitude is lower compared to the estimation. This is because of the arising peak at 3 Hz mentioned above, which introduces a certain error into the fit. The peak-to-peak noise amplitude

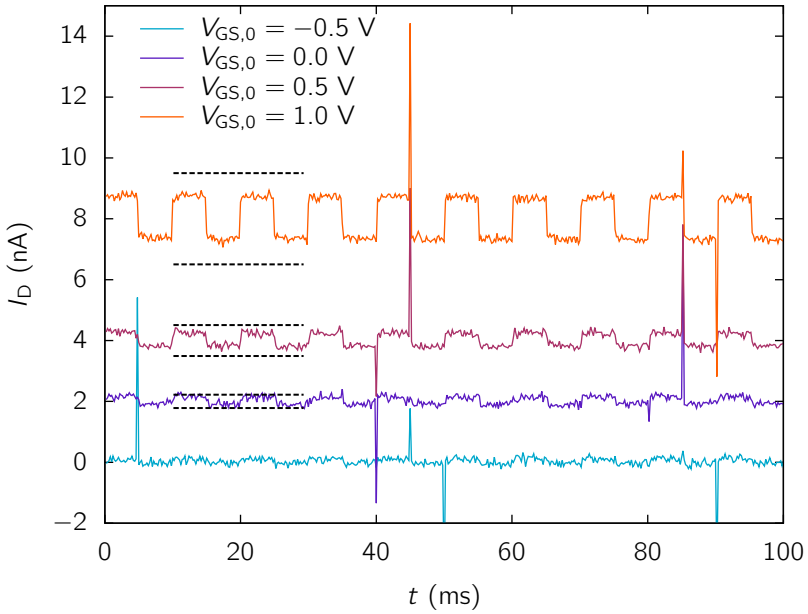

Figure 5.26.: Drain current variation for rectangular voltage pulses at the electrolyte, with a peak-to-peak amplitude of 10 mV.

is around 0.2 nA. For the pulse height of 10 mV we obtain a SNR of 10 at $V_{GS,0} = 1.0$ V. This is not yet sufficient for MEAs. Nevertheless, the concept is promising when the low conductivity of the ZTO layer is taken into account. With ZTO or β-Ga_2O_3 thin films of higher conductivity, higher transconductances could be reached. When the FET transconductance g_{FET} supercedes the high frequency transconductance g_{cap}, also the linearity of the signal transmission is improved. Thus, further optimization of the growth processes for thin layers of electrolyte resistant transparent semiconductors with thickness below 100 nm is needed. For the amorphous semiconductor ZTO the use of rf sputtering instead of PLD could introduce a new set of parameters for this optimization. For TFTs based on sputtered and post-annealed ZTO thin films, field-effect mobilities up to 50 cm^2/Vs have been reported [127].

6. Conclusion and Outlook

ZnO based devices Field-effect transistors with PLD-grown ZnO as channel material were evaluated regarding their static and dynamic characteristics. The measured characteristics of MESFETs were compared with device models, and in many situations good agreement was reached. It was found, that Schottky diodes on ZnO channels used for MESFET fabrication are best described by thermionic field emission, while diodes in literature on thicker films are usually modelled with thermionic emission, due to lower doping concentrations. For a correct description of the MESFETs, the series resistances and a formalism for the subthreshold regime were considered. An open question concerning the theoretical description is the ideality factor in the TFE formalism for the Schottky gate diodes, which corresponds also to the unsatisfactory description of the FET's subthreshold regime. This empirical parameter prevents a complete physical description of the devices.

The examined transistor types were JFETs with $ZnCo_2O_4$ gates, MESFETs with reactively sputtered Au, Pt and Ag gates, and MISFETs with WO_3 as gate insulator. All devices stayed functional in the examined temperature range up to 150°C, although not without certain changes in their characteristics. At room temperature the devices were compared to the required performance for the measurement of nerve cell signals. The MISFETs and the MESFETs with Ag gates had the highest ON/OFF-ratio, but were ruled out by the dynamical characterization, as both exhibit cutoff frequencies below 1 kHz. The slow switching behavior of the MISFETs was attributed to trap states in the porous insulator, for the MESFETs the indiffusion of Ag into the channel material is held responsible. The cutoff of the other devices with a standard gate length of 10 μm could not be measured directly, due to the preamplifier cutoff at 550 kHz. Pt MESFETs with very long gate length of 120 μm exhibited a cutoff at 60 kHz. Based on this result the cutoff for a gate length of 10 μm was estimated to be around 5 MHz. MESFETs with Pt gates were chosen for the further experiments, due to good device stability, sufficient static device characteristics, and high cutoff frequency.

ZnO based simple inverters were investigated as potential circuits for on-chip amplification of voltage signals. The inverter characteristics close to maximum gain could be described well by an analytical model derived for this work from the MESFET characteristics. The highest gain values, above 150, were obtained with Au gates. However, cutoff frequencies below 1 kHz were observed for such devices. The reason for this comparably

slow switching behavior is a high capacitance between the input and output contacts, whose origin is not clear, yet. In order to shift a high frequency input signal always to the working point of maximum gain, an electronic circuit was developed an successfully tested. A proof-of-principle measurement for an active matrix circuit was conducted with ZnO based inverters.

Noise To evaluate the sensitivity limit of ZnO based FETs in sensor applications, noise measurements were performed. The self-built amplifier for MEA measurements was characterized concerning its internal noise, in agreement with calculated noise spectra. Homogenous ZnO samples were investigated, in order to obtain noise figures independently of the constitution of more complex devices. The current noise measured on thin films as well as on microwires had a power spectral density with $1/f$ proportionality at low frequencies (usually below 1 kHz). Measurements on samples with different geometries indicated, that the noise is generated in the bulk of the material, and not on the surface. Hooge constants for all samples were around 10^{-3}.

Noise measurements on MESFETs and simple inverters revealed, that the noise originating from the bulk of the ZnO channels is the dominant noise source, where the gate currents are negligible. The equivalent input noise of the drain current for signals applied at the gate was calculated to be around 40 μV, measurements resulted in a value of about 80 μV in a frequency interval from 10 Hz to 10 kHz. The noise level was defined as twice the standard deviation of the output signal. Compared to the requirements for neuron signal measurements, as defined by Lambacher *et al.* [31], the sensitivity of the MESFETs is sufficient, but only by a narrow margin. Under floating gate conditions a significantly higher noise level was observed, partly because of a higher channel current, but mostly because of a feedback loop between channel and gate contact.

Experiments in Electrolyte and with Cells Stability in electrolyte and biocompatibility was tested for several materials. PLD grown ZnO and GaZnO are very sensitive to aqueous solutions and must be adequately protected, while ZTO and Ga_2O_3 are very resistant against aqueous and acidic solutions. A stable and biocompatible insulator is the epoxy based SU-8 photoresist, which was used for the top layer of the MEA chips. Cell culture experiments were conducted in collaboration with the groups of Prof. J. Käs and Prof. A. Robitzki at the Universität Leipzig and with the group of Prof. A. Offenhäusser at the Forschungszentrum Jülich. Both primary neurons from rat cerebellum and the cardiac myocyte cell line HL-1 were cultivated on the MEA chips developed for this work.

The electric coupling between electrolyte and FETs was investigated by several methods. An important insight gave noise spectra of the drain current. They revealed that the

FETs operate under floating gate conditions, but the noise from the gate is damped in the relevant frequency range by the coupling with the electrolyte. Thus, capacitive coupling prevails at small electrolyte voltages. At electrolyte voltages lower than -1 V probably electrolysis of water sets in, while for positive voltages above ca. 0.5 V the electrodes degrade. The frequency-dependent investigation of the signal transmission from the electrolyte to the MEAs confirmed the mostly capacitive coupling and gave quantitative information about the amplification. Transfer measurements can provide similar results, but are as static characteristics less suitable for the evaluation of signal transmission at a certain frequency. This is an important difference to MEAs based on MISFETs, as for such transistors the capacitive coupling at the gate is the natural mode of operation.

Within this work it was often not possible to achieve a reproducible coupling between the electrolyte and the MESFETs. The upper limit of the MEA sensitivity is indeed set by the transistor properties, but for many devices this limit was not reached. A certain improvement was achieved by immersion in isopropanol and by the application of high negative voltages at the electrolyte. However, the reason for this behavior could not be clarified.

For MEA characterization and measurements on cells a preamplifier was built, since appropriate concepts for active MEAs can be found in literature but are not commercially available. Electrical measurements on HL-1 cell cultures were conducted, but no signals originating from cell action potentials could be identified. This was attributed to the low signal-to-noise ratio of many measurement electrodes, reducing the probability for successful measurements.

Solution-gated transistors were fabricated with PLD grown ZTO as channel material. With $\rho = 10\ \Omega$m the thin films had a comparably high resistivity, which resulted in low channel currents. Transfer curves with ON/OFF-ratio of 10 were recorded. The equivalent input noise was in the range of 1 mV. If the material conductance of ZTO or Ga_2O_3 can be improved for films with thickness below 100 nm, the SGFET approach might be an interesting alternative for transparent oxide semiconductor based MEAs.

Outlook Many processing issues limited the reproducibility and the production yield for MEAs in this work. Keeping the progress in all fields of semiconductor technology in mind, this seems to be the least problem, solvable by carefull assessment of all processing steps. For example the semiconducting channels could be fabricated by rc sputtering instead of PLD, which might result in better reproducibility. For the structuring of material layers the application of plasma etching instead of lift-off, or the use of special lift-off photoresists instead of the multipurpose resist used for this work could improve the fabricated devices. Still, considering the early age of transparent oxide electronics,

the necessary effort for process optimizations must not be underestimated.

The understanding of the electrode/electrolyte interface should be improved, in order to obtain a more controlled signal transmission between electrolyte potential and transistors. Especially the improving signal transduction after transfer measurements to high negative gate voltages should be further investigated. For conventional MEAs, a multitude of electrode materials and geometries has been proposed and evaluated (see e.g. [128, 129, 130]). Such studies could be the starting point for an improvement of the electrodes, and might give insight in the interaction between electrolyte and electrode materials. Application of plasma etching could clarify, if residues of some chemical compounds on the electrode surface is responsible for the unreliable signal transmission. As the coupling between electrodes and electrolyte is mostly capacitive, also the application of a thin insulating layer on the electrodes might be feasible, in order to vary the properties of the electrolyte-chip interface.

With a stable MEA fabrication process and controlled electrolyte-chip coupling, the improvement of the MESFET signal-to-noise ratio would be the next step. The similar noise level for ZnO thin films and microwires raises the question, whether further samples with different crystal qualities and doping densities exhibit similar noise figures, or whether a dependency of the noise on growth parameters can be found. Also an evaluation of noise in different oxide semiconductors would be very valuable, in order to find the ideal material configuration for transparent active MEAs.

Appendices

A. MEA Amplifier Components

part	description
$R^{(1)}_{\text{feedback}}$	220 kΩ
$C^{(1)}_{\text{feedback}}$	28 pF
$R^{(2)}_{\text{in signal}}$	22 kΩ
$R^{(2)}_{\text{in offset}}$	10 kΩ
$R^{(2)}_{\text{feedback}}$	220 kΩ
$C^{(2)}_{\text{feedback}}$	10 pF
$R^{(\text{off})}_{\text{in}}$	220 kΩ
$C^{(\text{off})}_{\text{feedback}}$	22 μF
$R^{(\text{inv})}_{\text{in}}$	22 kΩ
$R^{(inv)}_{\text{feedback}}$	22 kΩ
$C^{(inv)}_{\text{feedback}}$	470 nF
stage 1 op-amp	Linear Technology LT1112
stage 2 op-amp	Linear Technology LT1112
inverter stage op-amp	Linear Technology LT1112
offset stage op-amp	Linear Technology LT1112
stage 3 instrumentation amplifier	Linear Technology LT1167

B. MEA Fabrication Protocol

step	*method*	*materials, parameters etc.*
substrate		a-sapphire (double side polished) usually 10×10 mm^2
semiconductor	PLD	*target*: ZnO + 0.25wt-% MgO *substrate temperature*: 650°C *atmosphere*: O_2, 0.02 mbar 1500 pulses at 3 Hz (ca. 15 nm)
alignment markers	lithography mask	*exposure time*: 10 s *mask name*: 24-1
	dc sputtering	*target*: Au *atmosphere*: Ar, 0.02 mbar 20 s at 30 W
mesa	lithography mask	*exposure time*: 6 s *mask name*: 24-2
	lithography mask	*exposure time*: 30 s *mask name*: 24-8
	etching	*etchant*: H_3PO_4/H_2O (1:80) *duration*: 20 s
inner conductors	lithography mask	*exposure time*: 10 s *mask name*: 24-3
either	dc sputtering	*target*: Au *atmosphere*: Ar, 0.02 mbar 20 s at 30 W
or	PLD	*target*: ZnO + 4wt-% Ga_2O_3 *substrate temperature*: RT *atmosphere*: O_2, 0.002 mbar 3000 pulses at 10 Hz (ca. 100 nm)
	PLD	*target*: SnO_2 + 33wt-% ZnO *substrate temperature*: RT *atmosphere*: O_2, 0.025 mbar 600 pulses at 10 Hz (ca. 20 nm)

continued on next page

continuing previous page

step	*method*	*materials, parameters etc.*
outer conductors	lithography mask	*exposure time*: 10 s *mask name*: 27-1
	dc sputtering	*target*: Au *atmosphere*: Ar, 0.02 mbar 25 s at 30 W
gates	lithography mask	*exposure time*: 10 s *mask name*: 24-4
	dc sputtering	*target*: Pt *atmosphere*: Ar/O_2 (50:50), 0.02 mbar 15 s at 30 W
	dc sputtering	*target*: Pt *atmosphere*: Ar, 0.02 mbar 10 s at 30 W
	dc sputtering	*target*: Au *atmosphere*: Ar, 0.02 mbar 5 s at 30 W
insulation	SU-8 resist	*exposure time*: 11 s *mask name*: 27-2 (processing details below)

Lithographic structuring was conducted with the AZ 1514H photoresist. The resist was spin coated at 6000 rpm and subsequently baked on a hot plate for 90 s at 90°C. For exposure a Suss MJB3 maskaligner was used. The post-exposure bake was again on a hot plate for 90 s at 90°C. The samples were developed in the NaOH based AZ 351B for 40 s.

Dc sputtering was conducted in a self-built chamber for magnetron sputtering. The sample-target distance was 40 mm.

PLD For the used system see section 2.1.1 and e.g. [32, 33].

SU-8 resist was supplied from Gersteltec Sarl, Switzerland. The resist GM 1040 and the developer DRGM 5000 were used. Before the application of SU-8, the samples were rinsed with acetone and isopropanol, and dried with N_2 and on a hot plate for 5 min at 90°C. Plasma cleaning was conducted for some samples, however without clear evidence for improvement concerning the SU-8 adhesion. The resist was applied via spin coating at 3500 rpm. The sample backside and the corners were cleaned with acetone and cotton buds, in order to achieve a more reproducable exposure. After 5 min relaxing time the softbake was conducted on a programmable hot plate for 10 min at 65°C and for 10 min at 90°C. The temperature cycle started and ended at 50°C, while each temperature ramp took 5 min to avoid cracks in the layer. The resist was illuminated with a Suss MJB4 maskaligner with i-line filter and 12.5 mW/cm^2. As described in section 2.1.4 the samples were placed on a mirror during illumination, usually a polished silicon wafer. After exposure a delay time of 10 min is recommended by the supplier. Subsequently the post-exposure bake took place, for 5 min at 65°C and for 5 min at 80°C, again with 5 min long temperature ramps. The samples were developed for 40 s in a first bath and 5 s in a second bath. Finally they were rinsed with isopropanol and dried with N_2. The finished chips were cured for 90 min in an oven at 90°C.

C. Cell Culture Protocol

for 9 samples with each 30 mm^2, 2-2.5 million cells

- materials
    1. Sigma Aldritch Poly-D-Lysine hydrobromide
    2. Sigma Aldritch Laminin L2020
- cleaning
    1. rinse with millipore
    2. immerse 15 min in Hellmanex 1%
    3. rinse with millipore
    4. rinse with ethanol, dry with N_2
    5. plasma cleaning for 10 min at 0.5 mbar ambient atmosphere
    6. immerse overnight in ethanol under UV exposure
- poly-d-lysine coating
    1. rinse twice with PBS
    2. fill poly-d-lysine aliquot (0.1 mg/ml) with 500 μl PBS, stir
    3. distribute between samples
    4. rock gently to ensure even coating
    5. 2 h in the incubator
- laminin coating
    1. rinse thrice with PBS, do not stir
    2. fill laminin aliquot (20 mg/ml) with 500 μl PBS, stir
    3. distribute between samples
    4. 2 h in the incubator
- cell distribution
    1. rinse thrice with PBS, do not stir
    2. warm up cell medium

3. centrifuge cells / spin cells down 10 min at 800 rpm, after passaging or dissoziation
4. draw liquid off
5. add 1000 μl medium to the cell pellet, resuspend
6. distibute on samples in desired concentration
7. fill culture vessels with medium after 1 h

- check after 3 days

D. Script for Calculation of FET Characteristics

```
% tested with MATLAB R2008b

function [I Is Id Ig Si] = mesfet( aVsd, aVsg, varargin )

    % function input parameters:
    % aVsd: array of source-drain voltages
    % aVsg: array of source-gate voltages
    % varagin: parameter/value pairs

    % function output parameters:
    % I: channel current, without consideration of gate currents
    % Is,Id,Ig: currents after consideration of gate currents
    % Si: noise current density * f/aH

    e = 1.60217646e-19;       % elemtary charge
    me = 9.10938188e-31;      % electron mass
    k = 1.3806503e-23;        % Boltzmann constant
    h = 6.626068e-34;         % Planck constant
    eps0 = 8.854187817620e-12; % vacuum permittivity
    T = 300;                  % temperature

    eps = eps0 * 8.12;        % semiconductor dielectric constant
    meff = 0.27;              % semiconductor effective mass
    mu = 16e-4;               % semiconductor mobility
    Nd = 5e24;                % semiconductor doping density

    a = 16e-9;                % channel thickness
    Z = 30e-6;                % channel width
    L = 10e-6;                % channel length
    L2 = 10e-6;               % distance between gate and ohnic constants
    Vbi = 0.8;                % gate contact built-in voltage

    diode = 0;                % boolean, calculate gate current?
    x_res = 20;               % resolution for calculation of gate current
    Rp = 100;                 % thermionic emission: parallel resistance
    Rs = 761.677;             % thermionic emission: series resistance
    n = 1;                    % thermionic emission: ideality factor
    n_tunnel = 1;             % thermionic field emission: ideality factor
    Vbi_tunnel = Vbi;         % thermionic field emission: built-in voltage

    include_subth_slope = 1; % boolean, include subthreshold slope?
    ss_ideality = 1;          % ideality factor for subthreshold slope
    I_min = 1e-14;            % minimal channel current
    fet_with_n = 0;           % boolean, calculate with voltage dep. barrier?

    % resolve additional function parameters
```

```
47      if nargin > 2
48          for arg_idx = 1:2:(nargin-2)
49              disp( varargin{arg_idx} );
50              switch varargin{arg_idx}
51                  case 'Vbi'
52                      Vbi = varargin{arg_idx+1};
53                  case 'mu'
54                      mu = varargin{arg_idx+1};
55                  case 'Nd'
56                      Nd = varargin{arg_idx+1};
57                  case 'a'
58                      a = varargin{arg_idx+1};
59                  case 'Z'
60                      Z = varargin{arg_idx+1};
61                  case 'L'
62                      L = varargin{arg_idx+1};
63                  case 'L2'
64                      L2 = varargin{arg_idx+1};
65                  case 'n'
66                      n = varargin{arg_idx+1};
67                  case 'Rp'
68                      Rp = varargin{arg_idx+1};
69                  case 'Rs'
70                      Rs = varargin{arg_idx+1};
71                  case 'Vbi_tunnel'
72                      Vbi_tunnel = varargin{arg_idx+1};
73                  case 'n_tunnel'
74                      n_tunnel = varargin{arg_idx+1};
75                  case 'eps_r'
76                      eps = 8.854188e-12 * varargin{arg_idx+1};
77                  case 'diode'
78                      diode = varargin{arg_idx+1};
79                  case 'fet_with_n'
80                      fet_with_n = varargin{arg_idx+1};
81                  case 'ss'
82                      include_subth_slope = varargin{arg_idx+1};
83                  case 'ss_ideality'
84                      ss_ideality = varargin{arg_idx+1};
85              end
86          end
87      end
88
89      % constants
90      Nc = 2*(2*pi*meff*me*k*T/h^2)^(3/2);
91      As = 4*pi*e*me*meff*k^2/h^3;    % thermion. Em. (Richardson-Konstante)
92      A_Pt= 0.26 * 4*pi*e*me*k^2/h^3; % Richardson-Konstante f. Pt (http://simion.
            com/definition/richardson_dushman.html)
93      E00 = e*h/(4*pi) * sqrt(Nd/(eps*meff*me));
```

```
94      Vp = (e*a^2*Nd)/(2*eps);
95      Ip = (e^2*mu*Nd^2*Z*a^3)/(6*eps*L);
96      Rs_channel = L2 / (e*Nd*mu*Z*a);
97      beta = 1/(k*T);
98      A0 = Z*L;
99
100     I = zeros(numel(aVsd),numel(aVsg));         % channel current
101     Is = zeros(numel(aVsd),numel(aVsg));        % source current
102     Id = zeros(numel(aVsd),numel(aVsg));        % drain current
103     Ig = zeros(numel(aVsd),numel(aVsg));        % gate current
104     Si = zeros(numel(aVsd),numel(aVsg));        % noise current density * f/aH
105     Vch = zeros(numel(aVsd),numel(aVsg),x_res+1); % potential along the channel
            length
106     hch = zeros(numel(aVsd),numel(aVsg),x_res+1); % depletion layer width along
            the channel
107
108     % --- START CALCULATION ---
109     for isd = 1:numel(aVsd)  % loop over drain-source voltages
110         for isg = 1:numel(aVsg) % loop over gate-source voltages
111             Vsd = aVsd(isd);
112             Vsg = aVsg(isg);
113
114             % calculate channel current, potentials and depletion layer widths
115             I(isd,isg) = calc_drain_current_with_Rs( Vsd, Vsg, Vbi );
116             Is(isd,isg) = -I(isd,isg);
117             Id(isd,isg) = I(isd,isg);
118             [depl_width, Vchannel] = calc_potential_distribution( Vsd, Vsg, Vbi,
                    I(isd,isg) );
119             Vch(isd,isg,:) = Vchannel;
120             hch(isd,isg,:) = depl_width;
121
122             % flicker noise factor
123             Si(isd,isg) = (Vchannel(end)-Vchannel(1)) * I(isd,isg) * e * mu / L
                    ^2;
124
125             % calculate gate current
126             if diode > 0
127                 for pos_index = 1:x_res+1
128                     diode_volt = Vsg - Vchannel(pos_index);
129                     % thermionic emission:
130                     % diode_current = calc_diode( diode_volt ) / (x_res+1);
131                     % thermionic field emission:
132                     if diode_volt >= 0
133                         diode_current = + calc_padovani_for( diode_volt ) / (x_res
                                +1);
134                     else
135                         diode_current = - calc_padovani_rev( diode_volt, 1 ) / (
                                x_res+1);
```

```
136                 end
137                 Ig(isd,isg) = Ig(isd,isg) + diode_current;
138                 if (diode_current > 0)
139                     Is(isd,isg) = Is(isd,isg) - diode_current;
140                 else
141                     Id(isd,isg) = Id(isd,isg) - diode_current;
142                 end
143             end
144         end
145
146     end % gate-source voltage loop
147 end % drain-source voltage loop
148 % --- END CALCULATION ---
149
150 function Id_loc = calc_drain_current_with_Rs( Vsd_loc, Vsg_loc, Vbi_loc )
151
152     % just calculate current without the effect of Rs
153     Id_loc = calc_drain_current( Vsd_loc, Vsg_loc, Vbi_loc, 0 );
154     % if Rs_channel is considered, solve implicit equation
155     if Rs_channel>0
156         Id_loc = fzero( @calc_drain_current_error, Id_loc );
157     end
158
159     function Id_loc0 = calc_drain_current( Vsd_loc0, Vsg_loc0, Vbi_loc0,
            Id_loc0 )
160         % calculate channel current for given potentials
161
162         % use Id_loc0 to correct potentials
163         Vsd_corr = Vsd_loc0 - 2*Rs_channel*Id_loc0;
164         Vsg_corr = Vsg_loc0 - Rs_channel*Id_loc0;
165         if (fet_with_n)
166             Vbi_corr = Vbi_loc0 + (1-1/n)*Vsg_corr;
167         else
168             Vbi_corr = Vbi_loc0;
169         end
170         if (include_subth_slope)
171             % compare "Liang et al.,Solid-State Electronics 34, 131 (1991)"
                    for derivation of subthreshold current
172             % and "Parker et al., Microwave Theory and Techniques 45, 1563
                    (1997)" for the method applied here for combination
173             % ss_ideality is introduced to enable adjustment of subthreshold
                    slope
174             Vsg_corr = 2*k*T*ss_ideality/e * log( 1 + exp( e*(Vsg_corr-
                    Vbi_corr+Vp)/(2*k*T*ss_ideality) ) ) + Vbi_corr - Vp;
175         end
176
177         % calculate
178         if Vsg_corr < Vbi_corr - Vp % FET off
```

```
179             Id_loc0 = 0;
180         elseif Vsg_corr >= Vbi_corr
181             if Vbi_corr - Vsg_corr + Vsd_corr <= 0 % no depl. layer, ohmic
                    conduction
182                 Id_loc0 = e*mu*Nd*a*Z/L*Vsd_corr;
183             elseif Vbi_corr - Vsg_corr + Vsd_corr < Vp % partially ohmic
                    conduction
184                 Id_loc0 = Ip * ( 3*(Vsd_corr-Vsg_corr+Vbi_corr)/Vp - 2*((
                        Vbi_corr-Vsg_corr+Vsd_corr)^(3/2))/Vp^(3/2) )...
185                     + e*mu*Nd*a*Z/L*(Vsg_corr-Vbi_corr);
186             else % depl. layer partially gone, at drain still in saturation
187                 Id_loc0 = Ip + e*mu*Nd*a*Z/L*(Vsg_corr-Vbi_corr);
188             end
189         else % normal FET characteristics
190             if Vbi_corr - Vsg_corr + Vsd_corr < Vp % linear regime
191                 Id_loc0 = Ip * ( 3*Vsd_corr/Vp - 2*((Vbi_corr-Vsg_corr+
                        Vsd_corr).^(3/2)-(Vbi_corr-Vsg_corr).^(3/2))/Vp^(3/2) );
192             else % saturation
193                 Id_loc0 = Ip * ( 1 - 3*(Vbi_corr-Vsg_corr)/Vp + 2*(Vbi_corr-
                        Vsg_corr)^(3/2)/Vp^(3/2) );
194             end
195         end
196
197         % minimal current
198         if Id_loc0 == 0
199             Id_loc0 = I_min;
200         elseif abs(Id_loc0) < I_min
201             Id_loc0 = I_min * sign(Id_loc0);
202         end
203
204     end
205
206     function Id_loc_err = calc_drain_current_error( param )
207         % calculates difference between FET current and current through
208         % series resistances
209         Id_loc_err = real( calc_drain_current( Vsd_loc, Vsg_loc, Vbi_loc,
                param ) - param );
210         if Rs_channel*Id_loc_err > Vsd_loc
211             Id_loc_err = Id_loc_err + 1e5;
212         end
213         if param < 0
214             Id_loc_err = Id_loc_err + 1e5;
215         end
216     end
217 end
218
219 function [hx Vx] = calc_potential_distribution( Vsd_loc, Vsg_loc, Vbi_loc,
        Id_loc )
```

```
220         % calculate potential distribution and depletion layer width along
221         % the channel, with a resolution of x_res+1 datapoints
222
223         % correct potentials
224         Vsd_loc = Vsd_loc - 2*Rs_channel*Id_loc;
225         Vsg_loc = Vsg_loc - Rs_channel*Id_loc;
226         if (fet_with_n)
227             Vbi_loc = Vbi_loc + (1-1/n)*Vsg_loc;
228         end
229
230         hx = zeros(1,x_res+1);
231         Vx = zeros(1,x_res+1);
232         if Vsg_loc < Vbi_loc - Vp % FET off
233             hx = hx + a;
234             Vx = Vx + Vsg_loc - Vbi_loc + Vp;
235         elseif Vsg_loc >= Vbi_loc
236             if Vbi_loc - Vsg_loc + Vsd_loc <= 0 % ohmic conduction
237                 Vx = Vsd_loc * (0:1/x_res:1);
238             elseif Vbi_loc - Vsg_loc + Vsd_loc < Vp % partially ohmic
239                 x0 = e*Nd*mu*a*Z * (Vsg_loc-Vbi_loc) / Id_loc;
240                 for ix = 1:x_res+1
241                     x = (ix-1) * L / x_res;
242                     if x < x0
243                         hx(ix) = 0;
244                         Vx(ix) = x * (Vsg_loc-Vbi_loc) / x0;
245                     elseif (x0==0)&&(x==0)
246                         hx(ix) = 0;
247                         Vx(ix) = 0;
248                     else
249                         hx(ix) = calc_depl_width( Vsd_loc-(Vsg_loc-Vbi_loc),
                                Vsg_loc-(Vsg_loc-Vbi_loc), Vbi_loc, Id_loc, x-x0 );
250                         Vx(ix) = hx(ix).^2*e*Nd/2/eps+Vsg_loc-Vbi_loc;
251                     end
252                 end
253             else % normal FET characteristics
254                 x0 = e*Nd*mu*a*Z * (Vsg_loc-Vbi_loc) / Id_loc;
255                 for ix = 1:x_res+1
256                     x = (ix-1) * L / x_res;
257                     if x < x0
258                         hx(ix) = 0;
259                         Vx(ix) = x * (Vsg_loc-Vbi_loc) / x0;
260                     elseif (x0==0)&&(x==0)
261                         hx(ix) = 0;
262                         Vx(ix) = 0;
263                     else
264                         hx(ix) = calc_depl_width( Vsd_loc-(Vsg_loc-Vbi_loc),
                                Vsg_loc-(Vsg_loc-Vbi_loc), Vbi_loc, Id_loc, x-x0 );
265                         Vx(ix) = hx(ix).^2*e*Nd/2/eps+Vsg_loc-Vbi_loc;
```

```
266                 end
267                 Vx(end) = Vp - Vbi_loc + Vsg_loc;
268                 hx(end) = a;
269             end
270         end
271     else
272         for ix = 1:x_res+1
273             hx(ix) = calc_depl_width( Vsd_loc, Vsg_loc, Vbi_loc, Id_loc, (ix
                    -1) * L / x_res );
274         end
275         Vx = hx.^2*e*Nd/2/eps+Vsg_loc-Vbi_loc;
276         if Vbi_loc - Vsg_loc + Vsd_loc >= Vp
277             Vx(end) = Vp - Vbi_loc + Vsg_loc;
278             hx(end) = a;
279         end
280     end
281     Vx = Vx + Rs_channel*Id_loc;
282 end
283
284 function depl_width = calc_depl_width( Vsd, Vsg, Vbi, Isd, x )
285     w0 = sqrt( 2*eps/e/Nd * (Vbi - Vsg) );
286     r = roots( [ 1/3, -a/2, 0, eps * Isd * x / (e^2*Nd^2*mu*Z) + a/2 * w0^2
            - 1/3 * w0^3 ] );
287     % choose smallest real positive root
288     r = min( r( logical((r>0).*(imag(r)==0)) ) );
289     if numel(r) == 1
290         depl_width = r;
291     else
292         depl_width = a; % might happen in subthreshold regime
293     end
294 end
295
296 function curr = calc_diode( voltdata )
297     Is0 = A0.*As.*T.^2.*exp(-(e.*Vbi).*beta);
298     coeff_a = exp((Is0.*e.*(Rp.*1.0e+009).*Rs.*beta)./(n.*((Rp.*1.0e+009)+Rs
            ))+(e.*voltdata.*beta)./(n)-(e.*Rs.*voltdata.*beta)./(n.*((Rp.*1.0e
            +009)+Rs))).*Is0.*e.*(Rp.*1.0e+009).*Rs;
299     coeff_b = (1./beta).*n.*((Rp.*1.0e+009)+Rs);
300     curr = -Is0./(1+Rs./(Rp.*1.0e+009))+voltdata./((Rp.*1.0e+009).*(1+Rs/(Rp
            .*1.0e+009)))+1./(e.*Rs).*n.*(1./beta).*lambertw(coeff_a./coeff_b);
301 end
302
303 function curr = calc_padovani_rev( volt, limit_voltage )
304     if limit_voltage
305         Voff = Vbi_tunnel - Vp; % for depletion layer width: average, not
                effective barrier height!
306         volt = max( volt, Voff*n_tunnel );
307     end
```

```
308         E0 = E00 * coth( E00 / (k*T) );
309         Eb = e*Vbi_tunnel; % should actually use barrier height!
310         eps_prime = E00 ./ (E00/(k*T) - tanh(E00/(k*T)) );
311         Js = A_Pt .* sqrt(pi * E00) / (k*T) .* sqrt( - e*volt ./ n_tunnel + Eb /
                (cosh(E00/k/T))^2 ) .* exp( - Eb/E0 );
312         curr = A0 .* Js .* ( exp( - e.*volt ./ eps_prime ./ n_tunnel ) - 1 );
313     end
314
315     function curr = calc_padovani_for( volt )
316         E0 = E00 * coth( E00 / (k*T) );
317         xi2 = k*T*log(Nd/Nc); % Energy of Fermi level of sc with respect to
                conduction band
318         Eb = e*Vbi_tunnel; % should actually use barrier height!
319         Em = (-e*volt + Eb + xi2)/(cosh(E00/k/T))^2; % tunnel height
320         if (Em>0)
321             Js = As .* sqrt(pi * E00) / (k*T) .* sqrt( - e*volt ./ n_tunnel + Eb
                    + xi2 ) / (cosh(E00/k/T)) .* exp( xi2/k/T - (Eb+xi2)/E0 );
322             curr = A0 .* Js .* ( exp( e.*volt ./ E0 ./ n_tunnel ) - 1 );
323         else
324             curr = Inf; %calc_diode_noR( volt );
325             disp( ['out of tunneling: ' num2str( volt ) ' V'] );
326         end
327     end
328
329 end
```

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Symbols and Abbreviations

α	slope of the FET saturation current
α_{H}	Hooge constant
χ_{s}	energy difference between vacuum energy and conduction band edge
ϵ_{s}	static dielectric constant of semiconductor
ϵ_0	vacuum permittivity
η	ideality factor
$\hbar$	$h/(2\pi)$
μ	charge carrier mobility
μ_{FE}	field-effect mobility
μ_{H}	Hall mobility
μ_{n}	electron mobility
Φ_{Bn}	Schottky barrier height
ρ	autocorrelation function
a	thin film thickness
a_{B}	Bohr radius
A^*	Richardson constant
A_0	area
C	capacitance
C-V	capacitance-voltage measurement
D_{n}	electron diffusion constant
e	elementary charge
E_{00}	characteristic energy for tunneling process
E_{B}	energy barrier height between grains
E_{C}	energy of conduction band edge
$E_{\mathrm{D}}^{\mathrm{b}}$	donor ionization energy
E_{F}	Fermi energy
E_{m}	energy of maximum tunneling probability
E_{V}	energy of valence band edge
f	frequency
f_{c}	cutoff frequency
F_{n}	electron quasi-Fermi energy
G	conductance
g	inverter gain
g_{max}	maximum transconductance

g_m	(forward) transconductance
h	Planck constant
I	electric current
I-V	current-voltage measurement
I_D	drain current
I_G	gate current
I_P	saturation current
j	current density
j_G	gate current density
k_B	Boltzmann constant
L	gate length of FET or device length
L_G	grain size
m^*	effective mass
m_0	electron mass
N	number of free charge carriers
n	concentration of free carriers
N_C	density of states at the conduction band edge
N_D	concentration of donors
n_H	Hall carrier concentration
R	resistance
R_S	series resistance
S	subthreshold swing
S_I	current noise power spectral density
S_V	voltage noise power spectral density
SNR	signal-to-noise ratio
T	temperature
V	voltage
V_bi	built-in voltage
V_DD	inverter operating voltage
V_DS	drain-source voltage
V_EIN	equivalent input noise level
V_ext	externally applied voltage
V_GS	gate-source voltage
V_in	input voltage
V_n	energy difference between conduction band edge and Fermi energy
V_out	output voltage
V_P	pinch-off voltage
V_T	threshold voltage
V_0	volume
W	device width
w	width of depletion layer
W_m	metal work function
AFM	atomic force microscope

DUT	device under test
FET	field-effect transistor
FIB	focussed ion beam
ITO	indium tin oxide
JFET	junction field-effect transistor
LSM	laser scanning microscope
MESFET	metal-semiconductor field-effect transistor
MISFET	metal-insulator-semiconductor field-effect transistor
MOSFET	metal-oxide-semiconductor field-effect transistor
PCB	printed circuit board
PLD	pulsed laser deposition
QSCV	quasi-static capacitance-voltage measurement
SEM	scanning electron microscope
TCO	transparent conductive oxide
TE	thermionic emission
TFE	thermionic field emission
TFT	thin film transistor
ZTO	zinc tin oxide

List of Own and Contributed Articles

[1] F. J. Klüpfel, H. von Wenckstern, and M. Grundmann. "Low frequency noise of ZnO based metal-semiconductor field-effect transistors". *Applied Physics Letters* 106(3), p. 033502 (2015).

[2] F. J. Klüpfel, F.-L. Schein, M. Lorenz, H. Frenzel, H. von Wenckstern, and M. Grundmann. "Comparison of ZnO-Based JFET, MESFET, and MISFET". *Electron Devices, IEEE Transactions on* 60(6), pp. 1828–1833 (2013).

[3] H. Frenzel, M. Lorenz, F.-L. Schein, A. Lajn, F. J. Klüpfel, T. Diez, H. von Wenckstern, and M. Grundmann. "Metal-semiconductor field-effect transistors and integrated circuits based on ZnO and related oxides". In: *Handbook of Zinc Oxide and Related Materials, Vol. 2 Devices and Nano-Engineering*. Ed. by Z. C. Feng. Taylor and Francis/CRC Press, Florida, USA, 2012. Chap. 11, pp. 369–434.

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