HIGH FREQUENCY SIGNALING ANALYSIS OF INTER-CHIP PACKAGE ROUTING FOR MULTI-CHIP PACKAGE

YONG KHANG CHOONG

UNIVERSITI SAINS MALAYSIA

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HIGH FREQUENCY SIGNALING ANALYSIS OF INTER-CHIP PACKAGE ROUTING FOR MULTI-CHIP PACKAGE

by

YONG KHANG CHOONG

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Khang Choong Yong, Wil Choon Song, Bok Eng Cheah and Mohd Fadzil Ain, "Signaling Analysis of Inter-Chip I/O Package Routing for Multi-Chip Package", 4th Asia Symposium on Quality Electronic Design (ASQED), pp.271-276, Jul. 2012.

LIST OF ABBREVIATION

SIA	Semiconductor Industry Association
Z_s	Driver Source Impedance
TDR	Time Domain Reflectometer
BW	Bandwidth
LEN	Inter-chip Length
CDRV	Driver Output Capacitance
CRCV	Receiver Input-gate Capacitance
FR4	Fiberglass-epoxy Resin
V_{ref}	Threshold Voltage
Z_s	Source impedance
FEXT	Far-End Crosstalk
NEXT	Near-End Crosstalk
PRBS	Pseudo-Random Bit Sequence
ISI	Intersymbol Interference
TOF	Time of Flight
Z_o	Characteristic Impedance
RT	Signal Rise Time
UI	Signal Unit Interval
MCP	Multi-Chip Package
Vmargin	Voltage Margin
Tmargin	Timing Margin

ANALISA ISYARAT FREKUENSI TINGGI ANTARA LALUAN PAKEJ CIP UNTUK PAKEJ BERBILANG CIP

ABSTRAK

Pakej berbilang cip telah menjadi satu bentuk adat integrasi dalam banyak alat elektronik yang canggih dan berprestasi tinggi. Penggunaan luas teknologi ini disumbangkan terutamanya oleh kelebihan penggunaan kuasa lebih rendah, integrasi heterogen bagi berbilang teknologi proses silikon dan penghasilan, masa-ke-pasaran yang lebih pendek dan kos yang lebih rendah. Walau bagaimanapun, ketumpatan tinggi halaan cip dalam pakej akan mendatangkan isyarat cabaran unik apabila digandingkan dengan kadar data beroperasi tinggi. Menangani isu yang betul pada peringkat awal rekabentuk adalah penting untuk mengelakkan keperluan untuk merekabentuk semula. Oleh itu, dengan tujuan untuk mewujudkan garis panduan rekabentuk untuk membolehkan saluran pakej berbilang cip berprestasi tinggi, kajian ini memberi tumpuan kepada analisis isyarat pakej laluan cip antara peranti silikon dalam pakej berbilang cip. Dalam kajian ini, kualiti isyarat dan sensitiviti margin mata dinilai dari 2.5 GHz ke 7.5 GHz. Kesan gelombang mikro didapati mendominasi komponen talian penghantaran yang mengakibatkan kemerosotan kualiti isyarat. Faktor limit utama seperti kesan cakap silang gandingan, pantulan isyarat dan kehilangan bergantung frekuensi yang menyebabkan kemerosatan kualiti isyarat telah dikenal pasti dan dikategorikan mengikut frekuensi operasi (2.5 GHz – 7.5 GHz) dan panjang saluran (3 mm – 30 mm) untuk pertimbangan rekabentuk masa depan pakej berbilang cip. Selain itu, pelbagai teknik pasif yang berkuasa rendah, iaitu persamaan dan penamatan, telahpun dikaji untuk memulihkan isyarat

kelajuan tinggi dalam pakej berbilang cip. Tambahan pula, keberkesanan teknik pemulihan isyarat kelajuan tinggi juga dikaji dan dibandingkan dari segi prestasi terlajak. Keputusan simulasi menunjukkan topologi yang dicadangkan mampu mencapai isyarat kualiti yang bagus, iaitu 300mV/40ps pada kelajuan 15Gbps. Gabungan siri sumber penamatan dan penamatan selari beban didapati adalah satu pendekatan yang baik dan kriteria yang penting (dari segi keseimbangan antara prestasi dan kos silikon) untuk merealisasikan isyarat kelajuan tinggi dalam pakej berbilang cip.

HIGH FREQUENCY SIGNALING ANALYSIS OF INTER-CHIP PACKAGE ROUTING FOR MULTI-CHIP PACKAGE

ABSTRACT

Multi-Chip Package (MCP) is becoming a customary form of integration in many high performance and advanced electronic devices. The vast adoptions of this technology are mainly contributed by the advantages for instance lower power consumption, heterogeneous integration of multiple silicon process technologies and manufacturers, shorter time-to-market and lower costs. However, the high density inter-chip I/O routing within package will presents unique signaling challenges when coupled with high operating data rate. Tackling the right issue at early design stage is essential to avoid the pitfall of redesign. Thus, with the aim to establish the design guideline to enable high performance MCP channel, this research focuses on the signaling analysis of the inter-chip I/O package routing between silicon devices in MCP. In this study, signal quality and eye margin sensitivity were evaluated from 2.5 GHz up-to 7.5 GHz. The microwave effect is found dominating the transmission line component that resulted in signal quality deteriorations. Key limiting factors such as crosstalk coupling effects, signal reflections and frequency dependent losses that caused signal quality degradations were identified and categorized from 2.5 GHz to 7.5 GHz with channel length of 3 mm to 30 mm for future MCP design considerations. Moreover, various low power passive signaling enhancement techniques i.e. equalization and termination to mitigate the signal integrity challenges of the high speed on-package inter-chip channels has been analyzed. The effectiveness of various signaling enhancement techniques and topologies were

studied and compared in terms of eye opening and overshoot performance. Simulation results show the recommended topology is able to achieve 300mV/40ps eye opening at 15 Gbps. The combination of series-source termination and parallel-load termination was found to be a good approach in view of optimum trade-off between performance and silicon area or cost.

CHAPTER 1

INTRODUCTION

1.1 Background

Microelectronic packaging technology has advanced rapidly over the past twenty years to keep pace with the demands of emerging business market segments driven by mobility applications such as smart-phones, tablets, ultra-small form factor laptops and personal computers (Kong et al., 2011). Market forces such as declining computer prices, increased user experience via miniaturized devices with increased functionality, wireless connectivity bandwidth, and longer battery life will continues to be the important trend in mobile computing (Ang, 2012). These trends result in the pressure on component and platform-level solutions to provide smaller packages, denser, and higher-bandwidth interconnect solutions. High density and small form-factor requirements push package level transmission lines to a very small cross section and the insertion loss becomes a dominant part of the whole system loss budget. Enabling high data rate turns package interconnect into transmission line with higher ISI that distort the transmitting signal with noises.

Multi-chip package (MCP) is regards as the alternative solution to meet the next generation mobility application requirements. In (Ang, 2012), the state-of-the-art of MCP has been discussed. In general, MCP is the preferred solution from total die cost ownership compare to single chip solution. In addition, MCP finds its niche in packaging as transitory stage between product needs and chip integration through insertion of several dies into the same package that allows much faster introduction

of the product into the market compared to integrating all the desired functions on a new single chip. Timely introduction is essential since the highest profit margins are always achieved in the early stages of the product life cycle.

1.2 Motivation and Problem Statement

MCP provides solution for miniaturization (high-density package-routing) yet high computing performance requirement (increased data rate, increased IO count), by shortening the inter-chip distance to suppress the impacts of delay and high-speed effects. Nonetheless, increase core frequency and routing density will continue to be the trend in digital design. The increased in processing speed in MCP has brought the challenges of power delivery and thermal management due to multiple heat sources. The package design challenges and thermal management on MCP and the potential solutions to meet all design constraints have been addressed in (Boon Howe Oh et al., 2006). In addition, high density routing is unavoidable due to the confined package gap (typically in the range of millimeters) between the silicon devices. Due to the physical limitation of inter-chip spacing, imposed by technology and finite form-factor of a chip, combination of high density inter-chip package routing and increased operating frequency presents unique signaling challenges. In fact, our simulation shows that closed eye was obtained as MCP was transitioned from 1 GHz to 2.5 GHz. The transmission lines suffer from the inter-symbol interference (ISI) when frequency goes higher, which can be a limiting factor for pushing ultra-high on-package communication bandwidth. Thus, this leads to a finite maximum achievable data rate offered by the MCP solution. Owing to this, a systematic analysis that allows identifying the maximum bandwidth per interconnection density for different types of transmission lines has been presented in (Víctor H. Vega-Gonzalez et .al, 2009) (G. Katopis et al., 2004) . Besides, the maximum system

frequency as a function of line length, type of driver and noise in MCP has also been developed in (Claudio Truzzi et al., 1997).

Their analysis, however, considers only the uniform transmission channel which comprise of striplines or microstrip lines in single ended or differential configurations. Element such as discontinuity and crosstalk due to non-ideal characteristic of the transmission channel such as bump break out/break in region are not being considered. In fact, overall system performance is largely depends on the interaction between various component that comprises the I/O channel (driver, bump break out, main route, bump break in, and receiver). In addition, identify the underlying root cause of the overall system failure and solving these problems before they occur will eliminate having to deal with them further into the project cycle, and will in turn cut down the development cycle and reduce the cost (Ang, 2012)

Therefore, with the aim to establish a design guideline that extend and ensure robust high performance for next generation MCP implementation, this scenario necessitates a comprehensive signaling analysis of the inter-chip I/O package interconnection that addresses the electrical performance challenges and the underlying root cause of the system failure in MCP by taking into consideration of the full I/O transmission channel effects.

1.3 Objectives

The main aim of this research is to enable next generation high-speed MCP channel. Figure 1.1 shows the topology of the MCP channel assessed in this thesis.

Figure 1.1: MCP Channel

The following research objectives have been identified to achieve the aim:

- To analyze the signal integrity of the inter-chip I/O routing in MCP as frequency surged.
- To examine the key challenges and limiting factors that constraint the enabling of high-speed inter-chip I/O routing in MCP.
- To investigate the dominant factors in accordance to operating frequency and package channel length for future MCP design references.
- To establish a design guidelines to extend the system bandwidth functions favorably under the next generation MCP operating frequency (>2.5 GHz).

1.4 Contribution

This research addressed the challenges posed by the effort to enable multi-gigahertz-MCP channel. Comprehensive SI analysis of MCP channel has been performed and published in ASQED 2012.

Key challenges and root causes were identified and discussed. The knowledge of the root causes were translated into an effective signal enhancement

strategy that extend the bandwidth of the MCP channel. Hence, significant time can be saved by concentrating on the potential solution instead of trial-and-error search, and turns complex signal integrity problems into a practical design solution.

Furthermore, a new design criterion for gigahertz highly-coupled inter-chip I/O routing in MCP has also been established. Both source and load termination is another essential criteria to extend the bandwidth of the MCP channel, besides the standard high-speed design criteria reported in (Víctor H. Vega-Gonzalez et al., 2009) (Bogatin, 2003), for instance: Type of topology (point-to-point), interconnect (stripline), bus architecture (single-ended, unidirectional), and termination scheme (source-series termination).

In addition, the findings in this research could be leveraged as the technology readiness analysis for the next generation MCP design implement in Broadwell Intel Processor (Mark Bohr, 2011). Thus, shorten the overall design cycle and allow faster time-to-market in order to achieved highest profit margins in the early stages of the product life cycle.

1.5 Scope of Research

In this research, the industrial designed MCP channel was leveraged as the reference to examine the design guideline that enable higher data-rate MCP channel. The examined MCP channel is a single-ended-unidirectional bus with point-to-point stripline routing. Besides, the bus was source on-die termination, and no equalization scheme was adopted. Likewise, this architecture was examined to take advantage of higher maximum achievable data-rate per unit area as reported in (Víctor H. Vega-Gonzalez et al., 2009).

In addition, this research focuses on the signal qualities analysis from the perspectives of eye opening margins and the reliability consideration indicated by the amount of signal overshoot/undershoot. This research was only focus on signal quality of one net (reflection), including bandwidth limitation (by driver, interconnect losses, and the receiver), and cross talk between multiple nets. Other SI issues such as rail collapse in the power and ground distribution, and electromagnetic interference (EMI) and radiation from the entire system will be consider in the future work.

Furthermore, the range of operating frequency and inter-chip length enveloped in the analysis were confined to 2.5 GHz, 5 GHz, 7.5 GHz with three inter-chip length ranging from 3 mm, 15 mm, 30 mm - sufficient for a typical MCP design – and only focus on data bus. Driver and receiver models which are specifically compatible with the next generation MCP speeds were not readily available. Therefore, both driver and receiver were assumed CMOS, and the operation remains as source synchronous to take advantage of low-power high-speed design (Bogatin, 2003). Besides, signaling enhancement scheme such as termination

scheme and equalization was assessed. We focus on the passive signaling enhancement techniques instead of active to take advantage of lower power overhead but with the trade-off of chip area. Nonetheless, package design/stack up was not being analyzed in this research. This is due to the growth of package technology is much slower compare to the advancement of silicon technology. Therefore, similar package stack up will usually be leveraged for few generations until new package technology is mature to be deployed. Besides, information of the package stack-up contains sensitive propriety information about the current technology adopted by the Intel that is not allowed to be disclosed.

1.6 Thesis Organization

An overview of the examined MCP channel architecture, together with the theoretical knowledge that was required for this thesis work was first presented in Chapter 2. The methodology to realize this research towards achieving the research's aim was highlighted in Chapter 3. Chapter 4 presented the SI analysis to determine the origin of signal distortion mechanisms (reflection, crosstalk, 3-db BW) associate to the MCP channel. In Chapter 5, sensitivity analysis was performed to determine the root cause of signal degradations. Besides, a set of termination and equalization schemes were also analyzed and compared. The findings were then being compiled and translated into a set of design guideline for the enabling of next generation MCP implementation as detailed in the last section of Chapter 5. Chapter 6 concluded the thesis work and discussed possible future directions.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter provides the essential theoretical background (based on the materials in (Bogatin, 2003) and (Hall, Hall, & Mccall, 2000)), and the related work from literature to gain better understanding of this thesis. In section 2.2, the basic principle of digital system and the challenge in modern digital design were recap. The background of MCP technology and the fundamental of SI were presented in section 2.3 and section 2.4. The related work for modeling, signaling analysis, and the enhancement techniques were reviewed in section 2.5 and section 2.6.

2.2 Modern High-Speed Digital Design

In this section, the basic principle of digital system was first recap. Then, the trend and challenges in digital design were introduced.

2.2.1 Basic Principle of Digital System

The basic idea in digital design is to enable the right communication between devices with signals representing 1s or 0s (digital symbol). The medium connecting the devices and allow the signal to be transferred between devices is known as interconnects or sometime refer as transmission channel. This includes the entire electrical pathway from the chip sending a signal to the chip receiving the signal.

Ideally, receiver will switch high as long as the input voltage exceed a threshold voltage (Vref), and switch low as long as the input voltage falls below the

threshold voltage. This threshold voltage associates to the silicon that makes the transistor. However, due to the fact that the characteristic of the silicon varies with temperature, supply voltage, silicon process, and other variables, there are usually high-and low-voltage thresholds, known as Vih and Vil, associated with the receiving silicon, above which and below which a high or low value can be guaranteed to be received under all conditions.

Figure 2.1 illustrates the difference between the actual and ideal case of the digital system. Thus, the main objective of digital design is to ensure that the system can, under all conditions, deliver high voltages that do not, even briefly, fall below Vih, and low voltages that remain below Vil, by controlling the integrity of the data.

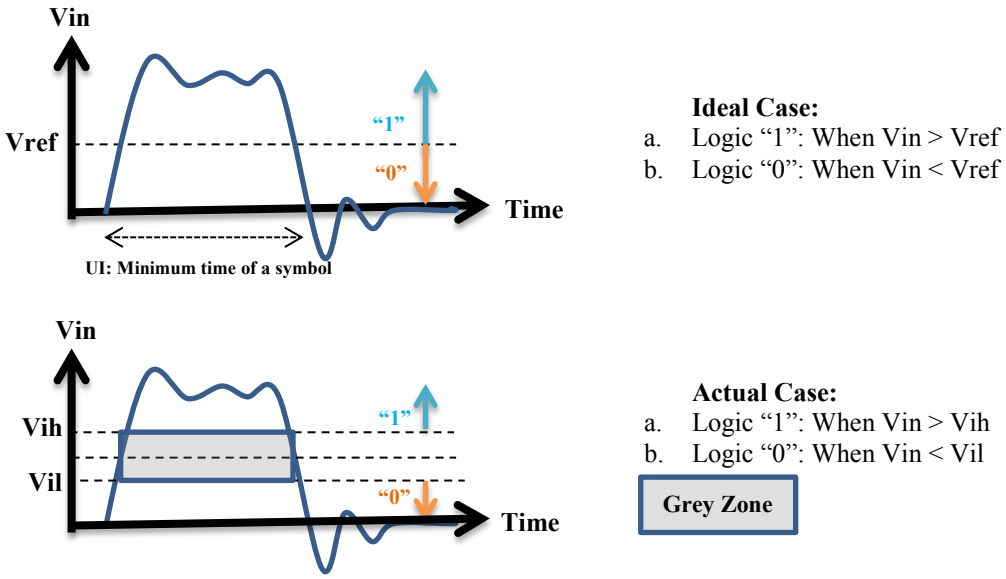


Figure 2.1: Ideal versus actual signal threshold

Once the receiver has been switched, it needs to sample the signal in order to obtain the binary encoded information. The data sampling process is usually triggered by the rising edge or the falling edge of a clock signal. Data must arrive at the receiving gate on time and settle down to a non-ambiguous logic state when the receiving component starts to latch in, defined by setup and hold time. Any delay of

the data or distortion of the data waveform will result in a failure of the data transmission. Imagine if the signal exhibits excessive ringback into the logic gray zone while the sampling occurs, then the logic level cannot be reliably detected.

The minimum time required for a signal is limited by the minimum time requires performing all the operations in one cycle. Usually, there are three main factors that contribute to this minimum time: the intrinsic time for all the gates that need to switch in series, the time for the signals to propagate through the system to all the gates that need to switch, and the setup and hold times needed for the signals at the inputs to be read by the gates (Bogatin, 2003).

For source synchronous operation and if sources of signal distortion are absence, the main factor determine the unit interval (UI) of a symbol (minimum time of a symbol) is the setup and hold times needed for the signals at the inputs to be read by the gates. In actual case, however, due to imperfection of the system such as finite signal rise time, random and deterministic noise in the channel, the UI is usually larger to accommodate those impacts. At the same time, to enable lower power and higher data rate operation, the voltage level and the minimum time per symbol need to be reduced, which means shrink in noise and timing budgets. This scenario illustrates the challenges face in modern low-power high-speed digital design where magnitude of noises needs to be confined within the reduced timing and voltage budget of a system.

2.2.2 Trend in Digital System

The dominant factor influencing the minimum cycle time is the switching speed of the transistors. If the switching time can be reduced, the minimum total time required for one cycle can be reduced. This is achieved by continue reducing the

transistor feature size, i.e. shorten the gate channel length of transistors to enable the transistor to switch faster. Furthermore, the smaller the chip size, the more chips can be fit on a wafer and the lower the cost per chip. Thus, chip-fabrication factory can increase the overall yield. Therefore, it is inevitable that as transistor feature size continues to reduce, rise time will continue to decrease and clock frequencies will continue to increase. The projections from the 2001 Semiconductor Industry Association (SIA) International Technology Roadmap for Semiconductors (ITRS) for future on-chip clock frequencies, based on projected feature size reductions, compared with the Intel processor trend are shown in Figure 2.2. This shows the projected trend for clock frequency increasing at a slightly diminishing but still growing rate for the next 15 years as well.

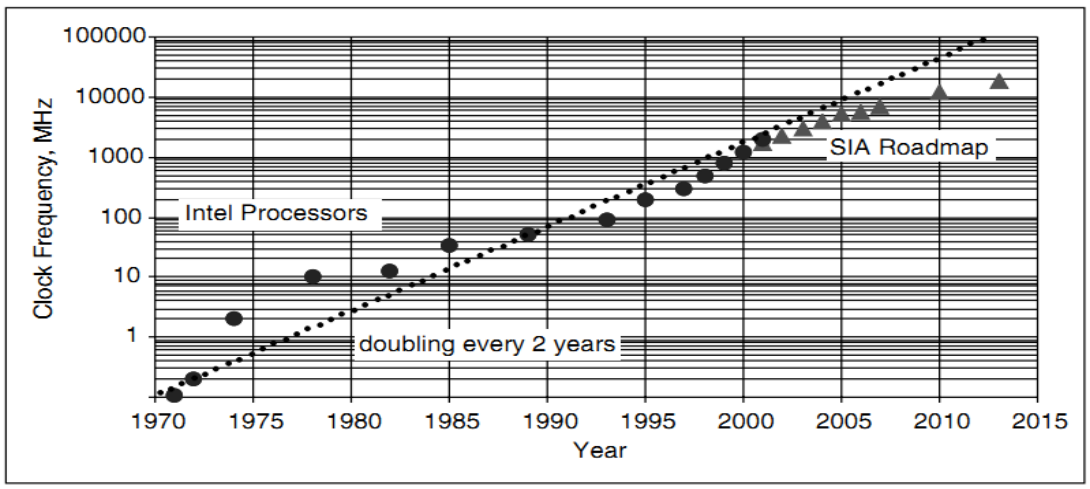


Figure 2.2: Trend in the clock frequency processors and the Semiconductor Industry Association roadmap expectations (Bogatin, 2003).

2.2.3 Design Challenges

As shown in previous section, core frequency will continue to increase, faster data rates will be demanded from the buses that feed the information from/to the core. This means only a short time is left for the signal to be in transition, and the

rise-times will continue their inevitable march toward shorter values. In most high-speed digital systems, the time allocated to the rise time (RT) is about 10% of the clock cycle time (Bogatin, 2003). Based on this generalization, the RT is roughly related to the clock frequency by Equation 2.1:

$$RT = \frac{1}{10\ x\ F_{clock}} \tag{2.1}$$

The consequence is, signal integrity (SI) problems will get more severe. It is unavoidable that as RT decrease, the noise problems will increase and be more difficult to solve. Shrink in timing budget together with increase in SI problems are the design challenges need to be overcome in order to continue Moore's law. SI problems may become the bottleneck of the overall system performance. Thus, this scenario necessitates the SI analysis to be performed during the early design phase to ensure reliable high-speed data transmission.

2.3 Multi-Chip Package (MCP)

In this section, the background of MCP technology as well as the type of bus architecture was recap.

2.3.1 MCP Technology

MCP is an electronic module system where multiple bare die are packaged on a single substrate as shown in Figure 2.3. It has emerged as another compelling solution to enable high performance and power efficient electronic devices e.g. tablets, smart-phones and small form-factor laptops. Besides, it is also driven by the product definition, time-to-market, reusability as well as cost as the main driver. The advantages of MCP implementation are summarized as follows: (Ang, 2012)

- Lower Cost: Fewer packages with few numbers of leads, a simplified board layout, and the feasibility of mixed technologies in the same package results in cost saving.
- Lower Power Consumption: Lower I/O drive strength configuration is required for inter chip transfer within the same package.
- Higher Integration Density: Allow substitution of several packages for one slightly larger but single package, and will either free board real estate for other use or help reduce the board size.
- Time-to-Market: Allows much faster introduction of the product into the market compared to integrating all the desired functions on a new single chip via insertion of several dies into the same package.

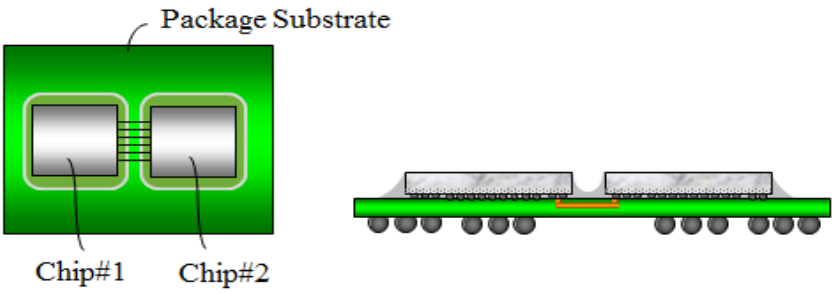


Figure 2.3: Top and side view of MCP

2.3.2 Overview of Bus Architecture

In general, there are two type of buses, multi-drop and point-to-point bus. Traditional multi-drop buses, such as Peripheral Component Interface (PCI), have moved to point-to-point links, such as PCI-express, RapidIO interconnect and Redwood parallel interface (Zhang, 2009). The reason is that multi-drop buses suffer from impedance mismatches which limit the switching frequencies, and the capacitive loading and stub effects which limit the bus scalability. As opposed to

multi-drop buses, point-to-point links provide tight control of electrical parameters of the bus and therefore enable higher operating frequencies.

Point-to-point links can be serial links or parallel buses. Parallel buses can provide higher bandwidth by increasing clock frequency or the width of the bus, and it has lower latency because the drivers and receivers are simple. However, the number of pins available limits the bus width, and routing can be challenging since signal trace lengths have to precisely match the length of clock trace. Compared with parallel buses, serial links use fewer pins and avoid the trace-matching problem by embedding clock into data stream. By doing this, the component costs and board layout complexity are reduced. One of the disadvantages of serial links is the large latency introduced by complex transceivers, serialization/deserialization, encoding/decoding and clock recovery. Over the last decade, serial links have all but replaced parallel buses for high speed chip-to-chip and backplane communication. High-speed serial signaling over transmission lines is a robust, power-efficient alternative to global parallel buses. Serial signaling removes the requirement to match multiple bus lines. Properly designed PCB traces form low loss transmission lines, and offer propagation speeds close to the speed of light. Serial links based on transmission lines allow higher data rates, yet generate less noise and are less prone to interference than parallel buses. (M. P. Flynn et al., 2005)

In addition, bus can be common-clock or source synchronous bus. Common-clock bus is replaced by source synchronous bus to take advantage of significant increase in maximum bus speed. Strobe and data signal are sent from the same driver. Therefore, internal propagation delay in driver circuit and flight time are theoretically no longer a factor in the timing equation for the source synchronous bus, therefore it free-up the timing budget. The maximum bus speed is now limited

by the receiver setup and hold time, difference between data and strobe signal, and the manifestation of the transmission line effects. Figure 2.4 shows the block diagram of a source synchronous and common-clock bus.

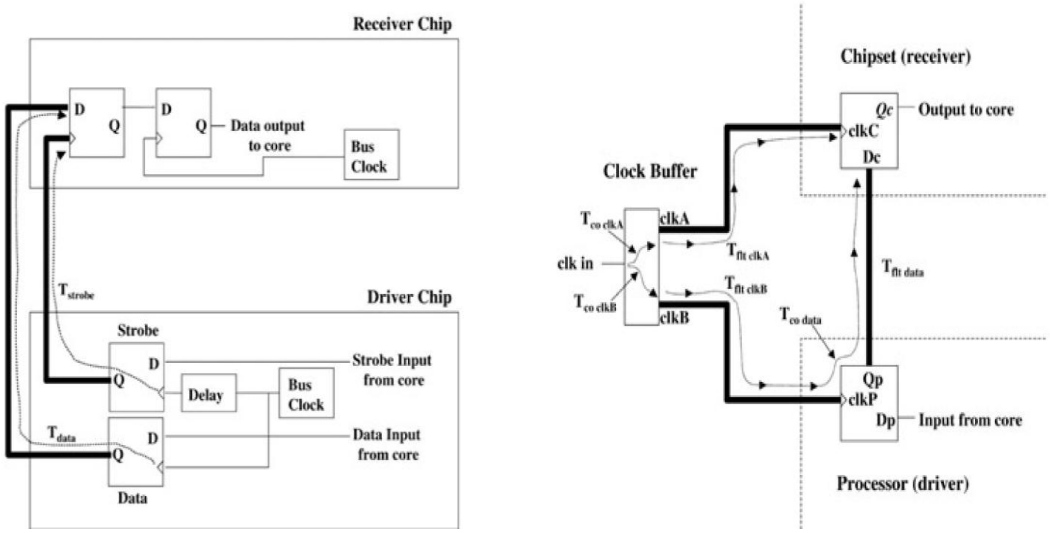


Figure 2.4: Block diagram of a source synchronous (left) and common-clock (right) bus (Hall, Hall, & Mccall, 2000).

2.4 Signal Integrity (SI)

In this section, the understanding of SI, and the theoretical basis of transmission line were recap.

2.4.1 What is Signal Integrity

SI problems relate to all the problems that arise in high-speed products due to the interconnects i.e. how the physical interconnects - interact with the digital signal's voltage and current - screw up pristine signals coming from the integrated circuits (Bogatin, 2003). SI addresses two concerns in the electrical design aspects, the timing and the quality of the signal. The goal of SI analysis is to ensure reliable high-speed data transmission.

When SI problems happen and the system noise margin requirements are not satisfied then it will cause logic error and results in system failure. These types of noise faults are extremely difficult to diagnose and solve after the system is built or prototyped. Understanding and solving these problems before they occur will eliminate having to deal with them further into the project cycle, and will in turn cut down the development cycle and reduce the cost (Chou, 1994). In general, there are three ways in which the electrical properties of the interconnect can affect system performance: by degrading timing, by introducing excessive noise, and by radiating enough to exceed an Electro Magnetic Interference (EMI) compliance test. All of the signal integrity problems fall into one of the following categories: timing, noise and EMI (Bogatin, 2003). Furthermore, signal-integrity noise problems are related to one of the following four unique families of noise sources:

1. Signal quality of one net, including losses on the line
2. Cross talk between two or more nets, including ground and power balance
3. Rail collapse in the power and ground distribution
4. Electromagnetic interference and radiation from the entire system

2.4.2 What is Transmission Line

Transmission Line Properties

A transmission line is a new ideal passive circuit element with very different properties compare to other ideal passive element such as resistors, capacitors, and inductors. It comprises two conductors, i.e. the signal path and the return path where electric field is established (Bogatin, 2003). The basic electrical characteristics that define a transmission line are its characteristic impedance and time delay$\left(\frac{\text{propagation velocity}}{\text{line length}}\right)$, whereas other passive circuit elements are characterized

by impedance alone. In addition, unlike other passive element, signal will propagate in transmission line - it takes time to travel down the line at the propagation velocity depends on the surrounding medium – and will reflect when encountered any impedance changed during its propagation.

Transmission Line Structures

The two most common types of transmission lines used in digital designs are microstrips and striplines. A microstrip is typically routed on an outside layer of the PCB and has only one reference plane. There are two types of microstrips, buried and nonburied. A buried (sometimes called embedded) microstrip is simply a transmission line that is embedded into the dielectric but still has only one reference plane. A stripline is routed on an inside layer and has two reference planes. Figure 2.5 represents a PCB with traces routed between the various components on both internal (stripline) and external (microstrip) layers.

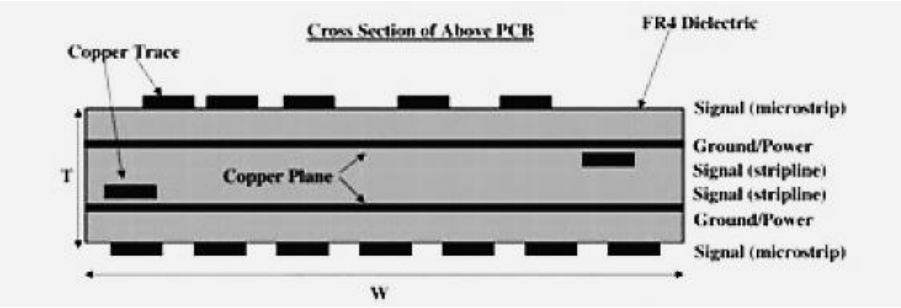


Figure 2.5: Type of transmission line structure (Hall, Hall, & Mccall, 2000)

2.4.3 SI Problem – The Cause of Eye Collapsed

The theoretical understanding of the sources of eye collapsed such as reflection, line losses, crosstalk as well as the intersymbol interference (ISI) mechanism were reviewed in this section.

2.4.3.1 Reflections

When the signal leaves the output driver, the voltage and the current, which make up the signal, see the interconnect as an electrical impedance. If the impedance the signal sees stays the same, the signal continues undistorted. If, however, the impedance changes, the signal will reflect from the change and continue through the rest of the interconnect with a different amplitude. This can be at the ends of lines or wherever the topology of the line changes, such as layer change through a via, through a connector, a branch, tee, or stub, corner, a gap in return-path plane, line-width change, etc. The locations where the instantaneous impedance changed are called impedance discontinuities. The amount of signal that reflects depends on the magnitude of the change in the instantaneous impedance as illustrated in Figure 2.6.

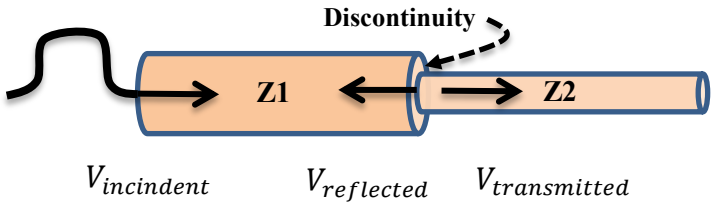
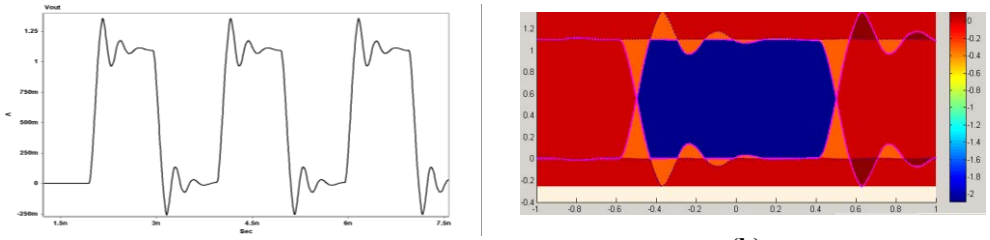


Figure 2.6: Incident signal, reflected signal, and transmitted signal

Reflections give rise to degradation in timing and signal quality such as ringback, overshoot and undershoot. The overshoot, when the signal level exceeds its steady state value, can cause device reliability issue. The undershoot, when the signal level drops or ring back, can eat into the noise budget and contribute to false triggering. One example of the reflection noise generated from impedance discontinuities at the ends of a short-length transmission line is shown in Figure 2.7.



(a) (b)

Figure 2.7: (a) Reflection noise and (b) eye diagram at the receiver end of a 5mm interconnect created because of impedance mismatches and multiple reflections

Two coefficients describe the reflection activity as shown in Equation 2.2 and Equation 2.3:

a) Initial voltage, $V_{incident}$ launched to the transmission line.

$$V_{incident} = V_s \frac{Z_1}{Z_1+Z_s} \tag{2.2}$$

b) Reflection coefficient, ρ describes the fraction of the voltage that reflects back to the source.

$$\rho = \frac{V_{reflected}}{V_{incindent}} = \left(\frac{Z_2-Z_1}{Z_2+Z_1}\right) \tag{2.3}$$

c) Transmission coefficient, Γ that describes the fraction of the incident voltage that is transmitted through the interface into the second region.

$$\Gamma = \frac{V_{transmitted}}{V_{incindent}} = 2 * \left(\frac{Z_2}{Z_2+Z_1}\right) \tag{2.4}$$

where:

$V_{reflected}$= the reflected voltage

$V_{incindent}$ = the incident voltage

$V_{transmitted}$ = the transmitted voltage

Z_1 = the instantaneous impedance of the region where the signal is initially

Z_2 = the instantaneous impedance of the section where the signal just enters

Z_s = the driver source impedance

ρ = the reflection coefficient

Γ = the transmission coefficient

To avoid reflection, the goal is to keep the instantaneous impedance the signal sees as constant as possible. The important strategy to minimize impedance changes and reflection noise are: 1. Keep the instantaneous impedance of the line constant. 2. Manage the impedance changes at the ends of the line with a termination strategy. 3. Maintain a linear routing topology with no branches or stubs. 4. Minimize any geometry discontinuities (Bogatin, 2003).

2.4.3.2 Line Loss (Component Bandwidth)

Practical transmission lines have significant losses. If the losses were independent of frequency, low-frequency components were attenuated the same as high-frequency components. Then, the entire signal waveform would uniformly decrease in amplitude, but the rise time would stay the same, and that effect may not be a concerned as it could be compensated with some gain at the receiver.

Nonetheless, the losses associate to the real lossy transmission line is frequency dependence. When the signal propagates down the real lossy transmission line, frequency dependence loss causes amplitudes of the higher-frequency components being reduced and the low-frequency components stay about the same (Bogatin, 2003). This results in reduction of the signal bandwidth which means the rise time of the signal has increased. The fundamental problem caused by lossy lines is rise-time degradation, which appears as deterministic jitter and may results in ISI as operating frequency surged. Figure 2.8 shows the collapsed eye diagram, and increased jitter (indicated by the widening of the cross-over regions) for the same 30 mm line operating at 5 GHz waveform, with and without losses.

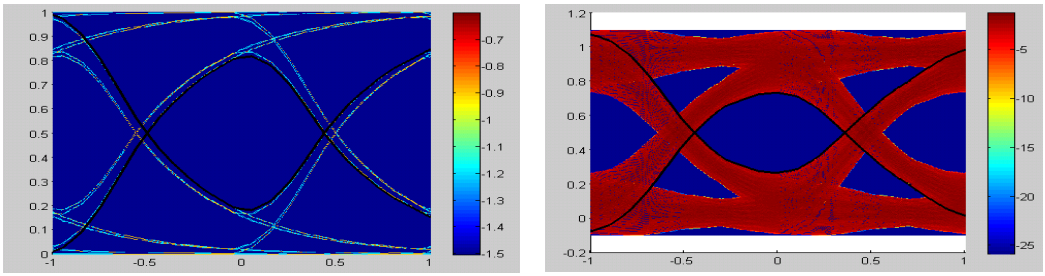


Figure 2.8: Eye diagrams of 30 mm interconnect line at 5 GHz transmission rate. Left: Ideal loseless line. Right: Real lossy transmission line.

There are five ways energy can be lost to the receiver while the signal is propagating down a transmission line (radiative loss, coupling to adjacent traces, impedance mismatches, conductor loss, and dielectric loss) that explicates the origin of the line loss. In spite of everything, conductor loss is the primary loss mechanisms cause the attenuation in transmission line (Bogatin, 2003).

The frequency dependence of skin depth, δ is account for the frequency dependence resistance which account for the conductor loss, not the resistivity of copper which is very constant across frequency (Hall, Hall, & Mccall, 2000). At a high frequency, the cross section through which current will be flowing in a copper conductor is in a thickness approximately equal to the δ. At higher frequencies, the current in each conductor wants to spread out as far apart as possible to minimize the partial self-inductance of each conductor, and simultaneously, the oppositely directed current in each conductor will move as close together as possible to maximize the partial mutual inductance between the two currents. Therefore, at higher frequencies the current will be using a thinner section of the conductor, and this explains the resistance of the conductor at high frequency is higher than at low frequency.

2.4.3.3 Intersymbol Interference (ISI)

ISI is a significant contributor to signal distortion in any high-speed design, especially so when the period is smaller than two times the delay of the transmission line (Hall, Hall, & Mccall, 2000) (Bogatin, 2003). If the rise time were short compared to the bit period, there would be no ISI. ISI noise occurs when signal is not fully settled before the next transition. For instant, signal is transmitted down a transmission line and the noise on the bus due to reflections, crosstalk, or previous signal have not stabilized and reached the final value/settled completely, the signal launched onto the line will be affected, degrading both the timing and the signal integrity margins.

In addition, the degree of ISI from losses and other effects, such as capacitive discontinuities of vias, will collapse the eye diagram. The time for the signal to reach the switching threshold will change depending on the previous data pattern. If the transmitted signal in displayed in an eye diagram where each bit is overlaid with the previous one, synchronized to the clock, a distorted eye with large jitter and interference is observed as shown in Figure 2.9. If there is no ISI, the eye pattern will be perfectly open. In other words, each bit, no matter what the previous pattern was, would look the same and be identical to the previous bit. Its eye diagram would look like just one cycle. If the eye collapses more than the noise margin of the receiver, the bit error rate will increase and may cause faults.

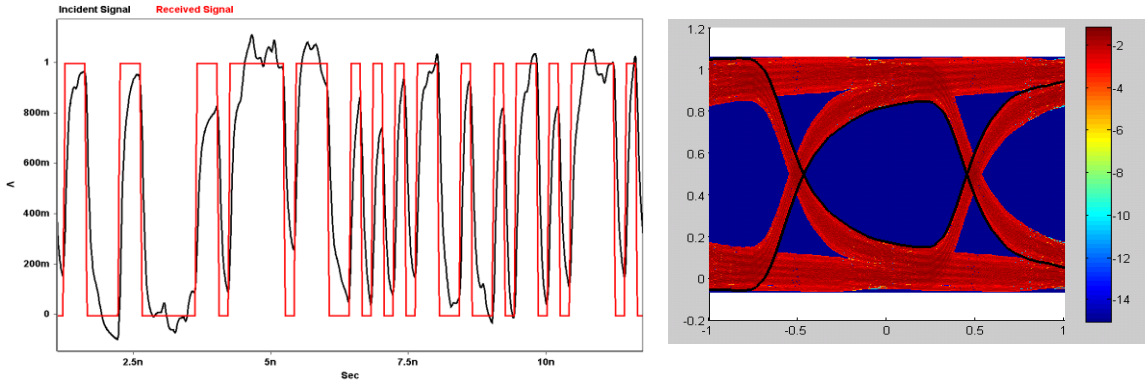


Figure 2.9: ISI occur when a signal is transmitted down a transmission line where previous signal have not stabilized and reached the final value/settled completely

2.4.3.4 Crosstalk between Nets

Crosstalk is an effect where an unwanted signal from one net is transferred to an adjacent net. Crosstalk happens between the signal and return paths of one net and the signal and return paths of a second net. The entire signal-return path loop accounts for the crosstalk, not just the signal path. When one net carries a signal (aggressor net), some of this voltage and current can pass over to an adjacent quiet net (victim net), and appear as unwanted noise. Crosstalk can cause two detrimental effects, and is depends on total coupled length. First, crosstalk will change the performance of the transmission lines in a bus by modifying the effective characteristic impedance and propagation velocity, which will adversely affect system-level timings and the integrity of the signal. Additionally, crosstalk will induce noise onto other lines, which may further degrade the signal integrity and reduce noise margins. These aspects of crosstalk make system performance heavily dependent on data patterns, line-to-line spacing, and switching rates (Hall, Hall, & Mccall, 2000).

Various terminologies have been used to describe crosstalk between transmission lines. For the sake of studying the crosstalk mechanism, we define forward crosstalk to be the crosstalk coincident with wave propagation. Hence, the

forward crosstalk does not depend on termination conditions. On the other hand, backward crosstalk is defined to represent any coupling due to reflection, so it is a direct function of line impedance and termination conditions. We reserve NEXT and FEXT to be the total coupled or net voltage from the forward and backward crosstalk components at the source-end and load-end of the victim line, respectively (Oh et al., 2011).

The origin of crosstalk is illustrated as follows. When a signal propagates down a transmission line, there are electric-field lines between the signals and return paths and rings of magnetic-field lines around the signal and return path conductors. These fields are not confined to the immediate space between the signals and return paths. Rather, they spread out into the surrounding volume. We call these fields that spread out fringe fields. Fringe fields drop off very quickly as we move farther away from the conductors. Neighbor quiet transmission lines are being coupled through mutual capacitor - between every pair of sections of the transmission lines - and loop mutual inductor - between every pair of signal- and return-loop sections - if they are at the vicinity of the fridge field. When the signal voltage and current in the active line changes or the electric and magnetic fields changes, unwanted signal is coupled to the quiet line by the flow of the noise-current through the mutual capacitor, and is induced in a mutual inductor (Bogatin, 2003).

Crosstalk occurs in two different environments: when the interconnects are uniform transmission lines, as in most traces in a circuit board, and when they are not uniform transmission lines, as in connectors and packages. When the return path is a wide, uniform plane, as is the case for most coupled transmission lines in a circuit board, the capacitively coupled current and inductively coupled currents are of the same. When the return path is not a wide uniform plane, but is a single lead in a