Accurately Modeling of Zero Biased Schottky-Diodes at Millimeter-Wave Frequencies

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Abstract: This paper presents and discusses the careful modeling of a Zero Biased Diode, including low-frequency noise sources, providing a global model compatible with both wire bonding and flip-chip attachment techniques. The model is intended to cover from DC up to W-band behavior, and is based on DC, capacitance versus voltage, as well as scattering and power sweep harmonics measurements. Intensive use of 3D EM (ElectroMagnetic) simulation tools, such as HFSS^{TM}, was done to support Zero Biased Diode parasitics modeling and microstrip board modeling. Measurements are compared with simulations and discussed. The models will provide useful support for detector designs in the W-band.

Keywords: W band; Schottky Diode Detectors; ZBD modeling; wire bonding; flip-chip

1. Introduction

Schottky diodes play an important role in several functions, such as rectification [1,2], mixing [3,4], and detection in all the range of microwave frequencies, up to the W-band and beyond [4].

In general, modeling of the diodes is a critical task in the design process of circuits operating at high frequencies [3,4]. Antimony (Sb) heterostructure backward diodes offer better noise performance with easier matching to 50 Ohm [5] compared to GaAs Schottky diodes, but may not always be easily accessible or available as discrete components [6]. Series 9161 diodes (Keysight HSCH and MACOM-Metelics MZBD) models are frequently used for hybrid detectors below the W-band [7–9], though also in the W-band [10–13]. Zero-bias Schottky diodes from ACST (Advanced Compound Semiconductor Technologies GmbH) (https://acst.de/) operating as power sensors have been reported in [14]. Zero Bias Diodes Schottky diodes from Virginia Diode Inc. (VDI) were used for W-band detection in [6,15]. Available manufacturer information (https://www.vadiodes.com/images/pdfs/Spec_Sheet_for_VDI_W_Band_ZBD.pdf) is limited and, in the absence of diode models developed by the designers themselves, commercially available models could be required.

Usually, the device modeling is accomplished by discriminating between the modeling of the intrinsic component (characterized by quasi-static I-V and C-V measurements) and the extrinsic elements (characterized by 3D Electro-Magnetic (EM) tools, along with the measurement of the Scattering parameters at some specific bias points). In [16], modeling techniques are presented to extract a Schottky diode model analytically using additional fabricated structures (such as short and open circuits) for the de-embedding of parasitic capacitances and other effects. Unfortunately, it is not

always possible to have such customized cal kit (calibration kit) structures available. Previous efforts in Schottky diode modeling of Single Anode (SA) VDI devices were presented in [17]. In this paper, ZBD (Zero Bias Diode) devices from VDI have been carefully modeled, considering two different diode-mounting techniques to attach them to the final circuit assembly: wire bonding and flip-chip (also known as controlled collapse chip connection). From DC measurements, the intrinsic nonlinear current source, along with the parasitic resistor can be obtained. Scattering measurements of the ZBD provide data which can be used to identify the parasitic and extrinsic elements up to the W-band; in this sense, in Section 2, the modeling of ZBDs for wire bonding assembling is presented. In Section 3, the modified model oriented to the flip-chip attachment technique, obtained from the previously extracted diode model, is shown; low-frequency noise sources are included in the complete diode model in Section 4. Finally, some conclusions are drawn in Section 5.

2. Nonlinear Zero Bias Diode Modelling

Modeling of the ZBD was based on the procedures presented in [16,17]. Firstly, a 3D model of the passive parts for EM simulation (HFSS^{TM}) was built based on microphotographs (Figure 1) and physical measurements of the critical dimensions, performed with a Scanning Electron Microscope (SEM) available in the Laboratory of Science and Engineering of Materials of the University of Cantabria (LADICIM).
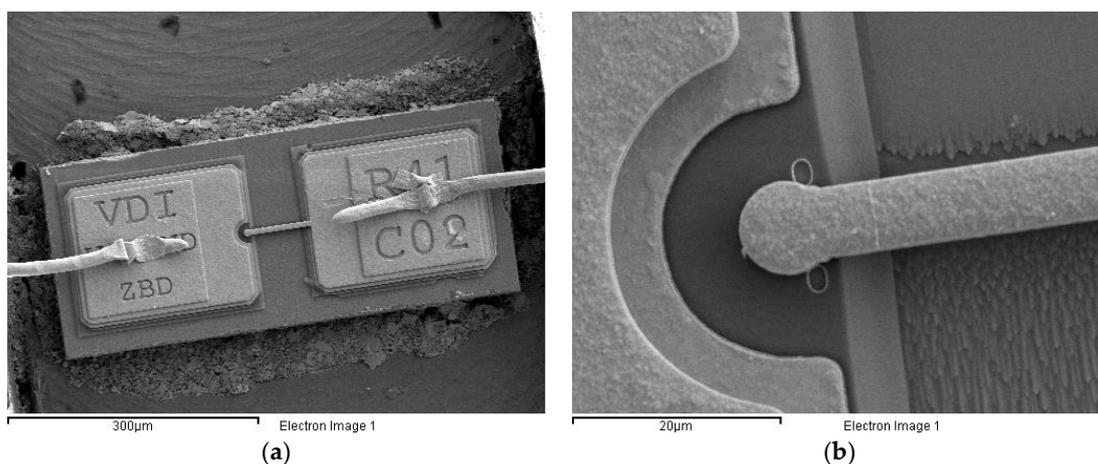

Figure 1. (**a**) General View of the ZBD using SEM (Dice about 600 × 250 μm; anode finger length about 100 μm). (**b**) Detail of the anode finger of the ZBD (diameter about 9 μm). Reference scale is at the bottom of the figures.

2.1. DC Measurements and Nonlinear Model

For modeling purposes, as a starting point, the diode equivalent circuit presented in Figure 2 is here considered. In this circuit, the main non-linearities (Id Current Source and Cj Capacitance), as well as parasitic elements due to metallization (Rs) and packaging (Cpp, Cp, and Lf), can be observed.
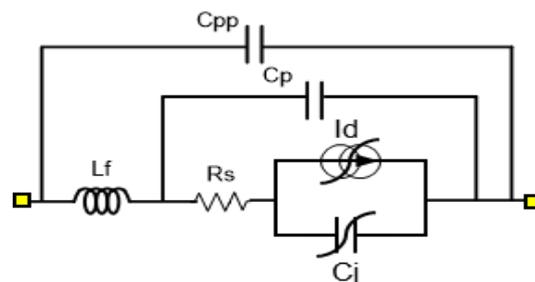

Figure 2. Diode equivalent circuit model.

Using a specific high-accuracy voltage-controlled current source to ensure both protection of the device during the test process and accurate current/voltage measurements in the low current level region (below 1 mA), the static I/V characteristic of the ZBD was measured (Figure 3). By means of proprietary extraction software, the value of the thermionic-field emission model parameters [18] for the nonlinear current source (1) were obtained (Table 1).

$$I(V_d, T) = I_s e^{\left(\frac{q(V_d - I_d\,R_s)}{\eta KT}\right)} \tag{1}$$
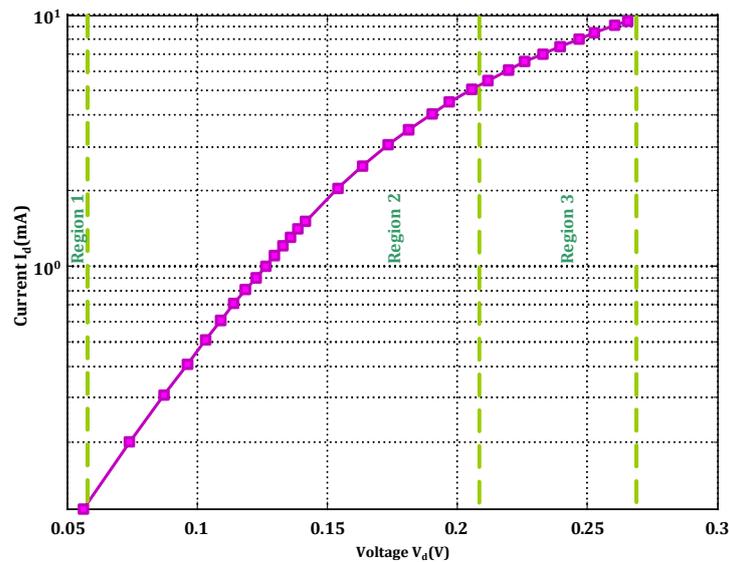

Figure 3. I-V measured current for the ZBD Schottky diode under testing.

Table 1. Extracted value of parameters in Equation (1).

Parameter	Value
I_s (A)	2.78×10^{-5}
η	1.37
$\alpha = \frac{q}{\eta kT}$ (1/V)	28.6
R_s (Ω)	6.48

2.2. Low-Frequency Model

At lower microwave frequencies, the equivalent circuit of the unbiased, or negatively biased, diode can be reduced to a "π" electrical network of capacitances, as depicted in Figure 4.
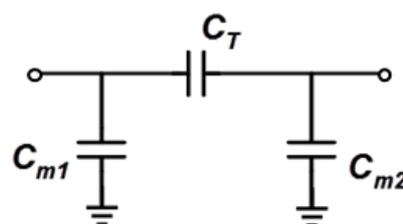

Figure 4. Low-frequency equivalent circuit model of the passive diode.

The above "π" network accounts for the total capacitance C_T, as well as the small-value parasitic capacitances to the ground (if considered), C_{m1} and C_{m2}, where C_T is the sum of the junction capacitance C_j and the parasitic capacitances C_{pp}, as shown in Equation (2).

$$C_T = C_j(V) + C_{pp} = \frac{C_{j0}}{\sqrt{1 - \frac{V_d}{\phi_{bi}}}} + C_{pp} \tag{2}$$

An accurate estimation of the total capacitance can be extracted from the measured value of the S_{21} scattering parameter (Figure 5) when a negative bias, V_d, is applied to the diode. Parameter S_{21} essentially depends on the total capacitance, C_T (the junction capacitance C_j at $V_d = 0$ V, C_{j0}, junction potential, ϕ_{bi}, and the parasitic capacitance C_{pp}). Scattering parameters of the diode were measured from 2 GHz up to 50 GHz; however, for capacitance extraction purposes, only the frequency range of 3–10 GHz was used, considering the equivalent circuit in Figure 4. By varying the negative V_d voltage applied to the diode, and performing the measurement of the scattering parameters of the diode at each voltage, it was possible to extract the values of the C_T capacitance as a function of this voltage. In Figure 6, the extracted Capacitance versus Voltage (*C-V*) plot is presented. In Table 2, the values of the elements of the circuit in Figure 2, as well as the parameters of Equation (2), are presented.
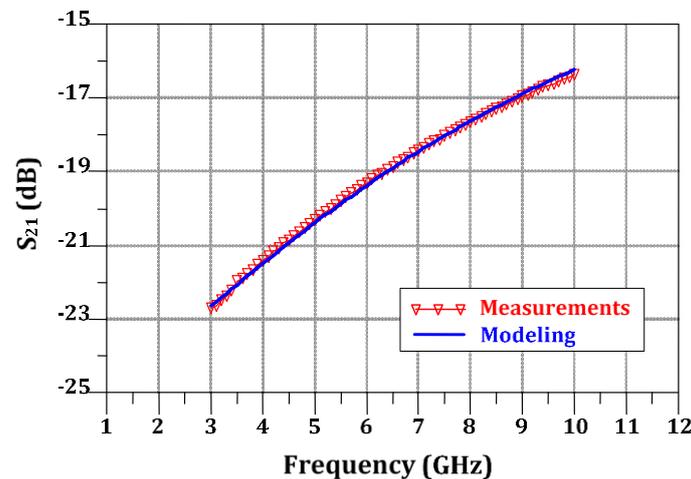

Figure 5. Measurements and modelling of transmission coefficient for the unbiased ($V_d = 0$ V) ZBD.
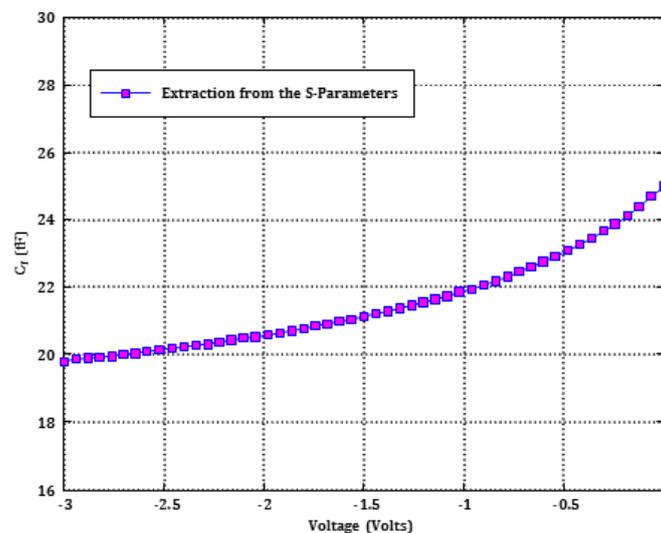

Figure 6. Results for the extraction of total capacitance of the ZBD from scattering parameters.

In principle, the results obtained in the extraction from the S-parameters offer more accurate estimations of nonlinear and parasitic capacitances of this diode, compared to other extraction methods based on low-frequency impedance measurements. This also avoids other potential problems of low-frequency measurements, such as uncertainty in the de-embedding of the parasitic effects of probes.

Table 2. Value of parameters of Equation (2).

Parameter	Value
C_T (fF)	26
C_{j0} (fF)	10
C_{pp} (fF)	16
ϕ_{bi} (V)	0.16
C_{m1} (fF)	50
C_{m2} (fF)	50

2.3. Modified ZBD Model Up to W-Band

At high frequencies, from 75 GHz up to 110 GHz, additional parasitic effects arise which affect the behavior of the diode; thus, it is critical to evaluate and model them. This is really a complex task due to the difficulties involved in the de-embedding process of the access elements, such as coplanar-to-microstrip (CPW-M) transitions and bonding wires used in the circuit assembly to implement the input and output connections. This is the reason why, although the diode is usually considered as a one-port element, with the cathode or the anode grounded, we are going to perform measurements being anode and cathode the electric ports, considering the diode as a two-port electrical network, allowing to identify the effect of grounding.

Firstly, modeling of the coplanar to microstrip (CPW-M) transitions was performed, as reported in [17]. Once the model of the CPW-M transition was obtained, the modeling of the ZBD, when using the wire bonding attachment technique, was possible from the measurements performed at the coplanar probe station using a LRRM (Line-Reflect-Reflect-Match) calibration. A de-embedding procedure in Keysight ADS™ [19] was performed considering the previously obtained model of the CPW-M transition along with the gold bonding wire model.

In Figure 7, the reflection and transmission coefficients from the equivalent circuit simulation are compared with the experimental measurements in two frequency ranges (2–50 GHz and 75–110 GHz) for the unbiased diode ($V_d = 0$ V). From these results, it can be concluded that the degree of agreement between both results is excellent. Therefore, the modeling procedure proposed provides a model that can simulate the behavior of ZBD from the DC up to 110 GHz.
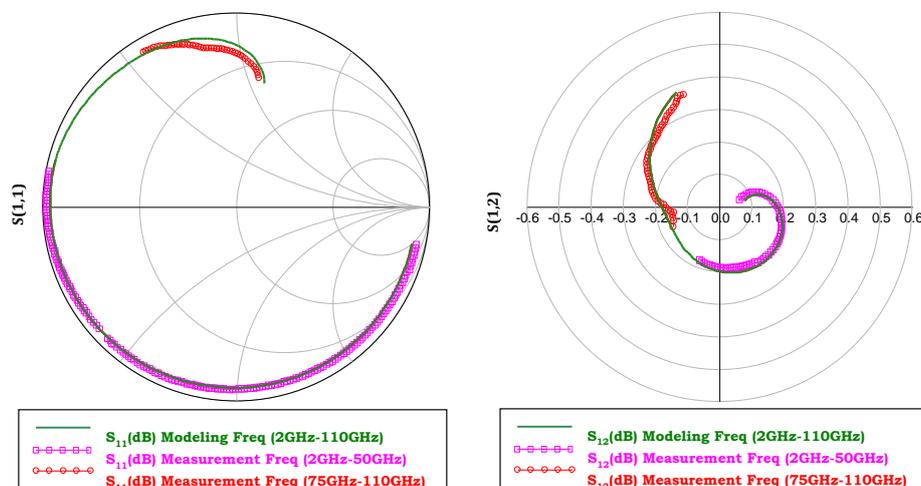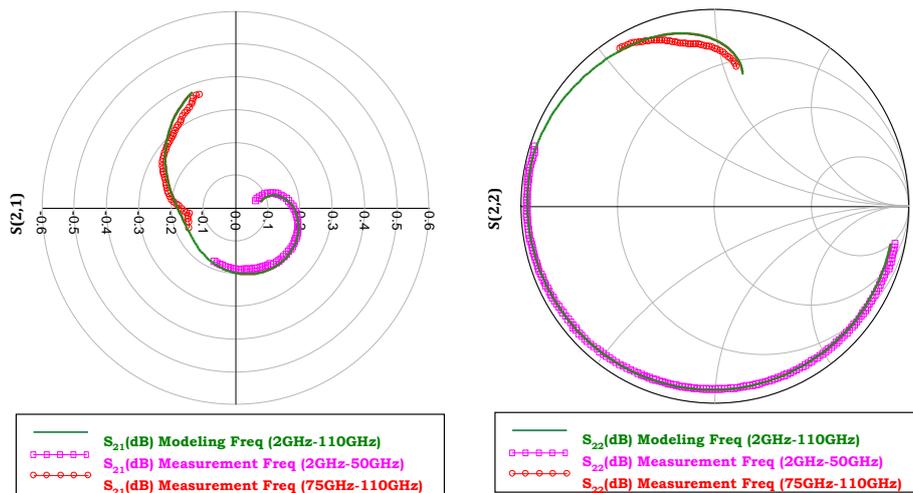

Figure 7. *Cont.*

Figure 7. Modelled and measured [S]-parameters of the unbiased diode (0 V) after the de-embedding in the wire bonding configuration.

An increase in the series resistance value was observed in the W-band measurements; this singular behavior can be associated with the skin effect above 50 GHz, the bonding wires, and probably some other measurement uncertainties. The study of the extent of this effect becomes difficult in this frequency band as measurements are limited by calibration accuracy, as well as some possible inaccuracies in the determination of other equivalent circuit parameters, such as finger inductance and parasitic capacitances. Nevertheless, the increase in resistance in the W-band was consistently found when fitting measurements of several devices, as previously reported in the literature [20].

2.4. Large Signal Model Extraction and Validation

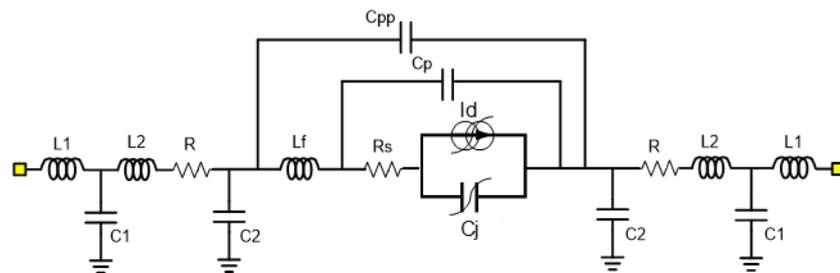The final topology of the proposed diode's large signal model is shown in Figure 8 [6].

Figure 8. Equivalent circuit model of the diode, including the extrinsic elements.

In Table 3, the values of the model parameters obtained from the different measurements performed using the extraction procedures [16,17] are presented. In this model, C_p represents the finger-to-pad capacitance between the anode contact finger and the underlying active GaAs. The bonding resistance, R is fixed to 0 Ohm at "low frequencies", while its value equals to 3 Ohm in the W-band.

In order to validate the large-signal model of the diode, output power versus input power measurements were compared with harmonic balance simulations performed in Keysight ADS™ [19]. In Figure 9, comparisons between measurements and simulations, when a signal of 1 GHz is applied to the device, are depicted. In this graph, a reasonable global agreement between measurements and simulation results can be seen at the fundamental frequency and the second and third order harmonics. If we focus on the highest input power level, simulations tend to overestimate the first harmonic, while the second is more accurate as the power is higher. The third harmonic is well-estimated in values, but with slight differences in the slope. This could be due to several reasons: the source current mode was originally intended to simulate the nonlinear current source in DC conditions;

however, the large-signal behavior depends on the model's ability to predict harmonics, something that, in general, is difficult to guarantee as it requires a more elaborate development of the nonlinear current source model. Furthermore, the influence of nonlinear capacitance should be considered, which could require a more accurate characterization at the highest power levels.

Table 3. Extracted values of the parameters for the ZBD model.

| Parameter	Symbol	Value	Parameter	Symbol	Value
Saturation Current (A)	I_{sat}	28×10^{-6}	Parasitic Finger Capacitance (fF)	C_p	1
Ideality Factor	η	1.4	Pad-to-Pad Capacitance (fF)	C_{pp}	16
$\alpha = \frac{q}{\eta kT}$ (1/V)	α	28.6	Bonding Inductance (pH)	L_1	73
Junction Capacitance ($V_d = 0$ V) (fF)	C_{j0}	10	Bonding Inductance (pH)	L_2	42
Series Resistance (Ω)	R_s	6.5	Pad Capacitance (fF)	C_1	88
Junction Potential (V)	ϕ_{bi}	0.16	Pad Capacitance (fF)	C_2	51
Finger Inductance (pH)	L_f	50	Bonding Resistance (Ω)	R	0 (Low Frequency) 3 (W Band)
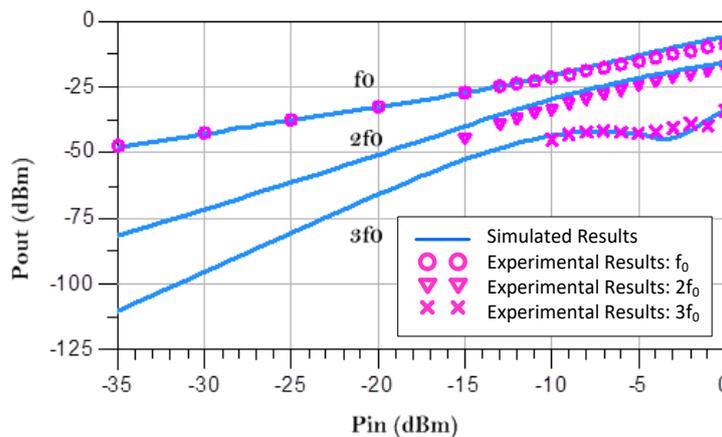
Figure 9. Simulated (continuous line) and measured output power versus input power. (Circles: f_0, Inverted Triangle: $2f_0$, Cross: $3f_0$).

3. Diode Modelling Oriented to Flip-Chip Attachment Technique

The previous model is a basic general-purpose model, but particularly considering W-band applications, it was necessary to achieve a better approximation for the most commonly used attachment technique of the ZBD to the circuit assembly, while being well-based on the previously presented model extraction. Therefore, a new circuit was assembled by attaching a ZBD using the flip-chip technique, as shown in Figure 10. This attachment technique is the most critical in terms of the location of the diode, in order to achieve a symmetrical structure and to avoid destroying the finger of the diode by placing it in contact with the CPW-M transition. Please note that, to attach the flip-chip into a circuit, the chip must be inverted to bring the solder dots (made of H20E silver epoxy) down onto the connectors on the circuit board; then, the solder is re-melted (120 °C for 15 min) to produce an electrical connection, leaving a small space between the diode and the underlying mounting.
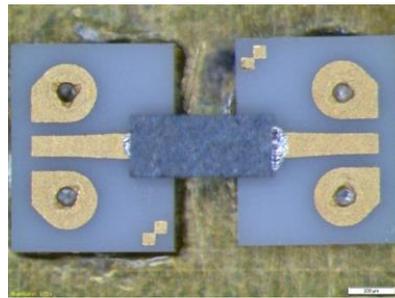
Figure 10. Photo of the ZBD in the flip-chip assembly.

As performed for the previously presented modeling procedure, CPW-M transitions were used, and their model was used in the optimization in Keysight ADS^{TM}, in order to obtain an equivalent circuit model consisting only of the intrinsic and parasitic elements of the diode. A comparison between experimental measurements and the model (described below) simulation results is shown in Figure 11, showing a better match at the lower frequencies of the W-band.
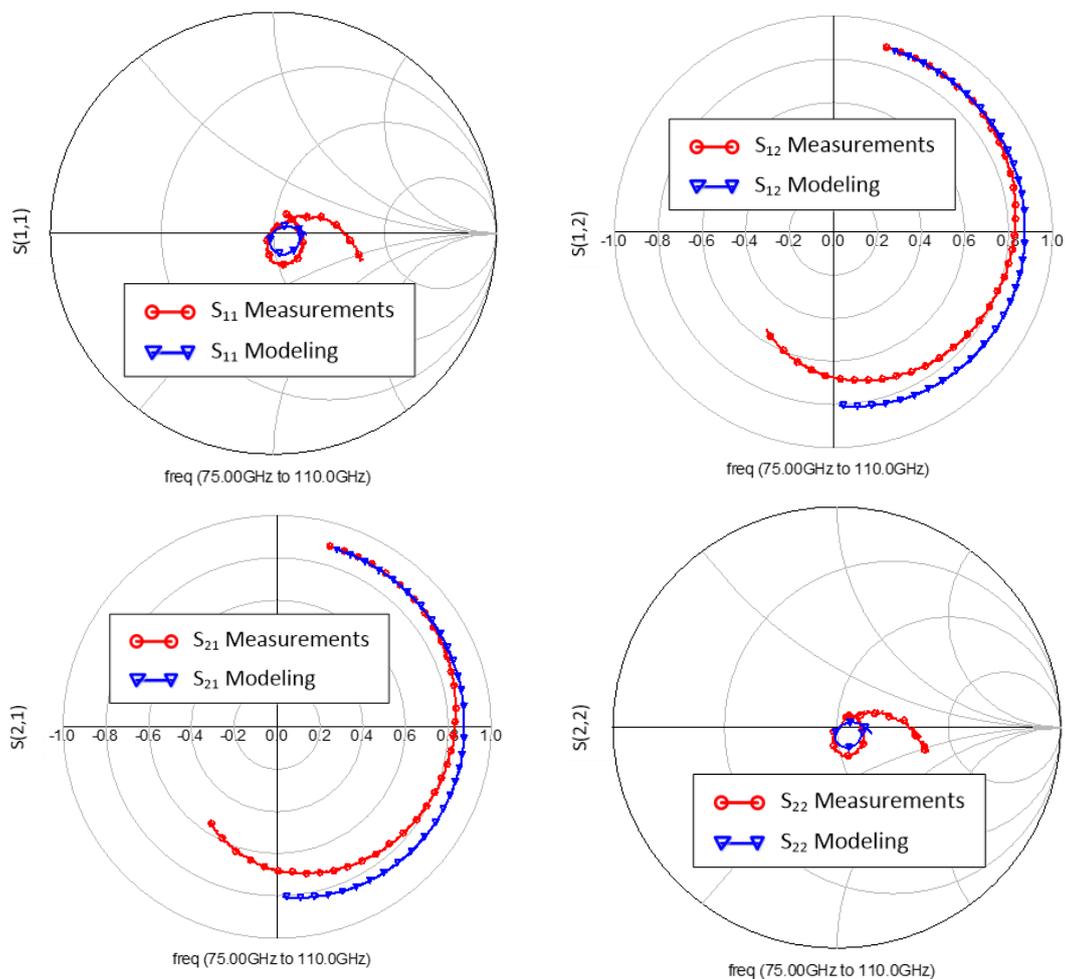

Figure 11. Comparison between S-parameter measurements and modeling simulation of the unbiased ZBD (0 V) for the flip-chip assembly in the W-band.

Flip-Chip Zero Bias Diode Complete Model

The resulting equivalent circuit model is presented in Figure 12. Comparing this equivalent circuit with the previous model (Figure 8), the main difference is that some capacitances have been added to account for some newly existing parasitic effects. In the flip-chip assembly, the diode was attached

to the carrier upside down, compared to the conventional mode with bonding wires. Therefore, capacitances C_2 in Figure 8 are identified in Figure 12 as C_{PAD1} and C_{PAD2}, being connected to a new capacitance, C_{GNDs}, which represents a new, slightly capacitive coupling effect between the microstrip reference plane of the diode bulk and the ground plane of the total circuit assembly. An additional capacitive coupling effect is thus originated, $C_{COUPLING}$, which is related to the capacitive coupling between the CPW-M transitions since, in this assembly, both transitions are placed closer than in the previous one. The L_{IN}-C_{IN}-R_{IN} and R_{OUT}-C_{OUT}-L_{OUT} electrical networks simulate the microstrip line effect at the connection between the diode and the CPW-M transition; besides, R_{IN} and R_{OUT} also include the losses related to the H20E conductive silver epoxy used to attach the diode. It should be emphasized that fitting in Figure 7 covers the range from 2 to 110 GHz, de-embedding the effect of the wire bonding, while Figure 11 covers a frequency range from 75 to 110 GHz, comparing measurements and simulations without de-embedding. The upside-down positioning of the diode causes some uncertainty in the parasitic capacitances with the ground, but at the same time, other parasitic elements must be maintained for coherence with grounded-microstrip ZBD model (Figure 8). Those restrictions limit the capability for a perfect impedance matching.
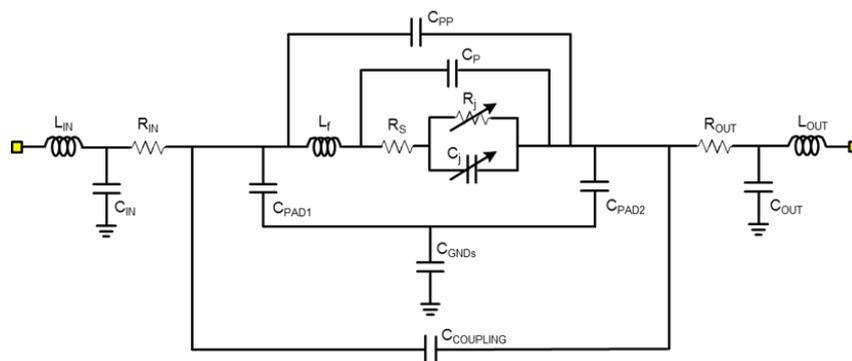

Figure 12. Equivalent circuit model for the ZBD in flip-chip assembly.

The resulting model parameters extracted for this second diode assembly technique are listed in Table 4.

Table 4. Results of the parameter extraction of the total capacitance of ZBD.

Parameter	Symbol	Value
Saturation Current (A)	I_{sat}	28×10^{-6}
Ideality Factor	η	1.4
$q/\eta kT$ (1/V)	α	28.6
Junction Capacitance ($V_d = 0$ V) (fF)	C_{j0}	10
Series Resistance (Ω)	R_S	6.5
Junction Potential (V)	ϕ_{bi}	0.16
Finger Inductance (pH)	L_f	50
Parasitic Capacitance (fF)	C_P	1
Pad-to-Pad Capacitance (fF)	C_{PP}	16
Input Inductance (pH)	L_{IN}	59
Output Inductance (pH)	L_{OUT}	48
Input Capacitance (fF)	C_{IN}	3.4
Output Capacitance (fF)	C_{OUT}	0.3
Input Resistance (Ω)	R_{IN}	2.3
Output Resistance (Ω)	R_{OUT}	2.3
Coupling Capacitance (fF)	$C_{COUPLING}$	18
PAD IN Capacitance (fF)	C_{PAD1}	39
PAD OUT Capacitance (fF)	C_{PAD2}	203
Ground Capacitance (fF)	C_{GNDs}	11

4. Including Low-Frequency Noise in the Zero-Bias Model

For a complete evaluation of diode performance, which is of significant use in detectors, a knowledge of low-frequency noise behavior becomes quite relevant—not only as proof of technology quality, but also to establish the noise floor, which limits the dynamic range. Thus, this ensures a stable response in a dynamic mode of operation. In this sense, a set-up was developed to measure and model low-frequency noise sources present in the ZBD, following [9]. The set-up diagram is shown in Figure 13, and the corresponding photo is shown in Figure 14. In this case, the diode was mounted in the conventional way (grounded, not Flip-Chip) inside a shielded box to avoid unwanted interference in the measurements. In this low-frequency range, a distinction between the flip-chip and wire bonding is not relevant.
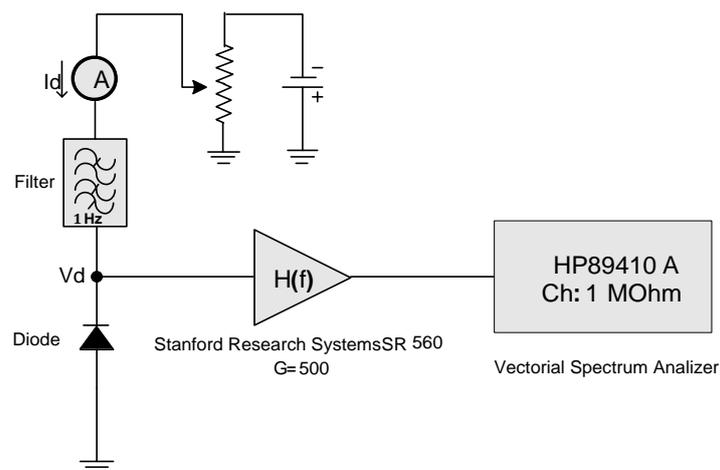

Figure 13. Setup to evaluate low-frequency noise under different DC biases.
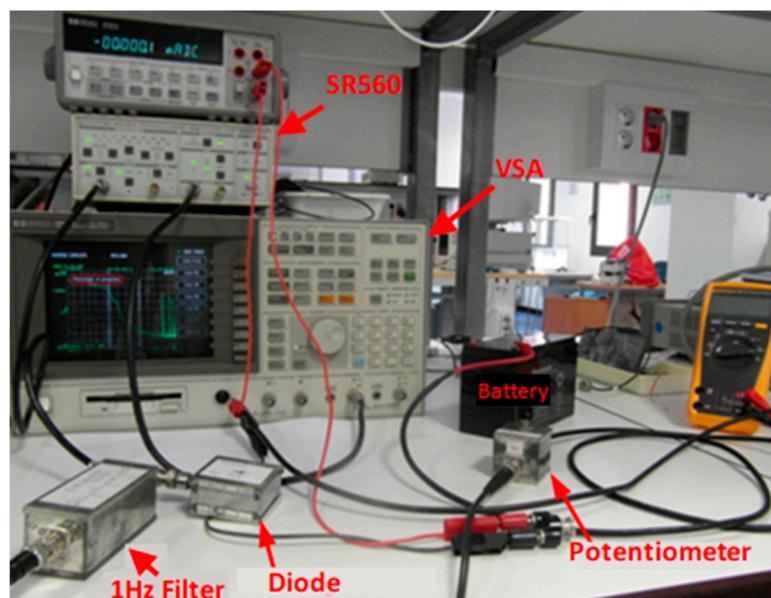

Figure 14. Photo of the measurement setup for low-frequency noise, corresponding to the diagram in Figure 13.

The main low-frequency noise contributions expected in the current spectral density (CSD) were: thermal noise associated with the series resistance R_s, shot noise, and flicker noise. The equations governing the different noise sources are given in Equations (3)–(5) (where K is the Boltzmann constant, f is the low frequency, q is electron charge, I_s is the saturation current, and I_{diode} is the actual current,

whereas K_f, a_f, and b_f are parameters to be determined). Noise sources were placed in the circuital model of the diode, as shown in Figure 15.

$$\langle CSD_{thermal} \rangle = \overline{i^2_{nR_s}} = \frac{4KT}{R_s} \tag{3}$$

$$\langle CSD_{shot} \rangle = \overline{i^2_{nshot}} = 2q(I_{diode} + 2I_s) \tag{4}$$

$$\langle CSD_{flicker} \rangle = \overline{i^2_{n_{1/f}}} = k_f \frac{I^{a_f}}{f^{b_f}} \tag{5}$$
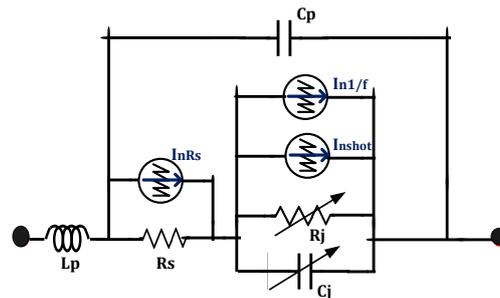

Figure 15. Insertion of noise sources in the diode model.

The low-frequency noise spectrum measured with the set-up in Figures 13 and 14 is shown in Figure 16, including the system noise floor (NF trace) and measurements for the four different current bias points: 0.05 mA, 0.1 mA, 0.15 mA, and 0.2 mA. The set-up was also simulated considering all the noise contributions and Flicker noise parameters in Equation (5), which were optimized to fit with the measurements at these four bias currents. In Table 5, the optimized parameters are listed.
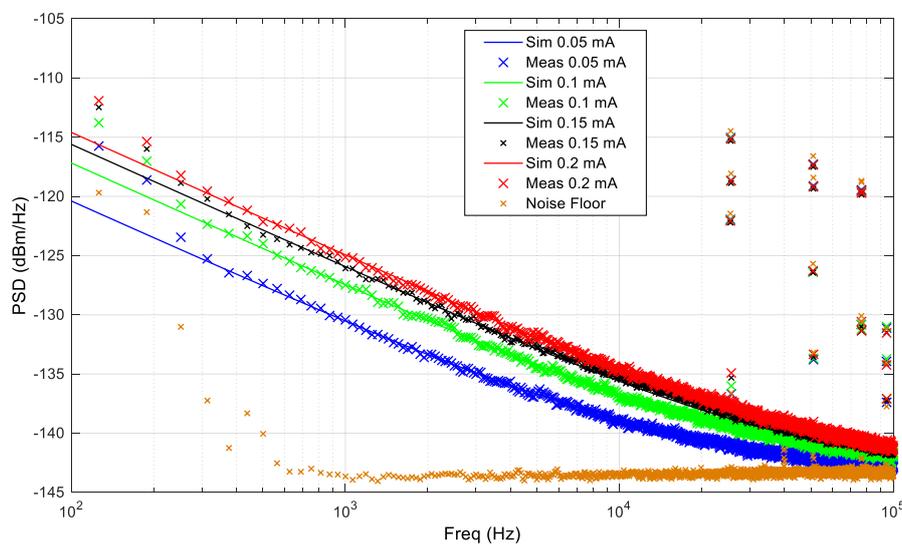

Figure 16. Low-frequency noise spectrum measurements of the set-up, shown in Figure 13, and simulations using the model in Figure 15.

Table 5. Low-frequency noise parameters.

Parameter	Value
k_f	1.08×10^{-7}
a_f	2.48
b_f	1.04

5. Conclusions

In this paper, two models for Zero-Biased Diodes (VDI) considering wire-bonded or flip-chip techniques have been presented, with particular emphasis on the flip-chip model in the W-band. Equivalent circuit models were complemented with the extraction of low-frequency noise sources (Flicker) and its incorporation in the proposed models, allowing for a more complete prediction of the response of the diodes, for example, in detectors. The obtained models were validated under different operating conditions, and power prediction abilities of the model were probed performing nonlinear harmonic measurements ranging the appropriate power levels, in comparison with harmonic balance simulations in commercial software (Keysight ADS™).

Comparisons up to the W-band between measured and simulated scattering parameters using the complete model and showing a good agreement were performed, probing the validity of the extraction methods applied using both wire bonding and flip-chip attachment techniques.

Finally, low-frequency noise measurements and simulations were performed to validate the noise model added to the previously extracted diode model, which showed an adequate level of agreement.

As a general remark in "normal" operations, Zero Bias diodes are expected to be self-biased by the input RF power, as it happens in the measurements shown in Figure 9, where input power was swept. In Figure 3, ZBD diodes were biased for DC fitting, and scattering parameters were also measured in low microwave frequencies under a DC bias to fit the capacitance model (Figures 5 and 6). For low-frequency noise measurements also, the DC bias was applied to put into the evidence bias dependence of the Flicker noise parameters. We considered that those measurements would cover the usual scenarios for ZBD operations. A combined application of W-band power and DC bias to the Zero Bias diodes was avoided, keeping in mind the fragility of the diode because of its low-threshold voltage, where voltages applied any higher than the safe one would totally or partially damage it, leading to unreal measurements of the device's high-frequency behavior.

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