A Low Phase Noise All-Digital Programmable DLL-Based Clock Generator

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Abstract—**This paper proposes a low phase noise all-digital programmable DLL-based clock generator. The proposed clock generator is fabricated in a 0.18 µm standard CMOS process with a 1.8 V supply voltage. The proposed digital programmable DLL-based clock generator is easy migration over different processes and low power dissipation. The measurement results show that the input and output frequency ranges can operate 100 MHz ~ 600 MHz and 100 MHz ~ 1.2 GHz, respectively. At 800 MHz, the phase noise is -112.36 dBc @ 1MHz offset frequency. The total power consumption of the clock generator is 23.87 mW, and the active die area of the clock generator is 0.14 mm^2.**

Keywords*—*Delay-Lock Loop (DLL); digital control delay line; multiphase; frequency multiplier; clock generator

I. INTRODUCTION

In recent years, there have been increasing demands on clock generators capable of providing multiple-frequency clock signals in a wide frequency band for high-speed microprocessors, clock/data recovery (CDR) and mobile communication systems. Delay-locked loop (DLL)-based clock generators present strong advantages over conventional phase locked loop (PLL)-based approaches: better phase noise performance, robustness under robustness under process, voltage and temperature (PVT) variations, are easier to design, and fast settling times, and occupy smaller area due to a simpler loop filter.

However, in conventional analog DLL-based clock generators, the power consumption of the frequency multiplier is large as compared to the other blocks. Besides, conventional analog DLL-based clock generator uses capacitors to form low-pass filter which would occupy large chip area. Conversely, the digital DLL-based clock generator is easy migration over different processes and low power dissipation. Therefore, the all-digital DLL-based clock generator will become more important in the future [1]-[4].

In this paper, an all-digital low phase noise programmable DLL-based clock generator is proposed. To resolve the power consumption and large chip area in conventional analog DLL-based clock generator, it consists of digital control delay line, pulse generator, multiplier selector, and edge combiner. Moreover, clock generator can programmable by external bits to produce ×1 ~ ×8 of the reference frequency, operating over the widest frequency range among the various programmable frequency multipliers. Since the proposed clock generator occupies a small area and low power dissipation, it is quite attractive for system-on-a-chip (SoC) applications with dynamic frequency scaling.

This paper is arranged as follows. Section II briefly overview the architecture of proposed all-digital low phase noise programmable DLL-based clock generator. Circuit description is presented in Section III. In Section IV, experimental result, chip micrograph, and performance comparison are presented. Finally, Conclusions are presented in Section V.

II. OVERALL ARCHITECTURE

The architecture of the proposed all-digital programmable DLL-based clock generator is shown in Fig. 1. It consists of DLL core and frequency multiplier. The DLL core consists of an initial circuit, coarse tune loop, fine tune loop, and digital- controlled delay line (DCDL). The course tune is composed of phase comparator (PC) and successive approximation register (SAR) [6]-[8]. And fine tune is composed of phase detector (PD) [9] and up/down counter [12] [13]. Frequency multiplier comprises multiplier selector, pulse generator and edge combiner.

The reference signals (Ref_clk) inject the reference clock to initial circuit, phase detector and digital control delay line to make a start signal that initial SAR and up/down counter at the mid to avoid harmonic locking, stuck locking. At the same time, sixteen uniform phases will be produced by digital control delay line. It can choose different feedback signals (Int_clk) to produce several multiplier by controlling the external input signal.

After the Int_clk has been chosen, feedback signal is compared with the Ref_clk by PC. If the Ref_clk is in the lead, the Comp signal will be high. In contrast, if the Ref_clk fall behind with the Int_clk, the Comp signal will be low. The Comp signal make SAR to control the delay time of the

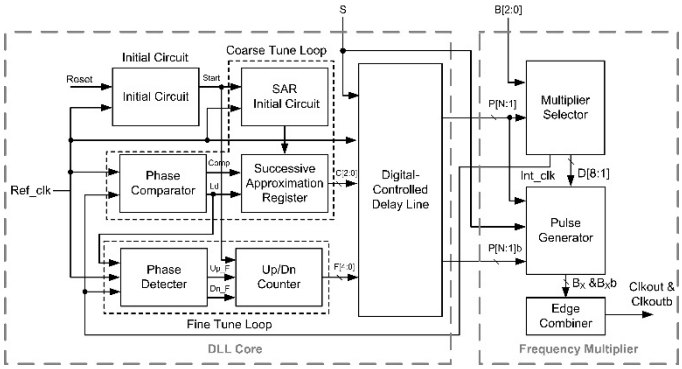

Fig. 1. The architecture of the proposed all-digital programmable DLL-based clock generator.

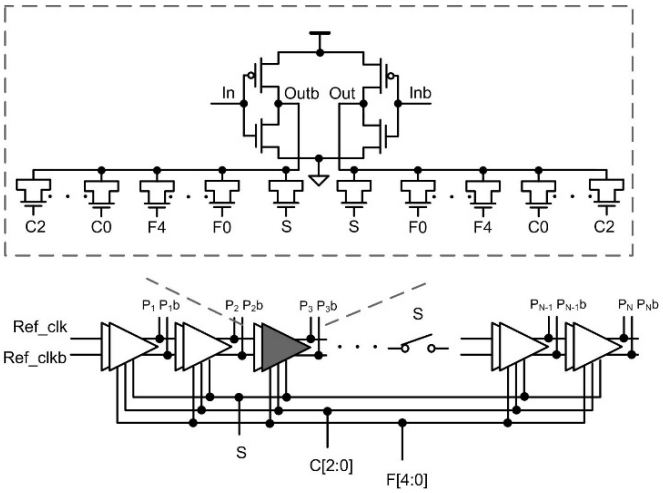

Fig. 2. The architecture of digital-controlled delay line.

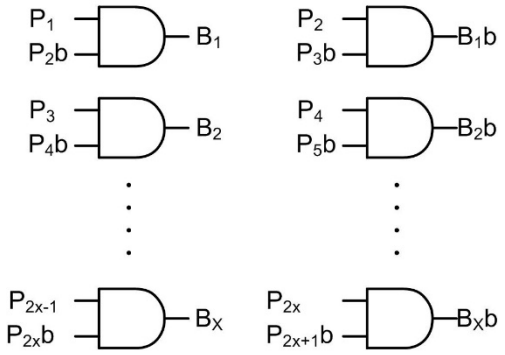

Fig. 3. The architecture of pulse generator.

delay loop until the PC can't distinguish whether the Int_clk lead or lag. At the moment course tune is locking that lock signal (LD) is high. After the PC is locking, the fine tune phase detector (PD) starts working. The fine tune PD distinguish whether the Int_clk lead or lag to the Ref_clk and generating up/dn signals to control up/down counter to adjust the delay time of delay loop. When the phase difference of the Ref_clk and Int_clk is within the dead zone of the PD, then the PD will stop counting.

III. Circuit Description

A. Digital-Controlled Delay Line (DCDL)

The adopted delay cell is shown in Fig. 2. DCDL consists of differential delay cells. Every delay cell is made up of two identically delay elements. It produces different delay to make sixteen phase output.

The digital-controlled delay line comprise 8-bit delay element. Three-bit C[2:0] is from the course loop that control by binary weight to achieve wide delay range. And the five-bit F[0:4] is from fine loop that control by thermal code. It provides high resolution delay time to reduce static phase error.

B. Pulse Generator

The architecture of pulse generator is shown in Fig. 3. It's made up of AND gate which generated various clocks. The clocks P1 and P2b use AND operation in pulse generator to made B1 pulse. Likewise, the clocks P2 and P3b use AND operation in pulse generator to made B1b pulse and so on. The following is function of pulse generator:

$$Bx = P_{2X-1} \cdot P_{2X}b$$

$$Bxb = P_{2X} \cdot P_{2X+1}b \quad \text{where } x = 1 \sim 8$$

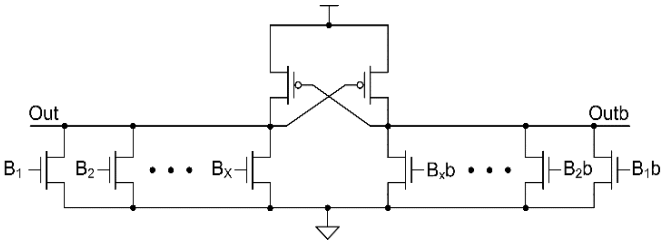

Fig.4. The architecture of edge combiner.

Table I: The truth table of pulse generator

B2	B1	B0	Int_clk	Multiplier
0	0	0	P2	X1
0	0	1	P4	X2
0	1	0	P6	X3
0	1	1	P8	X4
1	0	0	P10	X5
1	0	1	P12	X6
1	1	0	P14	X7
1	1	1	P16	X8

Table II: The truth table of edge combiner

B_x	B_xb	Out	Outb
1	0	0	1
0	1	1	0

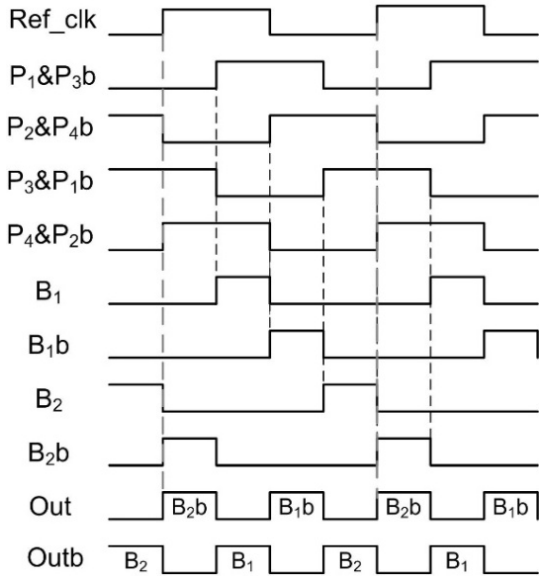

Fig. 5. The timing diagram of 2× reference frequency.

C. Multiplier Selector and Edge Combiner

The multiplier selector use three external bits to control pulse generator what it contribute different clocks. The truth

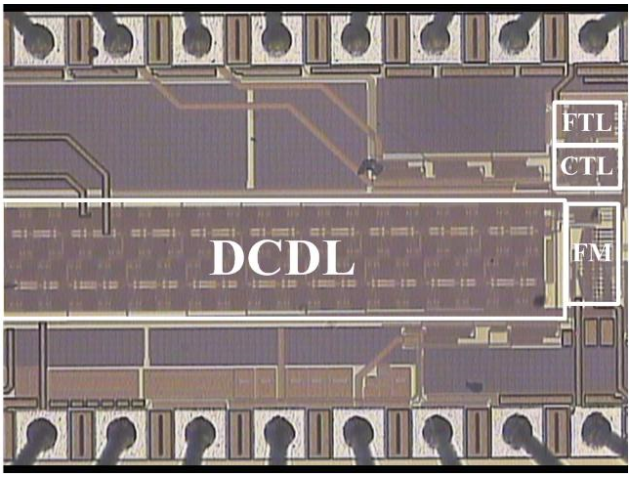

Fig. 6. The chip micrograph of the proposed clock generator.

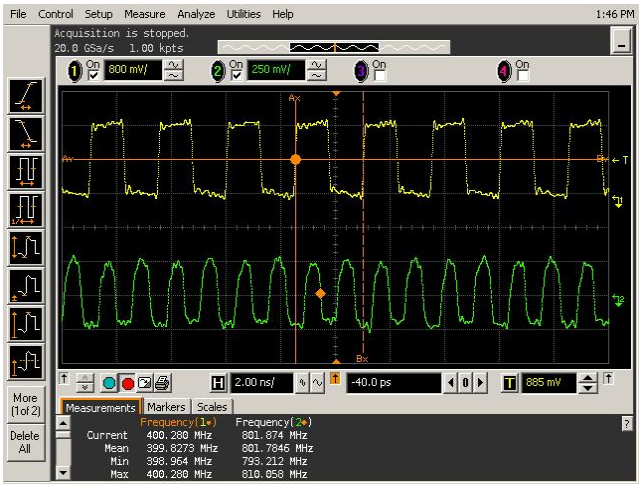

Fig. 7. 800 MHz for 2× reference frequency.

table is shown in table I. The architecture of edge combiner is shown in Fig. 4. When the Bx is high then the Bxb will be low. On the other hand, when the Bx is low then the Bxb will be low. The truth table of edge combiner is shown in Table II. After the edge combiner completes the synthesis procedure, the out signals Out and Outb will be produce. Following is the function of edge combiner:

$$Out = \overline{B1 + B2 + \cdots Bx}$$

$$Outb = \overline{B1b + B2b + \cdots Bxb} \quad \text{where } x = 1 \sim 8$$

The timing diagram of 2× reference frequency is shown in Fig. 5. When the B[2:0] is "001", the P1 and P3b, P2 and P4b, P3 and P1b, P4 and P2b also have same output clock. Finally, the B1, B1b, B2, B2b will be operated by edge combiner to output clock 2× what the reference clock is input.

IV. Experiment Result

The proposed low phase noise all-digital programmable DLL-based clock generator was fabricated in a 0.18-μm CMOS process with a 1.8 V supply voltage. Fig. 6 shows the chip micrograph of the proposed clock generator. The active die area of the chip is 0.14 mm^2. The frequency multiplier generates 2×, 3× 5×, 8× of reference clock, as shown in Fig. 7, Fig. 8, Fig. 9 and Fig. 10, respectively. The spectrum of the clock generator is shown in Fig. 11. The phase noise is -112.36 dBc@1 MHz offset frequency, as shown in Fig. 12. The comparison between the proposed clock generator and previous work is displayed in Table III. The proposed clock generator can provide an odd multiplication factor of up to 8. Moreover, the proposed clock generator has better performance in phase noise.

Fig. 8. 1.2 GHz for 3× reference frequency.

Fig. 9. 1 GHz for 5× reference frequency.

Fig. 10. 1.2 GHz for 8× reference frequency.

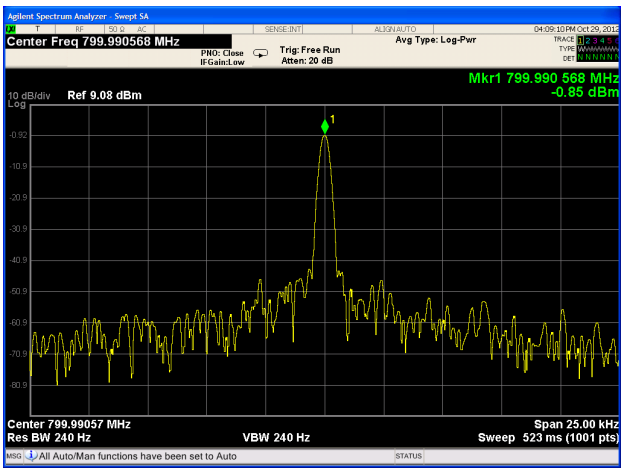

Fig. 11. Measured output spectrum of the proposed clock generator.

Fig. 12. Measured phase noise plot.

V. Conclusion

The low phase noise all-digital programmable DLL-based clock generator is proposed that can be applied to microchip, clock data recovery, mobility communication system and SoC. The proposed clock generator can produce ×1~×8 clock what it provides several clocks to different system. The chip is fabricated in a 0.18 µm standard CMOS process with a 1.8 V supply voltage. The active die area of the chip is 0.14mm^2. The proposed clock generator can operate with input clock range is 100 MHz ~ 600 MHz and the output range is 100 MHz ~ 1.2 GHz. The phase noise is -112.36 dBc @ 1MHz offset frequency.

Acknowledgment

This work was supported by the National Science Council (NSC), Taiwan. The authors would also like to thank the National Chip Implementation Center (CIC) of Taiwan for chip fabrication and equipment services.

Table III: Performance comparison with prior works

	[1]	[2]	**This work**
Process	0.18-µm	0.25-µm	**0.18-µm**
Supply Voltage	1.8 V	2.5 V	**1.8 V**
Programmability	×4, ×8, ×12, ×24	No	**×1~×8**
Output Range	30 MHz ~ 2.16 GHz	120 MHz ~ 1.2 GHz	**100 MHz ~ 1.2 GHz**
Phase Noise	-82.6 dBc @ 1 KHz -87.7 dBc @ 10 KHz -99.8 dBc @ 100 KHz	-88 dBc @ 10 KHz	**-73.95 dBc @ 1KHz -89.83 dBc @ 10KHz -108.26 dBc @100 KHz -112.36 dBc @ 1MHz**
Power Consumption	16.2 mW @ 2.16 GHz	52.5 mW @ 1.2 GHz	**23.87 mW@ 800 MHz**
Active Area	0.051 mm^2	0.13 mm^2	**0.14 mm^2**

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