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A Robust Oscillator for Embedded System without External Crystal

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Abstract: The robust voltage-controlled oscillator is presented by using the constant current reference and the ring oscillator for the embedded system application. The constant current reference generates the constant current for the succeeding ring oscillator to produce a stable 4MHz oscillation frequency. The proposed VCO circuit was fabricated in a 0.35 μm CMOS technology and worked with a supply voltage of 3.3 V. The chip area of the VCO was 150 $\mu m \times 130\ \mu m$. According to measured results, the oscillation frequency drift of the proposed VCO was 986 ppm/°C over a temperature range of -25°C to 100°C. The phase noise of -62.29 dBc/Hz was obtained at 1 MHz offset from the carrier. Moreover, total current consumption of the entire VCO was 234.72 μA. Therefore, the proposed VCO is suitable for integration into the embedded system.

Keywords: Constant current reference, Voltage-Controlled Oscillator, Ring Oscillator

1 Introduction

In modern portable and consumer electronic devices, the embedded system is used to control data transmission between multimedia, memory, and I/O. As shown in Fig. 1(a), an external crystal oscillator provides the embedded system with a clock signal for data acquisition [1]. This study integrated a voltage-controlled oscillator (VCO) into the embedded system to reduce component count and cost, as shown in Fig. 1(b). However, the challenge in implementing on-chip clock source is to achieve high frequency stability and accuracy over environmental alterations, such as process, voltage, and temperature (PVT) variations. Fig. 2 shows traditional voltage-controlled oscillator. It is composed of a current reference and a ring oscillator. In the current reference part, the reference current I is generated by an analog voltage signal, V_{ctrl}. Subsequently, the oscillation frequency (F_{OSC}) of the VCO varies with the reference current I.

The current reference is an essential basic block of several analog circuits, such as the bias sources for oscillators, amplifiers, and phase-locked loops (PLL). For these applications, the current references must have high immunity against supply voltage and temperature variations. Therefore, the bandgap circuit is commonly used to generate a voltage reference or a current reference that can be derived from voltage references by applying Ohm's law for voltage to current conversion [2][3]. In general, the voltage reference of the bandgap circuit is generated by on-chip resistors, bipolar junction transistors (BJTs), and an operational amplifier. However, BJTs and an operational amplifier cause large silicon area penalty. In [4][5], a temperature-compensated technique is provided to generate a stable reference current of the bandgap circuit. Cascade NMOS transistors are used in [4][5] instead of on-chip resistors. Therefore, the area overhead and supply voltage cannot be reduced. The proportional to absolute temperature (PTAT) like technique was used to generate a reference current under a low supply voltage [6]. Moreover, the on-chip resistor was replaced by an NMOS transistor working in the triode region. Therefore, it can work with a power supply voltage as low as 1.2 V.

However, this current reference is proportional to $T^{0.5}$, and is strongly dependent on the supply voltage. This paper proposes a robust voltage-controlled oscillator for the embedded system. The proposed voltage-controlled oscillator has two main advantages, as follows: (1) the new constant current reference is provided for the oscillator; and (2) the chip area is effectively reduced by using only CMOS transistors. The remainder of this paper

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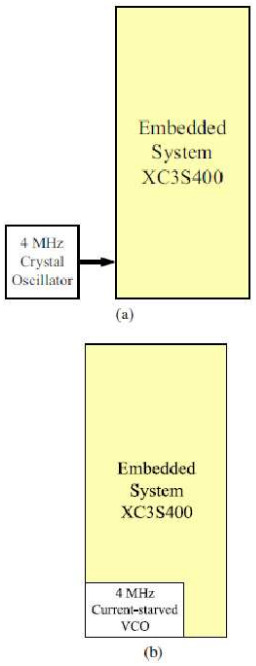


(a)

Fig. 1: (a) Embedded system with external crystal (b) Embedded system without external crystal

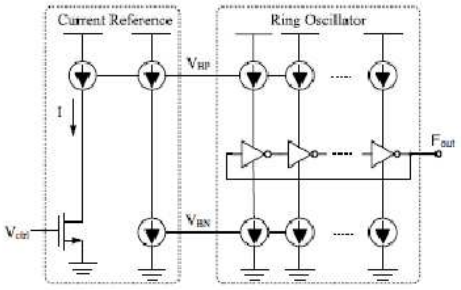
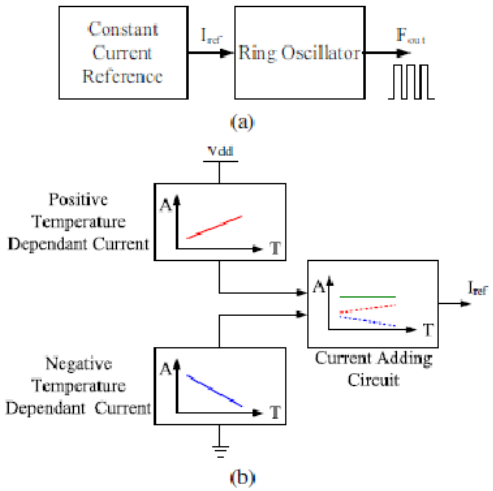


Fig. 2: The traditional voltage-controlled oscillator

is organized as follows: Section 2 introduces the circuit structure and operation principle of the proposed VCO; the simulation and experimental results are shown in Section 3; and finally, conclusions are offered in Section 4.

2 Circuit Description and Analysis

Fig. 3(a) shows the design concept of the proposed VCO. It is composed of the constant current reference and the ring oscillator. The constant current reference generates



(a)

Fig. 3: (a) The proposed voltage-controlled oscillator architecture (b) The design concept of constant current reference

the constant current I_{ref} to the succeeding ring oscillator. The output oscillation frequency (F_{out}) of the proposed VCO is generated according to I_{ref}. The design concept of constant current reference is shown in Fig. 3(b). The circuit generates positive and negative temperature dependent currents and combines two currents to produce a reference current I_{ref} with a zero temperature coefficient. The detailed circuit structures and operating principles of two parts are discussed in the following paragraphs.

2.1 Constant Current Reference circuit

As shown in Fig. 4, the circuit generates positive temperature dependent current (PTDC) and negative temperature dependent current (NTDC) and combines two currents to generate a reference current I_{ref} with a zero temperature coefficient.

2.1.1 Positive Temperature Dependent Current (PTDC) Circuit

The positive temperature dependent current circuit is shown in Fig. 5. According to [7], the positive temperature coefficient current I_{C1} is generated by a constant-Gm biasing circuit. The formula of I_{C1} can be briefly represented as:

$$I_{C1} \propto \frac{1}{\mu_n * R^2} \quad (1)$$

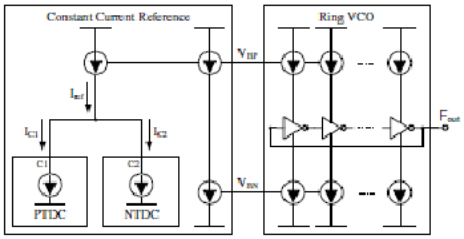


Fig. 4: The design concept of the proposed voltage-controlled oscillator

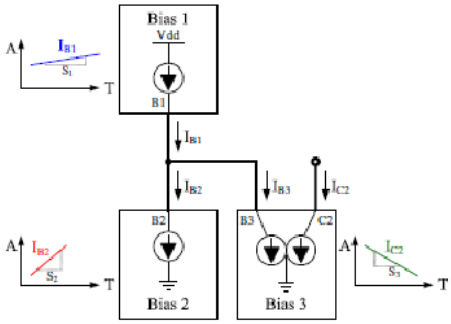


Fig. 6: The negative temperature dependent current circuit architecture

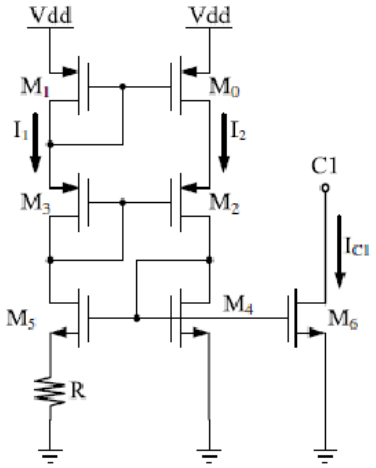


Fig. 5: The positive temperature dependent current circuit architecture

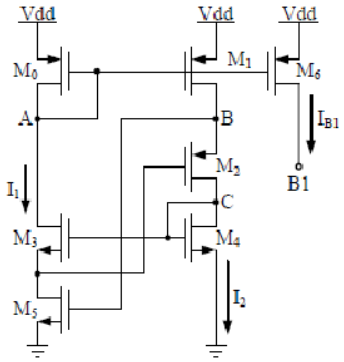


Fig. 7: The Bias 1 circuit architecture of negative temperature dependent current circuit

where μ_n and R are NMOS mobility and bias resistor, respectively. Because the μ_n is proportional to temperature ($T^{-2.2}$), the current reference I_{C1} has positive temperature coefficient characteristic. Moreover, this current can be set by adjusting resistor R.

2.1.2 Negative Temperature Dependent Current (NTDC) Circuit

As shown in Fig. 6, the NTDC circuit is composed of three bias current circuits with various types of current-to-temperature slope ratio. The output current slope ratios of Bias 1 and Bias 2 are S_1 and S_2, respectively. Although both have positive temperature coefficient characteristics, the slope ratios of S_1 are smaller than S_2. Consequently, the current I_{B3}, which is equal to subtraction of two input currents, has a negative temperature coefficient characteristic. According to the current I_{B3}, the negative temperature coefficient current I_{C2} is also generated by the Bias 3 circuit.

2.1.3 The Bias 1 circuit architecture

Fig. 7 shows the Bias 1 circuit architecture. The crucial design concept of the Bias 1 circuit is to design NMOS transistor M_5 to operate in the triode region. To enable transistor M_5 operation in the triode region, the PMOS transistor M_2 was added between PMOS transistor M_1 and NMOS transistor M_5 to provide the gate voltage of the transistor M_5. Therefore, the positive temperature dependent current I_1 can be written as:

$$\begin{aligned} I_1 &= \mu_n C_{ox}(\frac{W}{L})_5(V_{GS}-V_{TH})V_{DS} \\ &= \mu_n C_{ox}\gamma V_{DS}(\frac{W}{L})_5(V_{DD}-\frac{V_{TH}}{\gamma}) \\ &= \alpha_1(\frac{W}{L})_5(V_{DD}-\beta_1) \end{aligned} \quad (2)$$

where $V_{GS}=\gamma\times V_{DD}$, $\alpha_1=\mu_n C_{ox}\gamma V_{DS}$, $\beta_1=V_{TH}/\gamma$, and γ is the linearity relatively of the voltages of V_{GS} and V_{DD}. By adjusting $\alpha_1(W/L)_5$ ratio of the transistor M_5, the current-to-temperature slope S_1 of the current I_1 is not excessively

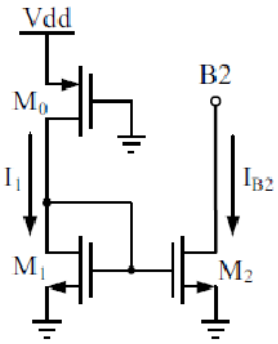


Fig. 8: The Bias 2 circuit architecture of negative temperature dependent current circuit

sharp. Therefore, the current I_{B1} of the transistor M_6 is a duplicated current of I_1.

2.1.4 The Bias 2 circuit architecture

The Bias 2 circuit architecture of negative temperature dependent current circuit is shown in Fig. 8. To generate positive temperature dependent current I_1, the PMOS transistor M_0 was designed to work in the triode region. Therefore, the current I_1 can be written as:

$$I_1 = \mu_n C_{ox}(\frac{W}{L})_1[(V_{GS}-V_{TH})V_{DS}-\frac{1}{2}V_{DS}^2]$$
$$= \alpha_2(\frac{W}{L})_1(V_{DD}-\beta_2) \quad (3)$$

where $V_{GS} = V_{DD}$, $\alpha_2 = \mu_n C_{ox} V_{DS}$, and $\beta_2 = V_{TH} + 1/2(V_{DS})$. By adjusting $\alpha_2(W/L)_1$ ratio of the transistor M_1, the current-to-temperature slope S_2 of the current I_1 can be designed more sharply. The positive temperature dependent current I_{B2} of the transistor M_2 is a duplicated current of I_1.

2.1.5 The Bias 3 circuit architecture

As shown in Fig. 9, the positive temperature dependent current I_{C2} of the transistor M_1 is a duplicated current of I_{B3}. The I_{C2} current value can be selected from an aspect ratio of $(W/L)_1/(W/L)_0$. According to PTDC circuit and NTDC circuit, the circuit architecture of the constant current reference is shown in Fig. 10. The reference current I_{ref} of the constant current reference is generated by combining current I_{C1} of the PTDC and I_{C2} of the NTDC. Therefore, reference current I_{ref} is insensitive to temperature and supply voltage variations.

2.2 Ring Oscillator

Fig. 11 shows the ring oscillator of the proposed VCO. The ring oscillator is composed of a chain of an odd

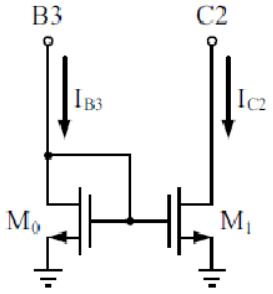


Fig. 9: The Bias 3 circuit architecture of negative temperature dependent current circuit

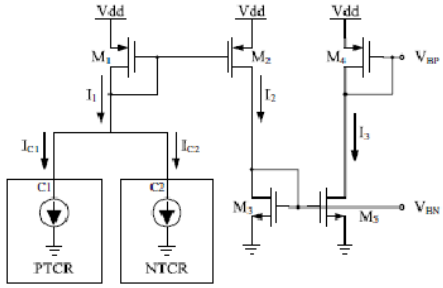


Fig. 10: The circuit architecture of the constant current reference

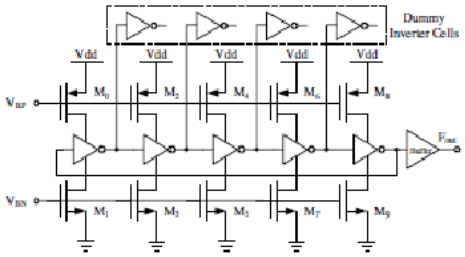


Fig. 11: The ring oscillator of the proposed VCO

number of inverters, which is feedback to the input to cause oscillation. The output frequency of oscillation depends on the delay of each inverter, which is determined by the parasitical capacitance of each successive inverter, maximal peak-to-peak voltage, and the bias current. The output frequency of oscillation can be represented as:

$$F_{out} \approx \frac{1}{V_{pp} * C_{para}} \quad (4)$$

where V_{pp}, C_{para} and I are maximal peak-to-peak voltage, parasitical capacitance, and bias current, respectively. According to (4), the oscillation frequency is proportional

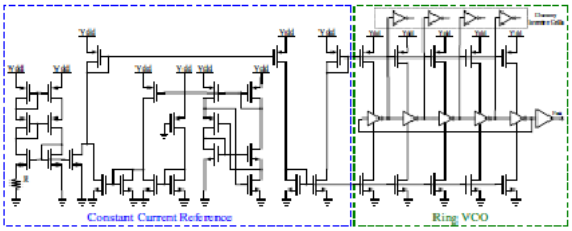


Fig. 12: The circuit architecture of the proposed VCO

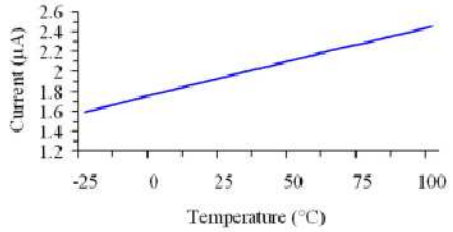


Fig. 13: The simulation results of I_{c1} with temperature drifts

to bias current. Therefore, a constant oscillation frequency can be achieved by providing a constant bias current. Moreover, dummy inverter cells were added to reduce output mismatch of each inverter.

2.3 The Proposed Voltage-Controlled Oscillator

The circuit architecture of the proposed VCO is shown in Fig. 12. The constant oscillation frequency F_{out} was achieved by combining the constant current reference and the ring oscillator. The proposed VCO circuit does not cause any silicon area penalty.

3 Simulation and Experimental Results

The Hspice simulation results are based on the device parameters of a TSMC 0.35 μm 3.3 V CMOS process. As shown in Fig. 13, the current I_{C1} of the PTDC circuit is positive and proportional to absolute temperature. Simulation results of the current I_{C2} with temperature drifts is shown in Fig. 14. Consequently, the current I_{C2} of the PTDC circuit is negative and proportional to absolute temperature. As shown in Fig. 15, the reference current I_{ref} was produced by combining current I_{C1} of the PTDC and I_{C2} of the NTDC. According to the simulation result, the current I_{ref} experienced a drift of 3%. Therefore, reference current I_{ref} of the constant current reference is almost insensitive to temperature drift. Fig. 16 and Fig. 17

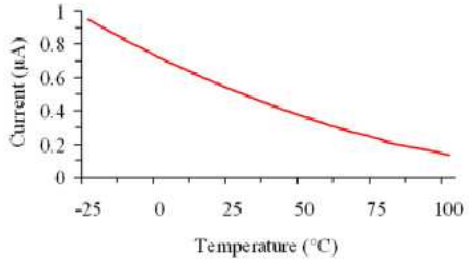


Fig. 14: The simulation results of I_{c2} with temperature drifts

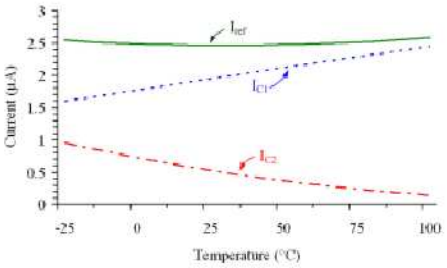


Fig. 15: Variation of the constant current I_{ref}, I_{c1} and I_{c2} with temperature drifts

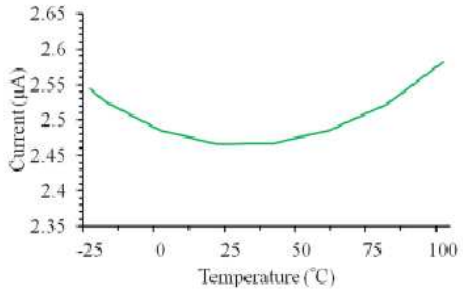


Fig. 16: Variation of the constant current I_{ref} with temperature drifts

shows the simulation result of oscillation frequency of the proposed VCO with temperature drifts. Consequently, the oscillation frequency of the proposed VCO was insensitive to temperature with a variation of 400 ppm/°C over a temperature range of -25°C to 100°C. The proposed VCO circuit was fabricated in a TSMC 0.35 μm CMOS process. The die photo of the proposed VCO chip is shown in Fig. 18. The area of the CCO circuit is 150 $\mu m \times 130\ \mu m$. Fig. 19 shows the measured waveform of the proposed VCO. The oscillation frequency of F_{out} was approximately 4 MHz. The variation of the output frequency with temperature drifts is shown in Fig. 20.

Table 1: Performance comparisons with previous works

Parameters	[8]	[9]	[10]	[11]	[12]	This work
Process (μm)	0.25	0.35	0.25	0.28	0.5	0.35
Frequency (Hz)	800M	80k	7M	2.4G	12.8M	4M
Supply Voltage (V)	2.5	1	2.5	2.5	3	3.3
Consume current (μA)	7580	1.14	600	7680	133	234.72
Temperature (°C)	-20∼100	0∼80	-40∼125	-40∼120	-40∼125	-25∼100
Temperature coefficient (ppm/°C)	360000	842	90.9	73	3030	986
Phase noise @ 1MHz offset (dBC/Hz)	N/A	N/A	N/A	-96	N/A	-62.29
Area (mm^2)	N/A	0.24	1.6	0.0121	0.1848	0.02

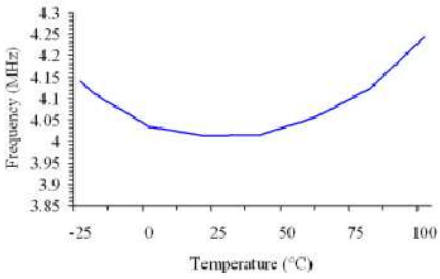


Fig. 17: Oscillation frequency of the proposed VCO with temperature drifts

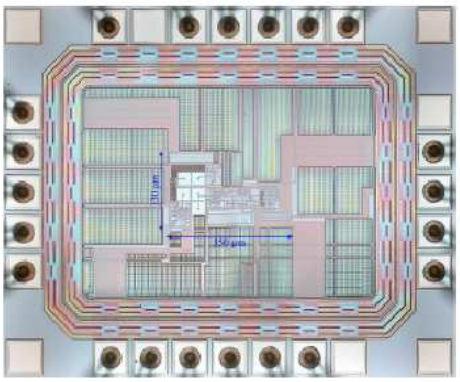


Fig. 18: The die photo of the proposed VCO chip

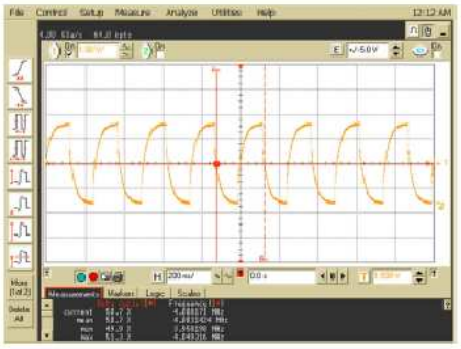


Fig. 19: The measured waveform of the proposed VCO, F_{out} =4MHz

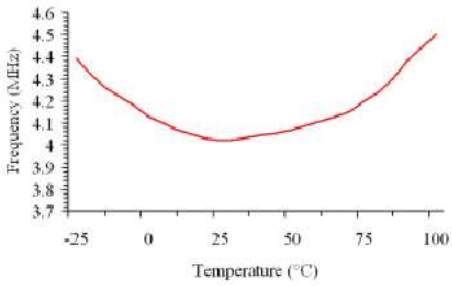


Fig. 20: Measured frequency of the proposed VCO with temperature drifts

Consequently, the oscillation frequency variation of the proposed VCO was approximately 986 ppm/°C over a temperature range of -25 °C to 100 °C. Because a number of MOS transistors worked in the triode region, the frequency variation was slightly large. However, the slight frequency variation was tolerated by using low operation frequency digital circuits. Fig. 21 shows the measured output frequency spectrum at 4 MHz. Consequently, the phase noise of -62.29 dBc/Hz was obtained at 1 MHz offset from the carrier. Table 1 shows the measurement and comparison results with previous works. According to measurement results, the proposed VCO provides stable oscillation frequency and occupies small area. Therefore, the proposed VCO is suitable for integration into the embedded system.

4 Conclusions

This paper proposes a robust VCO for the embedded system. The proposed VCO was composed of the constant current reference and the ring oscillator. The constant current reference generated the constant current for the succeeding ring oscillator to produce a stable 4

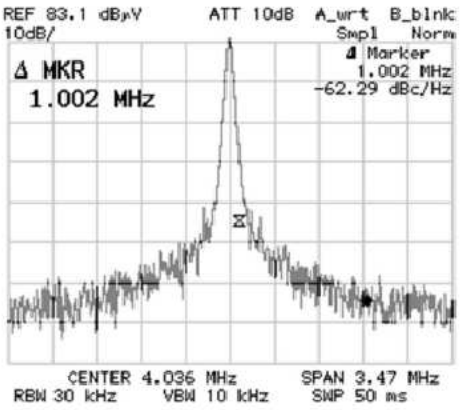


Fig. 21: Measured frequency spectrum of the proposed VCO, F_{out} = 4MHz

MHz oscillation frequency. The proposed VCO circuit was designed and fabricated in TSMC 0.35 μm CMOS process. The chip area of the VCO was 150 $\mu m \times$ 130 μm. According to measured results, the oscillation frequency variation of the proposed VCO was approximately 986 ppm/°C over a temperature range of -25°C to 100°C. The phase noise of -62.29 dBc/Hz was obtained at 1 MHz offset from the carrier. Therefore, the proposed VCO is suitable for integration into the embedded system.

Acknowledgement

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