An Ultralow Power Multirate FSK Demodulator With Digital-Assisted Calibrated Delay-Line Based Phase Shifter for High-Speed Biomedical Zero-IF Receivers

Horng-Yuan Shih, *Member, IEEE*, Chun-Fan Chen, Yu-Chuan Chang, and Yu-Wei Hu

***Abstract*— An ultralow power (ULP), multirate frequency shift keying (FSK) demodulator applied for high-speed biomedical zero-IF receivers is presented. A digital-assisted calibrated delay-line (DL) based phase shifter is used for realizing multirate and low jitter demodulation under reported highest data rate. All circuits are operated in subthreshold region for achieving ULP consumption. Moreover, the power consumption of the demodulator is relative to the data rate. Therefore, energy consumption per received bit can be optimized according to the applications. Implemented in 0.18 μm CMOS process, a minimum energy consumption of 11 pJ per received bit and demodulated peak-to-peak jitter of 1.89 ns are achieved under the maximum data rate of 40 Mb/s.**

***Index Terms*— Biomedical, demodulator, digital-assisted calibration, frequency shift keying (FSK), multirate, ultralow power (ULP), zero-IF receiver.**

I. Introduction

RECENTLY, ultralow power (ULP) and high-speed wireless transmission interface is urgently required by wearable/implantable biomedical devices. ULP receivers carrying out super-regenerative architecture for demodulating on-off keying (OOK) signals can achieve a maximum data rate of 1 Mb/s under an energy consumption of 0.5 nJ per received bit [1]–[5]. However, transmission through amplitude-based modulation scheme like OOK or amplitude shift keying (ASK) is highly sensitive to interferers. For realizing high-speed and reliable transmission between wearable/implantable biomedical devices, frequency-based modulation scheme like frequency shift keying (FSK) is considered to be used by the ULP wireless receivers in wearable/implantable biomedical devices [6].

A low-IF architecture-based conventional FSK receiver is shown in Fig. 1(a) [7]. The FSK receiver consists of a front-end circuit (an LNA and a down-conversion mixer) and a demodulator (a phase shifter and a mixer). The front-end circuit is used to convert high-speed received signals into intermediate frequency (IF) signals. The demodulator is composed of a phase shifter and a mixer. The phase shifter is designed to provide a phase shift of 90° at the IF frequency. Consequently, the phase shifter provides a phase shift more or less than 90° as the received FSK signal has frequency high (mask frequency) or low (space frequency) than the IF frequency. After mixing the received FSK signals and the phase-shifted received FSK signals by a mixer, a positive or negative voltage at output of the mixer can be found according to the received data of 1 or 0, respectively. The conventional FSK receiver has an advantage of easy implementation. Data rate of FSK signals is limited by the frequency difference between the mask frequency (data of 1) and the space frequency (data of 0) [8]. For sustaining high data rate, frequency difference between the mask frequency and the space frequency should be large enough, which leads a high IF frequency of the FSK receiver. Therefore, the demodulator (the phase shifter and the mixer) is needed to operate under high frequency, which leads to large power consumption.

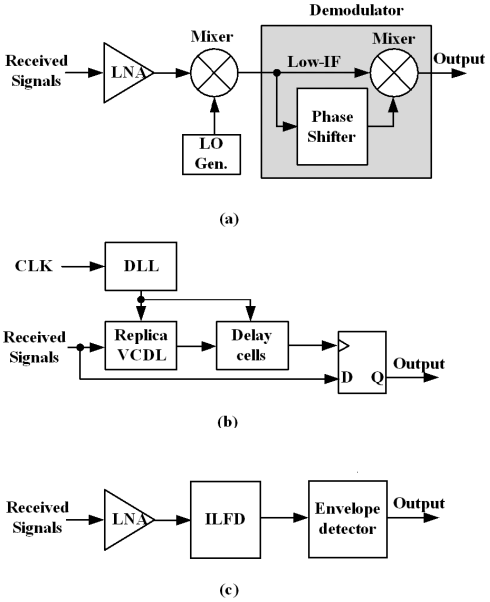

Fig. 1. FSK demodulator. (a) Low-IF, (b) DLL-based, and (c) ILFD architectures.

As shown in Fig. 1(b), an FSK demodulator is implemented using a delay locked loop (DLL) [9]. The DLL is designed to provide a time delay equal to half of a symbol period of

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the received data. Therefore, a signal featured half of symbol period delay to the received signal is used as sampling clock to sample the received signal. Consequently, the received signal is demodulated. The DLL-based demodulator has advantage of less power consumption and higher data rate when comparing with the analog implemented conventional architecture. As shown in Fig. 1(c), an on injection-locked frequency divider (ILFD) architecture-based ULP FSK receiver was proposed to realize a data rate of 5 Mb/s with an energy consumption of 84 pJ per received bit [10]. Moreover, there are some digitally implemented FSK demodulator like zero-IF DFF-based [11], cross differentiate multiply BFSK [12] demodulators. As low-modulation index (MI) is adopted, transition predictive detector (TPD) is added to digitally implemented FSK demodulators [13] to improve jitter performance of the digitally implemented FSK demodulator.

In this paper, by combining both advantages of the conventional low-IF FSK demodulator and the DLL-based FSK demodulator, an ULP zero-IF FSK demodulator is proposed. Rather than using low-IF architecture, the zero-IF demodulator directly processes signals in baseband, which has the ability to demodulate signals with higher data rate under ULP consumption. Moreover, to demodulate FSK signals with extremely high data rate, a digital-assisted calibrated delay-line-based phase shifter is adopted in the proposed demodulator. The proposed ULP FSK demodulator with the digital-assisted calibrated delay-line-based phase shifter also features multirate demodulation for dynamic optimizing energy consumption per received bit according to required operating conditions. The minimum energy consumption of 11 pJ per received bit is achieved under maximum data rate of 40 Mb/s. Measured RMS jitter and peak-to-peak jitter are 316 ps and 1.89 ns, respectively.

The proposed multirate FSK demodulator can be adopted using receivers applied for human body communication to accomplish high-power efficiency data transmission. Owing to less path loss, the human body communication realizes transmission between implantable or wearable biomedical devices under ULP consumption. The measured maximum path loss of the human body channel is about 40 dB under 600 MHz [14]. As maximum output power of 10 dBm is transmitted by a FSK transmitter, the required sensitivity of the FSK receiver needs to be better than -30 dBm (-40 dBV). As the front-end of the FSK receiver provides a gain of 30 dB, a voltage swing of 316 mVp (-10 dBV) can be found at the input of the FSK demodulator.

This paper is organized as follows. The demodulator architecture is described in Section II. Section III describes in detail about the circuits of the demodulator. Finally, Section IV is dedicated to the measurement results of the demodulator, in terms of demodulated data rate and consumed power.

II. System Architecture

Instead of adopting low-IF architecture, a FSK receiver carried out by zero-IF (direct-conversion) architecture is shown in Fig. 2. The FSK receiver is composed of a zero-IF front-end circuit and a demodulator for demodulating

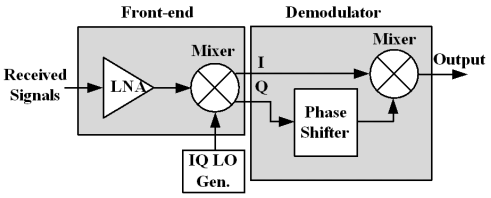

Fig. 2. Zero-IF FSK receiver.

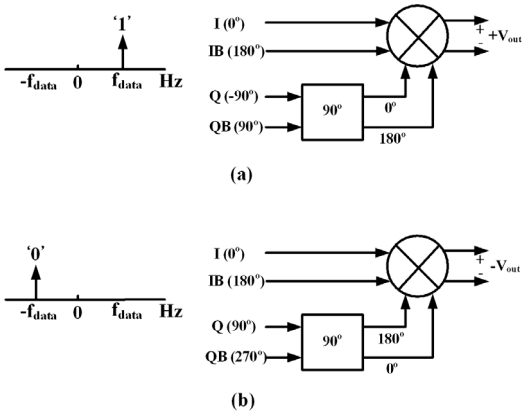

Fig. 3. Zero-IF FSK demodulation. (a) Data is 1. (b) Data is 0.

baseband signals. The zero-IF front-end converts received FSK signals into in/quadrature (I/Q) phase baseband signals. It is worth mentioning that the baseband signals feature constant in amplitude and frequency. The received FSK signals are converted into phase-modulated baseband signals by the zero-IF front-end. I/Q phase baseband signals will 90° lead or lag to each other according to the received data. Principle of demodulating the baseband signals is shown in Fig. 3(a) and (b) for mask frequency (data of 1) and space frequency (data of 0), respectively. As shown in Fig. 3(a), when demodulating mask frequency by the demodulator, the Q-channel (quadrature-phase channel) baseband signals lead I-channel baseband signals by 90°. A phase shifter is used to provide 90° phase shift for the Q-channel baseband signals. Therefore, the Q-channel baseband signals will in-phase with the I-channel signals. After mixing the Q-channel baseband signals with the I-channel baseband signals by a mixer, a positive output voltage can be found at the output of the mixer. Consequently, the data of 1 is demodulated. On the contrary, as shown in Fig. 3(b), when demodulating space frequency by the demodulator, the Q-channel signals lag I-channel baseband signals by 90°. As phase shifting by the phase shifter, the Q-channel baseband signals will out-of-phase with the I-channel baseband signals. After mixing the I-channel and Q-channel baseband signals by the mixer, a negative output voltage can be found at the output of the mixer. Consequently, the data of 0 is demodulated.

As shown in Fig. 4, the proposed ULP multirate FSK demodulator for high-speed biomedical zero-IF receivers is composed of a digital-assisted calibrated DL-based phase shifter and an ULP double-balance mixer. The digital-assisted calibrated DL-based phase shifter for realizing an automatic tunable phase shifting comprises a DL-based phase shifter, a digital-assisted dc-offset calibration circuitry and a MUX.

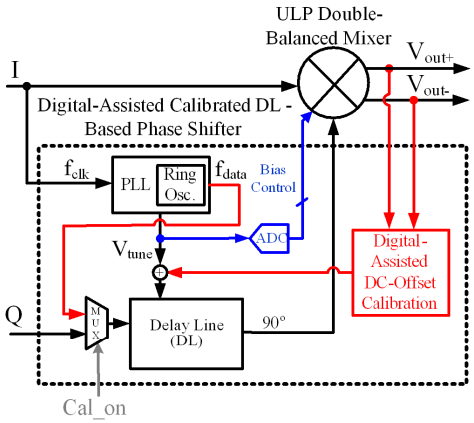

Fig. 4. Architecture of the ULP multirate FSK demodulator.

The DL-based phase shifter is used to provide 90° phase shift to the Q-channel baseband signals.

As mentioned above, data rate of FSK signal is limited by the frequency difference between mask frequency (data of 1) and space frequency (data of 0). For example, to sustain an FSK signal with data rate of 10 Mb/s, the frequency difference between mask frequency and space frequency is at least 5 MHz, which is the smallest FSK modulation index (MI) that can be chosen such that the waveforms for 0 and 1 are orthogonal. When down-converting the FSK signal to I/Q baseband signals by the zero-IF receiver, the frequency of the I/Q baseband signals is 2.5 MHz. Thus, the frequency of the I/Q baseband signals is proportional to the data rate of the FSK signal. As the proposed DL-based phase shifter can provide a phase shift of 90° for the baseband signals with different frequency, the multirate FSK demodulation can be achieved.

Inaccuracy of the phase shift provided by the DL-based phase shifter and dc-offset of the ULP double-balance mixer owing to process, supply voltage, and temperature (PVT) variations all result in a dc-offset at output of the demodulator, which leads to an increase in bit error rate (BER) of the demodulator specially as operating under high throughput conditions. Thus, the digital-assisted dc-offset calibration circuitry is used to calibrate the dc-offset.

For achieving ULP consumption, all circuits (including analog circuits and digital circuits) operate in subthreshold region. Additionally, due to operating frequency of the proposed DL-based phase shifter is proportional to the data rate of the baseband signals, the power consumption of the proposed DL-based phase shifter can be reduced as the data rate decreased. Besides, power consumption of the ULP double-balanced mixer is also adjustable according to the data rate. The proposed demodulator achieves a high data rate of 40 Mb/s with a power consumption of only 440 μW. Thus, a minimum energy consumption of 11 pJ per received bit is achieved in this paper.

III. Circuit Design

A. DL-Based Phase Shifter

As shown in Fig. 5, the proposed DL-based phase shifter consists of a PLL and a delay line (DL). The received FSK

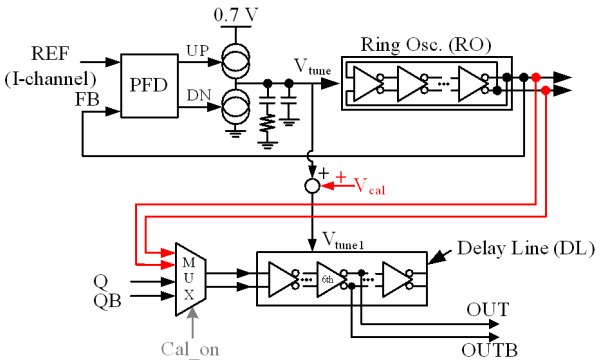

Fig. 5. Architecture of DL-based phase shifter.

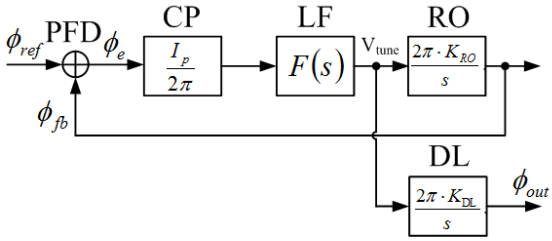

Fig. 6. S-domain model of the DL-based phase shifter.

signal is converted into the phase-modulated I/Q baseband signals by the front-end of the zero-IF receiver. It is implying that the frequency of the I/Q baseband signals is constant. Therefore, the frequency of the I/Q baseband signals can be recovered by the PLL through the I/Q baseband signals (I-channel baseband signal in this design) is served as the reference clock (REF) of the PLL. As the frequency of the I/Q baseband signals is recovered by the PLL, the DL shared the same tuning voltage with the PLL can provide a 180° phase shift to the Q-channel baseband signals (Q and QB). The ring oscillator (RO) used in the PLL comprises 12 stages of delay cells, so as the DL. Therefore, using the half stages of the DL (six stages) can provide a phase shift of 90° to the Q-channel baseband signals.

Rather using DLL + DL, PLL + DL is adopted in the DL-based phase shifter owing to the PLL + DL provides a low-pass filtering to both the jitter of I-channel baseband signals and the jitter of the RO. As shown in Fig. 6, jitter transfer from the reference CLK (the I-channel baseband signal) or the RO to the output of the DL is derived as

$$G(s) = \frac{I_p}{2\pi} \cdot F(s) \cdot \frac{2\pi \cdot K_{\mathrm{RO}}}{s} \tag{1}$$

$$\frac{\phi_{\mathrm{out}}}{\phi_{\mathrm{ref}}} \text{ or } \frac{\phi_{\mathrm{out}}}{\phi_{\mathrm{RO}}} = \frac{\frac{I_p}{2\pi} \cdot F(s) \cdot \frac{2\pi \cdot K_{\mathrm{DL}}}{s}}{1 + G(s)} \tag{2}$$

where I_p is bias current of the CP, F(s) is transfer function of a second-order loop filter, and K_{RO} and K_{DL} are gain of the RO and the DL, respectively. The second-order loop filter is designed with a bandwidth of 1 MHz.

For minimizing the power consumption of the PLL, supply voltage of the PLL is reduced to 0.7 V and ensures that the PLL operates up to 40 MHz. To operate up to 40 MHz under 0.7 V, TSPC-based PFD is adopted in the PLL. The schematic of charge pump is shown in Fig. 7. The charge pump also operates under supply voltage of 0.7 V and bias under a current

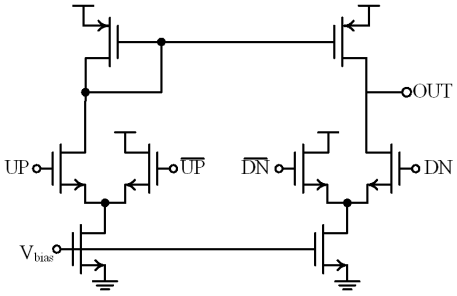

Fig. 7. Schematic of charge pump.

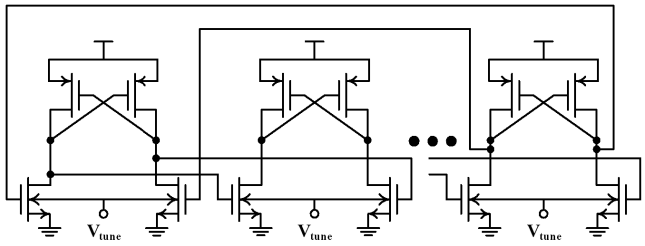

Fig. 8. Schematic of RO. Delay line (DL) is open-loop version of the RO.

of 25 uA. Owing to the small charge pump current is used, a high VCO gain of 100 MHz/V is needed for maintaining the loop gain of the PLL.

Fig. 8 shows the schematic of the RO and DL. nMOS transistors have separated substrate by using deep N-well. The threshold voltage of the nMOS transistors is derived as

$$V_{\text{th}} = V_{\text{th0}} + \gamma \cdot \left(\sqrt{|2\phi_F - V_{\text{BS}}|} - \sqrt{2\phi_F}\right). \tag{3}$$

As V_{BS} increases, V_{th} will decrease, which leads to an increase in the trans-conductance of the nMOS transistors. Both the power consumption and oscillating frequency increase as the bulk voltage (V_{BS}) of the nMOS transistor increases. Therefore, by tuning the bulk voltage (V_{BS}) of the nMOS transistor, a positive frequency tuning characteristics of the RO and DL can be found. The proposed DL-based phase shifter provides 90° phase shift for the Q-channel baseband signals with frequency up to 40 MHz under an ULP consumption of 168.4 μW in 0.18 μm CMOS process.

B. ULP Double-Balanced Mixer

The schematic of the ULP double-balanced mixer is shown in Fig. 9. The double-balanced mixer is pMOS Gilbert cell type (M1–M6) with dynamic source degeneration (M7–M8). All transistors are operated in subthreshold region for fulfilling the requirement of ULP. The trans-conductance of a MOS transistor operated in subthreshold region is

$$g_m = \frac{I_D}{n \cdot V_T} \tag{4}$$

where n is a process dependent constant value around 1.5, V_t is thermal voltage (25 mV), I_D is bias current of the MOS transistor. As the MOS transistor is operated in subthreshold region, trans-conductance of the MOS transistor is proportional to I_D. Therefore, under being biased at the same current, the MOS transistor operated in subthreshold region is more power efficient than operated in strong inversion region (g_m is proportional to square root of I_D). For example, as the MOS transistor is operated in subthreshold region and is biased under a current of 10 μA, a trans-conductance of 0.4 ms can be provided. The relative small g_m causes a small intrinsic gain provided by a transistor operated in subthreshold. Comparing with being operated in strong inversion region, transistors operated in subthreshold region have a small (around 100 mV in 0.18 μm CMOS process) and V_{GS}-independent $V_{\text{DS,sat}}$ (the required minimum V_{DS} for a transistor is operated in saturation region). Therefore, to have a required gain as a transistor is operated in subthreshold region, cascode configuration is adopted to increase output impedance. Moreover, all current sources are cascode configuration for improving common-mode rejection ratio (CMRR) performance.

For ensuring enough gain of common-mode feedback under PVT variation, a common-mode feedback loop (M11–M14) is used for defining output dc of the mixer. Moreover, a dc feedback loop (M9–M10) is also used for defining output dc of the mixer.

The frequency of the I/Q baseband signals is proportional to the data rate. When recover the frequency of the I/Q baseband signals by the PLL in the DL-based phase shifter, tuning voltage of the PLL in the DL-based phase shifter is proportional to the frequency of the I/Q baseband signals. Therefore, the tuning voltage of the PLL in the DL-based phase shifter is proportional to the data rate. Adjusting bias current of the mixer according to the tuning voltage of the PLL in the DL-based phase shifter causes the decrease of power consumption of the mixer as the data rate decreases. As shown in Fig. 10, a 5-bit analog-to-digital converter (ADC) converts the tuning voltage (V_{tune}) of the PLL in the DL-based phase shifter into a digital word for further adjusting bias current of the mixer by a 5-bit digital-to-analog converter (DAC) (shown in Fig. 9).

C. Digital-Assisted DC-Offset Calibration Circuitry

As shown in Fig. 11(a), the inaccurate 90° phase shift provided by the DL-based phase shifter ($\Delta\Phi$) and dc-offset of the mixer ($V_{\text{in,os}}$) all lead to a dc-offset ($V_{\text{out,os}}$) at the output of the demodulator, which results in increasing of (BER) specially operating under high data rate. The differential output voltage of the demodulator is shown in Fig. 11(b). The differential output voltage increases or decreases from 0 V according to the received data. Magnitude of the differential output voltage is dependent on the data rate. Higher data rate leads to a smaller magnitude of the output voltage. As the magnitude of the differential output voltage is smaller than the dc-offset, a wrong decision of output data is happened. A digital-assisted dc-offset calibration circuitry is proposed to eliminate the dc-offset before receiving data. As calibrating dc-offset of the demodulator, instead of inputting Q-channel baseband signals into the DL of the DL-based phase shifter, the output signals of the RO of the DL-based phase shifter is switched into the DL by a control pin called Cal_on (shown in Fig. 4). The output signals of the RO are in-phase with the I-channel signals. The DL provides a phase shift of 90°

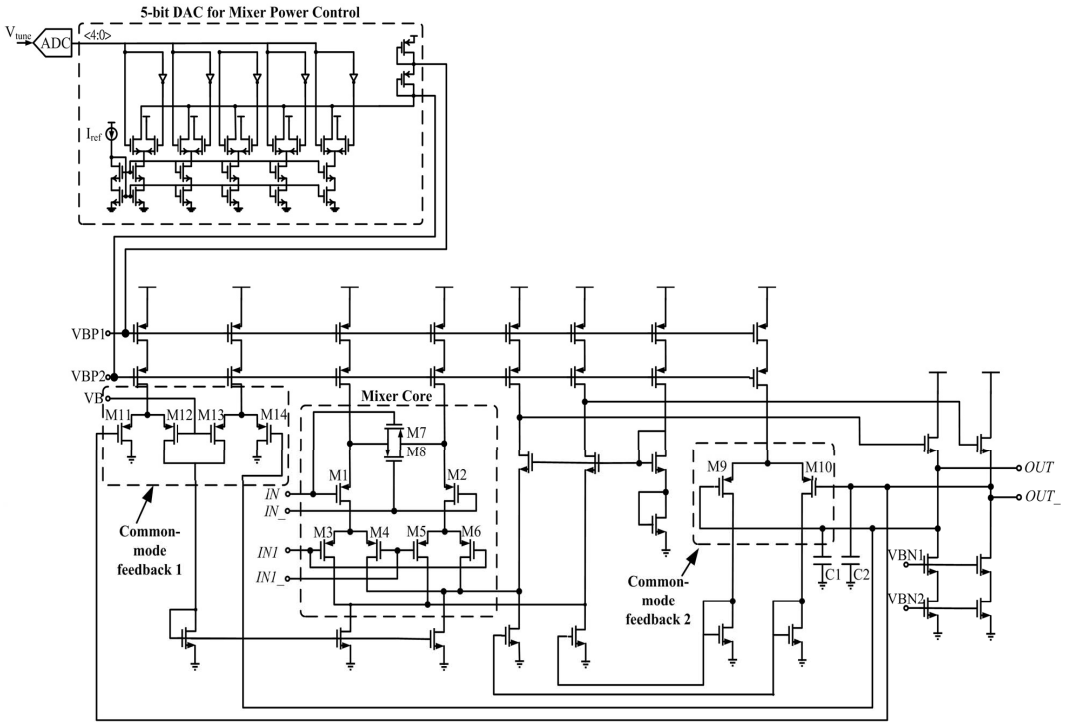

Fig. 9. Schematic of ULP double-balanced mixer.

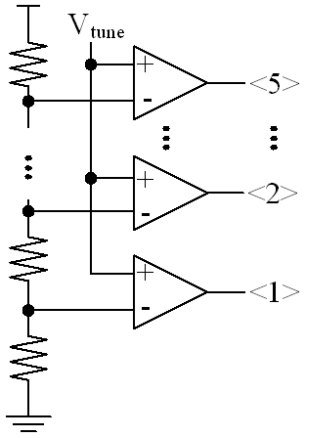

Fig. 10. Five-bit ADC.

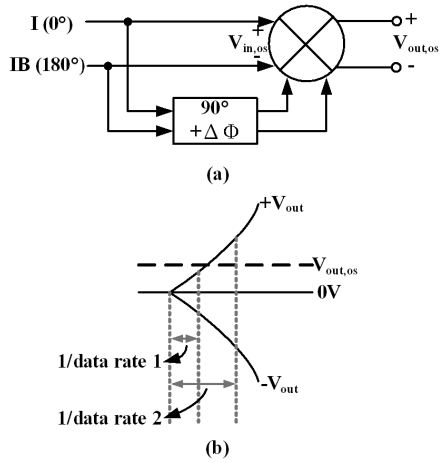

Fig. 11. Output dc-offset of the demodulator.

to the output signals of the RO. Therefore, the output signals of the DL are out-of-phase to the I-channel baseband signals. After mixing the I-channel baseband signals and the 90° phase shifted output signals of the RO by the mixer, an output dc-offset of the demodulator contributed by the inaccurate phase shift of the DL-based phase shifter and the dc-offset of the mixer can be found.

As shown in Fig. 12, the digital-assisted dc-offset calibration circuitry is composed of a comparator, a successive approximation (SAR) digital control unit and two 7-bit DACs. The comparator is designed to convert the output dc-offset of the demodulator into a 1-bit digital word. The SAR digital control unit is designed to control one of the two 7-bit DACs based on the output of the comparator for generating an output voltage ($V_{\rm dac}$). Another 7-bit DAC is used to generate the middle voltage ($V_{\rm middle}$) of the entire calibration voltage range. Finally, the difference voltage ($V_{\rm cal}$) of $V_{\rm dac}$ and

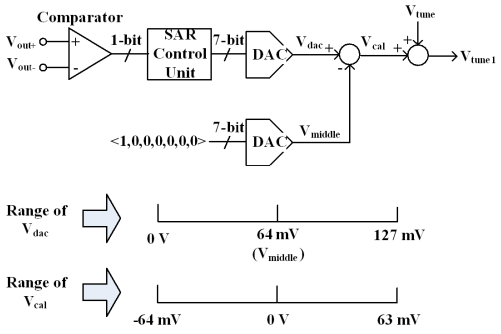

Fig. 12. Architecture of digital-assisted dc-offset calibration circuitry.

$V_{\rm middle}$ is added to the tuning voltage ($V_{\rm tune}$) of the DL-based phase shifter for further adjusting the phase shift provided by the DL-based phase shifter until the output dc-offset of the

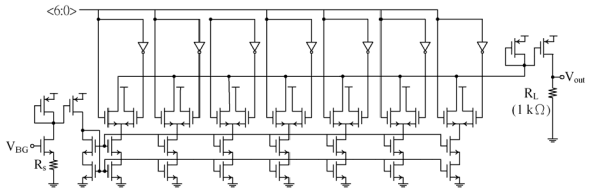

Fig. 13. Schematic of 7-bit DAC.

demodulator reaches its minimum. The minimum dc-offset and the range of dc-offset that the calibration circuitry can process are dependent on the resolution and the number of bits of the DACs, respectively. In this design, a 7-bit DAC with LSB current of 1 uA is adopted. Consequently an output current of $0 \sim 127$ uA corresponding to an output voltage of $0 \sim 127$ mV can be provided by the 7-bit DAC with an output resistance of 1 kΩ, which corresponds to an output voltage (V_{cal}) range from -64 to 63 mV with a resolution of 1 mV can be found to adjust the phase shift provided by the DL-based phase shifter for eliminating the output dc-offset. Because the tuning gain of the RO in the DL-based phase shifter is 100 MHz/V, the additional tuning voltage (V_{cal}) provided by the dc-offset calibration circuitry leads to a frequency tuning range of the RO in the DL-based phase shifter from 13.6 to 26.3 MHz with resolution of 100 kHz. Therefore, the DL-based phase shifter can provide a precise phase shift of 90° for Q-channel baseband signals from 13.6 to 26.3 MHz to against PVT variation. I/Q mismatch also leads to a dc-offset at the output of the demodulator. Phase mismatch can be cancelled by the dc-offset calibration in this paper (by changing the phase shift provided by the DL-based phase shifter). Amplitude mismatch can be compensated by the additional phase shift provided by the DL-based phase shifter.

The comparator is composed of a differential amplifier and a latch [15]. The differential amplifier is also designed with an auto-zeroing function for eliminating its own dc-offset. The schematic of the 7-bit DAC is shown in Fig. 13. The reference current of the DAC is generated as

$$I_{\text{ref}} = \frac{V_{\text{BG}} - V_{\text{GS}}}{R_s} \tag{5}$$

where V_{BG} is generated by a bandgap reference circuit. The output voltage of the DAC is

$$V_{\text{out}} = I_{\text{ref}} \cdot R_L \cdot \sum_{n=0}^{6} (A_n \cdot 2^n) \tag{6}$$

where A_n (n is from 0 to 6) is the 7-bit control word of the DAC. According to (5) and (6), the PVT variation of R_s and R_L can be cancelled each other by using the same type of resistor and the appropriate layout. PVT variation of V_{GS} will lead to PVT variation of I_{ref} and V_{out}. Because V_{out} is added to the V_{tune} for controlling phase shift of the DL in the DL-based phase shifter, V_{GS} of the transistors in the DL in the DL-based phase shifter also varies with the same PVT variation. Therefore, the trans-conductance of the transistors in the DL in the DL-based phase shifter can be kept constant under PVT variation.

A simulated procedure of the SAR dc-offset calibration is shown in Fig. 14. Initially, the DAC is set as

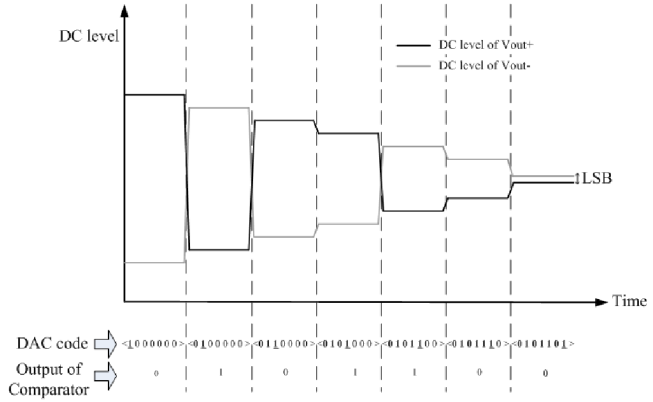

Fig. 14. Simulated procedure of the dc-offset calibration.

TABLE I
SIMULATED POWER CONSUMPTION OF EACH BUILDING BLOCK IN THE DEMODULATOR

Building Block	Current Consumption	Supply Voltage	Power Consumption
ULP Double-Balanced Mixer	148.5 μA (40 Mb/s) 110.6 μA (20 Mb/s) 72.4 μA (10 Mb/s) 52 μA (5 Mb/s)	1.8 V	267.3 μW (40 Mb/s) 199.08 μW (20 Mb/s) 130.32 μW (10 Mb/s) 93.6 μW (5 Mb/s)
PFD	14.4 μA (40 Mb/s) 5.8 μA (20 Mb/s) 2.8 μA (10 Mb/s) 1.4 μA (5 Mb/s)	0.7 V	10.08 μW (40 Mb/s) 4.06 μW (20 Mb/s) 1.96 μW (10 Mb/s) 0.98 μW (5 Mb/s)
Charge Pump	50 μA	0.7 V	35 μW
RO + DL	88 μA + 88 μA	0.7 V	123.2 μW
Total			436.3 μW (40 Mb/s) 361.34 μW (20 Mb/s) 290.48 μW (10 Mb/s) 252.78 μW (5 Mb/s)

$\langle 1\ 0\ 0\ 0\ 0\ 0\ 0 \rangle$. Then, the SAR digital control unit performs SAR search according to the one-bit output of the comparator. After six clock cycles, the output dc-offset of the demodulator is minimized.

D. Data Rate-Dependent Power Consumption

The simulated power consumption of each building block in the demodulator under different data rates is listed in the Table I. The ULP double-balanced mixer supplied by 1.8 V consumes from 93.6 to 267.3 μW according to the tuning voltage (V_{tune}) of the DL-based phase shifter as received data rate varies from 5 to 40 Mb/s. PFD in the DL-based phase shifter consumes from 0.98 to 10.08 μW according to the

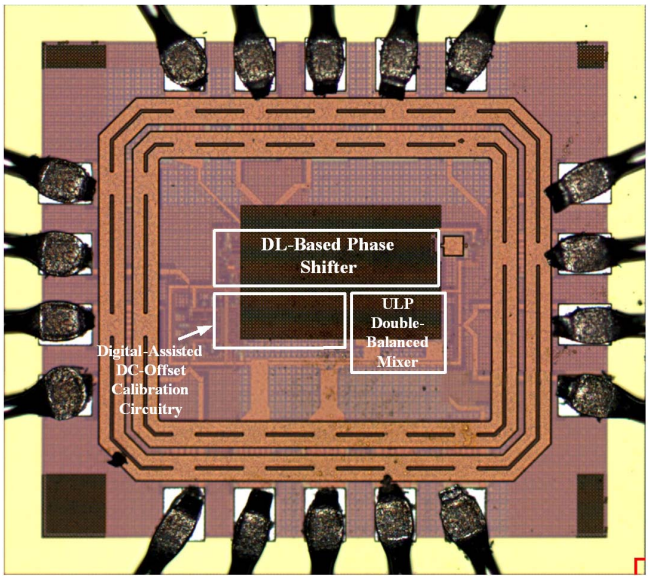

Fig. 15. Die photo of the ULP multirate FSK demodulator.

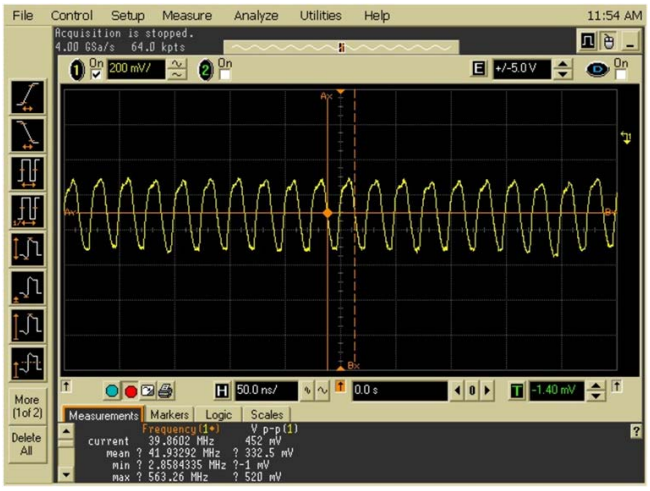

Fig. 16. Output waveform of the RO in the PLL.

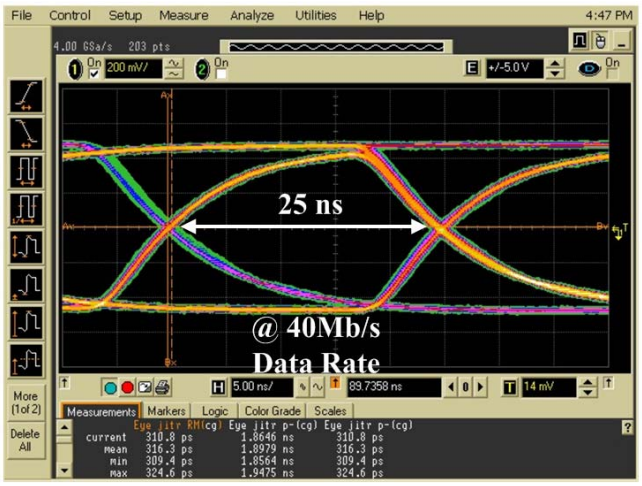

Fig. 17. Eye diagram of demodulated bit streams under data rate of 40 Mb/s.

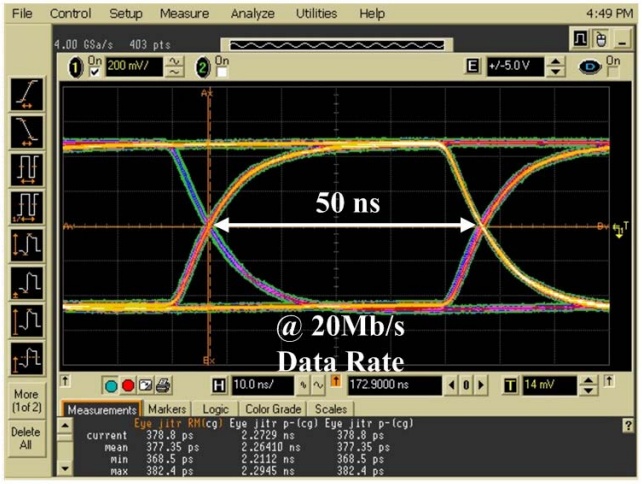

Fig. 18. Eye diagram of demodulated bit streams under data rate of 20 Mb/s.

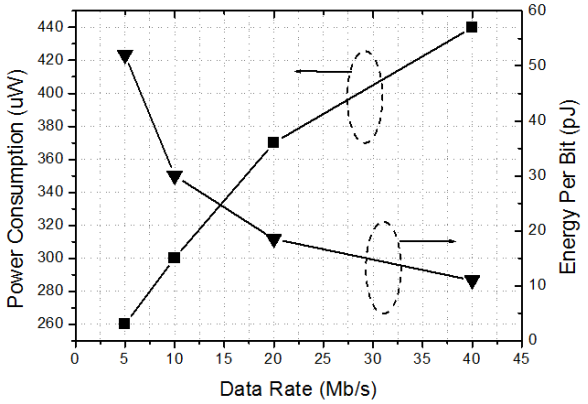

Fig. 19. Measured power consumption and energy consumption per received bit versus data rate.

frequency of the I-channel baseband signals under supply voltage of 0.7 V. The charge pump, the RO, and the DL consumes 35, 61.6, and 61.6 μW, respectively. Therefore, the overall demodulator consumes from 252.78 to 436.3 μW as received data rate varies from 5 to 40 Mb/s.

IV. Measurement Result

The ULP multirate FSK demodulator for zero-IF receivers has been implemented in standard 0.18 μm CMOS technology and occupies 470×210 mm^2. The chip micrograph is shown in Fig. 15. To optimize performance of the demodulator under minimum power consumption, two different supply voltages of 1.8 and 0.7 V are applied for analog and digital circuits, respectively. FSK modulated I/Q baseband signals with amplitude of 300 mV$_p$ is applied to the demodulator. The measured output waveform of the RO in the PLL is shown in Fig. 16. The RO is locked with the frequency of the I-channel baseband signals (40 MHz). The measured eye diagram of the output of the demodulator under the $2^7 - 1$ PRBS bit streams with data rate of 40 Mb/s is shown in Fig. 17. The measured RMS jitter and peak-to-peak jitter are 316 ps and 1.89 ns, respectively. The demodulator is also tested under different data rates. The measured eye diagram of the output of the demodulator under $2^7 - 1$ PRBS bit streams with data rate of 20 Mb/s is shown in Fig. 18. The measured RMS jitter and peak-to-peak jitter are 377 ps and 2.26 ns, respectively. Measured power consumption

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This Work	[7]	[9]	[10]	[13]	[16]
Technology	0.18 μm CMOS	0.25 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.13 μm CMOS
Supply Voltage (V)	1.8 (analog) / 0.7 (digital)	2.5	1.2	0.7	1	1
Demodulator Architecture	Digital-Assisted Calibrated DL-based Phase Shifter	Low-IF	DLL-based	Injection-Locked Frequency Divider (ILFD)	DLL+TPD	Digital
Max. Data Rate	40 Mb/s	1 Mb/s	N.A.	5 Mb/s	10 Mb/s	200 kb/s
Demodulated Jitter	1.89 ns (peak-to-peak)	N.A.	N.A.	N.A.	4 ns	N.A.
Power Consumption of demodulator	440 μW	5 mW	360 μW	210 μW	80 μW	12 μW
Energy/bit of demodulator under Max. Date Rate	11 pJ/bit	5 nJ/bit	N.A.	42 pJ/bit	8 pJ/bit	24 pJ/bit

and energy consumption per received bit versus data rate are shown in Fig. 19. The performance summary of the proposed demodulator and comparison with the reported state-of-the-art demodulators are listed in Table II. As shown in Table II, this paper achieves the highest data rate of 40 Mb/s with an energy consumption of 11 pJ per received bit.

V. CONCLUSION

A ULP multirate FSK demodulator implemented in standard 0.18 μm CMOS technology and applied for high-speed biomedical zero-IF receivers was presented in this paper. The demodulator features variable data date. Power consumption of the demodulator is optimized according to the required data rate. Therefore, the energy consumption per received bit can be optimized on the basis of the applications. The minimum energy consumption of 11 pJ per received bit and demodulated peak-to-peak jitter of 1.89 ns are achieved under maximum data rate of 40 Mb/s.

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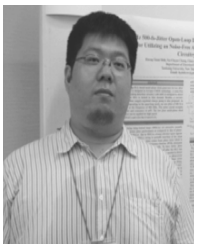

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