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Applying the selective Cu electroplating technique to light-emitting diodes

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Abstract We successfully fabricated a predefined patterned copper (Cu) substrate for thin GaN light-emitting diodes without barriers by the selective electroplating technique. The contours of Cu bumps fabricated using different electroplating modes and parameters were measured. We observed that the average thickness diminished with increasing current density. The current density conditions to obtain the best upright structure in the process were 40 and 80 mA/cm².

Keywords Electroplating · Selective electroplating · LED · GaN · Cu bump

Introduction

GaN-based light-emitting diodes (LEDs) have been applied to solid-state lighting for many years [1–3]. There are three types of packaging for GaN-based LED structures: mesa type, flip chip, and thin GaN. Among these, the mesa-type structure is the most commonly used, but it has poor heat dissipation due to the inferior heat conductivity of its sapphire substrate. To solve this problem, the thin GaN structure is used to transfer the GaN epilayer to a new substrate with relatively high thermal and electrical conductivity, such as silicon, nickel (Ni) or copper (Cu). However, it is difficult to displace the substrate owing to the new techniques of wafer bonding and laser lift-off in the thin GaN process [4–6]. The wafer bonding process will make the wafer bend and degrade the yield, especially in large wafer-scale

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production. On the other hand, high temperature in the wafer bonding process will also force the GaN thin film to bear high thermal stress and induce cracking and lower quality of the GaN epilayer. To avoid the above disadvantages, electroplating is an alternative technique to replace the technique of wafer bonding. The electroplating technique has been developed by the semiconductor industry over a long span of time. Compared with the Cu electroless technique, electroplating is much cheaper and easier to control in production [7]. Use of electroplating in the thin GaN LED process also has several advantages: It is much cheaper in industrial applications, and uses a lower temperature, which reduces damage to the GaN epilayer as well as wafer bending. In summary, applying the electroplating technique to the thin GaN LED process could improve production yield.

In this study, Cu was chosen as the new substrate material because of its high thermal and electrical conductivity. To reach the goal of chip definition, some researchers have used photoresist (PR) as a barrier to electroplate Cu foil onto a defined chip [8, 9]. However, this method has some disadvantages. Firstly, it is limited by the PR's thickness. The electrodeposited Cu layer in the LED chip process is expected to be thicker than $100\ \mu\text{m}$, but in general it is very difficult to reach such thickness using PR. When the electrodeposited Cu layer becomes thicker than the PR barrier, the Cu pillar will grow horizontally to form a mushroom shape, which is unfavorable for subsequent processing. In addition, the stability of PR has been shown to be poor. PR is usually an organic material, being extremely unstable in the electroplating process, so we developed a novel selective electroplating technique without use of a PR barrier. This technique enables one to produce a predefined chip while avoiding possible damage in subsequent Cu cutting processes.

Moreover, various electroplating modes have been studied, including potentiostatic and pulse-potential electroplating. We obtained a high selection rate using pulse-potential electroplating. By controlling factors such as the current density, electroplating mode, and electrolyte composition and additives, we achieved different types of electroplated films. Excellent upright structures could be obtained by using different additives and applying different current densities in the Cu electroplating process [10, 11]. Different types of Cu films can be achieved by using different current densities.

In this study, the morphology of the deposited Cu film is an important issue. Scanning electron microscopy (SEM) and alpha-step profilometry were used to analyze the morphology. Also, the relationship between the change of the reduction potential and various current densities is discussed.

Experimental

First, we fabricated predefined $800 \times 800\ \mu\text{m}^2$ pads on the LED wafer, separated by gaps of approximately $300\ \mu\text{m}$. A metal layer comprising Ti/Ni/Au ($500/500/4,000\ \text{\AA}$) was then deposited on the pads using an E-beam vaporization system. The Au layer served as the seed layer for Cu deposition. Finally, we removed the PR and lifted off the metallization on it using acetone before electroplating. The metal pads on the substrate had no metal connections. All the experimental processes are illustrated in Fig. 1.

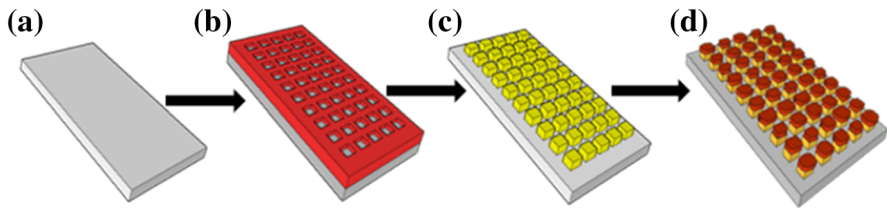


Fig. 1 Flowchart of the fabrication process: **a** semiconductor substrate, **b** PR patterned by photolithography, **c** metal deposited by E-gun, and **d** Cu deposited by selective electroplating

The electrolyte consisted of 83.14 g/L CuSO_4 and 200 g/L H_2SO_4 as the base. It also contained 600 ppm polyethylene glycol, 100 ppm HCl, 10 ppm Janus Green B, and 5 ppm bis(3-sulfopropyl) disulfide as additives. The electroplating process with constant current density was carried out in a three-electrode system. The semiconductor wafer was the working electrode. A Pt coil and Ag/AgCl electrode were the counter and reference electrodes, respectively. For potentiostatic electroplating, we set the electric potential at $E = -0.8$ and -0.9 V. The electroplating time was 2,400 s. Besides, we set the electric potential of the pulse-potential electroplating at $E_{\text{on}} = -0.8$ V/ $E_{\text{off}} = 0$ V and $E_{\text{on}} = -0.9$ V/ $E_{\text{off}} = 0$ V. The on-off time was set around 0.5–1.0 s, while the total on-time was 2,400 s. The electroplating was performed with constant charge at various current densities of 20, 40, 80, 100, and 160 mA/cm². The experimental parameters are presented in Table 1.

Finally, the Cu bumps were observed by SEM (S-2600H; Hitachi), and the thickness was measured by alpha-step profilometer (Surfcoorder ET3000; Kosaka Lab. Ltd., Japan).

Results and discussion

Surface morphology of Cu bumps

Figure 2 shows the SEM results after applying the different electroplating approaches, i.e., potentiostatic and pulse-potential electroplating. Figure 2a and b show the results when stabilizing the electric potential at -0.8 and -0.9 V, respectively. Figure 2a reveals a much more obvious white brim of the Cu bumps than in Fig. 2b. In other words, the greater the voltage, the steeper the sides of the Cu bumps became. Moreover, we also tried to electroplate Cu using pulse-potential electroplating. Figure 2c and d show the results obtained when applying pulse-potential electroplating at $E_{\text{on}} = -0.8$ V/ $E_{\text{off}} = 0$ V and $E_{\text{on}} = -0.9$ V/ $E_{\text{off}} = 0$ V, respectively. The on-off time was set around 0.5–1.0 s, while the total on-time was 2,400 s. We observed that the result of pulse-potential electroplating was similar to that of the potentiostatic method. Figure 2c shows that, after pulse-potential electroplating at $E_{\text{on}} = -0.8$ V/ $E_{\text{off}} = 0$ V, the edges of the Cu bumps were rather smooth. However, when applying pulse-potential electroplating at

Table 1 Experimental parameters

Current density (mA/cm ²)	20	40	80	100	160
Time (s)	5,400	2,700	1,350	1,080	675

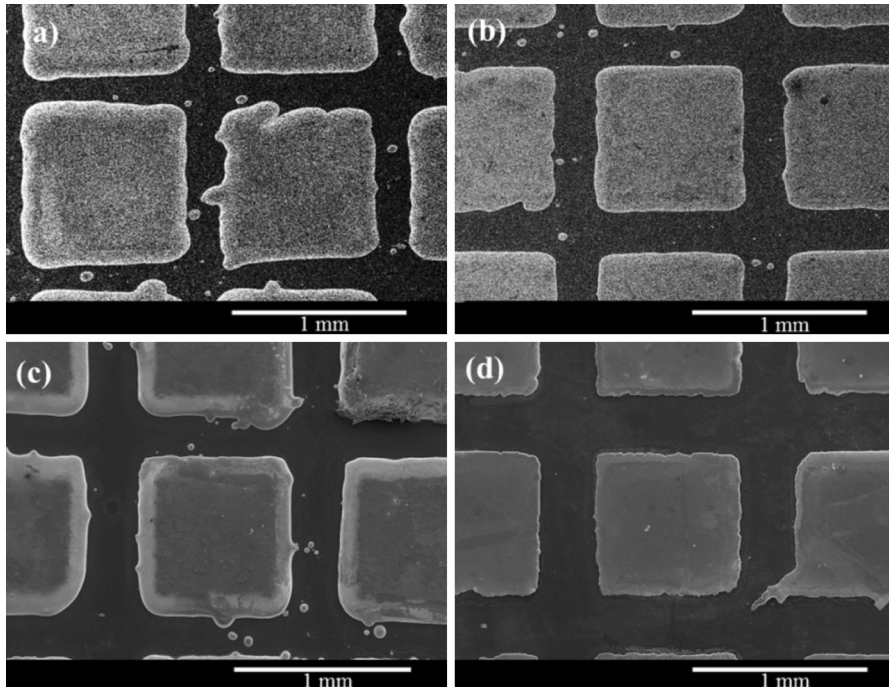


Fig. 2 SEM images of Cu bumps deposited by **a** potentiostatic electroplating at -0.8 V, **b** potentiostatic electroplating at -0.9 V, **c** pulse-potential electroplating at $E_{\text{on}} = -0.8$ V/ $E_{\text{off}} = 0$ V, and **d** pulse-potential electroplating at $E_{\text{on}} = -0.9$ V/ $E_{\text{off}} = 0$ V

$E_{\text{on}} = -0.9$ V/ $E_{\text{off}} = 0$ V, we found that the edges of the Cu bumps became steep, as shown in Fig. 2d. In other words, the more negative the electric potential, the steeper the edges of the Cu bumps became. Therefore, we conclude that we will get different results under different voltages. We also wanted to know what results would be obtained when applying different electroplating approaches, thus experiments were also performed under different current densities.

The surface morphologies of Cu bumps deposited using different current densities were observed by SEM. Figure 3a shows predefined Au pads before Cu electroplating. The shape of the Cu bumps deposited at 20 mA/cm² was almost the same as the predefined Au patterns (Fig. 3b). The edges of the Cu bumps became obtuse when deposited at current density of 40 mA/cm² (Fig. 3c). The edges of the Cu bumps became sharper when current density of 80 mA/cm² was used for the

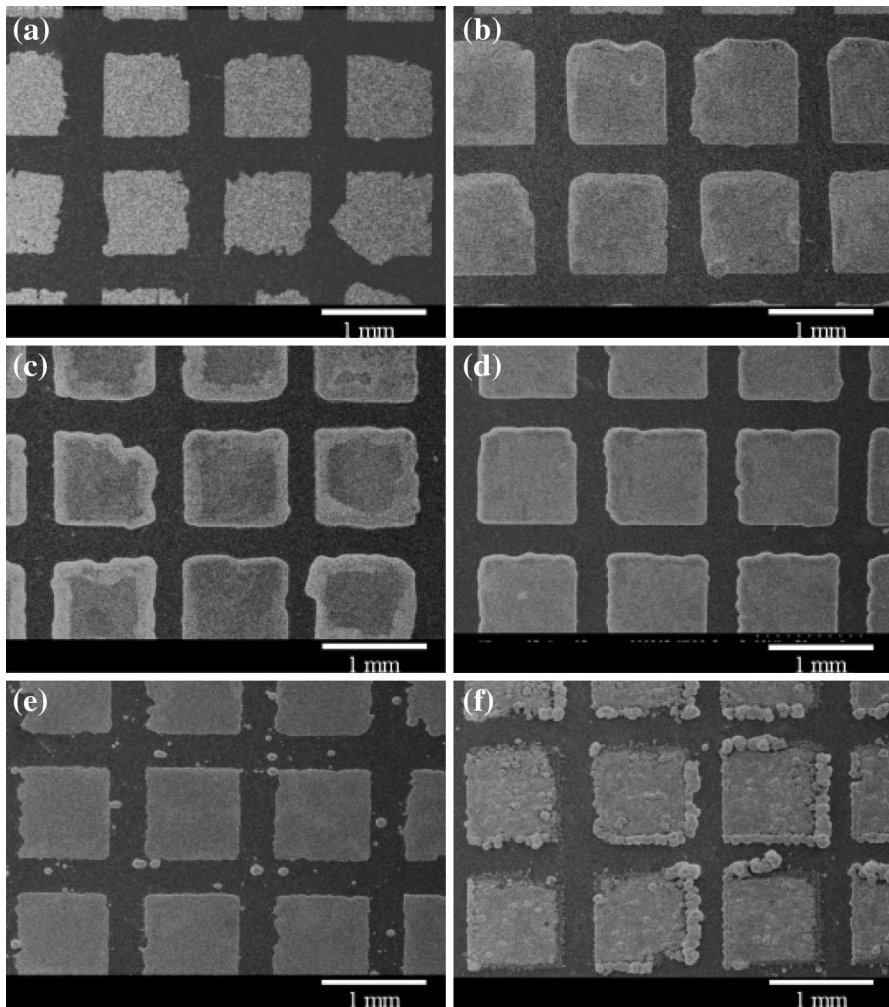


Fig. 3 SEM images of **a** predefined Au patterns, and Cu bumps deposited at current density of **b** 20 mA/cm², **c** 40 mA/cm², **d** 80 mA/cm², **e** 100 mA/cm², and **f** 160 mA/cm²

deposition (Fig. 3d). As shown in Fig. 3e, many small particles started to form on the gaps when Cu deposition was carried out at 100 mA/cm². These particles enlarged when the deposition current density was increased to 160 mA/cm² (Fig. 3f). We found a rough surface and also many large particles deposited on the gaps between and the edges of the Cu bumps. The edge and center of the Cu bumps were smooth and flat when deposited at current density below 40 mA/cm². It is difficult to control the morphology of the Cu bumps if the deposition current density reaches 160 mA/cm². In a word, independent of whether we used the potentiostatic or pulse-potential technique, or the current density, Cu bumps on thin GaN LEDs could be successfully produced by selective electroplating without barriers.

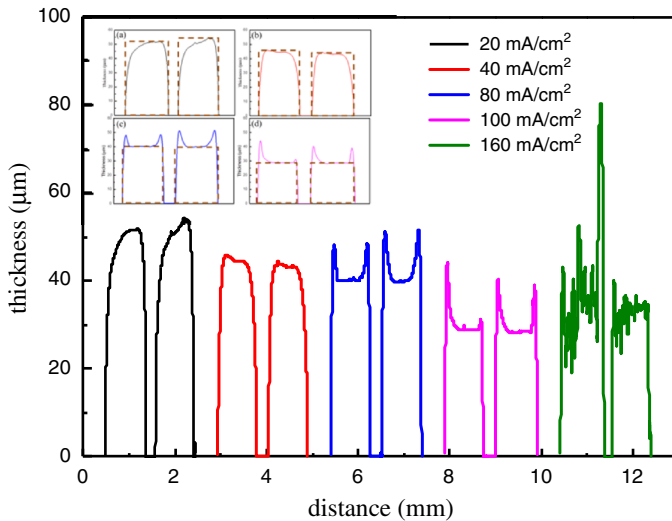


Fig. 4 Cross-sectional profiles of Cu bumps deposited at different current densities and the ideal and real surface morphologies of Cu bumps deposited at (a) 20 mA/cm², (b) 40 mA/cm², (c) 80 mA/cm², and (d) 100 mA/cm²

Thickness of the Cu bumps

The surface profile of Cu bumps deposited at different current densities was measured by alpha-step profilometry, and the results are shown in Fig. 4. It was found that the edges of the Cu bumps were obtuse when deposited at 20 mA/cm². They became smoother when the deposition current density was increased to 40 mA/cm². However, the edges of the Cu bumps became sharp and grew outward when we increased the deposition current density to 80 or 100 mA/cm². The current density of 160 mA/cm² was too high for the deposition process since the Cu bump surface became extremely coarse. Measurements of the height at the center of the Cu bumps showed that the average thickness decreased with increasing deposition current density. In the upper-left inset in Fig. 5, the dotted line indicates the ideal morphology of the Cu bumps, in comparison with the real situation shown by the solid line. The Cu bumps obtained at the current densities of 20 and 40 mA/cm² were not as thick as the rim of the ideal Cu bump morphology. On the contrary, the sharp edges of bumps deposited at 80 and 100 mA/cm² extended beyond the dotted rectangle. Therefore, we judge that the best morphology was obtained between 40 and 80 mA/cm².

The steady-state reduction potential and average Cu bump thickness are plotted against the deposition current density in Fig. 5. The average thickness decreased while the steady-state reduction potential became more negative. We suppose that the more negative reduction potential might indicate the occurrence of unwanted side reactions, which probably resulted in the degraded current efficiency. According to the above results, the deposition current efficiency affects the average

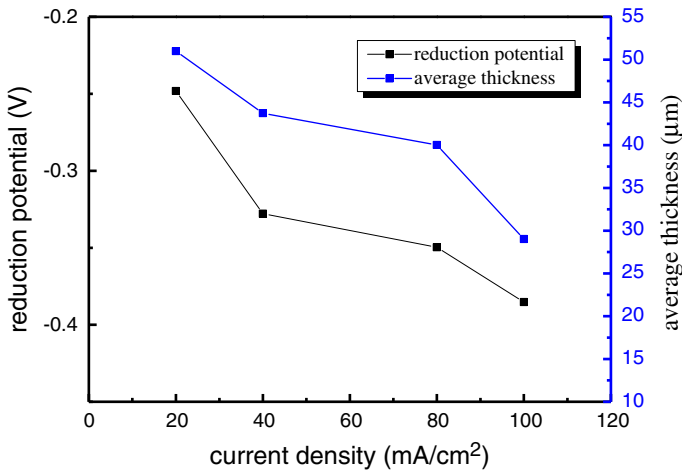


Fig. 5 Steady-state reduction potential and average thickness of Cu bumps deposited at different current densities

thickness of the Cu bumps, which decreased with increasing deposition current density.

Conclusions

We successfully used various electroplating modes for predefined Cu bumps without any barriers. The surface morphologies of the Cu bumps deposited at different current densities were observed by SEM. Cu bumps with smooth surfaces were obtained for deposition current density less than 100 mA/cm². The average thickness of the Cu bumps decreased with increasing deposition current density. According to these results, we suppose that Cu bumps with well-defined rectangular surface morphology can be obtained for deposition current density between 40 and 80 mA/cm².

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References

1. S. Nakamura, T. Mukai, M. Senoh, *Jpn. J. Appl. Phys.* **30**, L1998–L2001 (1991)
2. P. Schlotter, J. Baur, Ch. Hielscher, M. Kunzer, H. Obloh, R. Schmidt, J. Schneider, *Mater. Sci. Eng. B* **59**, 390–394 (1999)
3. M. Koike, N. Shibata, H. Kato, Y. Takahashi, *IEEE J. Sel. Top. Quantum Electron.* **8**, 271–277 (2002)
4. S.C. Hsu, C.Y. Liu, *Electrochem. Solid-State Lett.* **9**, 171–173 (2006)
5. M.-S. Lin, C.-F. Lin, W.-C. Huang, G.-M. Wang, B.-C. Shieh, J.-J. Dai, S.-Y. Chang, D.S. Wu, P.-L. Liu, R.-H. Horng, *Appl. Phys. Express* **4**, 062101-1–062101-3 (2011)

6. Z.S. Luo, Y. Cho, V. Loryuenyong, T. Sands, N.W. Cheung, M.C. Yoo, *IEEE Photonics Technol. Lett.* **14**, 1400 (2002)
7. H. Juyeon, Y.Y. Woo, Y.B. Ji, H.K. Sang, *Res. Chem. Intermed.* **40**, 57–65 (2014)
8. R.H. Horng, C.E. Lee, S.C. Hsu, S.H. Huang, C.C. Wu, C.Y. Kung, D.S. Wu, *Phys. Status Solidi* **201**, 2786–2790 (2004)
9. W.Y. Lin, D.S. Wu, K.F. Pan, S.H. Huang, C.E. Lee, W.K. Wang, S.C. Hsu, Y.Y. Su, S.Y. Huang, R.H. Horng, *IEEE Photonics Technol. Lett.* **17**, 1809–1811 (2005)
10. A.A. Rasmussen, J.A.D. Jensen, A. Horsewella, M.A.J. Somers, *Electrochim. Acta* **47**, 67–74 (2001)
11. P.V. Dudin, O.V. Reva, T.N. Vorobyova, *Surf. Coat. Technol.* **204**, 3141–3146 (2010)