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A multiple frequency clock generator using wide operation frequency range phase interpolator

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ABSTRACT

This paper presents a multiple frequency clock generator that is composed of the wide operation frequency range phase interpolator and the phase combiner. The wide operation frequency range phase interpolator is developed using a delay-time-adjustment phase interpolator (DTAPI) circuit with various oscillation frequencies for different clock domain applications. The phase combiner generates multiple clock frequencies through various phase combination inputs generated by the preceding proposed phase interpolators. The varying output transition delay time of the proposed DTAPI is the result of the various oscillation frequencies of the voltage-controlled oscillator. The test chip was fabricated in a 0.18 μm CMOS process with a 1.8 V supply voltage. The measured phase noise and power dissipation are −87.28 dBc/Hz at 1 MHz offset frequency from 88.8 MHz and 1.32 mW, −77.47 dBc/Hz and 2.06 mW from 797.8 MHz, respectively. The duty cycle error rate of the output clock frequency is less than 1.5%.

1. Introduction

The phase-locked loop (PLL) and delay-locked loop (DLL) often serve as clock generators to support multiple clock domains on the motherboards of personal computers (PCs) and notebooks (NBs) [1–5]. However, the clock frequencies of the I/O bus and various subsystems on the motherboard, including the memory system, Host bus and PCI bus, vary significantly. The operating frequency of the memory system in [5] can achieve an effective data rate of 1600 Mbps with data transferred on both edges of the clock. These tight timing requirements make it difficult for an internal on-chip clock to align with an external system clock. To release this tight timing requirement, the phase interpolator circuit is integrated in the clock generator [1–4,6–10] to generate additional phases to produce a high output frequency. The phase interpolator circuit can be implemented using analog [8–10] and digital [1,2,6,7] design techniques. Although an analog phase interpolation circuit has a high phase resolution and a high operating speed, its circuit architecture is complex and sensitive to variations in process, voltage, and temperature (PVT). However, digital phase interpolation circuits have simple and easy to design property. An inverter phase-blender circuit uses various inverter size ratios to achieve phase blending [1,6,7]. However, an inverter phase-blender circuit consumes a large short-circuit current and increases power dissipation. The short-circuit-current-suppression (SCCS) approach can eliminate the short-circuit power dissipation of a phase-blender circuit [2]. However, the charging current does not equal the discharging current because a SCCS phase interpolator has asymmetrical circuit architecture. Hence, the output duty cycle of the SCCS phase interpolator is not 50%. Thus, conventional analog and digital phase interpolation circuits cannot work at various frequencies. The transition delay time of the interpolated phase of conventional analog and digital phase interpolators is fixed between two input phases, and does not vary with the oscillation frequency. Hence, the two conventional interpolator circuit architectures are unsuitable for applications involving a wide range of oscillation frequencies.

This study proposes a new phase interpolator architecture with a wide range of operating frequencies to solve these problems and generate multiple frequency outputs. The transition delay time of the interpolated phase of the DTAPI can be adjusted by bias currents with various frequencies. Moreover, the DTAPI has an inherently symmetrical circuit architecture. Therefore, the proposed wide operation frequency range phase interpolator has two key advantages: (1) the transition delay time of the interpolated phase can be adjusted with varying frequencies; (2) the duty cycle of the output clock is approximately 50% because of the symmetrical circuit architecture.

The remainder of this paper is organized as follows. Section 2 introduces the circuit structure and operation principle of the proposed wide operation frequency range phase interpolator. Section 3 presents the simulation and experimental results. Finally, Section 4 offers a conclusion.

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2. The proposed wide operation frequency range phase interpolator

As shown in Fig. 1, the proposed multiple frequency clock generator consists of the wide operation frequency range phase interpolator and phase combiner. The wide operation frequency range phase interpolator consists of the modified VCO and DTAPIs. DTAPIs receive four phase signals (Φ_0, Φ_{90}, Φ_{180}, Φ_{270}) from the modified VCO to generate 12 output phases, $P_{0\text{-}11}$ which are sent to the succeeding phase combiner. Various output frequencies of the phase combiner is generated by the different selected phase sequence.

This section presents an analysis and discussion of the circuit architecture and associated operating principle of the proposed wide operation frequency range phase interpolator.

2.1. Basic conception of the DTAPI

Fig. 2a shows the basic design concept of the proposed wide operation frequency range phase interpolator. It consists of the modified VCO and the proposed DTAPI circuit. The proposed DTAPI receives two phase input signals, Φ_1 and Φ_2, whose phases are separated by the modified VCO. Four switched current sources are controlled to charge and discharge capacitance (C) load using simple NAND, NOR and a NOT gates. The internal charge/discharge currents sources of the DTAPI are mirrored and m and $(n–m)$ amplified to the current source I of the modified VCO. The value of I is related to the oscillation frequency of the modified VCO. The m and n can be set to provide the desired charge/discharge currents for generating the interpolated signal Φ_{12}. The duty cycle of the interpolated signal Φ_{12} is approximately 50% because of the symmetrical circuit architecture

2.1.1. Operation principle of the DTAPI with various oscillation frequencies under fixed m and n

When the oscillation frequency is high, the time interval T_{diff1} between the Φ_1 and Φ_2 input pulses is narrow and the currents $m \times I$ and $(n–m) \times I$ become large (Fig. 2b). The large charge and discharge currents produce a high slew rate (HSR) in the internal node Int_SR. In contrast, when the oscillation frequency is low, the time interval T_{diff2} between the Φ_1 and Φ_2 input pulses is wide and the currents $m \times I$ and $(n–m) \times I$ become small. Hence, the slew rate of the internal node Int_SR is low (LSR). In traditional phase interpolators [1,2,9,10], the transition delay time (T_{b1} or T_{b2}) of the interpolated signal Φ_{12} is fixed and cannot vary with the oscillation frequency. In the proposed DTAPI, the slew rates at different oscillation frequencies produce different transition delay times (T_{b1} or T_{b2}) of the interpolated signal Φ_{12} in generating the desired inter-rising edge. Therefore, the proposed DTAPI is suitable for applications involving a wide operating frequency range. For example, if $m=1$ and $n=2$, the interpolated signal Φ_{12} is always generated in the half of the time interval between Φ_1 and Φ_2 with various oscillation . Then, the delay T_{b1} is equal to $T_{diff1}/2$ and the delay T_{b2} is equal to $T_{diff2}/2$. Therefore, the transition delay time of the interpolated signal can be adjusted with various oscillation frequencies.

2.1.2. Operation principle of the DTAPI with various m and n under a fixed oscillation frequency

Fig. 3 shows the design concept and timing diagram of the DTAPI with various m and n implemented in the DTAmn block, where m and n are parameters amplified to the current source I of the modified VCO, respectively. In the DTAmn phase interpolator, $n \times I$ is the total current that flows along two current paths and $m \times I$ is the current that flows along one parallel current path. The term Δt is a delay time that can be adjusted according to m and n

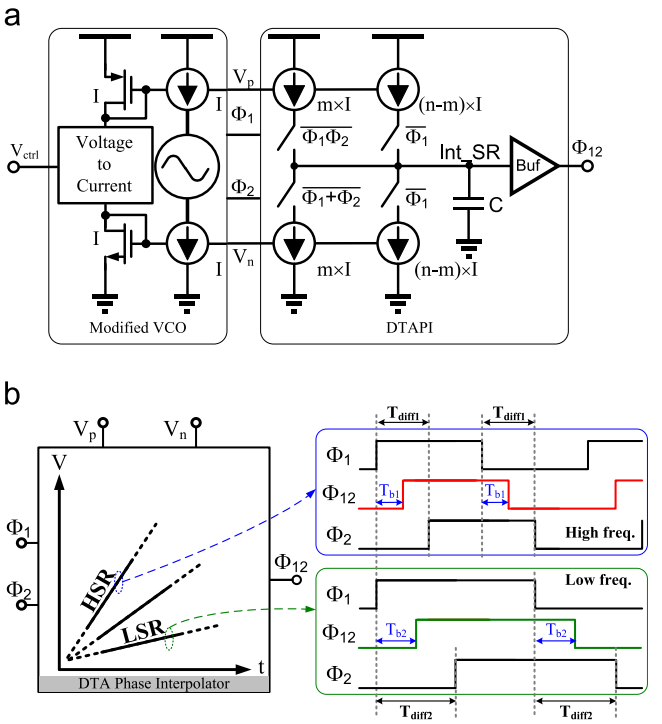


Fig. 2. (a) Basic design conception of the wide operation frequency range phase interpolator circuit, and (b) the timing diagram of the DTA phase interpolator with various oscillation frequencies.

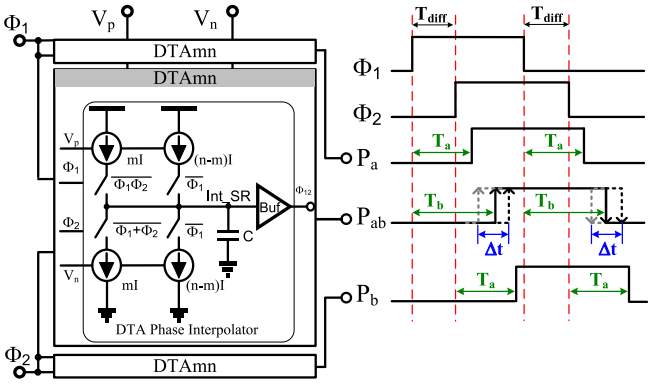


Fig. 3. Design conception and timing diagram of the DTA phase interpolator with various m and n.

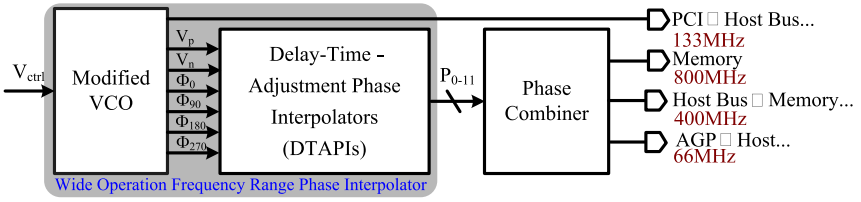


Fig. 1. Circuit architecture of the multiple frequency clock generator.

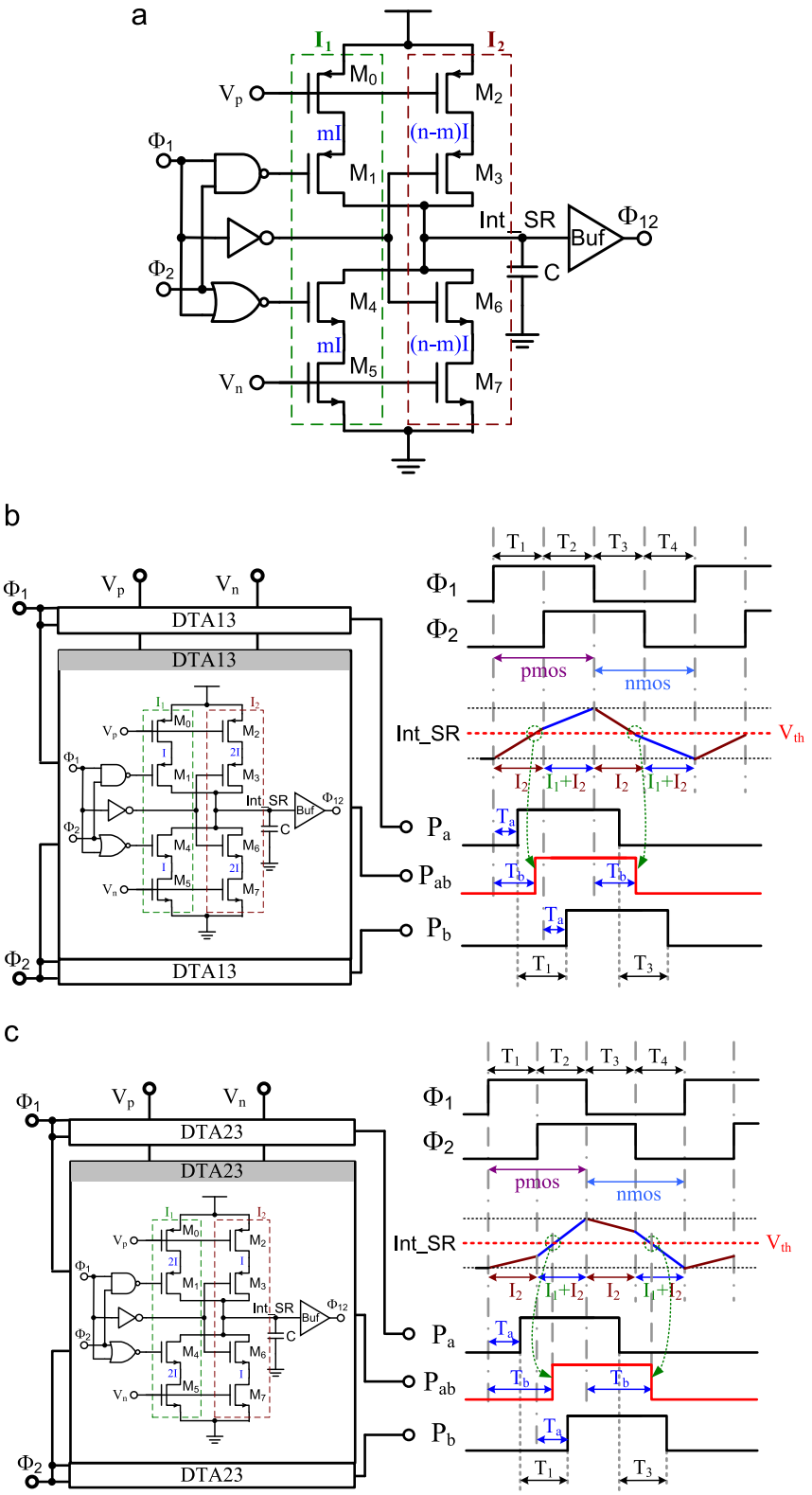


Fig. 4. (a) Circuit architecture of the DTA phase interpolator, (b) the timing diagram of the DTA13, and (c) the timing diagram of the DTA23.

under a fixed current I. Because of different values of m and n, the delay time of the interpolator can be expressed as

$$T_a = CV_{th}/nI \tag{1}$$

$$T_b = T_{diff} + (CV_{th} - m \times I\, T_{diff})/nI \tag{2}$$

$$= T_a + ((n-m)T_{diff}/n), (m < n) \tag{3}$$

where T_a is the delay time of the upper/lower DTAmn that directly passes Φ_1 and Φ_2 signals to generate output signals P_a and P_b. The term T_b is the delay time of the middle DTAmn, which blends the Φ_1 and Φ_2 signals to generate a interpolated signal P_{ab}. The term

T_{diff} is the time interval between the Φ_1 and Φ_2 input pulses. The V_{th} is the logic threshold voltage of the succeeding output buffer (Buf), and C is the capacitance for charging and discharging the voltage of the node Int_SR to V_{th}.

2.2. The circuit architecture and timing diagram of the DTAPI

Fig. 4 shows the DTAPI circuit architecture and timing diagram. Fig. 4a shows that the DTAPI consists of a NAND gate, a NOR gate, a NOT gate, and two current blocks I_1 and I_2. These logic gates are implemented to control four switches (M_1, M_3, M_4, and M_6) to charge or discharge capacitance (C) load. The charging and discharging current sources are controlled by the voltage signals V_p and V_n through MOS transistors M_0, M_2, M_5, and M_7. The value of I is related to the oscillation frequency of the modified VCO and m and $(n-m)$ are parameters amplified to the current source of I. This design uses two types of DTAmn in the wide operation frequency range phase interpolator. One is DTA13 ($m=1$ and $n=3$) and the other is DTA23 ($m=2$ and $n=3$).

2.2.1. The DTA13 phase interpolator

Fig. 4b shows the timing diagram of the DTA13. The currents of the DTA13 flowing in the blocks I_1 and I_2 are I and $2I$, respectively. During the time interval T_1, the PMOS transistor M_3 is turned on. The charging current $2I$ of the current block I_2 charges the capacitive node Int_SR. After a delay of T_b behind the leading phase Φ_1, the output signal P_{ab} rises from low to high at one third of the time interval T_1 when the voltage of the node Int_SR exceeds V_{th}. After Φ_2 rises from low to high, the PMOS transistor M_1 turns on in the time interval T_2. The charging current I of the current block I_1 also charges the same node. Hence, the pull-high slew rate of the node Int_SR increases at a total current of 3I. The NMOS transistor M_6 is turned on during the time interval T_3. The discharging current $2I$ of the current block I_2 discharges the capacitive node Int_SR. After a delay of T_b behind the leading phase Φ_1, the output signal P_{ab} falls from high to low at one third of the time interval T_1 when the voltage of the node Int_SR falls over V_{th}. After Φ_2 falls from high to low, the NMOS transistor M_4 is turned on in the time interval T_4. The discharging current I of the current block I_1 also discharges the same node. Hence, the pull-low slew rate of the node Int_SR increases at a total current of $3I$. The output signal achieves a duty cycle of 50% because the proposed DTA13 circuit has a symmetrical architecture.

2.2.2. The DTA23 phase interpolator

Fig. 4c shows the timing diagram of the DTA23. The currents of the DTA23 ($m=2$ and $n=3$) flow in the blocks I_1 and I_2 are $2I$ and I, respectively. During the time interval T_1, the PMOS transistor M_3 is

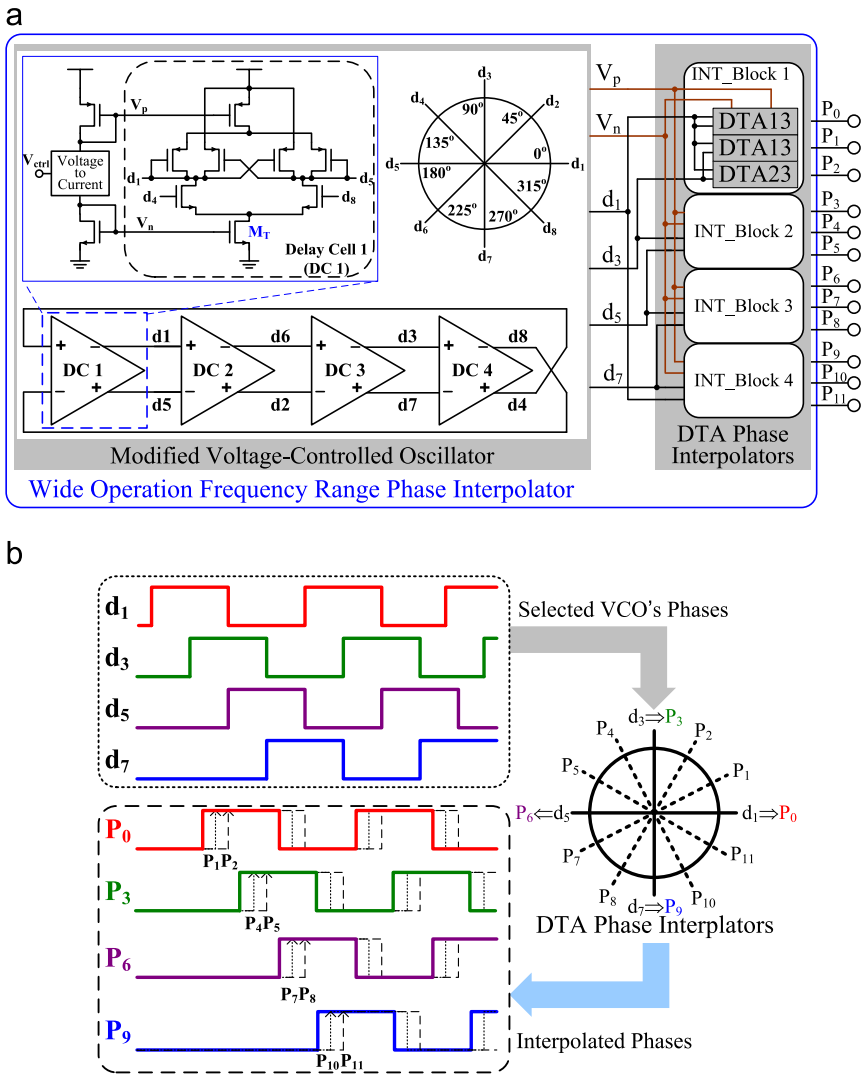


Fig. 5. (a) Circuit architecture of the wide operation frequency range phase interpolator, and (b) the operation conception and timing diagram of the wide operation frequency range phase interpolator.

turned on. The charging current I of the current block I_2 charges the capacitive node Int_SR. After Φ_2 rises from low to high, the PMOS transistor M_1 is turned on in the time interval T_2. The charging current $2I$ of the current block I_1 also charges the same node. Hence, the pull-high slew rate of the node Int_SR increases at a total current of $3I$. After a delay of T_b behind the leading phase Φ_1, the output signal P_{ab} rises from low to high at two thirds of the time interval T_1 when the voltage of the node Int_SR exceeds V_{th}. Similarly, the pull-low slew rate of node Int_SR increases at a total current of $3I$ in the time interval T_4. After a delay of T_b behind the leading phase Φ_1, the output signal P_{ab} falls from high to low at two thirds of the time interval T_4 when the voltage of node Int_SR falls below V_{th}. The output signal achieves a duty cycle of 50% because the proposed DTA23 circuit has a symmetrical architecture.

2.3. The circuit architecture and timing diagram of the wide operation frequency range phase interpolator

Fig. 5 shows that the wide operation frequency range phase interpolator consists of the modified VCO and the DTAPIs. Fig. 5a shows the modified four-stage differential VCO structure and DTAPIs. Adding the NMOS transistor M_T to the delay cell [11] improves the linearity of the VCO. The oscillation frequency of the modified VCO is depends on the control voltage V_{ctrl} and VCO's eight output phases are evenly spaced between d_1 and d_8. Therefore, each phase difference is 45° (=360°/8). The $d_1(\Phi_0)$, $d_3(\Phi_{90})$, $d_5(\Phi_{180})$, and $d_7(\Phi_{270})$ signals of the modified VCO output are selected as the input signals of the DTAPIs. The DTAPIs have four interpolator circuit blocks (INT_Blocks 1–4). Each INT_Block consists of two DTA13 phase interpolators and one DTA23 phase interpolator. Therefore, the DTAPIs generate twelve phases for the phase combiner.

Fig. 5b shows the operation concept and timing diagram of the wide operation frequency range phase interpolator. As described in the preceding paragraph, DTA13 and DTA23 generate interpolated phases at one-third (P_1, P_4, P_7, and P_{10}) and two-thirds (P_2, P_5, P_8, and P_{11}) of the time intervals between the interpolated P_0, P_3, P_6, and P_9 signals. The first DTA13 of each INT_Block directly passes d_1, d_3, d_5, and d_7 signals to generate output signals P_0, P_3, P_6, and P_9 without any interpolation. Therefore, the four output phases of the modified VCO generate interpolated $P_i(i=0–11)$ signals through DTAPIs. Hence, each phase difference is 30° (=360°/12).

3. Simulation and experimental results

The proposed wide operation frequency range phase interpolator and phase combiner were implemented in a 0.18 μm 1P6M CMOS process. Fig. 6 shows the interpolated output waveforms P_0–P_3 of the INT_Block 1 at oscillation frequencies of 100 MHz and 133 MHz, respectively. The phase difference of each interpolated phases is 833.3 ps at 100 MHz and 626.6 ps at 133 MHz, respectively. As shown in Fig. 7, the phase difference error ($\triangle T_{err}$) is normalized to ideal phase difference (T_{phi}) between two successive phases with various oscillation frequencies. As a result, the phase difference error is less than 2%. As Fig. 1 shows, various clock frequency outputs can be generated by combining the phase interpolator with various phase combination circuits [9,10]. Table 1 shows various combinations of x/y and its relatively different phase sequences for the phase combiner. The frequency relationship between the output of the phase combiner and the

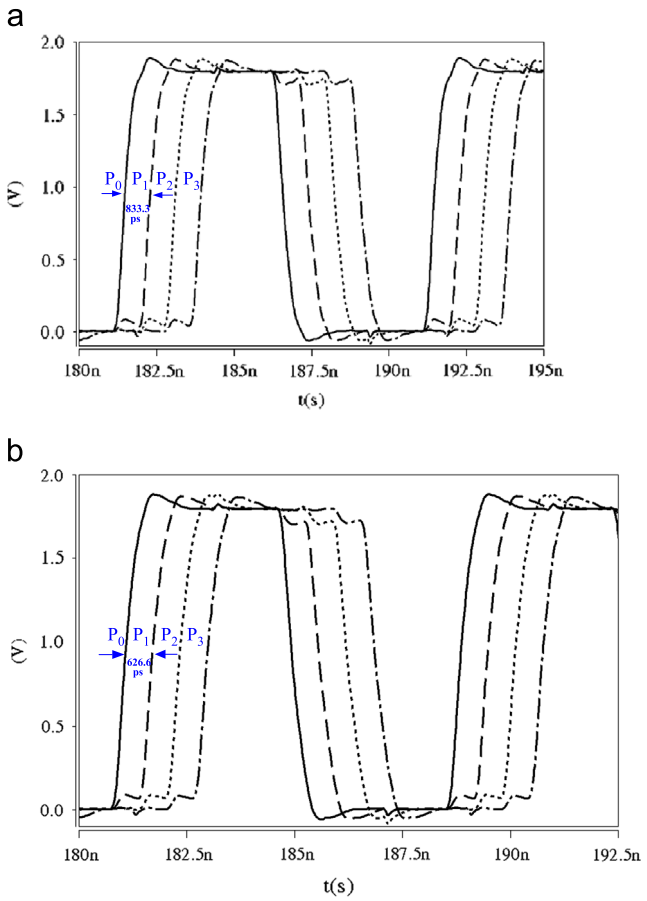


Fig. 6. Simulation output waveforms of the INT_Block 1 at (a) 100 MHz and (b) 133 MHz.

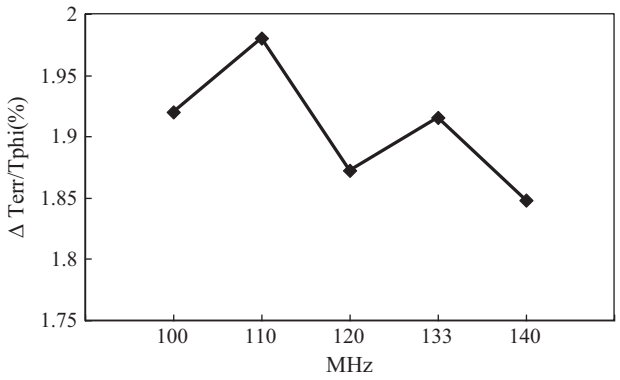


Fig. 7. Normalized phase difference error with various oscillation frequencies.

Table 1
Various combinations of x/y and its relatively different phase sequences for the phase combiner.

x/y	Phase sequences
6/1	$P_0 \rightarrow P_1 \rightarrow P_2 \rightarrow P_3 \rightarrow P_4 \rightarrow P_5 \rightarrow P_6 \rightarrow P_7 \rightarrow P_8 \rightarrow P_9 \rightarrow P_{10} \rightarrow P_{11} \rightarrow P_0 \ldots$
3/1	$P_0 \rightarrow P_2 \rightarrow P_4 \rightarrow P_6 \rightarrow P_8 \rightarrow P_{10} \rightarrow P_0 \ldots$
2/1	$P_0 \rightarrow P_3 \rightarrow P_6 \rightarrow P_9 \rightarrow P_0 \ldots$
3/2	$P_0 \rightarrow P_4 \rightarrow P_8 \rightarrow P_0 \ldots$
6/5	$P_0 \rightarrow P_5 \rightarrow P_{10} \rightarrow P_3 \rightarrow P_8 \rightarrow P_1 \rightarrow P_6 \rightarrow P_{11} \rightarrow P_4 \rightarrow P_9 \rightarrow P_2 \rightarrow P_7 \rightarrow P_0 \ldots$
6/7	$P_0 \rightarrow P_7 \rightarrow P_2 \rightarrow P_9 \rightarrow P_4 \rightarrow P_{11} \rightarrow P_6 \rightarrow P_1 \rightarrow P_8 \rightarrow P_3 \rightarrow P_{10} \rightarrow P_5 \rightarrow P_0 \ldots$
3/4	$P_0 \rightarrow P_8 \rightarrow P_4 \rightarrow P_0 \ldots$
2/3	$P_0 \rightarrow P_9 \rightarrow P_6 \rightarrow P_3 \rightarrow P_0 \ldots$
3/5	$P_0 \rightarrow P_{10} \rightarrow P_8 \rightarrow P_6 \rightarrow P_4 \rightarrow P_2 \rightarrow P_0 \ldots$
6/11	$P_0 \rightarrow P_{11} \rightarrow P_{10} \rightarrow P_9 \rightarrow P_8 \rightarrow P_7 \rightarrow P_6 \rightarrow P_5 \rightarrow P_4 \rightarrow P_3 \rightarrow P_2 \rightarrow P_1 \rightarrow P_0 \ldots$

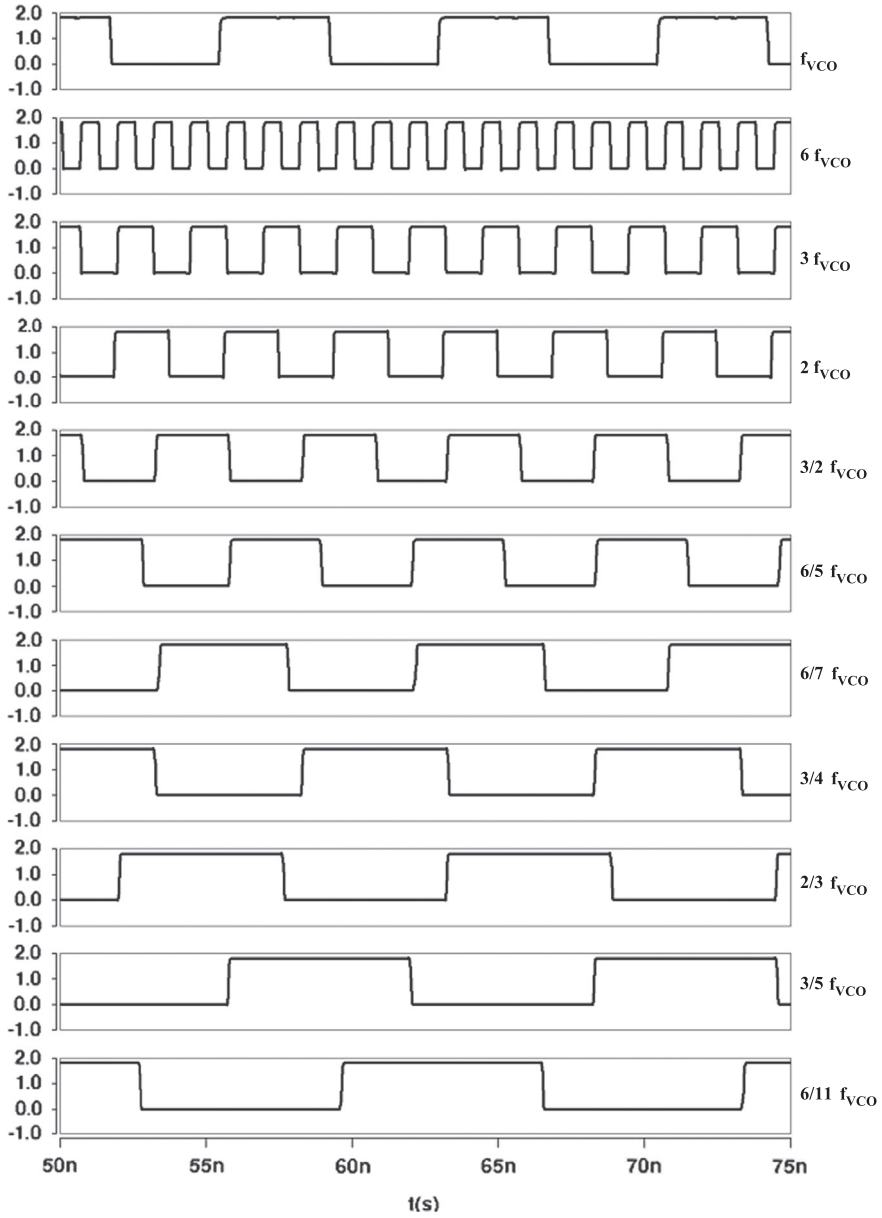


Fig. 8. Simulation output waveforms of the multi-frequency outputs.

frequency (f_{vco}) of the modified VCO can be expressed as

$$\text{Output frequency of the phase combiner} = \frac{x}{y} \times f_{VCO} \quad (4)$$

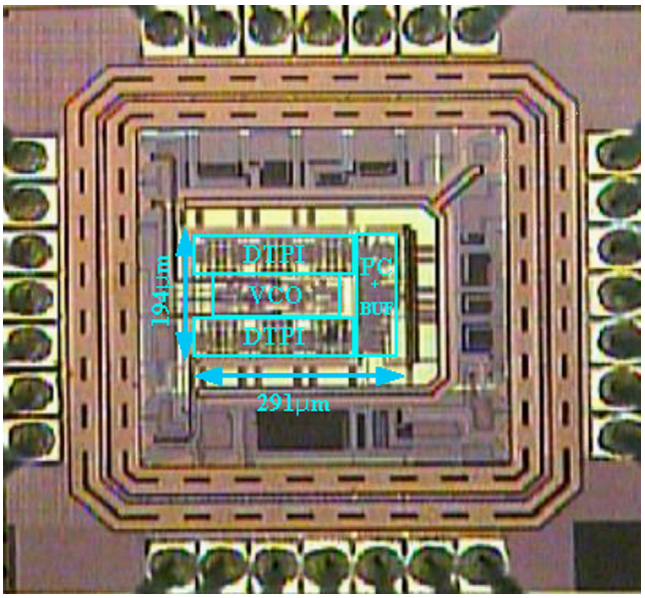
where x and y are multiplied and divided parameters, respectively. This study implements the fractional and integral output frequencies of the phase combiner using the methods in [12,13], respectively. Hspice simulation results demonstrate that the oscillation frequencies of the modified VCO range from 100 MHz to 150 MHz. Fig. 8 shows the simulation output waveforms of the multi-frequency outputs. When the modified VCO oscillation frequency (f_{vco}) is 133 MHz, the output frequencies of 6/1, 3/1, 2/1, 3/2, 6/5, 6/7, 3/4, 2/3, 3/5, and 6/11 times f_{vco} are 799.56 MHz, 399.78 MHz, 266.52 MHz, 199.89 MHz, 159.91 MHz, 114.22 MHz, 99.95 MHz, 88.84 MHz, 79.96 MHz and 72.69 MHz, respectively. As Table 2 shows, the duty cycle error rates of the output clock frequencies are between 0.1% and 1%. The simulation results of the proposed clock generator with PVT variations are shown in Table 3. There are three simulation conditions: (1) the best case is FF process, 1.98 V ($=1.8+1.8\times10\%$) and -20°; (2) the typical case is TT process, 1.8 V and 27°; (3) the worst case is SS process, 1.62 V ($=1.8-1.8\times10\%$) and 85°. According to simulation results, the output frequency variation is less than 4%.

Table 2
Simulation results of duty cycle.

Output frequencies (MHz)	Duty-cycle (%)
$f_{VCO}=133.26$	50.1
$6\times f_{VCO}=799.56$	50.2
$3\times f_{VCO}=399.78$	49.7
$2\times f_{VCO}=266.52$	50.3
$3/2\times f_{VCO}=199.89$	49.5
$6/5\times f_{VCO}=159.91$	49.6
$6/7\times f_{VCO}=114.22$	50.1
$3/4\times f_{VCO}=99.95$	49.8
$2/3\times f_{VCO}=88.84$	50.1
$3/5\times f_{VCO}=79.96$	49.9
$6/11\times f_{VCO}=72.69$	51

Table 3
Simulation results of the proposed clock generator.

f_{vco}=133 MHz						
	$2/3 \times f_{vco}$			$6/1 \times f_{vco}$		
Conditions	SS_1.62 V _85°C	TT_1.8 V _27°C	FF_1.98 V _−20°C	SS_1.62 V _85°C	TT_1.8 _27°C	FF_1.98 V _−20°C
Output frequency (MHz)	86.12	88.84	92.39	768.43	799.56	820.55
Duty cycle (%)	49.6	50.1	50.2	49.5	50.2	50.3
RMS Jitter (ps)	25	22	20	16	14	12
Power dissipation (mW)	1.1	1.2	1.3	1.8	2.0	2.3



*PC+BUF: Phase Combiner + Output Buffer

Fig. 9. Microphotograph of the multiple frequency clock generator.

Fig. 9 shows the die photograph of the multiple frequency clock generator. The total area of the proposed clock generator, including VCO, DTPI, PC (Phase Combiner) and output buffer (BUF), is 291 μm × 194 μm. However, the area of one DTA13 is only 25 μm × 20 μm. Fig. 9 shows the measured output frequencies spectra of the proposed multi-frequency outputs circuit. As shown in Fig. 10a and b, the measured frequency spectra of output frequencies are 88.8 MHz (=2/3 × 133 MHz) and 797.8 MHz (=6/1 × 133 MHz) at f_{vco}=133 MHz, respectively. The measured phase noises are −87.28 dBc/Hz at 1 MHz offset frequency from 88.8 MHz and −77.47 dBc/Hz from 797.8 MHz, respectively. Table 4 shows the measure results of the proposed clock generator and performance comparisons with previous works [2–8]. According to previous works, the phase interpolator circuit is integrated into PLL/DLL [3,6,7], CDR [8] and other macro circuit [2,4]. Hence, the performance of the phase interpolator cannot be extracted from these papers along. However, some parameters of Table 4 deserve to be mentioned. The proposed work has two important properties: (1) the transition delay time of the interpolated phase can be adjusted with varying oscillation frequencies; (2) it can generate simultaneously multiple frequency outputs. Previous works do not have these properties. Besides, the proposed clock generator only includes modified VCO, phase interpolator and phase combiner. Therefore, the power dissipation of the proposed clock generator is 1.32 mW at 88.8 MHz and 2.06 mW at 797.8 MHz, respectively. As measured results, the duty cycle error rate of the output clock

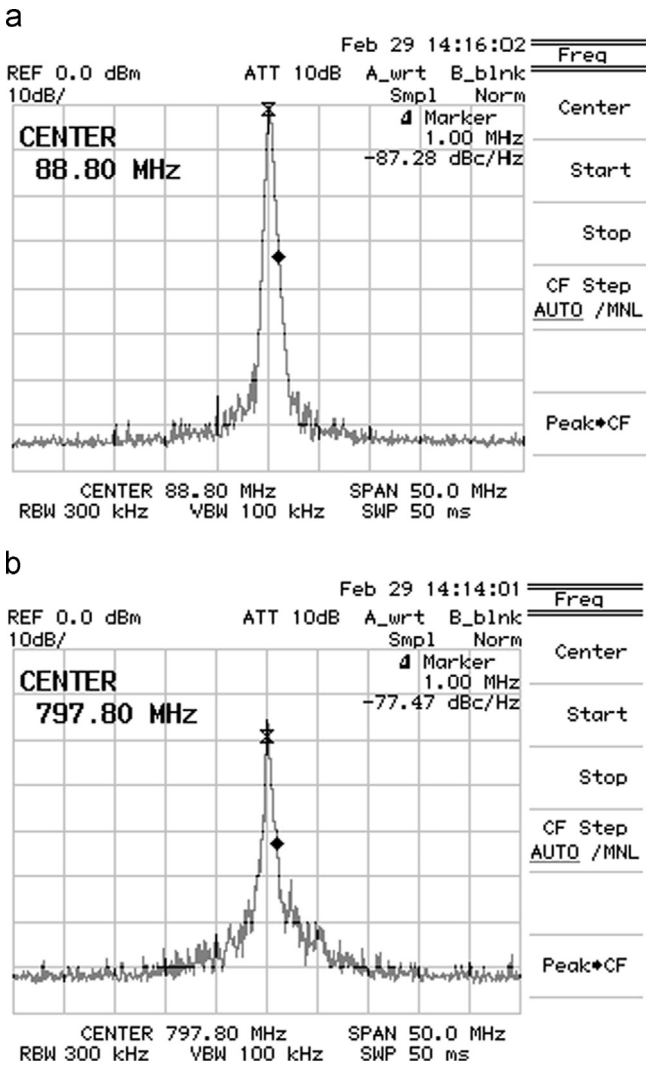


Fig. 10. Measured frequency spectra of the output frequency (a) 88.8 MHz (=2/3 × 133 MHz) and (b) 797.8 MHz (=6/1 × 133 MHz).

frequency is less than 1.5% and the output frequency variation is smaller than 1%. Therefore, the proposed clock generator is suitable for digital system applications.

4. Conclusion

This study demonstrates a phase interpolator with a wide range of operating frequencies for using in multi-frequency outputs. At various oscillation frequencies of the modified VCO, the different slew rates of the DTAPI produce various transition delay

Table 4
Performance comparisons with previous works.

	[2]	[3]	[4]	[6]	[7]	[8]	**This work**
Technology (μm)	0.25	0.1	0.13	0.18	0.18	0.25	**0.18**
Supply voltage (V)	2.5	1	1.2	1.8	1.8/3.3	2.2–2.8	**1.8**
Variable oscillation frequency range	No	No	No	No	No	No	**Yes**
Multiple frequency outputs	No	No	No	No	No	No	**Yes**
Output frequency range (Hz)	1.2 G	650 M	1 G	2.4 G	2.001 G	25 M–100 M	**72.69 M–799.56 M (@f_{vco}=133 M)**
Phase noise (@1 MHz offset)	NA	NA	NA	NA	−78.33 dBc/Hz@1 kHz	NA	**−87.28 dBc/Hz@88.8 MHz −77.47 dBc/Hz@797.8 MHz**
RMS jitter (ps)	75.47	6*	4.1	2.81	NA	250	**18@799.56 MHz**
Power (mW)	15[a]	38[b]	15[c]	36[d]	35.3[e]	44[f]	**1.32@88.8 MHz 2.06@797.8 MHz**

(*) Peak-to-peak jitter.
[a] Multiphase clock multiplier.
[b] DLL.
[c] Digital-to-phase converter.
[d] PLL.
[e] PLL.
[f] CDR.

times when generating interpolated signals. The interpolated signal rises at different delay times between two selected phases with various m and n parameters. Hence, the phase combiner can generate different clock frequencies using different combinations of phases. Measurements show that the phase noise and power dissipation are −87.28 dBc/Hz at 1 MHz offset frequency from 88.8 MHz and 1.32 mW, −77.47 dBc/Hz and 2.06 mW from 797.8 MHz, respectively. The duty cycle error rate of the output clock frequency is less than 1.5%. Therefore, the proposed multi-frequency outputs based on a phase interpolator with a wide range operating frequencies is suitable for using in SoC applications.

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