Implemented LDO Chip With Output Capacitors Free

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Abstract. In this paper the process of implementing a low dropout regulator (LDO) chip is presented; it is using uses Taiwan Semiconductor TSMC's Manufacture Inc. 0.35um 2P4M process. The circuit designed with the described process can be is operated at 3-5V input voltage to generate 2.5V output voltage. Maximum output current can be running up to 200mA. This LDO is implemented without placing output capacitors to reduce BOM (Bill of Material) cost and stable between 0~200mA loading current and the chip is stable when the loading current is in the range 0~200mA. [8] The new proposed LDO chip can be implemented in the handheld mobile devices, battery powered equipment, wireless devices, cordless phones, or PC peripherals.

Introduction

Shown in Fig. 1. is the functional block diagram of a LDO [1-4]. It can supply 150mA output current when the output voltage is set at 2.5V. The bandgap voltage reference circuit has a fix reference voltage which is independent of the variations of the supply voltage and the environment temperature. In order to generate an output voltage with great precision it includes an error amplifier in the LDO to compensate the voltage difference between the input reference voltage and the output feedback voltage. The error amplifier controls the pass element (PMOS). The pass element acts as a resistor with variable resistance to the control supply voltage through the output voltage. The resister ratio of R1 and R2 decides the level of the output voltage; the output voltage can be found as (Vref*(R1+R2))/R2.

The proposed chip circuit consists of bandgap voltage reference circuit, error amplifier circuit and power PMOS transistors block. The circuit design process, the theoretical analysis of the chip characteristics, the data measured and the circuit performance simulation result are all discussed detailed in this paper.

Circuit Desigh

Bandgap Voltage Reference Circuit. The bandgap voltage reference circuit is implemented in VLSI structure; it can generate a stable output voltage that is independent of the variations of the supply voltage and the environment temperature [2-3].

The proposed bandgap circuit has the structure as shown in Fig. 2. The output voltage of the circuit shown in Eq.(5). The voltage variation of Vref with respect to temperature has the simulated result as shown in Fig.6. The temperature coefficient of the proposed bandgap circuit at supply voltage of 5V is about 31ppm/°C.
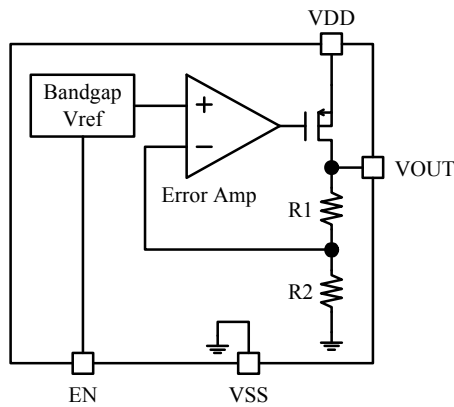
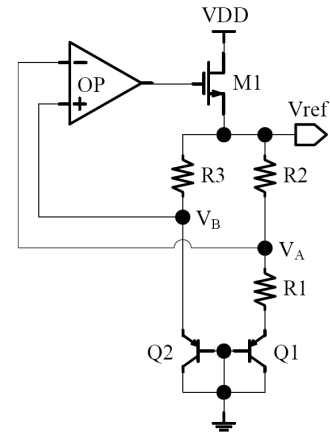Fig. 1 The architecture of the LDO.

Fig. 2 The proposed Bandgap circuit.

The variation of Vref appears to vary in a parabolic form it has the largest variation 3.2mV when the temperature varies from -40°C to 125°C. The voltage variation of the proposed bandgap circuit is about 0.2ppm/V at temperature of 25°C. When the supply voltage varies from 3 V to 6 V the Vref has the largest variation of 6.2uV.

Operational Amplifier. Shown in Fig. 3. is a two stage operational amplifier [2]. The simulated frequency response of the operational amplifier. The open loop gain has value 74dB and its corresponding phase is 71 deg at the supply voltage of 5V.

Error Amplifier. The proposed error amplifier circuit with operational transconductance amplifier (OTA) has a structure as shown in Fig. 4. [2-3]. The OTA is an operational amplifier without including output buffer.

LDO Circuit. As shown in Fig. 1. is the proposed functional block diagram of our LDO circuit. It results in constant output voltage without implementing any output capacitors [6]. It shows some important characteristics in the designed LDO circuit, e.g. it is load regulation, line regulation, PSRR, and stable etc.
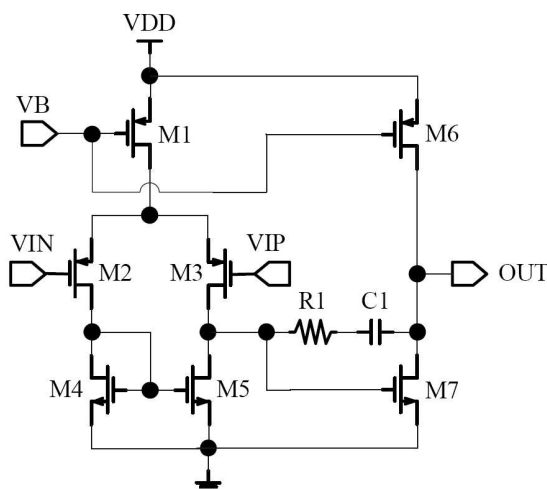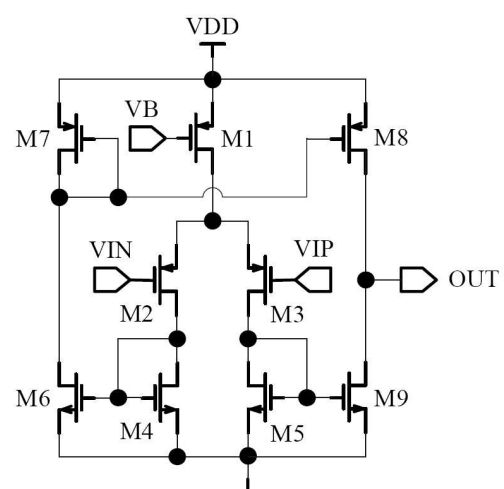

Fig. 3 A two stage operation amplifier.

Fig. 4 The proposed error amplifier circuit.

We then determine the extra amount of capacitance a LDO circuit can be suffered in order to maintain the circuit's stability. The frequency response of the LDO circuit is shown in Fig. 5. [3-4], In the Fig. 5., (a) is open loop transfer function gain response and (b) is open loop transfer function phase response. The PM is phase margin of LDO at unit gain frequency.

P1 is the first pole of LDO. P2 is the second pole of LDO. In the design, we can set up the P1 within the LDO unity-gain frequency bandwidth while the P2 is selected out of the LDO unity-gain frequency bandwidth to make LDO stable.

Circuit Layout

The circuit layout is provided to make mask, and the foundry uses the completed mask to fabricate IC. The resulted photographic layout of our IC is shown in Fig. 6; it has die size with pads of 0.6 mm x 0.6 mm.

Measurement Results

A designed LDO chip is fabricated and packaged, its input power supply is selected at 5V and the output loading current is running from 0 to 200mA. As shown in Fig. 7. is the loaded transient response of the designed LDO chip. When the oscilloscope is ac coupled and the load regulation is with 20 mV it has the output waveform as shown at the oscilloscope channel 3 while at channel 4 it shows the output current waveform. In Fig. 8., it shows the LDO frequency response. The LDO DC gain is around 50 dB; it has phase margin of 55°at the unity-gain of LDO response. We put the RC circuit between VDD and Bandgap circuit, then the LDO can approve PSRR. The LDO has bandwidth around 65MHz and at 10 kHz its PSRR is 80dB as shown in Fig. 9.[5]. The dropout voltage is defined as the deviation voltage between the supply voltage and the output voltage when the supply voltage (red line) various from 2.5 to 3.2V when the output voltage (blue line) reaches 2.5V, it has dropout voltage of 513mV. The LDO output voltage (Vout) vs. temperature curve show in Fig. 10. The measured LDO circuit performance is summarized in Table 1. We Comparison this work LDO with previously is summarized in Table 1.
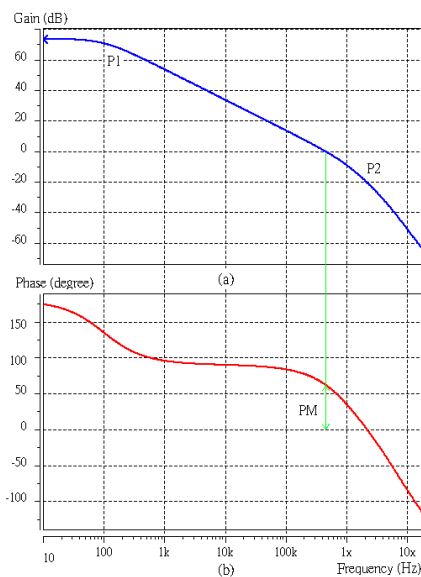

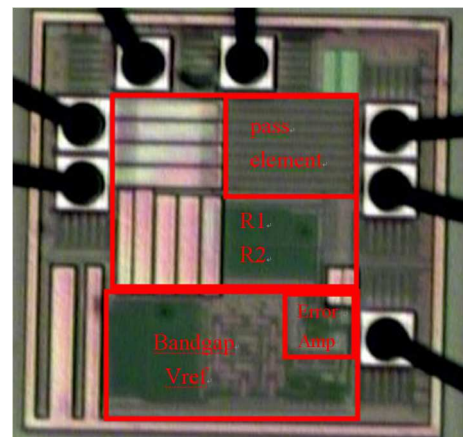Fig. 5 The simulated frequency response of LDO chip.

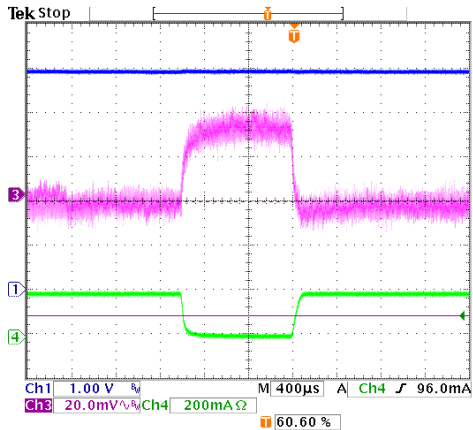Fig. 6 The photographic layout of LDO chip.

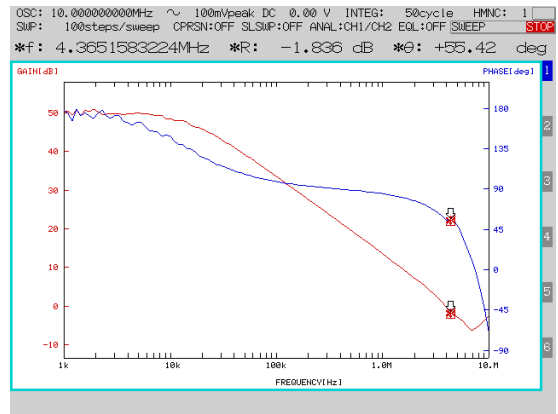Fig. 7 Measured load transient response of LDO chip.
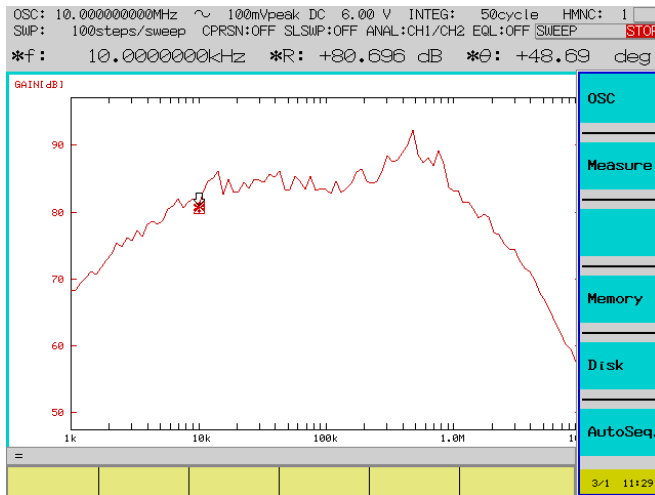

Fig. 8 Measured frequency responses of LDO chip.
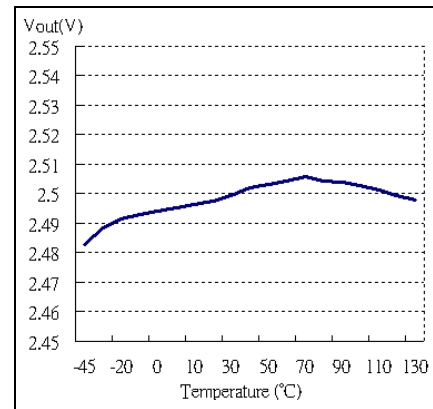

Fig. 9 Measured PSRR of LDO chip.

Fig. 10 Measured LDO Vout vs. temperature.

Table 1 LDO Performance Comparison with previously reported

	(a) [7]	(b) [8]	(c) [9] simulation	This work
Year	2004	2009	2009	
Technology (um)	0.5	0.35	0.6	0.35
Supply Voltage (V)	3~7	1.73~5	3.5~5	3.1V~5
Output Voltage (V)	2.3~2.5	1.5	3.3	2.497
$I_{out\,(max)}$ (mA)	150	100	100	200
Quiescent Current (uA)	90	40	36.7	28.3
Line Regulation (mV/V)	1.47	2.5	1	0.916
Load Regulation (mV/mA)	30	0.16	0.17	0.267
Dropout Voltage (V)	0.446	0.230	NA	0.513
PSRR	NA	71dB	NA	80.7
Cout	no	no	no	no
Area (mm^2)	NA	0.14	no	0.12

Conclusion

In this paper we design a LDO to fabricate a chip. In the design we used error amplifier to control the pass element so as to maintain a constant output voltage when the loading varies from 0mA to 200mA. The LDO work without any output capacitor, high PSRR and less chip area.

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