Low Power Sigma Delta Modulator with Dynamic Biasing for Audio Applications

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***Abstract*—In this paper, a low power sigma delta modulator with dynamic biasing technique is presented. According to the analysis of the operations of the switched-capacitor integrator, the folded-cascode operational amplifier can be designed with optimized biasing currents in three different phases to reduce power dissipations. The total power saving is 20% of the general one. A prototyping fourth order single-bit MASH 2-2 sigma delta modulator is designed with the technique of dynamic biasing to achieve dynamic range of 95dB and peak signal-to-noise-and-distortion-ratio of 93dB. The experimental circuit is designed in 0.35µm 2P4M CMOS technology. The chip area is 3.11mm^2, and the power dissipation is only 5mW from a supply voltage of 3V.**

I. INTRODUCTION

Recently, with the popularity of the portable devices, the low power devices became a very important topic. To reduce power consumption is to extend the life of the battery and to bring the convenience to the users. The sigma delta modulator (SDM) based on switched-capacitor (SC) circuits is well suited for many applications. Since the SC circuits allow for very sophisticated, accurate, and tunable analog circuits to be manufactured without using resistors in CMOS process, it becomes the most popular approach for completing analog signal processing. Therefore, the proposed multi-stage-noise-shaped (MASH) 2-2 SDM is composed of SC circuits. In the traditional design, the operational amplifier (opamp) in SC circuits usually uses a fixed biasing current in every phase. According to the analyses of the SC circuits in the next sections, the required biasing currents in different phases may be changeable, and thus the dynamic biasing method is based on such idea to reach the feature of low power. The dynamic bias circuit has been proposed several years ago [1], [2]. The SC circuits have been analyzed to obtain the formula of the optimized currents in different phases. According to the derived formula, the optimized currents can be obtained in the sampling phase, the slewing phase, and the settling phase respectively. The dynamic biasing circuits realize the current changing in the three phases with only some extra switches added to switch the specific currents. The resolution of the audio signal locates in the vicinity of 16 bits and the required bandwidth is 25 kHz. Several SDM analog to digital converters (ADCs) with 16-bit resolution are proposed in [3], [4] and [5]. These ADCs all operate with fixed biasing currents and the power is wasted in the view of dynamic biasing technique. In this design, significant power saving has been achieved by the dynamic biasing technique.

The rest of this paper is organized as follows: Section II discusses the operations of the dynamic biasing current of the SC integrator. In Section III, the implementation of the circuits and system is discussed. In Section IV, the simulation results and the comparison with other works are presented. Finally, a brief conclusion is given in Section V.

II. ANALYSIS OF THE DYNAMIC BIASING INTEGRATOR

A SDM is usually realized with SC circuits, which are composed of switches, capacitors and opamps. Generally, the opamps are the components consuming the most power in SC circuit. Fig. 1 shows a general SC integrator [6]; its operation can be separated into three phases: sampling phase, slewing phase, and settling phase.

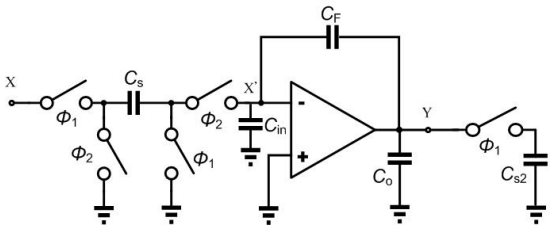

Figure 1. The general SC circuit.

A. Sampling Phase (φ1)

In this paper, the equivalent circuits can be depicted as Fig. 2. The equivalent capacitor ($C_{eq,\ \varphi 1}$) and the feedback factor ($\beta_{\varphi 1}$) can be derived as (1) and (2). In phase φ1, the opamp is almost inactive. The SC circuit only samples the input signal to C_s and charges the next stage C_s. It only needs a small current for the operation of the opamp. Owing to that C_{in} is smaller than C_F, the feedback factor value is very close to 1 during φ1.

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$$C_{eq,\varphi 1} = \frac{C_F \cdot C_{in}}{(C_F + C_{in})} + C_o + C_{s2} \quad (1)$$

$$\beta_{\phi 1} = \frac{X'_{\phi 1}}{Y_{\phi 1}} = \frac{C_F}{C_F + C_{in}} \quad (2)$$

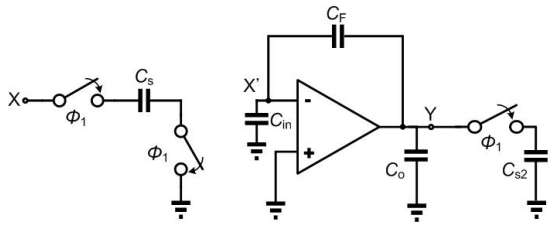

Figure 2. The SC integrator during the sampling phase (φ1).

B. Slewing and Settling Phases (φ2)

In these two phases, the equivalent circuits can be depicted as Fig. 3. We can derive the equivalent capacitor ($C_{eq,\varphi 2}$) and the feedback factor ($\beta_{\varphi 2}$) as (3) and (4). In phase *φ2*, the opamp begins to activate. The SC circuits evaluate the signal and C_s starts to redistribute charge. Owing to that C_{in} and C_S are smaller than C_F, but cannot be omitted, the feedback factor is smaller than 1 during *φ2*.

$$C_{eq,\varphi 2} = \frac{(C_s + C_{in}) \cdot C_F}{(C_s + C_{in}) + C_F} + C_o \quad (3)$$

$$\beta_{\phi 2} = \frac{X'_{\phi 2}}{Y_{\phi 2}} = \frac{C_F}{C_F + C_{in} + C_S} \quad (4)$$

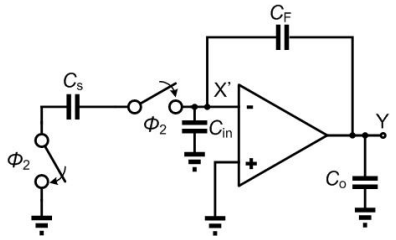

Figure 3. The SC integrator during the slewing and settling phases (φ2).

According to the relationship between the closed-loop and the opened-loop as (5), the $f_{u,OL}$ can be defined by $f_{u,CL}$, where $f_{u,CL}$ and $f_{u,OL}$ denote the unit-gain-bandwidth (GBW) of the closed-loop and the opened-loop, respectively. $f_{u,OL}$ can also be described as the GBW of the opamp.

$$f_{u,CL} = \beta \cdot f_{u,OL} \quad (5)$$

When the clock phase operates in this phase (φ2), the SR and GBW are the main considerations of the opamp. Assuming that the activation of the slewing phase has to complete during a ratio of the switching time, which is denoted as *b*, (7) and (8) can be used to determine the time of the slewing and settling phase. $T_{slewing}$ and $T_{settling}$ are the times of the slewing and the settling phases, respectively, and the sum of them is $T_s/2$. In order to obtain the optimized current, it is assumed that the switching time is changeable, where T_S is the period of clock; V_S is the step voltage, and $C_{eq,\varphi 2}$ is the equivalent capacitance of the opamp.

$$T_{slewing} = \frac{1}{b} \times \frac{T_S}{2} \quad (6)$$

$$T_{settling} = \left(1 - \frac{1}{b}\right) \times \frac{T_S}{2} \quad (7)$$

$$I_{slewing} = \frac{V_s}{T_{slewing}} \cdot C_{eq,\varphi 2} \quad (8)$$

The accuracy, *a*, with which the required GBW of the opamp can be determined, is described as (9) [7], where τ denotes the time constant of the integrator. In (5), owing to that $1/\beta$ is always larger than 1, the needed GBW of the opamp will be larger than that of the integrator. From the general formula of GBW of the opamp, the GBW is positive proportional to the transconductance of the input pair. With the derived transconductance, the current of the settling phase can be calculated from (10). On the other hand, the current in the sampling phase is similar to that in the settling phase. According to the same formula of GBW, the current of the sampling phase can be derived as (11).

$$e^{-\frac{t}{\tau}} \le a \quad (9)$$

$$I_{settling} = GBW_{OP(\varphi 2)} \cdot \pi \cdot C_{eq,\varphi 2} \cdot (\Delta V) \quad (10)$$

$$I_{sampling} = GBW_{OP(\varphi 1)} \cdot \pi \cdot C_{eq,\varphi 1} \cdot (\Delta V) \quad (11)$$

C. Dynamic Biasing Technique

According to (8), (10), and (11), the curves of the switching time ratio, *b*, versus the currents can be plotted during the three phases as Fig. 4, where I_{total} is the sum of the $I_{sampling}$, $I_{slewing}$, and $I_{settling}$.

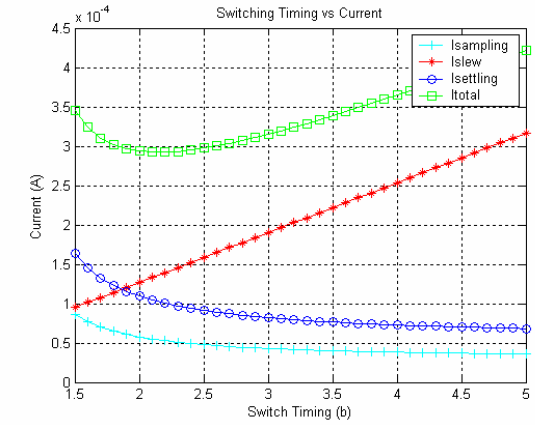

Figure 4. The diagram of the switching timing and current.

From Fig. 4, the optimal b during the three different phases can be obtained. When b equals 2.25, I_{total} is almost the smallest. It is yielding optimal total power dissipation. With a fixed b, the current in different phases can be obtained as for 0.001 accuracy with a clock period of 0.3125μs: $I_{sampling}$, $I_{slewing}$ and $I_{settling}$ are about 60μA, 130μA, and 110μA, respectively.

III. SYSTEM IMPLEMENTATION

Fig. 5 shows the experimental topology of a fourth-order two-stage MASH 2-2 modulator [8] which combines two second-order single-bit SDMs. In the cancellation logic, two outputs, $Y_1(z)$ and $Y_2(z)$, are combined with two digital filters, $H_1(z)$ and $H_2(z)$, to cancel the coarse quantization noise, $E_1(z)$. The transfer functions, $H_1(z)$ and $H_2(z)$, are equal to z^{-2} and $(1-z^{-1})^2$, respectively. The output, $Y(z)$, can be expressed as:

$$Y(z) = X(z)\cdot z^{-4} + E_2(z)\cdot(1-z^{-1})^4 \qquad (12)$$

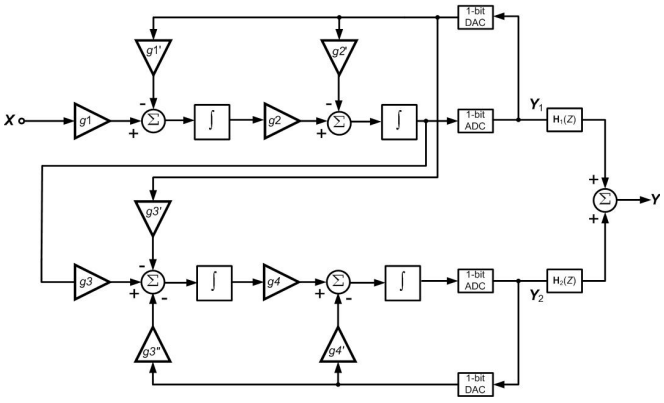

Figure 5. The schematic of the fourth order 2-2 cascadeΣΔ Modulator.

Fig. 6 shows the dynamic biasing circuit for the three different phases. The operations of the circuit are described as follows:

1) *When P and P1 turn off at the same time, the output current will be $I_{samping}$.*
2) *When P1 turns on and P turns off, the output current will be $I_{settling}$.*
3) *When P and P1 turn on at the same time, the output current will be $I_{slewing}$.*

Generally, the current of an opamp is fixed as $I_{slewing}$ in every phase. The total charge equals $I_{slewng}\times T_s$. The dynamic biasing technique makes $I_{settling}$ and $I_{sampling}$ reduced as 11/13 and 6/13 of $I_{slewing}$, respectively. The total charge then equals 9/13 of $I_{slewing}\times T_s$, resulting in the total power saving about 30%. The clock phases of the dynamic biasing circuit and the corresponding currents are shown in Fig. 6. The performances of the folded-cascode opamp in three different phases are summarized in Table I.

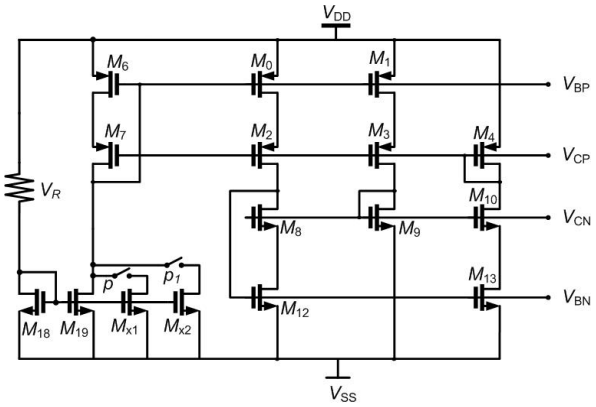

Figure 6. The dynamic biasing circuit.

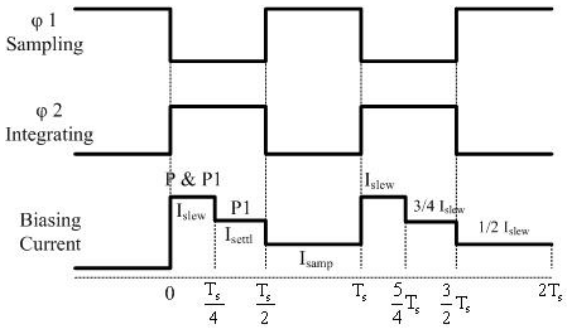

Figure 7. The clock phases of dynamic biasing circuit.

TABLE I. PERFORMANCE SUMMARY OF THE OPAMPS

Performance	Folded-cascode opamp		
Corner (TT)	***Slewing***	***Settling***	***Sampling***
DC Gain	74 dB	73 dB	70 dB
UGBW (C_{eq}=5.5p)	25.7 MHz	22.3 MHz	12.9 MHz
SR (C_{eq}=5.5p)	11.7 V/us	9.8 V/us	6.1 V/us
Phase Margin	69°	71°	72°
Maximum Current	150-μA	130-μA	75-μA
Power	1.8-mW	1.6-mW	0.88-mW

IV. SIMULATION RESULTS

According to the discussions of the previous sections, a fourth-order MASH 2-2 SDM is designed with 2P4M 0.35µm CMOS process for audio applications. The peak-signal-to-noise-and-distortion-ratio (SNDR) is 93dB as shown in Fig. 8, and the dynamic range (DR) is 95dB as shown in Fig. 9. Table II lists the performance summary. The power dissipation of the SDM is about 5mW. The technique of dynamic biasing reaches the total power saving of 20%. According to the figure of merit (FOM) as (13) [9], Table III lists the comparisons with other SDMs.

$$FOM = \frac{DR(dB) \times f_N(Hz)}{Power(W)} (\mu J). \quad (13)$$

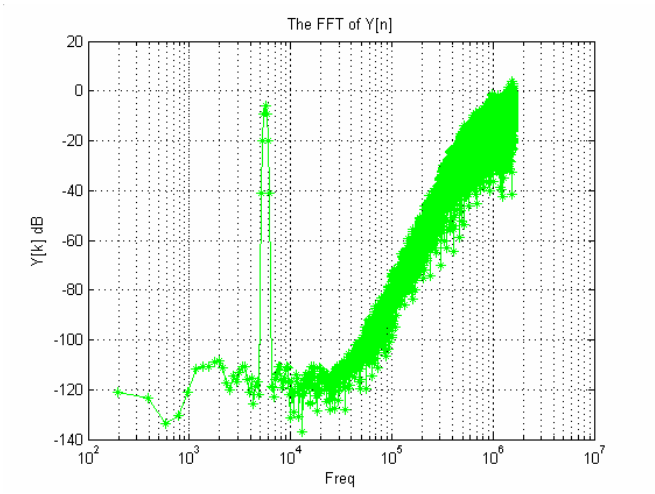

Figure 8. The output spectrum of the modulator

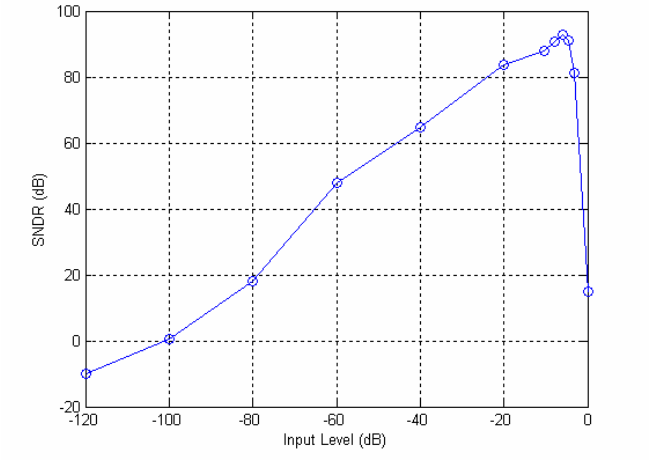

Figure 9. The dynamic range of the modulator

V. CONCLUSION

In this paper, a low power SDM is designed for audio applications. A dynamic biasing technique is used in the SDM, which results in low power consumption. The total power saving of the opamp is about 30% with the dynamic biasing circuits. The power consumption is only 5 mW and the DR is 95 dB.

TABLE II. DYNAMIC BIASING TECHNIQUEPERFORMANCE SUMMARY

Specifications	Value
Sampling rate	3.2 MHz
OSR	64
Signal bandwidth	25 kHz
Peak SNDR	93 dB
Dynamic Range	95 dB
Power consumption	5 mW
Process	TSMC 2P4M 0.35um CMOS

TABLE III. SDM PERFORMANCE COMPARISONS

Specs. / Ref.	DR (dB)	f_N (kHz)	Process	Power (mW)	FOM (µJ)
Garcia-Gonzalez[4]	105	40	0.35µm/3.3V	14	300
F. Medeiro[5]	110.1	40	0.35µm/3.3V	14.7	299.6
This work(simulated)	95	50	0.35µm/ 3V	5	950

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