An Efficient Algorithm to Selectively Gate Scan Cells for Capture Power Reduction

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Abstract

Recently, power dissipation in full-scan testing has brought a great challenge for test engineers. In addition to shift power reduction, excessive switching activity during capture operation may lead to circuit malfunction and yield loss. In this paper, a new algorithm is proposed with using clock gating technique on a part of the scan cells to prevent the internal circuit from unnecessary transitions. These scan cells are divided into several exclusive scan groups. For each test vector, only a portion of the scan groups are activated to store the test response per capture cycle. The proposed method can reduce the capture power dissipation without any influence on fault coverage or testing time. Experimental results for ISCAS'89 benchmark circuits show that the capture power reduction in test sequence can up to 55%.

***Key Words*:** Clock Gating, Scan Test, Low Power Scan Test, Full-Scan Testing, Design for Testability, Yield Loss

1. Introduction

Full scan testing, one of the DFT (design-for-testability) technique, is a strategy based on full-scan design by changing all the storage elements into scan cells and stitch them together to form to single or multiple scan chains. In a full-scan design circuit, there are two operation modes during scan testing, shift mode and capture mode, respectively. In shift mode, the test vectors can be shifted into the circuit under test (CUT) in serial through the scan chain. In capture mode, the test responses are captured into each scan cell hence shifted out at the next shift cycle. Fault coverage, test application time, area overhead, etc, were the main factors for test engineers previously [1]. However, as the coming of high clock frequency and deep sub micron (DSM) technology, power saving is a critical objective, if not so, excessive power dissipation can bring the risk of chip to overheating or damaging, even unstable behaviour or manufacturing yield loss due to the occurrence of power peaks. As a result, power dissipation can not be ignored in test development. To achieve power reduction, ad hoc solutions for industrial were practiced [2] early. The first solution is to reduce the test clock frequency. The second solution is to divide the system-under-test (SUT), or to scheme out an adoptable test schedule. The third solution is to oversize the power supply, or cooling device, break points are even added during test application. The first solution cost less hardware than the second and the third solutions, but is difficult to detect the dynamic faults due to the reduced frequency. Although the second solution can detect dynamic faults, the cost of hardware is increased, such as the third solution. Test application time is also lengthened due to these three solutions.

Switching activity in test mode usually causes much power dissipation than that in normal mode [3], according to several reasons [1,4,5]:

(a) Parallel testing is often used in SOCs by test engineers to reduce the test application time.
(b) The extra components added in the circuits to reduce the test complexity are usually idle in the normal mode but may be used intensively in test mode.

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(c) In normal mode, vector pairs between the present state and the next state are reachable, low switching model can be designed for functional operations. During test operation, these correlations are not reachable.
(d) During test operations, all the gated storage elements must be clocked in each test clock to let the circuit be testable thus higher switching activity may occur.

There are two types of dynamic power dissipation during full scan testing. Shift power is caused by the switching activity in CUT due to the successive test vectors is shifted into the scan chain through numerous clock pulses. Capture power is caused by the switching activity in the CUT due to the opposite value between the test vector and its capture response, which at several scan cells.

Heat and hotspots are usually the problem during scan shifting, depending on the amount of average power dissipation and test length. Increased average power can cause overheat that lead the circuit into damage. Previous methods were proposed for shift power reduction. For example, specified ATPG algorithm [6] minimizes the switching activity by exploiting don't care bits (Xs) during scan shifting, test application, and test responses. Adjacent fill of X-filling techniques [7], which fill the Xs in the test vectors with the same value of the last specified bit (from left to right) to minimize the transitions during scan shifting. Based on the properties of circuit structure, all the Xs filled with 1/0 can reduce more transitions [8]. The advantage of the above non-random filling is zero cost of hardware, and further more minimize the peak power in shift mode. Reordering techniques such as vector reordering, the author in [9] apply Hamming distance between the test vectors to estimate the internal switching activity which caused by a given input pair. To circuit modification, a Scan chain reordering method in [10] arranges the scan cells with considering the ratio of switching activity that a scan cell impacts on the internal circuit. Using a modified scan latch reordering algorithm was proposed in [11]. [11] used scan latch reordering to minimize hamming distance between columns. Scan chain partition such as [12,13], the author in [12] breaks the scan chain into several length-balanced segments. In each shift cycle, only one segment is enabled by a stimulus from an added controller. In recent year, a graph-based algorithm was proposed in [14]. The proposed method in [14] partitions the scan chain into several segments. It also increase the number of don't cares in the given test set.

Moreover, no special APTG algorithm is required for this method thus it is adaptable to various test set. Approach in [13] uses gated clock scheme, where half the main clock frequency into two non overlapping clocks, to feed the odd scan cells and even scan cells thus achieve peak power reduction and clock tree power saving. To input blocking techniques, the author in [15] apply a special control pattern to the primary inputs hence the switching activity in the internal circuits due to the transitions on scan chain is eliminated. In [16], signal probabilities are calculated at the gate outputs to find the frozen value, and identify the scan cells which can cause large impact to the internal circuit. Therefore, the shift power can be reduced by blocking the above scan cells with the frozen value. This approach is independent to the test set so it can be performed directly at RT-level.

Compared with to shift power dissipation, capture power reduction is more difficult to be handled due to the peak power problem. The main reason is all scan cells have to be activated to store the test responses per single capture cycle, large amount of transition on scan cells may occur unpredictably. The most peak power is occurred in capture mode [17], and is useless by reducing the test clock frequency to avoid it. During capture operation, excessive peak power can generate large current drawn from the power source that causes the supply voltage drop and ground bounce, which can increase the gate delay and produce inductive switching noise, respectively [18]. This phenomenon can fail the chip to test, thus result in manufacturing yield loss despite the average power is low.

Approaches for capture power reduction are less than that for shift power reduction. To ATPG-based, a new ATPG algorithm [19] introduces the target fault selection and backtracking to assign proper logic values at the primary inputs or pseudo primary inputs for capture power reduction without fault coverage loss. LCP (Low Capture Power) X-filling [20] minimizes the transitions between a test vector and its test responses in flip flops during capture operation, and is also used for at-speed testing [19]. To furthermore improve the test result from [18,19], the power estimation in [20] not only consider the transitions on scan cells but also consider the switching activity in the internal circuit. To reduce capture

power based on scan chain modification, approaches such as scattering the capture power into different times [5,17], or scan chain disable [21], both can avoid the occurrence of peak power violation efficiently. Based on the scan chain partition with shift power reduction [12, 13], the authors in [5] further more reduce the capture power by applying multiple capture clocks to the scan portions. In [17], based on the conventional multiple scan chain, delay elements are added between the scan chains to interleave the capture cycles which for different scan chains. The approach in [21] assigns the flip flops into multiple scan chains and reorder the test vectors that some of the scan chains can be deactivated for a portion of the set. This approach not only reduces the capture power but also reduce the shift power.

In this paper, we gate a portion of the scan cells which can cause high impact to the circuit during capture operation. In each capture cycle, these scan cell is enabled/disabled according to the control signal, as described latter. Unlike the approach in [5], test responses are captured only in single capture cycle. The proposed method is independent of don't care bits in test vectors. X-filling techniques can be applied to don't care bits such as 1/0-filling, or MT-filling, which according to the circuit structure to reduce the shift power.

The remainder of this paper becomes as follow. Section 2 is the preliminary description for capture power estimation and weighted scan cell approximation. Section 3 explains the proposed algorithm and scan architecture. Section 4 and section 5 are the experimental results and conclusion, respectively.

2. Preliminaries

2.1 Power Dissipation and Power Evaluation

Power dissipation in CMOS circuits includes two parts, static power dissipation and dynamic power dissipation (Figure 1). Static power dissipation is mostly caused by the static current or Leakage that drawn from the power supply. In the past, the problem of leakage is very small. As the feature size scales down, leakage is critical and must be controlled significantly to avoid the increase of static power dissipation, especially with the use of low-Vt devices. Dynamic power dissipation is mostly caused by the switching activity, i.e., charge or discharge of load capacitances in CMOS circuits. It can be the main source of power dissipation. As shown in Figure 1, where CL is the load capacitance, and V_{dd} is the power supply voltage.

The formulation in (4) can be denoted as the instantaneous power in each clock cycle. T will denote the clock period. By definition, the instantaneous power is the power consumed during one clock period. Therefore, the average power and peak power are expressed as in (1) and (2), respectively.

$$P_{avg} = \sum_{t=1}^{n} P(t)/T \quad (1)$$

$$P_{peak} = \max[P(t)]/T \quad (2)$$

By (1) and (2), it is known that the amount of average power is usually related to the shift power due to the accumulation of instantaneous power during shift operation. Although average power can be reduced by lower the scan clock frequency, the peak power issues still exist. Excessive peak power due to high switching activity at CUT may cause large current drawn from the power supply thus the source voltage drops (IR-drop). Reduced voltage on some of the logic gates can be suffered by higher delay. Besides, Ground bounce effect can cause negative impact to signal stabilization at circuit line, especially in high speed, high density chips. These influences can change the logic state, finally leading the chip to failed test, resulting in yield loss.

In order to estimate the instantaneous power, according to (1), many previous researches regard c_0, V_{dd} and f as a constant. Therefore, weighted transition count (WTC) [17] is a good metric to estimate the power dissipation in each clock cycle, as defined as

$$WTC(t) = \sum_{g=1}^{N} s(i,k)F(g) \quad (3)$$

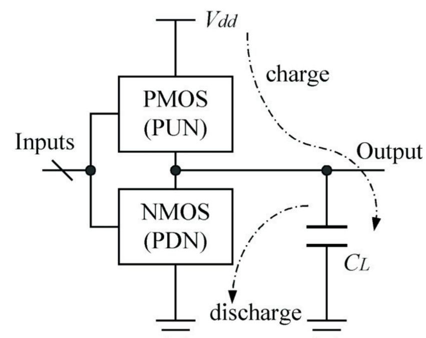


Figure 1. Dynamic power dissipation in a CMOS logic gate.

In this paper, we will use the WTC function to estimate the capture power dissipation in each capture cycle.

2.2 Calculation of Scan Cell Weight

In scan-based design circuit, the external inputs and outputs are referred to primary inputs (PIs) and primary outputs (POs), respectively. The inputs and outputs of each scan cell are referred to pseudo primary inputs (PPIs) and pseudo primary outputs (PPOs), respectively. Based on the circuit topology, most logic gates in CUT are derived from each circuit input (PI or PPI). On the other hand, each input has a fan-out cone, as shown in Figure 2. Transitions on some of the inputs can cause more switching activity in the internal circuits than those the other inputs.

The author in [22] proposes an impact function to evaluate the impact on switching activity in the internal circuit by a transitive input (i.e. the weight of transitions by each input). For a given CUT with n pseudo primary inputs ppi_j, j = 1, 2, …, n, the impact function IMP_j can be expressed as

$$IMP_j = \sum_{\forall l \in C(ppi_j)} D_{ppi_j}(l) \cdot F(l) \tag{4}$$

where l is the circuit line in CUT. F(l) is the fan out of circuit line l, $C(ppi_j)$ is the fan-out cone of input ppi_j, and $Dppi_j(l)$ is the transition density of circuit line l due to the transition on input ppi_j. In this paper, the transition density of each gate is calculated only depends on the number of the correlative inputs (PIs and PPIs), i.e., if there are two circuit line which has the same number of correlative inputs, then the transition density of these two circuit line are equal. Although the accuracy of impact function value is degraded, we can reduce the process time preliminarily.

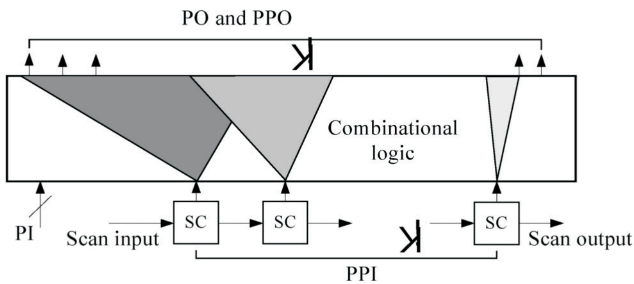


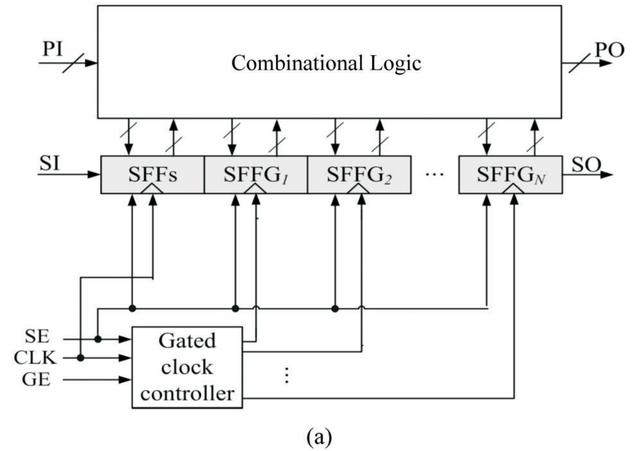
Figure 2. Fan-out cone of each scan cell.

3. Proposed Method

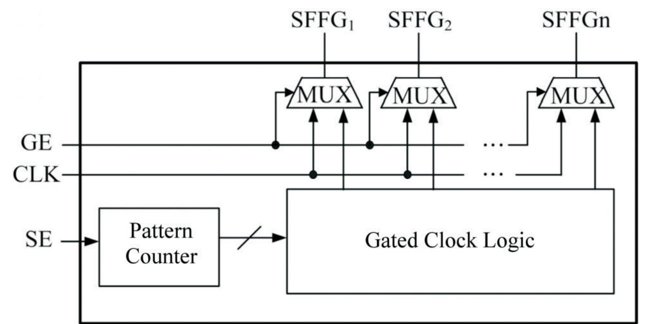
3.1 Scan Architecture with Gated Clock Controller

In order to prevent excessive switching activity in the internal circuit, clock gating technique is used to disable a portion of the scan cells in capture cycle. As shown in Figure 3(a), we propose new scan architecture, which is similar to the one in [2]. In our architecture, the SE and GE are derives from the tester. A gated clock controller is added into the CUT. The scan chain is divided into several scan groups and the scan groups colored in gray are enable/disable by the gated clock controller.

In Figure 3(a), The SE is decide that selected scan chain shifts a test vector or captures a test response. The GE is determination of the SFFG selects. Figure 3(b) is the architecture of the gated clock controller which is composed of pattern counter, gated clock logic and multiplexers (depending on the number of scan groups). Figures 3, 4 shows the timing diagram to illustrate the function of the gated clock controller. In each shift mode during scan testing, the gated enable (GE) signal is low. All



(a)



(b)

Figure 3. (a) Proposed scan architecture. (b) Architecture of gated clock controller.

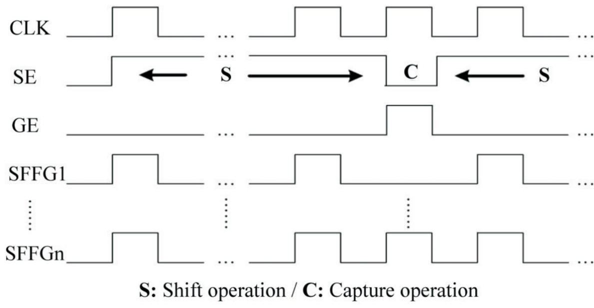


Figure 4. Timing diagram.

scan groups are operated by the original clock signal (CLK). In capture cycle, GE is high and a binary control signal (e.g. 100...10) from the gated clock logic is loaded into the scan groups. The scan groups which receive zero will be disabled. The bit values of each control signal are depended on the count by the pattern counter which can cumulate the number of test vectors while SE is enabled.

3.2 Proposed Algorithm

According to the proposed scan architecture, each test vector is indicated to a corresponding control signal. In capture cycle, the more scan groups can be disabled, the more power reduction we can gain. However, there still exist some limitations on assigning bit values to the control signals.

(a) For a test vector, if a detectable fault is propagated to a scan cell, then the scan cell cannot be disabled for that test vector or else the fault coverage will loss.

(b) During scan testing, if the number of test vectors and scan cells are large, it is difficult to assign individual control signals to each test vector because of the complexity of gated clock controller can increase extremely.

Due to the above two limitations, there are two objectives in the assignment of the control signals. The first one is to minimize the number of used scan cells for each test vector during capturing the test responses. The second one is to minimize the number of the control signals. Therefore, fault diagnosis is implemented to observe the test responses between circuit outputs and faults thus to make each fault only be transferred to a single output. In addition, the fault dropping is performed to drop the faults that detected by at least one test vector. The less test vectors can detect each fault, the more unused outputs can be obtained per test vector so we can assign more zero to each control signal. For example, the fauly 2 is detected by test vector1 and its number of output is 3 (output 1, output 2, output 3). In this care, the output 3 is selected for fault 2, then output 1 and output 2 is unused. Now we assign the control signal value use our algorithm. The output 3 is assigned to 1 (open), the output 1 and output 2 is assigned to 0 (disable).

To minimize the number of the control signals, test vectors are grouped into several exclusive clusters. In a cluster, a common control signal is produced to the test vectors where in this cluster, i.e., the control signals of these test vectors will be identical.

As shown in Figure 5, the process flow of the proposed algorithm is presented. The impact function value at each pseudo primary input is calculated first in step 1. From step 2 to step 3, we perform the process as the above description to make the bit values in each control signal to be zero as far as we can. In step 4, a function of vector grouping procedure is performed to group the test vectors into several clusters. The detail of step 2 to step 3 is explained as bellow.

Step 2. Output-selection for each fault

We first perform a work similar to the fault-propagation path in [22]. As shown in Figure 6(a), if a fault f can caught by primary output PO and scan cell SC, then PO is selected to catch fault f. If there is no any primary output, as shown Figure 6(b), there are three scan cells SC_1, SC_2 and SC_3 that can catch the fault f. Assume that the scan cells SC_3 has the minimum impact function value, therefore, SC_3 is selected to catch the fault f.

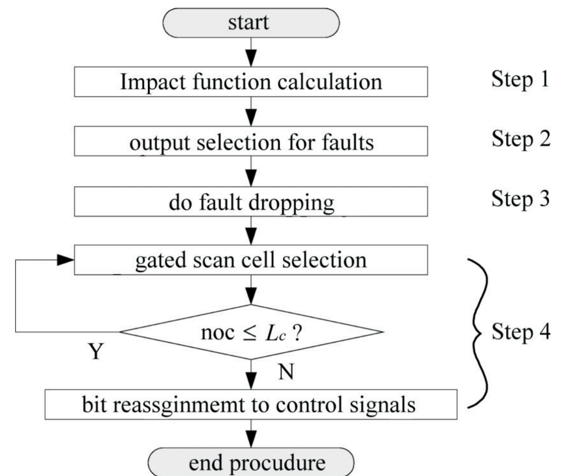


Figure 5. Flow of the proposed algorithm.

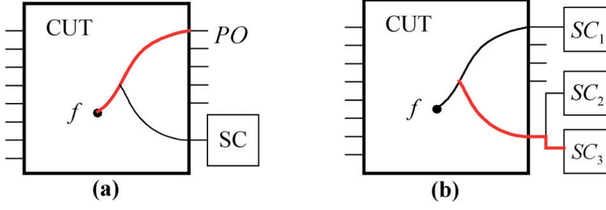


Figure 6. Output-selection to fault f. (a) PO is exist for fault f. (b) PO is not exist for fault f.

Step 3. Fault dropping

As soon as the output selection is processed, each fault is propagated only to a single output. The procedure of fault dropping to test vectors can gain more zero bits (disable signals) to each control signal, as a result, outputs that can catch the essential faults are considered first. Figure 7(a) shows an example. Assume that f1 is an essential fault (for a given test set, only one test vector can detect this fault), which can detected by test vector v at scan cell SC_i, hence SC_i must be activated when capturing the test response of v. If there is a fault f2, which is able to be detected by v at SCi either, then f2 is regarded as a sub essential fault to v and is assigned to be detected by v. The other test vectors that can detect f2 can drop it.

When all essential faults and sub essential faults are assigned, the remaining faults are collected and dropped by some of the test vectors. As shown in Figure 7(b), consider a remaining fault f3, which only can be detected by test vectors v_i and v_j at scan cell SC_k. F_i and F_j are the fault set belong to v_i and v_j on scan cell SC_k, respectively. Both F_i and F_j cover f3. The selection between v_i and v_j to detect f3 is according to the number of faults in the fault set F_i and F_j. If the number of faults in F_i is smaller than the number of faults in F_j, then v_j is selected to detect f3 and f3 can be dropped by vi. After the fault dropping is performed, some of the scan cells that are unused during capturing can be disabled for the test vectors, individually. In addition, if a test vector contains no any fault set, then it can be dropped from the test set.

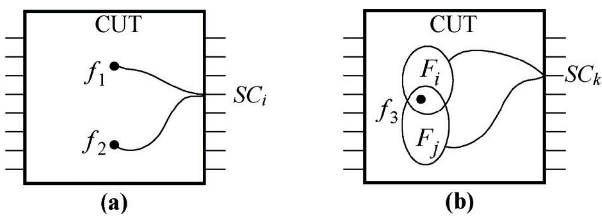


Figure 7. Procedure of fault dropping. (a) f_1 is an essential fault. (b) f_3 is a remaining fault.

Step 4. Vector grouping procedure

Figure 8 shows the algorithm of vector grouping. After the fault dropping to test vectors is performed, the new control signals are achieved and are rebuild in matrix A (line 2). As we mentioned in the previous discussion, in order to reduce the complexity of the gated clock controller, the test vectors are grouped into several exclusive clusters. The control signals in matrix A can be merged in OR operation without too many zero loss. However, it can be recognized that merging the control signals with the consideration of impact function value is an NP-complete problem. Therefore, we propose a heuristic methodology to group the test vectors. The variable L_c is an upper limit of the number of clusters. To perform the selection, first is to find out the scan cells which can cause the maximum unnecessary impact in each cluster (line 16) and compare all of it, two by two. The specific scan cell which has the maximum unnecessary impact in a cluster is selected to be gated and the test vectors among the above cluster that need the specific scan cell being activated is then grouped into a new cluster (line 19~line 26). When the number of clusters is equal to L_c, bit reassignment is implemented, i.e., in each cluster, enable signals are assigned to the scan cells that are not selected.

```
01 #define
02     A: control signal table, where A=[a_ij]_nov×nos
03     TR: transition table, where TR=[tr_ij]_nov×noc
04     (V, O, R): (test set, PPO set, test response set)
05     (nov, noc, nos): (#test_vector, #cluster, #scan_cell)
06     Lc: upper limit of cluster
07 begin
08     noc=1;
09     TR = find_transitions(V, O, R);
10     ∀ cluster ← Φ;
11     gate ← Φ;
12     cluster_1 ← store_row(A);
13     do{
14         for each cluster_i (i=1 to noc)
15             for each SC_j ( j ∉ gate)
16                 W ← find_the_max_UI_SC(cluster_i, O, TR );
17             endfor
18         endfor
19         (cluster_max, SC_n) ← select_the_max_UI_SC(W);
20         gate ← n;
21         for each a_mn, (a_mn ∈ row_m) ∩ (row_m ⊂ cluster_max)
22             if a_mn ==1 then
23                 noc ++;
24                 cluster_noc ← row_m;
25             endif
26         endfor
27     }while( noc ≤ Lc)
28     A=bit_reassignment();
29 end
```

Figure 8. Algorithm of vector grouping.

We illustrate an example as follows. As shown in Figure 9. A matrix A is presented. Each row $row(A)_1$ to $row(A)_6$ denotes the control signal of test vector v_1 to v_6, respectively. Matrix TR records the condition of transitions between each test vector and fault free responses by itself, e.g. $tr_{ij} = 1$ means there is a transition occurred at scan cell SC_j by test vector v_i. In a cluster C, the unnecessary impact of each scan cell SC_j, $j = 1, 2, \ldots, n$, is defined as

$$UI_c(j) = \sum_{\forall row_i \subset C} \overline{a_{ij}} \cdot tr_{ij} \cdot IMP_j \tag{5}$$

where IMP_j is the impact function value at scan cell SC_j.

Before grouping the test vectors, we suppose that every test vector is already included in cluster 1. As shown in Figure 10, by using (5), we first find out that SC_2 causes the maximum unnecessary impact by the test vectors in cluster1 thus SC_2 is selected to be gated and set into scan group SG_1. The test vectors with the respect to the control signals which has to be assigned activate SC_2 are grouped into a new cluster (cluster 2 = $\{v_1, v_2, v_5\}$). After SC_2 is gated, it will not be compared in the future. In the second selection, SC_3 is found that has the maximum unnecessary impact in cluster 1, where is compared with each scan cells in $cluster_2$. Because of all the control signals in cluster 1 do not have to activate SC_3, therefore, the test vectors in cluster 1 need not be separated and SC_3 can be grouped with SC_2 into SG_1. To perform as same as the above operation in the third selection, we can obtain $cluster_3$ and SG_2. After all of the test vectors are grouped, by the implementation of bit reassignment, as shown in Figure 11, the new control signals for each cluster is formed. Finally, it is observed that in the duration of capturing the test response of v_3, v_4 and v_6, scan cell SC_2 and SC_3 is disabled. SC_4 is disabled while capturing the test responses of v_2 and v_5. SC_1 is always enabled per capture cycle. Therefore, it does not belong to any scan group.

$$A = \begin{bmatrix} 0 & 1 & 1 & 1 \\ 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \qquad TR = \begin{bmatrix} 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 \\ 0 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 \end{bmatrix}$$

Figure 9. Sample of matrix A and matrix TR in our illustration.

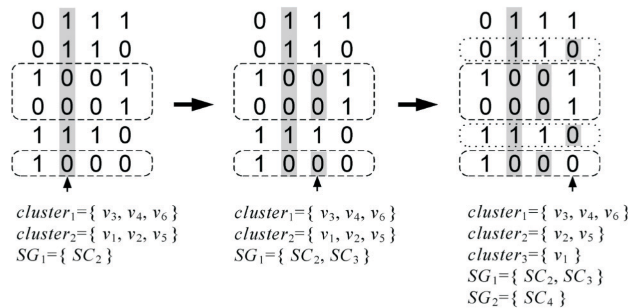


Figure 10. Example of gated scan cell selection.

4. Experimental Results

We accomplished the proposed method in C programming language with GNU CC 3.2.3 running on Linux system and the experiments were carried out on ISCAS'89 benchmark circuits. A test set is generated for each circuit by ATALANTA [23] with MT-filling of the X's. We use the weight transition count per a clock cycle to approximate the capture power dissipation. The transition count is not calculated in shift mode only in capture mode.

As shown in Table 1, we present the experimental results of the seven large benchmarks circuits by grouping the test vectors into number of 16 clusters (number of 15 scan groups are established). The detail of the experimental results is shown in the appendix. In Table 1, the seventh and the eighth column show the number of gated scan cells and the percentage of the total number of scan cells in the benchmark circuits, respectively. We can find that during the process of vector grouping, for a cluster, the more scan cells that can be gated with the identical control signal, the more power reduction can be approached. E.g. to s38417, there are amount of 113 scan cells can be gated only by the grouped of 16 vector clusters. Table 2 shows the improvement of the maximum WTC and is compared with the method in [5]. The test results in [5] are achieved by an ATPG generated test set (0-filling of the X's) under three scan segments. In order to obtain more power saving, we can increase the number of

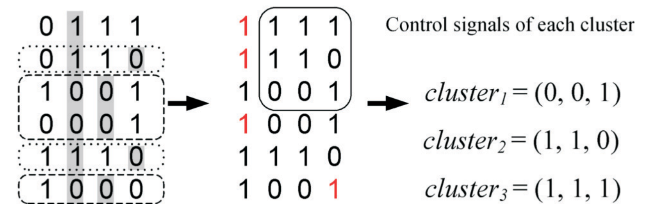


Figure 11. Bit reassignment to matrix A.

vector cluster for a test circuit, however, the power saving and the complexity of gated clock controller is a trade off. If the number of cluster is too large hence it may also increase the total circuit area and the gated clock controller will cause more extra power that will inhibit the performance of power saving.

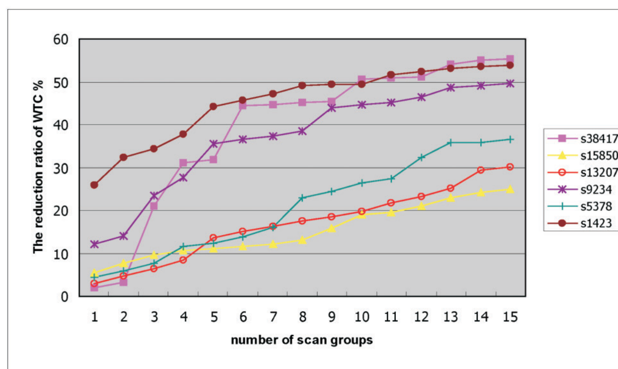
In the last page of this paper, Figures 12(a) and (b) shows the reduction ratio of WTC from 1 to 15 scan groups, and the increasement ratio of the gated scan cells, respectively. As shown in Figure 12(a), due to the "estimation" of impact function value at each pseudo primary input, the reduction ratio of WTC in some of the circuits are not presented in decreasing order, i.e., the gated scan cell which can cause more WTC reduction is not be gated preferentially. Figure 13 shows the reduction of WTC in each capture cycle from the above six large benchmark circuits under 15 scan groups, most capture transitions from the circuits are reduced. Be-

Table 1. Experimental result of the seven large benchmarks on amount of 16 clusters

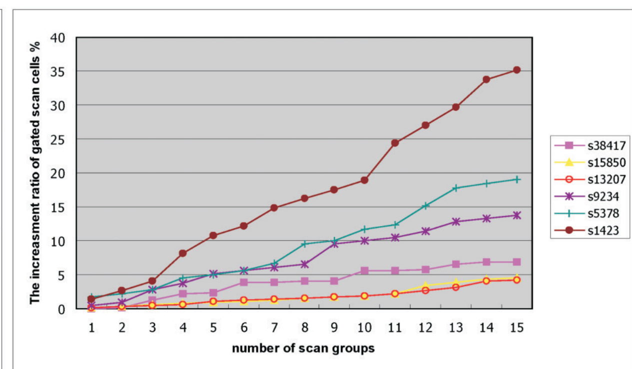
Circuit			Weight Transition Count (WTC)			Gated scan cells		CPU time (sec)
name	#scan cell	#vec.	original	proposed	Improv. %	#	%	
s1423	74	68	7826	3614	53.82	26	35.14	1
s5378	179	269	162744	103075	36.66	34	18.99	5
s9234	211	455	451827	227159	49.72	29	13.74	13
s13207	638	547	7544083	527618	30.06	27	4.23	37
s15850	534	507	505219	379008	24.98	24	4.49	47
s38417	1636	934	4254769	1904662	55.23	113	6.91	1445
s38584	1426	790	2289212	2093820	8.54	18	1.26	182

Table 2. Comparison between the method in [5] and the proposed method

Circuit	Max. WTC					
	Proposed			Method in [5] (3 segments)		
	original	final	Improv. %	original	final	Improv. %
s1423	206	11	94	-	-	-
s5378	779	431	44	2250	1336	39
s9234	1394	727	47	2711	2247	17
s13207	1814	1262	30	3776	2235	41
s15850	1589	1140	28	3594	2642	26
s38417	5810	2582	55	10083	8060	20
s38584	5113	4817	5	11342	6551	35



(a)



(b)

Figure 12. Trade-off between (a) the number of scan groups and the number of reduction ratio. (b) the number of scan groups and the percentage of gated scan cells.

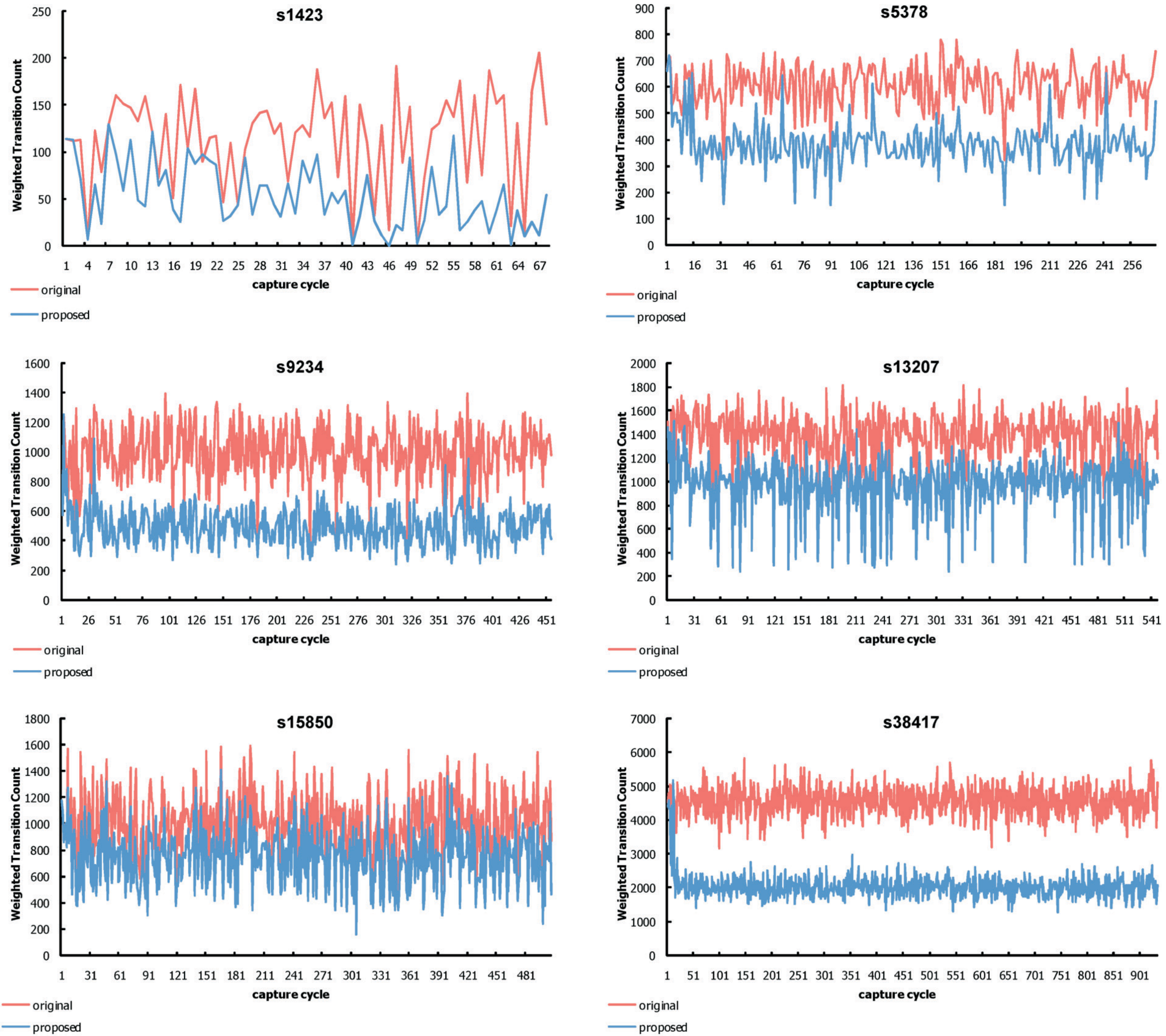


Figure 13. Graphs showing the reduction of WTC on six large benchmark circuits during capture operation under 15 scan groups.

cause of the random pattern testing (RPT) is included before deterministic test pattern generation in ATPG, many faults may be detected by the earlier test vectors thus the size of fault sets of these test vectors are large. Due to the proposed fault dropping procedure, these earlier test vectors are unable to drop the detectable faults. Therefore, a few high transitions still occurred in the earlier capture cycle. As a result, we can perform bit-stripping to the test vectors which corresponding to those of the capture cycle if it exist peak power violation.

5. Conclusion

In this paper, we propose a new method by using clock gating technique on scan cells to prevent the internal circuit from unnecessary transitions. The weight of transition by each input is calculated and the fault processing is performed in the proposed algorithm to select the suitable scan cells for gating. The proposed method can reduce the capture power dissipation without fault coverage losing or testing time increasing. Experimental results show that most transitions in capture cycles are reduced. In future work, we hope to synthetize the circuit to estimate the area overhead, and the precise value of capture power dissipation.

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