Inductorless CMOS Receiver Front-End Circuits for 10-Gb/s Optical Communications

Hsin-Liang Chen*, Chih-Hao Chen, Wei-Bin Yang and Jen-Shiun Chiang

Department of Electrical Engineering, Tamkang University,
Tamsui, Taiwan 251, R.O.C.

Abstract

In this paper, a 10-Gb/s inductorless CMOS receiver front end is presented, including a transimpedance amplifier and a limiting amplifier. The transimpedance amplifier incorporates Regulated Cascode (RGC), active-inductor peaking, and intersecting active feedback circuits to achieve a transimpedance gain of 56 dBΩ and a bandwidth of 8.27 GHz with a power dissipation of 35 mW. The limiting amplifier employs interleaving active feedback to achieve a differential voltage gain of 44.5 dB and a bandwidth of 10.3 GHz while consuming 226 mW. Both circuits are realized in 0.18-μm CMOS technology with a 1.8-V supply.

Key Words: Transimpedance Amplifier, Limiting Amplifier, Inducorless, Optical Communication

1. Introduction

With the rapid growth of the data volumes in tele-communication networks, the interest in high-speed optical and electronic devices and systems has been rekindled [1]. The highly demand for high speed data rates in communications causes the rapid development of the high speed data transport. As the information traffic in modern communication networks grows at an ever increasing speed, the data rates are approaching the physical limit of general links, such as copper wire, between the nodes in the networks. Thus, there is an urgent need for those networks to possess communication with higher speed. Optical fiber is a well-known medium suitable for such demand due to its extremely wide bandwidth. The researches of the optical system are therefore the works we strive for. Figure 1 shows a typical block diagram of an optical communication (OC) system that briefly consists of a transmitter, transmission medium such as a fiber, and a receiver [2]. The transmitter contains an electro-optical transducer and associated drivers while the receiver comprises a photo detector (PD), a transimpedance amplifier (TIA), a limiting amplifier (LA), and a

decision circuit. In the past, those circuits were usually implemented with expensive technologies such as GaAs, HBT, HEMT, and BJT. While cutting the cost by using cheaper technologies has become a trend, it poses challenges because of the extraordinarily high speed that the system requires.
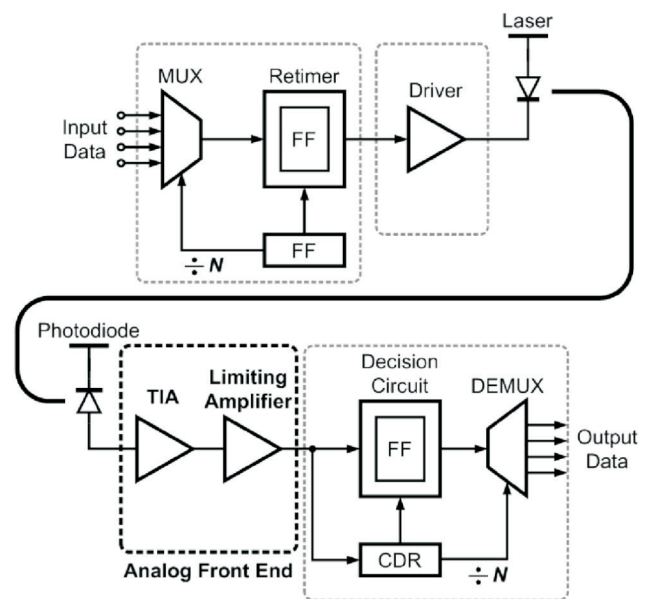

Figure 1. Optical communication system.

---

*Corresponding author. E-mail: hlchen@ee.tku.edu.tw

Owing to the blooming advancement of the deep-submicron CMOS process, the implementation of the optical system with standard CMOS process is more and more practicable. With the characteristics of low power dissipation and low cost, the CMOS technology makes it easier for us to integrate the analog front-end circuits and the digital circuits in optical system. In the past few years, there are many designers who have implemented high-speed front-end circuits with CMOS process [3–9]. However, the circuits with CMOS technology are still limited by its inherent speed limitation. To overcome this drawback, several high-speed techniques have been proposed. For example, the feedback compensation and inductor peaking are used to extend the operational bandwidth of TIA and LA. Unfortunately, these methods reach the target of high-speed with the issues of more power dissipation or more area cost. Especially, the passive-inductor peaking and the passive feedback compensation techniques dominate the most area cost. Generally, the active cases are preferred for developments. In this paper, the analog front-end circuits are hence implemented with standard CMOS process, while the active-inductor peaking technique takes the place of the passive-inductor peaking technique. Also, the active-feedback compensation technique is used to TIA and LA. Therefore, the advantages of the area saving and the performance maintaining are reachable. Moreover, the behavioural simulations with MATLAB are provided for the quick system verification and the choices of the circuit architecture.

This paper comprises six sections. Section II lists the specifications of the systems and the circuits. Sections III and IV describe the architecture and circuit design of the TIA and the LA, respectively. Finally, Sections V and VI give the simulation results and our conclusion.

2. Specifications of System and Circuit

2.1 System Specifications

The Synchronous Optical Network (SONET) standard was published and developed in the mid-1980s by American National Standards Institute (ANSI). SONET, which remains in widespread use today, is the standard specifying the formats in optical communication systems. In Europe, a similar standard to SONET, which was published by the International Telecommunications Union (ITU), is known as Synchronous Digital Hierarchy (SDH). SONET and SDH are both sets of related standards for synchronous data transmission over fiber optical networks. The differences between them are slight, and the main one occurs in the basic frame format. However, SONET and SDH are approximately the same beyond the Electrical Synchronous Transport Signal level-3 (STS-3). Table 1 lists the hierarchy of the most common data rates of SONET/SDH. The design in this paper is made to meet the data rate of 10 Gb/s, i.e., SONET OC-192 standard.

2.2 Circuit Specifications

The sensitivity is one of the most important indexes in a receiver, which represents the minimum incident optical power at a given BER. According to SONET OC-192 standard, the sensitivity required for short-range (17–20 km) communication is -12 dBm [10]. Considering a 3-dB margin, we obtain that the required sensitivity of the receiver should be better than -15 dBm.

Since the receiver front end mainly consists of two blocks, TIA and LA, the total gain of a receiver can be separated into two parts, the transimpedance gain of TIA and the voltage gain of LA. Owing to that the sensitivity of the LA at BER = 10^{-12} is generally about 5 mV, the transimpedance gain must achieve 250 Ω (48 dBΩ) under the worst case with input current of about 20 μA in response to optical power of -15 dBm. In the aspect of LA, since the required voltage swing of the CDR is about 400 mV, the voltage gain of LA must achieve at least 80 V/V (38 dB). The overall receiver front end with required gain and signal swing for SONET OC-192 is demonstrated in Figure 2.

The bandwidth of an overall receiver in SONET OC-192 must be 6.5 GHz to avoid intersymbol interference (ISI) [11]. The bandwidth of the overall receiver is

Table 1. The data rates of SONET/SDH standards

SONET Standard (Optical Level)	STS (Electrical Level)	SDH Standard	Bit Rate (Mb/s)
OC-1	STS-1	-	51.840
OC-3	STS-3	STM-1	155.520
OC-12	STS-12	STM-4	622.080
OC-48	STS-48	STM-16	2488.320
OC-192	STS-192	STM-64	9953.280
OC-768	STS-768	STM-256	39813.120

determined mostly by that of the TIA. However, the typical bandwidth chosen for TIAs is approximately 70% of the data rate so as to improve the noise-ISI trade-off. On the other hand, if two stages with the same bandwidth are cascaded, the overall small-signal bandwidth is quite narrower. Thus, the bandwidth of LAs is deliberately set greater, usually equal to the data rate. Table 2 shows the specifications of the receiver front end.

3. Transimpedance Amplifier Design

In optical transceiver, when a light signal travels through an optical fiber and arrives at the receiver, a photo detector, such as a photodiode, will detect the incoming light signal. The light is first transformed into electrical current, and subsequent TIAs then convert the current to voltage for following stages of the receiver. Therefore, TIAs play essential roles in bridging the photo detector and the subsequent circuit.

3.1 Transimpedance Amplifier Core

Generally, a photodiode possesses a large parasitic capacitance, which easily produces a large time constant with the input impedance of TIA and hence results in a narrow bandwidth. Such capacitance of various com-
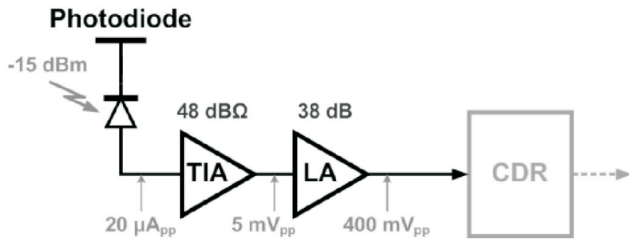
mercial products falls in the range from 130 fF to 300 fF. Thus, for a given photodiode capacitance, the bandwidth of a TIA can be extended by reducing the input resistance of the circuit. The common-gate (CG) topology is therefore a best choice. However, in order to further lower the input impedance, the circuit should be modified.

3.1.1 Regulated Cascode (RGC) Configuration

Figure 3(a) illustrates a general CG input stage and Figure 3(b) depicts the CG input stage modified with the regulated cascade (RGC) configuration [3]. With the addition of the common-source stage M_2 and the resistive load R_{D2}, the RGC stage acts as a local feedback stage and hence reduces the input impedance. From the small-signal analysis, the impedances seen looking into the CG stage with RGC configuration, Z_b, will be significantly reduced by a factor of $1 + g_{m2}R_{D2}$, where $g_{m2}R_{D2}$ is the loop gain of the local feedback stage.

Unfortunately, such RGC configuration suffers from a voltage headroom problem. In Figure 3(b), the voltage drop of the circuit is equal to

$$V_{DD} = V_{RD2} + V_{GS2} + V_{GS1} \tag{1}$$

which is at least the order of $(V_{RD2} + 2V_{TH})$, where V_{TH} is the threshold voltage of a MOS transistor. Moreover, the large threshold voltage of M_2 shrinks the gate-source

Table 2. The specifications of receiver front end

Parameter	Overall Receiver	TIA	LA
Gain	> 86 dBΩ	> 48 dBΩ	> 38 dB
−3-dB Bandwidth	6.5 GHz	7 GHz	10 GHz
Sensitivity @ BER = 10^{-12}	−15 dBm	20 μA$_{pp}$	5 mV$_{pp}$

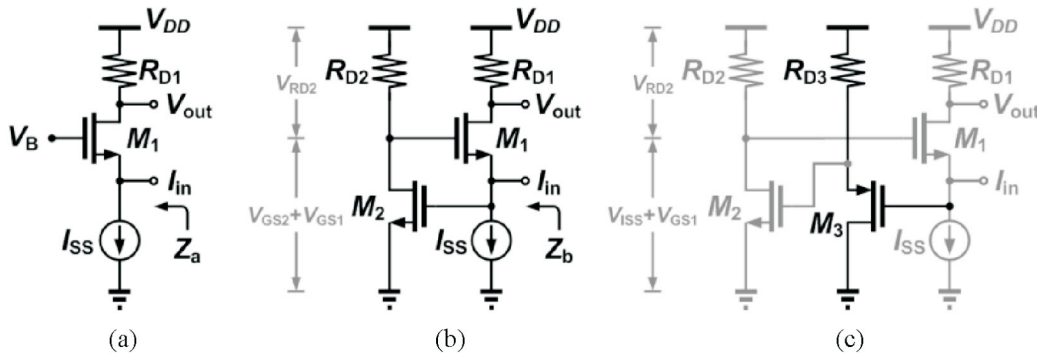**Figure 2.** Receiver front end with gain/swing requirements for SONET OC-192.

Figure 3. (a) CG input stage, (b) RGC input stage, and (c) modified RGC input stage.

voltage of M_1, V_{GS1}, which leads to a large M_1, bringing an undesirable parasitic-capacitance effect. In Figure 3(c), a modified RGC input stage with a PMOS source follower is presented [4]. By inserting the PMOS source follower, the voltage drop of the circuit thus becomes

$$V_{DD} = V_{RD2} + V_{ISS} + V_{GS1} \tag{2}$$

where V_{ISS} denotes the voltage across I_{SS}, minimally equal to an over-drive voltage of a MOS transistor, V_{OD}. The required supply voltage is therefore reduced to the level of ($V_{RD2} + V_{OD} + V_{TH}$). Furthermore, even with a constant voltage drop at the gate terminal of M_1, the voltage limitation of V_{GS1} is loosened, resulting in a smaller M_1 with the same driving capability. Meanwhile, the gate-source capacitance of M_2 can be isolated by the PMOS source follower, benefiting the bandwidth.
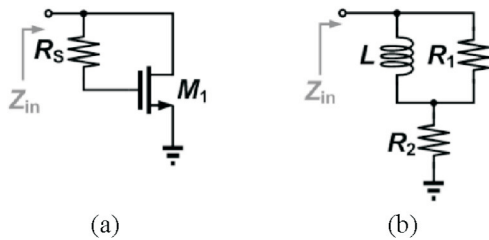
3.1.2 Active-Inductor Peaking

The inductor peaking techniques have become more and more popular in high speed circuits with the progress of the monolithic inductors. An inductor can resonate with the capacitance that limits the bandwidth, thereby significantly improving the speed. Even though the size of passive inductors tends to scaling down while maintaining the same inductance, the large expense of the occupied area is still undesirable. Therefore, if the area is critical, inductive peaking can be realized with active devices.

Consider the diode-connected NMOS shown in Figure 4(a), where a resistor R_S is inserted between the gate and drain of M_1. From the derivation of input impedance, we can obtain a simplified equivalent model as depicted in Figure 4(b), where R_1, R_2, and L are as follows:

$$R_1 = R_s - \frac{1}{g_{m1}} \tag{3}$$

$$R_2 = \frac{1}{g_{m1}} \tag{4}$$

Figure 4. (a) Active-inductor peaking and (b) simplified equivalent model of (a).

$$L = \frac{C_{GS}}{g_{m1}}\left(R_S - \frac{1}{g_{m1}}\right) \tag{5}$$

3.2 Gain Stage

The input current turns into voltage form through the transimpedance amplifier core. However, the magnitude of the voltage signal is insufficient for the requirement of the specification. Thus, we need a gain stage to boost the signal and maintain the speed at the same time. For a gain stage, the cascaded gain cells are conventionally used to achieve a high gain and a wide bandwidth. Nevertheless, the circuit has to employ more broadband techniques to approach a higher speed.

3.2.1 Third-Order Gain Stages with Active Feedback

Negative feedback topology is a powerful broadband skill which is used widely in high-speed analog circuits. Different from the traditional resistive feedback, the proposed gain stage employs active negative feedback to avoid the direct resistive load on the preceding transimpedance stage. Moreover, active devices suffer less process variations than passive ones in fabrication. Figure 5 illustrates the block diagram of the third-order gain stages with active feedback. Each cell, including the feedback cell, is realized with common-source (CS) topology.

With the incorporation of the feedback loop M_F, the -3-dB bandwidth is increased at the cost of the reduction in the gain. However, under a maximally-flat frequency response, the overall bandwidth of the TIA is still not sufficient for requirement. Thus, an additional effort should be made for bandwidth extension.
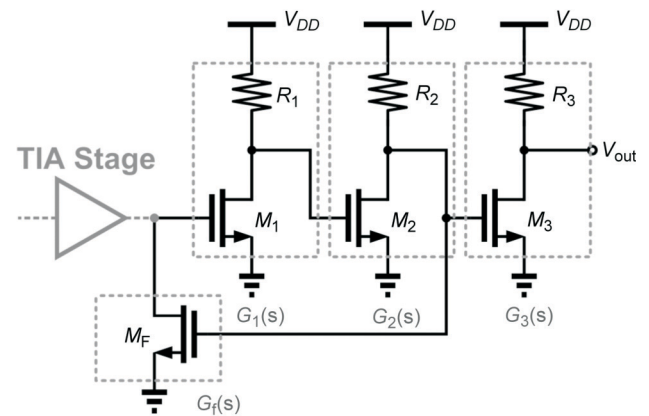
Figure 5. The third-order gain stages with active feedback.

3.2.2 Third-Order Gain Stages with Intersecting Active Feedback

Figure 6 illustrates the block diagram and circuit realization of the third-order gain stages with intersecting active feedback. By means of intersecting an additional feedback loop M_{F2} in the third-order gain stages, there is a remarkable achievement in bandwidth extension. Furthermore, the intersecting feedback architecture alleviates the zero accumulation in the vicinity of the roll-off frequency, yielding less gain peaking and hence less overshoot. Therefore, such structure makes it possible for a TIA to achieve the required speed in 10 Gb/s system without any inductor used. The detail of the bandwidth enhancement of the novel structure will be presented by means of the behavioral simulations below.

3.2.3 Behavioral Simulations

Consider the conventional and the proposed structures in Figure 5 and Figure 6. The transfer functions of the conventional architecture and the proposed one can be described as

$$\frac{V_{out}}{V_{in}} = \frac{G_1(s)G_2(s)G_3(s)}{1+G_1(s)G_2(s)G_f(s)} = \frac{G^3(s)}{1+G^2G_f(s)} \tag{6}$$

and

$$\frac{V_{out}}{V_{in}} = \frac{G_1(s)G_2(s)G_3(s)}{1+G_1(s)G_2(s)G_{f1}(s)+G_2(s)G_3(s)G_{f2}(s)}$$
$$= \frac{G^3(s)}{1+2G^2(s)G_f(s)} \tag{7}$$

respectively while assuming that

$$G_1(s) = G_2(s) = G_3(s) = \frac{G_m R}{1+sRC} \tag{8}$$

and

$$G_{f1}(s) = G_{f2}(s) = G_f(s) = \frac{G_{mf} R}{1+sRC} \tag{9}$$

With the transfer functions, we can plot the frequency response. The simulated frequency responses of the different gain stages are shown in Figure 7. It is obvious that the novel structure extends the bandwidth while suppressing the gain peaking. Figure 8 shows the overall circuit of the proposed inductorless TIA, which contains a BIAS circuit, RGC configuration, TIA core, and gain stage. Meanwhile, the photodiode is modelled with parasitic capacitor (C_{PD}) and current source (I_{in}).

3.3 Single-to-Differential Conversion

Since photodiodes produce a single-ended current, the input signal of TIAs is not naturally differential. However, in order to alleviate the effect of noise, the design of TIAs with differential topology is a trend. Moreover, owing to the differential input of the following circuit, a single-to-differential conversion circuit has to bridge the TIA and the subsequent circuit.

Figure 9 depicts a single-to-differential conversion circuit used in this design. R_1 and C_1 comprise a low-pass filter which extracts the dc level of the TIA output, resulting in an offset-free differential output. However, the

Figure 6. The third-order gain stages with intersecting active feedback.
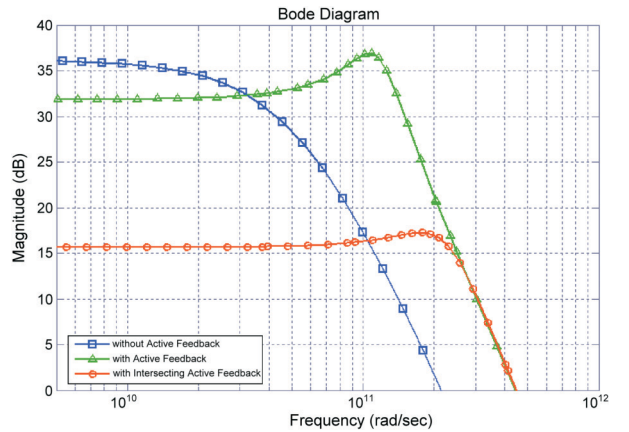
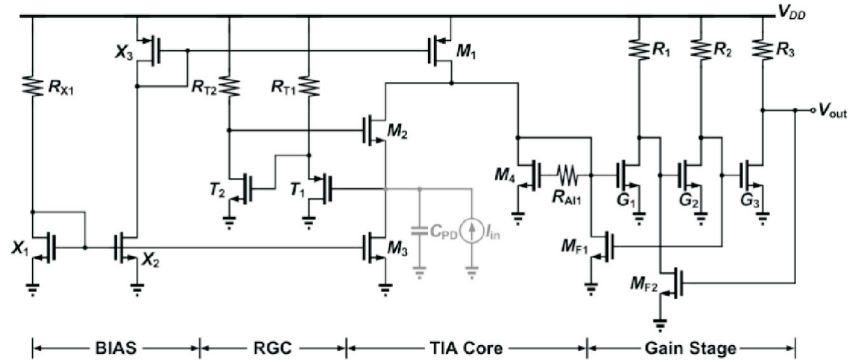**Figure 7.** Simulated frequency response of the gain stages with and without active feedback.

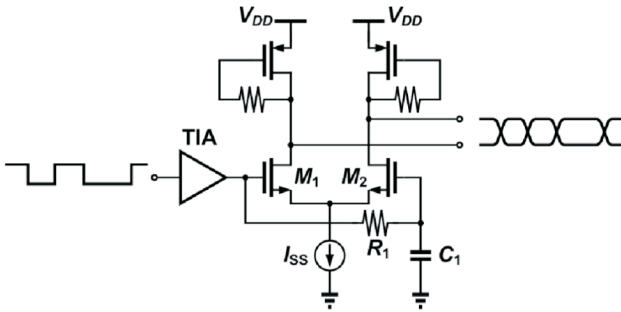**Figure 8.** Overall circuit diagram of the proposed TIA.

Figure 9. Single-to-differential convertor.

time constant $\tau = R_1 C_1$ must reach tens of microseconds if a lower corner frequency of a few tens of kilohertz is expected. Besides, the active-inductor peaking technique is also employed here for a wider bandwidth.

4. Limiting Amplifier Design

Since the output signal of the TIA is inadequate for the CDR circuit, an LA is supposed to be interposed between the TIA and the CDR circuits. The LA must be able to boost the signal swing produced by the TIA to a required level, e.g., 400 mV. As illustrated in Figure 10, the architecture of the proposed LA comprises four
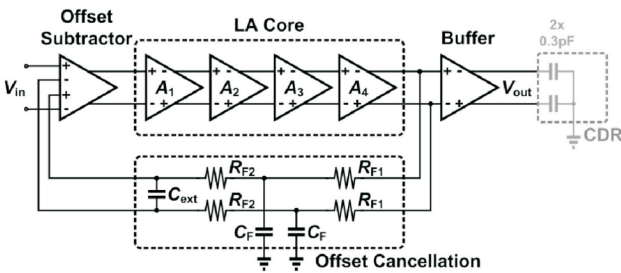
blocks: an LA core composed of four cascaded gain cells, an offset subtracter, an offset cancellation circuit, and an output buffer. The details of each part will be discussed in the subsequent subsections respectively.

4.1 Limiting Amplifier Core

While the LA core circuit has to provide a sufficient gain and a wide bandwidth, the third-order active-feedback architecture is commonly employed.

4.1.1 Third-Order Gain Cell with Active Feedback

As usual, active negative feedback is again introduced for bandwidth improvement. In Figure 11, the circuit diagram of the third-order gain cell with active-feedback architecture is depicted. The gain and bandwidth are quite high even without inductor peaking due to the three-stage CS amplifier and active local-feedback topology respectively. However, such structure suffers from severe gain peaking and overshoot. Therefore, some technique must be employed.
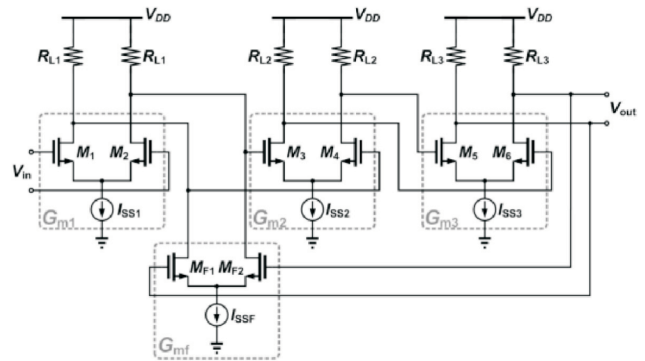

Figure 10. Limiting amplifier architecture.

Figure 11. Realization of the third-order gain cell with active feedback.

4.1.2 Third-Order Gain Cell with Interleaving Active Feedback

Consider two stages of the third-order gain cells. The idea of the interleaving active-feedback architecture is to interleave an additional active feedback cell between each two successive gain cells while each cell already possesses a local active feedback. The architecture of the interleaving active-feedback cell is identical to that of the local one, as depicted in Figure 12. Surprisingly, the -3-dB bandwidth is substantially extended at only a few costs in voltage gain by interleaving the feedback cell.

4.1.3 Behavioral Simulations

In addition to the significant improvement in bandwidth, it is interesting that the interleaving feedback cell also suppresses the excess gain peaking excellently and hence the overshoot. One idea is that the interleaving feedback alleviates the gain peaking accumulation near the -3-dB frequency brought by the cascaded identical gain cells. Consider the two-stage third-order gain cells in Figure 12. The transfer functions of the gain cells without and with interleaving active feedback are as follows:

$$\frac{V_{out}}{V_{in}} = \frac{G^6(s)}{1 + 2G^2(s)G_f(s) + G^2(s)G_{fl}(s) + G^4(s)G_f^2(s)} \quad (10)$$

respectively, where

$$G_1(s) = G_2(s) = G_3(s) = G(s) = \frac{G_m R_L}{1 + sR_L C_L} \quad (11)$$

$$G_f(s) = \frac{G_{mf} R_L}{1 + sR_L C_L} \quad (12)$$

and

$$G_{fl}(s) = \frac{G_{mfl} R_L}{1 + sR_L C_L} \quad (13)$$

With transfer functions, we can plot the frequency response. The simulated frequency responses of the gain cells with and without interleaving active feedback are shown in Figure 13. From observation, we can clearly find that the interleaving active feedback is able to suppress the gain peaking. The overall LA core with interleaving active feedback is shown in Figure 14. There are
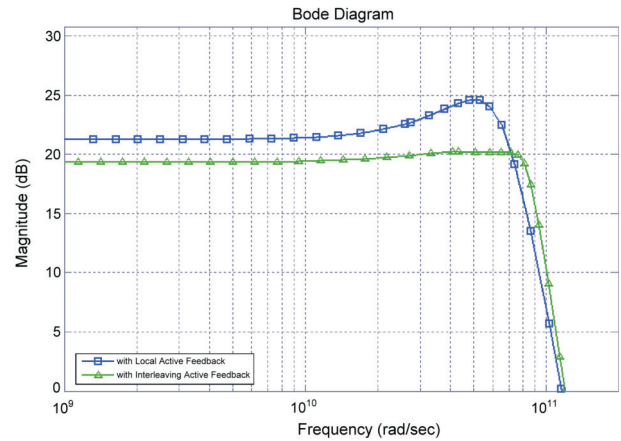
Figure 13. Simulated frequency response of the two-stage gain cells with and without interleaving active feedback.
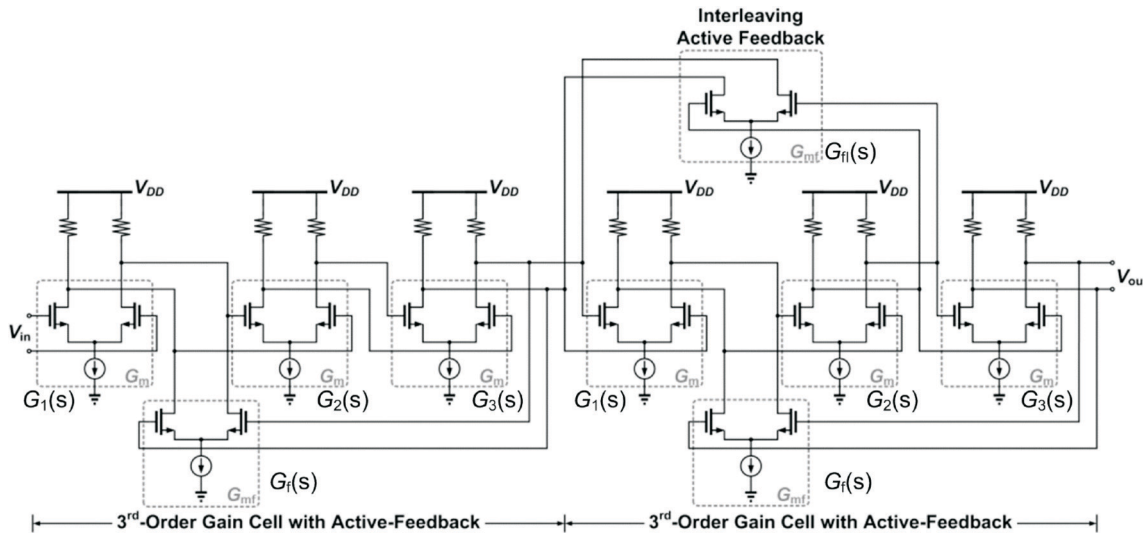
Figure 12. Realization of two-stage third-order gain cells with interleaving active-feedback architecture.
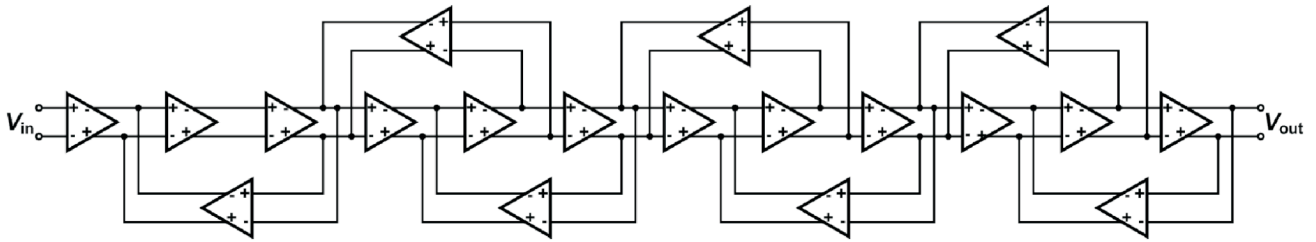
Figure 14. Overall LA core realized with interleaving active feedback.

four stages of gain cells with three interleaving active feedback cells placed between adjacent gain cells.

4.2 Offset Subtracter and Cancellation Circuit

The offset cancellation comprises an offset subtracter and a low-pass filter, as shown in Figure 15. R_F and C_F in the feedback path function as a low-pass filter to extract the output dc level of the gain stage. The lower corner frequency of such RC LPF usually has to sit in the range of several tens of kilohertz, yielding large R_F and C_F.

4.3 Output Buffer

A buffer driving the off-chip loads usually suffers from low bandwidth owing to the large transistors for large driving capability [6]. However, large transistors result in large capacitive loads to the output of the preceding LA core, bringing the overall bandwidth a bottle-neck to meet the required specification. To solve such problem, an f_T doubler is adopted as the output butter [1]. As depicted in Figure 16, the circuit quarters the input capacitance while maintaining the driving capability.

5. Simulation Results

The TIA and LA have been designed in standard 0.18-μm CMOS technology with a 1.8-V supply. Figures 17 and 18 show the layouts of the proposed TIA and LA with 106 μm × 100 μm and 1500 μm × 350 μm of area cost, respectively. They are both simulated with Hspice. Figure 19(a) plots the frequency response of the TIA. With a photodiode capacitance of 300 fF, the total tran-simpedance gain is 56 dBΩ, and the -3-dB bandwidth is 8.27 GHz. Figure 19(b) is the simulated eye diagram for
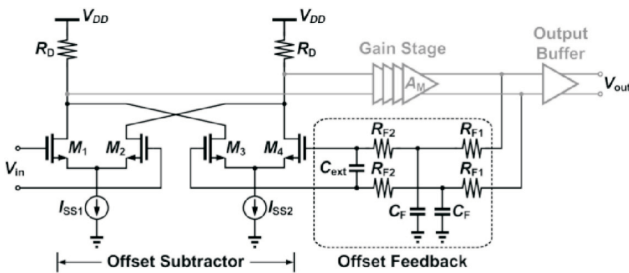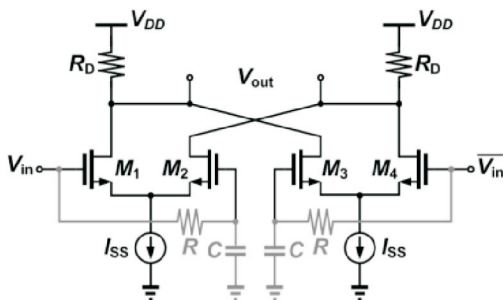

Figure 15. Offset cancellation.

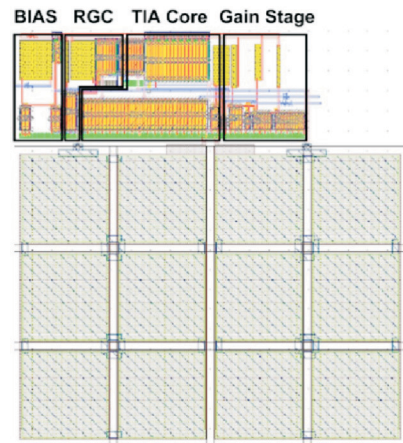**Figure 16.** The f_T doubler.

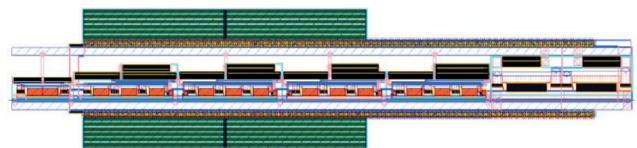
Figure 17. The layout of the proposed TIA.

**Figure 18.** The layout of the proposed TIA.

the TIA with an 8-bit BER PRBS input, indicating an output voltage swing of 10 mV$_{pp}$. Table 3 summarizes the performance of the TIA.

Figure 19(c) shows the frequency response of the proposed LA. With a load capacitance of 300 fF, the overall differential voltage gain is 44.5 dB, and the -3-dB bandwidth is 10.3 GHz. Figure 19(d) shows the simulated eye diagram of the LA with the same PRBS pattern as the one for TIA, revealing a differential output voltage swing of about 1.6 V$_{pp}$. Table 4 lists the performance of the LA.

6. Conclusion

In this work, the performance of a transimpedance amplifier and a limiting amplifier for 10-Gb/s systems in 0.18-μm CMOS technology are presented. The system design with MATLAB offers quick system verification and an efficiently architectural decision for circuit design. The TIA employs some broadband techniques such as RGC configuration, active-inductor peaking, and intersecting active feedback. The LA also uses some techniques including interleaving active feedback and f_T
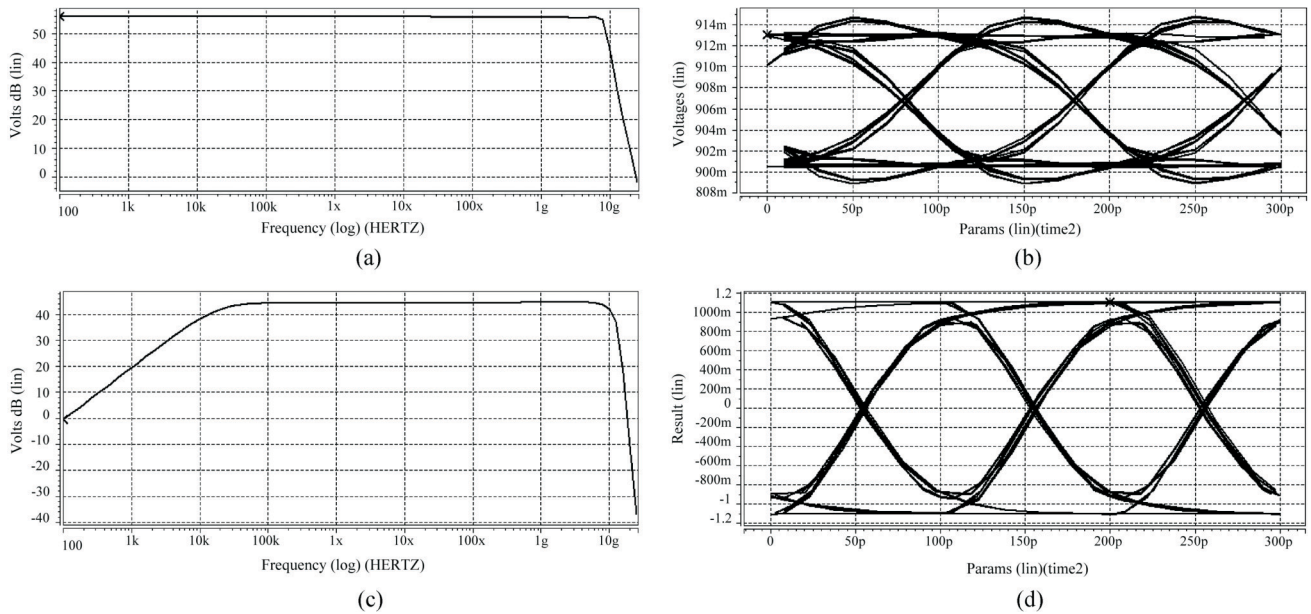
Figure 19. TIA simulation results: (a) Frequency response and (b) eye diagram for a 10-Gb/s PRBS input. LA simulation results: (c) Frequency response and (d) eye diagram for a 10-Gb/s PRBS input.

Table 3. Performance comparison of 10-G/bs TIAs with $FoM = \dfrac{R_T \cdot BW}{Power\ Dissipation}$

Parameter	[4]	[7]	[8]*	[9] *	This Work
Technology (μm)	0.18	0.18	0.18	0.18	0.18
Supply Voltage (V)	1.8	1.8	1.8	1.8	1.8
PD Cap. (fF)	300	300	250	-	300
R_T (dBΩ)	61	58	61	50	56
BW (GHz)	7.7	6.3	7.2	8	8.27
Power (mW)	-	-	70.2	33	35
Inductor	No	No	Yes	Yes	No
FoM (Ω-GHz/mW)	-	-	115.1	76.7	149.1
Area Cost (mm^2)	0.03	0.770	0.140	0.182	0.011

*Measured results

Table 4. Performance comparison of 10-G/bs LAs with $FoM = \dfrac{Gain \cdot BW}{Power\ Dissipation}$

Parameter	[5]*	[6]*	[7]	[9]*	This Work
Technology (µm)	0.18	0.18	0.18	0.18	0.18
Supply Voltage (V)	1.8	1.8	1.8	1.8	1.8
Load Cap. (fF)	-	-	-	150	300
Diff. Gain (dB)	42	50	37	46	44.5
BW (GHz)	9	9.4	6.7	8.4	10.3
Power (mW)	189	150	-	185	226
Inductor	No	Yes	No	Yes	No
FoM (GHz/mW)	6.0	19.8	-	9.1	7.7
Area Cost (mm²)	0.192	0.750	0.770	1.012	0.543

*Measured results

doubler. Those techniques make it possible for inductor-less circuits to operate at a high speed with less area cost. Table 3 compares the performance of the proposed TIA with that of prior works. It shows that the proposed TIA has the most efficiency in power by employing the intersecting active feedback technique. Also, the performance comparison of the LA with other works is summarized in Table 4. Both of the proposed circuits fit to the system specifications.

Acknowledgement

References

[1] Razavi, B., *Design of Integrated Circuits for Optical Communications,* McGraw Hill (2003).

[2] Galal, S. and Razavi, B., "40-Gb/s Amplifier and ESD Protection Circuit in 0.18-µm CMOS Technology," *IEEE J. Solid-State Circuits,* Vol. 39, pp. 2389–2396 (2004).

[3] Park, S. M. and Yoo, H. J., "1.25-Gb/s Regulated Cascode CMOS Transimpedance Amplifier for Gigabit Ethernet Applications," *IEEE J. Solid-State Circuits,* Vol. 39, pp. 112–121 (2004).

[4] Chan, C. T. and Chen, O. T. C., "Inductor-Less 10Gb/s CMOS Transimpedance Amplifier Using Source-Follower Regulated Cascode and Double Three-Order Active Feedback," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS),* May, pp. 5487–5490 (2006).

[5] Huang, H. Y., Chien, J. C. and Lu, L. H., "A 10-Gb/s Inductorless CMOS Limiting Amplifier with Third-Order Interleaving Active Feedback," *IEEE J. Solid-State Circuits,* Vol. 42, pp. 1111–1120 (2007).

[6] Galal, S. and Razavi, B., "10-Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18-µm CMOS Technology," *IEEE J. Solid-State Circuits,* Vol. 38, pp. 2138–2146 (2003).

[7] Chan, C. T. and Chen, O. T. C., "A 10Gb/s Optical Reciever Using Modified Regulated Cascade Scheme," in *Proc. IEEE Midwest Symp. Circuits and Systems (MWSCAS),* Vol. 1, pp.171–174 (2005).

[8] Wu, C. H., Lee, C. H., Chen, W. S. and Liu, S. I., "CMOS Wideband Amplifiers Using Multiple Inductive-Series Peaking Technique," *IEEE J. Solid-State Circuits,* Vol. 40, pp. 548–552 (2005).

[9] Chen, W. Z., Cheng, Y. L. and Lin, D. S., "A 1.8-V 10-Gb/s Fully Integrated CMOS Optical Receiver Analog Front-End," *IEEE J. Solid-State Circuits,* Vol. 40, pp. 1388–1396 (2005).

[10] Kim, H. H., Chandrasekhar, S., Burrus, Jr., C. A. and Bauman, J., "A Si BiCMOS Transimpedance Amplifier for 10-Gb/s SONET Receiver," *IEEE J. Solid-State Circuits,* Vol. 36, pp. 769–776 (2001).

[11] Kim, H. and Bauman, J., "A 12 GHz 30 dB Modular BiCMOS Limiting Amplifier for 10 Gb SONET Receiver," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,* Feb., pp. 160–161 (2000).