Designing an Ultralow-Voltage Phase-Locked Loop Using a Bulk-Driven Technique

Yu-Lung Lo, Wei-Bin Yang, *Member, IEEE*, Ting-Sheng Chao, and Kuo-Hsing Cheng, *Member, IEEE*

***Abstract*—This brief describes an ultralow-voltage phase-locked loop (PLL) using a bulk-driven technique. The architecture of the proposed PLL employs the bulk-input technique to produce a voltage-controlled oscillator (VCO) and the forward-body-bias scheme to produce a divider. This approach effectively reduces the threshold voltage of the MOSFETs, enabling the PLL to be operated at an ultralow voltage. The chip is fabricated in a 0.13-μm standard CMOS process with a 0.5-V power supply voltage. The measurement results demonstrate that this PLL can operate from 360 to 610 MHz with a 0.5-V power supply voltage. At 550 MHz, the measured root-mean-square jitter and peak-to-peak jitter are 8.01 and 56.36 ps, respectively. The total power consumption of the PLL is 1.25 mW, and the active die area of the PLL is 0.04 mm^2.**

***Index Terms*—Bulk driven, forward body bias (FBB), phase-locked loop (PLL), ultralow voltage, voltage-controlled oscillator (VCO).**

I. Introduction

IN MODERN wireless communication systems, handheld electronic products have become essential in daily life. In the design of handheld electronic products, reducing power consumption to extend the lifetimes of batteries and the products themselves is important. The total power consumption of a circuit can be approximated as the sum of $\alpha C_{\rm eq} V_{\rm DD}^2 f$ and $I_{\rm off} V_{\rm DD}$. Therefore, reducing the operating voltage is the best way to reduce power consumption. However, in practice, reducing the operating voltage commonly means reducing the operating frequency. Therefore, attention must be paid to increasing the frequency of operation while reducing the voltage.

Phase-locked loops (PLLs) are important blocks in wireless communication systems and are regarded as one of the most power-consuming components. The voltage-controlled oscillator (VCO) and the frequency divider (prescaler or programmable counter) are fundamental blocks of a high-frequency synthesizer. The VCO is the major contributor to the PLL output phase noise outside the bandwidth of the PLL loop. A linear control characteristic of the VCO and a small VCO gain $K_{\rm VCO}$ can reduce the PLL phase noise and significantly improve spur performance. However, the voltage-to-current (V–I) characteristic of the VCO determines the linearity of $K_{\rm VCO}$, and it is difficult to design a linear V–I characteristic of the VCO with a low supply voltage. Therefore, the design of a highly linear VCO gain that can operate with a low supply voltage is very challenging.

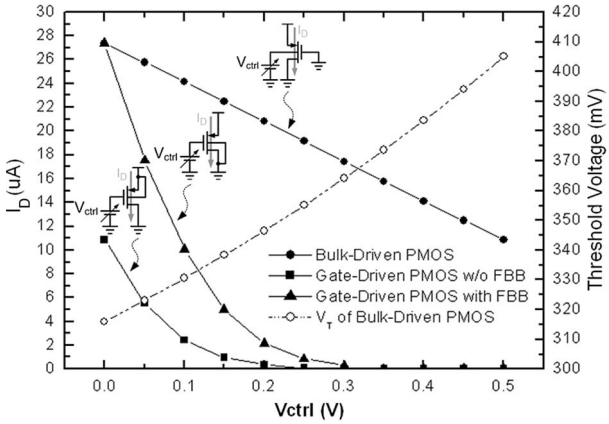

Fig. 1. Characteristics of gate- and bulk-driven PMOS transistors.

A significant problem in mixed-signal circuit design is that reducing the size of technological features requires proportional downscaling of the supply voltage to maintain device reliability, although the transistor threshold voltage V_T still remains fairly high [1]. Various approaches for ultralow-voltage circuit design have recently been developed to compensate for the performance degradation that is associated with the scaling down of supply voltages. These approaches include the bulk-driven technique [1]–[3] for analog circuits and the body-biasing scheme [4], [5] for digital circuits.

In this brief, the bulk-input and forward-body-bias (FBB) techniques are adopted to enable operation at supply voltages of as low as 0.5 V, to solve the threshold voltage problem. This brief is organized as follows. Section II discusses the bulk-driven technology. Section III describes the design of the ultralow-voltage PLL. Section IV presents simulation and measurement results. Finally, Section V draws conclusions.

II. Bulk-Driven Technique

The most important solution to the threshold voltage limitation is the bulk-driven (or bulk-input) technique, which is typically applied in implementing operational amplifier designs in low-voltage analog circuits [2]. The bulk-driven MOSFET has numerous important advantages. The most important advantage is the depletion characteristic, which allows zero, negative, and even small positive bias voltages to achieve the desired dc currents, extending input common-mode ranges that could not otherwise be achieved at low power supply voltages.

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Y.-L. Lo is with the Department of Microelectronics Engineering, National Kaohsiung Marine University, Kaohsiung 811, Taiwan (e-mail: yllo@mail.nkmu.edu.tw).

W.-B. Yang is with the Department of Electrical Engineering, Tamkang University, Taipei 251, Taiwan (e-mail: robin@ee.tku.edu.tw).

T.-S. Chao is with the Industrial Technology Research Institute (ITRI), Hsinchu 300, Taiwan (e-mail: AnsonChao@itri.org.tw).

K.-H. Cheng is with the Department of Electrical Engineering, National Central University, Jungli 320, Taiwan (e-mail: cheng@ee.ncu.edu.tw).

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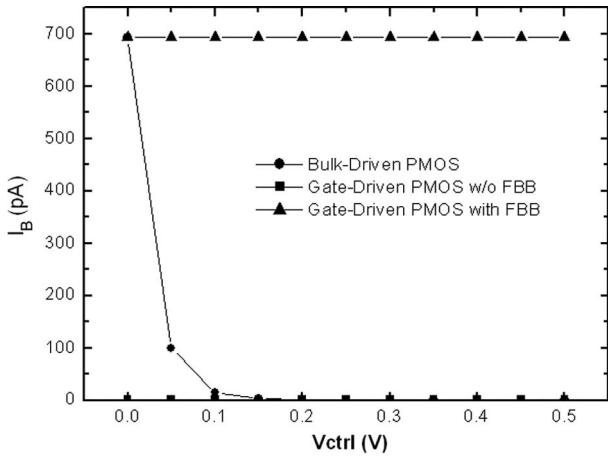

Fig. 2. Bulk leakage current of gate- and bulk-driven PMOS transistors.

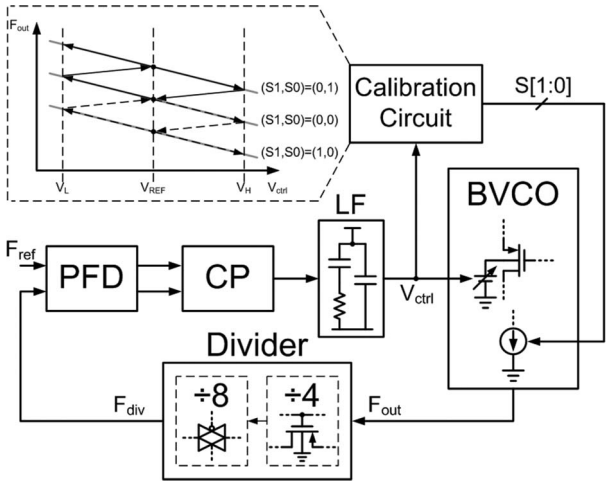

Fig. 3. Architecture of the proposed PLL.

In normal circuit design, the bulk terminals of MOSFETs are always connected to the highest (or lowest) voltage in the circuit for PMOS (or NMOS) transistors, to avoid forward biasing of the bulk–source junction, which can cause the latch-up problem. In a 0.5-V design, no risk of forward biasing of this junction exists, and the bulk terminal can be used with a rail-to-rail input without reservation [1]. Fig. 1 shows the characteristics of the gate- and bulk-driven PMOS transistors. In the gate-driven PMOS without FBB, the source-to-gate voltage must be greater than the absolute value of the threshold voltage, which is approximately 0.4 V. Nevertheless, the bulk-driven technique can eliminate the limitation in the operating current that is caused by V_T, yielding a linear current. For a fixed transistor size ($W/L = 1.2\ \mu\text{m}/0.13\ \mu\text{m}$), the maximum currents of the gate-driven PMOS without FBB and the bulk-driven PMOS are 10.9 and 27.4 μA, respectively. Additionally, the V_T of the bulk-driven PMOS transistor is reduced from 405 to 315 mV.

The leakage current of the MOSFET is a critical problem in low-power circuit design, particularly when body-biasing or bulk-input approaches are adopted. The effect of such a leakage current can be simulated by sweeping the control voltage (V_{GS} and V_{BS}) of PMOS transistors. The leakage current I_B of the bulk terminal in the bulk-driven PMOS is less than 700 pA under all conditions, as shown in Fig. 2. Therefore, the bulk-driven technique can remove the threshold voltage requirements, and these devices can operate even at 0.5 V (for $V_T \approx 0.4$ V). In this brief, the proposed VCO employs only the depletion characteristic of the bulk-driven PMOS transistors to support a rail-to-rail input range and to meet the low supply-voltage requirement.

III. Ultralow-Voltage PLL Design

Fig. 3 shows the architecture of the proposed 0.5-V PLL. It consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a bulk-input VCO (BVCO), a divider, and a calibration circuit. To enable the BVCO to operate at an ultralow voltage, the bulk-input technique is utilized. The current source of the BVCO is digitally controlled using a 2-bit word (S1, S0) via the calibration circuit to select the optimum frequency subband that covers the desired frequency for process, voltage, and temperature (PVT) variations. A divider with a division ratio of 32 is implemented using the proposed FBB floating-input D flip-flop (FBB-FIDFF) to form a divide-by-4 counter as the first stage; the second stage utilizes the traditional transmission-gate DFFs (TGDFF) to form a divide-by-8 counter. The self-calibration technique is adopted to accommodate the PVT variations in this PLL. The calibration circuit monitors the voltage of the loop filter V_{ctrl}, which is compared with a voltage range (between V_L and V_H) until V_{ctrl} settles within the desired voltage range. A zigzag track is applied to the PLL according to a self-calibration technique, although the voltage and temperature change. The loop filter is connected to V_{DD} instead of ground, to reduce supply noise coupling. Therefore, the relative voltage variation of V_{BS} in the PMOS transistor of the BVCO is fixed.

A. BVCO

A VCO is a key element in a PLL and critically determines the performance of a PLL. However, low supply-voltage operation is very difficult to achieve with high-frequency oscillation. Research has been performed on ultralow-voltage VCOs in RF circuits [6], [7]. Although an LC-tank oscillator offers some possibilities for improving noise performance, it depends on passive resonant elements that increase the chip area overhead. Additionally, an integrated LC-tank oscillator typically has a narrow tuning range, such that the performance of the frequency synthesizer is sensitive to process variations. In this brief, the bulk-input technique is employed to implement a VCO design to improve the operating frequency at a lower supply voltage. Fig. 4 shows the circuit configuration of the proposed BVCO. The proposed BVCO consists of a three-stage fully differential ring oscillator and a differential-to-single-ended converter. The fully differential structure can effectively reject common noise that is produced by power supply fluctuations or substrate noise coupling. The NMOS transistors M1 and M2 in the delay element are used for the positive feedback circuit to reduce the transition time of the output and ensure that the logic state, once established, is insensitive to supply-voltage variations. The bulk terminals of the PMOS transistors in the delay elements are directly controlled by the loop filter voltage V_{ctrl}. Therefore, the bulk-input technique can extend the dynamic range of the control voltage to rail-to-rail to provide a highly linear gain without a V–I converter.

The programmable current source I_{vco} is digitally controlled using a 2-bit word (S1, S0) from the calibration circuit to

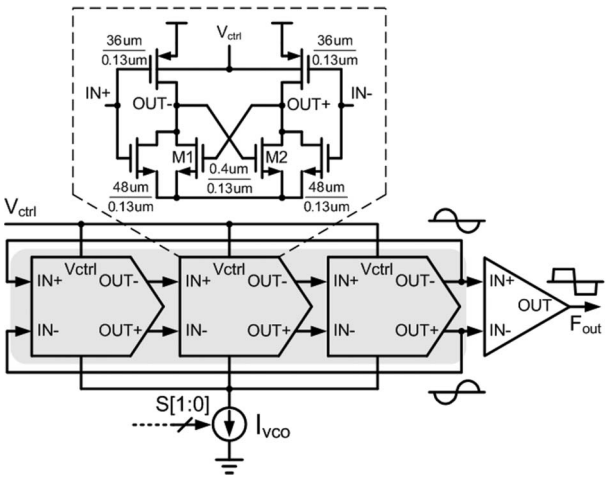

Fig. 4. Architecture of the proposed BVCO.

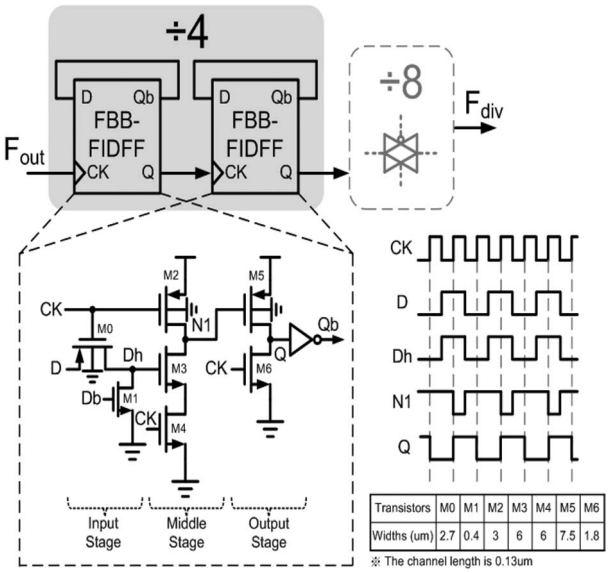

Fig. 5. Proposed divider and FBB-FIDFF.

prevent PVT variations and maintain the desired operating frequency. In addition, the biasing tail current source can reduce the sensitivity of the ground noise. The differential-to-single-ended converter is adopted to obtain the full-swing output signal and reduce the rising/falling time to drive the first stage of the frequency divider.

B. Divider Circuit

Fig. 5 shows the divider circuit, which is a divide-by-32 divider circuit. In the first stage, a divide-by-4 counter with the FBB-FIDFFs is the critical high-speed part. The divide-by-8 counter with the TGDFFs is the low-speed part in the second stage and can reduce the power consumption of the divider. Numerous examples of DFFs that are based on the true single-phase clock (TSPC) for high-speed applications have been presented, such as the extended TSPC (E-TSPC) DFF [8]. The proposed FBB-FIDFF consists of the floating input part in the input stage, the N-precharge part in the middle stage, and the clocking pseudo-PMOS inverter in the output stage. The proposed FBB-FIDFF operates as follows: In the precharge mode, the input signal CK falls from high to low, and the input

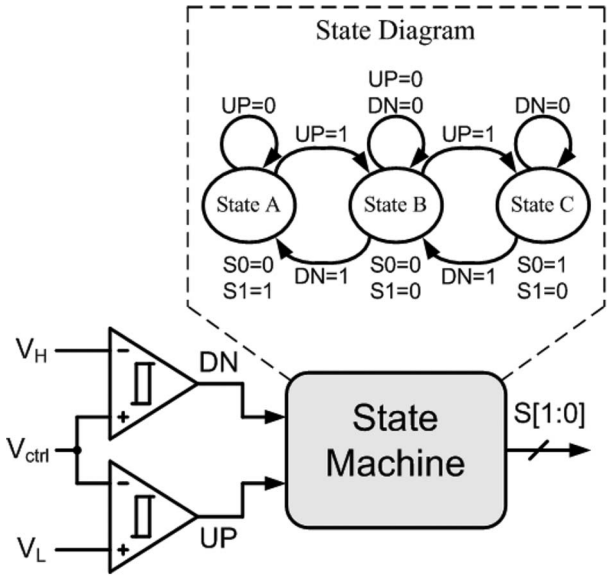

Fig. 6. Calibration circuit and state diagram.

data D are transferred to node Dh, whereas the output node Q keeps its previous value. In the evaluation mode, the input signal CK rises from low to high, and the output node Q is evaluated by the voltage of node Dh. However, the output stage of this DFF is ratioed logic [8], and the sizes of transistors M5 and M6 must be optimized to ensure that the output signal Q has the correct value when the signal CK is high and the value of node N1 is low. Additionally, a small transistor, i.e., M1, is added to ensure that node Dh is at the ground potential, whereas input data D and signal CK are low. In the FBB technique, the bulk terminals of PMOS transistors in the FBB-FIDFF are directly connected to the ground potential to reduce the threshold voltage. Therefore, the proposed FBB-FIDFF can achieve high-speed operation at a low supply voltage.

C. Calibration Circuit

A large VCO gain $K_{\rm VCO}$ can severely degrade the PLL phase noise and spur performance. To guarantee a small $K_{\rm VCO}$ under all PVT conditions, the multirange VCO with calibration has been developed [9], [10]. In this brief, the calibration circuit is performed using a structure similar to that presented elsewhere [9]. The calibration circuit consists of two comparators with hysteresis and the state machine circuit that is shown in Fig. 6. The two comparators are used to detect when the voltage of the loop filter $V_{\rm ctrl}$ crosses the V_L or V_H threshold and provide a rising edge in the UP and DN signals. The 2-bit word (S1, S0) of the state machine is determined by the UP and DN signals and automatically adjusts the current source $I_{\rm vco}$ of the BVCO under various conditions. The comparators with hysteresis are used to prevent unnecessary switching due to ripple in the control voltage. The state diagram of the state machine indicates that State A corresponds to the lowest frequency range, and the 2-bit word (S1, S0) is (1, 0). State B corresponds to the middle frequency range, and the 2-bit word (S1, S0) is (0, 0). State C corresponds to the highest frequency range, and the 2-bit word (S1, S0) is (0, 1). Since the threshold voltage values V_L and V_H dominate the input control voltage range of the VCO and the output voltage range of the charge

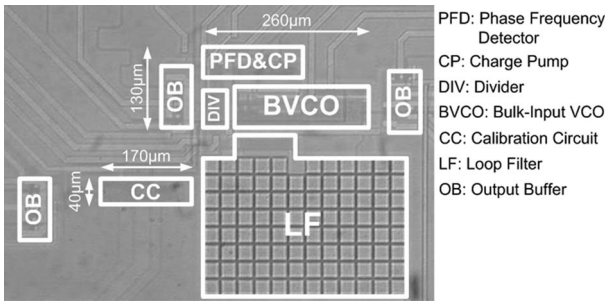

Fig. 7. Microphotograph of the proposed PLL.

TABLE I
COMPARISON RESULTS OF DIVIDE-BY-4 COUNTERS

Divide-by-4 Counter	F_{max} (MHz)	Power (μW)	PDP (fj)
TGDFF	200	2.1	10.5
E-TSPC DFF [8]	694	6.5	9.3
FBB-FIDFF	770	5.0	6.5

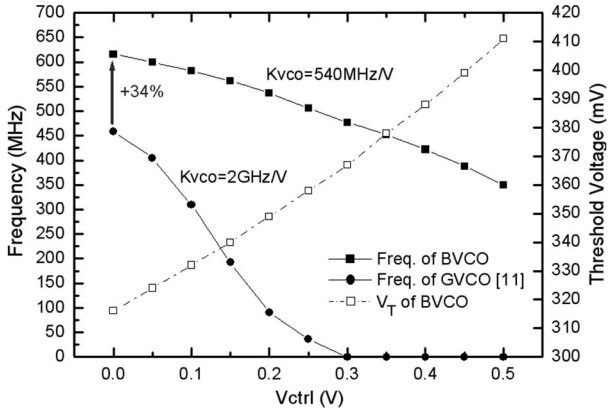

Fig. 8. Simulation results of the proposed BVCO and the GVCO.

pump, the various voltages were optimized to cover the desired frequency with PVT variations using an HSPICE simulation.

IV. SIMULATION AND MEASUREMENT RESULTS

The proposed PLL is demonstrated in a 0.13-μm N-well CMOS process, and the active die area of the PLL is 0.04 mm^2. Fig. 7 shows a microphotograph of this PLL. To verify that the proposed FBB-FIDFF can be operated at a low voltage, the divide-by-4 counter is simulated to compare the performance of the proposed FBB-FIDFF, TGDFF, and E-TSPC DFF [8] at the SS corner at a supply voltage of 0.5 V, as shown in Table I. The operating frequency of the divide-by-4 counter with the FBB-FIDFF is up to 770 MHz, and its power consumption is 5.0 μW. The power–delay product (PDP) of the proposed divide-by-4 counter with the FBB-FIDFF can be reduced by over 38% and 30% from those of the divide-by-4 counter with the TGDFF and E-TSPC DFF, respectively.

Fig. 8 compares the proposed BVCO with the previous gate-input VCO (GVCO) [11] at a supply voltage of 0.5 V. Under given simulation conditions, the bulk terminals of PMOS transistors in the BVCO are directly controlled by the control voltage $V_{\rm ctrl}$, and the bias voltage is fixed at a value of the 2-bit word (S1, S0), which is (0, 0). In the GVCO, the gate nodes V_p of PMOS transistors in the delay elements are also directly controlled by $V_{\rm ctrl}$ from 0 to 0.5 V. As a result, the maximum

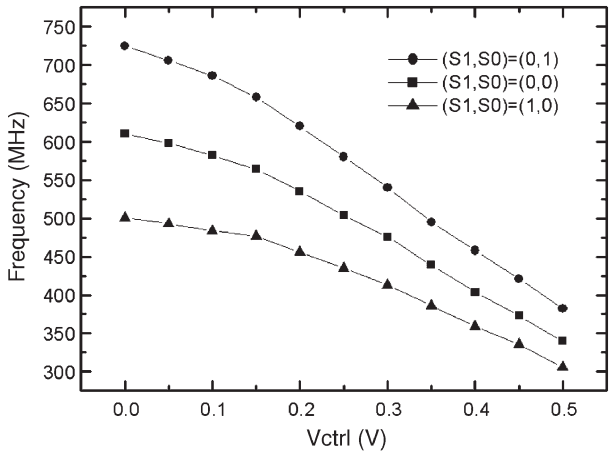

Fig. 9. Measurement results of $V_{\rm ctrl}$–frequency characteristics.

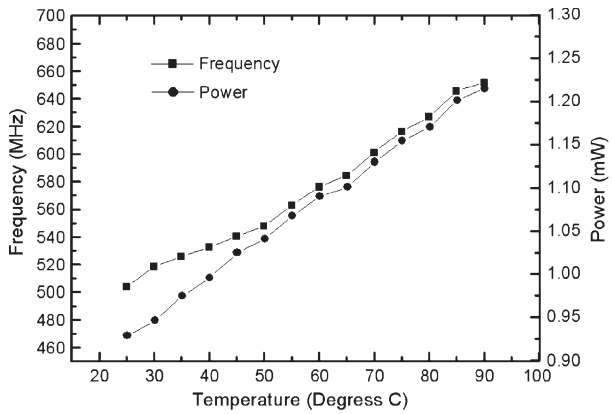

Fig. 10. Measured BVCO frequency and power consumption at different temperatures.

oscillation frequencies of the BVCO and GVCO are 616 and 459 MHz, respectively. The frequency range of the BVCO is from 616 to 350 MHz, in which $V_{\rm ctrl}$ varies from 0 to 0.5 V, and the threshold voltage V_T of the PMOS transistor is reduced to 310 mV. Therefore, the BVCO eliminates the limitation on the operating frequency that is caused by V_T. The dynamic range of the control voltage can be extended rail-to-rail, and $K_{\rm VCO}$ can then be reduced. The lower $K_{\rm VCO}$ is associated with lower phase noise and improved power supply rejection. Fig. 9 shows the measurement results of $V_{\rm ctrl}$–frequency characteristics. The measured BVCO frequency range is from 725 to 306 MHz, over which $V_{\rm ctrl}$ varies from 0 to 0.5 V with three digital control states, indicating that the BVCO has a highly linear $K_{\rm VCO}$, with $V_{\rm ctrl}$ from 0.15 to 0.5 V and an average $K_{\rm VCO}$ of 640 MHz/V.

In sub-1-V CMOS designs, issues of temperature and latch-up should be considered. The threshold voltage decreases as the temperature increases [5]. Therefore, the worst-case circuit performance at low temperatures must be simulated. Additionally, the latch-up immunity must be guaranteed under a wide range of operating conditions. Fig. 10 shows the measured BVCO frequency and power consumption at various temperatures. The measurement results are based on the 2-bit control signals (S1, S0), i.e., (0, 0), and the bulk terminals of PMOS transistors of the BVCO are at 0.25 V. According to the measurement results, the BVCO can fully operate from 25 °C to 90 °C with less leakage current. The measured plot of the phase noise is

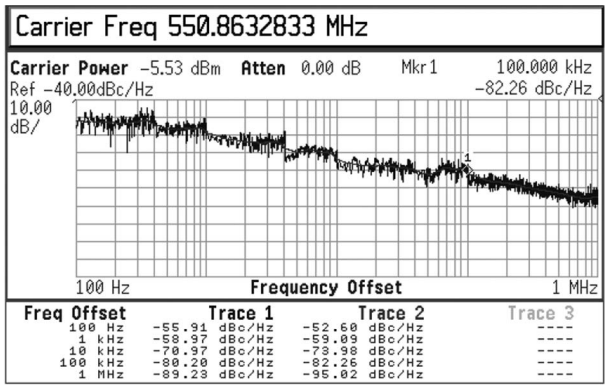

Fig. 11. Measured phase noise of the BVCO.

TABLE II
COMPARISON RESULTS OF SUB-1-V VCOS

Performance Parameter	REF [6]	REF [7]	This work
Supply Voltage	0.5V	0.34V	0.5V
VCO Type	LC	LC	Ring
VCO Tuning Range	3.65GHz~ 3.96GHz	1.06GHz~ 1.14GHz	306MHz~ 725MHz
Phase noise @ 1-MHz offset	-119dBc/Hz @ 3.8GHz	-121dBc/Hz @ 1.14GHz	-95dBc/Hz @ 550MHz
Power Consumption	570μW @ 3.8GHz	103.7μW @ 1.14GHz	210μW @ 550MHz
Area	0.23mm^2	0.49mm^2	0.017mm^2

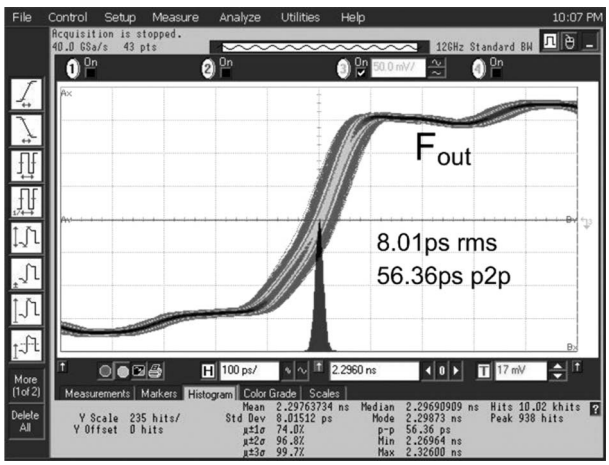

Fig. 12. Jitter histogram at 550 MHz with a 0.5-V supply voltage.

shown in Fig. 11. The resulting phase noise is −82.3 dBc/Hz at a 100-kHz offset and −95.0 dBc/Hz at a 1-MHz offset. Table II compares the performance of recently developed state-of-the-art sub-1-V VCOs. The comparison indicates that the proposed BVCO has a wider tuning range than that in [6] and [7] and the smallest area. Fig. 12 shows the jitter histogram of the PLL clock output at 550 MHz with a 0.5-V quiet supply voltage; the measured root-mean-square (RMS) jitter is 8.01 ps, and the peak-to-peak jitter is 56.36 ps ($>$ 10 000 hits). Moreover, when a single 0.5-V solar power with 50.5-mV supply noise was used, the peak-to-peak jitter increased to 67.27 ps. Table III summarizes the performance of the proposed PLL.

TABLE III
PERFORMANCE SUMMARY

Process	0.13-μm N-well CMOS
Supply Voltage	0.5V
PLL Locking Range	360MHz~610MHz
RMS Jitter @ 550MHz	8.01ps (quiet supply) 8.76ps (solar cell)
Pk-Pk Jitter @ 550MHz	56.36ps (3.1%) (quiet supply) 67.27ps (3.7%) (solar cell)
Power Consumption	1.25mW @ 550MHz
Locking Time	$<4.7\mu$s
Active Die Area	0.04mm^2

V. CONCLUSION

In this brief, the proposed PLL used bulk-input and FBB techniques to enable it to be operated at supply voltages of as low as 0.5 V, to circumvent the threshold voltage problem. The BVCO used the bulk-input technique to achieve a small $K_{\rm VCO}$ and, thus, reduce the phase noise and ensure a highly linear $K_{\rm VCO}$ characteristic. The measured BVCO frequency range was from 725 to 306 MHz. The FBB-FIDFF employed FBB and floating-input techniques in the divider circuit to improve the operating speed at a low supply voltage. The self-calibration technique was applied to prevent PVT variations and maintain the desired operating frequency. The proposed PLL was fabricated using standard 0.13-μm N-well CMOS technology with a nominal voltage of 1.2 V. The total power consumption of the PLL was 1.25 mW at an operating frequency of 550 MHz with a 0.5-V supply voltage. The measured RMS jitter and peak-to-peak jitter were 8.01 and 56.36 ps, respectively.

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