High Efficient 3-input XOR for Low-Voltage Low-Power High-Speed Applications

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Abstract

A new 3-Input XOR gate based upon the pass transistor design methodology for low-voltage, low-voltage high-speed applications is proposed. Five existed circuits are compared with the new proposed gate. It is shown that the proposed new circuit has at least 50% improvement in power-delay product than the CPL structure and than the CMOS structure. Moreover, the proposed new circuit could also be operated as low as 1V. Thus, the proposed new circuit is suitable for low-power, low-voltage and high-speed applications.

I. Introduction

At gate design level , a proper choice of a circuit style for implementing combinational circuits is very important. Depend on the applications, for example, a low-power and low-voltage requirement or a high-speed and low power-delay product requirement, different types of circuits may be adopted. The objective of this work is to propose a better solution to fit various kinds of requirements including low-voltage , low-power , power-delay product and operation speed by implementing 3-input exclusive-or (XOR) logic. Because the exclusive-or (XOR) and exclusive-nor (XNOR) functions are fundamental units in various circuits , such as , parity checker , full adder , error detecting , comparator, and so on. In Section II, is introduction of circuit we proposed to meet those requirements. The simulation results and performance comparisons between five existed and one new proposed circuits are shown in Section III. The new proposed circuit has the best power-delay product at all supply voltages in all circuits. Finally, some conclusions are shown in Section IV .The performance comparisons and simulation results are based upon 0.35-μm CMOS technology and supply voltages are 5V, 3.3V, 2.5V, 2V, 1.5V, 1V, respectively.

II. The proposed circuit

The new proposed 3-input XOR gate using the pass-transistor logic circuit is shown in Fig. 1. circuit (a). The design considerations and circuit operation principles of the proposed new circuit are shown in following:

First we construct the truth table of 3-input XOR gate as shown in Table 1. Then we circle four groups of dash circles term (1) , term(2) , term (3) and term (4) as pass variables. Term (1) pass signal B to output node controlled by $\overline{A}$ and $\overline{C}$ using PMOS p1, p3 and NMOS n4, n5. Term (2) pass signal $\overline{B}$ to output node controlled by $\overline{A}$ and C using PMOS p4, p5 and NMOS n1, n3. Term (3) also pass signal $\overline{B}$ to output node controlled by A and $\overline{C}$ using PMOS p2, p3 and NMOS n4, n6 which is different from term (1). At last , PMOS p4, p6 and NMOS n2, n3 are controlled by A and C pass the signal B in term (4). The proposed circuit are composed by 12 transistors. It has very short transition path and full-swing signal at output. But complimentary input signals are needed.

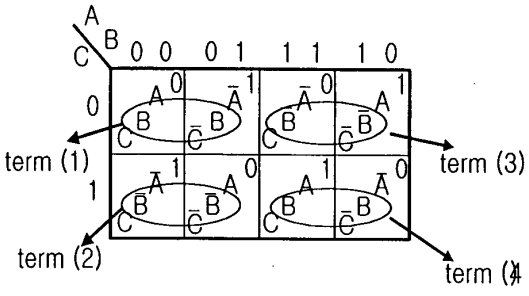
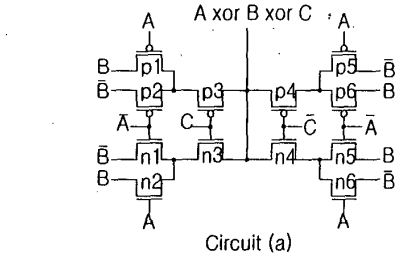
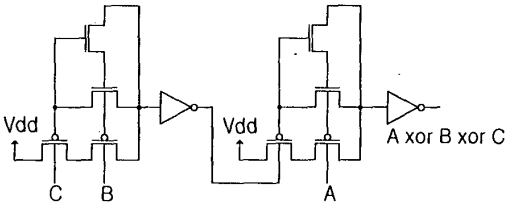


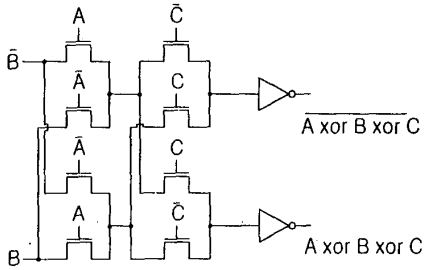
Table 1. 3-input xor truth table



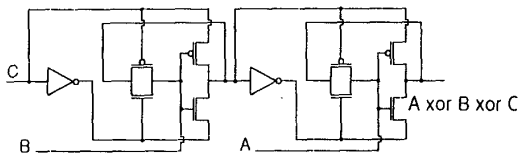
Circuit (a)



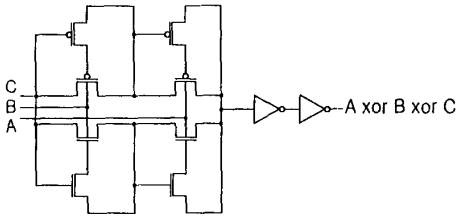
Circuit (b)



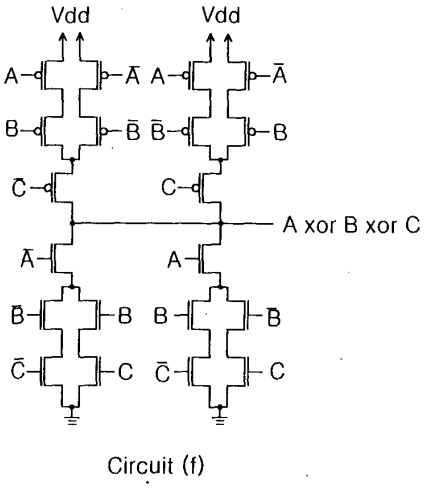
Circuit (c)



Circuit (d)



Circuit (e)



Circuit (f)

Fig. 1. Circuit (a) ~ (f)

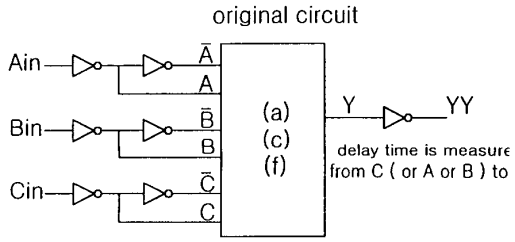
III. The Simulation and Comparison Results

The proposed 3-input XOR gate circuit simulation results are based upon CMOS 0.35-μm technology. Five existed 3-input XOR gate circuits , as shown in Fig. 1. (b)~(f)[1]~[3] , are simulated based upon the same CMOS technology. Fig. 1(b) has the simplest circuit structure for high voltage applications. But for low-voltage applications, it has poor performance due to the cascaded design without complimentary input signals. Fig. 1(c) shows the high-speed CPL circuit structure, but consume most power in all. A classical cascaded good for low-power and low-voltage applications design is shown in Fig. 1(d). Fig. 1(e) is a symmetric structure without complimentary input signals. The static CMOS structure is shown in Fig. 1(f), a good design for low-voltage application but low-speed and area wasted. Two measure circuits for delay and power dissipation simulation are shown in Fig. 2. Due to the pass transistor circuits using the passive MOS switches to implement a given logic function, in order to measure the power dissipation of the original circuits, some inverters are added in front of the input of the original circuits. The inverter after the output of the original circuits is used as an unit fan out loading and to check the output waveform and delay-time. The Grey code which changed one bit at a time is used as the simulation input signals. And the output will appeared "1" and "0" signals take terns which is

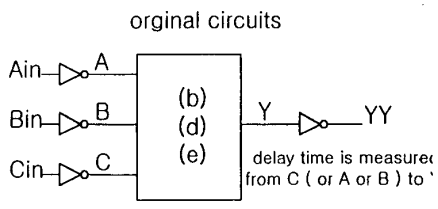
easier for observation and analysis. The average gate delay-time is calculated as shown in Table.3 with the input signals (Gray code) varying from ABC=000 to ABC=100. The simulated supply voltage are 5V, 3.3V, 2.5V, 2V, 1.5V, 1V, respectively. All simulation results are shown in Table (3)~(8).

At high supply voltages (5V or 3.3V), the new proposed circuit(a) has at least 54% improvement in power-delay product than the CPL structure and 57% improvement than the CMOS structure. At low supply voltage(1.5V) the new proposed circuit(a) has at least 79% improvement in power-delay product than the CPL structure and 48% improvement than the CMOS structure. Moreover the new proposed circuit could also be operated as low as 1V.

It is clear that although more transistors are used in the proposed circuit, but it does not mean extra power dissipation due to it's passive transistor switches and full output voltage swing property. So the proposed circuit can be a well design for low-power and low-voltage applications. And when it comes to low-voltage, low-power and high-speed applications the new proposed circuit seems the best choice.



(a) Measure circuit I



(b) Measure circuit II

Fig. 2.

Delay time(nS)									
	000→001→011→010→110→111→101→100→000								ave.
a	0.10	0.26	0.08	0.17	0.10	0.10	0.08	0.16	**0.135**
b	0.35	0.30	0.27	0.12	0.26	0.26	0.28	0.14	**0.253**
c	0.08	0.21	0.11	0.28	0.08	0.02	0.10	0.29	**0.183**
d	0.31	0.23	0.27	0.10	0.26	0.30	0.13	0.03	**0.218**
e	0.23	0.32	0.24	0.34	0.18	0.30	0.24	0.34	**0.278**
f	0.35	0.25	0.27	0.22	0.35	0.32	0.27	0.27	**0.293**

Table. 2 Delay-time measurement for supply voltage at 5v

IV. Conclusion

In this paper, a new design of 3-input XOR gate using Pass-Transistor Logic with modified K-map were presented. The proposed 3-input XOR gate circuit has an excellent performance at power-delay product factor at all supply voltages. At high supply voltages(5V or 3.3V), the new proposed circuit has at least 54% improvement in power-delay product than the CPL structure and 57% improvement than the CMOS structure. At low supply voltage(1.5V) the new proposed circuit has at least 79% improvement in power-delay product than the CPL structure and 48% improvement than the CMOS structure.

	average delay-time (nS)	power (mV)	normalize power-delay product	no.of tran-sistors
a	0.135	0.2732	1.00	18
b	0.253	0.3821	2.61	12
c	0.183	0.5189	2.61	18
d	0.218	0.2478	1.45	12
e	0.278	0.3377	2.53	12
f	0.293	0.3049	2.41	26

Table.3. Supply voltage at 5V

	average delay-time (nS)	power (mV)	normalize power-delay product	no.of tran-sistors
a	0.193	0.1005	1.00	18
b	0.351	0.1290	2.33	12
c	0.267	0.1610	2.21	18
d	0.297	0.0900	1.38	12
e	0.410	0.1138	2.40	12
f	0.397	0.1154	2.36	26

Table.4. Supply voltage at 3V

	average delay-time (nS)	power (mV)	normalize power-delay product	no.of tran-sistors
a	0.263	0.0505	1.00	18
b	0.493	0.0603	2.23	12
c	0.402	0.0697	2.01	18
d	0.405	0.0451	1.37	12
e	0.642	0.0548	2.64	12
f	0.533	0.0576	2.30	26

Table.5. Supply voltage at 2.5V

	average delay-time (nS)	power (mV)	normalize power-delay product	no.of tran-sistors
a	0.364	0.0281	1.00	18
b	0.770	0.0321	2.41	12
c	0.689	0.0342	2.30	18
d	0.564	0.0253	1.39	12
e	1.237	0.0292	3.52	12
f	0.716	0.0322	2.25	26

Table.6. Supply voltage at 2V

	average delay-time (nS)	power (mV)	normalize power-delay product	no.of tran-sistors
a	0.641	0.0125	1.00	18
b	2.210	0.0134	3.68	12
c	3.028	0.0130	4.91	18
d	1.033	0.0117	1.49	12
e	-	-	-	-
f	1.212	0.0141	2.12	26

Table.7. Supply voltage at 1.5V

	average delay-time (nS)	power (mV)	normalize power-delay product	no.of tran-sistors
a	2.414	0.00318	1.00	18
b	-	-	-	-
c	-	-	-	-
d	4.076	0.00319	1.69	12
e	-	-	-	-
f	4.118	0.00363	1.94	26

Table.8. Supply voltage at 1V

Reference

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