The Suggestion for CFS CMOS Buffer

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Abstract

Two recent papers, one by Huang et al. and the other by Cheng et al., on the driver buffer are commented on. The feedback-controlled split-path CMOS buffer (FS) claims that the 4-split-path buffer can reduce the power and power-delay product. But the voltage of the gates in the output inverter stage is not enough to turn-off the PMOS transistor and the NMOS transistor. Due to this, the charge-recovery must be used. The charge-transfer feedback-controlled split-path (CFS) CMOS buffer that has high-speed low-power performance by using transfer the charge stored in the split output-stage driver to the output node. Thus the power-delay product can be reduced greatly by combining the technology described in the former two papers. The HSPICE simulation results show that the power-delay product of the suggestion CMOS buffer is saving 20% to 40% times in comparison to conventional CMOS tapered buffer at 100MHz operation frequency at heavy capacitive load.

1. Introduction

In today's high-speed sub-micron CMOS integrated circuit technology, the increase of clock capacitive load and output buffers capacitive load are due to the increasing of high circuit integration. Such large capacitive load driving circuits take a relatively large portion of total power consumption and circuit delay of the chip[1]. To reduce the power dissipation and circuit delay in the driving buffer is increasingly important for low power high speed VLSI design.

In fixed-tapered buffer design [2] as shown in Fig.1, it consumes both the dynamic switching power dissipation and short-circuit power dissipation. The momentary tri-state (MT) buffer [3] eliminates the short-circuit current in the output stage by tri-stating the output node momentarily. The input signal is split into two paths with different waveform shapers designed by asymmetrical inverters. But the propagation delay time of the MT buffer is also increased due the asymmetrical inverters. The feedback-controlled split-path CMOS buffer (FS) [4] is designed with split output-stage driver paths controlled by the feedback signal to eliminate the short-circuit current. But it changes the logic state of the split output-stage driver twice during each output inverter transition. Thus the large charge stored in the split output-stage driver is waste. The voltage of the gates in the output inverter stage is not enough to turn-off the PMOS transistor and the NMOS transistor in the 4-split-path FS buffer as shown in Fig. 2(b). Due to this, the charge-recovery must be used. Four additional MOS transistors are used as the charge-transfer diodes, which can transfer the charge stored in the split output-stage driver to the output node as shown in Fig. 2(a). Thus the propagation delay and power dissipation of the charge-transfer feedback-controlled split-path CMOS buffer(CFS) [5] are reduced.

In this paper, the charge-recovery technology is used to the 4-split-path CFS CMOS buffer for reducing power-delay product. As shown in Fig.2(a), two additional MOS transistor diodes of the CFS CMOS buffer are used to increase the operation speed of the suggestion CMOS buffer. The power-delay product of the suggestion CMOS buffer is saving 1.2 to 1.4 times than the conventional buffers.

2. The Circuit Structure and Operating Principle

The schematic diagram and operating waveforms of the suggestion CMOS buffer are shown in Fig. 3 (a) and Fig. 3 (b), respectively.

A. Output pull-high operation:

As shown in Fig. 3(b), at the time t1, the input signal rises from 0 to 1 and the output node out keep it's previous state node out 0. Then the node 1na falls from 1 to 0 at t2, the node 4na rises from 0 to 1 at t3, and the node 5p falls from 1 to 0 at t4. Thus the PMOS transistor MP of the output stage is turned on and the output voltage rises from 0 to V_{dd} at t5. After the output pull-high evaluation, outb falls from 1 to 0. Due to the feedback signal outb connected to the NAND gate, the node 1na rises from 0 to 1 at t6, the node 1pa rises from 1 to 0 at t7, and the node 4na falls from 1 to 0 at t8. The node 4pa falls from 1 to 0 at t9, the node 5p rises from 0 to 1 at t10. Thus the output inverter PMOS transistor MP is turned off after the output pull-high operation. Due to the feedback control of the node 5p, the node 1pa falls from 1 to 0 at t11, and the node 4pa rises from 0 to 1 at t12. Thus the PMOS transistor P5a and NMOS transistor N5a are off and the node 5p is tri-stated. During the output pull-high operation, the PMOS transistor MP is only turned on when the input

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rises from 0 to 1. It remains off during the output pull-low operation.

B. Output pull-low operation:

During the time inverter t13-t18, the buffer is operated in the output pull-low operation. When the input signal falls from 1 to 0 at t13. At this time, the node out is 1and the node outb is 0. Then the node 1pb rises from 0 to 1 at t14. The node 4pb falls from 1 to 0 at t15, and the node 5n rises from 0 to 1 at t16. Thus the NMOS transistor MN of the output stage is turned on and the output voltage falls from V_{dd} to 0 at t17. After the output pull-down evaluation, outb rises from 0 to 1. Due to the feedback signal connected to the NOR gate, the node 1pb falls from 1 to 0 at t18, the node 1nb falls from 1 to 0 at t19, and the node 4pb rises from 0 to 1 at t20. The node 4nb rises from 0 to 1 at t21, and the node 5n falls from 1 to 0 at t22. Thus the output inverter NMOS transistor MN is turned off after the output pull-low operation. Due to the feedback control of the node 5n, the node 1nb rises from 0 to 1 at t23, and the node 4nb falls from 1 to 0 at t24. Thus the PMOS transistor P5b and NMOS transistor N5b are off and the node 5n is tri-stated. During the output pull-down operation, the NMOS transistor MN is only turned on when the input falls from 1 to 0. It remains off during the output pull-high operation.

After the output transition operation, the node voltage of the node 5p and 5n are 1 and 0, respectively. The output stage MOS transistor MP and MN are turned off. The node voltage of the node 4pa, 4pb and 4na, 4nb are 1 and 0, respectively. The MOS transistors P5a, N5a, P5b and N5b are turn off. Thus there is no simultaneously turned-on during next transition operation in the last two stage inverters, and the short-circuit current of the last two stage inverters can be eliminated.

C. The charge-recovery operation:

The charge-recovery devices are PMOS transistor Pp and NMOS transistor Np which are shown in Fig. 3(a). After the pull-high operation, the MOS transistor P5a and N5a are off and the node 5p is floating. The voltage of the node 5p is dropped by the couple capacitive (Cgd) in the PMOS transistor MP during the output pull-low operation. Due to this, the PMOS transistor MP is not turned off effectively. Thus the charge-recovery PMOS Pp is used to pull-up the voltage of the node 5p enough to turn off the PMOS transistor MP during the output pull-low operation. The voltage of the node 5p is just to turn off the PMOS transistor MP after the charge-recovery. Thus the PMOS transistor MP is turned on quickly during the output pull-high operation so the propagation delay time is reduced.

After the pull-low operation, the MOS transistor P5b and N5b are off and the node 5n is floating. The voltage of the node 5n is dropped by the couple capacitive (Cgd) in the NMOS transistor MN during the output pull-high operation. Due to this, the NMOS transistor MN is not turned off effectively. Thus the charge-recovery NMOS Np is used to pull-down the voltage of the node 5n enough to turn off the NMOS transistor MN during the output pull–high operation. The voltage of the node 5n is just to turn off the NMOS transistor MN after the charge-recovery. Thus the NMOS transistor MN is turned on quickly during the output pull-low operation so the propagation delay time is reduced.

The HSPICE simulated waveform of the suggestion buffer is shown in Fig. 4. The optimum buffer design for lower propagation delay and lower power dissipation can be achieved by individually sizing the four-split-path.

3. Simulation Results

The comparisons of the various capacitance loads of the conventional tapered buffer(tap_buffer), the feedback-controlled 4-split-path CMOS buffer(FS), the charge-transfer feedback-controlled split-path buffer(CFS) and the suggestion CFS CMOS buffer(SCFS) are shown in Table I. Table II shows the average propagation delay of the four buffers. The HSPICE simulation results are based upon the device parameters of 0.6um 5V CMOS process at 100MHz operating frequency. It is clear that the suggestion CMOS buffer can save of over 20% of power-delay product in comparison to conventional tapered buffer.

4. Conclusion

In this paper, the suggestion CMOS buffer is proposed and analyzed. By using the charge-transfer MOS diodes and feedback control signal, the suggestion CMOS buffer can eliminate the short-circuit power dissipation and improve the operation speed. Simulation result shows that the suggestion CMOS buffer is about 1.2 to 1.4 times faster than that of convention CMOS tapered buffer and consumes less power dissipation at heavy capacitive load. Thus it is suitable for low power high-speed heavy load interconnection applications.

5. References

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TABLE I

average power-delay product (J) (operating frequency 100MHz)				
CAP	tap_buffer	FS	CFS	SCFS
25P	10.36E-11	9.21E-11	8.86E-11	7.72E-11
125P	0.72E-09	0.48E-09	0.59E-09	0.43E-09
625P	0.37E-08	0.28E-08	0.25E-08	0.22E-09

TABLE II

average propagation-delay (s) (operating frequency 100MHz)				
CAP	tap_buffer	FS	CFS	SCFS
25P	1.32E-09	1.13 E-09	1.08E-09	0.94 E-09
125P	1.84E-09	1.27 E-09	1.57E-09	1.16 E-09
625P	1.84E-09	1.45 E-09	1.30E-09	1.15 E-09

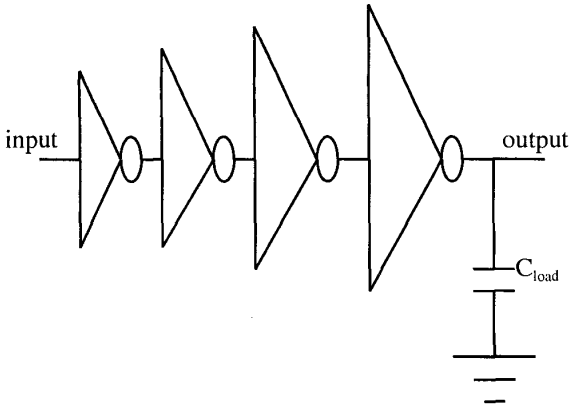
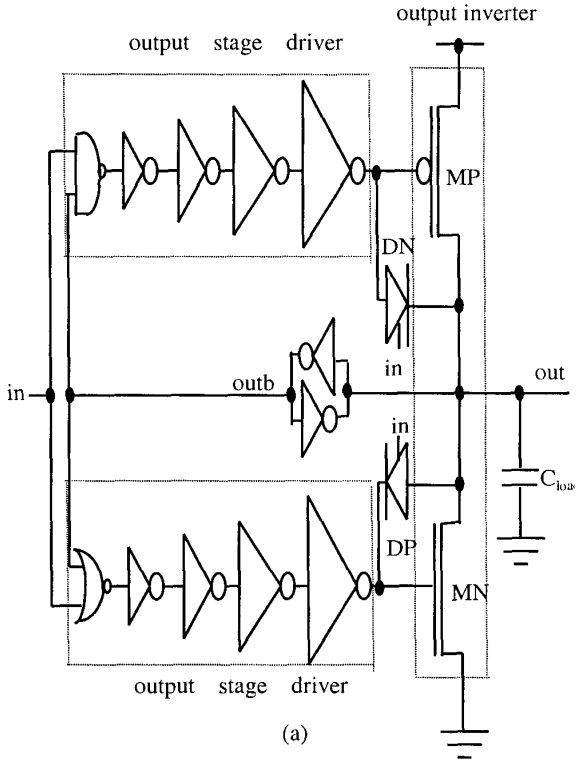


Fig. 1 The tappered buffer



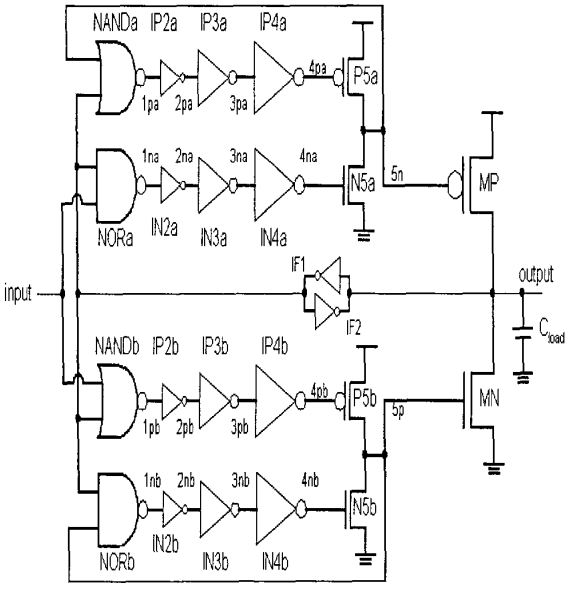
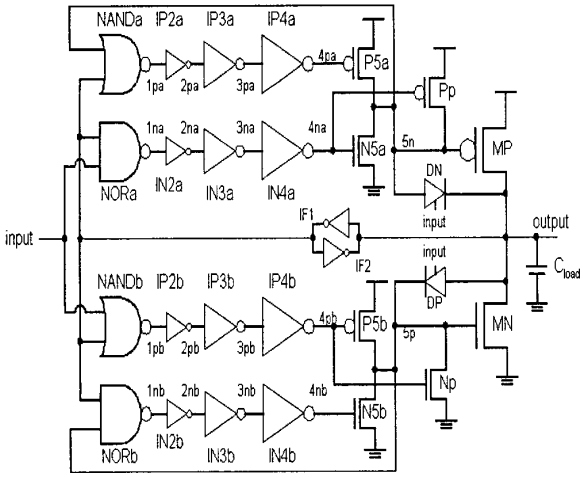
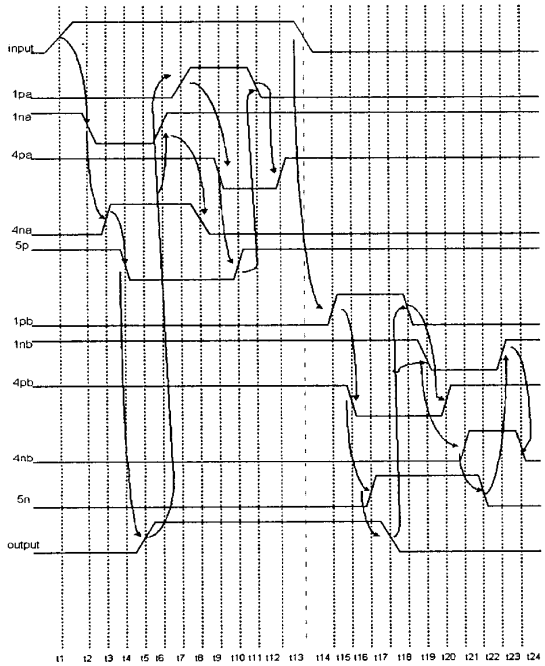


Fig. 2 the circuit structure of (a) the CFS buffer (b) the 4-split-path FS buffer



(a)



(b)

Fig.3 the suggestion CFS CMOS Buffer (a) circuit and (b) timing diagram

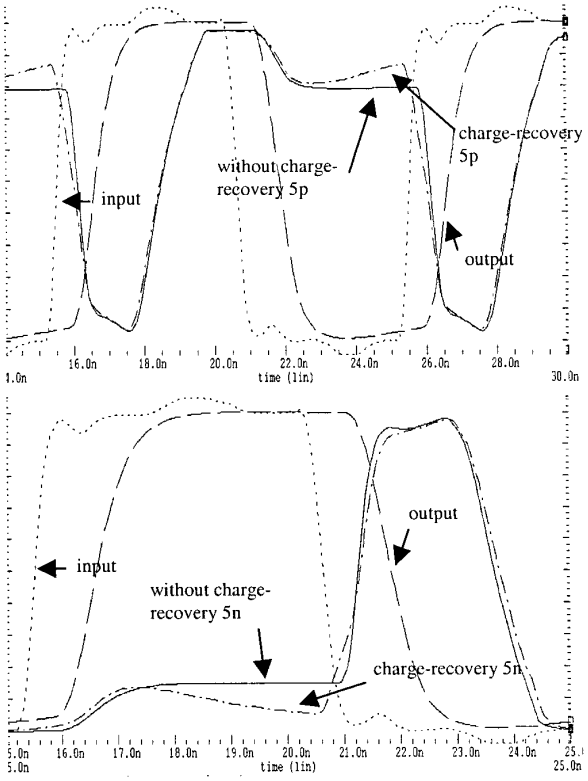


Fig. 4 simulated waveforms of the suggestion CFS CMOS buffer