The Novel Efficient Design of XOR/XNOR function for Adder applications

Kuo-Hsing Cheng* and Chih-Sheng Huang#
Dept. of Electrical Engineering, Tamkang University, Taipei Hsien, Taiwan, R.O.C.
TEL: 26215656 Ext. 2731FAX: 26221565
EMAIL: cheng@ee.tku.edu.tw* cshuang@ee.tku.edu.tw#

Abstract

A new concept to implement high performance XOR/XNOR functions that using pass transistor was proposed, it used only six MOS transistors. Base upon this concept, a new high-speed full adder was proposed for low-power application. We used the modified Karnaugh map (K-map) method to obtain the various pass transistor circuits. We modified the Boolean expression to simplify the control and input signals of the pass transistor logic (PTL) to realize a one-bit full adder. The analysis of proposed one-bit adders were compared with the static CMOS adder, the CPL transmission function adder [1], the DPL transmission gate adder, and the CPL transmission gate adder [2]. The simulation results shows that the proposed new circuit has the fewest power delay product performance.

Ⅰ. Introduction

Since addition is the fundamental operation of the arithmetic unit, the high performance adders for low-power application had been researched. The complementary pass-transistor Logic (CPL) and double pass-transistor logic (DPL) et. al, [2]-[7] are the solutions to the requirements. A pass transistor logic (PTL) circuit design for high speed and low-power adder based upon the modified K-map method is shown. The focus of the adder design is the implementation of XOR/XNOR functions. In Section Ⅱ, we will use the modified K-Map method to obtain the various PTL circuits. In Section Ⅲ, a new implementation of the XOR/XNOR functions for adder application is presented. In Section Ⅳ, a new circuit architecture of full adder is presented. In Section Ⅴ, the comparisons of proposed new adders and others are shown. And finally, a conclusion is given.

Ⅱ. The modified K-map method

The high performance XOR gate using the pass-transistor was proposed by [8]. [7] had a different opinion of the comparison of the static CMOS logic and the PTL circuits for low-voltage low-power applications. In this work, only the two-input XOR function implemented by various PTL circuits are shown. The other functions can use the same method to analysis.

The pass-transistor network is shown in Fig.1. The input signals can be used as the control or pass variables. The basic elements of pass-transistor network are the MOS transistor switches. The control variables are connected to drive the gates of the MOS transistors and the pass variables are connected to the sources/drains of the MOS transistors. The pass-transistor network pass the logic value from the set [0, 1, Xi, Xi', Z], where Xi is input variable and Z is the high impedance state [9].

The pass function shown in Table 1 can use the modified K-map to choose the pass variables and control variables, there are three versions of XOR function as shown in Fig.2, Fig. 3, and Fig. 4 respectively.

As shown in Fig. 2(a), the dash circles term(1) and term(2) of the modified K-map are used to determine the control and pass variables of the two-input XOR gate. The pass variables of term(1) is signal A and term(2) is signal A', where signal A can be passed under control of signal B' and signal A' can be passed under control of signal B. The switch implementations of pass-transistor is shown in Fig. 2(b). It can be implement used only PMOS or NMOS transistors or both used. If the switches only use the NMOS transistors, it is called CPL.

Fig. 3 shows that the pass variables signal B of term(1) is passed under control of signal A', the signal B' of term(2) is passed under control of signal A, the signal A of term(3) is passed under control of signal B', and the signal A' of term(4) is passed under control of signal B. The pass variables of the dash circles have double path to pass the signals, it is called DPL. It keeps the output voltage is full swing.

As shown in Fig. 4 which proposed by [8], term(1) pass signal A under control of signal B using a PMOS transistor, term(2) pass signal B under control of signal A using a PMOS transistor, and term(3) pass 0 under control of signal A and signal B using two NMOS transistors. This will not need complementary input signal, but when (A, B) = (0, 0), the output voltage will not reach to ground, it only pull down to |Vtp|. Attaching a tailing inverter can obtain a full swing XNOR function.

Using the modified K-map method, we can predict which circuits have full output voltage swing and which circuits need complementary control signals. Consequently, from these modified K-maps we can predict the characteristics of these pass-transistor circuits.

Ⅲ. The new circuit structure of XOR

The Boolean equations of a full adder are as follow:

$$Sum = A \oplus B \oplus C \quad (1)$$

$$Carry = AB + BC + AC \quad (2)$$

If we rewrite equations (1) and (2) as follow:

$$P = A \oplus B \quad (3)$$

$$Sum = P'C + PC' \quad (4)$$

$$Carry = P'B + PC \quad (5)$$

We can find that the Boolean equations of Sum and

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Carry are similar. They both pass input signals (B, C or C') under control of signal P or signal P'. As shown in equations (4), (5) and (6), P, i.e. XOR, and P', i.e. XNOR, are the critical functions to implement the Sum and the Carry. Therefore, it is significant to get a well method to implement the control signals P and P'. By the scheme shown in Section Ⅱ, we can use the skills of pass transistor logic (PTL) to implement the XOR/XNOR functions.

We have two new circuit versions of XOR as shown in following:

A. The first version of the proposed new XOR gate.

The first version of the proposed is shown in Fig. 5(a). The signal Pi (XOR function) is implemented by the dash circles term(1) and term(2), and the signal Pi' (XNOR function) is implemented by the dash circles term(3) and term(4).

1. When signals (A, B) = (1, 0), term(1) pass signal A under control of signal B using a PMOS Mp2; and when signals (A, B) = (0, 1), term(2) pass signal B under control of signal A using a PMOS Mp1.
2. When signals (A, B) = (0, 1), term(3) pass signal A under control of signal B using a NMOS Mn2; and when signals (A, B) = (0, 1), term(2) pass signal B under control of signal A using a PMOS Mn1.
3. When signals (A, B) = (0, 0) of function Pi and (A, B) = (1, 1) of function Pi', they both have two paths to propagate. It's operation voltage is limited above 2|Vtp|.
4. The implementations at (A, B) = (1, 1) of function Pi and at (A, B) = (0, 0) of function Pi' are using the feedback MOS transistors Mpf and Mnf to realize.

This structure only uses six MOS transistors to implement both XOR and XNOR functions. It offers the least power consumption and has the simplest circuit structure. But it's operation voltage is limited above 2|Vtp|. Thus it is suitable for higher operating voltage.

B. The second version of the proposed new XOR gate.

The second version of proposed is shown in Fig. 5(b). It can to solve the limited output voltage swing of the structure of Fig. 5(a).

1. We use signal B' to control a NMOS Mn3 to ensure that when (A, B) = (0, 0), the output voltage can be full swing.
2. We use signal B' to control a PMOS Mp3 to ensure that when (A, B) = (1, 1), the output voltage can be full swing.

The implementations of signal Pi and signal Pi' are symmetric, it help each other to pull up or pull down. The output voltages of signal Pi and signal Pi' are full swing, and it's operation voltage is limited above |Vtp|. Thus it can be operated at lower voltage.

Ⅳ. The new architecture of full adder

In order to make the performance comparison, the various full adder implementations are shown as follow:

1. The proposed new full adder: Fig. 6 and Fig. 7 shows the new architecture of the one-bit adders. Since they use PTL, which connected to the input signals and used only six MOS transistors to implement the XOR/XNOR functions, they can reduce the input capacitance. The feedback paths of signal P and signal P' are keep the XOR and XNOR functions complete and symmetric, and make the output nodes have full voltage swing.
2. As shown in Fig. 8, the static CMOS full adder has 28 transistors. A disadvantage of the static CMOS full adder is that the input capacitance is higher.
3. Transmission function full adder: As shown in Fig. 9, the full adder base upon transmission functions is presented [1]. It improves the CMOS full adders from gate level to switching level. It reduces the redundant transistor counts.
4. DPL transmission gate full adder: As show in Fig. 10, the adder uses transmission gate logic to realize. All nodes have the double paths.
5. CPL transmission gate full adder: As shown in Fig. 11, the CPL-TG full adder [2] uses the CPL logic to generate the signal XOR and use transmission gate to pass the sum and carry. The use of CPL circuit at the front end reduces the input capacitance. But the complementary input signals are needed.

Ⅴ. The comparisons of simulation result

In this section, the simulation results of one-bit adders and the 16-bit carry ripple adders based on the three full adder architectures are shown. The HSPICE simulation results are based upon 0.5 μ m CMOS technology and supply voltages are change from 5V to 2.5V respectively. As shown in table 2, the proposed version 1 adder is only using 18 transistors. From the simulations of one-bit full adders as shown in Fig. 12 to Fig. 14, and the simulations of 16-bit adders are shown in Table 3 to Table 5, the proposed new adders version 1 and version 2 are have the better power consumption saved. Consequently, the proposed adder structures are suitable for low-power applications.

Ⅵ. Conclusions

In this work, the design of a new full adder using PTL with modified K-map was presented. The presented XOR and XNOR functions had full voltage swing output, so had better driving capacity to drive the transmission gates which was used to generate the output signals sum and carry. Beside, full voltage swing was suited to operate at low voltage. Because the constitutions of new adder were almost passive MOS transistors, the power consumption was reduced.

References

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A	B	Y=A⊕B	Pass function		
0	0	0	A	B	0
0	1	1	A'	B	1
1	0	1	A	B'	1
1	1	0	A'	B'	0

Table 1. The truth table of XOR function

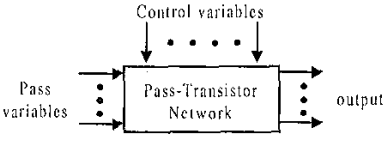

Fig. 1 Pass-transistor network

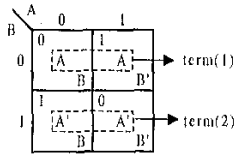

Fig. 2(a) The version 1 of XOR function

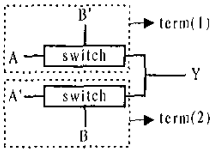

Fig. 2(b) The implementation of XOR function

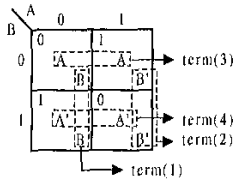

Fig. 3 The version 2 of XOR function

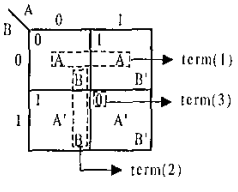

Fig. 4 The version 3 of XOR function

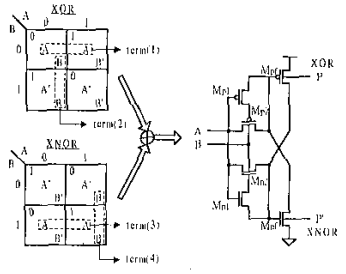

Fig. 5(a) The new structure of XOR/XNOR function with six MOS transistors

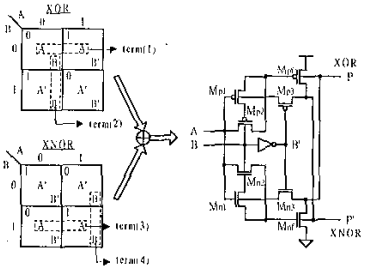

Fig. 5(b) The improvement of XOR/XNOR function for low voltage application

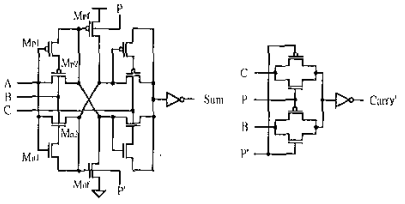

Fig. 6 The proposed new adder (version 1)

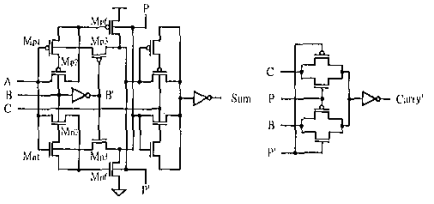

Fig. 7 The proposed new adder (version 2)

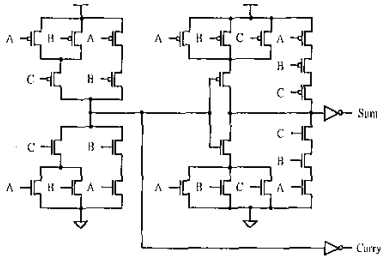

Fig. 8 The static CMOS adder (version 3)

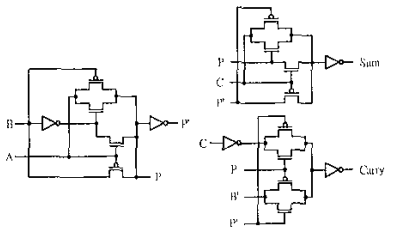

Fig. 9 The CPL transmission function adder proposed by [1] (version 4)

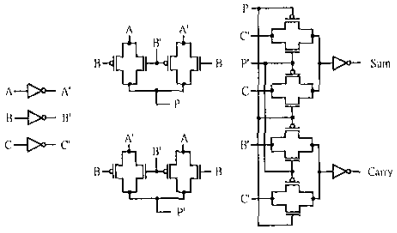

Fig. 10 The DPL transmission gate adder (version 5)

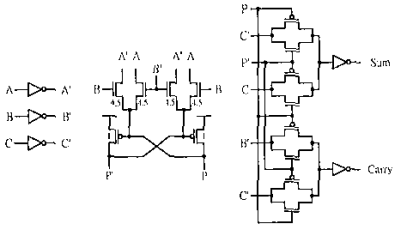

Fig. 11 The CPL transmission gate adder proposed by [2] (version 6)

	transistor counts
version 1	**18**
version 2	**22**
version 3	28
version 4	22
version 5	26
version 6	24

Table 2. The transistor counts comparison

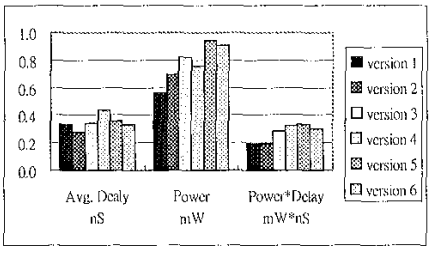

Fig. 12 The performance comparison of one-bit adders at voltage is equal to 5.0V

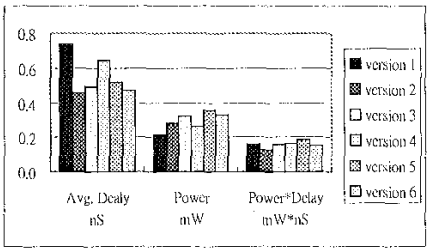

Fig. 13 The performance comparison of one-bit adders at voltage is equal to 3.3V

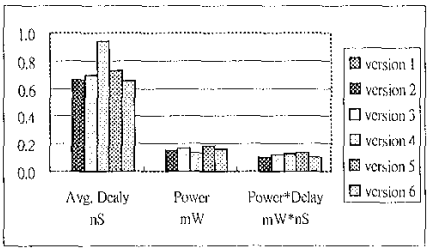

Fig. 14 The performance comparison of one-bit adders at voltage is equal to 2.5V

	Avg. Delay nS	Power mW	Power*Delay mW*nS
version 1	**6.3030**	**2.0180**	**12.7195**
version 2	**6.2560**	**2.0370**	**12.7435**
version 3	8.2050	2.7690	22.7196
version 4	8.2540	2.3110	19.0750
version 5	8.7100	2.3300	20.2943
version 6	8.6800	2.3500	20.3980

Table 3. The performance comparison of 16-bit adders at voltage is equal to 5.0V

	Avg. Delay nS	Power mW	Power*Delay mW*nS
version 1	**9.2300**	**0.6607**	**6.0983**
version 2	**9.1810**	**0.6714**	**6.1641**
version 3	11.1600	0.8651	9.6545
version 4	12.1600	0.7641	9.2915
version 5	12.5400	0.7762	9.7335
version 6	12.5200	0.7805	9.7719

Table 4. The performance comparison of 16-bit adders at voltage is equal to 3.3V

	Avg. Delay nS	Power mW	Power*Delay mW*nS
version 1	---	---	---
version 2	**13.3300**	**0.3077**	**4.1016**
version 3	15.2300	0.3846	5.8575
version 4	17.1600	0.3494	5.9957
version 5	17.8000	0.3555	6.3279
version 6	17.8700	0.3584	6.4046

Table 5. The performance comparison of 16-bit adders at voltage is equal to 2.5V