The Non-full Voltage Swing TSPC (NSTSPC) Logic Design.

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Abstract

In this paper, a new TSPC logic circuit is proposed for low-voltage high-speed applications. The proposed new circuit using non-full voltage swing scheme in internal node to reduce logic evaluation time and to save dynamic power. Thus the advantages of the new TSPC logic circuit over the conventional TSPC logic circuit are speed and power-delay product. Based upon the 0.35μm CMOS technology, the proposed new TSPC logic has 25% improvement then the conventional TSPC circuit in power-delay product. The new circuit can be operated at 250MHz with 1.2V supply voltage.

I. Introduction

Latches and flip-flops are basic building block of synchronous digital circuits. They determine circuit speed and power consumption. Their structures and performance are affected by clock strategies of the circuit [1]. The advantages of dynamic circuits are high operating speed and high packing density then static circuits. Recently, due to the fast development of low-voltage, low-power, and high-speed VLSI applications, low-voltage high-performance integrated circuit has become the main trade in modern VLSI design. In recent year, conventional True-single-phase-clock (TSPC) [2][3] flip-flops are used generally by many dynamic circuits.

The TSPC circuit contains two major stages, precharge stage and latch stage as shown in Fig. 1. If the supply voltage is low as 1.2V, the speed of the TSPC circuit will be slow down due to the slow evaluation (NMOS discharge) in the node A. When the clock signal CK is low, the node A will be pulled up to V_{DD}. When the clock signal CK is high, this circuit has two kinds of operating result: (1) If Q1 is turned-off by input signal IN, the node A is held at V_{DD}, and then output node B is discharged to V_{SS}. (2) If Q1 is turned-on, the node A will be discharged to V_{SS} and turns on the PMOS transistor Q3. During the first operating result (output evaluation low), the output node voltage V(B) is discharged quickly because the initial voltage of the node A is precharged to V_{DD} in the precharge phase. Thus the NMOS transistor Q2 is turned on quickly by the clock signal CK. During the second operating result (output evaluation high), we find the discharging time of the node A will slow down the operating speed of the PMOS transistor Q3 to charge the output node B. And it will increase the operating delay for low voltage applications. The delay time of the TSPC circuit is increased when the supply voltage is decreased as shown in Fig. 2. Therefor, if we can improve the discharging speed of the gate voltage of the PMOS transistor Q3, the circuit operating speed will be improved.

In this paper, a new TSPC logic circuit is proposed for low-voltage high-speed applications. The proposed new circuit using non-full voltage swing scheme in internal node to reduce logic evaluation time and to save dynamic power. In order to reduce the evaluation time (NMOS Q1 discharging time) of the internal node A, the non-full voltage swing scheme is used.

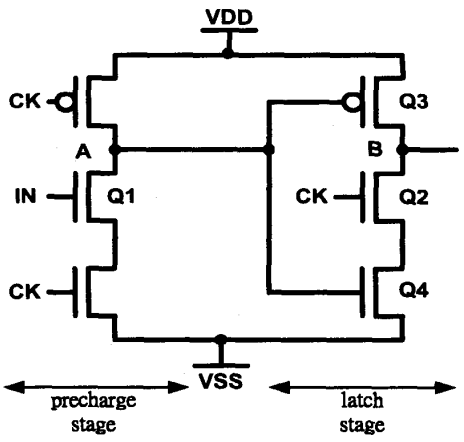


Fig. 1. The conventional TSPC circuit.

II. The Circuit Structure of the new Non-full Voltage Swing TSPC (NSTSPC) Logic

The schematic diagram of the non-full swing TSPC (NSTSPC) circuit is shown in Fig. 3. The proposed new logic circuit contains two parts: non-full voltage swing NMOS dynamic logic gate and N-type latch. The non-full voltage swing NMOS

0-7803-6470-8/00/ $10.00

dynamic logic gate performs the logic evaluation. The N-type latch senses the output signal of NMOS logic gate and holds output data at node D during the precharge phase. The detail operating principle of the new NSTSPC circuit is shown as follow:

A. The precharge/hold Phase (CK is low):

When the clock signal CK is low, the NSTSPC circuit is operated in the precharged/hold phase. The output nodes C and TC in the NMOS logic gate are precharged to high. The voltage of the node C is full voltage swing signal and the signal of node TC is non-full swing. The voltage of the internal node TC is

$$V(TC) = V_{DD} - V_{tn} \qquad (1)$$

Where V_{tn} is the threshold voltage of NMOS transistor QN. In this phase, node C is precharged to 1.2V and the node TC is precharged to 0.55V (The voltage V_{tn} is 0.65V). The PMOS transistor Q6 will be turned off by the voltage V(TC) of the node TC at

$$V(TC) > V_{DD} - V_{tp} \qquad (2)$$

The turned-on voltage of the PMOS transistor Q6 is under 0.45V. Therefore, the node D is hold the data of previous state.

B. The evaluation phase (CK is high):

When the clock signal CK is high, the NSTSPC circuit is operated in the evaluation phase. Based upon the input signals, the NSTSPC circuit has two different evaluation results, evaluation-low phase and evaluation-high phase. They are shown as follow:

B.1 Evaluation-low operation:

If NMOS transistor Q5 is turned off by the input signal IN during the evaluation phase, the node C is kept in high. It can turn on NMOS transistor Q8 to discharge the output node voltage. The node G is bootstrapped by the PMOS transistor QP and the voltage is

$$V(G) = V_{DD} + \Delta V \qquad (3)$$

Where ΔV is the bootstrapped voltage of the PMOS transistor QP. Thus the voltage of the node TC is also bootstrapped to

$$V(TC) = V_{DD} - V_{tn} + \Delta V \qquad (4)$$

This voltage is high enough to turn of the PMOS transistor Q6.

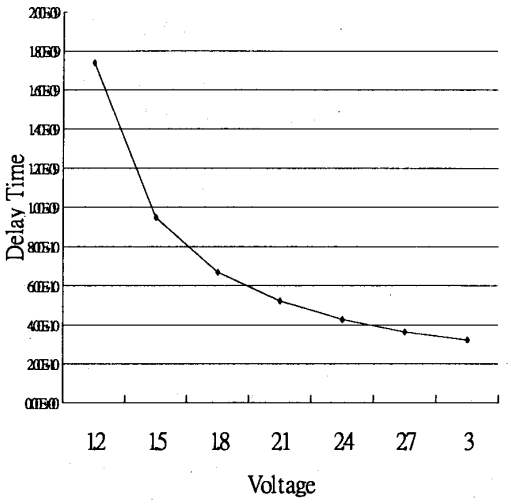


Fig. 2. Delays versus supply voltage for TSPC circuit.

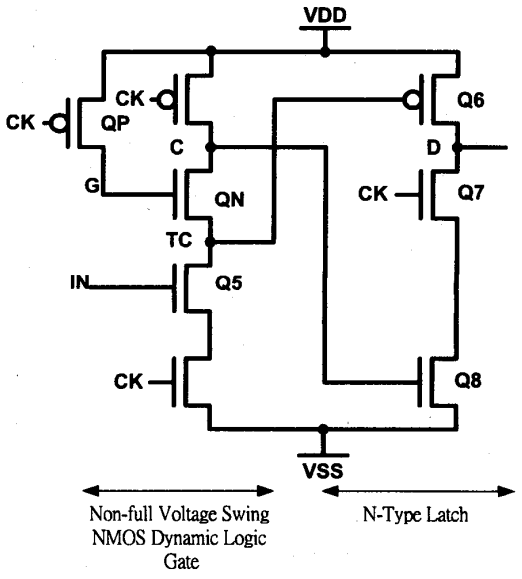


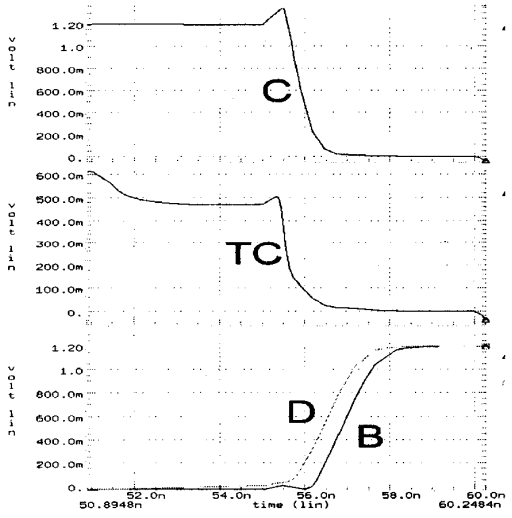
Fig. 3. The new NSTSPC TSPC circuit.

B.2 Evaluation-high operation:

If NMOS transistor Q5 is turned on by the input signal IN during the evaluation phase, the voltage V(TC) of the node TC and the voltage V(C) of the node C are discharged to V_{SS}. Because the highest voltage of node TC is $V_{DD} - V_{tn}$ during the

previous precharge phase, the discharging time of the node TC is fast than the time of the node C. The NMOS transistor Q8 is turned off until the V(C) is below 0.65V. Thus the PMOS transistor Q6 is turned on to charge the output node D to 1.2V very fast. Due to the non-full voltage swing in the node TC, the discharge voltage swing in the proposal new circuit is half as comparison to the conventional TSPC circuit for low voltage-applications. The discharging time of the node TC is faster then the time of the node A of conventional TSPC circuit as shown in Fig. 1. Therefor, the voltage of the output node D is pulled high very fast.

However, the discharged time of the node C may be longer then the time of the node A of the conventional TSPC circuit as shown in Fig. 1 because the discharging path of the conventional TSPC has less one NMOS then the new TSPC circuit. But the operating frequency does not influence.

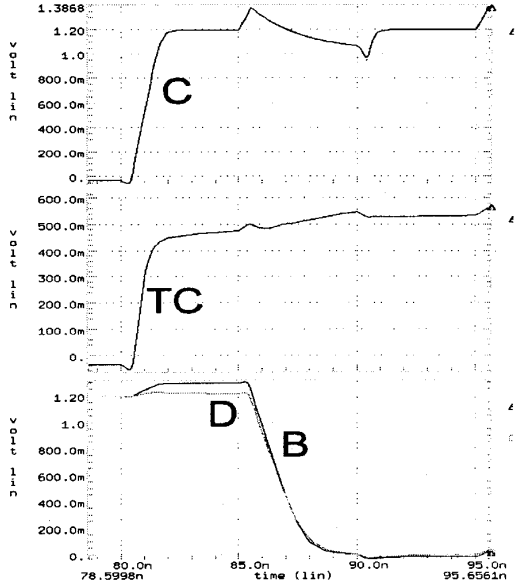


4(a)

Fig. 4(a). Simulated waveforms of the NSTSPC circuit at evaluation-high stage.

III. Simulation Result

Fig. 4 shows the output Evaluation-high and Evaluate-low waveforms of the proposed circuit. The waveforms C and TC are the internal node voltage of the new NSTSPC circuit, and the output voltage waveform is D. The output voltage of the conventional TSPC circuit is shown as the waveform B. The supply voltage is 1.2V. The highest voltage of node TC is 0.6V, and V_{tp} of 0.35um n-well CMOS process is -0.65V. The output PMOS transistor Q6 is turned off during the precharge/hold phase. Fig. 4(a) shows that the output voltage rises form V_{SS} to V_{DD}. The delay time of the new circuit (waveform D) is faster then the conventional TSPC circuit (waveform B). The pulled down delay time of the output is almost the same as the conventional TSPC circuit as shown in Fig. 4(b).



4(b)

Fig. 4(b). Simulated waveforms of the NSTSPC circuit at evaluation-low stage.

As shown in Fig. 5 and Fig.6, the D-type Flip-flop is implemented by the new NSTSPC circuit and the conventional TSPC circuit, respectively. The simulation result of power dissipation, delay time and power-delay product of the NSTSPC DFF and the TSPC DFF are shown in Table I. The operating frequency are changed from 10MHZ to 250MHZ. The power dissipation of the NSTPSC DFF is larger than the conventional TSPC DFF because the new circuit has two more transistors than the conventional TSPC circuit. And it has short circuit current by PMOS transistor Q6 during evaluation phase. But the new circuit has higher operation speed. The highest frequency of the new NSTSPC DFF can be operated at 250MHz, but the highest frequency of the conventional TSPC DFF is only 200MHz at 1.2V supply voltage. Therefor, the maximum operating frequency of the new NSTSPC circuit is improved 25%. The total power-delay product of new NSTSPC circuit is reduced over 25% then conventional TSPC

at 1.2V.

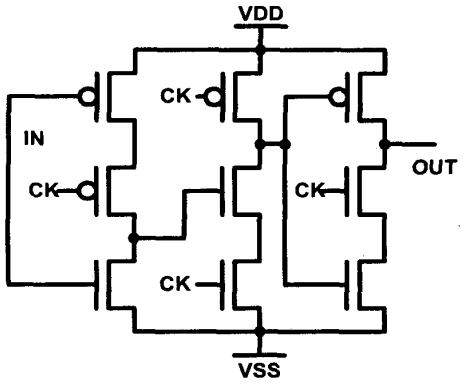


Fig. 5. The TSPC D-type Flip-Flop

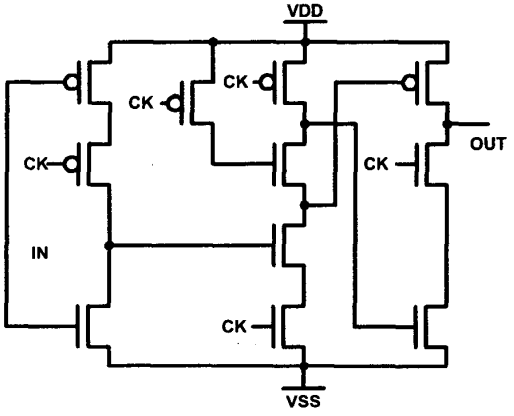


Fig. 6. The new NSTSPC D-type Flip-Flop

IV. Conclusion

In this paper, the low-voltage and high-speed NSTSPC DFF is designed and analysis. The internal delay will be reduced by non-full voltage swing scheme. Moreover, the bootstrapped technique is used to save the leakage current of the PMOS transistor.

Based upon the HSPICE simulation result, the power-delay product of the NSTSPC DFF can be reduced over 25%. And the clock frequency of the new circuit increases over 25%, respectively. The new NSTSPC DFF also can be applied to TSPC logic circuits or phase-frequency detector, or frequency divider for Phase-Lock Loop applications. Thus, the new NSTSPC DFF is suitable for low voltage high-speed applications.

Reference

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TABLE I.

The Power-delay products of the new NSTSPC DFF and the TSPC DFF

	POWER (uw)		Delay (ns)	
Frequency	NSTSPC	TSPC	NSTSPC	TSPC
10MHz	1.60	1.54	1.35	1.91
50MHz	4.60	4.43	1.36	1.89
100MHz	8.06	7.93	1.35	1.88
167MHz	12.5	12,4	1.36	1.87
200MHz	14.6	14.5	1.37	1.87
250MHz	17.1	----	1.36	----

(a) Power consumption and Delay time

	PD*		PD(normalize)	
Frequency	NSTSPC	TSPC	NSTSPC	TSPC
10MHz	2.17	2.95	1.00	1.36
50MHz	6.23	8.36	1.00	1.34
100MHz	10.9	14.9	1.00	1.37
167MHz	16.9	23.2	1.00	1.37
200MHz	19.9	27.1	1.00	1.36
250MHz	23.4	----	1.00	----

PD*: Power-delay product

(b) Power-delay product