Reducing Standby Power Applied to SR Forward Converters with Transient Load Response Considered

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***Abstract*-Up to the present, how to process standby power is getting more and more attractive. Therefore, in this paper, hybrid methods, including duty cycle detection and current detection, are applied to controlling operation states of the synchronous rectification (SR) forward converter, so as to reduce standby power as minimum as possible. At the same time, the performance of the transient load response due to a step load change from no/full to full/no load is also taken into consideration. The proposed approach is described in detail and verified by some simulation and experimental results.**

I. INTRODUCTION

Recently, DC/DC converters are getting more and more widely used in industrial applications, such as computers, communications systems, etc [1]. Among them, forward converters are getting more and more popular due to its inherent advantages, such as isolation, stability, etc. Up to now, some methods of reducing the standby power for the synchronous rectification (SR) forward converter are classified into two types. One is controlling the dead time between switches under different loads [2][3], and the other is exchanging operating states [4]. In practice, the latter has better effectiveness than the first. However, in [4], there is no consideration of the performance of transient load response. Consequently, in this paper, hybrid methods are presented to reduce standby power as well as to improve transient load response. Concerning the proposed topology, an field programmable gate arrays (FPGA) technique, together with an analogue to digital converter (ADC), is utilized not only to realize synchronous rectification (SR) control, but also to exchange operating states by using duty cycle detection for a step change from no to full load or by using both duty cycle detection and current detection for a step change from full to no load, in consideration of the performance of transient load response. Also, SR behavior and how to execute operating states exchange are described in detail. Eventually, some simulation and experimental results are provided to demonstrate the proposed technique.

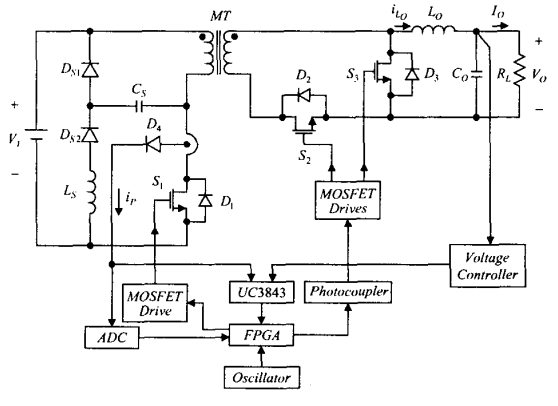

Fig. 1. System configuration of the experimental forward converter.

II. SYSTEM CONFIGURATION

In Fig. 1, the system configuration of the experimental forward converter with an FPGA-based SR control technique, together with one 12-bit ADC to get actual current information, is established according to the conventional PWM IC UC3843 control. In the beginning, the output voltage is tackled by the voltage controller whose resulting output signal, together with the sensed current flowing through the primary side of the main transformer MT after D_4, i_P, is sent to UC3843 to create a fixed-frequency PWM signal, PWM_I. This signal is fed into FPGA that is made by ALTERA with a production name of EPM7128SCL84, to generate desired switching signals to drive the main MOSFET switch S_1 after a MOSFET drive, and the high-side MOSFET switch S_2 and the low-side MOSFET switch S_3 after their corresponding photocouplers and MOSFET drives as well as to determine the operating state of this forward converter. Also, the diodes D_1, D_2 and D_3 are the body diodes for the MOSFET switches S_1, S_2 and S_3, respectively. As for the output filter, it consists of the output inductor L_O and the output capacitor C_O. As to the resonance snubber, it comprises the diodes D_{S1} and D_{S2}, the inductor L_S, the capacitor C_S and the magnetization inductance of MT. Most of all, by taking transient load response into account, operating states are exchanged by FPGA according to the duty cycle if in the case of a step change from no to full load, whereas operating states are exchanged by FPGA according to both the duty cycle and the sampled current if in the case of a step change from full to no load.

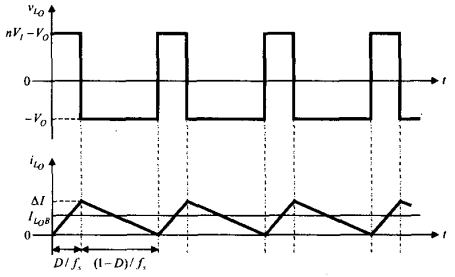

Fig. 2. Current flowing through L_O on the boundary between CCM and DCM under no SR, along with the voltage across L_O.

III. BOUNDARY EQUATION BETWEEN CCM AND DCM UNDER NO SR

In order to reduce the standby power at no load and to enhance the transient load response, this converter operates under hybrid conditions, SR and no SR. Therefore, under no SR, the boundary between the continuous current mode (CCM) and the discontinuous current mode (DCM) should be well defined herein. CCM is defined to be the condition that the current flowing through L_O is without zero current for some duration during the off time of the pulse modulation width (PWM) cycle at any time, whereas DCM is otherwise. Fig. 2 illustrates the voltage across Lo, v_{LO}, and the corresponding current flowing through L_O, i_{LO}. Thus, the boundary equation between CCM and DCM under no SR can be obtained according to Fig. 2 and hence the average current flowing through L_O on the boundary between CCM and DCM, I_{LOB}, can be obtained as follows.
From Fig. 2,

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$$I_{LOB} = \frac{\Delta I}{2} \quad (1)$$

Also,

$$\Delta I = \frac{(1-D)\cdot V_O}{L_O \cdot f_s} = \frac{(1-D)\cdot D \cdot n \cdot V_I}{L_O \cdot f_s} \quad (2)$$

Hence,

$$I_{LOB} = \frac{(1-D)\cdot D \cdot n \cdot V_I}{2 \cdot L_O \cdot f_s} \quad (3)$$

where

D: duty cycle

I_{LOB}: average current of i_{LO} on the boundary between CCM and DCM

n: turn ratio of the secondary to the primary sides of MT

f_s: switching frequency

V_O: DC output voltage

V_I: DC input voltage

ΔI: peak-to-peak current of i_{LO}

According to the statements above, for the fixed switching frequency and under no SR, the duty cycle in CCM is kept constant, whereas the duty cycle in DCM is varied according to the imposed load. Most of all, there is no current fed back to DC link in DCM, thus causing standby power to be reduced. However, under SR, the forward converter always operates in CCM, and there are two types of CCM, to be shown in Fig. 3. One is called CCM1 without negative current flowing through L_O, and the other is CCM2 with negative current flowing through L_O. Thus, in CCM2 there is current fed back to DC link, thereby causing standby power to be increased but transient load response to be improved [5]. So, in the following descriptions, CCM, DCM, CCM1 and CCM2 are abbreviations of CCM under no SR, DCM under no SR, CCM1 under SR and CCM2 under SR, respectively.

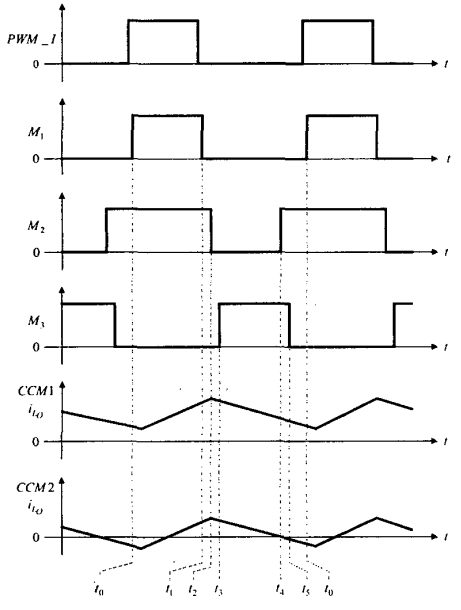

Fig.3. Timing sequences for CCM1 and CCM2 under SR.

IV. SR BEHAVIOR

The main power of the proposed FPGA-based SR forward converter is shown in Fig. 1 and described in Sec. II. For the convenience of describing this circuit behavior, the detailed operation of the resonance snubber that contains the diodes D_{S1} and D_{S2}, the inductor L_S, the capacitor C_S and the magnetization inductance of MT is neglected herein. The circuit operating modes in CCM1 and CCM2 are somewhat different even under the same FPGA-based SR control algorithm. Before going into depicting this SR behavior, as seen from Fig. 3, it is noted that PWM_I is indicative of the PWM cycle created from UC3843 shown in Fig. 1 and is the same as M_1 except for some delay due to logic operation, M_1, M_2 and M_3 denote the gate driving signals imposed on S_1, S_2 and S_3 respectively, and i_{LO} indicates the current flowing through L_O. It is noted that the detailed illustrations of SR behavior are omitted because of the limitations of space.

V. STATES EXCHANGE

Regarding transient load response, the method of exchanging states due to a step change from no to full load is different from that due to a step change from full to no load. Obviously, variations of duty cycle at the interval of a load change from no to full load is much larger than those at the interval of a load change from full to no load. This is because the first is varied from DCM in the beginning whereas the latter is from CCM2. Thus, for effectiveness in detection, duty cycle detection is used for a change from no to full load whereas both duty cycle detection and current detection are utilized for a change from full to no load. Besides, since the sensed current from the parasitic resistance of M_1 has much noise, one current transformer is used to sense current about in the middle of the duty cycle.

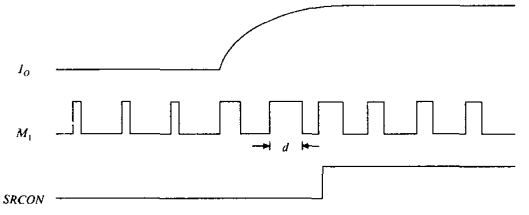

Fig. 4. How to determine states exchange from no to full load.

A. From No to Full Load

For the load to be changed from no to full load shown in Fig. 4, as a duty cycle of M_1 is over some value, say, d, the SR control signal, SRCON, is changed from the voltage reference low to the voltage reference high after the rising edge of the next duty cycle of M_1. So, DCM is moved to CCM1.

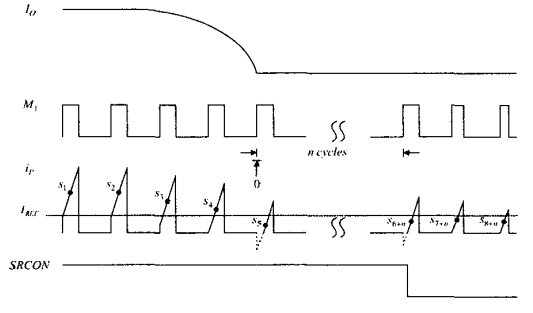

Fig. 5. How to determine states exchange from full to no load.

B. From Full to No Load

As shown in Fig. 5, information about the current on the primary side, sampled about in the middle of the duty cycle, is used to determined whether the state is changed or not for the load to be varied from full to no load. As the number, say, n of the events for the sampled current falling within the prescribed reference value, I_{REF}, defined by the output current I_O, happens, SRCON is altered from the voltage reference

high to the voltage reference low after the rising edge of the $(n+1)^{th}$ duty cycle of M_1. Thus, CCM1 is transferred to DCM via CCM2.

VI. SIMULATION AND EXPERIMENTAL RESULTS

Before discussing simulation and experimental results, the system specifications, how to create SRCON and hence to determine the operating state as well as to control the timing sequence of switches are described.

A. System Specifications

There are some key specifications required to be indicated: (i) system oscillation frequency for FPGA is set to 25MHz; (i) DC input voltage V_I is 12V; (ii) DC output voltage V_O is 5V; (iii) rated DC output current I_{O_rated} is 10A; (iv) switching frequency f_s is about 195kHz, which is obtained by dividing 25MHz by 128 which is created by a prescribed 8-bit counter set in FPGA; (v) output inductor L_O is 2.5uH; and (vi) turn ratio n is 5/6. Based on these statements, the average current flowing through L_O on the boundary between CCM and DCM, I_{LOB}, can be calculated to be about 2.56A by (3).

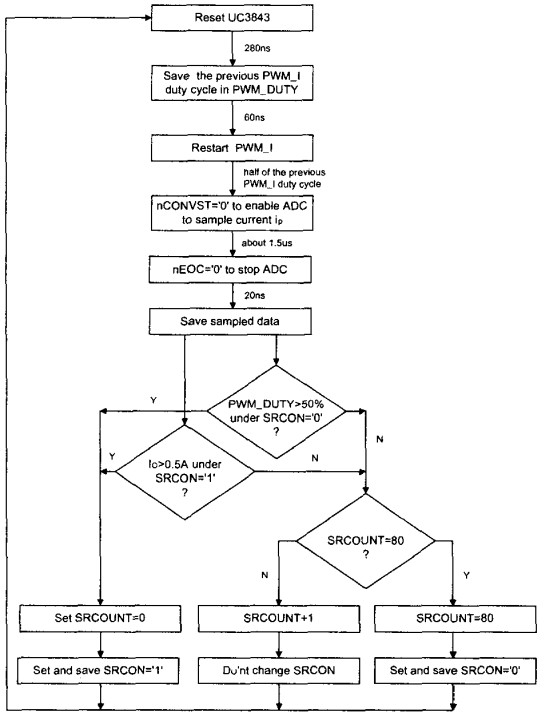

Fig. 6. How to generate SRCON.

B. SRCON Generation

As shown in Figs. 6, 8 and 9, where the last two figures are steady-state simulation results by FPGA in CCM1 at full load and DCM at no load respectively, for the sake of description, the process shown in Fig. 6 begins from resetting UC3843 by UC3843RST generated from FPGA. Based on this, after 280ns, the previous PWM_I duty cycle is saved and named as PWM_DUTY, where PWM_I is created from UC3843 mentioned in Sec. II. Then, after 60ns the present PWM_I gets restarted. Sequentially, after half of the previous PWM_I duty cycle, ADC is activated to sample i_P. From this time onwards, ADC is disabled after 1.5us and the sampled data is saved after 1.502us. Based on this sampled data, if I_O >0.5A or PWM_DUTY>50%, then reset the SR counter, SRCOUNT, and set SRCON to '1', whereas if I_O=<0.5A or PWM_DUTY=<50%, then if SRCOUNT reaches 80 then keep SRCOUNT constant at 80 and set SRCON to '0'; otherwise, increase SRCOUNT by one and do not change SRCON. It is noted that '1' indicates the voltage reference high, whereas '0' indicates the voltage reference low. By the way, i_P is sampled and used in exchanging states for a step load change from full to no load by comparing itself with I_{REF}, as mentioned in Sec. V.B. Since a 12-bit ADC is utilized herein with the voltage range from 0 to 5V, the ratio of the current transformer used to sense i_P is set to 25 with a resistance load of 3.5Ω. Thus, I_{REF} is obtained to be about 0.28A by setting the value of I_{REF} to 32 on condition I_O is set to 0.5A that is below I_{LOB} (=2.56A) and makes sure that such a forward converter operates in DCM if under no SR.

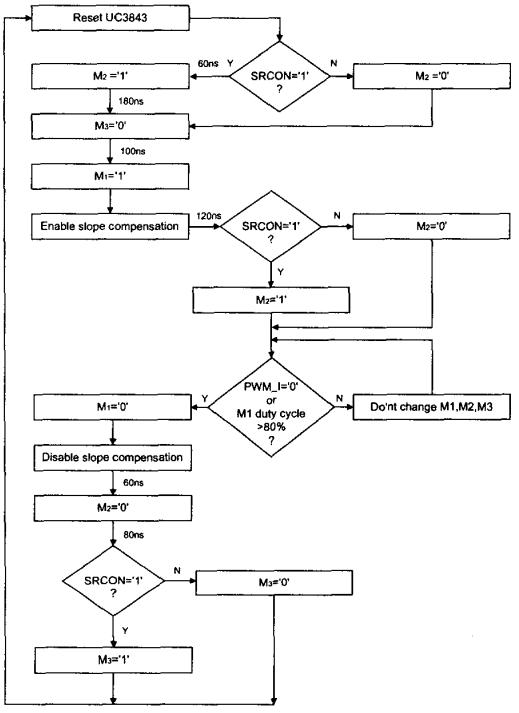

Fig. 7. How to generate the timing sequence for M_1, M_2 andM_3 based on SRCON.

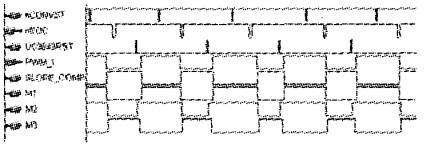

Fig. 8. Timing sequence of the associated events in CCM1 at full load, simulated by FPGA.

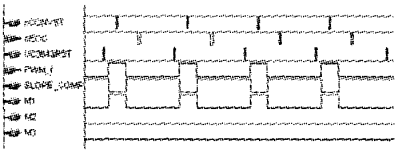

Fig. 9. Timing sequence of the associated events in DCM at no load, simulated by FPGA.

C. Operating States Exchange

As shown in Figs. 7, 8 and 9, the process also begins from resetting UC3843. For extending the duty cycle of PWM_I over 50%, the slope compensation signal SLOPE_COMP,

opposed to M_1, is needed and generated by FPGA. According to the information on SRCON mentioned above, SRCON is used to exchange operating states if the load is varied from no/full load to full/no load. To explain more briefly, if SRCON='1', the operating state is under SR; otherwise, under no SR. For M_1, M_2 and M_3 to be concerned, M_1 to drive S_1 is almost the same as PWM_I that is created from UC3843, except for some delay due to logic operation, and M_2 and M_3 to drive S_2 and S_3 respectively are ANDed with SRCON to determine the forward converter to operate under SR or no SR. And, the timing sequence between M_1, M_2 and M_3 can be described according to the flowchart in Fig. 7 along with SR behavior in Sec. IV. It is noted that there are three judgment events of SRCON and exchanging operating states occurs at the second judgment event. By the way, since a prescribed 8-bit counter in FPGA, reset by the rising edge of the duty cycle of M_1, is used to create switching frequency as well as to control the states exchange of SRCON after the counter number reaches a value of 3. Also, if the duty cycle of M_1 is over 80%, then M_1 is turned off in order to get enough resetting time for the main transformer MT.

D. Experimental Results

1) *Standby power comparison:* By comparing the standby power under SR with that under no SR, under the same condition that I_O = 0A and V_I=12V, the input currents under SR and no SR are measured to be 0.28A and 0.18A, respectively. That is to say, a difference in standby power between them is 1.2W. And this is why exchanging operating states is indispensable for reducing standby power. Thus based on this, the following are results taking into account minimization of standby power as well as improvement of transient load response.

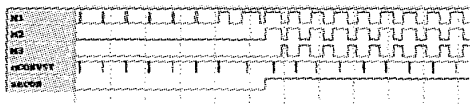

Fig. 10. Timing sequence from no to full load, obtained from a logic analyzer.

Fig. 11. Timing sequence from full to no load, obtained from a logic analyzer.

2) *Transient load response:* As shown in Figs. 10 and 11, a logic analyzer is mainly used to display the relationship between M_1, M_2, M_3 and SRCON due to a step load change. The result from no to full load shown in Fig. 10 demonstrates that as the duty of M_1 is larger than 50%, SRCON is forced to be '1' after the rising edging of the next duty cycle of M_1, and hence operating state is changed from DCM to CCM1. Also, the result from full to no load shown in Fig. 11 describes that as SRCOUNT reaches a prescribed value of 80, which is not shown clearly herein, the operating state is changed from CCM1 to DCM via CCM2 after the rising edge of the 81th duty cycle of M_1. It is noted that to avoid a large voltage spike occurring, M_2 is activated prior to turning on M_1 as soon as SRCON changes.

As demonstrated in [5], the recovery time of transient load response under SR is better than that under no SR, especially from full to no load. So, in Fig. 12, SRCON is changed from '0' to '1' almost at the instant of a step change in output current from no to full load, and hence the recovery time of the undershoot on V_O is almost controlled under SR. Regarding Fig. 13, as a step change in output current from full to no load occurs, there is elapsed time between output load variation and SRCON change, say, 470us in practice but 430us from calculation. This is because there is one spike noise or more over I_{REF}, thus making SRCOUNT to be reset and count from zero again. In this case, the recovery time of the overshoot on V_O is controlled also under SR, but it is to be explained clearly that the reason why the output voltage overshoot occurs once more as soon as SRCON exchanges states is that the time the duty cycle of M_1 is transferred to the desired value required in DCM needs several cycles, as referred to Fig. 11, thereby causing additional energy to be sent to the secondary side and hence the output capacitor C_O to be charged.

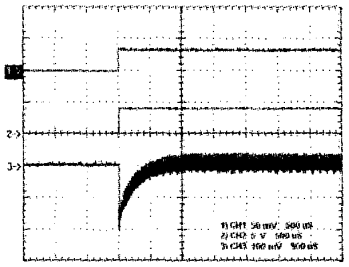

Fig. 12. Transient load response from no to full load with a time scale of 500us/div: (i) I_O with 15A/div for channel 1; (ii) SRCON with 5V/div for channel 2; (iii) output voltage variation with 100mV/div for channel 3.

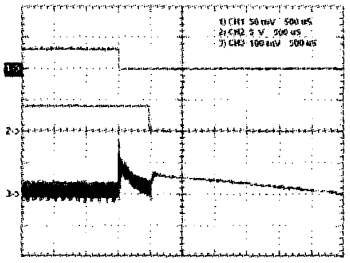

Fig. 13. Transient load response from full to no load with a time scale of 500us/div: (i) I_O with 15A/div for channel 1; (ii) SRCON with 5V/div for channel 2; (iii) output voltage variation with 100mV/div for channel 3.

VII. CONCLUSIONS

The motivation of this paper is to reduce standby power for the SR forward converter, along with taking transient load response into account. In order to realize this, duty cycle detection cooperates with current detection in controlling operation states. And the proposed approach is described in detail by some key flowcharts and then simulated and experimented with.

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