A Broadcast-Based Test Scheme for Reducing Test Size and Application Time

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Abstract- We present efficient method for reducing test application time by broadcasting test configuration. We compare our method based on single, multiple, 1-1 in-order mapping, even distribution, nearest signal probability matching, and in-order pseudo-exhaustive method. The results of our experiments indicate that our method reducing the test pattern number and the test application time by running the ATPG tool provided by SIS.

Key-Words: VLSI, Testing, BIST, Test Size, Test Application Time

1 INTRODUCTION

A structured test technique like the full scan is widely used in the industry to achieve high coverage and to reduce the complexity of test generation by making all memory elements in the circuit both controllable and observable through a scan chain. The full scan technique involves controlling (observing) the memory elements by serially shifting in (out) the values to (from) the flip-flops.

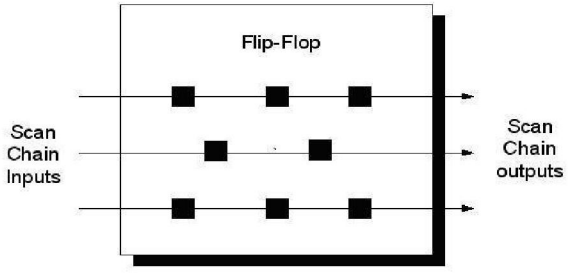

Figure 1:Traditional Multiple Scan Architecture

Single scan chains technique have the long test application time. In a traditional multiple scan architecture of Figure 1, it will require much higher number of extra I/O pins [1]. Many improvements to the test application time and test data volume for core-based designs have been suggested in the literature. An approach called the broadcast scan can share the test stimulus for a single input to support multiple scan chains [2]. A new architecture called the Illinois Scan Architecture (ILS) was recently proposed to accommodate the needs of embedded cores [3]. In [4] the efficient technique for test data volume reduction based on the shared scan-in (ILS) architecture and the scan chain reconfiguration architecture is proposed.

In the ILS architecture a single long scan chain is divided into many short segments, all of which are parallel loaded with the same vector. This method can effectively reduce both test data volume and test application time [5] and [6].

In this paper we shall describe a broadcast scan architecture that can reduce the test pattern and test application time. Based on the balance and longest common subsequence method. There, our method tries to balance assign pairwise similar flip-flops to the same position in each CUT scan chain.

To demonstrate the effectiveness of the proposed method, experiment results on both the ISCAS'85 combinational benchmark circuits [7] and the ISCAS'89 sequential benchmark circuits [8] will be given. The result shows that the proposed method can reduce the test patterns and the test application time. It is found that we only need 297 test patterns to detect all detectable faults in all five ISCAS'85 combinational circuits. For the sequential circuits, we show that with our method, 1322 test patterns are enough for the five ISCAS'89 scan-based sequential circuits.

The organization of this paper is as follows. Section 2 describes the basic concepts of broadcasting. We will illustrate our proposed method in Section 3 and show the experimental results by which we will compare our method with previous work on ISCAS'85 and ISCAS'89 benchmarks in Section 4. Finally, Section 5 presents the conclusions.

2 BASIC CONCEPTS

Test compaction can also be done after a set of test patterns has been generated. The basic idea here is to explore the compatibility among the generated test patterns and try to replace them with a new set of test patterns that has smaller size but still covers all faults that are detected by the original test set [9].

In the VLSI technology, the number of system primary inputs can be quite large. Hence how to select a virtual circuit such that the number of generated test patterns is minimum becomes the important problem. The "virtual

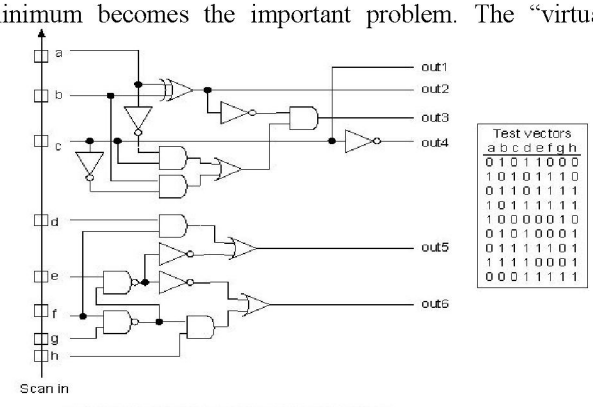

Figure 2: Traditional single scan test configuration

circuit" is just for ATPG process to generate common test vectors that are effective for all test circuits [10].

The "broadcasting test configuration" can reduce the test pattern and the test application time. As shown in Figure 2, we have the test width equal to 8, and a set of test vectors. We can find that the test pattern number is equal to 9. Using the proposed method -- the broadcasting test configuration, as shown in Figure 3, we bind together (a,d) ,

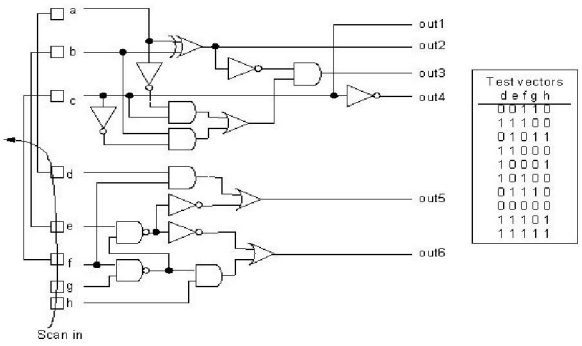

Figure 3: Broadcasting test configuration

(b,e) and (c,f) for 1-1 mapping method. The test width equal to 5, and the test pattern number is equal to 10. In this way, we can easily reduce the test application time from 8×9=72 to 5×10=50. In this paper, we present efficient method for reducing test application time by broadcasting test configuration. We used the balance and longest common subsequence method. Our method tries to balance assign pairwise similar flip-flops to the same position in each scan chain.

3 HEURISTIC METHOD

In this section, we show that our proposed method for broadcasting scan configuration. We call this method the balance and longest common subsequence (BL) algorithm. Next two subsections we will illustrate these two phases in detail.

3.1 Balance

In this phase, we try to evenly distribute the connection the CUT(1).The CUT(1) have the most of the input pins. Similar to the Even Distribution method in [10], we connect the CUT(2) to the first CUT(1), and the remaining circuits which can fit the last pins of CUT(1).This process continues until no circuits can fit the remaining pins of CUT(1).

3.2 Longest common subsequence (LCS)

3.2.1 Basic Concepts of an LCS

Here, we shall consider the longest common subsequence (LCS) problem. A subsequence of a given sequence is just the given sequence with some elements left out. Given a sequence $X = \langle x_1, x_2, \ldots, x_m \rangle$, we say that sequence $Z = \langle z_1, z_2, \ldots z_k \rangle$ is a subsequence of X if there exists a strictly increasing sequence $\langle i_1, i_2, \ldots, i_k \rangle$ of indices of X such that for all j = 1,2,…,k. For example, Z =<B, C, D, B> is a subsequence of X =<B, C, A, D, A, B> with corresponding index sequence <1,2,4,6>.

Given two sequence X and Y. A sequence Z is a common subsequence of X and Y if Z is a subsequence of both X and Y. For example, if X = <A, C, B, D, A, B, B> and Y = <B, A, C, A, B, A, B>, the sequence <A,C,B> is a common subsequence of both X and Y. The sequence <A, C, B> is not a longest common subsequence (LCS) of X and Y. However, since it has length 3 and the sequence <A, C, B, A>, which is also common to both X and Y, has length 4. The sequence <A, C, B, A> is an LCS of X and Y, as is the sequence <C, B, A, B>, since there is no common subsequence of length 5 or greater.

3.2.2 Computing the length of an LCS

The process of finding the optimum broadcast scan architecture will produce the minimum number of test pattern. We proposed a method to find the optimum broadcast scan architecture. Our method tries to assign pair similar flip-flops to the "same position" in each CUT scan chain.

The heuristic method first generates complete specified test sets for the each circuit under test. The test sets can represented two-dimensional matrix where each row is a test vector and each column is the values that will be assigned to a single flip-flop of the circuit. For any two columns, we can used the longest common subsequence method to compute these matrix are similar flip-flop value to the same position. An example test sets for circuit A and B in Figure 4 in which only X_1 and Y_3 have the most number of the LCS is 5. We can bind together X_1 and Y_3.

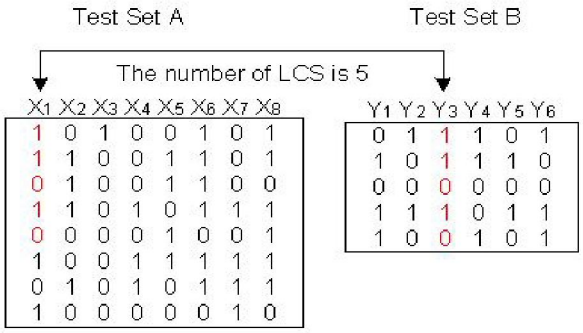

Figure 4. Test sets of circuits A and B

3.3 *Balance and Longest common subsequence (BL) method*

The BL algorithm for broadcast test configuration is show in Figure 5. First all of the CUTs are even distribution. This process continues until no circuits can fit the remaining pins of CUT(1). Then compute the number of the LCS for the all pins of CUT. Finally, if there have the most number of LCS for input pins, we can bind together.

1.All of the CUTs are even distribution.

2.Find the CUT(1),it must have the most input pins.

3.Choose the first pin of CUT(2)

4.Compute the most number of the LCS for the first pin of CUT(2) and the pins of CUT(1).

5.We bind together the most number of LCS for input pins.

6.Choose the next pin of CUT(2). And so on repeat Step4 and Step5 until all pins of CUT(2) binds finish.

7.Choose the next CUT. And so on repeat Step4, Step5 and Step6 until all pins of CUT binds finish.

Figure 5. BL algorithm for broadcast test configuration

4 EXPERIMENTAL RESULTS

We used the five ISCAS'85 combinational circuits and the five circuits of ISCAS'89 in our experiments. The longest common subsequence method is implemented on a

Intel pentium4-2.4G Windows XP machine in C language. A commercial ATPG tool is used to generate common test patterns for broadcast scan architecture. All experiments are performed on a SUN UltraSparc workstation.

Table 1 shows the ATPG results for each individual circuit in the ISCAS'85 benchmarks. We find that totally 397 test patterns are required to detect all 10157 detectable faults in the five ISCAS'85 benchmark circuits.

The experimental results for test application time for combinational circuits C432, C1355, C1908, C2670, and C6288 is shown in Table2. The columns in Table 2 present the single scan chains method, the multiple scan chains method, the 1-1 in-order mapping method, the even distribution method, the nearest signal probability matching method, the in-order pseudo-exhaustive method, balance and longest common subsequence methods.

The 8th of Table 2 show the results of our method

Table 1.Individual ATPG Results of ISCAS'85 Circuits

Circuits	# PI / PO	# Faults	#Gates	# RF	# TP
C432	36/7	498	160	1	50
C1355	41/32	1082	546	0	96
C1908	33/25	882	880	3	67
C2670	233/140	1900	1193	7	141
C6288	32/32	5840	2416	34	43
Total	375/160	10202	5195	45	397

PI/PO: Primary Input/Output,RF: Redundant Faults,TP: Test Patterns

Table 2.Experimental Results for ISCAS'85 Circuit

	Single	Multiple	# 1-1 map	# Balance	# Pro	# PE	# BL
Test Patterns	397	397	321	314	310	305	297
Scan Chain Length	375	233	233	233	233	233	233
TA Time	148875	92501	74793	73162	72230	71065	69201
Normalized TA Time	1	0.621	0.502	0.491	0.485	0.477	0.464

1-1 map:1-1 In-Order Mpping, Balance:Even Distribution, Pro:Nearest Signal Probability Matching

PE:In-Order Pseudoexhaustive, BL:Balance+Longest common subsequence ,TA:Test Application

(balance and longest common subsequence). Totally 297 test patterns are required to detect all faults in five ISCAS'85 circuits using our method. Clearly these numbers are significantly smaller than the total number of patterns required for five combinational circuits (397).The test application time is calculated by 297x233=69201 cycles for our method, which are about 46.4% of the single scan chain method, 74.8% of the multiple scan chain method, 92.5% of the 1-1 in-order mapping method, 94.5% of the even distribution method, 95.8% of the nearest signal probability matching method and 97.3% of the in-order pseudo-exhaustive method, respectively.

For the sequential benchmark circuits, we assume that only the flip-flops of the circuits are chain together. The results for individual circuits process is given in Table 3, where we find that totally 21341 faults can be detected by 2036 patterns. In Table 4, the results of our method are compared with the single scan chains method, the multiple scan chains method, the 1-1 in-order mapping method, the even distribution method, the nearest signal probability matching method, and the in-order pseudo-exhaustive method. The 1-1 in-order mapping method in which all the first pins of each circuit are connected together, all the second pins of each circuit are connected together, and so on. The even distribution method tries to "evenly distribute" the connection among the input of the first circuit under test. The nearest signal probability matching method is to connect the pins that have relatively closest probabilities of logic one or zero such that any two pins that will share the

same test data should have similar one or zero probability, but this method can't find the similar flip-flops to the same position. The pseudo-exhaustive method is to extend the possible construction of the 1-1 mapping method, but the ATPG process can be efficiently carried out. Our method tries to balance and assign pairwise similar flip-flops to the same position in each scan chain. The test application times is 789234 (1322x597) for our method. In Table 4, we can see that the test application time for our method is smaller than other methods.

Table 3.Individual ATPG Results of ISCAS'89 Circuits

Circuits	# PI / PO	# Faults	# FF	# Gates	# RF	# TP
S1238	14/14	1118	18	508	66	166
S1494	8/19	1218	6	647	12	145
S5378	35/49	3941	179	3400	50	360
S9234	19/22	6010	228	6326	446	623
S15850	14/87	10034	597	11739	406	742
Total	90/191	22321	1028	22620	980	2036

PI/PO: Primary Input/Output,FF: Flip-Flops,RF: Redundant Faults, TP: Test Patterns

Table 4.Experimental Results for ISCAS'89 Circuit

	Single	Multiple	# 1-1 map	# Balance	# Pro	# PE	# BL
Test Patterns	2036	2036	1518	1429	1437	1406	1322
Scan Chain Length	1028	597	597	597	597	597	597
TA Time	2093008	1215492	906246	853113	857889	839382	789234
Normalized TA Time	1	0.58	0.432	0.407	0.409	0.401	0.377

1-1 map:1-1 In-Order Mpping, Balance:Even Distribution, Pro:Nearest Signal Probability Matching

PE:In-Order Pseudoexhaustive, BL:Balance+Longest common subsequence ,TA:Test Application

5 Conclusions

In this paper, we presented a new method to reduce test pattern and test application time by balance and longest common subsequence method in broadcast test configuration. The balance and longest common subsequence are used to find the best broadcast scan architecture. The proposed technique utilizes a low test pattern. The experimental data for ISCAS'85 and ISCAS'89 circuits show that this method significantly reduces both the test pattern and test application time.

REFERENCES

[1] Zhang and R.D. Mcleod, "An Efficient Multiple Scan Chain Testing Scheme" in *6th Great Lakes Symp. VLSI*, March. 1996,pp.294-297.

[2] K-J. Lee, J-J. Chen and C-H. Huang, "Using A Single Input to Support Multiple Scan Chains," *Dig. Tech. Papers, IEEE/ACM Int. Conf. Computer-Aided Design*, 1998, pp.74-48.

[3] I. Hamzaoglu and J. H. Patel, "Reducing Test Application Time for Full Scan Embedded Cores," *Proc. IEEE Int. Symp. on Fault Tolerant Computing*, 1999, pp.260-267.

[4] S. Samaranayake, E. Gizdarski, N. Sitchinava, F. Neuveux, R. Kapur, T.W. Williams, "A Recofigurable Shared Scan-in Architecture," *Proc. VLSI Test Symp.*, 2003, pp.9-14.

[5] A.R. Pandey and J.H. Patel, "An incremental algorithm for test generation in illinois scan architecture based designs", in *Proceedings of the Design, Automation and Test in Europe Conference*, 2002, pp.369—375.

[6] A.R. Pandey and J.H. Patel, "Reconfiguration Technique for Reducing Test Time and Test Data Volume in Illinois Scan Architecture Based Design," *Proc. VLSI Test Symp.*, 2002,pp.9-15.

[7] F. Brglez and H. fujiwara, "A neutral netlist of 10 combinational benchmark designs and a special translator in Fortran," in *Proc. Int. Symp. Circuits and Systems,* June 1985, pp.663-6983

[8] F. Brglez, D.Bryan, and K. Kozminski, "Combinational profiles of sequential benchmark circuits, in *Proc. Int. Symp. Circuits and Systems,* May 1989, pp. 1929-1934.

[9] J. S. Chang and C. S. Lin, "Test set compaction for combinational circuits," *IEEE Trans. Computer-Aided Design*, vol. 14, pp. 1370–1378, Nov. 1995.

[10] K-J. Lee, J-J. Chen and C-H. Huang, "Broadcasting Test Pattern to Multiple Circuits, " in *IEEE Trans. on CAD,* December 1999, pp. 1793-1802.

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