The Design of A Delta-Sigma Modulator with Low Clock Feedthrough Noise, Op-Amp Gain Compensation, and More Correctly Transferring Charges between Capacitors

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Abstract — The performance of a delta-sigma modulator ($\Delta\Sigma$M) is degraded due to the low op-amp gain, the clock feedthrough noise, and the right or fault of charge transferring between capacitors. Hurst et al. in 1993 suggested an architecture which uses reduced sensitivity to the op-amp gain. Since the low op-amp gain is much easier to design and makes the design of a $\Delta\Sigma$M become very easy. However, they do not overcome the noise effect of the $\Delta\Sigma$M. Here, another design is proposed and the effect of noise is reduced.

1. INTRODUCTION

The performance of a $\Delta\Sigma$M is mostly affected by the following nonideal properties: (1) the low (finite) op-amp gain, (2) the clock feedthrough noise, and (3) the right or fault charge transferring between capacitors in the $\Delta\Sigma$M circuits [1-2]. Due to errors caused by the low op-amp gain, people try to design very high op-amp gain for $\Delta\Sigma$M. However, the op-amp with high gain is very difficult to design. On the other hand, some people try to find another approach that the $\Delta\Sigma$M can be designed by low op-amp gains but the performance is still good [1], [3-4]. Hurst et al. [1] gave a new architecture in 1993. They discuss how to reduce sensitivities to the op-amp gain in $\Delta\Sigma$M. However, their modulator is noise sensitive.

The clock feedthrough noise in $\Delta\Sigma$M is caused mainly from the clocks. The noise effects affect the performance of the modulator very significantly. By the way, the charge in the switched-capacitor may cause errors to the output of the modulator. How to transfer charge more correctly in $\Delta\Sigma$M becomes very important in the switched-capacitor $\Delta\Sigma$M.

In this paper, we employ the gain-compensated SC integrator that is proposed by Hurst et al. [1] to solve the problems of finite op-amp gain in $\Delta\Sigma$M. We improve the circuit given in Hurst et al. [1]. The op-amp is redesigned to be fully differential form. The fully differential op-amp can reduce the noise caused by the switching clocks significantly. The delay clock phase is used to control several switches to make charge transfer between capacitors to be more correct in the switched-capacitor $\Delta\Sigma$M circuits.

2. IMPERFECTION OF THE TRADITIONAL $\Delta\Sigma$M

Several imperfections of the traditional $\Delta\Sigma$M are discussed in this section and some solutions of the imperfections will be discussed in next section. Fig. 1 shows a conventional SC integrator. 'x' is a node, and C1 and C2 are capacitors. Vin and Vout are the input and output signals respectively. P1 is phase-1 clock and P2 is phase-2 clock. S11, S12, S21, and S22 are switches which are controlled by P1 and P2. During P1 is high then S11 and S12 are closed, and S21 and S22 are opened; during P1 is high then S11 and S12 are opened, and S21 and S22 are closed.

2.1 Imperfection of the Finite Op-Amp Gain

Suppose that the op-amp and switches are ideal, the conventional SC integrator, as shown in Fig. 1 can be analyzed as follows.

$$Vout(n)=Vout(n-1)+\frac{C1}{C2}Vin(n-1) \quad (1)$$

When the op-amp gain is finite, say A, the inverting inputs of the op-amp is not virtual ground but $\frac{-Vout}{A}$, where Vout is the output voltage of the op-amp, and Eq. (1) is changed to

$$Vout(n)=(1+A)Vout(n-1)\frac{C2}{[(1+A)C2+C1]}+ AVin(n-1)\frac{C1}{[(1+A)C2+C1]}. \quad (2)$$

The op-amp gain must be at least equal to the oversampling factor so as to introduce a negligible amount of excess quantization noise in the baseband [5,6]. If the op-amp gain is high enough, Eq. (2) approaches to Eq. (1). However the high gain op-amp is very difficult to design and therefore makes the $\Delta\Sigma$M very hard to design.

2.2 Imperfection of the Clock Feedthrough Noise

When a MOS switch turns on, it acquires and stores charge q in its channel; when it turns off, it releases the charge. When the clock feedthrough noise created and its weight is N, the charge of C1 changes from $C1\times Vin(n)$ to $Q_{C1}(n)$, which is equal to $C1\times[V1(n)+N(n)]$ in capacitor C1 during P1. During P2, the charge in $Q_{C1}(n)$ is injected to the capacitor C2 if the op-amp is ideal. The function of a conventional SC integrator with clock feedthrough noise is:

$$Vout(n)=Vout(n-1)+\frac{C1}{C2}Vin(n-1)+\frac{C1}{C2}N(n-1) \quad (3)$$

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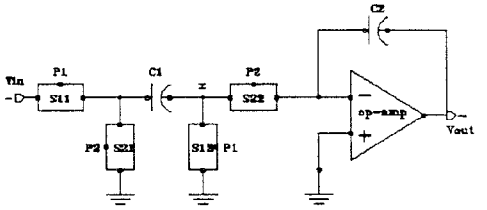

Fig. 1. The Conventional SC Integrator

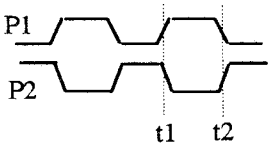

Fig. 2. The Phase of P1 and P2

Eq. (3) has one term, $-\frac{C1}{C2}N(n-1)$, more than Eq. (1). If the weight of N is large enough, the performance of the $\Delta\Sigma M$ is degraded.

2.3 Imperfection of Charge Transferring Between Capacitors

Fig. 2 shows the phases of P1 and P2, and t1 and t2 are points of time. At t1, P1 is pulling up and P2 is pushing down, and that causes switches S11 and S12 to be in between closing and opening, and S21 and S22 to be in between opening and closing. The charge of C1 is injected from Vin through S11 and charges from S21 to ground, and C2 losses charge from S22 to ground through S12. At t2, P1 is pushing down and P2 is pulling up, and that causes switches S11 and S12 in between closing and opening, and S21 and S22 to be in between opening and closing. C2 losses charge through S22 and S12 to ground and the charge is injected from Vin to C2 through S11, C1, and S22.

3. SOLUTIONS FOR THE THREE IMPERFECTIONS

Let us discuss the methods in this section to solve the three imperfections which are described in the previous section.

3.1 Gain-Compensated SC Integrators

we employ Larson's gain-compensated SC integrators GCI_1(as shown in Fig. 3), and Hurst's design GCI_2(as shown in Fig. 4) to solve finite op-amp gain of SC integrators.

3.2 Fully Differential SC Integrator

A fully differential SC integrator is shown in Fig. 5, and the capacitances of C11 and C12 are both equal to C1 (pf), and the capacitances of C21 and C22 are both equal to C2 (pf). Let us define Vij to be the input voltage; Voj(ta) be the output voltage, and N(ta) be the noise caused by clock at time ta and we find:

$$Vo1(tn-\tfrac{T}{2})=Vo1(tn-T)+\tfrac{1}{2}\tfrac{C1}{C2}[Vi1(tn-T)+Vi2(tn-T)]+N(tn-T) \quad (4)$$

$$Vo2(tn-\tfrac{T}{2})=Vo1(tn-T)-\tfrac{1}{2}\tfrac{C1}{C2}[Vi1(tn-T)+Vi2(tn-T)]+N(tn-T) \quad (5)$$

Let us set $Vo1(ta)-Vo2(ta)$ to equal $Vout(ta)$, and set $Vi1(ta)-Vi2(ta)$ to equal $Vin(ta)$ and the value of $\frac{C1}{C2}$ equal 1. We find the Vout becomes:

$$Vout(tn-\tfrac{T}{2})=Vout(tn-T)+Vin(tn-T) \quad (6)$$

Comparing Eq.(6) and Eq.(1), we find that these two equations are the same. Therefore, if we take fully differential SC integrators instead of the traditional integrators, the clock feedthrough noise can be reduced.

3.3 The Phase-Delay Design

The reason of the imperfection of charge transferring between capacitors, as discussed in Section 2.3 is that the switches are in between opening and closing. If the phase of S11 is slower than the phase of S12 for a little time, and the phase of S21 is slower than the phase of S22 for a while in the conventional SC integrator, as shown in Fig. 1. In this situation, the time when the charge of C1 in the S22 end is transferred to C2 through S22 is earlier than the time when the charge of C1 in the S21 end is flown to ground; the time when the charge is carried from Vin to C1 through S11. By this way the charge of C1 in the S22 end is fixed even the phase of S11 and the phase of S21 are overlapped. Fig. 6a shows the SC integrator with phase-delay design and Fig. 6b shows the form of the phases.

3.4 A Second Order $\Delta\Sigma M$ with Gain-Compensation, Fully Differential, and Phase Delay Design

A complete second-order $\Delta\Sigma M$ gain-compensation, fully differential, and phase-delay is shown in Fig. 7. The first stage of the $\Delta\Sigma M$ is a gain-compensated SC integrator GCI_1(as shown in Fig. 3) and the second stage is GCI_2(as shown in Fig. 4). All the circuits are designed symmetrically to fit the form of fully differential SC integrator. The eight clock signals by P1, P2, P1b, P2b, P1d, P2d, P1bd, and P2db using phase-delay approaches control the switches in the $\Delta\Sigma M$ and make the charge transferring between capacitors more exactly.

We have designed a second order $\Delta\Sigma M$ by the techniques of gain compensation, fully differential, and phase delay. The final layout is shown in Fig. 12. The process is UMC's 0.8 um DPDM. The result of the simulation described in next section is based on this layout.

4. THE RESULT OF SIMULATION

The clock feedthrough noise is added to the modified $\Delta\Sigma M$ and the results of the without-noise and with-noise are compared. The op-amp gain is 60dB, and the input signal is 2KHz with 0.2Vr amplitude and the sampling frequency is 2MHz. The

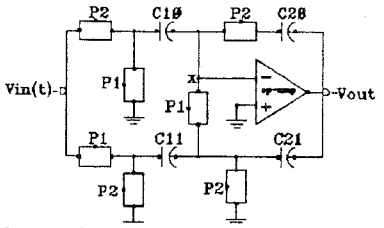

Fig. 3. A Gain-Compensated SC Integrator (GCI1) (C11=2C10 and C21=C20).

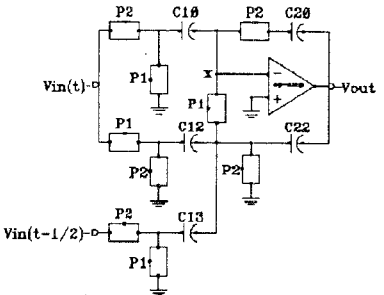

Fig. 4. A Gain-Compensated SC Integrator (GCI2) (C10=C10=C13 and C20=C22).

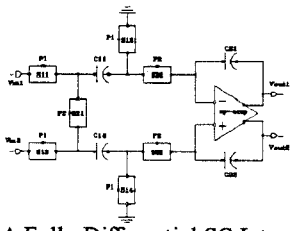

Fig. 5. A Fully Differential SC Integrator

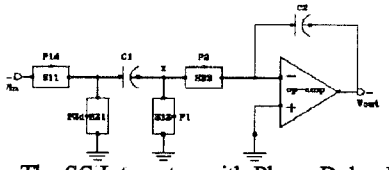

Fig. 6a. The SC Integrator with Phase-Delay Design

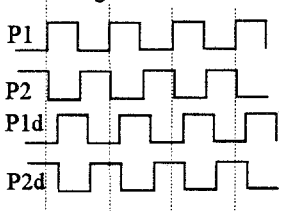

Fig. 6b. The Form of Phase-Delay

FFT result of the without-noise Δ ΣM is shown in Fig. 8, and the FFT result of the with-noise Δ ΣM is hown in Fig. 9. Comparing the two results, we find that both of them are the same, and the clock feedthrough noise is reduced by fully differential SC integrators.

The results of the FFT plot for a traditional Δ ΣM with fully differential SC integrator but without gain-compensation is shown in Fig. 10. Comparing Fig. 10 and Fig. 8, we find that the power of quantized noise in the voice band in Fig. 8 is lower than that of Fig. 10, therefore, the gain-compensation SC integrator can reduce the sensitivity to op-amp gain. Fig. 11 shows the FFT plot for the Δ ΣM as shown in Fig. 7 but without phase-delay design. Comparing Fig. 11 and Fig. 8, we find that the power of quantized noise in the voice band in Fig. 8 is lower than that of Fig. 11 , therefore, the phase-delay design can make the charge transfer to be more exact and the output performance be better. The baseband (about 0~40KHz) SNRs of Figs. 8, 9, 10 and 11 are shown in Table I. The SNR of Fig. 8 is greater than those of Figs. 9, 10 and 11 from Table I. The specification of this second-order Δ ΣM is as following:

(1) Power supply : ±2.5 V
(2) Power dissipation : 8.7 mW
(3) Sampling rate (Max.) : 20.48 MHz
(4) Input range : ±1 V
(5) SNR (baseband : 0~40KHz, sampling rate: 2.048 MHz) : 77.14 dB
(6) Active area : 2352 um × 1666 um
(7) Technology : UMC's 0.8 um DPDM CMOS

Table I: The Baseband (about 0~40KHz) SNR

	SNR (Baseband : 0Hz ~ 40KHz)
Fig. 8	77.14dB
Fig. 9	75.88dB
Fig. 10	45.20dB
Fig. 11	46.60dB

5. CONCLUSION

A Δ ΣM with gain-compensation, fully differential, and phase-delay SC integrator is presented. The Δ ΣMwith fully differential SC feature can reduce the clock feedthrough noise. The phase delay technique that makes charge transferring between capacitors more exactly can have the output of the Δ ΣM to be more accurate. Therefore, the efforts presented in this paper are not only easier to design a Δ ΣM but also have more correct results.

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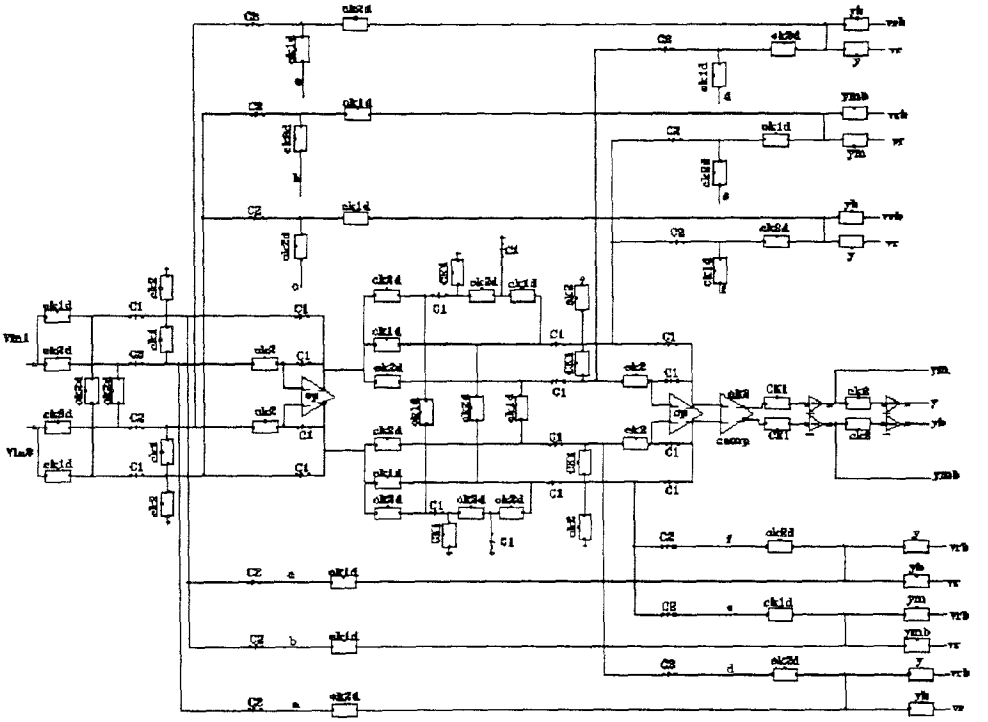

Fig. 7. A Second Order $\Delta\sum$M with Gain-Compensation, Fully Differential and Phase Delay Design

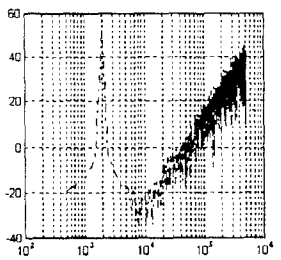

Fig 8. FFT Plot of the Output of the Without-Noise $\Delta\sum$M

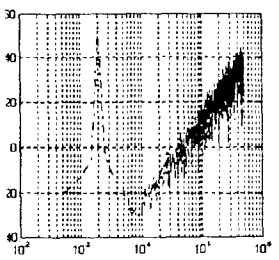

Fig 9. FFT Plot of the Output of the With-Noise $\Delta\sum$M in Fig. 8

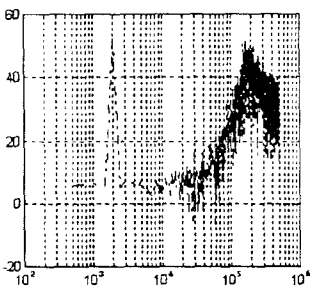

Fig 10. FFT Plot of the Output of the $\Delta\sum$M in Fig. 8 but without Gain-Compensation

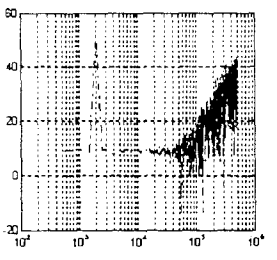

Fig 11. FFT Plot of the Output of the $\Delta\sum$M in Fig. 8 but without Phase-Delay Design

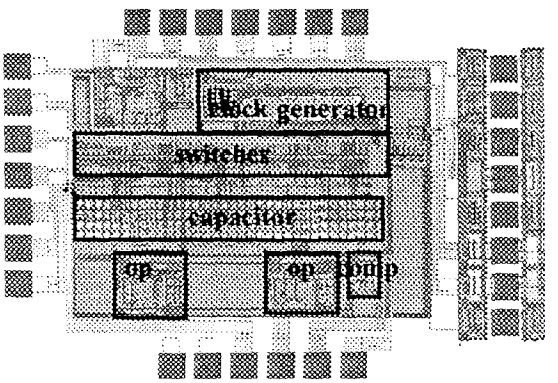

Fig. 12. The Final Layout of the circuit of Fig. 7

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