Design of Current Mode Operational Amplifier with Differential-Input and Differential-Output

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Abstract. In this paper, a CMOS implementation of a current operational amplifier (COA) with a differential input and a differential output is described. The amplifier is configured from a differential current mirror input transimpedance stage followed by a differential output transconductance gain stage. A differential mode design technique is proposed and used in the feedback circuit. This configuration is the current mode counterpart of the traditional voltage mode operational amplifier (VOA). In this design, the simulation results exhibit an open-loop differential gain of 51.71dB with the gain-bandwidth product 314MHz and a settling time of 14ns.

1. Introduction

The past few years have seen a great shift in analog circuit design towards representing signals with current instead of voltage. Current mode signal processing [1] is receiving considerable attention due to it's potential of two conceptual advantages over the classical voltage mode approach : higher frequency capabilities and higher dynamic range. Such current mode circuit is no longer directly restricted by the supply voltage but associated with the impedance level chosen by the designer. Various current mode building blocks have been proposed for active networks and analog computational applications [1].

The operation of the COA can be derived from that of the VOA by applying the theory of adjoint networks [2] to obtain the same transfer function. Following this approach, the interreciprocal network can then be used to transform almost all voltage mode continuous time active circuits to their current mode equivalent networks [3].

In this paper, a new differential-input, differential-output COA for equally useful general signal processing element is proposed and analyzed. It is configurated from an input transimpedance stage followed by a transconductance output stage. Section II shows the performances of the proposed COA. Section III presents some applications. Section IV shows the simulation results of the proposed COA. Finally the conclusion is given.

2. Current Operational Amplifier

In 1968, Sedra and Smith introduced a current conveyor [1] which they implemented using a VOA, complementary MOSFET's, and current mirrors. Applying the theory of adjoint networks, The COA replaces the VOA to a floating current controlled current source when converting from a voltage mode circuit configuration to a current mode configuration. By the theory, the COA use current conveyor as the basic active building block to form the COA had been described [4][5][6][7].

The equivalent circuit of a VOA is shown in Fig.1a. According to the adjoint network theory, the voltage controlled voltage source is replaced by a current controlled current source and the input/output terminals are interchanged. The resulting equivalent block is a COA and is shown in Fig.1b. A fully differential VOA shows in Fig.1c is transformed to the fully differential COA as shown in Fig.1d. Due to a differential-input current controlled floating current source (DCCCS). The COA exhibits ideally infinite differential current gain ,output impedance, zero common mode current gain and differential input impedance. Thus, the COA performs the current mode counterpart of the conventional voltage operational amplifier (VOA). The transconductance stage is realized in many different ways, i.e. a differential output current conveyor [5] using multiple-output current mirrors.

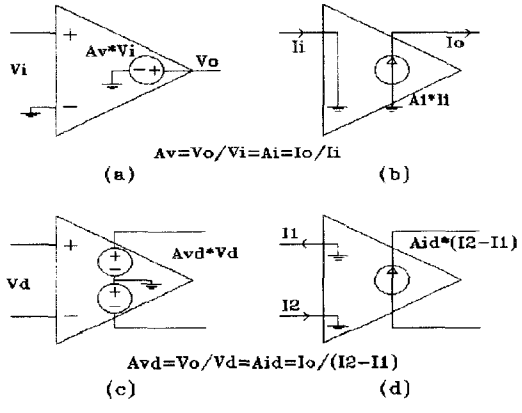

Fig.1 Interreciprocal network of VOA to COA.

In this paper, the COA is implemented using a transimpedance input stage followed by a transconductance output stage [8][9]. The new circuit schematic is shown in Fig.2. An output stage providing the complementary output is the differential floating current source (FCS) described in [10]. Essentially, this stage is just two matched CMOS inverters biased by a constant supply current and operated as an analogue transconductance stage.

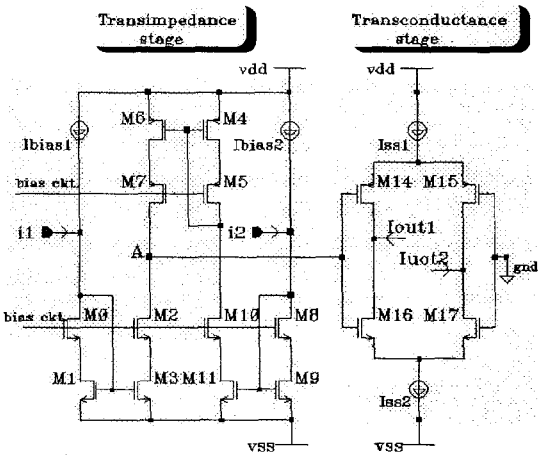

Fig.2 Transistor diagram of COA configuration.

2.1. Open-Loop Gain, Common Mode Rejection Ratio (CMRR), Input Offset Current

Extending the small signal analysis for the COA, we find:

$$i_{out1} = -i_{out2} = \left[(I_{bias1}+i_1)\lambda_1-(I_{bias2}+i_2)\lambda_2\lambda_3\right]R_A\left(\frac{g_{m14}+g_{m16}}{2}\right)$$

$$= \left[\left(\lambda_1 I_{bias1}-\lambda_2\lambda_3 I_{bias2}\right)-\left(\frac{\lambda_1+\lambda_2\lambda_3}{2}\right)(i_1-i_2)\right.$$

$$\left.+\left(\lambda_1-\lambda_2\lambda_3\right)\left(\frac{i_1+i_2}{2}\right)\right]R_A\left(\frac{g_{m14}+g_{m16}}{2}\right)$$

$$= \text{offset} + \text{differential gain} + \text{common gain} \quad \ldots\ldots (1)$$

Where I_{bias1}, I_{bias2} : bias current

λ_1 : current mirror ratio of $M_{0,1}$ to $M_{2,3}$

λ_2 : current mirror ratio of $M_{4,5}$ to $M_{6,7}$

λ_3 : current mirror ratio of $M_{8,9}$ to $M_{10,11}$

$$R_A = \left(\frac{1}{g_{ds3}}\frac{g_{m2}}{g_{ds2}}\right)//\left(\frac{1}{g_{ds6}}\frac{g_{m7}}{g_{ds7}}\right) \quad \ldots\ldots (2)$$

So I_{off} : equivalent input offset current

$$= \left(\lambda_1 I_{bias1}-\lambda_2\lambda_3 I_{bias2}\right) \quad \ldots\ldots (3)$$

assume Iss1 = Iss2

A_{dm} : differential mode current gain

$$= \left(\frac{i_{out1}}{i_d}\right)$$

$$= \left(\frac{\lambda_1+\lambda_2\lambda_3}{2}\right)R_A\left(\frac{g_{m14}+g_{m16}}{2}\right) \quad \ldots\ldots (4)$$

i_d : differential mode current input

$$= (i_1 - i_2) \quad \ldots\ldots (5)$$

i_c : common mode current input

$$= \left(\frac{i_1+i_2}{2}\right) \quad \ldots\ldots (6)$$

A_{cm1} : common mode current gain of stage 1

$$= \left(\frac{V_A}{\frac{i_1+i_2}{2}}\right) = (\lambda_1-\lambda_2\lambda_3)R_A \quad \ldots\ldots (7)$$

A_{cm2} : common mode current gain of stage 2

$$= \left(\frac{\frac{|i_{out1}|+|i_{out2}|}{2}}{V_A}\right) = \left(\frac{1}{4}\frac{1}{R_{SS1}//R_{SS2}}\right) \quad \ldots (8)$$

R_{SS1}, R_{SS2} : output resistance of the current source I_{SS1} and I_{SS2}, respectively.

A_{cm} : total common mode current gain [11]

$$= A_{cm1}\times A_{cm2} = \left(\frac{|i_{out1}|+|i_{out2}|}{i_1+i_2}\right)$$

$$= \frac{1}{4}(\lambda_1-\lambda_2\lambda_3)\left(\frac{R_A}{R_{SS1}//R_{SS2}}\right) \quad \ldots\ldots (9)$$

We also find the static common mode rejection ratio (defined as differential gain divided by common mode gain) is

$$CMRR = \frac{(\lambda_1+\lambda_2\lambda_3)}{(\lambda_1-\lambda_2\lambda_3)}(g_{m14}+g_{m16})(R_{SS1}//R_{SS2}) \quad \ldots (10)$$

It is seen that an arbitrarily high CMRR can be achieved through the use of current source. The impedance R_A is increased by employing high swing cascade current mirror[12]. So, the current gain is therefore increased by trading off power dissipation and die area.

2.2. Frequency Response, Gain-Bandwidth and Stability

The resulting configuration shown in Fig.2 has one high impedance node A in the signal path, creating a dominant pole at the frequency

$$f_{pd} = \frac{1}{2\pi}\frac{1}{R_A C_A} \quad \ldots\ldots (11)$$

$$C_A = C_{gd2}+C_{gd7}+C_{gd14}+C_{gd16}+\frac{C_{gs14}}{2}+\frac{C_{gs16}}{2} \quad \ldots (12)$$

C_A is the total capacitances of node A, it dominated by the gate-source capacitances of the transconductance stage. The first non-dominant pole is typically caused by the current mirror stage which contributes at angular frequencies on the order of gm/2Cgs. And, the parasitic capacitances (Cbd) influence the dominant and the non-dominant poles can be reduced by using an optimized transistor layout style, e.g. a finger

structure for the gate [7]. The gain -bandwidth product is

$$GBW = \frac{1}{2\pi C_A}\left(\frac{\lambda_1+\lambda_2\lambda_3}{2}\right)(g_{m14}+g_{m16}) \quad \ldots\ldots (13)$$

In VOA, the compensation capacitance separates the dominant and non-dominant poles to provide the desired unity gain phase margin, while in the COA, addition capacitance could be added at node A.

2.3. Input and Output Impedance

The input impedance is

$$R_{in} = \frac{1}{g_{m1}+g_{m3}} \quad \ldots\ldots (14)$$

The output impedance of the COA is the transconductance stage[5] can be increased using regulated cascades.

2.4. Input Common Mode Range (CMR)

For bias current Ibias1=Ibias2=I, the positive and negative common mode ranges are equal to bias current as shown in equation (15).

$$I = \frac{1}{16}\left\{V_{DD}\times\left[k_N\left(\frac{W}{L}\right)_N + k_P\left(\frac{W}{L}\right)_P\right]\right\}^2 \quad \ldots\ldots (15)$$

2.5. Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio [13] is

$$PSRR_{,vdd} \cong \left[-\left(g_{nodei1}+sC_{nodei1}\right)+\left(g_{nodei2}+sC_{nodei2}\right)+\left(\frac{g_{ds7}}{g_{m7}}g_{ds6}+sC_{gd7}\right)-\left(\frac{g_{ds10}}{g_{m10}}g_{ds11}+sC_{gd10}\right)\right]^{-1} \quad \ldots (16)$$

The PSRR,vss is also could be derived, we note that the power supply rejection ratio for the COA has the dimension of a resistor.

2.6. Noise Performance

The rms value of the equivalent input noise current [14] of the COA is

$$I_{ni}^2 = g_{mn}^2\left(\sum_{x=0,1,2,3,8,9,10,11} V_{nx}^2\right) + g_{mp}^2\left(\sum_{y=4,5,6,7} V_{ny}^2\right) + \left[\frac{2g_{m14}}{R_A\left(g_{m14}+g_{m16}\right)}\right]^2\left(V_{n14}^2+V_{n15}^2\right) \quad \ldots (17)$$

3. Current-OpAmp Application

Invoking duality, Fig.3 shows the examples to investigate the close-loop operation of the COA. As Fig.3 show that the close-loop gain depends on the resister ratio and not the open-loop gain characteristics. And negative feedback around the COA produces an accurate close-loop current gain insensitive to process, supply and temperature variations. It is found to have a constant gain-bandwidth independent of the open-loop current gain in a close-loop configuration [4][6]. So it is suitable for high frequency application. And an open-loop COA can be used as a current comparator in which the resolution is determined by the bias current and the open-loop current gain.

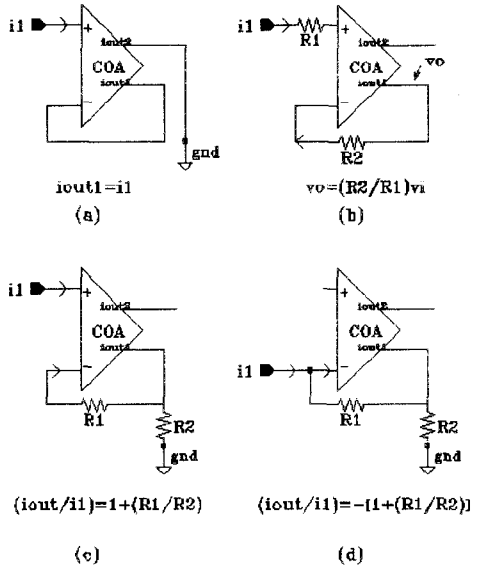

Fig. 3. Basic feedback controlled current amplifying (a) unity current gain, (b) voltage gain, (c) non-inverting, (d) inverting configurations.

4. Simulation Results

The proposed circuit of Fig.2 was simulated using HSPICE. The transistors were modeled using level 47 (BSIM3) parameters of 0.5um DPDM N-Well CMOS process. The simulation results are summarized in Table I. The simulation of the magnitude and phase response are shown in Fig. 4(a)(b). Fig. 4(c) shows the response of the buffer to a step input signal.

Table I. Summary of COA simulation results.

Power supply	±1.5volt.
DC gain	51.71dB
-3dB frequency	478.38KHz
Unity-gain frequency	314MHz
Compensation capacitance	5pF
Phase margin	50deg.
CMRR(0)	41.25dB
PSRR,*vdd* (0) / PSRR,*vss* (0)	287.3Ω /258.6Ω
1% settling time	14ns
Slew rate	160uA/6.4ns
Bias current Ibias1=Ibias2	291.43uA
Bias current Iss1=Iss2	1mA
Transimpedance stage $(W/L)_N$	60um/0.5um
Transimpedance stage $(W/L)_P$	40um/0.5um
Transconductance stage $(W/L)_N$	30um/0.5um
Transconductance stage $(W/L)_P$	200um/0.5um

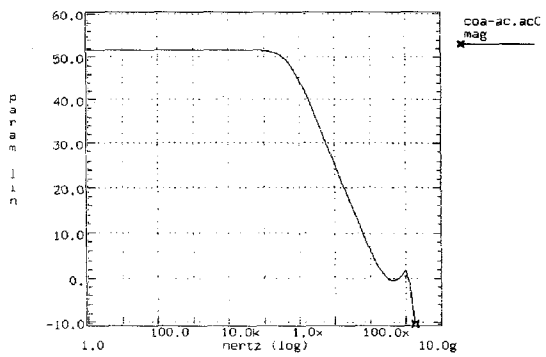

Fig. 4(a) Magnitude frequency response.

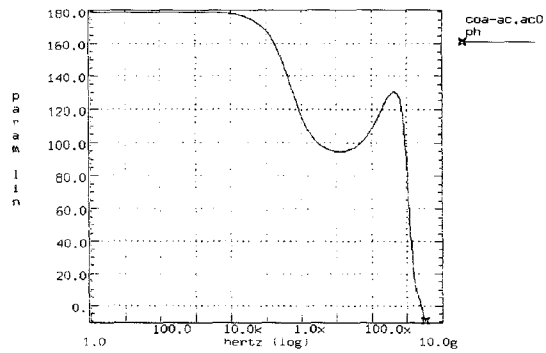

Fig. 4(b) Phase frequency response.

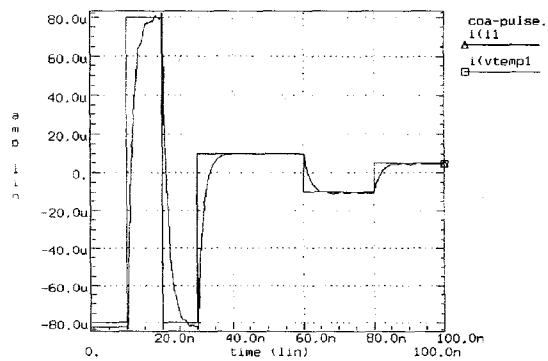

Fig. 4(c) Transient signal response.

5. Conclusion

A new circuit topology of a current mode amplifier with differential input and differential output is proposed and investigated. It is evident that significantly higher open-loop current gain can be obtained with much higher values of the current mirror output impedance and it uses in close-loop operation could obtain accurated gain.

The input offset, bias current errors and the common mode rejection (equation 3) are shown to be strongly dependent on the matching accuracy of the current mirrors. To minimize random offsets, all current mirrors must be matched by using common centroid geometry and unit-transistor layout techniques which balanced the oxide gradient contribution and reduced the current gain error due to process variation.

In frequency compensation optimization, the current mirror ratio function can be scaled to separate the dominant pole and the first non-dominant pole (reduced Cgs, Cgd), we note it should fit equation (10) to obtain high CMRR.

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