A 3.3V Two-Stage Fourth-Order Sigma-Delta Modulator with Gain Compensation Technique

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Abstract:

We propose a multistage fourth order sigma-delta (ΣΔ) modulator with reduced sensitivity to the gain of operating amplifier. In the low voltage high order ΣΔ modulator, the gain of the operating amplifier is usually the most critical problem of the design. In order to overcome the difficulties of the high gain low voltage operating amplifier, we try to use medium gain operating amplifiers to design a fourth order multistage ΣΔ modulator, and find that it functions very well. The modulator is realized in a 0.5 μm DPDM process with an active area of 1.8mm^2. The HSPICE simulation shows this ΣΔ modulator with a maximum signal-to-noise-ratio (SNR) of 91dB.

1. Introduction

Although real world signals are analog, it is often desirable to convert them into digital domain using an analog to digital converter (ADC). However, the architecture of the conventional ADC is very complicated and the resolution is very limited. On the other hand there is another approach by using sigma-delta (ΣΔ) modulator to implement the ADC [1-2]. The ΣΔ modulator has the characteristics of simple architecture and high resolution, and is very suitable to be applied in the high-end voice and audio systems [3]. The resolution of the modulators can be increased in various ways. Higher order ΣΔ modulator is one of the approaches. Nowadays people concern the power consumption of the system, especially the hand held systems, such as pagers, cellular phones, note book PC's, PDA's, ... etc., and lower power supply is one of the solution. The resolution of the ΣΔ modulator can be considerably affected by the oversampling ratio (OSR), the higher OSR the better resolution. However, high OSR may consume more power. The high order approach in the ΣΔ modulator can compensate the effect of the high OSR approach, and thus the high order design becomes important. Basically there are two categories, interpolative and multistage approaches, in the high order design of ΣΔ converter. Here we will concentrate in the multistage design.

In the multistage ΣΔ converter, the architecture is composed of several first- and second-order ΣΔ modulators that give the possibility of realizing almost ideal higher order noise shaping [4-5]. However, the multistage architecture is very sensitive to components used in the modulator. The non-ideal characteristics, such as finite op-amp gain, input offset voltage, charge transferring error, and capacitance mismatches, can cause noise leakage from first stage of modulator and hance reduce the dynamic range performance. The SC integrator is a very important component in the ΣΔ modulator design. In the SC integrator, we usually need a very high gain op-amp. However, the high gain op-amp is very hard to design and have to take special care, or the system may be unstable. In this paper we will propose reduced op amp gain architecture to implement the SC integrator. We also try to overcome the non-ideal characteristics of MOS mentioned above to design a fourth order ΣΔ modulator. By these efforts we have designed a 3.3V multistage fourth order ΣΔ modulator with 91dB signal-to-noise ratio (SNR).

In Section II the higher order multistage ΣΔ modulator will be described. In Section III we would like to discuss the fully differential gain-compensated SC integrator. In Section IV the fourth-order MASH ΣΔ modulator implementation is discussed. The result of simulation is shown in Section V, and finally we conclude this paper in Section VI.

2. Higher-Order Maltistage ΣΔ Modulator

In the high order multistage ΣΔ modulator, the overall architecture is cascaded by several first-order and second-order ΣΔ modulators. The schematic diagram of a L-order multistage ΣΔ modulator is shown in Fig. 1. The stability of first-order and second-order ΣΔ modulators is usually good. Therefore, the multistage ΣΔ modulator should remain stable, and makes the multistage design to be more stable than the interpolative one. Such multistage arrangement has been called "multistage noise shaping" or "MASH" [6].

In the multistage design as shown in Fig. 1, the quantization error, e(n), in each lower order ΣΔ modulator is fed to the succeeding modulator and finally the accumulated quantization error can be completely

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removed by the noise cancellation block. Assuming linear models for the quantizer, the straightforward linear analysis gives

$$Y(Z)=Z^{-L}U(Z)-(1-Z^{-1})^{L}E_{L}(Z) \quad (1)$$

Eventhough the stability of the MASH architecture is good, it has some drawbacks. Since it is cascaded by several first-order and second-order stages, and these low order stages are senstive to finite op-amp gain and mismatch between the analog and digital circuitry. Such nonideal behavior causes the low order noises to leak through from the first modulator and hance reduces the dynamic range performance.Let us discuss the non-ideal behaviors in next subsections.

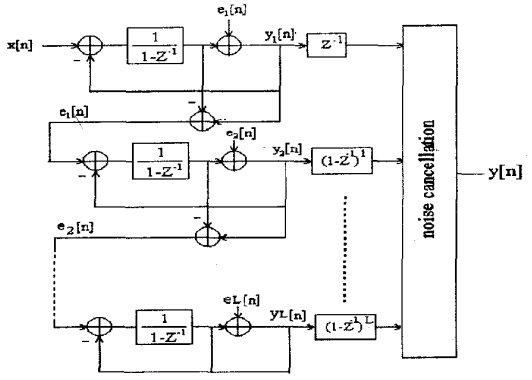


Fig.1:L-order MASH ΣΔ modulator

2.1 Finite Op-Amp Gain

Suppose that the op-amp and switch are ideal, the conventional transfer function of SC integrator can be shown as

$$Vo(n)=Vo(n-1)+\frac{C_1}{C_2}Vi(n-1) \quad (2)$$

Assuming that a SC integrator with a finite op-amp gain, A, result in the pole of integrator moving to the left of Z=1 by an amount of 1/A. We can determine the zero of the new noise transfer function (NTF) due to finite op-amp gain by substituting Z-1 with Z-(1-1/A) [7]. In other words, we substitute all ideal intgrators with damped intergrators and recaculate the transfer function. Such an approach results in the zero of the NTF, which is located at Z=1 for a low-pass design, to be moved to Z=(1-1/A). Therefore, the shaped quantization noise does not drop to zero, and the new tansfer function of the switch-capacitor integrator becomes

$$\begin{aligned} Vo(n) &= \frac{(1+A)C_2}{[(1+A)C_2+C_1]}Vo(n-1) \\ &+ \frac{AC_1}{[(1+A)C_2+C_1]}Vi(n-1) \end{aligned} \quad (3)$$

The op-amp gain must be least equal to the oversampling factor so as to introduce a negligible amount of excess quantization noise in the baseband.

2.2 Clock Feedthrough Noise

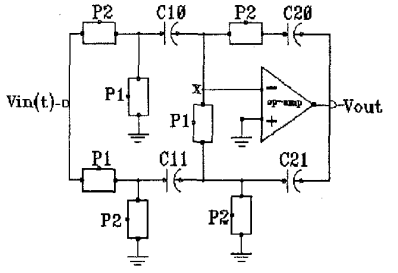
The clock feedthrough noise is injected into switches in the higher frequency of clock [8]. When the clock feedthrough noise is created and let us suppose its weight to be N, we can determine the charge of input capacitance by subtituting C×Vin(n-1) with C×[Vin(n-1)+N(n-1)]. Therefor, the new transfer function of SC integrator becomes

$$Vo(n)=Vo(n-1)+\frac{C_1}{C_2}Vi(n-1)+\frac{C_1}{C_2}N(n-1) \quad (4)$$

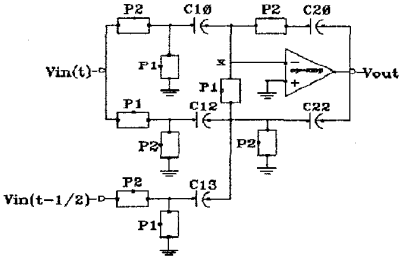
Equation (4) has one term, $(C_1/C_2)\times N(n-1)$, more than the ideal transfer function of the SC integrator. If the weight of N is large enough, the performance of the ΣΔ modulator is degraded.

3. Fully Differential Gain-Compensated SC Integrator

In order to reduce the interference of the non-ideal properties of MOS mentioned in the previous section, we would like to propose fully differential gain-compensation SC integrators to design the modulator. Here we employ a modified version of gain-compensated integrators that were proposed by Larson [9] and Hurst [10], and use fully differential technique to implement a new SC integrator. The gain-compensation approach can reduce the sensitivity of the modulator caused by the finite op-amp gain effect. The fully differential technique can reduce the feed-through noise in the SC integrator. Besides the architecture mentioned above, we use phase delay approach to prevent the faulty charge transferring between capacitors in the SC integrator.



(a)



(b)

Fig. 2: Gain compensated integrator(a) GCI_1 (b)GCI_2

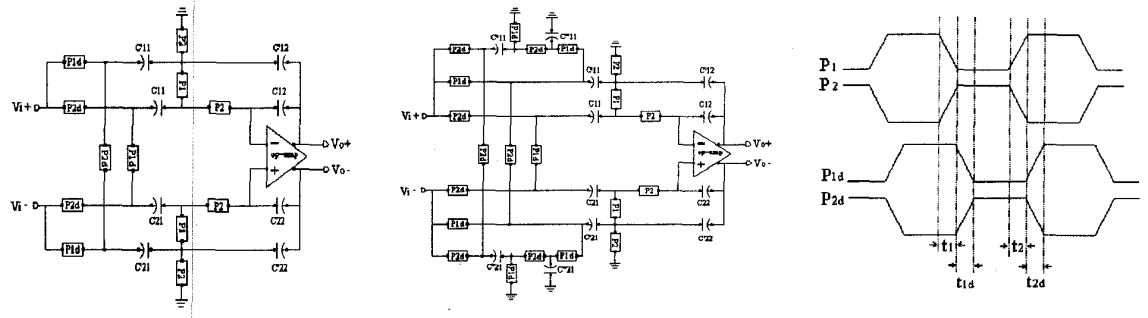


Fig.3: New structure of integrator(a) $FGCI_1$,(b) $FGCI_2$,(c) Timing diagram of phase delay

In the conventional SC integrator the finite DC gain of the integrator is equal to the op-amp gain [1]. Therefore, we need a very high gain op-amp to achieve good performance. However, a good high gain op-amp is not easy to design and implement. In the low voltage (below 3.3V) design the good high gain op-amp is even hard to be designed and implemented. Therefore, the gain-compensation approach is adopted. Here the gain-compensated SC integrators that were proposed by Larson [9] and Hurst [10] are used to enhance the DC gain, and the schematics are shown in Fig. 2(a) (GCI_1) and Fig. 2(b) (GCI_2) respectively.

GCI_1 works under the condition of slow-moving of input (the input signal frequency is much smaller than the sampling frequency). GCI_2 can handle fast-moving input. With fully differential technique and phase delay clock approach, we modify GCI_1 and GCI_2 to $FGCI_1$ and $FGCI_2$. $FGCI_1$ and $FGCI_2$ are shown in Fig. 3(a) and Fig 3(b) respectively. Because of the phase delay approach, there need four clock phases, which are P1, P2, P1d and P2d, and Fig. 3(c) is the timing diagram.

4. Fourth-Order MASH ΣΔ Modulator Implementation

The behavior model of the fourth-order MASH ΣΔ modulator is shown in Fig. 4. In order to alleviate mismatch problems, we design this multistage fourth-order ΣΔ modulator in two stages, and each stage is composed of a second-order ΣΔ modulator. Compared to the design of the first-order ΣΔ modulator in the first stage, our approach can reduce the leak-through noise much more.

In order to minimize errors due to input-offset voltage that might occur because of clock feedthrough noise or op-amp input-offset voltage, we realize the fourth-order MASH ΣΔ modulator with fully differential gain-compensated SC integrator and the schematic diagram is shown in Fig.5. Since the input of the ΣΔ modulator is changing slowly, therefore $FGCI_1$ is used for the input of the first integrator. The input signal of the other integrators is from the output of the previous integrator, and the frequency is changing with the sampling frequency. Therefore, $FGCI_2$ is used for the other integrators.

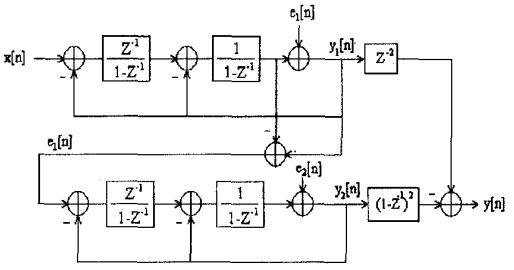


Fig. 4: Model of fourth-order MASH ΣΔ modulator

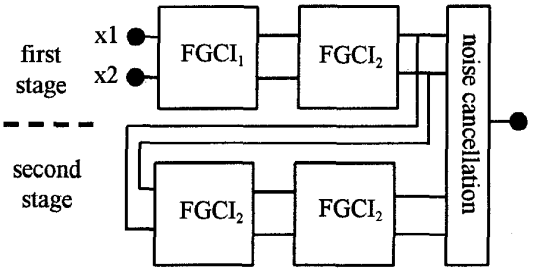


Fig. 5: The schematic diagram of fourth-order MASH ΣΔ modulator

5. The results of simulation

This MASH fourth-order ΣΔ Modulator is implemented in silicon with 0.5 μm double-poly double-metal CMOS process and the VLSI layout is shown in Fig. 8. The performance of this ΣΔ modulator is simulated by HSPICE. A sweep of the signal-to-noise ratio (SNR) versus input amplitude for this modulator is shown in Fig. 6. The peak SNR is 91.02dB. For this plot the modulator clock rate is 2MHz and the input frequency is 4KHz.

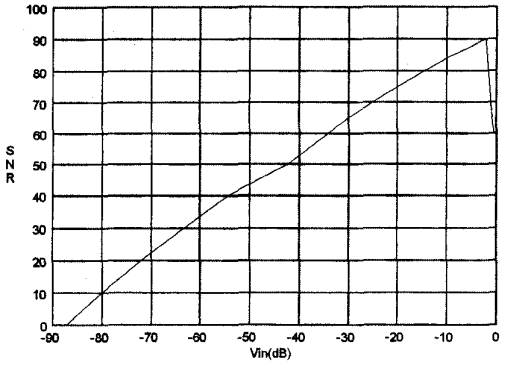


Fig. 6: Plot of SNR vs input amplitude

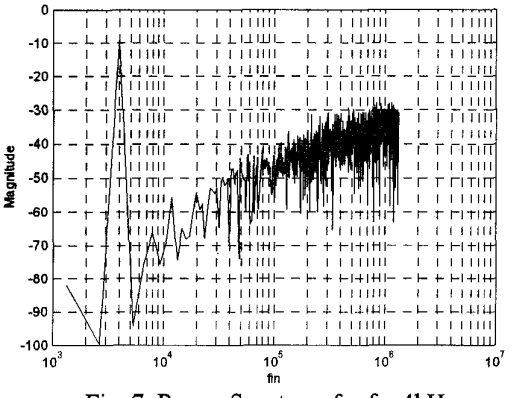


Fig. 7: Power-Spectrum for f_{in}=4kHz

To demonstrate the linearity of the modulator, a 4096-point FFT of output using a Blackman-Harries window is shown in Fig. 7. The input signal is at 2.1dB below full scale and its frequency is 4KHz. The overall performance and characteristics of 4th-order MASH ΣΔ modulator are summarized in Table I.

Table I: modulator measured performance

Parmeter	Value
Technology	0.5um CMOS
Signal bandwith	40kHz
Sampling rate	2MHz
Power supply	3.3V
Peak SNR	91.02dB
Power dispassion	4.22m Watt
Chip area	1.8mm^2

6. Conclusion

A 3.3V multistage fourth-order ΣΔ modulator with gain-compensation, fully differential pair, and phase delay SC integrator is presented. We use the gain-compensation structure to design the SC integrator and the gain of the integrator can be tolerated to a mid gain and make the design and implement more feasible. The other arrangements can reduce the noise and thus to achieve a high resolution ΣΔ modulator. The simulation of this modulator shows that this approach is good for the multistage ΣΔ modulator.

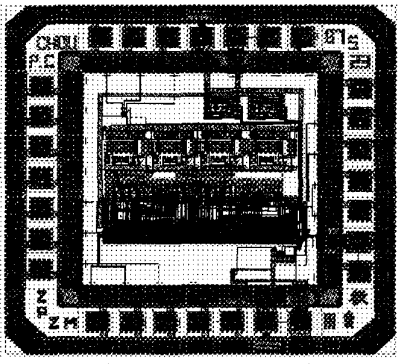


Fig. 8: Layout of modulator

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