Forward Converters Using a CPLD-based Control Technique to Obtain a Fast Transient Load Response

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Abstract—Today, using the conventional technique to obtain the fast transient load response for the forward converter is not easy. Therefore, in order to overcome this problem, a forward converter with a complex programmable logic device (CPLD) technique added is presented herein along with a hysteresis voltage-controlled pulse width modulation (PWM) scheme and the maximum current limiting, without any analogue-to-digital converters (ADCs). Also, some protection functions are added to enhance the reliability of the proposed topology, thereby allowing this converter to be likely to approach to industrial products. The validity of the proposed topology is demonstrated via some experimental results compared with those created from the conventional topology.

Keywords— CPLD, forward converter, hysteresis

I. INTRODUCTION

Conventionally, the controller for the forward converter is almost based on the analogue circuit which tends to be affected significantly by temperature variation, noise interference, system propagation delay, etc, thus allowing the instability to tend to occur. In general, the cascade control technique has been widely adopted to control the forward converter. Hence, the overall bandwidth of such a converter is limited, below about 10kHz. Thus, the digital signal control technique [1] has been presented. However, the digital signal processor (DSP) always comes along with the analogue to digital converter (ADC) that with high speed and accurate solution is expensive and hence limits the overall bandwidth of the forward converter to some extent. As a result, in this paper a complex programmable logic device (CPLD) based controller with the hysteresis voltage-controlled pulse width modulation (PWM) scheme and the maximum current limiting is presented without using any ADCs to realize the fast transient load response for the forward converter, along with some protection functions.

Since the CPLD belongs to the hardware circuit, it has no problem in timing sequence needed by the DSP, thereby allowing many processes to go at the same time with the system propagation delay reduced as minimum as possible. This is a key point in a system with fast transient load response required. The very high-speed integrated circuit hardware description language (VHDL) is utilized herein to design the hardware in the CPLD.

As generally acknowledged, there is poor utilization of the main transformer in the traditional forward converter when energy is being transferred from the primary side to the secondary side only during the on period [2], and hence there are many topologies of resetting magnetization current which are developed to increase the transformer utilization rate [3][4]. The structure in [4] is taken herein due to its easiness of solving the values of the components required by the snubber circuit and due to its better cooperation with the CPLD. Moreover, the forward converter is normally used in the continuous current mode (CCM), where the low current ripple does not place a heavy duty on the filter capacitor. Nevertheless, in the CCM, the closed-loop response is poor and can be difficult to stabilize. Therefore, in this paper, in order to improve the transient load response of the forward converter, the operating mode from no load to full load is designed to vary from the discontinuous current mode (DCM) to the CCM, and the overall design procedure for the proposed system begins from the definition of the current slew rate of the output inductor. Since in the DCM the switching frequency of the forward converter using the hysteresis voltage-controlled PWM scheme is varied with the load, several skills are applied to the CPLD not only to make the frequency of the PWM signal concentrated in the neighborhood of a certain value so as to render the output voltage ripple and noise filtered out conveniently over the whole range of loads, but also to upgrade the transient load response significantly.

II. OVERALL SYSTEM DESCRIPTION AND PRINCIPLES OF OPERATION

Fig. 1 shows the block diagram of the overall system of the proposed CPLD-based forward converter. The main power and its peripherals containing control and protection circuits are described below.

A. Main Power

The main power circuit is based on the conventional forward converter with some modifications. Not only is there an inductance-capacitance LC snubber in the primary side of the main transformer MT to reset the flux as soon as the main switch M_1 is turned off, but also there is a synchronous rectifier M_2 used to replace the diode so as to enhance the efficiency of the converter. Besides, because the source current from the CPLD is not sufficient to drive the MOSFET, one MOSFET drive MD is added to upgrade the CPLD's capability of current sourcing. The remainder of the main power contains the freewheeling diode D_O, the output inductor L_O, and the output capacitor C_O.

B. Under-voltage Lockout Circuit

The under-voltage lockout (UVLO) circuit is utilized to start this converter on the condition that the input voltage rises to some value, so as to avoid undesired destruction of components and error action of the system.

C. Maximum Current Limiting Circuit

The maximum current limiting (MCL) circuit is used to protect the converter from being damaged during an over-current fault condition and enables the converter to restart as the fault is removed.
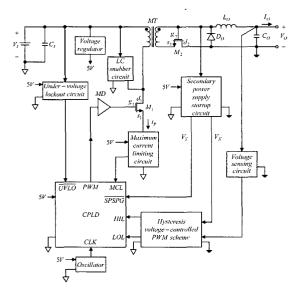

Fig. 1. Block diagram of the overall system of the proposed CPLD-based forward converter.

D. Primary Voltage Regulator and Secondary Power Supply Startup Circuit

The primary voltage regulator comprised of the LM7805 5V positive power regulator is used as the primary power supply feeding the components in the primary side of the MT. As to the secondary power supply startup circuit, it is employed not only to power the components in the secondary side of the MT, but also to tell the CPLD whether the secondary power supply startup circuit is ready or not, so as to avoid sending error signals to the CPLD.

E. Voltage Sensing Circuit and Hysteresis Voltage-controlled PWM Scheme

In order to obtain the fast transient load response of the proposed CPLD-based forward converter, the hysteresis voltage-controlled PWM scheme is taken herein, as in Fig. 1. For the convenience of derivation and design, assuming that the converter operates in the CCM without considering the overdrive of the comparator and the propagation delay of the system, the calculated hesteresis band h_c and then some observations are made as follows, according to Fig. 2.

Principles of operation:

$$\Delta V_O = V_{C_O} + V_{ESL} + V_{ESR}$$

$$= \begin{cases} \dfrac{1}{C_O} \cdot \int_{t_1}^{t_2} i_{L_O} d\tau + ESL \cdot \dfrac{di_{L_O}}{dt} + ESR \cdot i_{L_O} & \text{for } t_1 < t \le t_2 \\ \dfrac{1}{C_O} \cdot \int_{t_2}^{t_3} i_{L_O} d\tau + ESL \cdot \dfrac{di_{L_O}}{dt} + ESR \cdot i_{L_O} & \text{for } t_2 < t \le t_3 \end{cases} \quad (1)$$

From Fig. 2 and (1),

$$\Delta V_{Opp} = ESR \cdot \Delta I + ESL \cdot f_s \cdot \Delta I / [D' \cdot (1 - D')] . \quad (2)$$

Assuming $ESR \gg ESL \cdot f_s / [D' \cdot (1 - D')]$,

$$\Delta V_{Opp} = ESR \cdot \Delta I . \quad (3)$$

Also, $h_c \overset{\Delta}{=} k_v \cdot \Delta V_{Opp}$. \quad (4)

And, $\Delta I = D' \cdot V_O / (L_O \cdot f_s)$. \quad (5)

Thus, $h_c = k_v \cdot ESR \cdot D' \cdot V_O / (L_O \cdot f_s)$. \quad (6)

where $D' = t_{off} / T_s$. \quad (7)

$$f_s = 1 / T_s = 1 / (t_{on} + t_{off}) . \quad (8)$$

L_O : output inductor

C_O : output capacitor

ESL : equivalent series inductance of the C_O

ESR : equivalent series resistance of the C_O

ΔV_O : output voltage ripple

V_{C_O} : part of the ΔV_O created from the C_O

V_{ESL} : part of the ΔV_O created from the ESL

V_{ESR} : part of the ΔV_O created from the ESR

i_{L_O} : AC current flowing through the L_O

D' : complement of the duty cycle D

k_v : voltage sensing factor

f_s : switching frequency

h_c : calculated hysteresis band

ΔI : peak-to-peak current of the i_{L_O}

T_s : switching period

t_{on} : turn-on interval of the T_s

t_{off} : turn-off interval of the T_s

Observations:

If the operating condition is transferred from the CCM to the DCM, the corresponding D' is obviously reduced, and after the demagnetizing of the L_O, the output voltage is free running down because only the energy stored in the C_O is released to the load, thereby causing the f_s to be decreased.
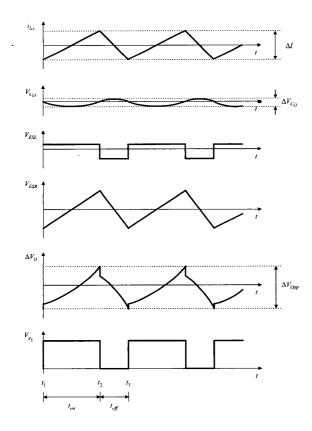
F. Oscillator and CPLD

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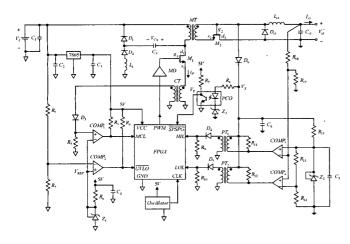Fig. 2. Details of the output voltage ripple ΔV_O .

Fig. 3. Detailed description of the overall system of the proposed CPLD-based forward converter.

The oscillator is utilized to provide the clock, CLK, to the CPLD. The purpose of the CPLD is to execute the logic operation. Based on the mention above, the resulting digital signals, created from the UVLO circuit, the

secondary power supply startup circuit, the MCL circuit and the hysteresis voltage-controlled PWM circuit, are all sent to the CPLD to involve generating the required PWM signal to drive the M_1. Besides, there are three skills applied to the CPLD, to be discussed later.

III. CIRCUIT DESIGN CONSIDERATION

The specifications of the proposed forward converter are given as follows.

DC input voltage: $V_I = 12$ V

Input voltage ripple at full load: $\Delta V_I \leq 500$ mV

Turn ratio of the main transformer: $N_{MT} = n_S / n_P = 5 / 6$

DC output voltage: $V_O = 5$ V

Rated DC output current: $I_{O\_rated} = 10$ A

Current slew rate of the L_O: $SR = di_{L_O} / dt|_{t_{on}} = 2$ A/μs

Switching frequency at full load: $f_s = 200$ kHz

Output voltage ripple: $\Delta V_O \leq 100$ mV

Operating condition at full load: CCM

Efficiency at full load: $\eta \geq 85$ %

A. Main Power

As shown in Fig. 1, the procedure for the overall circuit design begins from the point of view of the current slew rate of the output inductor L_O. Then, the value of the L_O can be calculated to be 2.5 μH according to (9).

$$L_O = (V_I \cdot N_{MT} - V_O) / SR . \qquad (9)$$

Therefore, the HK-RM136-15A1RA inductor is chosen for the L_O.

Since the converter operates in the CCM at full load, the D can be calculated to be 0.5 using (5) and hence the peak-to-peak value of the i_{L_O} is about 5 A using (12).

$$D = V_O / (V_I \cdot N_{MT}) . \qquad (10)$$

Also, $D' = 1 - D$. $\qquad (11)$

Combining (5) and (11), $\Delta I = (1 - D) \cdot V_O / (L_O \cdot f_s)$. (12)

Based on this mentioned above, it is obvious that this converter operates from the DCM to the CCM if the load is varied from no load to full load.

If the ΔV_{C_O} represents the peak-to-peak value of the V_{C_O} in the CCM, as illustrated in the first term of (1), then it can be expressed as following.

$$\Delta V_{C_O} = (\Delta I \cdot T_s) / (8 \cdot C_O) . \qquad (13)$$

If $\Delta V_{C_O} \leq \Delta V_{Opp} / 10$, where ΔV_{Opp} is shown in (3),

then $ESR \cdot C_O \geq 1.25 \cdot T_s$. $\qquad (14)$

Taking into account the values of both the C_O and the

ESR, two T510X477006AS solid tantalum capacitors, paralleled to reduce the ESR, are chosen herein for the C_O. Therefore, the values of the C_O and the ESR are about 940 μF and 12.5 mΩ respectively, corresponding to (14). In theory, the ΔV_{Opp} can be approximately calculated to be 62.5 mV according to (3). Nevertheless, in practice, the actual ΔV_{Opp} is larger than such a theoretical value in consideration of the system propagation delay under the condition that the voltage-controlled PWM scheme is applied.

As for the M_1 and M_2, PSMN005-55P MOSFETs are chosen herein. Since the CPLD's capability of current sourcing is not sufficient, one MIC4467 MOSFET drive is chosen for the MD to improve this. Then, according to the typical input charge Q_i characteristics of the MOSFET and the peak current i_{pk} of the MOSFET drive, the estimated switching interval Δt can be calculated to be 120 ns based on (15).

$$\Delta t = (2 \cdot Q_i) / i_{pk} . \tag{15}$$

Then, the value of the Δt is about one twentieth times of the turn-on interval of the switching period T_s in the CCM, that is, the Δt negligibly affects the turn-on performance of the MOSFET.

As to the LC snubber circuit depicted in Fig. 3, two diodes D_1 and D_2 are utilized to reset the flux and to discharge the energy stored in the capacitor C_S respectively. Before calculating the values of the snubber's parameters, the magnetization inductance L_m of the main transformer MT is approximately measured to be about 110 μH at full load. Then, the resonance period τ in terms of the L_m and C_S can be obtained as follows.

$$\tau = 2 \cdot \pi \cdot \sqrt{L_m \cdot C_S} . \tag{16}$$

As the main switch M_1 is turned off, the energy stored in the magnetization inductance L_m is passed to the C_S during the period τ_p which is one fourth times of the period τ.

$$\tau_p = \tau / 4 = 0.5 \cdot \pi \cdot \sqrt{L_m \cdot C_S} . \tag{17}$$

Without considering the leakage inductance of the MT, and with taking into account of the fundamental component of the switching frequency f_s because the amplitude of the other frequencies contributed to the $\hat{i}_m$ is attenuated by a factor of n^2 where n=2m+1, m=1, 2, 3..., the fundamental magnetization peak current $\hat{i}_m$ can be approximately calculated to be 0.09 A based on (18).

$$\hat{i}_m = V_I / (2 \cdot \pi \cdot f_s \cdot L_m) . \tag{18}$$

If the maximum voltage across the C_S, $\hat{V}_{C_S}$, is set to

about two times of the DC input voltage V_I, then the D_1 has the capability of enduring the reverse voltage which is about two times of the V_I, and hence an MBR0540 Schoktty diode is chosen for the D_1. As to the D_2, it endures only the reverse voltage of the V_I, and thus an MBR0520L Schoktty diode is selected. Also, based on the results above, the value of the C_S can be obtained to be 15 nF based on (19).

$$C_S = (L_m \cdot \hat{i}_m^2) / (2 \cdot V_I)^2 . \tag{19}$$

Since the value of the C_S is varied with the frequency, it is adjusted up to 4.4 nF to get $\hat{V}_{C_S} = 2V_I$. So, $\tau_p = 1.1 \, \mu s$. This value of the τ_p is obtained at full load, to be used later in participating in programming the CPLD. As for the L_1, it functions as a current limiter when the energy stored in the C_S is released to the ground through the M_1, or as a negligible component when the energy stored in the C_S is sent back to the DC link through the MT. Therefore, the value of the L_1 is set to about 12 μH, one tenth times of the value of the L_m. As to the D_O, an STPS20L25 Schottky diode is chosen herein. Besides, the value of the C_I is calculated to be 2350 μF based on (20) but is set to 3300 μF actually.

$$C_I = (2 \cdot V_O \cdot I_O) / (\Delta V_I^2 \cdot f_s \cdot \eta) . \tag{20}$$

B. Under-voltage Lockout and Maximum Current Limiting Circuits

As illustrated in Fig. 3, the voltage reference V_{REF} for the under-voltage lockout and maximum current limiting circuits is set to 2.5 V, which is created by the TL431 three-terminal shunt programmable regulator Z_1 with the resistor, $R_6 = 5.1 \, k\Omega$, used as a current limiter and the capacitor, $C_4 = 1 \, \mu F$, used as a filter. The information on the input voltage and the primary current i_P is sent to two LM319 comparators, $COMP_1$ and COM_2, whose pull-up resistors, R_3 and R_4, are both set to 5.1 kΩ and also employed to pull up the input ports of the CPLD to 5 V. As soon as the V_I rises to 10 V with the voltage dividing resistors, R_1 and R_2, set to 6 kΩ and 2 kΩ respectively, the $COMP_2$ sends a low level signal to tell the CPLD that power-on is ready. As for the maximum current limiting circuit, the turn ratio of the current transformer is set to $n_S/n_P = 26/1$. Thus, the maximum current limiting value, I_{MAX}, can be calculated to be about 15 A using (21) and $R_5 = 4.3 \, \Omega$.

$$I_{MAX} = [(n_S / n_P) \cdot V_{REF}] / R_5 . \tag{21}$$

The moment the i_P reaches 15A, the $COMP_1$ passes a high level signal to the CPLD to pull down the PWM signal to the ground. Moreover, the 1N4148 diode D_3 is used to avoid destroying the $COMP_1$ due to an undesired negative spike noise.

C. Secondary Power Supply Startup Circuit

As delineated in Fig. 3, the PC357N3T photocoupler PCO with the minimum current transfer rate, $CTR_{MIN} = 200\%$, is cascaded with the NTE5010SM zener Z_3 which has the nominal voltage, $V_{Z_3} = 5.1\,V$. The resistor, $R_8 = 499\,\Omega$, is used to create a proper current so as to generate a suitable voltage drop across the resistor, $R_7 = 1\,k\Omega$, which is also used as a pull-up resistor for the input port of the CPLD. As the voltage V_X is raised to the neighborhood of 7 V, the output voltage of the PCO, V_Y, can be calculated to be 0.2 V using (22).

$$V_Y = 5 - CTR_{MIN} \cdot [(V_X - V_{Z_3} - V_D) / R_8] \cdot R_7 . \quad (22)$$

where the V_D denotes the forward voltage drop across the diode in the PCO. Thus, this value gives the CPLD a low level signal to tell the CPLD that the secondary power supply startup circuit is OK. Furthermore, the 1N4148 diode D_6 is employed as a half rectifier, and the capacitor, $C_6 = 22\,\mu F$, is utilized to fix the V_X to a stable DC value.

D. Voltage sensing and Hysteresis
   Voltage-controlled PWM Circuits

As described in Fig. 3, the voltage divider, used to send the output voltage information to the LM319 comparators $COMP_3$ and $COMP_4$, is comprised of two resistors, $R_{16} = 1\,k\Omega$ and $R_{17} = 1\,k\Omega$, which are also used as a dummy load. Therefore, the voltage sensing factor k_v is obtained to be 0.5. By substituting the values of the associated components into (6), the calculated hysteresis band h_c can be calculated to be about 31 mV.

Also, the output reference voltage for the hysteresis voltage-controlled PWM circuits is set to 2.5 V, which is created by the TL431 three-terminal shunt programmable regulator Z_2 with the resistor, $R_{15} = 2.7\,k\Omega$, used as a current limiter, and with the capacitor, $C_5 = 22\,\mu F$, together with the R_{15}, used as a soft starter. According to the h_c, the resistors R_{13} and R_{14} are obtained to be 56 Ω and 4.7 kΩ, respectively. However, the actual hysteresis band h_a is smaller than the h_c due to the effect of the overdrive of the comparator. Consequently, the h_a is obtained by fixing the value of the R_{14} and adjusting the value of the R_{13} down so as to get the desired switching frequency, $f_s = 200\,kHz$, at full load. Eventually, the value of the R_{13} is obtained to be about 20 Ω and hence the h_a is about 11 mV. Therefore, the resulting output information from the $COMP_3$ and $COMP_4$ is passed to the CPLD through the pulse transformers PT_1 and PT_2 to involve partially determining the turn-on and turn-off instants of the PWM signal. The turn ratios of the PT_1 and PT_2 are set to $n_S/n_P = 20/36$, not only to reduce the output voltage sent to the CPLD but also to decrease the magnetization current required. Furthermore, the resistors, $R_{11} = 1\,k\Omega$ and $R_{12} = 1\,k\Omega$, are used not only to reset

the flux of the PT_1 and PT_2 but also to pull up the $COMP_3$ and $COMP_4$ to the V_X. Also, there are two 1N4148 diodes, D_4 and D_5, used to protect the CPLD from being destroyed by a negative spike noise, and two resistors, $R_9 = 5.1\,k\Omega$ and $R_{10} = 5.1\,k\Omega$, used not only to function as the loads of the PT_1 and PT_2 but also to always keep pulling down the I/O ports of the CPLD to the ground until the secondary power supply startup circuit is ready.

E. Oscillator and CPLD

As shown in Fig. 4, the external clock, CLK, created by the oscillator, is set to 8 MHz, i.e. the CLK period is $\tau_{CLK} = 0.125\,\mu s$, which is used as the system clock of the CPLD. Moreover, the rising edge of the CLK is employed as a synchronously triggering signal. The purpose of the CPLD is to execute the logic operation, therefore the resulting signals from the peripherals are all sent to the CPLD to generate a proper PWM signal to drive the M_1. In this case, an EPM7032S CPLD, made by Altera, has the capability of self-start as soon as the power feeds the CPLD. It is noted that '1' indicates that the bit's status is in the high voltage level and '0' implies that the bit's status is in the low voltage level. Before the converter enters into soft starting, the input voltage should be above the preset V_I, 10 V, corresponding to $\overline{UVLO} = '1'$, and after this, the secondary power supply startup circuit gives a power good signal to the CPLD if the V_X, denoted in Fig. 1, is above 7 V, corresponding to $\overline{SPSPG} = '1'$.
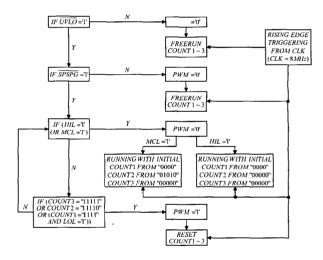

Fig. 4. Flowchart of the proposed CPLD-based control.

Most of all, there are three counters, COUNT1 with four bits, COUNT2 with five bits and COUNT3 with five bits. The COUNT1 is used to control the minimum turn-off period of the M_1 that is set to about two times of the period τ_p shown in (17), i.e. $2\,\mu s$, so as to give sufficient flux resetting time to the MT over the whole

range of loads. The COUNT2 is utilized to enhance the transient startup/load response, with the turn-on instant of the M_1 determined by the event that the turn-off period of the M_1 is over $2.5\,\mu s$ which starts to be calculated as soon as a maximum current limiting event occurs, that is to say, MCL $='1'$. Since the hysteresis voltage-controlled scheme possesses various switching frequencies under different loads in the DCM, the COUNT3 is employed to make the switching frequency f_s close to 200 kHz under any load in the steady state, by forcing the M_1 to turn on as soon as the turn-off period is over $4\,\mu s$. Moreover, these counters are reset if PWM $='1'$, while they begin counting from zero if PWM $='0'$. And, HIL $='1'$ implies that the output voltage after the voltage sensing circuit touches the top of the actual hysteresis band h_a, thereby turning off the M_1, whereas LOL $='1'$ denotes that the output voltage after the voltage sensing circuit touches the bottom of the h_a, thus turning on the M_1.

IV. EXPERIMENTAL RESULTS

To further demonstrate the validity of the proposed CPLD-based forward converter depicted in Fig. 1, the conventional UC3843-based forward converter under the same specifications is used as a comparison. The former adopts only single-loop control using the hysteresis voltage-controlled PWM scheme with the maximum current limiting, whereas the latter takes double-loop control using the peak current mode PWM control strategy.

Fig. 5 shows the measured transient load response of the proposed CPLD-based control from no load to full load. The variation in the load current shown in Fig. 5(a) is larger than that from no load to full load, because the dynamic load is created by a MOSFET switch, which is utilized to conduct associated resistors. The resulting droop and recovery time are measured to be about 120 mV and $15\,\mu s$ respectively, as illustrated in Fig. 5(b).

Moreover, the MCL event is actuated during the transient load period as shown in Fig. 5(c). However, under the same conditions described in Fig. 5, Fig. 6 shows the transient load response of the conventional UC3843-based control, where the resulting droop and recovery time are measured to be about 190 mV and $600\,\mu s$ respectively. As seen obviously, the droop of the proposed topology is three-fifths times of that of the conventional one and the recovery time of the proposed topology is one-fortieth times of that of the conventional one. This is because the proposed technique increases the overall bandwidth and hence reduces the system propagation delay.

V. CONCLUSIONS

Increasing the overall bandwidth of the forward converter and hence reducing its system propagation delay are considered to be the best method to upgrade its

performance of the transient load response. Therefore, the CPLD-based control, together with the hysteresis voltage-controlled PWM scheme and the maximum current limiting is presented herein. The performance of the transient load response of the proposed CPLD-based forward converter only under single-loop control is demonstrated by the experimental results compared with those generated from the conventional UC3843-based forward converter under double-loop control.
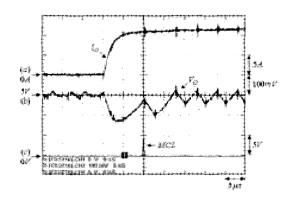

Fig. 5. Measured transient load response from no load to full load using the proposed CPLD-based control: (a) load current I_O; (b) output voltage V_O; (c) maximum current limiting MCL event.
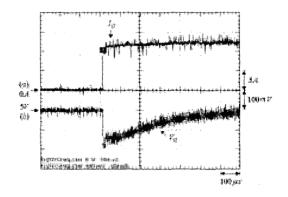

Fig. 6. Measured transient load response from no load to full load using the conventional UC3843-based control: (a) load current I_O; (b) output voltage V_O.

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