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Post-silicon Receiver Equalization Metamodeling by Artificial Neural Networks

Francisco E. Rangel-Patiño, José E. Rayas-Sánchez, Andres Viveros-Wacher, José L. Chávez-Hurtado, Edgar A. Vega-Ochoa, and Nagib Hakim

***Abstract*— As microprocessor design scales to the 10 nm technology and beyond, traditional pre- and post-silicon validation techniques are unsuitable to get a full system functional coverage. Physical complexity and extreme technology process variations severely limits the effectiveness and reliability of pre-silicon validation techniques. This scenario imposes the need of sophisticated post-silicon validation approaches to consider complex electromagnetic phenomena and large manufacturing fluctuations observed in actual physical platforms. One of the major challenges in electrical validation of high-speed input/output (HSIO) links in modern computer platforms lies in the physical layer (PHY) tuning process, where equalization techniques are used to cancel undesired effects induced by the channels. Current industrial practices for PHY tuning in HSIO links are very time consuming since they require massive lab measurements. An alternative is to use machine learning techniques to model the PHY, and then perform equalization using the resultant surrogate model. In this paper, a metamodeling approach based on neural networks is proposed to efficiently simulate the effects of a receiver equalizer PHY tuning settings. We use several design of experiments techniques to find a neural model capable of approximating the real system behavior without requiring a large amount of actual measurements. We evaluate the models performance by comparing with measured responses on a real server HSIO link.**

***Index Terms*— artificial neural network, equalization, HSIO, metamodels, post-silicon validation, receiver, simulation, system margining.**

I. Introduction

Technology scaling and advanced silicon packaging techniques are allowing high density integration. However, as process technologies scale down, traditional IC design methods are challenged by the problem of increased silicon process variation. Design-time optimization and post-silicon tuning are the techniques currently used to maximize the parametric yield based on statistical design for high-speed computer systems. Accurate simulations for design-time optimization techniques which exhaustively explore the design space are computationally very expensive given the complexity of the system involved [1].

On the other hand, adaptive tuning in analog design has been widely adopted to confront the silicon process variation. Tunable elements are proposed to adjust the analog circuit performance after chip fabrication [2], [3]. These tunable elements provide a way to reconfigure high-speed input/output (HSIO) links in post-silicon servers to mitigate the effects of system channels' variability [4], as illustrated in Fig. 1. The adoption of circuit tuning, however, introduces new design challenges. A tunable circuit may contain a large number of control knobs for reconfiguration, and it is extremely expensive to repeatedly run a large number of highly accurate simulations over all process variations and environmental corners to validate a given design during pre-silicon validation [5], making necessary to perform tuning at post-silicon based on physical measurements.

Post-silicon tuning requires first to measure the circuit performance and then determine the optimal knobs set based on measurement results. Current industrial practices for post-silicon tuning in HSIO links are very time consuming since they are typically based on exhaustive testing requiring massive lab measurements [4], resulting in an extremely high cost. Therefore, the challenge is how to make the post-silicon circuit tuning inexpensive by significantly reducing the number of lab measurements.

Several methodologies have been proposed to address the aforementioned challenge. A method to do transmitter (Tx) equalization based on eye diagram analysis and direct optimization is proposed in [1]. In contrast, the problem of receiver (Rx) equalization is addressed in [4] by doing surrogate-based optimization using Kriging modeling. An extension of [4] is presented in [6] by developing several surrogate models to choose the most accurate one at the expense of increasing data collection time on the real system, and then perform numerical optimization of the PHY tuning Rx equalizer settings for a SATA Gen 3 channel topology.

In this paper, we explore the application of machine learning techniques to address the aforementioned challenge with emphasis on the modeling process. In contrast to [6], here we are not looking for a highly accurate surrogate model, but we are looking for a suitable coarse neural model by employing a frugal DoE method for data collection. This is done not only for SATA Gen3, but also for USB3 Superspeed Gen 1. The ultimate goal will be to use the resultant coarse neural model in a space mapping optimization approach [7], [8]. Also in contrast to [6], in this paper we provide an abbreviated review

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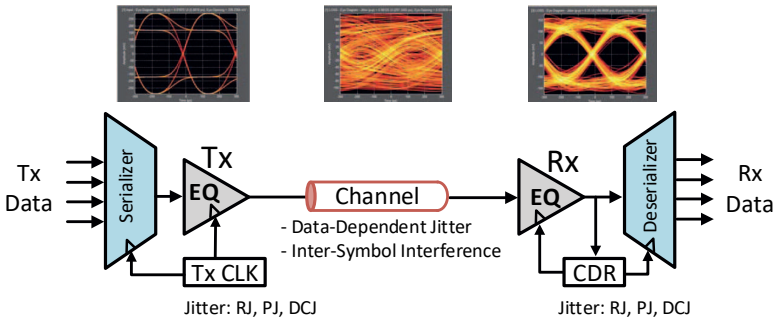

Fig. 1. HSIO link reconfiguration in post-silicon server validation to cancel out the effects of system channels' variability.

on machine learning techniques as applied to post-silicon validation, as well as a detailed formulation on the ANN-based modeling and training technique employed, including the regularization scheme to control ANN generalization. More specifically, we propose a metamodeling approach, based on artificial neural networks (ANN), to efficiently simulate the silicon equalizer circuitry of the Rx. The model is generated using a frugal set of training data exploiting several design of experiments (DoE) approaches to reduce the number of test cases. We evaluate the neural model performance by comparing with actual measured responses on an industrial server validation platform. First, a hardware mechanism provides automated measurements over multiple test cases. We then arrange the data collected to develop a learning procedure to predict the circuit behavior by an artificial neural network. This neural model can be later used for efficient circuit tuning at post-silicon validation. The proposed methodology is illustrated by the neural modeling of a silicon equalizer Rx circuitry of two current industrial HSIO channel topologies: USB3 Super-speed Gen 1 and SATA Gen 3.

The rest of this paper is organized as follows. In Section II, we provide a brief review on machine learning as applied to post-silicon validation. The ANN-based receiver modeling technique is presented in Section III. The system for experimental evaluation is described in Section IV. Results from the proposed modeling approach are compared to actual measured responses in Section V. The last section presents our conclusions.

II. Machine Learning in Post-Silicon Validation

Machine learning algorithms, a branch of artificial intelligence, build statistical models from examples, which are then used to make predictions when faced with cases not seen before. On the other hand, the goal of HSIO post-silicon validation is to understand and validate from physical examples the correct operation of the design, identify bugs, and determine the best settings to avoid any failure. Machine learning aims at a similar goal: learning from examples and identifying the structure in a system [9]. In addition, the large volume of data generated from typical post-silicon testing suggests the application of machine learning techniques to predict post-silicon behavior.

There has been recent research on machine learning applications to some areas of post-silicon validation. In [10], authors propose a trace signal simulation-based selection technique that exploits machine learning to efficiently identify a small set of key traceable signals, reducing the simulation cost. An algorithm that applies anomaly detection techniques is proposed in [9] for post-silicon bug diagnosis. Machine learning is applied in [11] to bug finding in post-silicon server power management. In [12], several neural models are developed to learn post-silicon unknown module-level behavior and diagnose localized design bugs.

It is seen that all the previously cited machine learning approaches to post-silicon validation have been focused on developing efficient and reliable techniques for diagnosis, failure detection, or bug identification. An assessment of several surrogate modeling and DoE techniques to identify the best approach for a HSIO link model and simulation is realized in [6]. From that assessment, polynomial-based surrogate modeling (PSM) combined with Sobol DoE with 150 samples was identified as the most accurate surrogate model [6]. While an accurate model is desirable for direct optimization, it can be still expensive since it requires a significant amount of lab measurements to develop. Additionally, the required time to evaluate and even to train any metamodel becomes, for practical purposes, insignificant as compared to the time required to collect the measurement data. On the other hand, it has been demonstrated [13], [14] that both ANN and polynomial functional surrogates perform better than SVM and Kriging surrogates in cases with a very limited amount of training data, while polynomial surrogates exhibit better performance than ANN only in cases with low-dimensionality and small regions of interest, Then, we propose a neural modeling approach to efficiently approximate the effects of a HSIO post-silicon receiver equalizer with a very reduced set of testing and training data, and possibly a large number of knobs. The resultant metamodel, obtained from the proposed inexpensive method, could later be used as a fast coarse model in a space mapping approach [7], [8] to find the optimal equalizer settings that maximize the actual HSIO performance.

Several other innovative approaches have been proposed to find out the optimal performance of the system in post-silicon validation. In [15], [16], and [5] a statistical framework, referred to as Bayesian model fusion (BMF), is proposed for post-silicon tuning. That methodology is based on the assumption that an early-stage (e.g. pre-silicon) model or data is already available. Then, a relatively small number of post-silicon measurements may be required by applying Bayesian

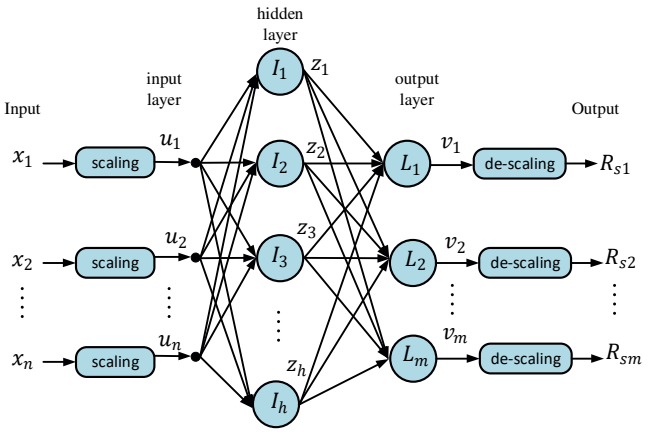

Fig. 2. Three-layer perceptron with n inputs, h inner-product hidden neurons and m linear output neurons [31].

inference, allowing the post-silicon cost of tuning to be substantially reduced. However, that BMF approach is not feasible in a post-silicon environment if not enough pre-silicon model information is available, as in our case. Similarly, in [17], a methodology for programming a reconfigurable RF receiver is proposed, showing a maximum efficiency of 27.5× speed-up as compared with the exhaustive search. In [18], a post-silicon tuning methodology is proposed based on a dynamic programming algorithm [19] combined with a fast Monte Carlo simulation flow for statistical analysis and discrete optimization. That method achieves 20× speed-up as compared with the exhaustive search. These methodologies allow very significant acceleration of the tuning time in post-silicon validation. However, it is unclear if they could be easily applied when dealing with a large number of circuit knobs, which is our case.

III. ANN-BASED RECEIVER METAMODELING

Metamodels are scalable parameterized mathematical models that emulate the component behavior over a user-defined design space. These techniques allow developing an approximation of a system response within a design region of interest, following a "black-box" approach. The problem of modeling in post-silicon validation can be mapped to a mathematical problem of function estimation in presence of noisy data points. The most popular estimators are neural networks and Kernel estimation. In [20], authors demonstrate the functional estimation capability of an artificial neural network (ANN).

ANNs are particularly suitable to approximate high-dimensional and highly nonlinear relationships, in contrast to more conventional methods such as numerical curve-fitting, empirical or analytical modeling, or response surface approximations [21]. ANNs have been used in many areas of applications, including RF and microwave circuits [22], EM-based design optimization [23], control process, telecommunications, biomedical, remote sensing, pattern recognition, and manufacturing, just to mention a few [24]. Recently, ANNs have been used for HSIO simulations, but they were focused to model the nonlinear relationships

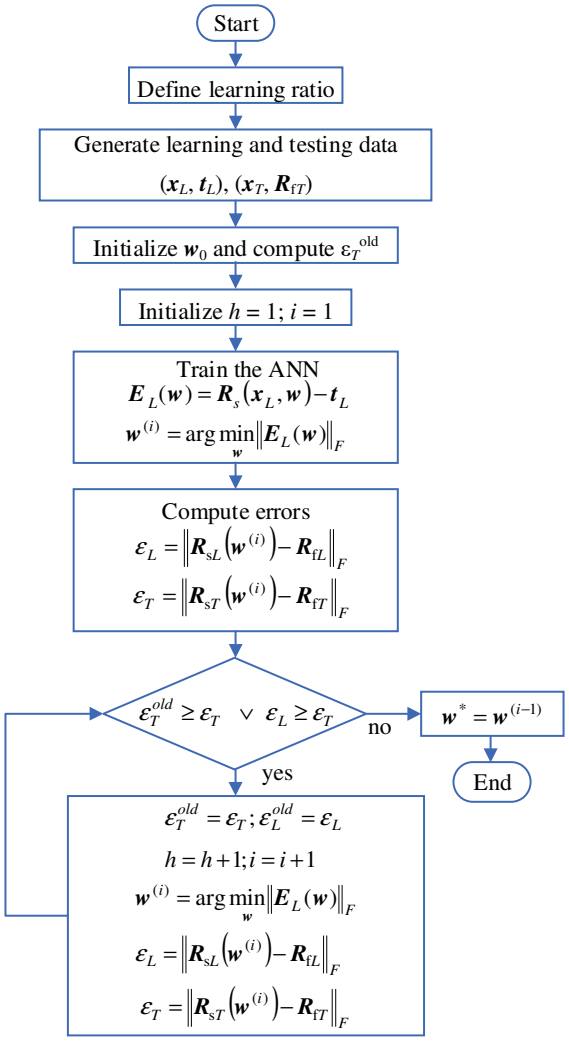

Fig. 3. Algorithm for training the neural model; ANN complexity is increased until generalization deteriorates.

between channel parameters and system performance to speed up system simulations, as in [25] and [26]. In [27], authors proposed ANNs for eye diagram modeling based on simulations, and they use an adaptive sampling method for data collection process.

Once trained, ANN provides a fast way to perform a large number of I/O links and channel simulations that take into account the die-to-die process variations, board impedances, channel losses, add-in cards, end-point devices, and operating conditions [28]. ANN modeling involves two inter-related process: a) neural network model development - that includes selection of representative training data, network topology, and training algorithms; and b) neural model validation - the neural network model is tested and validated according to its generalization performance in a given region of interest. A large amount of training data is usually needed to ensure model accuracy, and this could be very expensive in the post-silicon validation environment. An alternative to reduce the dimension of the learning set is to properly select the learning points by using DoE, to ensure adequate design space parameter coverage [29].

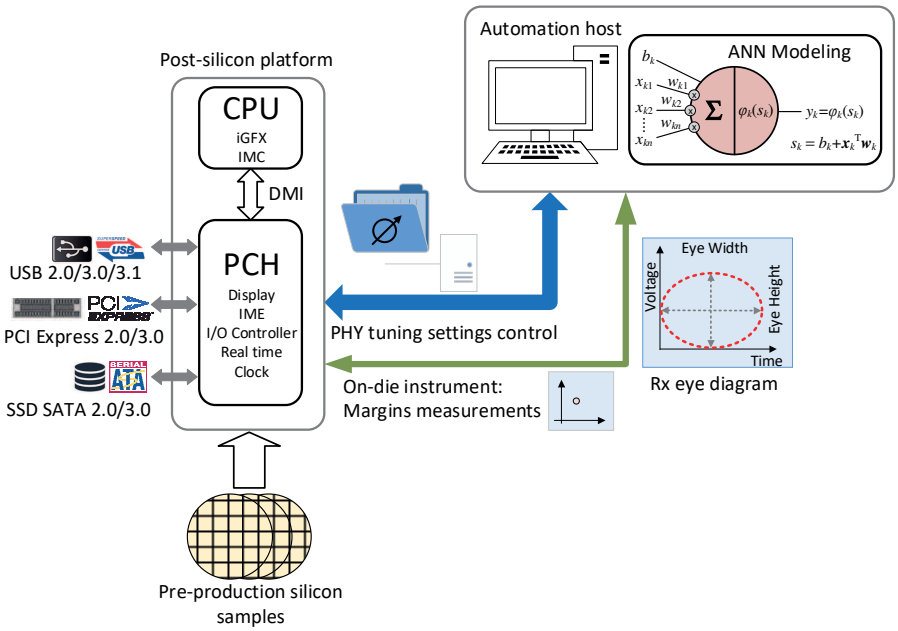

Fig. 4. HSIO server post-silicon hardware configuration for Rx metamodeling.

A. *ANN Topology*

Multilayer perceptrons are feedforward networks widely used as the preferred ANN topology. Since a 3-layer perceptron (3LP) is in principle sufficient for universal approximation [30], we use a 3LP to implement our neuromodel, with n inputs (equal to the number of Rx knobs), h hidden neurons, and m outputs (number of system responses of interest), as shown in Fig. 2. The required complexity of the ANN, determined by h, depends on the generalization performance for a given set of training and testing data [31]. Following [32], we gradually increase h during training as a regularization scheme.

B. *ANN Modeling and Training*

Let $\boldsymbol{R}_\mathrm{f} \in \Re^m$ represent the actual electrical margining system response, denoted as a fine model response, which consists of the eye width $e_\mathrm{w} \in \Re$ and eye height $e_\mathrm{h} \in \Re$ of the measured eye diagram,

$$\boldsymbol{R}_\mathrm{f}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = \left[e_\mathrm{w}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \quad e_\mathrm{h}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right]^T \tag{1}$$

The electrical margining system response depends on the Rx knobs settings $\boldsymbol{x} \in \Re^n$, the operating conditions $\boldsymbol{\psi}$ (voltage and temperature), and the devices $\boldsymbol{\delta}$ connected to the system. The ANN is trained to find an optimal vector of weighting factors $\boldsymbol{w}$, such that the ANN response, denoted as $\boldsymbol{R}_s$, is as close as possible to the fine model response for all $\boldsymbol{x}$, $\boldsymbol{\psi}$, $\boldsymbol{\delta}$ in the region of interest,

$$\boldsymbol{R}_\mathrm{s}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta},\boldsymbol{w}) \approx \boldsymbol{R}_\mathrm{f}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \tag{2}$$

The ANN main input-output relationship is denoted as

$$\boldsymbol{R}_s = \boldsymbol{f}(\boldsymbol{x}) \tag{3}$$

We aim to develop a fast and accurate ANN model for $\boldsymbol{f}$ by training the ANN with a set of measured learning data. The learning data are pairs of ($\boldsymbol{x}_L$, $\boldsymbol{t}_L$), with L = 1, 2…, l, where $\boldsymbol{t}_L$ contains the desired outputs or targets (obtained from measurements) for the ANN model at the $\boldsymbol{x}_L$ inputs, and l is the total number of learning samples. During training, we keep fixed the system at voltage/temperature (VT) nominal conditions and without changing the external device. Under these conditions, $\boldsymbol{\psi}$ and $\boldsymbol{\delta}$ remain constant. Therefore, the ANN model during training is treated as

$$\boldsymbol{R}_{sL} = \boldsymbol{R}_\mathrm{s}(\boldsymbol{x}_L,\boldsymbol{w}) \tag{4}$$

The ANN performance during training is evaluated by computing the difference between ANN outputs and the targets for all the learning samples,

$$\boldsymbol{E}_L(\boldsymbol{w}) = \boldsymbol{R}_{sL}(\boldsymbol{x}_L,\boldsymbol{w}) - \boldsymbol{t}_L \tag{5}$$

where $\boldsymbol{E}_L$ is the learning error matrix.

Following [32], the problem of training the ANN is formulated as

$$\boldsymbol{w} = \arg\min_{\boldsymbol{w}} \left\|\boldsymbol{E}_L(\boldsymbol{w})\right\|_F \tag{6}$$

To control the generalization performance while solving (6), we use T testing base points ($\boldsymbol{x}_T$) not used during training. The scalar learning and testing errors are given by

$$\varepsilon_L = \left\|\boldsymbol{R}_{sL}(\boldsymbol{x}_L,\boldsymbol{w}) - \boldsymbol{R}_{fL}\right\|_F \tag{7}$$

$$\varepsilon_T = \left\|\boldsymbol{R}_{sT}(\boldsymbol{x}_T,\boldsymbol{w}) - \boldsymbol{R}_{fT}\right\|_F \tag{8}$$

where $\boldsymbol{R}_{fT}$ and $\boldsymbol{R}_{sT}$ are the output matrices of the fine model and ANN model, respectively, at the T testing base points, and $\boldsymbol{R}_{fL}$ is the fine model response at the L learning base points.

The 3LP is trained by using the Bayesian regularization [33] method available in MATLAB Neural Network Toolbox. The algorithm for training the ANN is shown in Fig. 3. We first define the learning ratio to split the pairs of inputs and targets into the learning and testing datasets. The learning process often begins by initializing the ANN weights with arbitrary values using a random number generator [34], however, in our case we use a decoupling network process with initial set of inputs and outputs to compute initial weighting factors $\boldsymbol{w}_0$ and corresponding initial error $\varepsilon_T^{\mathrm{old}}$. Then, we start training the 3LP with just one hidden neuron (h = 1), and calculate the

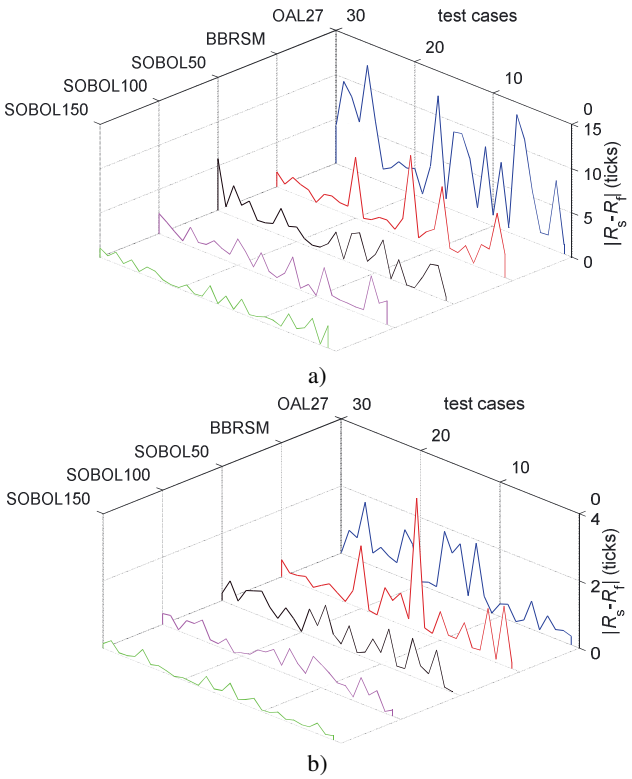

Fig. 5. Comparison of SATA neural model generalization performance for different DoE techniques: a) eye height error; b) eye width error.

corresponding learning and testing errors. We keep increasing the complexity of the ANN (h) until the current testing error is larger than the previous one, and the current learning error is smaller than the current testing error, as in [32] (see Fig. 3).

IV. Experimental System Configuration and DoE Approaches

The system under test is a server post-silicon validation platform, comprised mainly of a CPU and a platform controller hub (PCH). The PCH is a family of Intel microchips which integrates a range of common I/O blocks required in many market segments, and these include USB [35], PCI Express [36], SATA [37], SD/SDIO/MMC, and Gigabit Ethernet MAC, as well as general embedded interfaces such as SPI, I2C, UART, and GPIO. The PCH also provides control data paths with the Intel CPU through direct media interface (DMI), as shown in Fig. 4. This figure also shows the automation mechanism to read the Rx eye diagram parameters (eye width and eye height). Within the PCH, our methodology was tested on two different HSIO links: USB3 Super-speed Gen 1 and SATA Gen 3.

The measurement system is based in the system margin validation (SMV) process [4], [38], which is a methodology to verify the signal integrity of a circuit board and assess how much margin is in the design relative to silicon characteristics and processes. The SMV methodology consists of measuring the Rx functional eye width and eye height by using on-die design for test (DFT) features until the eye opening has been

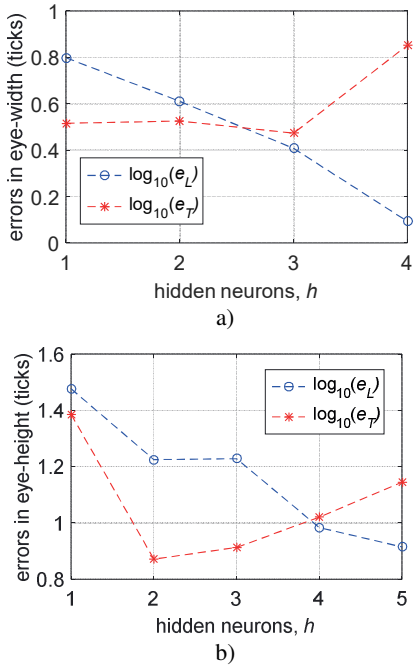

Fig. 6. Learning and testing errors during SATA neural training using Sobol50, for a) eye width and b) eye height.

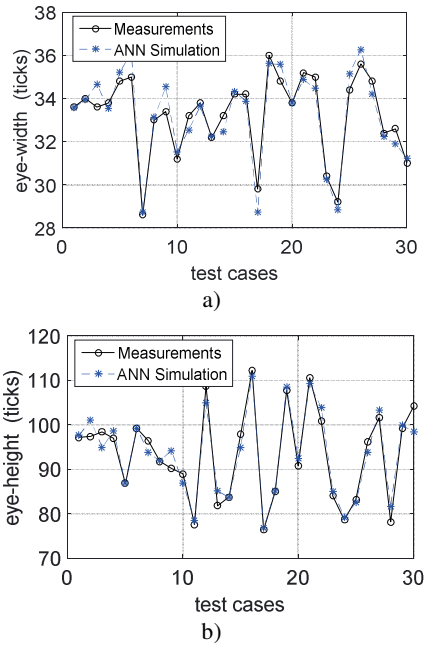

Fig. 7. Neural model generalization performance using Sobol50 for a) SATA eye width; b) SATA eye height.

shrunk to a point where the Rx detects errors or the system fails [6].

We employ three different DoE techniques to explore the desired solution space with a reduced number of test cases. For each test case, we use seven input variables that represent Rx knobs (n = 7), which are settings used in three main Rx circuitry blocks (CTLE, VGA, and CDR), and then we retrieve the eye measurements from the system under test. The employed DoE techniques are: 1) Box Behnken (BB), which is type of second order response surface methodology (RSM)

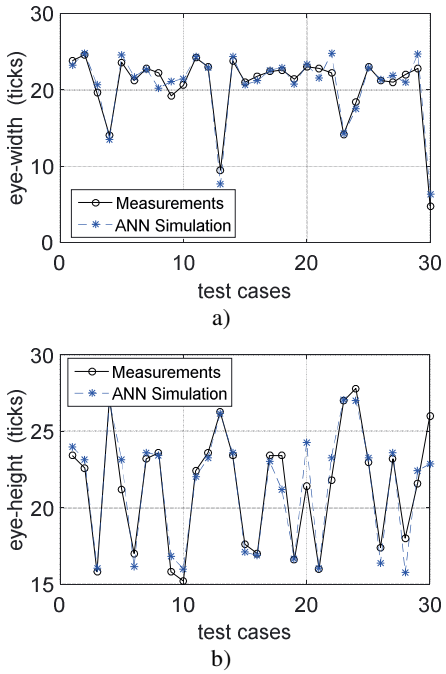

Fig. 8. Neural model generalization performance using Sobol50 for a) USB width; and b) USB eye height.

that combines factorial designs with balanced incomplete blocks designs [39], using 62 experiments; 2) orthogonal arrays (OA) [40], using an $L_{27}(3^9)$ array in order to capture non-linear effects in the objective function by only running 27 experiments; and 3) Sobol [41] low-discrepancy sequence to sample the solution space. Given the quasi-Monte Carlo sampling approach of Sobol, the solution space is better explored as the number of samples increases, at the expense of increasing test time on the real system. Therefore, we use three different Sobol DoE, denoted as Sobol50, Sobol100, and Sobol150, with 50, 100, and 150 samples, respectively.

System margining testing is very time consuming when running many test cases for PHY tuning. A single test case with 3 repetitions can take up 20 minutes, and then running a Sobol150 can take up 50 hours of testing for a single VT corner. The objective of comparing several DoEs is to find a suitable sampling strategy that provides adequate ANN model performance with the least amount of testing time.

V. Neural Modeling Results

Figure 5 shows the generalization error of the already trained neural model (at $\boldsymbol{w}^*$), comparing the different DoEs for SATA. It is seen that the best performance is achieved with Sobol150. The three Sobol cases provide the best generalization performance, as confirmed in Fig. 5. However, Sobol50 is able to achieve acceptable accuracy with only 50 samples.

Figure 6 shows the learning performance of the neural training algorithm for SATA. The best performance is achieved with h = 3 for the eye width ANN, achieving a maximum relative learning error of 3.65%, and 7.63% for the relative testing error. For the eye height ANN, best performance is achieved with h = 4, yielding 7.98% of learning error and 6.75% of testing error. Thus, the metamodels are able to reach above 90% of accuracy for these initial sampling points.

The neural model response at $\boldsymbol{w}^*$ and h = 3 for e_w and h = 4 for e_h from Sobol50 is compared in Fig. 7a and Fig. 7b, respectively, with the fine model (real measurements), by using 30 testing base points not used during training, in order to test the generalization performance. It is observed that the neural model effectively simulates the actual physical measurements with a total relative error of 1.7% for the e_w response and 2.5% for the e_h response. In other words, the ANN metamodel is able to predict margins with up to 95% of accuracy when using equalization values not used during the ANN training.

We obtained similar results for the case of USB3 Super-speed Gen 1, where we use ten input variables (n = 10) that represent the corresponding Rx knobs, which again are settings used in the three main Rx circuitry blocks. For the sake of brevity, we present only the final results in Fig. 8. It is seen that for USB, the resultant neural model also effectively simulates the fine model (physical platform), finding a total relative error of 6.7% for the e_w response, as shown in Fig. 8a, and a 5.7% relative error for the e_h response, as shown in Fig. 8b. This metamodel performance was achieved using also a Sobol50 DoE.

VI. Conclusions

We presented a metamodeling technique based on artificial neural networks to efficiently simulate the effects of the receiver equalization circuitry in industrial HSIO links. The neural model is trained using different DoE approaches to identify the best system response sampling strategy that yields an acceptable neural model with a very reduced set of learning and testing samples. The resultant neural model approximates with sufficiently accuracy the eye diagram of a real post-silicon HSIO validation platform. The proposed machine learning approach can be exploited to develop extremely efficient vehicles to drive fast PHY tuning in HSIO links.

References

[1] I. Duron-Rosales, F. Rangel-Patino, J. E. Rayas-Sánchez, J. L. Chávez-Hurtado, and N. Hakim, "Reconfigurable FIR filter coefficient optimization in post-silicon validation to improve eye diagram for optical interconnects," in *Int. Caribbean Conf. Devices, Circuits, and Systems (ICCDCS-2017)*, Cozumel, Mexico, Jun. 2017, pp. 85-88.

[2] H. Huang and E. K. F. Lee, "Design of low-voltage CMOS continuous time filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1168-1177, Aug. 2001.

[3] G. Miller, M. Timko, H.-S.Lee, E. Nestler, M. Mueck, and P. Ferguson, "Design and modeling of a 16-bit 1.5msps successive approximation adc with non-binary capacitor array," in *Proc. Int. Great Lakes Symp. on VLSI*, Washington, D. C, April 2003, pp. 161 - 164

[4] F. Rangel-Patino, A. Viveros-Wacher, J. E. Rayas-Sanchez, E. A. Vega-Ochoa, I. Duron-Rosales, and N. Hakim, "A holistic methodology for system margining and jitter tolerance optimization in post-silicon validation," in *IEEE MTT-S Latin America Microw. Conf. (LAMC)*, Puerto Vallarta, Mexico, Dec. 2016, pp. 1-3.

[5] F. Wang, P. Cachecho, W. Zhang, S. Sun, X. Li, R. Kanj, and C. Gu, "Bayesian model fusion: large-scale performance modeling of analog

and mixed-signal circuits by reusing early-stage data," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 35, no. 8, pp. 1255-1268, Aug. 2016.

[6] F. E. Rangel-Patiño, J. L. Chávez-Hurtado, A. Viveros-Wacher, J. E. Rayas-Sánchez, and N. Hakim, "System margining surrogate-based optimization in post-silicon validation," *IEEE Trans. Microwave Theory Techn.*, vol. 65, no. 9, pp. 3109-3115, Sep. 2017.

[7] J. W. Bandler, Q. Cheng, S. A. Dakroury, A. S. Mohamed, M. H. Bakr, K. Madsen and J. Søndergaard, "Space mapping: the state of the art," *IEEE Trans. Microwave Theory Tech.*, vol. 52, no. 1, pp. 337-361, Jan. 2004.

[8] J. E. Rayas-Sánchez, "Power in simplicity with ASM: tracing the aggressive space mapping algorithm over two decades of development and engineering applications," *IEEE Microwave Magazine*, vol. 17, no. 4, pp. 64-76, Apr. 2016.

[9] A. DeOrio, Q. Li, M. Burgess, and V. Bertacco, "Machine learning-based anomaly detection for post-silicon bug diagnosis," in *Europe Conf. & Exhibition (DATE) in Design, Automation & Test, Grenoble*, France, March 2013.

[10] K. Rahmani, S. Ray, and P. Mishra, "Postsilicon trace signal selection using machine learning techniques," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 2, pp. 570-580, Aug. 2017.

[11] P. Pridhiviraj, T. Dheerendra, and P. Muralidhar, "Adaptive post-silicon server validation using machine learning," *Int. J. Applied Information Systems (IJAIS),* vol. 9, no. 1, pp. 24-32, June 2015.

[12] S. Deyati, B. Muldrey, A. Banerjee, and A. Chatterjee, "Atomic model learning: A machine learning paradigm for post silicon debug of RF/analog circuits," in *IEEE 32nd VLSI Test Symp. (VTS),* Napa, CA, April 2014.

[13] J. L. Chavez-Hurtado and J. E. Rayas-Sánchez, "Polynomial-based surrogate modeling of RF and microwave circuits in frequency domain exploiting the multinomial theorem," *IEEE Trans. Microwave Theory Techn.*, vol. 64, no. 12, pp. 4371-4381, Dec. 2016

[14] J. E. Rayas-Sánchez, J. L. Chavez-Hurtado, and Z. Brito-Brito, "Design optimization of full-wave EM models by low-order low-dimension polynomial surrogate functionals," *Int. J. Numerical Modelling: Electron. Networks, Dev. Fields*., vol. 30, no. 3-4, e2094, May-Aug. 2017.

[15] J. Plouchart, F. Wang, X. Li, et al., "Adaptive circuit design methodology and test applied to millimeter-wave circuits," *IEEE Design & Test*, vol. 31, no. 6, pp. 8-18, July 2014.

[16] X. Li, F. Wang, S. Su, et al. "Bayesian model fusion: a statistical framework for efficient pre-silicon validation and post-silicon tuning of complex analog and mixed-signal circuits," in *IEEE/ACM Int. Conf. Computer-Aided Design (ICCAD)*, San Jose, CA, Dec. 2013.

[17] J. Tao, Y. Wang, M. Jun, et al., "Toward efficient programming of reconfigurable radio frequency (RF) receivers," in *19th Asia and South Pacific Design Automation Conf. (ASP-DAC)*, Singapore, Singapore, Feb. 2014.

[18] X. Li, B. Taylor, Y. Chien, et al., "Adaptive post-silicon tuning for analog circuits: concept, analysis and optimization," in *IEEE/ACM Int. Conf. Computer-Aided Design (ICCAD)*, San Jose, CA, Dec. 2007.

[19] D. Bertsekas, *Dynamic Programming and Optimal Control*, Belmont, MA: Athena Scientific, 2005.

[20] J. Y. Goulermas, P. Liatsis, Z. Xiao-Jun, and P. Cook, "Density-driven generalized regression neural networks (DD-GRNN) for function approximation," *IEEE Trans. Neural Netw.*, vol. 18, no. 6, pp. 1683-1696, Nov. 2007.

[21] G. Vicario, G. Craparotta, and G. Pistone, "Meta-models in computer experiments: Kriging versus artificial neural network," *Qual. Reliab. Engng. Int.*, vol. 32, no. 6, pp. 2055-2065, June 2016.

[22] Q. J. Zhang and K. C. Gupta, *Neural Networks for RF and Microwave Design*. Norwood, MA: Artech House, 2000.

[23] J. E. Rayas-Sánchez, "EM-based optimization of microwave circuits using artificial neural networks: the state of the art," *IEEE Trans. Microwave Theory Techn.*, vol. 52, no. 1, pp. 420-435, Jan. 2004.

[24] S. Haykin, *Neural Networks: A Comprehensive Foundation*. New Jersey, MA: Prentice Hall, 1999.

[25] S. Bistola, "High-speed interconnect simulation using artificial neural networks", in *Intel Design & Test Technology Conference (DTTC)*, Oregon, CA, Oct. 2015.

[26] M. Liu and J. H. Tsai, "USB3.1 silicon and channel design optimization using artificial neural network modeling", in *IEEE Electromagnetic Compatibility and Signal Integrity Symp.*, Santa Clara, CA, May. 2015.

[27] C. H. Goay and P. Goh, "Neural networks for eye height and eye width prediction with an improved adaptive sampling algorithm," in *Asian Simulation Conf. (AsiaSim),* Melaka, Malaysia, Aug. 2017.

[28] W. T. Beyene, "Application of artificial neural networks to statistical analysis and nonlinear modeling of high-speed interconnect systems," *IEEE Trans. Computer-Aided Design of Integrated Circuits Systems*, vol. 26, no. 1, pp. 166-176, Jan. 2007.

[29] Y. Mack, T. Goel, W. Shyy, R. Haftka, "Surrogate model-based optimization framework: A case study in aerospace design," in *Evolutionary Computation in Dynamic and Uncertain Environments. Studies in Computational Intelligence*, S. Yang, YS. Ong, Y. Jin, Ed., Berlin: Springer, 2007, vol. 51, pp. 323-342.

[30] K. Hornik, M. Stinchcombe, and H. White, "Multilayer feedforward networks are universal approximators," *Neural Networks*, vol. 2, no. 5, pp. 359-366, May 1989.

[31] J. E. Rayas-Sánchez, *Neural Space Mapping Methods for Modeling and Design of Microwave Circuits*, Ph.D. Thesis, Dept. of Electrical and Comp. Eng., McMaster University, Hamilton, Canada, 2001.

[32] J. E. Rayas-Sánchez and V. Gutiérrez-Ayala, "EM-based Monte Carlo analysis and yield prediction of microwave circuits using linear-input neural-output space mapping," *IEEE Trans. Microwave Theory Tech.*, vol. 54, no. 12, pp. 4528-4537, Dec. 2006.

[33] D.J.C. MacKay, "Bayesian interpolation," *Neural Computation*, vol. 4, no. 3, pp. 415–447, 1992.

[34] G. Thimm, and J. B. Ra, "High-order and multilayer perceptron initialization," *IEEE Trans. Neural Netw.*, Vol. 8, no. 2, pp. 349-359, Mar 1997.

[35] USB Org. (2016). *Universal Serial Bus Revision 3.1 Specification* [Online]. Available: http://www.usb.org/developers/doc

[36] PCI SIG Org. (2016), *Peripheral Component Interconnect Express 3.1 Specification* [Online]. Available: https://pcisig.com/specifications

[37] SATA Org. (2016), *Serial Advanced Technology Attachment 3.2 Specification* [Online]. Available: http://www.sata-io.org/

[38] A. Viveros-Wacher et al, "SMV methodology enhancements for high speed IO links of SoCs", in *IEEE VLSI Test Symposium (VTS)*, Napa, CA, Apr. 2014, pp. 1-5.

[39] C. F. J. Wu and M. Hamada, *Experiments: Planning, Analysis, and Parameter Design Optimization*, New York, NY: Wiley, 2000.

[40] Y. P. Chang et al, "Design of discrete-value passive harmonic filters using sequential neural-network approximation and orthogonal array", in *IEEE PES Transmission and Distribution Conference & Exposition: Asia and Pacific*, Dalian, China, Aug. 2005, pp. 1-6.

[41] I. M. Sobol, "On the distribution of points in a cube and the approximate evaluation of integrals," *U.S.S.R. Computational Mathematics and Mathematical Physics*, vol. 7, no. 4, pp. 86-112, 1967.

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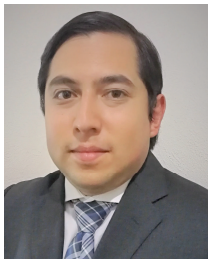

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