Instituto Tecnológico y de Estudios Superiores de Occidente

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Departamento de Electrónica, Sistemas e Informática	DESI - Artículos y ponencias con arbitraje

2018-03

Direct Optimization of a PCI Express Link Equalization in Industrial Post-Silicon Validation (poster)

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High-Speed Links Optimization in Industrial Post-Silicon Validation

Francisco E. Rangel-Patiño, José E. Rayas-Sánchez, and Nagib Hakim

0. ABSTRACT

The optimization of receiver analog circuitry in modern high-speed input/output (HSIO) links is a very time consuming post-silicon validation process. Current industrial practices are based on exhaustive enumeration methods. In this PhD thesis, direct and surrogate-based optimization methods, including space mapping, are proposed based on suitable objective functions to efficiently tune the transmitter (Tx) and receiver (Rx) equalizers coefficients. Evaluation is realized by lab measurements on realistic industrial post-silicon validation platforms.

1. INTRODUCTION

Within the computer server segment, there are conditions that further increase system complexities. These include non-flexible form factors which implies the channel designs remain unchanged. Therefore, physical layer (PHY) tuning based on equalization (EQ) techniques are used to cancel any undesired effect [1]. The current industrial practices to perform PHY tuning consist of an exhaustive enumeration method, turning them into the most time-consuming processes in post-silicon validation [2]. This thesis presents several optimization techniques based on novel objective functions to optimize the Tx and Rx equalizers in a server post-silicon validation platform.

2. RX EQ SURROGATE OPT.

In the current practice for PHY tuning the Rx eye diagram margins are measured and optimized, and then a trade-off analysis is done with the jitter tolerance (JTOL) tests to get a single set of EQ coefficients values that comply with the link specifications.

We present in [1]-[2] a holistic approach to concurrently optimize Rx system margins and JTOL, by defining an innovative objective function that combines both type of measurements. The methodology was tested in a post-silicon industrial environment (Fig. 2.1). Our methodology was tested on three different HSIO links (USB3.0, SATA, and PCIe3).
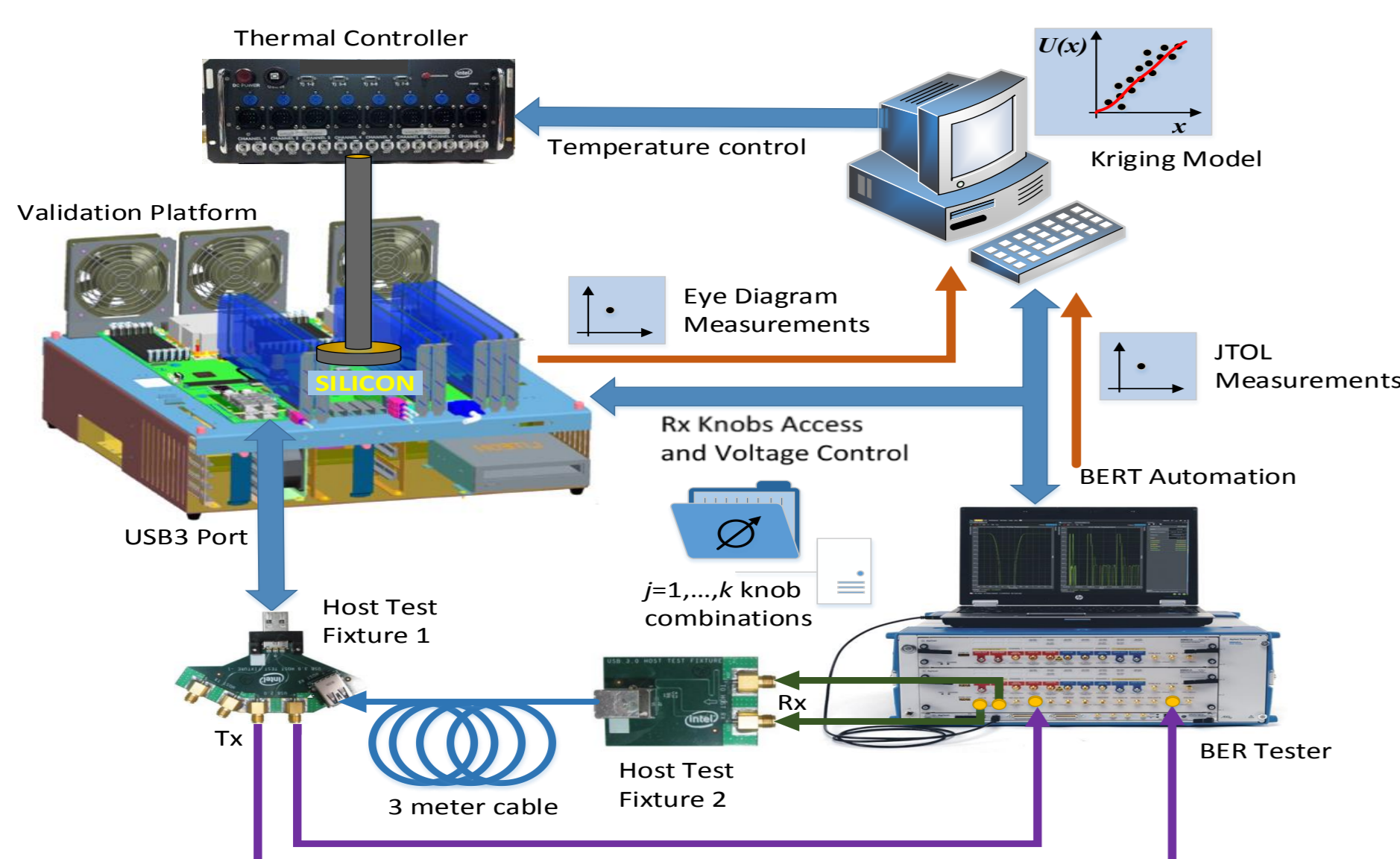

Fig. 2.1. Test setup for USB system margining and JTOL optimization.

We aim at finding the optimal set of coefficients to maximize the eye width (e_w) and eye height (e_h). The holistic approach is realized by adding a JTOL penalty function, such that the optimization finds a set of EQ coefficients that maximize the eye diagram and simultaneously satisfies the JTOL specified mask. Our objective function is defined as

$$U(x) = -w_1[e_w(x,\psi,\delta)][e_h(x,\psi,\delta)] + w_2[e_{wa}(x,\psi,\delta)] + w_3[e_{ha}(x,\psi,\delta)] + r_0^g\|G(x)\|_2^2$$

where $G(x)$ is the JTOL penalty function. x are the EQ coefficients, ψ are the operating conditions, δ are the devices, and r_0^g is the penalty coefficient. The area of the eye diagram and the asymmetries (e_{wa} and e_{ha}) are scaled by weighting factors w_1, w_2, w_3. To minimize $U(x)$, we use Kriging as the surrogate-based approximation method.

The results showed an improvement of 175% on eye diagram area as compared to the initial coefficients, and a 34% improvement as compared with the trade-off approach (Fig. 2.2a). Similarly, the JTOL results showed a substantial improvement (Fig. 2.2b).
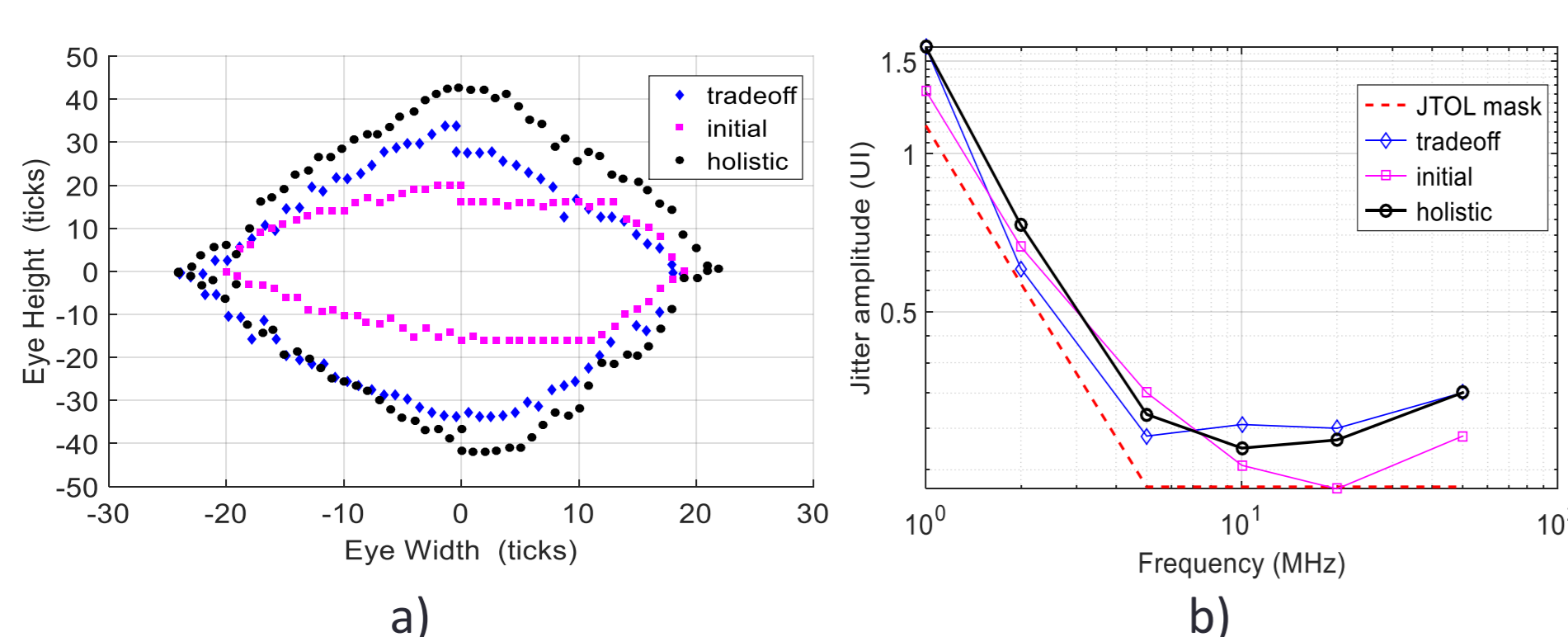

Fig. 2.2. Results comparing the proposed methodology against the initial design and the trade-off approach: a) Eye width versus eye height; b) Jitter tolerance (JTOL) testing.

3. PCIE TX/RX EQ DIRECT OPT.

PCIe specification defines an adaptive mechanism for EQ to determine the optimum value of the Tx and Rx EQ coefficients. The current practice is to find out a subset of coefficient combinations during post-silicon validation, and then program it into the system BIOS. The method consists of using maps of EQ coefficients, which are obtained by measuring the Rx system margins. In [3], we propose an efficient optimization methodology to find out the optimal subset of coefficients for the Tx and Rx.

We aim at finding the optimal set of coefficients to maximize the eye diagram. Here we follow our work in [2] for the objective function. However to avoid selecting an optimal solution with a too high sensitivity, the four margin responses around $u(x^*)$ must be at least 80% (Fig. 3.1) of the value of $u(x^*)$, where C_m, C_0, and C_p represent the three filter taps coefficients in the Tx, C_r is the tap coefficient in the Rx, and $u_{i,j}$ are the objective function values for the i-th C_m and j-th C_p values.
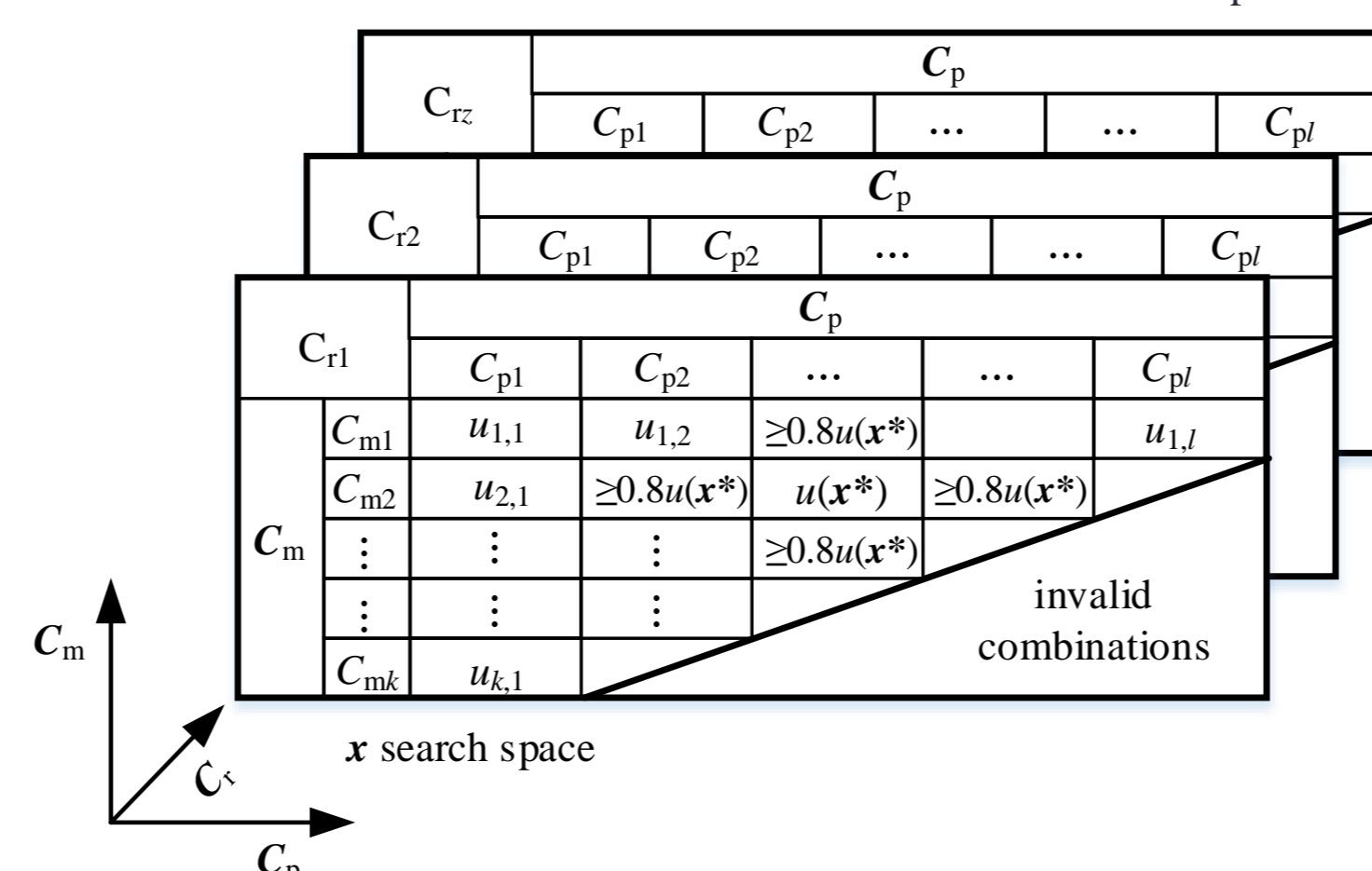

Fig. 3.1. EQ map coefficients search space for optimization.

The optimization problem can be defined through a constrained formulation by adding a penalty term, as

$$U(x) = -w_1[e_w(x,\psi,\delta)][e_h(x,\psi,\delta)] + w_2[e_{wa}(x,\psi,\delta)] + w_3[e_{ha}(x,\psi,\delta)] + \gamma_0^l|L(x)|^2$$

where γ_0^l is the penalty coefficient, and $L(x)$ is a corner limits penalty function. We solve $U(x)$ by using a combination of pattern search and Nelder-Mead methods. The system under test is an Intel validation platform as shown in Fig. 3.2.
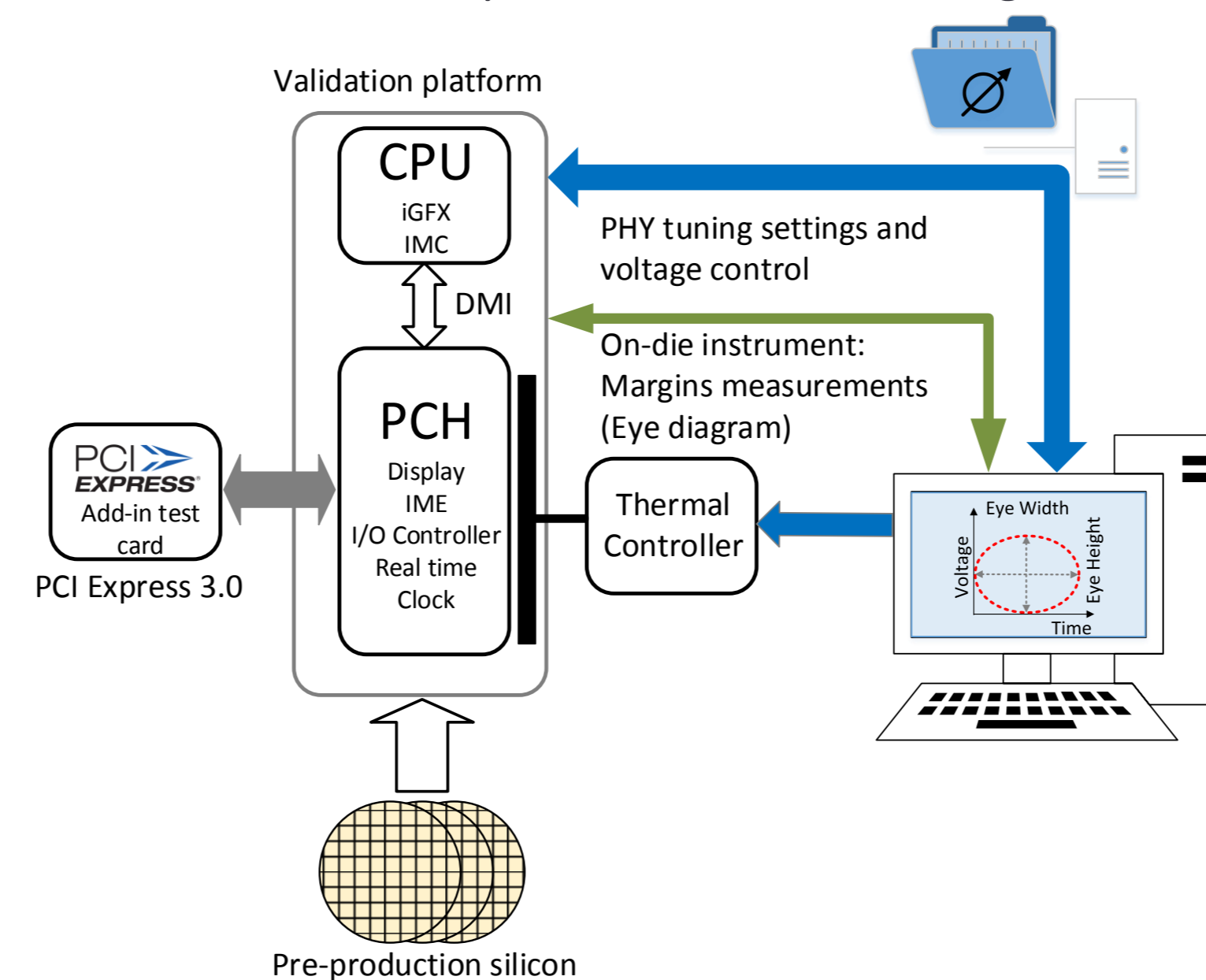

Fig. 3.2 PCI Express test setup: an Intel server post-silicon validation.

Through the optimization process, we arrive to a set of Tx and Rx coefficients in just 47 iterations, as shown in Fig. 3.3a.
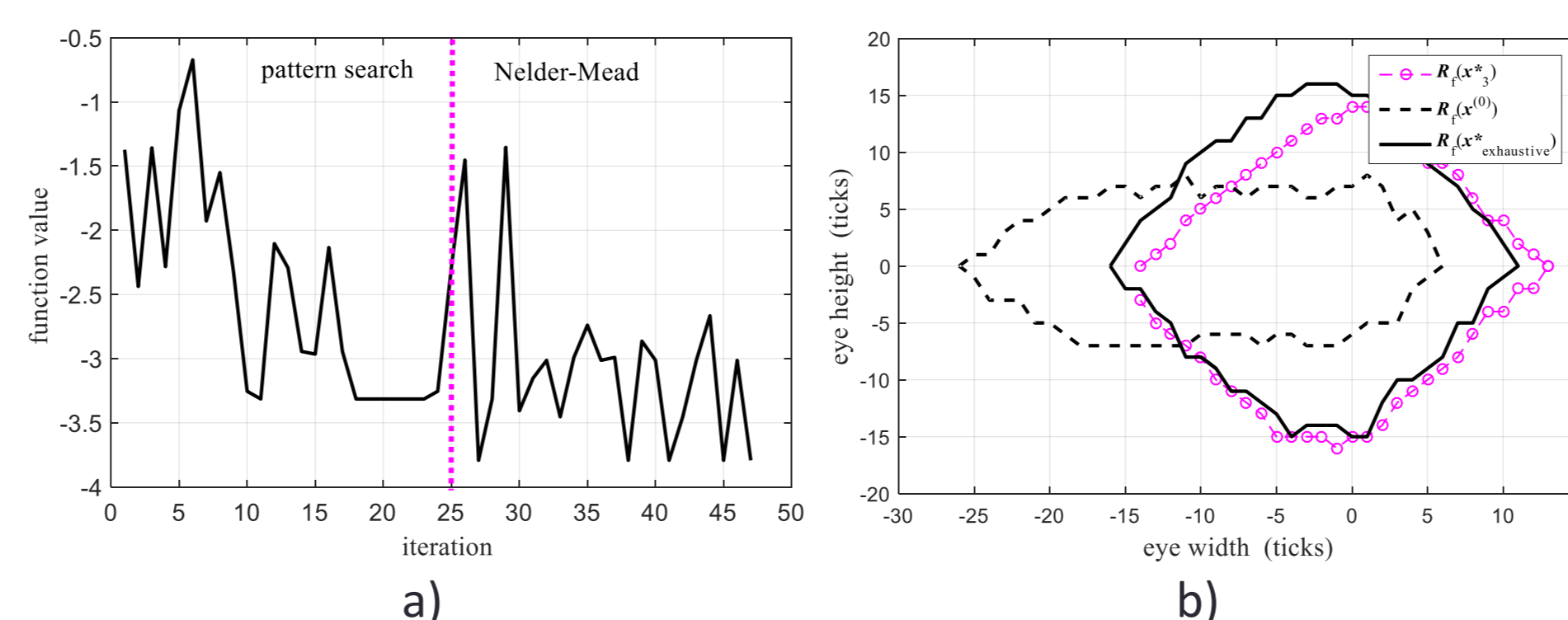

Fig. 3.3. a) Objective function across iterations; b) Eye diagram: proposed methodology ($R_l(x^*)$) vs initial design ($R_l(x0)$) vs current method ($R_l(x^*_{exhaustive})$).

The optimized coefficients yield an eye diagram improvement by 35% as compared to that one with the initial coefficients (Fig. 3.3b). The efficiency of this approach is demonstrated by a significant time reduction in post-silicon validation.

4. SFP TX EQ DIRECT OPT.

Ethernet enhanced small form factor pluggables (SFP+), are regulated by a Tx eye diagram mask in terms of voltage and time. Per IEEE standard, the EQ for SFP+ Tx may be accomplished with a 3-tap FIR filter, where C_m, C_0 and C_p represent the three filter coefficients. SFP+ Tx FIR filter is not self-adaptive, and then tuning is required during post-silicon validation. The current post-silicon practices for SFP+ tuning consumes a large amount of validation time. We propose in [4] an efficient optimization technique, by defining an effective objective function and by using direct numerical optimization in a post-silicon validation platform.

The eye height (e_h) is a function of the standard deviation (σ) of the histograms as shown in Fig. 4.1
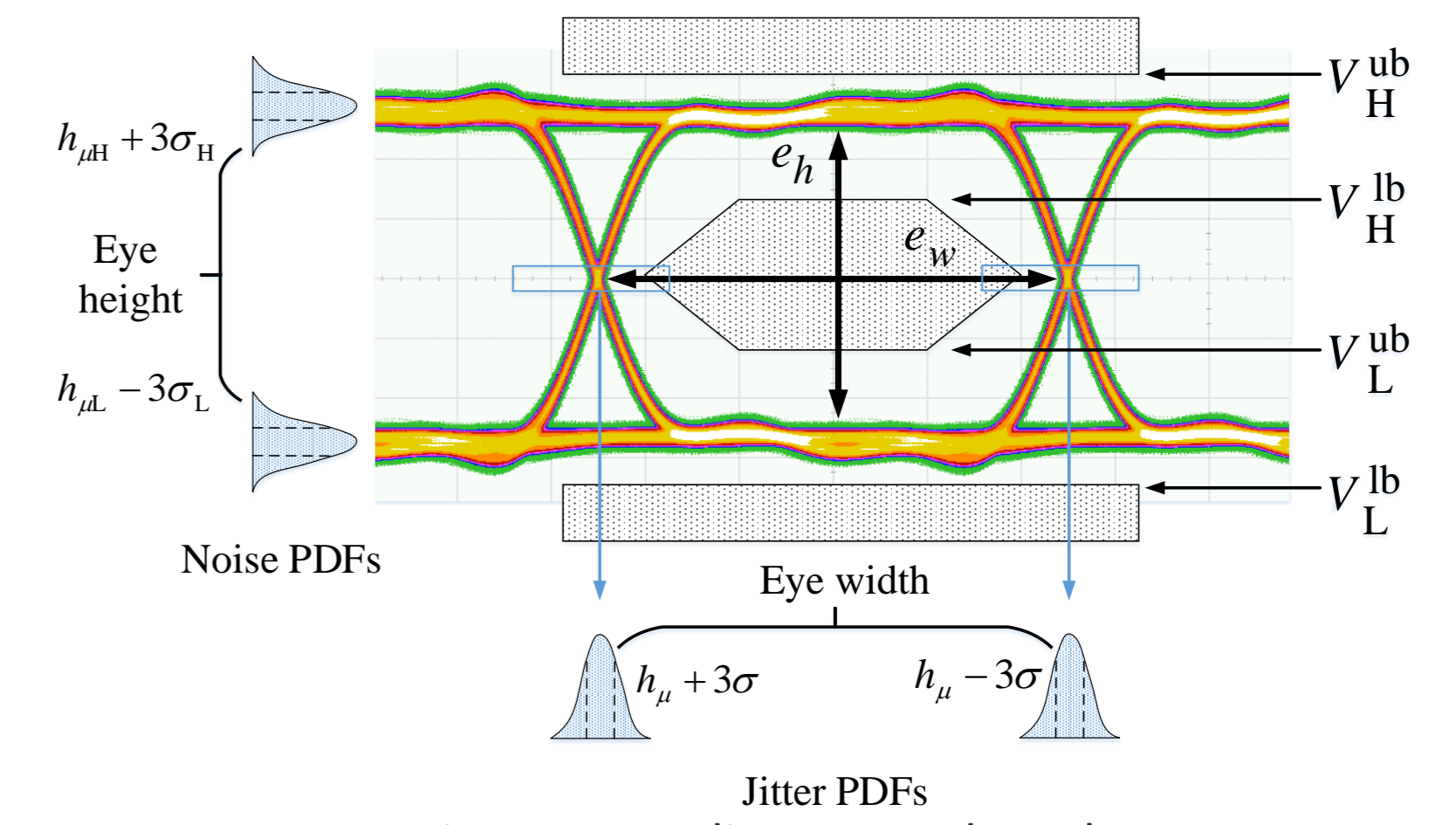

Fig. 4.1. Eye diagram and mask.

This signal integrity response is a function of the PHY tuning settings x, and the operating conditions ψ. Since we want to maximize the eye diagram, our objective function is defined as

$$U(x) = -w_1[e_h(x,\psi)] + w_2[J_T(x,\psi)] + \rho_0^l|L(x)|^2$$

where J_T is the total jitter, $L(x)$ is the eye mask limit penalty function, and r_0^l is the penalty coefficient. The e_h and J_T are scaled by weighting factors w_1, w_2. We aim at finding the optimal set of coefficients values x^* by solving $U(x)$ using the Nelder-Mead method. The results show a substantial improvement on e_h and e_w (Fig. 4.2). The efficiency was also demonstrated by a significant time reduction on validation.

e_h = 270 ticks e_w = 189 ticks V_{pp} = 1659 ticks

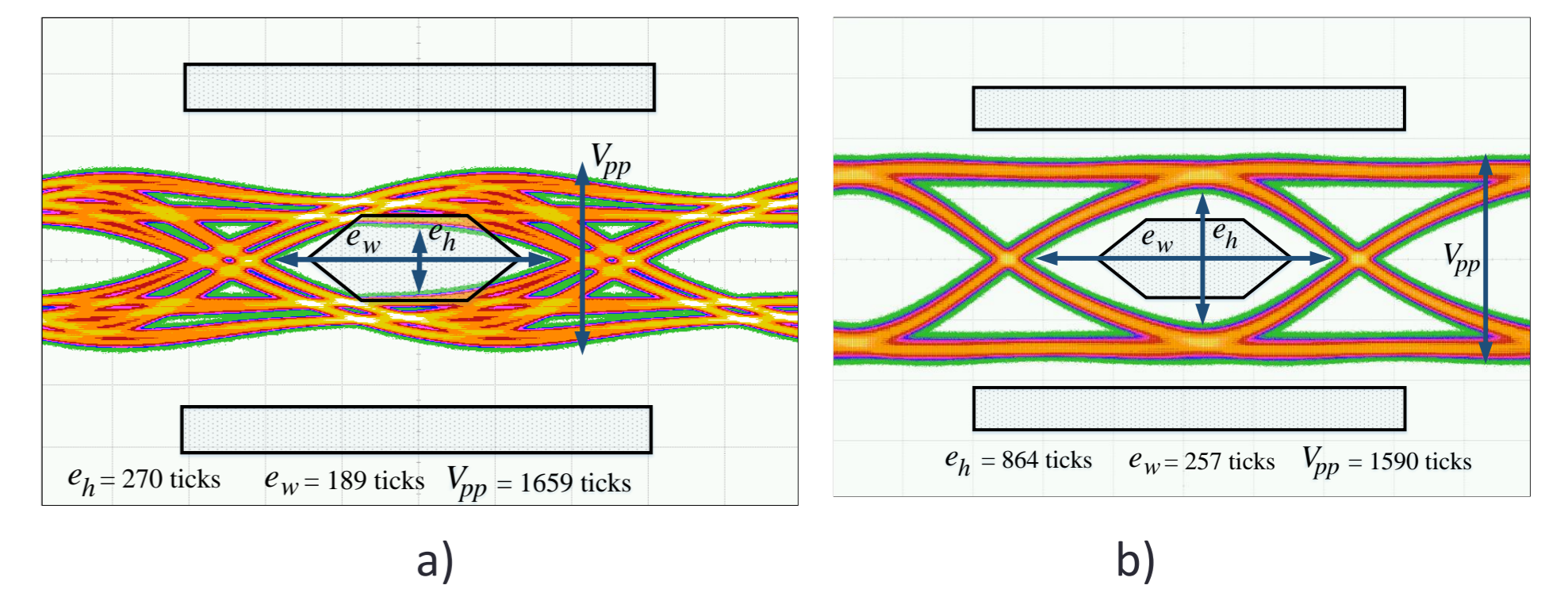e_h = 864 ticks e_w = 257 ticks V_{pp} = 1590 ticks

a)   b)

Fig. 4.2. Eye diagram over mask: a) before optimization; b) after optimization.

5. RX EQ SPACE MAPPING OPT.

While an accurate surrogate model is desirable for direct surrogate-based optimization, it can be very computationally expensive. However, by combining a good modeling technique with a suitable design of experiments (DoE) approach, an efficient surrogate model can be developed. In [5]-[6], we analyze several surrogate modeling methods and DoE techniques to find a model that approximates the system with a very reduced set of data. For future work, we are looking to use aggressive space mapping where a map between the coarse (surrogate) and fine model (real system measurements) responses is built, allowing the coarse model to perform as close as possible to the real system.

6. CONCLUSIONS

Product complexity, performance requirements and time-to-market have added big pressure on post-silicon validation. Therefore, validation teams have to continuously look for opportunities that make validation faster and cheaper. In this thesis we presented several optimization techniques based on novel objective functions to optimize the Tx and Rx analog circuitry equalizers. Our experimental results, based on a real industrial validation platform, demonstrated the efficiency of our methods, showing a substantial improvement as compared with the current industrial practice, and accelerating the typical required time for equalizers tuning.

7. SELECTED REFERENCES

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