FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Digitally-Modulated Transmitter for Wireless Communications

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MSc DISSERTATION

MESTRADO INTEGRADO EM ENGENHARIA ELETROTÉCNICA E DE COMPUTADORES

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Resumo

Transmissores digitais permitem a muito desejada integração do andar de saída de radio-frequência e da banda base digital numa única tecnologia de baixo custo. Extender esta abordagem para a generalidade dos transmissores de baixa potência é assim desejado. Além do mais, como resposta à sempre crescente demanda de troca de informação, transferências de dados eficientes e operação em diferentes standards são uma situação mandatária. Consequentemente, novos standards sem fios que permitam uma utilização mais eficiente do espectro saturado são necessários. Estes sinais geralmente forçam a operação do amplificador de potência num regime de potência médio muito longe da potência de pico. Esta condição gera a ocorrência de perda de eficiência, provocando assim a diminuição do tempo de vida útil das baterias dos dispositivos móveis. Assim sendo, esta dissertação tem como objectivo implementar um amplificador de potência digital com perda de eficiência reduzida. De modo a ultrapassar o decréscimo de eficiência observado quando o amplificador opera com modulações complexas, técnicas de aumento de eficiência serão também necessárias.

A dissertação começa por efectuar uma revisão dos últimos trabalhos relacionados com arquitecturas de transmissores digitais. Após isto, a técnica de modulação dinâmica de carga é estudada, verificando quais as vantagens e limitações das correntes implementações em CMOS. Tendo isto como suporte, a tipologia polar digital de amplificação de potência é seleccionada para ser implementada. De modo a possibilitar o desenho de um amplificador linear e eficiente, esta dissertação propõe o uso de uma tipologia de ângulo de condução reduzido baseada em fontes de corrente comutadas. Adoptando um ângulo de condução de 25%, um compromisso é assumido entre potência máxima de pico e eficiência do amplificador. Através de resultados de simulação, uma potência máxima de 17.92 dBm e uma eficiência de 43% são atingidas à frequência de operação de 2 GHz. O ponto de compressão de largura de banda de 1 dB em frequência é de aproximadamente 200 MHz, atingindo um pico de eficiência máxima de 48%. O incremento de eficiência para condição de operação de baixa potência foi conseguido através do uso de uma nova tipologia de modulação de carga dinâmica. Recorrendo a um algoritmo de optimização, operação multi-estado é realizada com uma rede de carga adaptativa. Resultados de simulação indicam um incremento de eficiência de $\times 1.2$ a $\times 1.6$ entre 3 dB e 12 dB de recúo de potência, tendo como referência um amplificador class B ideal, apresentando o mesmo uma eficiência de pico normalizada à operação com uma rede de carga com capacidades ideais. Em conclusão, os resultados obtidos durante o decurso desta dissertação demonstram a viabilidade do uso de modulação de carga dinâmica multi-nível em nós avançados de tecnologia CMOS.

Abstract

All-digital transmitters enable the constantly desired integration of both radio-frequency front ends and digital baseband in a single low-cost monolithic chip. Thus, the widespread of this well-founded approach over the generality of low-power wireless devices is appealing. Furthermore, as a response to the ever increasing user data rate transfer, efficient throughputs and multi-standard operation are required. Consequently, more demanding wireless standards are usually mandatory to allow a reasonable share between the overcrowded frequency spectrum. These signals usually present high crest factors, thereby pushing the transmitter operation away from the maximum output power, which imposes severe power losses. This, in turn, decreases the battery lifetime of portable devices. Hence, aiming the formerly evidenced challenges, this dissertation targets the development of a digital Power Amplifier solution with reduced power losses. To circumvent the typical efficiency degradation reported for complex modulated signals' amplification, an efficiency enhancement technique is also mandatory.

This dissertation begins by reviewing the latest works regarding all-digital transmitter architectures. Then, dynamic load modulation is also studied, assessing the benefits and limitations of current CMOS works. Based on that, the polar digital Power Amplifier is selected as the topology to be designed. To ease a linear and efficient digital Power Amplifier design, this dissertation proposes an approach based on reduced conduction angle switched-current sources. By adopting a 25% duty-cycle, a compromise is made between achievable peak output power and efficiency. From simulation results, maximum output power of 17.92 dBm and 43% peak efficiency are attained at 2 GHz. Moreover, the simulated point of 1 dB compression over frequency is approximately 200 MHz wide, achieving 48% of maximum efficiency. The efficiency enhancement for low-power operation was accomplished by resorting to a novel digitally amenable dynamic load modulation methodology. Relying on an optimisation algorithm, multi-level dynamic load modulation is achieved by employing a tunable matching network. Simulation results show an efficiency enhancement of $\times 1.2$ to $\times 1.6$ between 3 dB and 12 dB in power back-off over class-B operation, which was normalised to the peak performance of the static matching network under ideal capacitance elements. Hence, the results achieved during the course of this dissertation indicate the feasibility of multi-state dynamic load modulation in sub-micrometer CMOS nodes.

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First of all, I would like to convoy my sincere gratitude to my supervisor, Professor Cândido Duarte, for always being supportive and for providing an optimistic perspective about this work. His perseverance, guidance and knowledge were vital to achieve the results exposed in this dissertation. Secondly, I am also grateful to my co-supervisor, Professor José Carlos Pedro, for always putting his exceptional expertise, scientific knowledge as well as his experience to the best of this work interest.

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To my parents, I must provide an honest and sincere thank you. All of their positiveness and support through my life were the key to the person I am today. All theirs lessons and dull punishments built the person I have become. Resorting again to a serious tone, I must deeply acknowledge all their efforts to provide me an easy life and always keeping me aware of the reality around me. Their loving acts will never be forgotten.

At last, but not least, I have to write something to my bothersome girlfriend, whose major occupation was pressure me to write the acknowledgements. Hence, I shall put my best efforts onto it: All her positiveness and never ending support were crucial to both my academic and personal life evolution. Being my yang, she always fulfilled my short and long term needs by

supportive talks and never ending healthy discussions. Contrastingly with all the persons have I known in my life, she can make the best and the worst out of me. Obviously, most of the time, is the last one that arises. Steeping aside her lack of taste in occupational activities, she can sometimes be a worthy opponent in video games. However, when it comes to *nerf guns*, her lack of ability makes me roll-off on the floor laughing. That being said, I have no enough words to describe how important is her presence in my life, always keeping my head on the water's surface. I also must show my gratitude to her for being one of the main reasons of my academic success. For the years to come, I expect nothing more, also never less, from her.

Rui Filipe Pinho Gomes

"Only the unknown frightens men. But once a man has faced the unknown, that terror becomes the known"

Antoine de Saint-Exupery

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Abbreviations

ACPR	Adjacent Channel Power Ratio
AM-to-AM	Amplitude-to-Amplitude Modulation
AM-to-PM	Amplitude-to-Phase Modulation
ac	alternating current
BOM	Bill of Materials
CLM	Channel Length Modulation
CS	Common-Source
CMOS	Complementary Metal-Oxide Semiconductor
CORDIC	Coordinate Rotation for Digital Computer
CMDC	Current-Mode Class D
DCO	Digitally-Controlled Oscillator
DPD	Digital Pre-Distortion
DSP	Digital Signal Processing
DAC	Digital-to-Analog Converter
DR	Dynamic Range
DRAC	Digital-to-RF-Amplitude Converter
dc	direct current
DCR	Direct Current Resistance
DT	Duty-Cycle
DLM	Dynamic Load Modulation
EER	Envelope Elimination and Restoration
ET	Envelope Tracking
EVM	Error Vector Magnitude
FoM	Figure of Merit
GaN	Gallium Nitride
HEMT	High-Electron-Mobility Transistor
IoT	Internet-of-things
LDMOS	Laterally Diffused MOSFET
LTE	Long Term Evolution
LUT	Look-Up Table
LPF	Low-Pass Filter
M2M	Machine-to-Machine
MNT	Matching Network
MiM	Metal-Insulator-Metal
MoM	Metal-oxide-Metal
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor

OFDM	Orthogonal Frequency-Division Multiplexing
PAE	Power Added Efficiency
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PBO	Power Back-Off
PSO	Particle Swarm Optimisation
PUF	Power Utilization Factor
QAM	Quadrature Amplitude Modulation
Q	Quality factor
RF	Radio-Frequency
RF-DAC	Radio-Frequency Digital-to-Analog Converter
SOI	Silicon-on-Insulator
SDR	Software Defined Radio
SC	Switched-Capacitor
SCA	Switched-Capacitor Array
SCS	Switched-Current Sources
SRA	Switched-Resistances Array
SoC	System-on-Chip
TMNT	Tunable Matching Network
IM3	Third-order Intermodulation
PDLM	Pulse Dynamic Load Modulation
WCDMA	Wideband Code Division Multiple Access

Chapter 1

Introduction

Since the dawn of the mobile phone, wireless communication has progressively been a natural part of our daily life. From smart-phones to tablets or even smart watches, portability and connectivity are now a key feature of almost all technological devices. It is estimated that by 2020 it will exist more than 24 billion devices connected to the cloud, in which internet-of-things (IoT) gadgets will nearly consist of 70%, while traditional mobile devices will comprise merely 10 billion [1]. IoT applications encompass machine-to-machine (M2M) interfaces and software defined radio (SDR) [2], both expecting a substantial leap in consumer electronics. As an astonishing example, some of the world's biggest electronics vendors are already providing electro-domestics that allow a direct connection to the internet [3]. This phenomenal growth is only partially possible due to the reduced cost of digital signal processing (DSP) blocks, which are traditionally implemented in complementary metal-oxide semiconductor (CMOS) technology, owing to low production costs and process maturity. Additionally, CMOS enables increased system complexity and higher integration, while maintaining a relatively small chip area.

1.1 Towards All-Digital Transmitters

Seeing such an uprising in the number of internet dependent devices, the market and research community are focused on finding new ways to deploy low-cost multi-mode transmitters. In order to enable this ferocious growth, these devices must be compliant with the new wave of wireless standards, while attaining reduced size and cost. CMOS technology appears as the number one option to enable this ambitious goal. Consequently, several efforts have been invested into a complete system-on-chip (SoC) realization of fully integrated multi-mode transmitter in bulk CMOS [4]. However, the power amplifier (PA) block still remains a major roadblock due to its inherent paltry performance in CMOS [5]. In modern nanometre nodes, *traditional* PA design imposes several technical challenges that radio-frequency (RF) engineers must deal with, such as: lossy substrate, low breakdown voltage, low carrier mobility and relatively large output capacitance [6]. Hence, the PA will achieve inadequate performance, degrading the energetic efficiency of the system as a result of its dominance in total device power consumption.

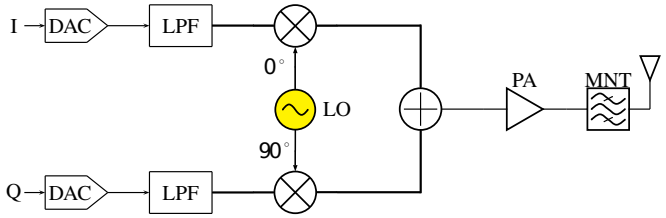


Figure 1.1: Typical analog direct conversion transmitter.

Figure 1.1 shows a typical analog direct conversion transmitter architecture. This architecture presents both in phase (I) and in quadrature (Q) paths, each one with a dedicated digital-to-analog converter (DAC) and low-pass filter (LPF) followed by a mixer. After the filtering and multiplication processes, both paths should be combined to drive the linear (*traditional*) PA. As we can see, from baseband (BB) to the antenna, the data needs to go across several blocks before reaching the PA. For instance, DACs and mixers are known for being either power hungry or quite lossy, imposing several design constraints in advanced CMOS nodes. Hence, this conventional architecture is not as amenable to be implemented in nanometre CMOS nodes due to the inherent poor performance and linearity of the traditional analog blocks [7].

As the available RF spectrum gets more and more crowded, new modulation formats, such as orthogonal frequency-division multiplexing (OFDM), aiming to achieve better spectral efficiency and higher throughputs are being widely adopted [9]. These complex modulation formats often require the transmitter to operate in large power back-off (PBO) regime. Figure 1.2 shows a typical PAPR cumulative distribution function of the OFDM IEEE 802.11a standard for wireless communications [10]. The depicted curve indicates that the probability of the output power being backed-off is considerably high, thus forcing the PA to operate in PBO during large periods of time. Conventional transmitters, as the one presented in figure 1.1, only present the highest dc to RF conversion efficiency when operating close to the peak power. As the transmitter enters in PBO, its efficiency is severely degraded, therefore, shortening the battery life-time. As a consequence, several architectures that propose efficiency enhancement in PBO were developed during the last few decades, namely Doherty, outphasing [11] and envelope tracking (ET) [12]. Due to the non-linear nature of most of these transmitters, digital signal processing techniques are either used to compensate the non-linear behaviour or to generate the desired control signals. More-

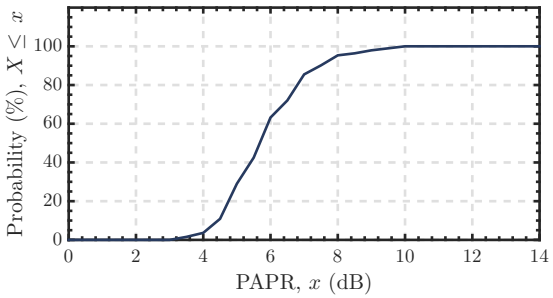


Figure 1.2: Cumulative distribution function of PAPR of OFDM IEEE 802.11a [8].

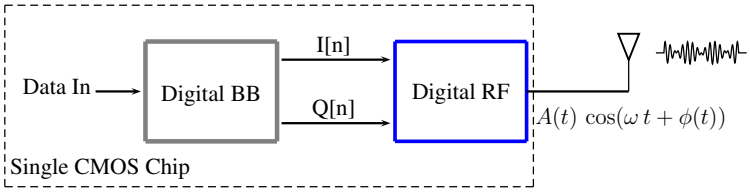


Figure 1.3: System level overview of all-digital transmitters architecture.

over, these architectures are not amenable for nanometre CMOS integration as a consequence of their analog operation nature, inasmuch as they rely on the use of bulky analog blocks. For this reason, the desire for performance enhancement of these traditional architectures is driving the scientific community onto new paradigms that intend to empower amenable nanometre CMOS RF transmitters.

CMOS active devices have been experiencing a tremendous scaling in size, while still increasing even further the current and power gain bandwidths (f_T and f_{max}) [13]. Thus, digital circuitry is more suitable to be implemented in the most advanced nodes than the bulky analog blocks. These features are enabling new research paradigms where digital integration and programmability are being used to overcome the inherent paltry performance of traditional analog blocks in the RF transceiver chain [4]. Furthermore, intensive digital approaches that enable the successful integration and merge of the PA simultaneously with traditional analog blocks in advanced CMOS nodes were reported [14]. Besides, by taking advantage of the CMOS increase in digital signal processing capabilities, numerous novel architectures that intend to overcome the well-known backoff efficiency problem are emerging. For instance, dynamic load modulation (DLM) [9, 15–18], digital outphasing [19], or digital Doherty [20, 21] are among the recent trending architectures that are suitable for large scale integration in nanometre CMOS nodes. Figure 1.3 illustrates the basic conceptual system level overview of an all-digital transmitter architecture, where both digital BB and RF front end are integrated together in a single bulk CMOS chip.

As a consequence, pushing the digital world towards the antenna is becoming more and more attractive. By exploiting these concepts is possible, as amenable to integrate baseband and RF digital-like front ends in a single chip, hence lowering the system final cost, improving the transmitter efficiency and, at the same time, allowing higher programmability. A whole new world of architectures and re-use of traditional analog concepts in digital fashion is right ahead of us. As a summary, the main advantages of utilizing these intensive RF digital approaches are:

- Suitability of integration in advanced bulk CMOS processes;
- System efficiency can be improved eliminating some traditional analog blocks (as we will see further in section 2.1);
- Allows reconfigurable multi-standard operation;
- Amenable to efficiency enhancement methods that rely on signal processing techniques.

1.2 Problem Statement

The increase in digital circuitry density is paving the way for *cost-free* signal processing capabilities in CMOS SoC. This, in turn, enables numerous untapped techniques that can resort to digital control to enhance the linearity of PBO efficient architectures [19, 22]. Low-power applications have recently been emerging [18], where the peak output power is in the range of 13 dBm to 20 dBm. Furthermore, the required modulation bandwidth is usually between 5 to 20 MHz [18, 23], which somewhat alleviates the design constraints. Thus, digital polar architectures seem to be a reasonable approach to achieve the desired operating conditions. Since long-term lifetime is an appreciable feature for portable devices, empowering a highly-efficient transmitter is a must have characteristic. Moreover, this aspect is of higher importance, considering the sparse efficiency performance of all-digital transmitters in PBO. Thus, exploring techniques whose principles rely on digital control seems a logical approach. Unfortunately, leaving all the linearisation burden to the BB may affect the system efficiency. Considering that the transmitter operates at a relatively low power, employing advanced digital pre-distortion (DPD) techniques [24, 25] may require significant BB power consumption. Additionally, the necessity of a sophisticated DPD is conflicting with multi-mode/standard operation [16].

1.2.1 Dissertation Objectives

Based on the aforementioned challenges and requirements, this dissertation targets the design of an efficient and linear all-digital transmitter. By virtue of its characteristics, digital polar architectures seem the best candidate (as we will shortly see), hence, being the focus of this implementation. Furthermore, the attained peak output power must be located between 17 dBm and 20 dBm. Resorting to a 130 nm CMOS technology, a linear and efficient polar transmitter is predicted to be presented. In order to address the PBO dilemma, an efficiency enhancement technique must also be explored. Moreover, the selected approach is expected to require little overhead in terms of both DPD and complexity. This condition is necessary to allow seamless multi-standard operation.

To summarize, this dissertation's main objectives are:

- Implementation of a polar based digital PA;
- RF peak output power in between 17 dBm and 20 dBm;
- Must present arguably good linearity;
- Good peak power efficiency;
- PBO efficient;
- Minimise the linearity degradation;

As complementary goals, i.e. sub-objectives, the targets are:

- An innovative polar digital PA shall be investigated;

- Some means will be investigated to overcome the efficiency degradation noticed in all digital PAs;

1.3 Document Outline

This dissertation is organized as follows:

Chapter 2 presents the concept of all-digital transmitters and highlights the advantages over its analog counterpart. RF-DAC and DRAC concepts are also object of discussion forasmuch as they are the heart of the RF digitalization concept. The most widely adopted all-digital transmitter architectures are also reviewed, followed by a discussion of the paramount state-of-the-art works.

Chapter 3 is dedicated to dynamic load modulation. A theoretical analysis using a class B PA is first presented in order to provide a solid background, while discussing the power matching condition that ensures device minimum power dissipation. Afterwards, the paramount works related to non-CMOS designs are reviewed along with their pros and cons. Subsequently, CMOS designs that rely on DLM are presented and the advantages of each topology are also analysed.

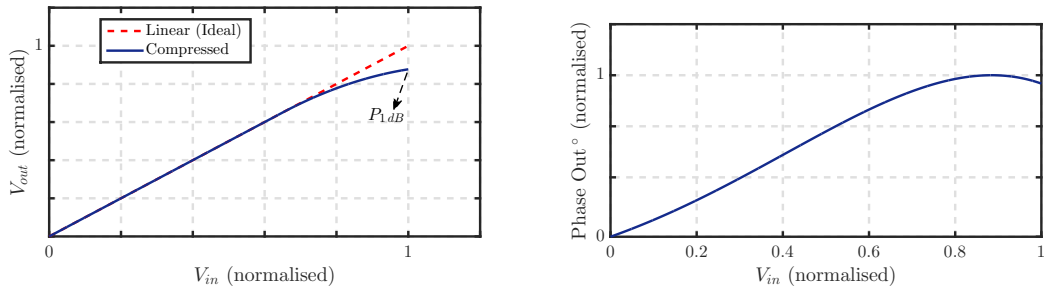
Chapter 4 proposes a digital PA to be integrated in all-digital polar transmitters. The presented architecture resorts to a novel reduced conduction angle topology to achieve a satisfactory trade-off between peak output power and peak drain efficiency. Section 4.1 presents the theoretical foundations of the proposed architecture, while section 4.2 documents its non-ideal operation as well as the distortion origins. Finally, section 4.3 presents the simulation results of the introduced DPA.

Chapter 5 addresses the PBO efficiency enhancement method. A dynamic load modulation based approach is initially discussed. To deal with the design requirements, an optimisation procedure is introduced in section 5.2. To validate the methodology, a double π matching network is used. Section 5.3 portrays the simulations results of the proposed approach.

At last, but not least, the chapter 6 draws the dissertation final conclusions. The outcome is highlighted as well as future research directions are suggested.

Chapter 2

All-Digital Transmitters



(a) (b)

Figure 2.1: The two most common forms of distortion in transmitters: AM-to-AM distortion is depicted in (a), while AM-to-PM is illustrated in (b).

Energetic awareness is the today's hot topic due to the ever growing number of electronic devices that the average person owns. Forasmuch as the efficiency of almost all smart devices is dominated by the transmitter performance, its efficiency is used as a fruitful figure of merit (FoM). Drain efficiency, η, is defined in (2.1) as the ratio of the RF output power at the fundamental frequency delivered to the load and the power drawn from the supply.

$$\eta = \frac{P_{RF_{out}}}{P_{dc}} \tag{2.1}$$

Another well-known FoM is the power-added efficiency (PAE), which takes into account the power wasted in driving the transmitter, $P_{RF_{in}}$, and is generally defined as:

$$PAE = \frac{P_{RF_{out}} - P_{RF_{in}}}{P_{dc}} \tag{2.2}$$

Figure 2.1a portrays a typical transmitter transfer curve, which depicts the evolution of the output amplitude as a function of the input signal amplitude. When the transmitter is driven with small amplitude, i.e. small signal approximation, the system can be considered approximately linear. However, as soon as the input voltage approaches the upper limit, the transfer curve starts

to compress, yielding non-linear operation. Beyond this point, the transmitter starts to generate additional harmonic content. This phenomena is know as AM-to-AM distortion [26]. To ensure proper operation when amplifying complex modulated signals, the transmitter must be backed-off from the point where the gain drops by 1 dB, also referred as one decibel compression point, $P_{1\,\mathrm{dB}}$. In linear PAs this phenomenon arises from the fact that after a certain input power level the output voltage swing exceeds the maximum allowed, thus forcing the transistor into triode region (compression) [27]. Although there exists several different forms and causes for AM-to-AM distortion, this one is the most simple and is intended to be used as an introductory example.

Another typical signal distortion source is the amplitude to phase conversion, or AM-to-PM. For instance, let us start by assuming that the system is being excited by the following signal, $f_{in}(t) = V_{in}(t) \cdot \cos(2\pi\omega_c t + \phi_{in}(t))$. The envelope of the signal reveals a dependency of $V_{in}(t)$[1], which is variable over time. For simplicity, it will be assumed that the input phase is set fixed, $\phi_{in}(t) = const$. Consequently, the only variable in the system that is changing over time is the signal amplitude, $V_{in}(t)$. If we measure the output signal and observe a time varying phase, $\phi_{out}(t)$, the signal is said to be under AM-to-PM conversion, and again, non-linear operation is attained. Voltage dependent capacitances are partially responsible for this amplitude induced phase modulation [26]. As an example, figure 2.1b illustrates an amplitude to phase conversion transfer curve. Both axes are set normalized to peak values, respectively.

Complex modulated signals employ both phase and amplitude modulation, thusly requesting highly linear transmitters. As previously seen, transmitters can (usually) only be approximated as *quasi-linear* systems in a well defined region of operation. Therefore, methods to check the signal integrity (linearity) after being conveniently amplified are needed. Since AM-to-AM and AM-to-PM are some of the responsible for spectral regrowth and signal distortion, error vector magnitude (EVM) and adjacent channel power ratio (ACPR) are useful tools to test the robustness of the signal after the transmitter [28]. As it will be promptly addressed in chapter 2.1, the previously enumerated tests also measure the influence of the output noise in the signal integrity and out-of-band noise.

2.1 RF-DAC Fundamentals

As it was previously observed, conventional analog blocks and linear PAs present sparse performance in advanced low power CMOS nodes. Hence, the development of new architectures that are amenable for digital integration is currently driving the scientific community onto new paradigms. Figure 2.2 illustrates a digital direct conversion architecture employing an RF-DAC block, as proposed in [29]. This revolutionary concept proposes the merge of the DAC and mixer in just one mixed-signal block, obviating the need for a LPF. The goal of this novel topology is to promote a unit that can effectively produce an RF phase and amplitude modulated carrier, while enabling efficient linear modulation. By employing a sigma-delta ($\Sigma\Delta$) RF-DAC based on eight current steering cells [29], a successful prototype was built to demonstrate the concept. The unit-cell

[1] Although not stated, $V_{in}(t)$ could be assumed to present a sinusoidal waveform.

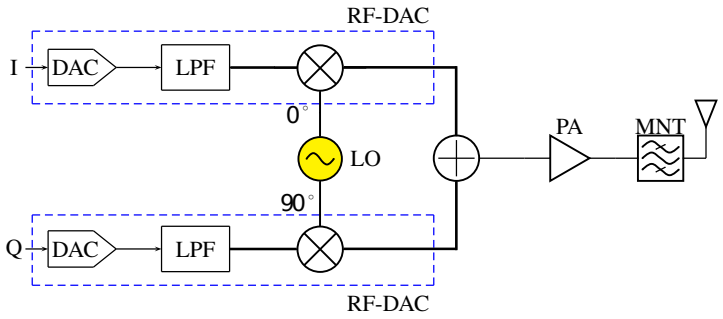


Figure 2.2: RF-DAC conceptual system level as proposed in [29].

differential-pair, as depicted in figure 2.3, is driven by a differential data path (1 bit control) that modulates the output current on and off. This way, it is possible to reconstruct an RF output signal whose amplitude is time varying and digitally controlled by the data path. Hence, this RF-DAC works as an amplitude modulator for the RF carrier signal, f_{osc}, thus also acting like a *mixer* between the digital data and the RF signal. The switching action of the data path must be timely accurate with the f_{osc} signal in order to reduce glitches. Hence, $f_s = \frac{f_{osc}}{n}$, where n is a fixed integer that ensures the required timing. Also, the phase between f_s and f_{osc} should be aligned to guarantee on-off action in the zero crossing of the oscillator signal. Suppressing the LPF enables better performance while reducing even further the number of elements in the transmitter. As a matter of fact, this novel topology has the potential to allow better noise performance and, concurrently, providing hardware reduction [29].

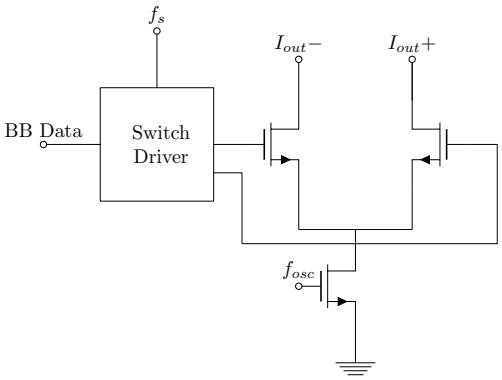


Figure 2.3: One of the RF-DAC eight unit cells based on current steering [29].

Although this concept was revolutionary, one piece of the puzzle was still missing. In [14] a modified RF-DAC architecture was proposed, including now the PA in the same block. The key difference here is that the unit cell is now comprised by a *miniaturized* PA, thus the digital-to-analog conversion is now performed by acting on the several PAs units. From now on, we will also address this topology as digital-to-RF-amplitude converter (DRAC) (i.e. power RF-DAC). The authors propose a current summation at the output, as depicted in figure 2.4. By controlling the applied digital signal in the 64 cascode transistors, V_{ctr_n}, digital amplitude modulation is

performed similar as in an RF-DAC. Considering that now the power RF-DAC is comprised by several small PA units, it allows a direct connection to the antenna, hence performing digital-to-RF up-conversion in the *power domain*. Each unit cell was implemented using cascode class A PAs,

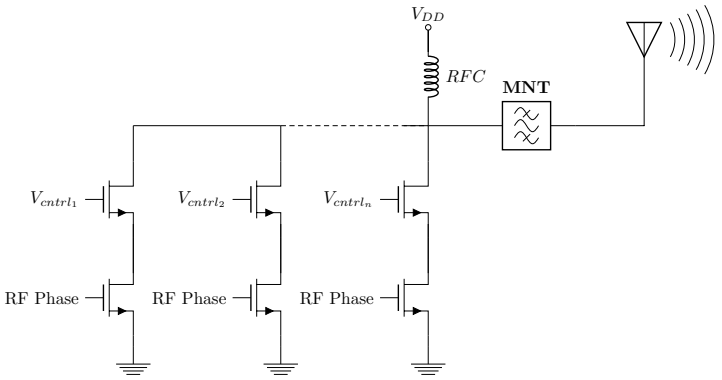


Figure 2.4: Digital polar architecture employing switched current array as proposed in [14].

thus leading to an inadequate average PAE of 6.7% while transmitting an OFDM signal. Nonetheless, a peak output power of 13.6 dBm was achieved and superior performance in comparison with analog class A PA is verified. Besides the paltry performance of the proposed architecture, this work cleared the way for the crave digitalization of the entire RF transmitter chain, demonstrating the superior performance of this digital approach over the analog counterpart due to the suppression/merge of several bulky analog blocks.

A more power efficient solution to implement a DRAC can be accomplished by switching several resistances in parallel, thus taking advantage of CMOS switching speed [4]. This allows the use of non-linear PAs classes, which are inherently more efficient [30]. Conceptually, the architecture is the same as adopted in figure 2.4. Now, instead of class A PAs, the authors use near-class E unit cells without cascode topology, therefore improving the power efficiency. However, this switching resistance topology yields highly non-linear operation, thus degrading the system linearity [6].

As it was previously stated, adopting the RF-DAC/DRAC topology obviates the need for a LPF, an advantage that, unfortunately, does not come for free. Since the LPF was responsible for the so-called reconstruction process, where the replicas at the multiples of the sampling frequency were erased, the output spectrum will now present extra undesired content around the RF frequency [31]. Furthermore, due to the zero-hold-order nature of the DRAC, the output spectrum will also present noise-floor that is dependent of the resolution of the transmitter, similar as in a DAC [31]. All this unwanted emissions will be redirected to the antenna, thusly degrading the signal quality. However, due to the presence of a bandpass filter between the all-digital transmitter and antenna, the constraints are somewhat relaxed, but not completely eliminated. Therefore, DRAC based all-digital transmitters must the carefully designed in order to ensure that EVM and ACPR wireless standards specifications are fulfilled.

A diversity of digital processing techniques are widely adopted to reinforce the performance of all-digital transmitters. In [14] discrete-time digital interpolation and up-sampling methods are

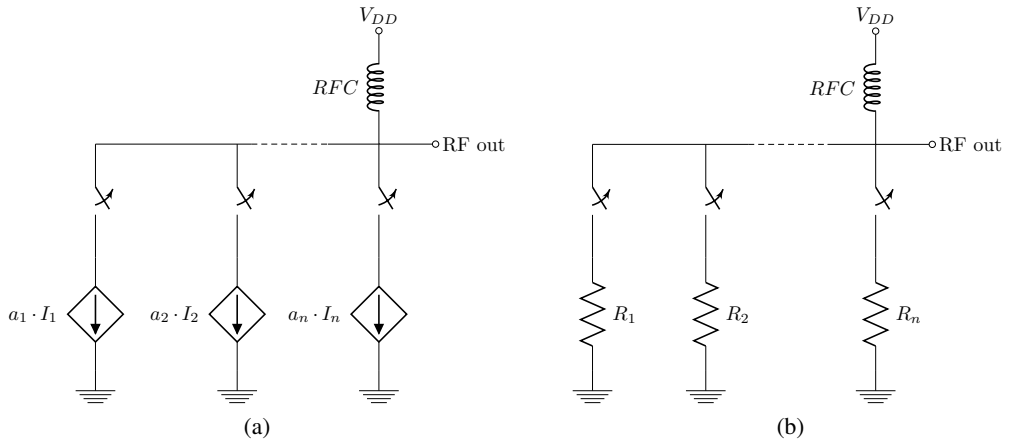


Figure 2.5: DRAC implementation as: (a) switched-current array or (b) switched-resistances as depicted in [27].

presented in order to mitigate the output spectral images generated by the DRAC. To tackle the noise floor adversity, the resolution of the DRAC must be properly selected. Generally, a trade-off between binary and unit weighted cells is used to achieve a satisfactory performance and, at the same time, low complexity [32].

To summarize, as depicted in figure 2.5, DRAC based transmitters usually rely either on switched-current sources or switched-resistances [27]. While the first one usually reconstructs the output envelope more accurately, the later achieves higher efficiency and is the most amenable for implementation in advanced CMOS nodes. As a matter of fact, none of the above is a panacea for all applications, and the right choice is influenced by several factors, such as modulation format, frequency, etc.

2.2 All-Digital Transmitters Architectures

Transmitter architectures suited for digital integration comprise the ultimate goal of CMOS SoC transmitters. Therefore, some of the most widely used digital approaches will be presented. Subsections 2.2.1 and 2.2.2 intend to present the state-of-the-art works related to digitally enhanced polar and I/Q DRACs, respectively, while the subsection 2.2.3 has the purpose of reporting all-digital outphasing architectures. The various trade-offs are also analysed, while highlighting the novel aspects of each one of the proposed works.

2.2.1 Digital Polar Transmitter

Figure 2.6 depicts a generalized digital polar architecture. Instead of the typical I and Q paths, this approach uses digital signal processing to originate separated phase, θ, and amplitude, ρ, paths. This way, the phase modulated carrier drives a DRAC, which is then responsible to perform amplitude modulation, thus, originating at the output the required complex-envelope signal, $S =$

$\rho e^{j\theta}$ [31]. A coordinate rotation digital computer (CORDIC) algorithm [33] is normally used for I/Q-to-polar conversion. This non-linear conversion, stated in (2.3) and (2.4), gives rise to bandwidth expansion, hence, degrading the system performance [31]. Regardless, this architecture shows the most promising power efficiencies, as we will promptly see.

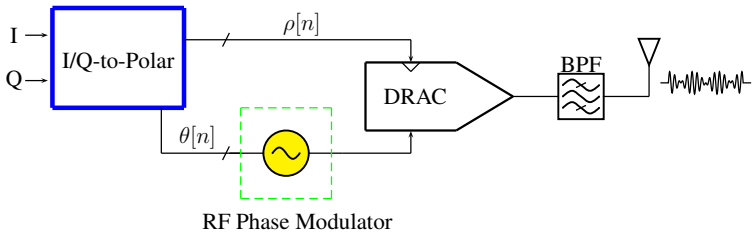


Figure 2.6: DRAC based digital polar transmitter.

$$\rho[n] = \sqrt{I^2 + Q^2} \tag{2.3}$$

$$\theta[n] = \tan^{-1}\left(\frac{Q}{I}\right) \tag{2.4}$$

In [14], a novel switched current DRAC is presented, achieving high linearity but poor efficiency. To solve this efficiency issue, various digital polar architectures were recently presented.

In [34], a switched resistance DRAC is proposed with enhanced dynamic range. Cascode topology is adopted with a bias controlled voltage that allows the extension of the output power dynamic range. Furthermore, 43% peak efficiency is achieved at 800 MHz, attaining 24.4 dBm peak output power.

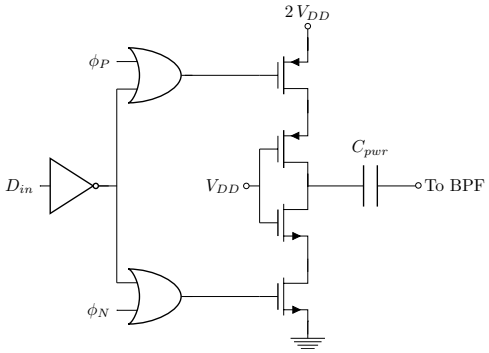


Figure 2.7: SC unit cell based on cascode Class D and MiM capacitor as proposed in [35]

Switched-capacitor (SC) DRAC [35] also appears as an appealing solution for digitally enhanced polar transmitters. Instead of using switched current/resistance arrays, the proposed solution uses a bank of binary and unitary weighted capacitors, whose charging process is accomplished using unit class D PAs acting as switches. As depicted in figure 2.7[2], each unit cell is

[2]Although proposed in the original work, the required level shifter is omitted in this figure.

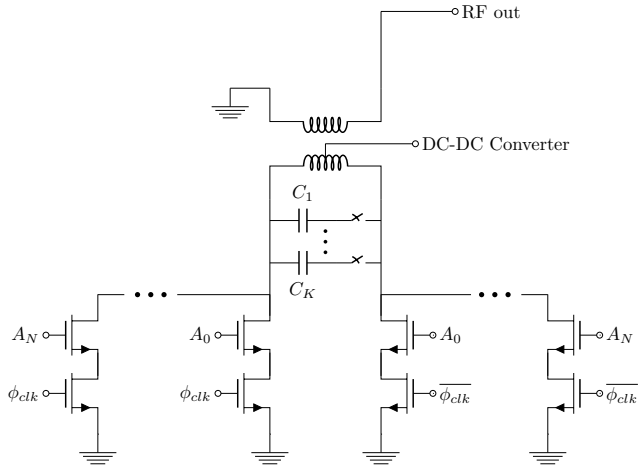


Figure 2.8: DRAC based digital polar transmitter with extended dynamic range and frequency tunable MNT as proposed in [36].

composed by a stacked class D driver and capacitor, C_{pwr}. If the unit cell is on (signal D_{in}), the class D unit is switching between ground and supply at the carrier frequency, ϕ_P/ϕ_N, otherwise it is constantly connected to one of them. Clock signals, ϕ_P and ϕ_N, are digitally controlled in order to avoid the overlapping switching process, hence improving the transmitter performance. The output power is a function of how many capacitors are being charged, therefore amplitude modulation is performed. This architecture presents an average efficiency of 27% when transmitting an OFDM 802.11g 64-QAM signal. Furthermore, on-chip matching is included, which lowers the bill of materials (BOM) of the transmitter.

Nakatani *et al.* [36] presented a digital polar transmitter based on current-mode class D (CMDC) unit cells with a digitally controlled buck converter. Figure 2.8 depicts the simplified structure of the DRAC core. Phase modulated signals, $\overline{\phi_{clk}}$ and ϕ_{clk}, are responsible for the switching action of the bottom transistors of the cascode, while the control voltage, A_N, digitally modulates the amplitude. By adopting stacked unit cells, the feed-through due to C_{GD} capacitance is reduced, which improves the polar transmitter performance. The proposed topology intends to overcome the dynamic range issue imposed by recent modulation standards. In order to do so, tri-state CMCD unit cells are employed jointly with a digitally controlled DC-DC converter. Capacitors C_1 to C_K are used in shunt with the transformer to enable frequency operation between 0.75 GHz and 2 GHz. This architecture achieves peak efficiency of 11.5% at 850 MHz, while the upper band (1.75 GHz) efficiency is near 22%. Improved PBO performance is also claimed and a remarkable output power of 29 dBm is disclosed. Ineptly, the overall transmitter efficiency is one of the lowest among the recent proposed works, which negatively affects the approach followed by the authors.

In [16], the authors proposed a polar transmitter based on a CMCD switched array PA. Instead of using a digital algorithm for phase digital code generation (i.e. CORDIC), this work presents an integrated 9-bit phase modulator. This is achieved using a fully differential RF-DAC structure and, afterwards, limiting the amplitude variation. Employing a 1-bit dynamic load modulation, this design achieves an $50-60\%$ improvement at 6 dB PBO. Complete linearisation is also presented

and the reported peak efficiency is 43% when delivering 23.3 dBm output power.

Another possible approach to implement a digital polar architecture can be accomplished using a digital approach to the conventional Doherty topology [20]. This approach uses a digital main amplifier based on CMDC that is powered on for the entire time. The peak digital amplifier is only toggled on from 0 dB to 6 dB, hence performing the active load modulation. This implementation achieves good performance between 3.10 GHz and 3.98 GHz. The measured peak efficiency is above 25% in the entire frequency spawn, while attaining an average improvement of $40-50\%$ in comparison with ideal class B operation [12]. Moreover, the obtained output power is 27.3 dBm.

In [22], the authors propose a dual supply digital Doherty. The core of the transmitter is based on the architecture proposed in [20] and the superior performance observed in this implementation is related to the usage of supply switching. By switching from V_{DD} to $V_{DD}/2$ at 12 dB PBO, the efficiency is greatly improved. This design also reports an incredible fractional bandwidth of 48%, which is claimed by the authors to be the best in class between fully integrated CMOS Doherty PAs. In order to accomplish this phenomenal fractional bandwidth, the authors propose a linearisation scheme that compensates the mismatch verified in the quadrature signals. By placing varactors at the output of the drivers, controlling their biasing introduces adjustments in the phase of the signals, hence maintaining the quadrature over the entire spawn. Furthermore, these same varactors can be used to compensate the AM-PM non-linearity of the transmitter. Peak efficiency of 42% while producing 26.7 dBm output power is reported.

2.2.2 I/Q Digital Transmitter

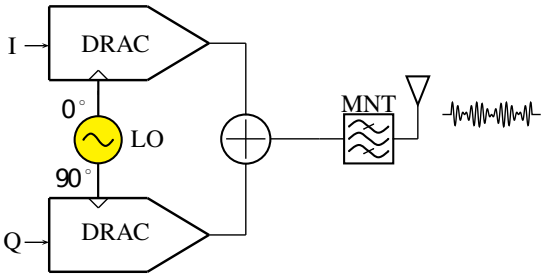


Figure 2.9: Digital I/Q transmitter DRAC based.

Although digital polar architectures present state-of-the-art efficiency results, the bandwidth expansion problem imposes a limit on the instantaneous bandwidth that the transmitter can support. Digital quadrature transmitter (I/Q) shows an auspicious position to solve this issue. Figure 2.9 presents the typical all digital I/Q transmitter. Both in-phase and in-quadrature signals are up-converted and amplified by two different DRACs. This ensures minimum signal expansion, since the out-coming signal is summed right upon amplification, forming then the desired complex modulated signal without non-linear conversion processes involved.

In [21], a four-phase I/Q Doherty digital transmitter is proposed. Each path has an own dedicated differential DRAC, being the output power combined in a main and peak transformer. The

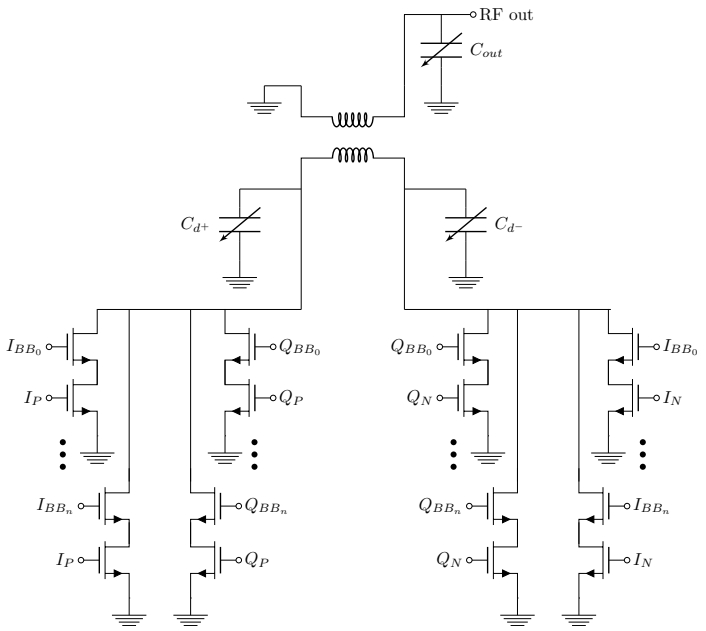


Figure 2.10: Quadrature digital transmitter with four quadrant control based on class E unit cells propsed in [37].

achieved output power is 24.8 dBm with a peak drain efficiency of 26%. Despite the peak efficiency being very poor, due to the load modulation nature of the Doherty architecture, the quadrature transmitter achieves 26% efficiency at 6 dB PBO. Furthermore, the transformer network is modulated with tuning capacitors to further enhance the efficiency below 6 dB. Even though the metrics are promising, the reported signal instantaneous bandwidth is limited to 10 MHz.

Alavi *et al.* presented in [37] a wideband 2×13-bit quadrature digital transmitter that addresses the four quadrants. The DRAC core reported in this work is illustrated in figure 2.10. Based on a novel approach employing 25% duty-cycle (DT) in each data path, i.e. I_P, I_N, Q_P and Q_N, orthogonal summation is performed, thereby reducing I/Q load interaction. Signals I_{BB} and Q_{BB} control the amplitude modulation of each baseband data path, in which a blend of binary and unitary weighted unit cells is adopted. Since the signal reconstruction is performed in quadrature, the carrier phase modulation process is no longer needed, therefore reducing the system complexity and related bandwidth extension issues reported in the polar architecture. Capacitors C_{out}, C_d^+ and C_d^- are employed here to ensure that the load interaction between each data path is minimized within the intended operation frequency range. Each DRAC unit cell is designed to work in class E PA. Unfortunately, this condition is only achieved when the transmitter is operating in peak power. The maximum output power and efficiency are 22.8 dBm and 42%, respectively. A remarkable maximum channel bandwidth of 154 MHz is reported, being the profile efficiency the downside of this approach, which is quite similar to a class B.

In [38] another I/Q quadrature digital transmitter is successfully deployed. Based on CMCD unit cells, the transmitter is able to reconstruct signals with bandwidth as high as 80 MHz, while still attaining an impressive 17% average drain efficiency. Authors also state that this transmitter

is able to amplify signals with 160 MHz while still presenting satisfactory EVM performance.

Once again, the SC topology is reported in the implementation of a DRAC based transmitter [39]. Similar as in the polar architecture [35], the core of the DRAC cell is the same. Instead of a polar architecture, the DRAC is now divided in four different sections, comprising the I^-, I^+, Q^- and Q^+, therefore, addressing all the four quadrants. Peak reported efficiency is only 21%, thus supply switch is adopted for efficiency enhancement. The maximum reported channel bandwidth is only 10 MHz. Moreover, the output power achieved is 20.5 dBm.

2.2.3 Outphasing Digital Transmitter

The outphasing concept was born in 1935 by the hand of H. Chireix [40]. The basic principle of the contemporary version of this architecture is the reconstruction of the complex signal at the output at the expense of summing two phase modulated RF signals with constant envelope, $s_1(t)$ and $s_2(t)$. Baseband signals, I and Q, are pushed into a DSP block that generates two phase modulated signals, $\theta + \Delta\phi$ and $\theta - \Delta\phi$, which are time varying. The phase information is encoded in the variable θ, similarly as in the polar architecture, while the amplitude modulation is now performed by $2\Delta\phi$ out-phase angle. This information must be used to modulate two RF carriers

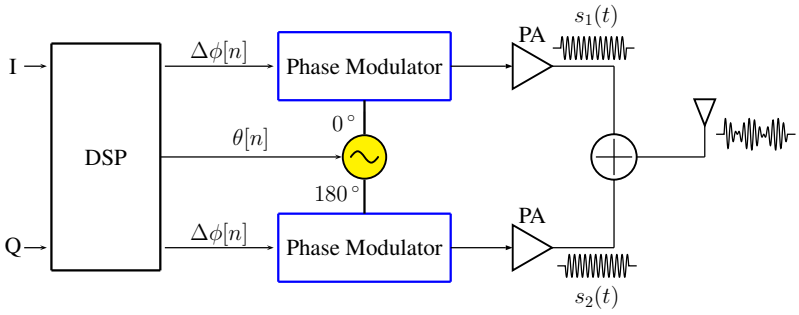


Figure 2.11: System level schematic of an all-digital outphasing system.

with constant envelope, giving origin to the desired signals $s_1(t)$ and $s_2(t)$ as in (2.5) and (2.6), respectively [11]. Each phase modulated carrier drives a separated high efficiency PA (generally switched PA), whose output power must be summed. Due to the *out-phase* action of the $2\Delta\phi$ angle between the two RF carriers, amplitude modulation is performed when both are added.

Despite of presenting an excellent theoretical efficiency performance in PBO, this architecture presents two main drawbacks: how to efficiently perform the output power summation from each PA and how to modulate the RF carriers. Since nanometre CMOS nodes present high capabilities for enhanced time resolution [4], digital processing capabilities are bringing new approaches to the phase modulators. Hence, all-digital phase modulators can be successfully accomplished. As the digital polar architecture, the outphasing also suffers from bandwidth expansion issue due to the non-linear nature of the I/Q-to-outphasing conversion process [11]. Figure 2.11 illustrates a typical digital outphasing modulator architecture. As previously stated, the DSP block generates the

digital phase signals, which now feed two different digital phase modulators. After this process, the following part is similar as in the analog version.

$$s_1(t) = 0.5V_o \cdot \sin(2\pi\omega_c t + \theta[n] + \Delta\phi[n]) \tag{2.5}$$

$$s_2(t) = -0.5V_o \cdot \sin(2\pi\omega_c t + \theta[n] - \Delta\phi[n]) \tag{2.6}$$

In [19] a digitally outphasing approach for wideband applications was successfully presented. The phase modulation is decomposed in two sequential tasks. First, the RF carrier is phase modulated ($\theta[n]$) using a digitally-controlled oscillator (DCO) [4], which is then used to feed two digital modulators that are now responsible to perform the desire additional phase modulation that enables the time varying amplitude at the output (after summation). These two digital modulators are based on delay-locked-loops, thus taking advantage of digital integration and enhanced time resolution of advanced nanometre CMOS nodes. By adopting this approach, $1-5$ GHz wideband[3] operation is attained. It is worth to note that the focus of this work is the digital phase modulator instead of the following PAs. Another reported digitally intensive outphasing modulator can be found in [41]. The peak output power is 20 dBm with 22% PAE when implemented in 32 nm CMOS process.

Although this architecture seems very promising to achieve higher levels of integration than its analog counter part, the research work with a complete all-digital outphasing transmitter is still scarce. Moreover, when compared with the quadrature or polar all-digital approaches, this implementation requires more system level blocks, which may imply more complexity and a overall lower system efficiency.

2.3 Conclusions

Resorting to the peak efficiencies attained, it is clear that the digital polar is the most strong candidate to accomplish the highest transmitter power efficiency. Moreover, they also present the best enhanced efficiencies in PBO. Also, a novel multi-band polar transmitter is reported, being able to operate between a large frequency spawn. Despite the enumerated advantages, the bandwidth expansion issue as well as the timing mismatch verified in the combination of both paths at the output are still a major roadblock for the deployment of wideband polar architectures.

Quadrature modulators present the best in class instantaneous channel bandwidth at the expense of orthogonal I/Q summing. A record 154 MHz modulated instantaneous bandwidth is reported, while other work meets the EVM requirements for 160 MHz channel bandwidth. Since nothing comes for free, this excellent *linearity* comes at the expense of lower average efficiencies than the polar counter parts.

[3] This frequency spawn is related to the frequency range that this architecture can address, opposing to the instantaneous modulated bandwidth.

All-digital outphasing appears as a promising candidate to meet in between the quadrature and polar digital transmitters. Although few research is found in literature, this architecture seems very promising to achieve higher channel bandwidths than the digital polar architecture, while still showing a better efficiency profile than digital quadrature transmitters.

Each architecture presents its pros and cons and the desired transmitter architecture must be selected in order to achieve the required specifications. Despite everything, it is clear that by relying on this new wave of digital transmitter architectures and resorting to digital signal processing techniques for linearisation, which are native of CMOS processes, pleasant performances can be attained. Table 2.1 presents a summary of the reported state-of-the-art all-digital transmitters.

Table 2.1: Comparision of most relevant all-digital transmitters architectures.

					Measurement with modulated signal				
	CMOS Tech.	**Architecture**	**Freq. (GHz)**	**Peak P_{out} (dBm)/η(%)**	**BW (MHz)**	**Signal (PAPR (dB))**	**PAE**	**DPD**	**Eff. Enhanced**
[16]-2013	65nm	Polar	2.4	23.3/43	20	64-QAM OFDM (6.5)	24.5%	**Yes**	**Discrete DLM**
[20]-2015	65nm	Polar Doherty	3.10-3.98	27/32.5	N.A.	16-QAM(N.A.)	28.8%$^{+}$	**Yes**	**Active Load Modulation**
[21]-2012	90nm	I/Q Doherty	2	24.8/26	10	Multi tone OFDM	18.8%$^{+}$	**Yes**	**Active Load Modulation**
[34]-2014	65nm	Polar	0.8	24.4/43*	N.A.	WCDMA(3.4)	35%*	**Yes**	**-**
[35]-2011	90nm	Polar	2.25	25.2/45	20	64 OFDM(6.5)	27.7%	**Yes**	**-**
[36]-2016	150nm	Polar	0.85 & 1.75^{++}	29/22	-	-	-	**-**	**ET**
[22]-2016	65nm	Polar Doherty	3.7 - 4.3	26.7/40.2	N.A.	16-QAM	28.8%$^{+}$	**Yes**	**Class G and Doherty**
[37]-2014	65nm	I/Q	1.36-2.51	22.8/42	154MHz	Multi-tone OFDM	N.A.	**Yes**	**-**
[39]-2016	65nm	I/Q	2	20.5/20**	10	64-QAM LTE(N.A.)	12.2%	**Yes**	**Class G**
[38]-2013	40nm	I/Q	2.4	24.7/37	80	256-QAM OFDM(N.A.)	17%$^{+}$	**Yes**	**-**
[41]-2012	32nm	Outphasing	2.4	26/N.A.	20	64-QAM OFDM (6.5)	22%*	**No**	**Outphasing**

N.A. - Not available
* - External matching network/balun
** - PAE
$^{+}$ - Drain efficiency
$^{++}$ - Frequency tunable matching network

Chapter 3

Dynamic Load Modulation

Several approaches that enhance the PA PBO efficiency have been proposed, such as Doherty [42], outphasing [43], envelope elimination and restoration (EER) [44] and ET [45]. Doherty and outphasing are inherently narrow-band, so RF scientists are working towards highly integrated approaches that increase the bandwidth [19, 20, 22, 41, 46]. EER and ET rely on the use of power supply modulators, which moves the problem of efficiency and complexity from the PA itself to the envelope modulator. Despite the good results achieved in this approach, circuitry overhead and complexity along with bandwidth concerns are severe [47].

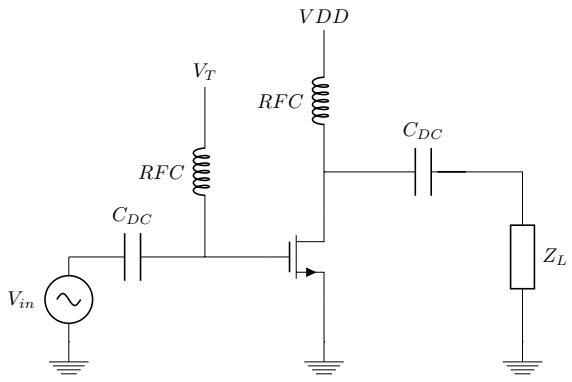


Figure 3.1: Basic schematic of class B power amplifier with idealized transistor.

3.1 Fundamentals of Dynamic Load Modulation

An alternative approach for efficiency enhancement is the use of dynamic load modulation. This technique makes use of a tunable matching network (TMNT) for proper adjustment of the PA load impedance according to the instantaneous magnitude of the signal envelope. The power amplifier schematic depicted in figure 3.1 shows us a n-channel MOSFET with the gate properly biased at

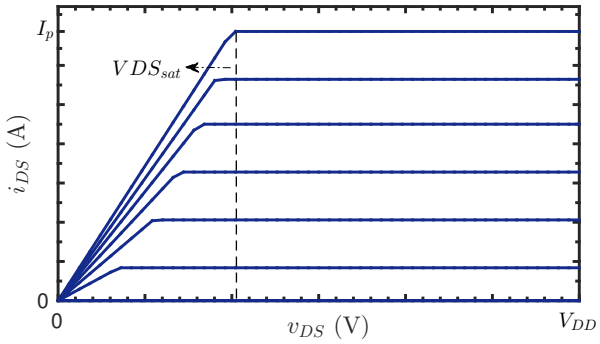


Figure 3.2: I-V characteristic of idealized n-channel MOSFET.

V_T and with a given complex drain load impedance,

$$Z_L = \begin{cases} R_L + j0\,\Omega & : f = f_1 \\ 0\,\Omega & : f \neq f_1 \end{cases} \tag{3.1}$$

For the time being, we will assume that the n-channel MOSFET behaves solely as an ideal voltage controlled current source, whose ideal I-V curve is portrayed in figure 4.7. In the interest of simplifying the following analysis, it shall be assumed that the evolution of the i_{DS} current has a linear dependency of v_{GS} (in saturation).

Since the transistor in figure 3.1 is biased at the pinch-off voltage, and for the case where $v_{GS} \leq V_{DD}$ considering sinusoidal input excitation, one can verify that the drain current has the waveform depicted in figure 3.3, which corresponds to the classical half-wave rectified sinusoid given as a function of the conduction angle, $\theta \in [0, 2\pi]$. From now on, v_{GS} will be used to represent the actual peak value of the combined dc plus ac signal magnitude of the gate to source voltage value, and i_{DS} to identify the actual peak magnitude value of the composite dc plus ac current signal. This classical class B configuration is usually designed to operate under the maximum possible (peak) power that the given MOSFET can support. Considering that the drain load impedance, Z_L, is given by (3.1), R_L must be designed according to the loadline theory [12], which leads to,

$$R_L = \frac{\Delta V_{ac}}{\Delta I_{ac}} = \frac{2 \cdot (V_{DD} - VDS_{sat})}{I_p} = \frac{2 \cdot \Delta V_{max}}{I_p} \tag{3.2}$$

where $I_p = I_{max}$ is the maximum peak drain current and $\Delta V_{max} = (V_{DD} - VDS_{sat})$ is the peak allowable output (i.e. drain) voltage swing (v_{DS}) that guarantees that the MOSFET still behaves as an ideal current source (transistor does not enter the ohmic region). One can define the highest output power at the fundamental frequency as

$$P_{out_{max}} = \frac{i_{DS_{max}} \cdot \Delta V_{max}}{4} = \frac{R_L \cdot {I_p}^2}{8} \tag{3.3}$$

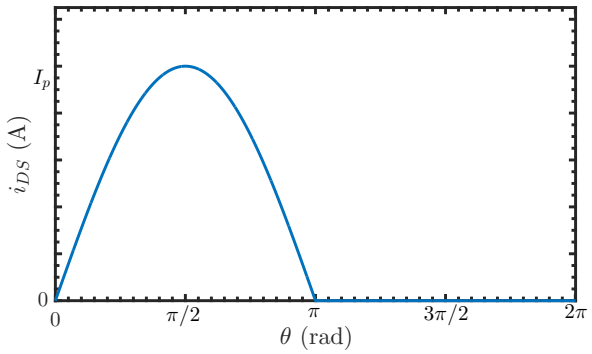


Figure 3.3: Ideal half-wave rectified sinusoid for a class B PA.

and the dc power consumption, $P_{dc_{max}}$, as

$$P_{dc_{max}} = \frac{V_{DD} \cdot i_{DS_{max}}}{\pi} = \frac{V_{DD} \cdot I_p}{\pi} \tag{3.4}$$

Given (3.3), (3.4) and recalling (2.1) we shall now determine the peak drain efficiency, η_{max}, with

$$\eta_{max} = \frac{P_{out_{max}}}{P_{dc_{max}}} = \frac{\pi R_L {I_p}^2}{8 V_{DD} I_p} = \frac{\pi}{4 V_{DD}} \times \frac{R_L I_p}{2} = \frac{\pi}{4} \times \frac{\Delta V_{max}}{V_{DD}} \tag{3.5}$$

Taking a closer look into (3.5), one can state that the class B maximum drain efficiency is defined by the ratio between the peak output voltage swing and the supply voltage; if $\Delta V_{max} \rightarrow V_{DD}$, we should get the maximum admissible drain efficiency for an ideal class B PA, given by $\eta'_{max} = \pi/4 = 78.5\%$ [12].

The former derived equation only predicts the drain efficiency when the MOSFET is operating under full power condition, where $v_{IN} = v_{GS_{max}}$ has the maximum possible amplitude given by $v_{IN} = v_{GS_{max}} = V_{DD}$. Let it now be defined that the output power is a function of the drive signal magnitude, $v_{GS} = v_{IN}$. Since the transistor under consideration reveals a drain current whose relation is linear with v_{GS}, it will be assumed from now on that the drain current can be given by[1]

$$i_{DS}(v_{GS} = v_{IN}) = \frac{I_P \cdot v_{GS}}{v_{GS_{max}}} = \frac{I_P \cdot v_{IN}}{v_{GS_{max}}}, \quad 0 \leq v_{IN} \leq V_{DD} - V_T \tag{3.6}$$

whereas the fundamental current amplitude, $I_{f_1}(v_{IN})$, can be stated as

$$I_{f_1}(v_{IN}) = \frac{I_P \cdot v_{IN}}{2 v_{GS_{max}}} \tag{3.7}$$

and the dc component, $I_{dc}(v_{IN})$, by

$$I_{dc}(v_{IN}) = \frac{i_{DS}(v_{IN})}{\pi} = \frac{I_P \cdot v_{IN}}{\pi v_{GS_{max}}} \tag{3.8}$$

The drain efficiency as a function of the current $i_{DS}(v_{IN})$ can now be easily defined as

[1] To ease the demonstration, the threshold voltage was omitted in this $i_{DS}(v_{GS})$ representation.

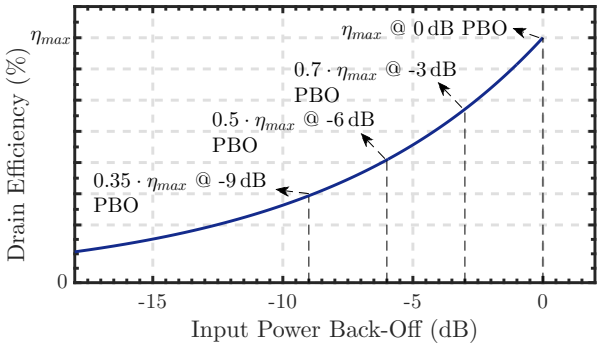


Figure 3.4: Drain efficiency evolution as a function of the normalized input power.

$$\eta(v_{IN}) = \frac{P_{out}(v_{IN})}{P_{dc}(v_{IN})} = \frac{\frac{[I_{f_1}(v_{IN})]^2 R_L}{2}}{\frac{V_{DD} I_{dc}(v_{IN})}{1}} = \frac{{I_p}^2 {v_{IN}}^2 v_{GS_{max}} R_L \pi}{4 {v_{GS_{max}}}^2 2 V_{DD} I_p v_{IN}} = \frac{\pi}{4} \times \frac{I_p v_{IN} R_L}{2 v_{GS_{max}} V_{DD}} \tag{3.9}$$

and the actual peak voltage swing, $\Delta V(v_{GS} = v_{IN})$, is now dependent of $I_{f_1}(v_{IN})$, which leads to,

$$\Delta V(v_{IN}) = \frac{I_p v_{IN} R_L}{2 v_{GS_{max}}} \tag{3.10}$$

As one can see in (3.9), the term that gives the actual voltage swing, $\Delta V(v_{GS} = v_{IN})$, can be found in the equation. Rewriting the expression in (3.9) into (3.11), it is now evident that the drain efficiency reveals a dependency on the actual output voltage swing at the drain plane.

$$\eta(v_{IN}) = \frac{\pi}{4} \times \frac{\Delta V(v_{IN})}{V_{DD}}. \tag{3.11}$$

It should be taken in consideration that the class B PA in figure 3.1 only presents the peak efficiency, η_{max}, when the input signal magnitude is $v_{IN} = V_{DD} = v_{GS_{max}}$, which yields $\eta(v_{IN} = v_{GS_{max}}) = \eta_{max}$. As it was shown before in (3.9), the efficiency reveals a linear dependency with respect to the input magnitude, v_{IN}, which implies $\eta \propto \sqrt{P_{out}(v_{IN})}$.

Defining the normalized input power as $P_{in_{norm}} = 10\log_{10}(\frac{{v_{IN}}^2}{{v_{GS_{max}}}^2})$ dB, the drain efficiency profile shall now be expressed as a function of the normalized input power, or equivalently, as a function of the input PBO. Figure 3.4 presents the situation formerly introduced. It is easily recognized that the drain efficiency is severely degraded when the input power, or equivalently, the output power are reduced. Furthermore, a simple reduction of 3 dB will lead to a efficiency degradation of 30%, whereas a reduction of $6-9$ dB will lower the efficiency by $50\%-65\%$. Due to the nature of today's wireless modulation formats, this kind of degradation in efficiency will lead to lower battery life time of mobile devices.

Inspecting once again (3.11), it is possible to see that the *cause* of the efficiency degradation is the reduction of the output voltage swing, $\Delta V(v_{IN})$. This happens due to the spanning of the loadline being maximum only when the drain current is at its peak value, lowering when v_{IN} reduces. Dynamic load modulation attempts to solve this problem by means of a *dynamic loadline*.

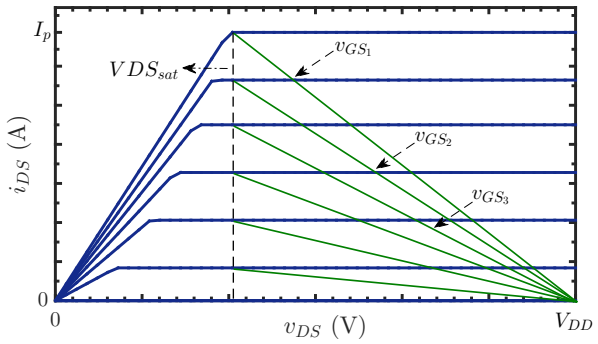


Figure 3.5: Different load ines for different v_{GS} and i_{DS} values. In this plot $v_{GS_1} > v_{GS_2} > v_{GS_3}$.

The basic goal is to maintain the output voltage swing at its maximum, ΔV_{max}, regardless of the v_{IN} value. The desired drain load impedance can now be defined as a function of the input signal, ${R_L}'(v_{IN})$, as,

$$ {R_L}'(v_{IN}) = \frac{\Delta V_{max}}{I_{f_1}(v_{IN})} = \frac{(V_{DD} - VDS_{sat}) \cdot 2 \cdot v_{GS_{max}}}{I_p \cdot v_{IN}} = R_L \times \frac{v_{GS_{max}}}{v_{IN}} \tag{3.12} $$

where R_L is the load impedance for the maximum output power condition. It is possible to notice that the evolution of the ideal drain load impedance, ${R_L}'(v_{IN})$, is inversely proportional to the input signal magnitude. For simplicity, it will be assumed that the peak output voltage swing, VDS_{sat}, is independent of v_{GS}. Figure 3.5 illustrates the trajectory that the load impedance should follow in order to maximize the output voltage swing. As the magnitude of the input signal goes lower than the maximum allowable value, $v_{GS_{max}}$, the loadline must be moved according to $i_{DS}(v_{GS} = v_{IN})$, that in the case depicted is towards higher resistance values.

Concerning the operation under dynamic load modulation, the output power is given by

$$ {P_{out}}'(v_{IN}) = \frac{[I_{f_1}(v_{IN})]^2 {R_L}'(v_{IN})}{2} \tag{3.13} $$

and bringing back (3.7) and (3.12), it can now be expressed as

$$ {P_{out}}'(v_{IN}) = \frac{{I_p}^2 R_L v_{IN}}{8 v_{GS_{max}}} = \frac{\Delta V_{max} I_p v_{IN}}{4 v_{GS_{max}}} \tag{3.14} $$

while the dc power consumption term remains the same as in (3.9). Being so, the drain efficiency can be calculated as

$$ \eta'(v_{IN}) = \frac{{P_{out}}'(v_{IN})}{P_{dc}} = \frac{\pi}{4} \times \frac{\Delta V_{max}}{V_{DD}} \tag{3.15} $$

which yields constant efficiency regardless of the input or output power levels. This result is the basic cornerstone of the dynamic load modulation technique, which intends to ensure constant *power match* over the entire output range [12]. Measuring this situation against the normal operation of the class B PA, superior efficiency in PBO is attained. In figure 3.6 it is possible to observe

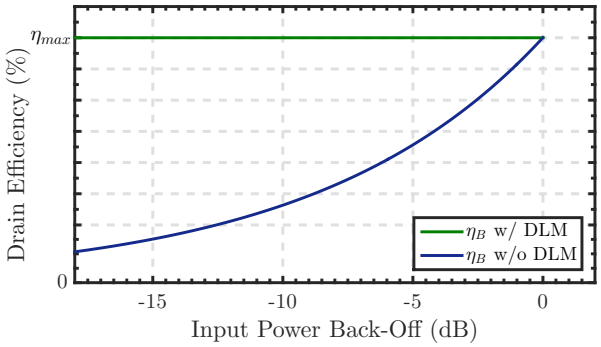


Figure 3.6: Different theoretical drain efficiency profiles when operating the class B PA with or without DLM.

the theoretical drain efficiency evolution for both situations. It is more than clear that the use of DLM greatly increases the efficiency performance in power back-off, thus reducing the device power dissipation.

One of the first downgrades that this technique for efficiency enhancement introduces in the system is related to the non-linear characteristic of the output power. Comparing the output power evolution with and without DLM (see figure 3.7), one can recognize that their evolution is not equal. Although they present the same value in peak output power, when it comes to PBO operation, they present distinct evolution. Nominal operation indicates that the output power is quadratically proportional to the input voltage, while under DLM the power delivered to the load is $\propto v_{IN}$. Hence, DLM operation offers higher output power in PBO, which is inherent due to the efficiency enhancement process (lower device power dissipation). This superior performance in PBO introduces a phenomena known as AM-to-AM non-linearity. In order to correct this distortion, simple DPD techniques, such as look-up tables (LUT), can be used [48].

Even though the deduction and analysis of DLM technique was conducted for a linear class B PA, the same analysis principle can be further applied to other linear classes, such as class AB, C or J. When it comes to non-linear classes, like E or D^{-1}, a more careful analysis should be carried,

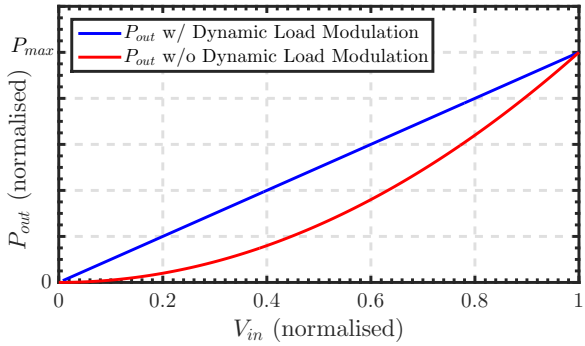


Figure 3.7: Different theoretical output power profiles when operating the class B PA with or without DLM.

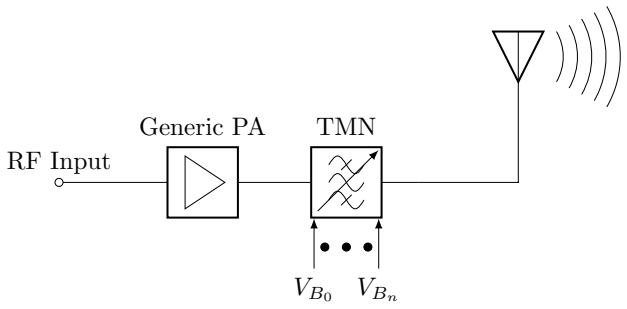


Figure 3.8: Simplified system level schematic of DLM. Input matching network and biasing circuitry omitted.

considering that some of the principles taken here are not valid. Such analysis goes beyond the scope of this dissertation.

A more realistic, yet still simplified system level schematic of this technique can be observed in figure 3.8. It consists of a generic PA followed by a TMNT, which control is performed by BB signals, V_{B_0} to V_{B_n}, each one controlling a tunable element. These elements assume numerous types, but in the general case voltage-variable capacitance elements are the chosen ones. Control signals, V_{B_0} to V_{B_n}, are generated through baseband signal processing and can be of continuous or discrete type, giving birth to continuous DLM [24, 49–58] or discrete DLM [59–62], respectively. The tunable matching network plays the key role in DLM inasmuch as it is the block that is responsible to dynamically transform the load impedance to the desired one at the drain plane. Therefore, its performance will largely dominate the final system efficiency.

3.2 Previous Work

In this section, the state-of-the-art works related to DLM will be addressed. Starting with a extensive review on non-CMOS realizations, we will then focus our attention on CMOS paramount works.

3.2.1 Non-CMOS Designs

The use of DLM as a way of linearly amplify signals with high efficiency was first addressed by Freederick H. Raab [63]. The simplified schematic of the proposed transmitter can be observed in figure 3.9. It consists of a high power MOSFET and two cascaded T networks. The first network (L_1-C_3-L_2) provides the needed inductive reactance and variable impedance at fundamental, while the second T network (L_4-C_6-L_5) is set fixed. A switched mode PA is chosen where (class E), while the RF output power is controlled by the baseband signal, V_B. The voltage-variable element in use is a pair of high voltage MOSFETs with grounded gates. It is interesting to observe that the voltage-variable instantaneous capacitance is a function of the actual RF output voltage swing plus bias voltage, V_B. Therefore, as the RF voltage swing is much faster than the baseband signal swing, it will give rise to a modulation of the actual capacitance value, thus creating additional

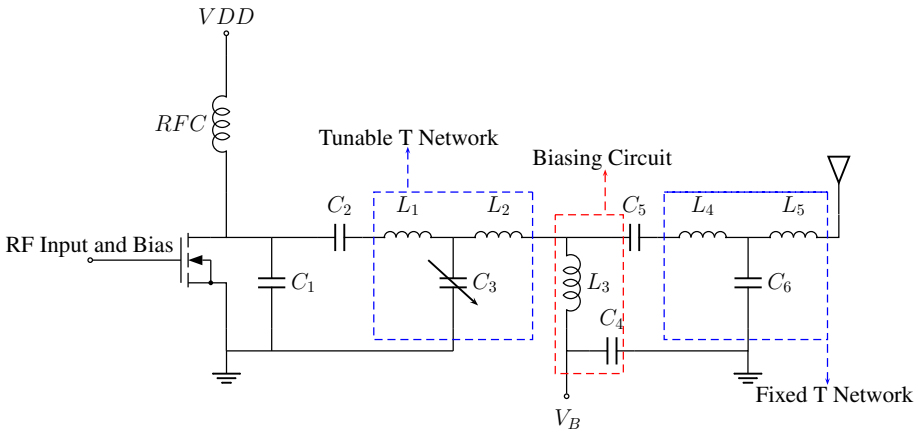


Figure 3.9: Simplified schematic of proposed dynamic load modulation architecture in [63].

harmonics. The second T network is designed to attenuate this ill-favoured harmonic content and, consequently, improving the system linearity. To promote efficient fast switching the gate is biased near threshold voltage. The resulting efficiency profile under the described operation condition leads to an efficiency enhancement when comparing with the ideal class B operation. Moreover, when transmitting signals with PAPR of 10 dB the average efficiency is more than doubled.

The first obvious advantage of this technique over ET is that we no longer need the variable supply modulator block, which enforced a bandwidth-efficiency trade-off [47]. Furthermore, the baseband control, V_B, has a negligible contribution to the dc power consumption. Notwithstanding, this approach presents some problems, namely, non-linear behaviour of varactors, signal processing for V_B generation, optimum characterization and tracking of load impedance locus and, ultimately, the need of advanced DPD techniques to correct phase and gain variation.

In order to overcome the non-linear behaviour of varactors, several works addressing this problem can be found in literature. The use of exotic technologies [64, 65] along with the adoption of anti-series topology, as depicted in 3.10, can theoretically lead to no distortion, i.e. zero third-order intermodulation products (IM3) [64].

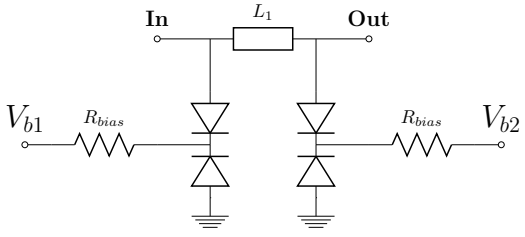


Figure 3.10: Matching network with varactors in anti-series configuration used to reduce IM3 products proposed in [64].

Another way of mitigating the capacitance variation can be accomplished if one addresses this problem using discrete DLM. The topology in discussion can be observed in figure 3.11. In this configuration, the tunable element is based on an array of binary arranged parallel capacitors in

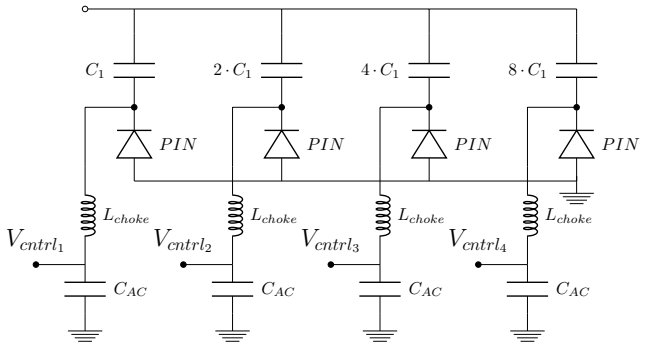


Figure 3.11: Discrete tunable element configuration proposed in [60] to increase linearity.

series with PIN diodes [60]. Instead of having tunable elements that exhibit a capacitance variation as a function of the (continuous) bias signal plus the RF output voltage swing, we now have fixed capacitance values in series with PIN diodes. When V_{cntrl_x} is active, the PIN diode is switched on and the actual capacitance is a function of how many PIN diodes are on. Using this configuration, a linear characteristic of capacitance versus control word can be achieved, while low capacitance variation is attained (higher linearity). Moreover, the bandwidth expansion issue reported in [66] for the continuous counterpart is eliminated. Unfortunately, PIN diodes present low quality factors (Q), which reduces the overall system efficiency.

Another possible approach to effectively deploy DLM in front-ends can be done by the so called *separated design*. The system schematic illustration can be seen in figure 3.12. Recalling figure 3.8, the matching network that provides the needed impedance transformation and harmonic suppression is the same. This design technique is also known as *co-design*. On the other hand, the *separated design* uses two different matching networks. While the first one is responsible to perform the desired fixed impedance transformation and harmonic suppression, the second one is only responsible for the tuning process. Hence, both matching networks can be properly tested and optimized separately. Some examples of this approach can be found in [25], [56] and [58]. Although this design technique presents more flexibility, in general it achieves lower bandwidths due to the required interconnection $50\,\Omega$ transmission line. Moreover, it generally lowers the overall efficiency due to the excessive number of elements.

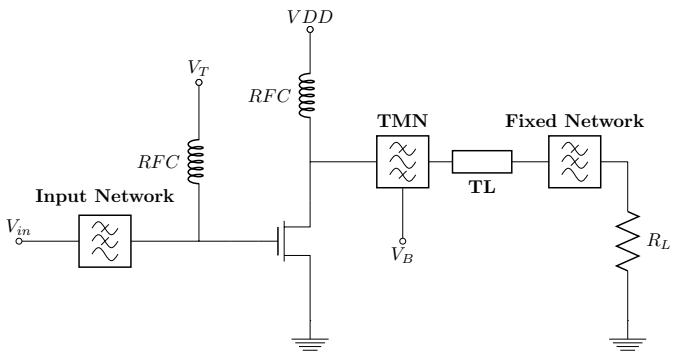


Figure 3.12: Simplified schematic of DLM with the *separated design* approach.

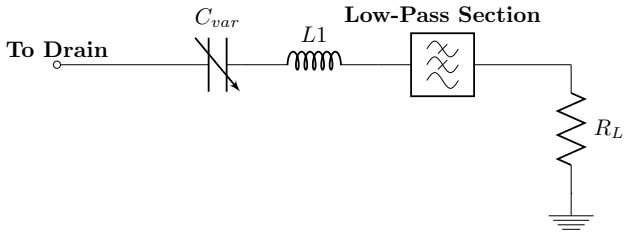


Figure 3.13: Matching network composed by a low-pass section followed by a tunable element.

Chen *et al.* presented in [52] a octave-bandwidth design based on a class B GaN HEMT. The approach in use is the *co-design*, which is responsible for the reported bandwidth extension. The matching network is depicted in 3.13. It is comprised by an inductor in series with a tunable element. The variable element is based on the anti-series varactor topology previously introduced. Following, we have a low-pass section that is responsible for harmonic suppression. Silicon varactors were preferred here due to their inherent high break-down voltage. This transmitter covers the entire frequency span between $1-1.9\,\text{GHz}$, achieving peak efficiencies between $64-70\%$. The reported efficiency at 10 dB PBO exceeds 30% over the entire frequency range. However, the transistor in use is rated for 25 W and the transmitter only achieves 10 W peak output power, which results in a fairly low transistor power capability usage.

In [24], the reported DLM design exploits the use of a single anti-series varactor element with a relatively simple matching network. The combination between lumped and discrete elements provides higher design flexibility without excessively compromising the overall efficiency. The design methodology followed by the authors was based on the usage of genetic algorithms in order to optimize the performance of the TMNT at two different central frequencies. Hence, multi-band operation is reported with excellent efficiency profile. At 685 MHz, a successful transmission of a complex modulated signal (WCDMA) with 6.5dB PAPR is achieved, with an average efficiency of 52.6%. The same signal is also successfully transmitted in the upper band (1.84 GHz) with an average efficiency of 53.6%. Nevertheless, DPD was used in order to linearise the transmitter, attaining an adjacent channel leakage ratio of $-47.5\,\text{dB}$. Moreover, the channel modulated instantaneous bandwidth is only 5 MHz, which is considerably insufficient for today's data requirements. It is also worth to state that the linearisation cost was not included in the efficiency calculations.

Class J [12] PAs are good candidates for the task as well. In [53], [67] and [68] successful implementations are reported. High fractional bandwidth is achieved with excellent efficiency profile in [68]. The reported efficiency is in excess of 40% over 18 dB PBO. In [67] a complete transmitter implementation, including linearisation, is presented. Moreover, a frequency span between $1.8-2.2\,\text{GHz}$ is attained with PAE over 40% at 6 dB PBO. When transmitting a 20 MHz modulated signal (LTE) with PAPR of 9 dB the average produced efficiency is 33%. In [55], Fager *et al.* presented a LDMOS class J design that achieves 53% of PAE while transmitting a 5 MHz modulated signal. The amplification is performed at 1 GHz and the signal presents 7 dB PAPR.

3.2.2 CMOS Designs

The never ending development of digital signal processing capabilities is a key enabling component for the deployment of intensive digital RF transmitters. Likewise, discrete dynamic load modulation with extensive backup support from baseband rises as a promising technique for next generation of mobile transceivers.

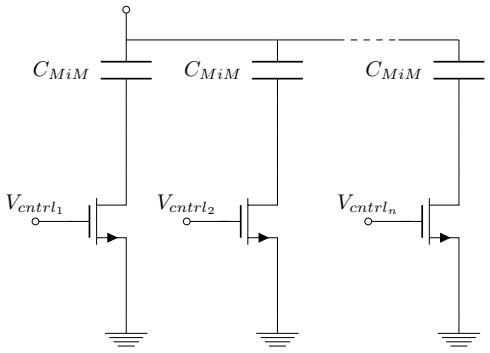


Figure 3.14: Matching network used to implement switched array capacitor in bulk CMOS proposed in [69].

CMOS based reconfigurable matching network is proposed in [69]. The variable capacitors are based on a switched array capacitor scheme as illustrated in figure 3.14. Each metal-insulator-metal (MiM) capacitor is connected to ground via a NMOS transistor. By careful layout of both NMOS transistor and MiM capacitor, quality factors higher than 50 are reported.

RF performance is greatly boosted if one chooses to use SOI-CMOS instead of bulk CMOS technology. In [15], a SOI-CMOS PA with a reconfigurable matching network is reported. A pseudo-differential power stage was selected due to the inherent required lower transformation ratio, thus reducing the transformer size and losses. The variable elements, C_S and C_P, are based on a switched capacitor array (similar as in figure 3.14). Multiple stacked NMOS transistors are employed in order to accommodate higher voltage headroom. Peak efficiency reported is in excess of 60% and the resulting efficiency improvement is between 34% and 20% for 6 dB and 10 dB PBO levels, respectively. As we can observe, superior performance in PBO is attained. Despite that, measurements with modulated signals are not reported. Furthermore, authors state that the efficiency roll-off profile is significantly degraded at lower power levels due to higher losses in TMNT.

Pulse dynamic load modulation (PDLM), reported in [18], was successfully demonstrated in a SOI-CMOS prototype. By switching between two different impedance states and controlling the time spent in each one of them, the pulse-dynamic technique improves the overall efficiency in PBO regime. Despite the excellent efficiency profile, this approach is inherently narrow-band due to the extra noise generated during the switching operation, consequently requiring a high Q band-pass filter before the antenna. In addition, the required DPD scheme is excessively complex.

The dual mode PAPR CMOS PA reported in [17] combines a closed-loop power control block that tunes both the bias of driver and power stages and the output TMNT. The differential π

network illustrated in figure 3.15 was the elected choice to implement the TMN. Although the tunable elements in use are capacitors, no schematic specification is reported. Nevertheless, in the authors approach, an extensive study of phase and gain discontinuities was conducted in order to access the impact of both in EVM test. Hence, the power control block was designed to ensure minimum distortion, eliminating the need for DPD. The peak efficiency reported is 25.5%, while attaining a $\times 2.61$ efficiency improvement at 7 dB PBO when comparing to the situation without closed-loop power control. Moreover, a successful transmission of a 5 MHz 16-QAM LTE signal is reported.

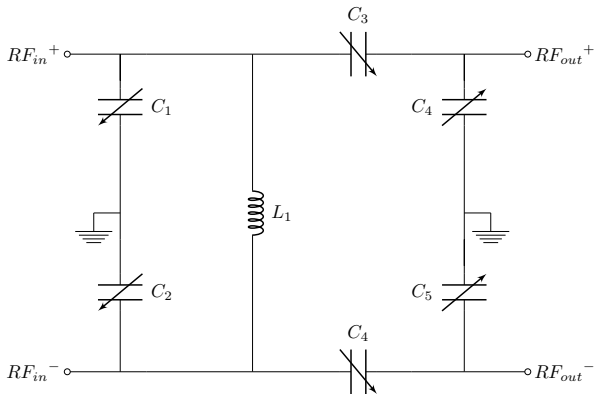


Figure 3.15: Differential matching network for discrete DLM in CMOS as proposed in [18].

In [16], it is proposed a transformer based DLM. In this approach, the load modulation is accomplished by turning on/off one of the stages of the PA, resulting in superior efficiency in PBO (60% increase at 6 dB PBO). Gain and phase discontinuities are also analysed and taken into consideration during the design. The attained overall transmitter average efficiency while transmitting a 802.11g 64-QAM 54 Mb/s signal is 19.3%.

Recently, Yin *et al.* proposed a stacked CMOS transmitter with enhanced efficiency [9] . To maximize the efficiency, the authors proposed a dynamic load tuning scheme based on an input power control block, where load is switched between two different states, thus achieving the desired improvement. PAE is improved by $\times 2$ at 5 dB PBO and the maximum achieved output power is 27 dBm while attaining 26.1% peak PAE. Moreover, a successful 40 MHz channel bandwidth transmission is reported.

3.3 Conclusions

Dynamic load modulation has been recently emerging as a promising solution to the ever increasing energetic efficiency paradigm for portable devices and base-stations. Although the most significant advances are found in more expensive technologies, such as LDMOS, GaN or SOI-CMOS, bulk CMOS based implementations can be suitable for this technique as well.

When designing a transmitter with DLM, linearity and losses are the two main adversities that one must overcome. Although several solutions can be found in literature, few of them are suitable

to be implemented in low-cost low-power CMOS transceivers. Furthermore, bulk CMOS based implementations only achieve two-level DLM operation [9, 16, 17, 35]. This opens the way for research opportunities focusing on the integration of this technique in bulk CMOS technology. Table 3.1 summarizes the previous presented state-of-the-art works related to DLM.

Table 3.1: Comparision of DLM based transmitters performance.

	Technology	PA type	Frequency (GHz)	TMN	Measurement with modulated signal			
					BW (MHz)	**PAPR (dB)**	**PAE**	**DPD**
[9]-2015	CMOS	Class-B Cascode	2.4	Discrete (SC - Two States)	40	7.6	21.3%	**No**
[16]-2013	CMOS	Class-D^{-1}	2.5	Discrete (Two States)	22	6.5	24.5% *	**Yes**
[17]-2016	CMOS	N.A.	0.7-1	Discrete (SC - Two States)	5	5	15.4%	**No**
[18]-2015	SOI-CMOS	Class-S	0.837	Discrete - PDLM	10	7.5	43.4%	**Yes**
[24]-2015	GaN HEMT	N.A.	0.685 & 1.84	Continuous (Anti-Series)	5	6.5	56.2-53.2^{++} *	**Yes**
[53]-2013	GaN HEMT	Class-J	2.14	Continuous (Anti-Series)	3.84	6.7	34% *	**Yes**
[55]-2010	LDMOS	Class-J	1	Continuous (Anti-series)	5	7	53%	**Yes**
[56]-2010	GaN HEMT	Class-F^{-1}	2.6-2.7	Continuous (LDMOS Varactor)	44^{+}	7	44%	**Yes**
[67]-2015	GaN HEMT	Class-J	1.8-2.2	Continuous (Varactor)	20	9	33%	**Yes**

N.A. - Not available
$^{++}$ - Lower and upper frequency
$^{+}$ - Extrapolated from graphic
* - Drain efficiency

Chapter 4

Proposed Digital Transmitter

As presented in the former chapters, there are several options when it comes to implement all-digital transmitters. Cartesian transmitters, employing quadrature up-conversion (I/Q), present the widest modulation bandwidth among the published works. All-digital outphasing transmitters are still in an embryonic phase owing to scarce published work. Yet, with the increased CMOS node scaling this architecture may ascend as an promising solution. Digital polar transmitters present the highest peak efficiency compared to the architectures just mentioned. Notwithstanding, the bandwidth expansion in both the amplitude and phase paths along with the required timing to sum both at the output imposes serious problems when targeting amplification of wideband signals. Furthermore, polar transmitters are usually based on switched-resistance array (SRA), which directly affects the system linearity [27]. To address both the efficiency and linearity requirements, this dissertation proposes a single-ended digital polar PA based on switched-current sources (SCS). Reduced conduction angle topology is exploit in order to reduce device power dissipation, thus increasing the system efficiency. To validate the proposed topology an implementation in 130 nm bulk CMOS with RF option is performed, aiming to achieve between 17 and 19 dBm peak output power, validated in simulation.

4.1 Switched-Current Sources: Theoretical Analysis

Figure 4.1 depicts an array of N voltage controlled current sources in series with switches, which are toggling at the RF frequency, controlled by $\theta[n]$. To be able to reconstruct the required RF output signal, $\theta[n]$ must be encoded with the phase information, while signals a_1 to a_n must deliver the required envelope data, according to the previously seen equations (2.3) and (2.4), respectively. Likewise as in a CMCD PA, the desired current waveform that we intend to impose at the transistor drain is an ideal square wave[1], thereby exploiting the advantages of increased digital (switching) capabilities of nanometre CMOS. To simplify, let us assume that the switches are ideal, i.e. they dissipate zero power both in ON or OFF states. Connected to the switched-current sources, we have a matching network followed by the equivalent antenna resistance, R_L

[1] Since the proposed topology is single ended, the current square wave is in between zero and I_p current levels.

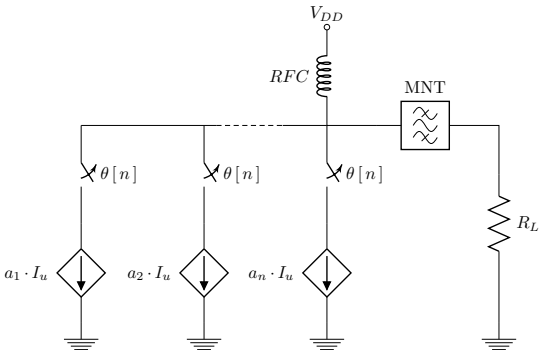


Figure 4.1: Single-ended switched-current source array.

(usually 50 Ω). Since we are only interested in delivering to the antenna power at the fundamental frequency, the matching network must present an impedance given by

$$Z_L = \begin{cases} R_{opt} + jX_{opt}\ \Omega & : f = f_1 \\ 0\ \Omega & : f \neq f_1 \end{cases} \tag{4.1}$$

hence, ensuring zero power dissipation at higher order harmonics, f_n, where $n \geq 2$. For the time being, it will be assumed that the load is solely real ($X_{opt} = 0$). As a natural consequence, the voltage waveform created at the terminals of the current sources will present sinusoidal shape, with average value of V_{DD}, similar as in a class B PA [12].

There is a vast number of options to implement the previously depicted concept. Cascode topology is one of the options, presenting its own benefits. The isolation provided between the RF input and RF output, thus avoiding the typical C_{GD} feed-trough, is a characteristic that favours the cascode based implementation. Nonetheless, the need of higher supply voltage together with increased output capacitance are some of the downsides of this topology. Given that systems targeting relatively low-power communications usually operate with low supply voltage, maintaining this condition at the transmitter stage is advantageous [70]. Therefore, the architecture proposed in this chapter resorts to a non-cascode configuration to explore the topology portrayed in figure 4.1. Reduced conduction angle is investigated as a mean to achieve a satisfactory trade-off between output power and efficiency.

Figure 4.2 illustrates the selected CMOS topology. The depicted AND gates act like digital *mixers* between the RF phase modulated carrier, $\theta[n]$, and the amplitude information, a_n. The resulting waveform is then used to drive each unit NMOS (unit PA cell). Let us start by assuming that each NMOS device acts like a perfect voltage controlled current source, only presenting dependency of the overdrive voltage, $v_{OV}(\theta[n]) = |v_{GS}(\theta[n]) - V_T|$, assuming $v_{DS} \geq 0$. This idealised behaviour can be described by the following elementary mathematical representation

$$i_{DS_u}(\theta[n]) = \begin{cases} \frac{I_u\, v_{OV}(\theta[n])}{V_{ovmax}} & : V_T \leq v_{GS}(\theta[n]) \leq V_{DD} \wedge v_{DS} \geq 0 \\ 0 & : v_{GS}(\theta[n]) < V_T \vee v_{DS} < 0 \end{cases} \tag{4.2}$$

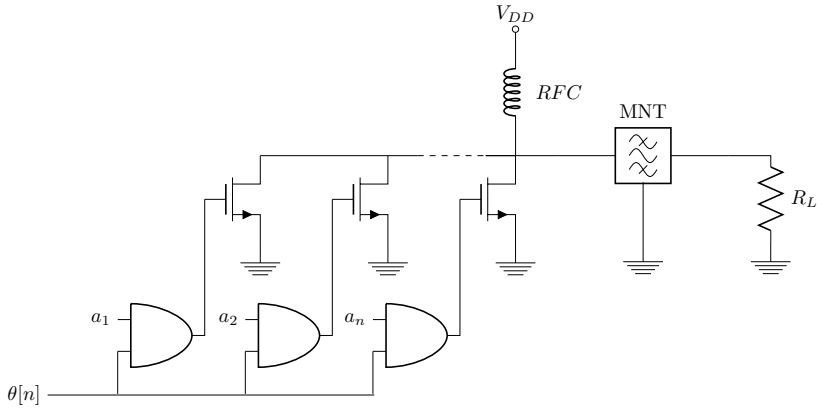


Figure 4.2: Single-ended switched-resistance array as proposed in [4].

where $V_{ov_{max}} = V_{DD} - V_T$ represents the maximum admissible overdrive voltage. Since the topology we propose operates with square waves, it will be assumed that the $v_{OV}(\theta[n])$ voltage will only present two well defined states, i.e. $v_{OV_{max}} = V_{DD} - V_T$ and $v_{OV_{min}} = V_T$, presuming $V_{DD} > V_T$. Considering now all NMOS devices in the ON state ($i_{DS_{peak}} = \sum_1^{n=N} I_u a_n = I_p$), figure 4.3 presents the idealised current and drive waveforms in the right and left graphics, respectively. Both x-axis are set normalised to radians (from 0 to 2π), which enables a more thorough representation in the present analyses. The conduction angle, θ_c, marked in both figures, illustrates the waveform duty-cycle (DT). Although traditional implementations generally assume DT= 50% ($\theta_c = \pi$), more recently, various works make use of different DT combinations, either to perform orthogonal summing [37, 21], amplitude enhanced resolution [71] or RF pulse width modulation [72]. Furthermore, as stated in the previous cited works, realising non-nominal duty-cycles in modern CMOS nodes is fairly simple and does not add excessive complexity to the transmitter. This creates an opportunity to focus our attention in non-nominal DT architectures, exploiting then the possible up-coming benefits.

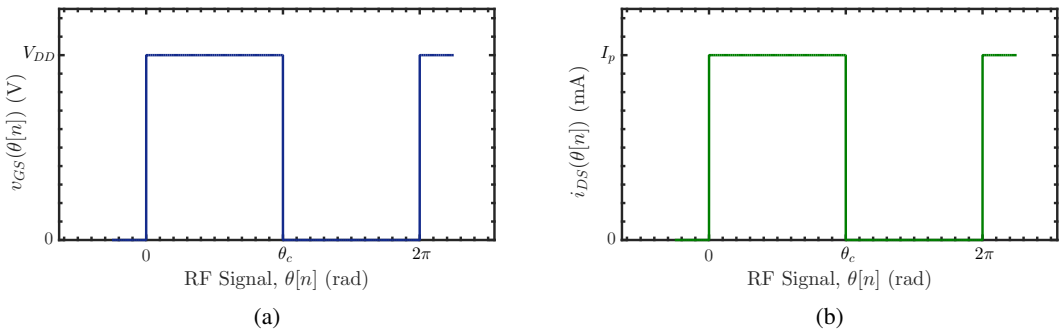


Figure 4.3: DRAC idealised waveforms: (a) $v_{GS}(\theta[n])$ voltage and (b) $i_{DS}(\theta[n])$ current.

The $i_{DS}(\theta[n])$ current can be expressed as an infinite sum of sines and co-sines terms, best known as the Fourier series, given by

$$i_{DS}(\theta[n]) = a_o + \sum_{k=1}^{\infty} a_k \cos(k\,\theta[n]) + \sum_{k=1}^{\infty} b_k \sin(k\,\theta[n]) \tag{4.3}$$

where a_0 represents the dc coefficient, while a_n and b_n represent the co-sinusoidal and sinusoidal terms. As previously affirmed, assuming that only the fundamental power, P_{rf_1}, is dissipated in the load, we can then restrict our analyses to a_0, a_1 and b_1. The dc term, a_0, is simply defined as

$$a_0 = \frac{1}{2\,\pi} \int_0^{2\,\pi} i_{DS}(\theta[n])\,\mathrm{d}\theta[n] = \frac{I_p\,\theta_c}{2\,\pi} \tag{4.4}$$

while a_1 and b_1 are described by (4.5) and (4.6), respectively.

$$a_1 = \frac{1}{\pi} \int_0^{2\,\pi} i_{DS}(\theta[n]) \cos(\theta[n])\,\mathrm{d}\theta[n] = \frac{I_p \sin(\theta_c)}{\pi} \tag{4.5}$$

$$b_1 = \frac{1}{\pi} \int_0^{2\,\pi} i_{DS}(\theta[n]) \sin(\theta[n])\,\mathrm{d}\theta[n] = \frac{I_p\,(1-\cos(\theta_c))}{\pi} \tag{4.6}$$

As one can see, all the terms of interest present dependency of the conduction angle, θ_c. Since the desired current waveform is the resulting sum of two sinusoidal terms in quadrature, we can express the resulting current amplitude as:

$$I_{f_1}(\theta_c) = \sqrt{{a_1}^2 + {b_1}^2} = \frac{I_p \sqrt{[\sin(\theta_c)]^2 + [1-\cos(\theta_c)]^2}}{\pi} \tag{4.7}$$

The peak RF output power, P_{rf_1}, can now be calculated as

$$P_{rf_1}(\theta_c) = \frac{I_{f_1}(\theta_c) \cdot \Delta V_{max}}{2} = \frac{V_{DD}\,I_p}{2\,\pi} \sqrt{[\sin(\theta_c)]^2 + [1-\cos(\theta_c)]^2} \tag{4.8}$$

where the maximum allowed voltage excursion, ΔV_{max}, limited by (4.2), equals V_{DD}. The power drawn from the supply can be expressed as

$$P_{dc}(\theta_c) = I_{dc}\,V_{DD} = \frac{I_p V_{DD}\,\theta_c}{2\,\pi} \tag{4.9}$$

whereas the peak drain efficiency, η_{peak}, is given by:

$$\eta_{peak}(\theta_c) = \frac{P_{RF_{f_1}}}{P_{dc}} = \frac{\sqrt{[\sin(\theta_c)]^2 + [1-\cos(\theta_c)]^2}}{\theta_c} \tag{4.10}$$

w Figure 4.4 illustrates the evolution of both $\eta_{peak}(\theta_c)$ and $10\log_{10}\left(\frac{P_{RF_{f_1}}}{P_{RF_{f_1}}(\theta_c=\pi)}\right)^2$. Let us focus first our attention in the nominal case, $\theta_c = \pi$, in which the DRAC conducts current for half of the RF cycle. In this scenario, the attained theoretical drain efficiency is only 63.66%, which is

[2]It is assumed that the resistive load constantly presents the necessary value to ensure the loadline theory.

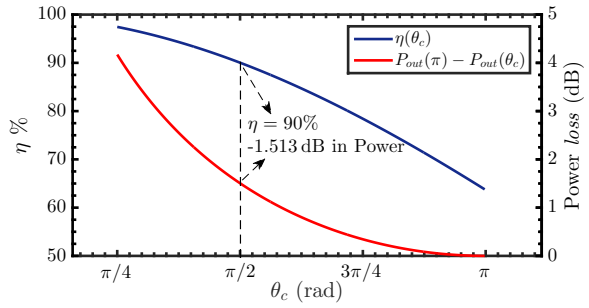


Figure 4.4: Evolution of both efficiency and output power *loss* (dB) as a function of the the conduction angle, θ_c.

fairly low even when compared with the ideal class B operation ($\eta_B = 78.5\%$). Nevertheless, the obtained power utilization factor (PUF) [12][3] goes as high as PUF($\theta_c = \pi$) $= \frac{4}{\pi} \approx 1.273$.

Recalling again figure 4.4, we observe that as the conduction angle reduces the attained efficiency increases, ideally approaching 100% as θ_c is made smaller and smaller, similarly as in a class C PA [12]. Notwithstanding, as θ_c decreases, the output power is also reduced. Therefore, this behaviour indicates a trade-off between efficiency and peak output power. When assuming $\theta_c = \pi/2$, which represents DT$=25\%$, the attained efficiency is now increased to $\eta_{peak} = 90.03\%$, while the output power is decreased by a factor of ≈ 1.5 dB. Despite the verified power loss, the efficiency enhancement makes this solution quite attractive. Moreover, the attained PUF is 0.9, which when compared with the class B PA, results only in a small decay (0.1). Besides the increment in efficiency at expanse of a small power *loss*, this conduction angle also enables a simple and low-power solution to perform the conversion from DT $= 50\%$ to DT $= 25\%$, as it will be later presented in section 4.3.3.

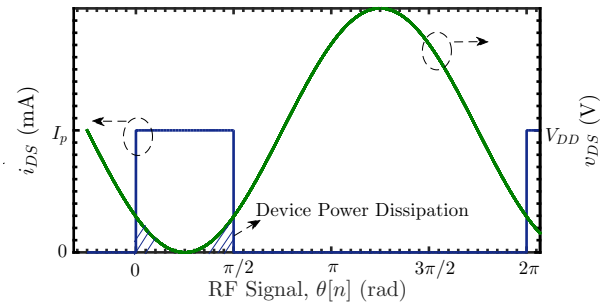


Figure 4.5: Idealised waveforms of DRAC topology: green depicts the v_{DS} voltage and blue illustrates i_{DS} current.

Under the stated conditions, the idealised current and voltage waveforms at the drain plane can be inspected in figure 4.5. The shaded area represents the power being dissipated by the NMOS transistors whenever toggled ON. This takes place due to the existent overlap between current and

[3]PUF is defined as the ratio between a PA output power and the output power that a class A would produce under the same conditions [12].

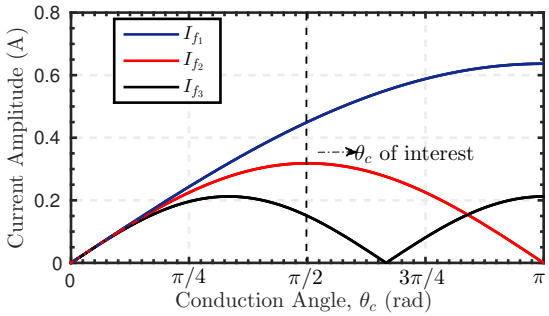


Figure 4.6: Fundamental and harmonics evolution as a function of the conduction angle, considering $I_p = 1$.

voltage at the drain plane, originating power loss that can be calculated as:

$$P_{loss} = \frac{1}{2\pi}\int_0^{2\pi} i_{DS}(\theta[n])\, v_{DS}(\theta[n])\, \mathrm{d}\theta[n] \tag{4.11}$$

This clearly indicates, in a more intuitively way, that the reduction of the conduction angle effectively decreases the power loss, improving the transmitter efficiency.

Figure 4.6 illustrates the evolution of the fundamental, second and third order harmonics as a function of the conduction angle. With the reduction of the time that NMOS transistors are active, the first and third harmonics start decreasing their magnitude, while the second one effectively increases. Contemplating now the conduction angle of interest, $\theta_c = \pi/2$, we get $I_{f_1} = 0.45$, $I_{f_2} = 0.3183$ and $I_{f_3} = 0.1502$. By comparing the magnitude of the fundamental with the two following harmonics, we can predict that their contribution to the drain voltage waveform may not be negligible under a practical MNT. Hence, when designing the DRAC MNT their contribution must not be neglected, given that their presence may cause a shift in the region of operation of the NMOS devices[4].

The coexistence of both high current and voltage in the MOSFET channel can introduce destructive phenomenons in the device structure, usually related to hot carrier effects [73]. Hot carrier injection takes place when large drain voltage coexists with high intensity currents. In the presence of high lateral electric fields, electrons can be accelerated in such a way that can cause impact ionization[5] with the silicon lattice in the drain. As a result, it induces high energetic electron/hole pairs, which may be trapped under and into the gate oxide. These trapped charges can greatly influence the device performance [73], degrading its key parameters overtime. By reducing the time that the transistor is pulling high currents (in this specific case we reduce it to half) the probability of performance degradation overtime is decreased.

[4]When the second harmonic adds in phase (or near in phase) with the fundamental, the resulting waveform will present lower valleys and higher peak values. This in turn may result in lower drain voltage, which can push the NMOS device into triode region.

[5]In semiconductors, this process usually takes place when an electron/hole presents sufficiently high kinetic energy, being able to hammer a bonded electron (in its valence band) and send it to the conduction band, creating a new electron-hole pair.

Selecting a conduction angle of 25% is, therefore, a trade-off that we propose here to achieve both high efficiency and acceptable peak output power and, simultaneously, reducing the device performance degradation.

4.2 Switched-Current Sources: Non-Ideal Analysis

In the previous analysis, some of the ideal assumptions were only taken for the sake of simplifying the reasoning. In order to materialise the impact of device non-idealities in the proposed polar DRAC architecture, multiple aspects need to be considered. Firstly, the simplified NMOS model adopted in (4.2) presents a few ideal assumptions, namely the non-existing triode region. Secondly, this type of PA (i.e. SCS) follows a non-conventional loadline, which can introduce new phenomena that may impact the device performance. This instigates the need to investigate the loadline of the proposed DRAC topology. Moreover, as it will be promptly presented in this chapter, channel-length modulation (CLM) [74] also needs to be taken into account to correctly predict the DRAC behaviour.

4.2.1 NMOS I-V Characteristic

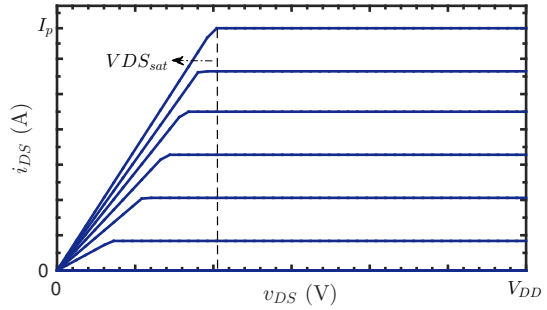


Figure 4.7: I-V characteristic of an idealized n-channel MOSFET.

The assumption taken in (4.2) to describe the drain current assumes that the NMOS device presents no triode region. As a matter of fact, CMOS devices present a soft separation of the triode and saturation regions [74], condition that will be later addressed. Figure 4.7, which was already introduced in chapter 3, illustrates a more realistic NMOS I-V curve. Aside its simplicity, this representation already includes the drain saturation voltage as a function of both v_{DS} and v_{GS}, while still neglecting CLM.

When considering $v_{GS} = V_{DD}$, the saturation voltage, VDS_{sat}, imposes the lower limit of the voltage swing. Since the former proposed topology operates the NMOS devices as current sources, the v_{DS} voltage swing must be confined inside the saturation region. This way, we guarantee that the total output current is (ideally) linearly proportional to the digital amplitude code word (ACW), enabling a linear AM-AM characteristic. Resorting to equation (4.8), we state that the output power is given by the product of the current and voltage amplitude at the fundamental frequency.

The thin-gate 1.2 V NMOS devices in use present $VDS_{sat} = 0.45\,\text{V}$, which results in a maximum allowable voltage swing of $\Delta V_{sat} = V_{DD} - VDS_{sat} = 0.75\,\text{V}$, considering $V_{DD} = 1.2\,\text{V}$. Calculating now the maximum achievable efficiency leads us to:

$$\eta_{SAT} = \eta_{peak} \times \frac{\Delta V_{sat}}{V_{DD}} \approx 56.27\% \tag{4.12}$$

There is a dramatic reduction in efficiency caused by the non-zero saturation voltage. To achieve higher efficiency the drain voltage swing must be increased, either by using higher supply voltage or allowing the transistor to enter the triode region. While enabling the transistor to work as a resistance results in higher efficiency, it also impairs the DRAC linearity. On other hand, increasing the supply voltage results in higher efficiency. However, this approach presents a major drawback, since NMOS devices are generally regarded as being able to tolerate dc voltage stresses as high as twice the nominal supply voltage [75]. The foundry information states that the typical maximum voltage for the n+ diffusions and gate oxide are 2.7 V and 2.4 V, respectively. Thus, considering that the maximum v_{DS} voltage is limited by $v_{DS_{max}} = 2.4\,\text{V}$, one can calculate supply voltage by:

$$\begin{aligned} v_{DS_{max}} \leq 2.4\,\text{V} &<=> V_{DD} + V_{DD} - V_{DS_{sat}} \leq 2.4 \\ &<=> V_{DD} \leq \frac{2.4 + V_{DS_{sat}}}{2} = 1.425\,\text{V} \rightarrow 1.4\,\text{V} \end{aligned} \tag{4.13}$$

Hence, considering $V_{DD} = 1.4\,\text{V}$ and resorting to (4.12), we are now able to compute the new maximum theoretical efficiency, given by

$$\eta_{SAT} = \eta_{peak} \times \frac{\Delta V_{sat}}{V_{DD}} = \eta_{peak} \times \frac{1.4 - 0.45}{1.4} \approx 61\% \tag{4.14}$$

which represents an increase of 4.8% when compared against the nominal case. Additionally, numerous published works state that even when NMOS transistors are operated with RF voltage stress higher than the nominal maximum dc voltages, the devices present no evident performance degradation [9, 37, 75]. Therefore, the proposed digital transmitter will employ a supply voltage of $V_{DD} = 1.4\,\text{V}$ at the DRAC core.

4.2.2 DRAC Loadline

The loadline of a given PA can be seen as the I-V path that the transistor follows under the influence of v_{GS}, v_{DS} and Z_L. The drain complex load impedance and the harmonic component of the v_{DS} voltage can present immense influence in the DRAC behaviour. Nonetheless, for the time being, we will still assume the same load conditions as before. Let us first consider the most rudimentary case, where the drain load impedance is assumed to be purely real. Assuming now that our MOSFET presents $v_{DS_{sat}} > 0$, the drain current and voltage waveforms are depicted in figure 4.8. Voltage value V_1 and V_2 mark the *enter* and *exit* conduction points, respectively, and in the presence of resistive load $V_1 = V_2$. Figure 4.9 illustrates the loadline path that the transistor follows under the considered circumstances. Assuming that v_{GS} only presents two different values,

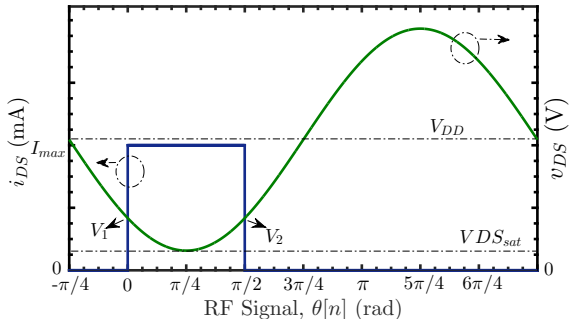


Figure 4.8: Drain current and voltage waveform under resistive load.

and considering zero transition time between each state, the loadline is fairly simple. As long as the resistive load does not exceed the value given by the (4.15), one can assume that the DRAC always operates between cut-off and saturation regions, avoiding the unwanted triode operation. As stated before, this condition ideally ensures a highly linear AM-AM characteristic.

$$R_{opt} = \frac{V_{DD} - VDS_{sat}}{I_{f_1}} = \frac{V_{DD} - VDS_{sat}}{0.45 \cdot I_p} \tag{4.15}$$

Let us now assume that the drain load is not purely real. This condition can either be consequence of the output NMOS capacitance (C_{DS}) or imperfect MNT termination. Under this circumstances, the drain impedance, Z_L, is expressed by

$$Z_L = R_d + jX_d \tag{4.16}$$

where X_d can be either inductive or capacitive, giving rise to a time difference between i_{DS} and v_{DS}. To hold the transistor in the saturation region, the magnitude of v_{DS} must not exceed $V_{DD} - VDS_{sat}$. Hence, the $|v_{DS}|$ can be expressed as

$$|V_{ds}| = |R_d I_{f_1} + jX_d I_{f_1}| = I_{f_1} \sqrt{{R_d}^2 + {X_d}^2} \tag{4.17}$$

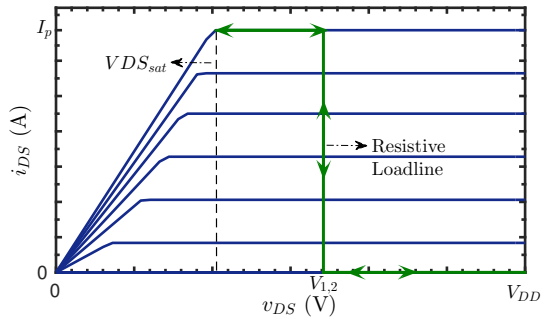


Figure 4.9: Loadline under resistive drain load.

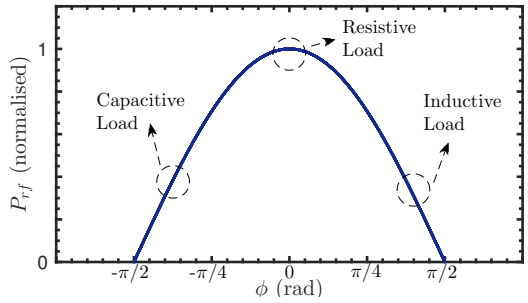


Figure 4.10: Output power as a function of the ratio between resistive and reactive load components.[6]

while the phase difference is given by:

$$\phi = \angle V_{ds} = \arctan\left(\frac{X_d}{R_d}\right) \tag{4.18}$$

By inspecting (4.17), $|v_{DS}|$ is function of both the real and imaginary part. Thus, to keep $|v_{DS}|$ below the maximum allowed voltage swing, the real part must decrease its value whenever the imaginary component assumes a non-zero value.

Considering the simplified I-V curve shown before, this situation imposes a modified loadline. To quantify the impact of such condition, let us recall the definition of power dissipated in the NMOS device (4.11), which results in:

$$P_{diss} = \frac{1}{2\pi}\int_0^{2\pi} i_{DS}(\theta[n])\, v_{DS}(\theta[n])\, \mathrm{d}\theta[n] = \frac{1}{2\pi}\int_0^{\pi/2} I_p\,(V_{DD} - v_{ds}(\theta[n]))\, \mathrm{d}\theta[n] = P_{dc} - P_{rf} \tag{4.19}$$

Due to the conservation of the energy, the power lost in the transistor, P_{diss}, is simply the difference between the power drawn from the supply, P_{dc}, and the power delivered to the load, $P_{rf} = P_{out}$[7]. The dc power is independent of the angle ϕ, while the RF output power can be calculated as[8]

$$P_{rf} = \frac{1}{2\pi}\int_0^{\pi/2} {I_p}^2\, |Z_L|\, [\sqrt{{a_1}^2 + {b_1}^2}\cos(\theta[n] - \pi/4 + \phi)]\, \mathrm{d}\theta[n] \tag{4.20}$$

and given that for $\theta_c = \pi/2$ coefficients $a_1 = b_1 = 1/\pi$, we can solve the integral and obtain

$$P_{rf} = \frac{|Z_d|\, {I_p}^2 \sqrt{(1/\pi)^2 + (1/\pi)^2}}{2\pi}\big(\sin(\pi/2 - \pi/4 + \phi) - \sin(-\pi/4 + \phi)\big) \tag{4.21}$$

where ϕ is given by (4.18) and $|Z_d| = \sqrt{{R_d}^2 + {X_d}^2}$. Figure 4.10 depicts the evolution of the RF output power normalised to its peak value as a function of the phase ϕ, while keeping the $|Z_d|$

[6] The magnitude of the drain complex load impedance, Z_d, is assumed to be kept constant, only varying the ratio between the resistive and reactive components (relation given by ϕ).

[7] It is assumed that all the other elements, such as the matching network, are ideal, i.e. dissipate zero power.

[8] The drain current is given by the sum of $a_1\cos(\theta) + b_1\sin(\theta)$, which can also be represented as $\sqrt{{a_1}^2 + {b_1}^2}\cos(\theta - \tan^{-1}(b_1/a_1))$.

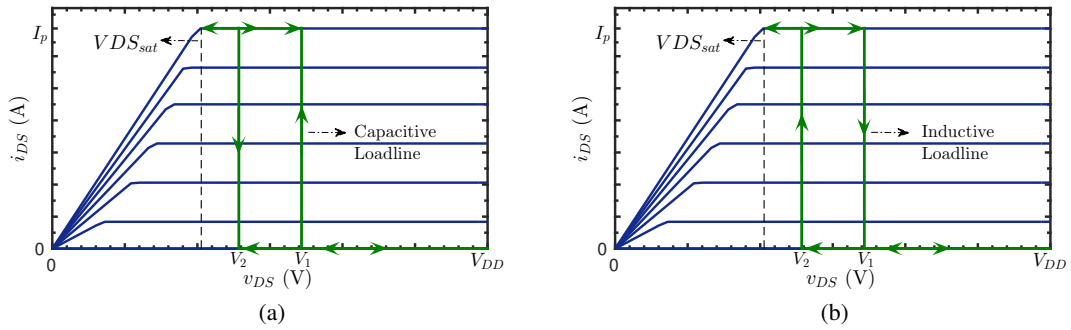


Figure 4.11: Reduced conduction angle DRAC loadlines: (a) under lightly capacitive load and (b) under lightly inductive load.

constant. As expected, whenever the real part is lowered and the voltage swing is maintained, $P_{out} = P_{rf}$ is decreased. Not surprisingly, the maximum occurs when the load is purely real, i.e. $\phi = 0$, while both minimums take place when $\phi = \pm\pi/2$. Figure 4.11 illustrates the loadline paths under slightly capacitive and inductive loads in the left side and right side, respectively.

4.2.3 DRAC Loadline under CLM and Soft-V_{knee} Voltage

The former analyses were conducted under the assumption of infinite output resistance[9], $r_o = +\infty$, and hard triode-saturation transition. Unfortunately, modern CMOS nodes present CLM, where the v_{DS} voltage actually contributes with non-negligible influence on the drain current. Moreover, the separation between triode and saturation regions is not well-defined, being particularly smooth in short channel devices. Hence, to access the complete impact of the aforementioned effects in the proposed DRAC a detailed investigation must be done. Although in [76] it is presented a simplified analysis and expression to quantify CLM, we will present here a more thorough approach that will allow us to materialise and separate both CLM and soft saturation-triode transition impact. Furthermore, this approach can also be extended to other DPAs architectures as well.

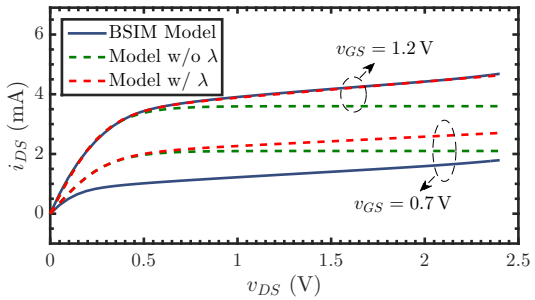


Figure 4.12: Fitting of the proposed model to to describe BSIM $i_{DS}(v_{DS})$ behaviour.

[9]Channel length modulation effect is represented in the equivalent MOSFET small-signal model as a resistance, r_o, that appears in parallel with the voltage controlled current source.

Considering that the drain to source current of a given NMOS can be expressed by

$$i_{DS}(v_{GS}, v_{DS}) = k_c \cdot f_1(v_{GS}) \cdot f_2(v_{DS}) \tag{4.22}$$

where $f_1(v_{GS})$ and $f_2(v_{DS})$ model the gate to source and drain to source voltage dependence of the i_{DS} current, respectively. It will be assumed that the $i_{DS}(v_{GS})$ dependency is linear and it is given by

$$f_1(v_{GS}) = \begin{cases} 0 & : v_{GS} < V_T \\ \frac{v_{GS}-V_T}{V_{ov_{max}}} & : V_T \leq v_{GS} \leq v_{GS_{max}} \\ 1 & : v_{GS} \geq v_{GS_{max}} \end{cases} \tag{4.23}$$

where $v_{GS_{max}}$ is the supply voltage, V_{DD}, and $V_{ov_{max}} = V_{DD} - V_T$. The i_{DS} dependence of v_{DS} is represented as:

$$f_2(v_{DS}) = \begin{cases} 0 & : v_{DS} \leq 0 \\ \tanh(\alpha\, v_{DS}) \cdot (1 + \lambda\, v_{DS}) & : v_{DS} \geq 0 \end{cases} \tag{4.24}$$

The coefficient λ models the CLM effect, while $\alpha \approx \frac{1}{VDS_{sat}}$ controls the knee voltage. Figure 4.12 depicts in blue, the simulated $i_{DS}(v_{GS} = 1.2\,\text{V}, v_{DS})$ curve for a 1.2 V RF modelled NMOS device with $L = 120\,\text{nm}$ and $W_T = 6.6\,\mu\text{m}$. The red dashed line portrays the fitted model that we will use from now on to model the CLM effect, while the green dashed curve depicts the fitted curve under no CLM effect. The fitting process was conducted using MATLAB® fitting toolbox `lsqcurvefit` routine, considering $v_{GS} = 1.2\,\text{V}$. As it is possible to observe, assuming that both VDS_{sat} is independent of v_{GS} and $i_{DS}(v_{GS})$ presents a linear relation is not valid. However, given the nature of the proposed DRAC loadline, this model reveals to provide reasonable accuracy under negligible $v_{GS}(\theta[n])$ rise/fall time. The obtained parameters for each case can be observed in table 4.1. It is noteworthy that when considering $\lambda = 0$, α and k parameters were adjusted in order to guarantee the same saturated current level.

Table 4.1: Parameters obtained using MATLAB® non-linear curve fitting.

	With CLM	**Without CLM**
k_c	3.36 m	3.60 m
λ	0.158	0
α	3.6	3.45

Let us concentrate now on figure 4.13. Left-sided graphic illustrates the loadline under high drain to source voltage swing, while the graphic in the right depicts the loadline path for low v_{DS}[10]. Seeing that the current amplitude at the fundamental frequency, I_{f_1}, is dependent of $i_{DS}(\theta[n])$ integral (recall (4.7)), it seems fair to assume that the situation depicted in the right side, i.e. under

[10]For the time being, the peak current was assumed to be the same for both cases. Nonetheless, as it will be later addressed, this situation usually occurs under different current values.

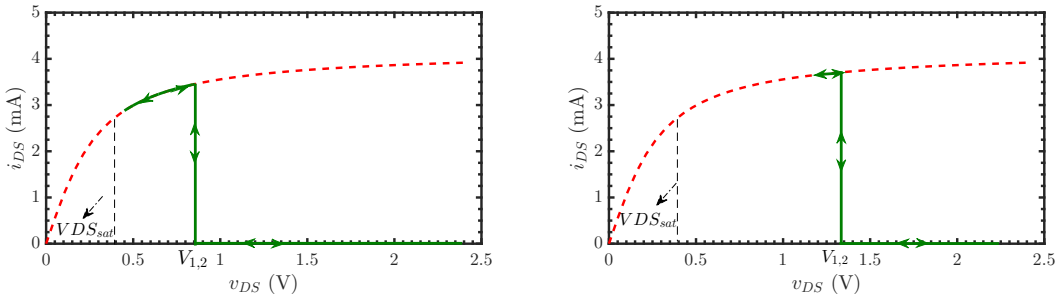


Figure 4.13: Resistive loadline: (a) full v_{DS} voltage swing (b) low v_{DS} voltage swing.

low v_{DS} voltage swing, will result in higher I_{f_1}/ACW than the situation shown in the left graphic. Even though these two situations generally occur for different ACW values, they augment the need to take into account the CLM as well as the triode-saturation soft transition effects in the AM-AM performance. Recalling (4.5) and (4.6), we must now include the formerly introduced dependence of v_{DS}, resulting in equations (4.25) and (4.26), respectively. One can also write (4.25) and (4.26) into (4.27) for a more compact representation.

$$a_1 = \frac{1}{\pi}\int_0^{2\pi} k_c \cdot f_1(v_{GS}(\theta[n])) \cdot f_2(v_{DS}(\theta[n])) \cdot \cos(\theta[n])\,\mathrm{d}\theta[n] \tag{4.25}$$

$$b_1 = \frac{1}{\pi}\int_0^{2\pi} k_c \cdot f_1(v_{GS}(\theta[n])) \cdot f_2(v_{DS}(\theta[n])) \cdot \sin(\theta[n])\,\mathrm{d}\theta[n] \tag{4.26}$$

$$I_{f_1} = \frac{1}{\pi}\int_0^{2\pi} k_c \cdot f_1(v_{GS}(\theta[n])) \cdot f_2(v_{DS}(\theta[n]))\,\cos(\theta - \pi/4)\,\mathrm{d}\theta[n] \tag{4.27}$$

However, v_{DS} itself shows dependency of the fundamental current, I_{f_1}, yielding

$$v_{DS}(\theta[n]) = V_{DD} - R_L \cdot I_{f_1} \cdot \cos(\theta[n] - \arctan(b_1/a_1)) \tag{4.28}$$

under the assumption of purely real drain impedance. Using equation (4.28) in (4.27) culminates in a non-linear differential equation. In order to solve it, numerical integration can be used, existing a wide variety of methods, such as Newton-Raphson, secant or bisection [77]. MATLAB® routine `fzero`[11] will be used to solve the differential equation.

The model and equations previously delineated will be applied in the following section. A comparison with the BSIM results is expected, assessing then the CLM effects as well as the soft triode-saturation transition impact.

[11] This routine uses a combination of bisection, secant and inverse quadratic methods, thus bearing better and faster convergence than Newton-Raphson method [77]

4.3 Switched-Current Sources: Simulation Results

4.3.1 DRAC Design

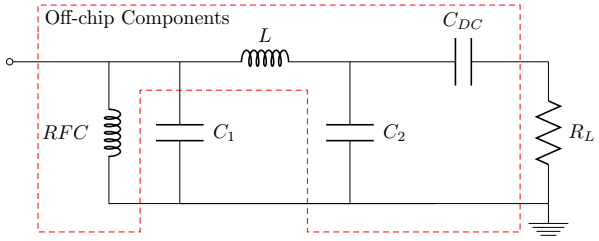


Figure 4.14: π MNT with the inclusion of the RF choke and dc de-coupling capacitor.

As previously stated, this dissertation implementation intends to achieve moderate output power, i.e. between 17 and 20 dBm. Hence, this design will be conducted to attain ≈ 18 dBm, considering that the frequency of operation, f_c, is 2 GHz. Thus, to maximise the transmitter performance, the MNT must be co-designed together with the DRAC.

To achieve impedance transformation and bandpass like filtering, there are assorted options available [78]. Amid them, the π MNT and the two-ladder L MNT are the most widely adopted [9, 17, 18, 35, 39, 49]. Considering that inductors are usually the main contributors to power loss in transmitters, avoiding or reducing their usage is beneficial. Hence, the π MNT seems the most advisable topology. Recalling (4.13), we observe that the supply voltage is considerably low, imposing the need for high currents, thus, high transformation ratios[12]. Therefore, the target drain load impedance, R_{opt}, is set to $\approx 5\,\Omega$. The loaded quality factor, Q_l, plays a key role in the transmitter performance. On one hand, selecting a high value guarantees excellent harmonic attenuation, while on the other hand it increases the power loss in the inductor [17][13], which is given by

$$P_{loss} = P_{out} \cdot \frac{Q_l}{Q_u} \tag{4.29}$$

where Q_u represents the intrinsic quality factor of the inductor. As a compromise, $Q_l = 4.5$ is selected. Besides, being efficiency one of the most important transmitter FoM, off-chip inductor is employed. Figure 4.14 illustrates the MNT in use. Capacitor C_1 is realised on-chip and its value should already contemplate C_{DS} and C_{pad}. Inductors RFC and L are set off-chip. Due to the required high transformation ratio, L value will be small. Hence, bond wire will be used, which usually present $Q_u \approx 20-30$ [79, 80] for short bond wires. DC blocking capacitor, C_{DC}, and C_2 are also off-chip components.

Different procedures can be adopted to design the π MNT, such as equivalent RLC parallel or back-to-back L network [73]. For brevity, design equations will not be exhibit in here. Table 4.2 shows the ideal and optimised values on the left and right, respectively. The ideal values were deduced without the influence of the dc blocking capacitance, while the optimised values already

[12] Transformation ratio is the ratio between the antenna load (usually 50 Ω) and the required optimum drain load, R_{opt}.

[13] This assumption is valid considering $Q_{u_{cap}} >> Q_{l_{ind}}$.

Table 4.2: Ideal and optimised components values of the π MNT.

	Ideal Values	**Optimised Values**
RFC	6 nH	6 nH*
C_1	16.9 pF	14.7 pF^{+}
L	1.04 nH	1 nH^{-}
C_2	7.16 pF	5.8 pF^{++}
C_{DC}	100 pF	100 pF**

* - Coilcraft 0302CS6N0 (model indicates DCR = 0.5 Ω against DCR = 0.104 Ω from website)
$^{+}$ - MiM capacitor plus pad capacitance, $C_{pad} \approx 0.26$ pF and $C_{DS} \approx 0.6$ pF
$^{-}$ - Considering the guidelines of the previous enumerated works, it will be assumed $Q_{bw} = 25$ (short bond wire).
$^{++}$ - Murata GJM0332C1E5R8WB01. At $f_c = 2$ GHz presents $C_{eq} \approx 7.2$pF
** - Murata GQM1882C1H101GB01.

take into account all the factors that affect the frequency response, such as bond wire parasitics and external capacitances behaviour[14]. Thus, the fundamental load obtained after optimisation is:

$$Z_{f_1} = 4.76 - 0.074\,\Omega \tag{4.30}$$

Taking in mind the goal output power as well as the MNT characteristics, we must ensure that the DRAC delivers enough output power to the MNT, which can be expressed by:

$$P_{RF} = P_{MNT} - P_{loss} = P_{MNT} - P_{MNT} \cdot \frac{Q_l}{Q_u} \tag{4.31}$$

Solving the equation above in order to P_{MNT} yields:

$$P_{MNT} \geq \frac{P_{RF}}{1 - \frac{Q_l}{Q_u}} = \frac{60\,\text{mW}}{0.82} = 73.17\,\text{mW} \tag{4.32}$$

Given the actual fundamental impedance, and recalling (4.15), the required fundamental current to follow the loadline theory, I_{f_1}, is:

$$I_{f_1} = \frac{V_{DD} - VDS_{sat}}{\Re\left\{Z_{f_1}\right\}} = 199.6\,\text{mA} \tag{4.33}$$

Hence, assuming perfect driving conditions[15] and $I_{f_1} \approx 200$ mA, the peak drain current can now be calculated by

$$I_p \approx \frac{I_{f_1}}{\sqrt{{a_1}^2 + {b_1}^2}} = 440\,\text{mA} \tag{4.34}$$

Under ideal circumstances, the output power would be given by $P_{rf} = P_{MNT_{peak}} \cdot 0.82 = 78.06$ mW, where $P_{MNT_{peak}} = 0.5 \cdot 4.76 \cdot {I_{f_1}}^2$. Moreover, the attained drain efficiency would be $\eta = \frac{78.06}{155.4} = 50.02\%$.

[14] Owing to the frequency dependent behaviour of the off-chip capacitors.
[15] As we will shortly see, the driving conditions influence the drain current profile, thereby, affecting the value of the fundamental current component.

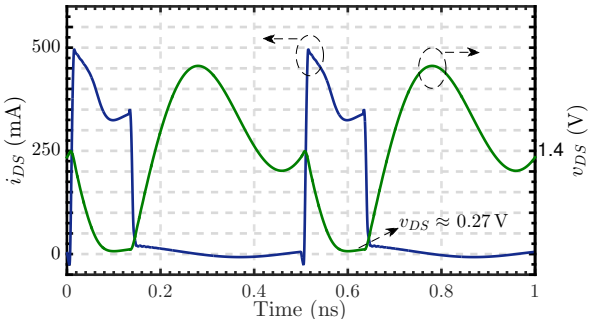


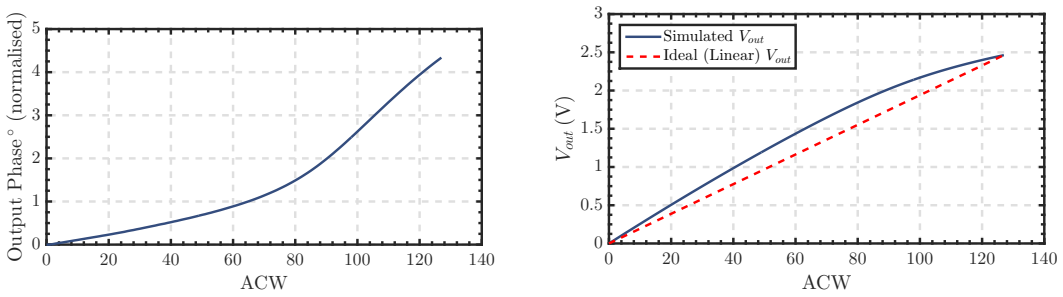
Figure 4.15: Current (blue) and voltage (green) waveforms under ideal driving conditions.

If one assumes that the DRAC loadline stays most of the time near the VDS_{sat} voltage, it is now possible to calculate the needed transistor width. Employing dc simulations and assuming $V_{GS} = 1.2\,\mathrm{V}$ and $V_{DS} = 0.45\,\mathrm{V}$, we verify that $W_T = 838\,\mu\mathrm{m}$ is capable of providing $I_p = 425\,\mathrm{mA}$. As previously predicted, the soft triode-saturation region and the strong i_{DS} harmonic component may conceive constraints to the DRAC operation. Therefore, we will start by assuming $W_T = 838\,\mu\mathrm{m}$ and only afterwards optimise the total width. Hence, assuming the former width allows to theoretically achieve $P_{rf} = 86.8 \cdot 0.82 = 71.18\,\mathrm{mW}$ and $\eta \approx 48\%$.

The adopted thin-gate 1.2 V RF NMOS transistors hamper the minimum width to $3.6\,\mu\mathrm{m}$. Sectioning the DRAC to make use of minimum width active devices would require 233 cells. This value is not practical, since it does not make use of the total 8-bit binary word. Being so, the DRAC will be divided into 127 unit cells, each one with a correspondent width of $6.6\,\mu\mathrm{m}$. In [20] Hu *et al.* adopted 5-bit AM path word resolution, proving to be enough to fulfil the spectral mask requirements[16]. As stated in [76], unary-weight cells provide better matching performance, at cost of increased complexity. However, employing only 127 unary-weight cells allows for a straightforward implementation. As a result, this proof-of-concept implementation is going to explore a DRAC with 7 bits (thermometer code) AM resolution.

Under the aforementioned conditions, the schematic of the figure 4.2 was simulated considering ideal driving conditions. Figure 4.15 shows us the simulated i_{DS} and v_{DS} waveforms for ACW= 127. The $\theta[n]$ waveform was set to own DT= 25% with rise/fall time $t_{rt} = 15\,\mathrm{ps}$, while its fundamental frequency is kept the same. The drain current and voltage waveforms present a deviation from what was initially expected. The voltage waveform presents not only the fundamental component, but also higher order harmonics. Simulated fundamental, second and third harmonic voltage components are $V_{ds_1} = 0.865\,\mathrm{V}$, $V_{ds_2} = 0.385\,\mathrm{V}$ and $V_{ds_3} = 0.248\,\mathrm{V}$, respectively. This indicates us that the initially assumed condition of perfect harmonic short circuit does not hold any longer. Accordingly, the simulated impedance provided by the MNT at the second and third harmonics is non-negligible and is given by $Z_{f_2} = 0.059 - j\,3.07\,\Omega$ and $Z_{f_3} = 0.027 - j\,1.94\,\Omega$. For that reason, the existence of the second and third voltage harmonic components disturbs the loadline, pushing the transistor beyond the minimum allowed voltage VDS_{sat}. This in turn obliges the

[16] Modulation formats employed were QPSK and 16-QAM.



(a) (b)

Figure 4.16: Figure (a) depicts the output phase evolution (i.e. AM-PM), while (b) illustrates the AM-AM linearity.

DRAC into the triode region, compressing the $i_{DS}(\theta[n])$ waveform and, simultaneously, trimming I_{ds_1}.

The peak output power is 60.65 mW, while the attained efficiency is 42.7%. The discrepancy found between the theoretical and simulated values is related to the previously identified loadline *distortion*. Recalling (4.14), we state that the efficiency is given by the ratio of the fundamental drain voltage amplitude and the voltage supply. The simulated fundamental drain voltage amplitude is lower than $V_{DD} - VDS_{sat}$, which consequently decreases the efficiency, as expected. Taking also the simulated $I_{ds_{f_1}} = 181\,\text{mA}$, the peak power delivered to the MNT is $P_{MNT} = 0.5 \cdot 0.8655 \cdot 0.181 = 78.33\,\text{mW}$. Thus, reminding (4.31), $P_{rf} = 64.22\,\text{mW}$, which is a quite good result, considering that we are neglecting losses on other passive elements (e.g. RF choke) and assuming same Q_l[17]. Hence, the strong second harmonic component appears as the main responsible of the reported decrease in peak power and efficiency.

Figure 4.16 illustrates the amplitude and phase variation as a function of ACW in figures 4.16a and 4.16b, respectively. As previously introduced, the proposed transmitter should attain linear AM-AM and AM-PM profiles. However, by inspecting the previous reported graphics, it is possible to verify that these characteristics are somewhat degraded. As already stated, $v_{DS_{min}} < VDS_{sat}$ condition is verified, which pushes NMOS transistors into the triode region, therefore, compressing the relation between I_{f_1} and ACW. Hence, this comportment is the responsible for the reported compression in the drain current waveform, i.e. AM-AM profile. Besides that, low v_{DS} voltage also introduces a new phenomenon, where the drain-bulk junction capacitance changes its value based on the v_{DS} voltage [74]. This behaviour is widely accepted as one of the roots of AM-PM linearity degradation [81]. Accordingly, this capacitance modulation induces the AM-PM distortion reported in figure 4.16a.

Figure 4.17 depicts now the proposed DRAC with the π MNT in which is possible to find an harmonic trap (series LC) whose function is to short-circuit the second harmonic at the drain plane. By adding this, we deviate the second harmonic current from the π network, restoring

[17] This assumption is reasonably good given that we are assuming that the Q_l of the optimised MNT is kept the same, i.e. $Q_l = 4.5$.

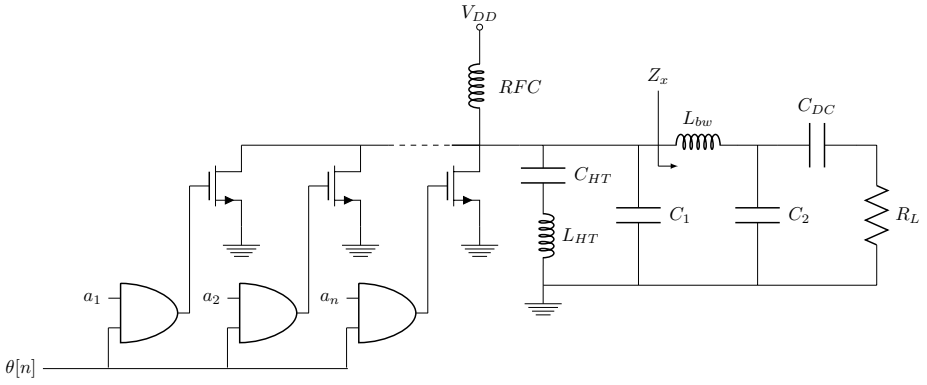


Figure 4.17: Proposed DRAC with additional LC harmonic trap.

the idealised loadline. For a compact design, the short circuit will be done with one short bond wire plus an on-chip capacitor. Although it will not be detailed nor employed in this dissertation, the series capacitor could be made tunable in order to adjust the harmonic trap against process variations. To preserve a compact design, we will assume $L_{HT} \approx 0.6\,\text{nH}$, while having the same unloaded quality factor as L_{bw} ($Q_u = 25$). The series capacitor is given by:

$$C_{HT} = \frac{1}{L_{HT}\, {w_0}^2} = 2.62\,\text{pF} \tag{4.35}$$

Selecting this inductor-capacitor combination ensures a compact design without affecting higher-order harmonics terminations. The fundamental impedance of the harmonic trap is $Z_{HT} = 0.3 - j\,22.83\,\Omega$, which allows us to calculate the current that flows into the π MNT:

$$I'_{f_1} = \frac{I_{f_1} Z_{HT}}{Z_{HT} + Z_{f_1}} \approx I_{f_1} \cdot (0.9532 - 0.2\,j)\,\text{A} \tag{4.36}$$

We can now express the amount of current that flows towards the antenna, i.e. that travels through the bond wire inductor, L_{bw}, by

$$I''_{f_1} = \frac{Z_{C_1} I'_{f_1}}{Z_{C_1} + Z_x} \tag{4.37}$$

where Z_x is pointed in figure 4.17 and its simulated value is $Z_x = 2.62 + j\,2.38\,\Omega$, while C_1 impedance at the carrier frequency is $Z_{C_1} = -5.41\,j\,\Omega$. Thus, the total amount of current that circulates towards the antenna is given by $I''_{f_1} = I'_{f_1} \cdot (0.95 - j\,0.784)\,\text{A}$. Consequently, the power delivered to the π MNT is calculated by

$$P_{MNT} = \frac{1}{2} \cdot \Re\{V\, I^*\} = \frac{1}{2} \cdot \Re\{Z_{f_1}\, {I_{f_1}}'\, {I_{f_1}}'^*\} \tag{4.38}$$

whereas the power being dissipated in the bond wire resistance, R_{bw}, at the frequency of interest is expressed as:

$$P_{loss} = \frac{1}{2} \cdot \Re\{V\, I^*\} = \frac{R_{bw}}{2} \cdot \Re\{{I_{f_1}}''\, {I_{f_1}}''^*\} \tag{4.39}$$

Assuming the same conditions as in above and solving (4.38)–(4.39) results in $P_{MNT} = 82.4\,\text{mW}$

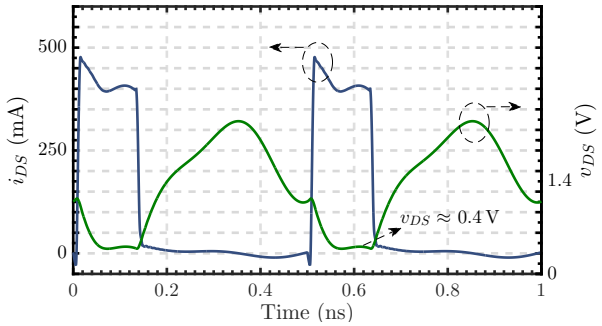


Figure 4.18: Drain voltage influence under second harmonic trap.

and $P_{loss} = 13.2\,\mathrm{mW}$, respectively. These results are valid as long as the second harmonic remains correctly short-circuited. Hence, the minimum v_{DS} voltage will no longer push the DRAC into triode region. Furthermore, the only additional source of power loss is related to the harmonic trap[18], which can be calculated as

$$P_{diss_2} \approx \frac{1}{2} \cdot R_{HT}\, I_{f_2}^2 \tag{4.40}$$

where $R_{HT} \approx 0.6\,\Omega$ represents the bond wire resistance at $f = 2 \cdot f_c$ and $I_{f_2} = 0.3183 \cdot 0.425\,\mathrm{A}$. Solving the previous equation results in $P_{diss_2} \approx 5.5\,\mathrm{mW}$, which is considerably low. Thus, the power being delivered to the antenna is expressed as

$$P_{rf} = P_{MNT} - P_{loss} = 69.2\,\mathrm{mW} \tag{4.41}$$

while the drain efficiency is calculated as

$$\eta = \frac{P_{rf}}{P_{dc}} = \frac{69.2\,\mathrm{mW}}{148.6\,\mathrm{mW} + 5.5\,\mathrm{mW}} = 44.9\% \tag{4.42}$$

assuming no extra sources of loss in the MNT nor other passive elements.

Figure 4.18 portrays the simulated drain voltage and current waveforms. Performing a correlation between the simulations with and without (recall figure 4.15) harmonic trap, it is possible to observe uncanny differences. When employing the LC series, the voltage waveform reduces both the minimum and maximum values from $0.27\,\mathrm{V} \rightarrow 0.4\,\mathrm{V}$ and $2.335\,\mathrm{V} \rightarrow 2.28\,\mathrm{V}$, respectively. This is consequence of the second harmonic absence. Moreover, when v_{DS} is a its minimum, the voltage acquires a square wave-like shape, which indicates us the presence of the third harmonic, similar to what occurs in class F PA [82]. Au contraire, here we pretend to maintain the current waveform square, hence, minimising the AM-AM distortion.

Figure 4.19 illustrates the evolution of both the power and drain efficiency in solid blue and green lines. Firstly, the attained peak power under second-harmonic short circuit is incremented from 60.65 mW to 66.5 mW, which represents a relative enhancement of $\approx 10\%$. The predicted output power was 69.2mW, which results in a reasonably good agreement. Secondly, the drain

[18] At the fundamental frequency the impedance of the series LC is considerably higher than Z_{f_1} ($|Z_{ht}|/|Z_{f_1}| \approx 5$), thus being reasonable to assume negligible contribution to the total power loss.

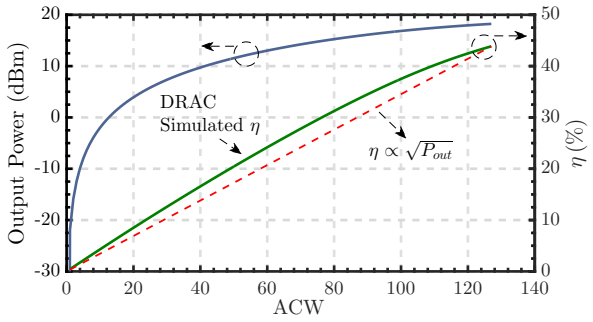


Figure 4.19: DRAC output power (solid blue) and efficiency (solid green) under second harmonic termination. Red dashed line represents the ideal efficiency of a class B PA (i.e. $\propto \sqrt{P_{out}}$).

efficiency goes as high as 43.9%, representing then a increment of 1.2% against the former situation. Again, the simulated efficiency is in agreement with the theoretical derivation ($\eta = 44.9\%$). Furthermore, the η profile is closely related to the ideal class B PA (red dashed line in the previous cited figure), feature common to almost all the state-of-the art DPAs [22, 76]. In addition, the simulated dynamic range (DR) of the proposed DRAC is: $\text{DR} = P_{rf}(ACW = 127) - P_{rf}(ACW = 1) = 18.22\,\text{dBm} - (-21.91\,\text{dBm}) = 40.13\,\text{dB}$.

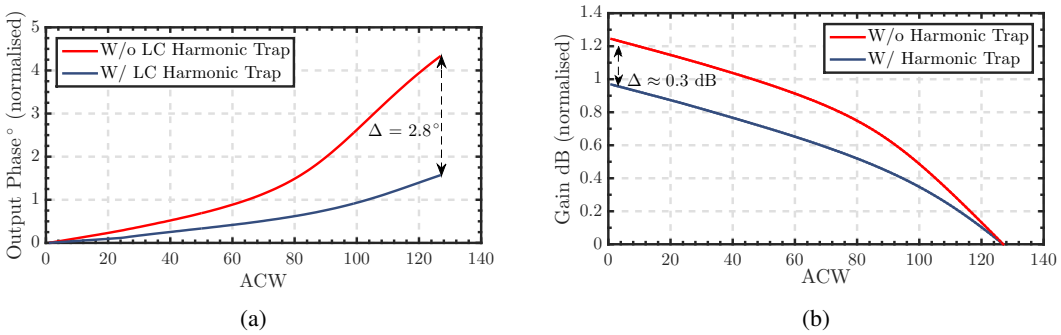


Figure 4.20: Figure (a) depicts the AM-PM linearity, while (b) illustrates the gain evolution (i.e. AM-AM).

Despite of the slightly enhanced efficiency and augmented output power, the major advantage of the LC series trap is the improved transmitter linearity. In order to verify this condition, let us inspect the figure 4.20, where both gain(ACW)$= V_{out}(ACW)/ACW$ (logarithmic scale) and $\angle V_{ou}$(ACW) are portrayed in the left-sided and right-sided graphics, respectively. Gain profile is normalised to the peak power operation, whereas the phase is normalised[19] to ACW$= 1$. The gain distortion is reduced by 0.3 dB, while the AM-PM distortion is merely 1.6°, representing a decrease of 2.8°. Hence, the proposed reduced conduction angle DRAC achieves good linearity, while still attaining relatively high drain efficiency, however, at the cost of using external inductors.

[19] In simulation, when ACW $= 0$ the output phase (at RF frequency) is represented with 0°, value that differs from ACW$= 1$. Therefore, for representation purposes, this case is ignored given that it corresponds to zero output power, i.e. no signal (information) being transmitted.

Regardless, one must keep in mind that the proposed topology is single-ended, operates from a relatively low-power supply voltage and attains high load transformation ratio (> 10). Additionally, the co-existence of both a strong harmonic content as well as non-null MNT impedance termination at higher order harmonics present a non-negligible, nonetheless relatively small, impact in both η_{peak} and $P_{rf_{peak}}$, as formerly demonstrated.

4.3.2 Assessing CLM and Soft Triode-Saturation Transition Impact

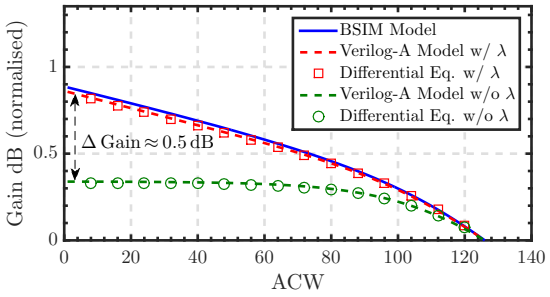


Figure 4.21: Simulated gain characteristic with BSIM (solid blue), verilog-A models with (dashed red) and without CLM (dashed green) and by solving the differential equation for the same cases (red markers for CLM and green ones without).

In the previous sub-sections, the analyses conducted assumed that the soft triode-saturation region as well as the CLM effect presented negligible impact on the DRAC performance. By inspecting figures 4.16b and 4.20b, it is observable some degree of AM-AM distortion. Indeed, the triode-saturation region impact on the current waveform compression, i.e. AM-AM degradation, was already identified. Nevertheless, by inspecting more closely figure 4.20b, which reports the gain variation of the proposed DRAC, an interesting behaviour in the AM-AM characteristic is found: the typical AM-AM behaviour of PAs whose working principles are based on current sources, i.e. NMOS are kept in saturation whenever they are ON, (class B/AB) is characterized by a constant value, starting to decrease (compress) when approaching the maximum output power [83, 84]. Yet, the reported gain variation is always incrementing (from peak to the off condition), indicating that the CLM effect may also present non-negligible contribution. Furthermore, in [76] the authors state that the cause of the reported AM-AM profile is related to the variable output impedance. The cited work makes use of differential class-B based DPA[20], where the drive signal is assumed sinusoidal. Hence, this imposes a different behaviour in the loadline (typical loadline of *analog* class B), whereas most of the widely adopted DPAs present loadlines similar to the ones shown in 4.13[21]. This instigates the need to further investigate and quantify the CLM effect in DPAs, namely to explain the observed gain(ACW) behaviour in the proposed topology.

[20] As a matter of fact, the DPA proposed in the cited work varies its operation from class B like to class E and class E^{-1}. However, their explanation regarding the AM-AM distortion addressed the class B style operation.

[21] Although only depicted the case of SCS, the SRA behaviour possesses similar behaviour, i.e. the NMOS is pushed into the triode, with fast transitions between triode and cut-off (assuming peak power operation).

With regard to assess and quantify the CLM effect, a new set of simulations shall be performed, only this time considering a *RLC* parallel filter. This will remove the strong v_{DS} harmonic component as well as simplifying the theoretical $v_{DS}(\theta[n])$ prediction, thereby easing the use of the expression derived in (4.27). These new set of simulations will be performed at a relatively low frequency, e.g. $f_c = 100\,\text{MHz}$, mitigating the non-linear C_{DB} output capacitance influence. By reason of attaining the same minimum $v_{DS}(\theta[n])$, i.e. $v_{DS_{min}} \approx 0.4\,\text{V}$, we will consider the following load:

$$R_L = \frac{\Delta V_{ds}}{I_{f_1}} = \frac{1}{0.191} = 5.236\,\Omega \tag{4.43}$$

The model described in (4.22)–(4.24) assumes linear $i_{DS}(v_{GS})$, thus, the rise/fall time will be set to $t_{r,f}/T << 1$, where $T = 1/f_c$. Moreover, the chosen loaded quality is 8.

Taking in mind that each unit cell width is $W_{unit} = 6.6\,\mu\text{m}$, the values presented in table 4.1 will be used both in a verilog-A model and in the procedure to solve equation (4.27). Figure 4.21 illustrates the simulation[22] results as well as the output given by (4.27). Solid blue line represents the BSIM results, while the red markers and dashed line depict the results of both the equation and verilog-A model with CLM, respectively. Green markers and dashed line represent the same as the previous, though under no CLM effect. Thus, it is clearly possible to notice the gain variation caused by the finite output resistance. As a matter of fact, under the described conditions $r_o(\text{ACW})$ is responsible for an increase of $\approx 0.5\text{dB}$ when compared with no CLM. Hence, the CLM effect actually contributes with more distortion than the soft triode-saturation transition. Comparing the previous results with the profiles reported in figure 4.20, one can state that they are closely related, validating then the proposed explanation for the incremental gain variation. Moreover, it also seems valid to state that the non-linear C_{DB} capacitance presents negligible effect on the AM-AM profile. It is also worthy to notice the accuracy of the proposed elementary model against the BSIM simulation.

4.3.3 25% Duty-Cycle Clock Generation and Digital Domain Implicit Mixer

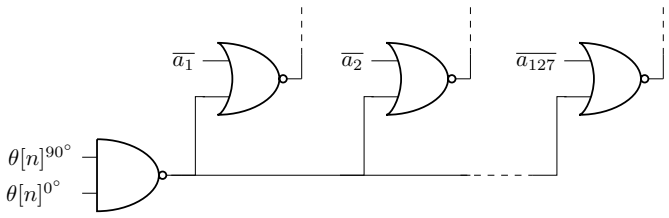


Figure 4.22: 25% duty-cycle converter and implicit digital mixer.

Throughout the simulations performed in the previous sections, it was always assumed that the RF modulated signal arrived at the DRAC core with DT= 25%. Obviously, there are numerous ways to generate the required signal. RF pulse-width-modulation (PWM) architectures proposed

[22] All simulations were carried out in Cadence SpectreRF with periodic-steady state simulation.

in [71, 85] employ delay-based chains (usually inverters) to produce the required variable duty-cycle. In [37], Alavi *et al.* generate four quadrature 25% DT clocks running at 2 GHz in 65 nm CMOS node. To do so, differential clock dividers plus AND gates are used, since the input clock runs at $f = 8$ GHz. Although both the previous solutions may produce the required driver waveform, the hardware overhead as well as the power consumption is demanding[23]. Hence, a simple chain topology will be introduced here to address the clock conversion, trying to achieve both low-power consumption and mitigate wanted effects in the driver waveform. Furthermore, the solution unveils the use of complementary logic, being advantageous in terms of area and power consumption.

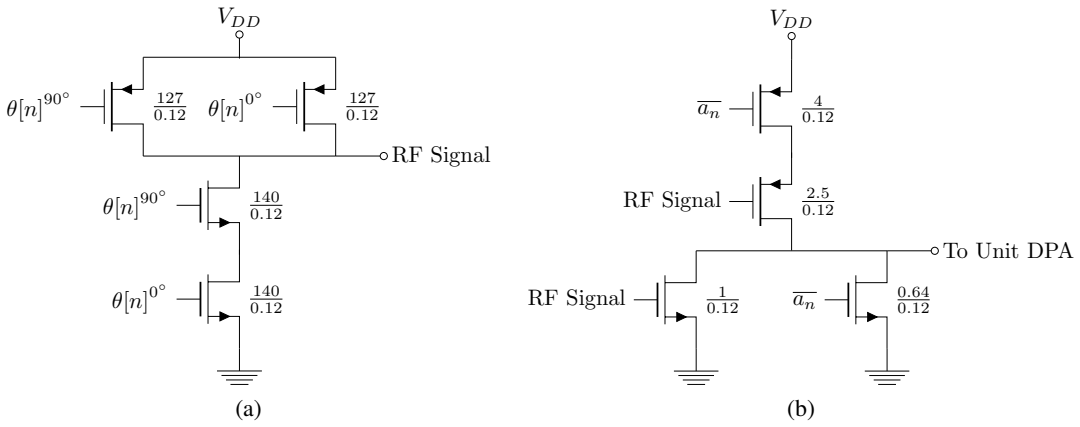


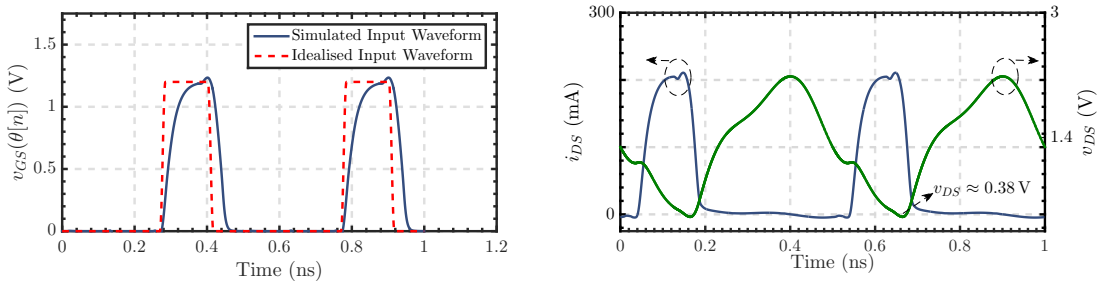
Figure 4.23: Transistor level implementation of: (a) 25% DT generator and (b) implicit unit digital mixer.

If the in-phase and in-quadrature versions of the RF phase modulated signal, i.e. $\theta[n]^{0^\circ}$ and $\theta[n]^{90^\circ}$, are available, a very simple, yet elegant approach can be followed in order to generate the wanted signal. Figure 4.22 depicts the proposed driver and 25% duty-cycle generator. The first NAND gate receives both 0° and 90° square-wave clocks, producing at its output a signal whose DT is 75%. The generated complementary version of the wanted signal drives each one of the 127 unit *mixers*. The NOR logic gates will in turn generate the required waveform, i.e. DT= 25%, at the DPA unit cell input. From the initial schematic depicted in figure 4.2, the control signals (a_1-a_{127}) are now their complementary version due to the NOR use [20]. In addition, this digital mixer implementation outperforms the transmission-gated-based multiplexer [4], since it achieves lower rise/fall times[24].

Figure 4.23 details the transistor level implementation of the proposed clock converter plus gate driver/mixer, while figure 4.24a illustrates the input waveform of each unit PA cell (output signal of figure 4.23b). The rise and fall time of each logic gate induce a small *distortion* in the drive waveform. Fortunately, the observed deformity is not awfully harmful to the DRAC expected

[23] Using inverter based chains to generate the required signal would result in higher power consumption, whereas the solution adopted in [37] would originate unnecessary area overhead, given that it is designed to address differential DPA.

[24] This is due to the decelerated MOS channel charging/discharging process [37]



(a) (b)

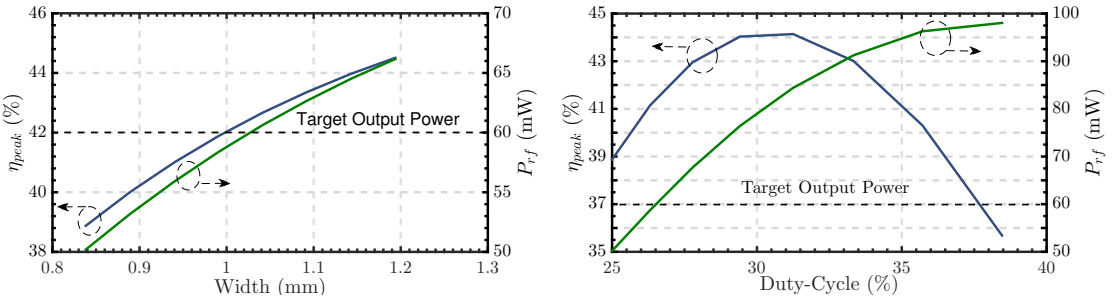
Figure 4.24: Figure (a) depicts the ideal and simulated input waveform while (b) portrays the i_{DS} and v_{DS} current and voltage waveforms, respectively.

performance, while its impact can (and will) be easily outweighed. Therefore, the selected total width (in µm) of each NAND transistor can be found in figure 4.23a, while the sizing of each unit mixer is depicted in figure 4.23b. Operating from $V_{DD} = 1.2\,\text{V}$, the proposed clock converter and implicit mixer maximum power consumption is only 8.5 mW. The sizes were chosen as a comprise between area overhead, driver waveform and power consumption.

Simulating the proposed driver chain with the previously demonstrated DRAC results in a drain current and voltage waveforms that can be found in figure 4.24b. As previously described, the deformed driver waveform should impact the transmitter performance. Indeed, the simulated peak output power and efficiency drop slightly to $P_{rf} = 50.3\,\text{mW}$ and $\eta = 39\%$. Therefore, the $v_{GS}(\theta[n])$ deformity impacts the $i_{DS}(\theta[n])$ harmonic component, which is somewhat altered, leading to lower output power and efficiency. We can also confirm this behaviour by inspecting the drain voltage waveform. Thus, we still need to add circa 10 mW to reach the goal output power.

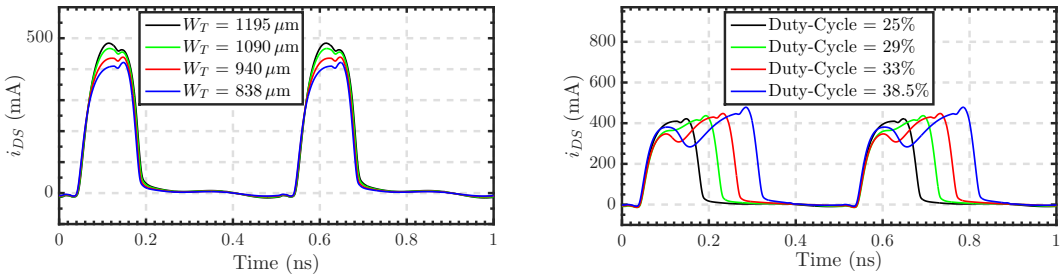
Two possible solutions come quick in handy to address this situation: the first obvious one is to increment the total DRAC width, therefore delivering more current to the output load; likewise, we could also enlarge the duty-cycle[25] (recall figures 4.4 and 4.6). Figure 4.25 illustrate both the

[25]This was achieved by incrementing the total amount of time that both the in-phase and quadrature $\theta[n]$ signals overlapped. This way, the DT generator and unit mixer were kept in the transmitter chain (i.e. DRAC).



(a) (b)

Figure 4.25: Efficiency and output power evolution as a function of the (a) DRAC width and (b) duty-cycle.



(a) (b)

Figure 4.26: Drain current profile in time for various: (a) DRAC width and (b) duty-cycles.

evolution of η_{peak} and P_{rf} under the conditions of varying width (left-sided sub-figure) and driver duty-cycle (right-sided sub-figure). Interestingly, changing the width or DT seems to result in a antithetic behaviour: while the first one improves the η_{peak} while attaining lower power increase, the last one presents higher P_{rf} increment, however, decreasing η right after. Changing the width from 838 µm to about 1000 µm allows us to achieve the desired power level as well as keeping the initial width (838 µm) and increment the DT. Figures 4.26a and 4.26b portray the drain current under four different widths and duty-cycles scenarios, respectively. By incrementing the total width it is possible to achieve the desired power level while maintaining almost intact the $i_{DS}(\theta[n])$ waveform. This indicates that trying to achieve the target output power through this alternative, may not add substantial static non-linearity to the proposed DRAC. Differently, increasing the DT leads to a compression in the i_{DS} waveform, thus worsening the AM linearity. Furthermore, modifying the current DT would lead to readjustments in both the clock converter and implicit mixer topologies. Thence, it is rather preferable to implement the first option. Thus, the final selected width is 1090 µm[26].

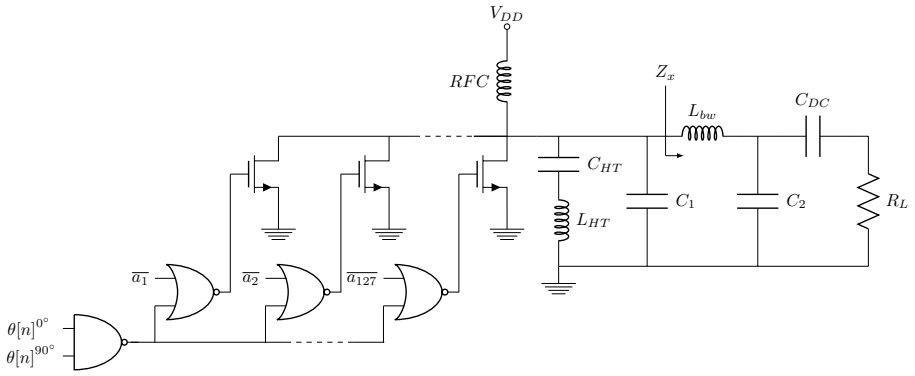


Figure 4.27: Final schematic of the proposed reduced conduction angle DRAC.

Under the aforementioned conditions, we will now fully characterise the proposed DRAC performance through simulation. The final schematic can be observed in figure 4.27, where the

[26]Comparing this new W_T with the former, we could now segment the DRAC to be controlled by a 8-bit code word. However, for the sake of simplicity, we will proceed with the 7-bit code word.

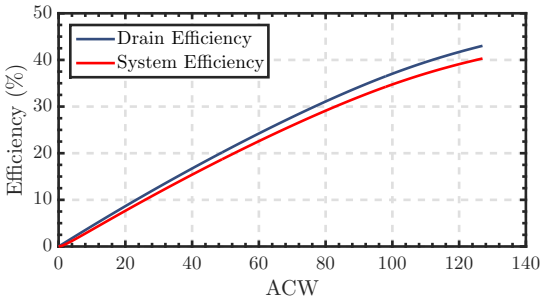
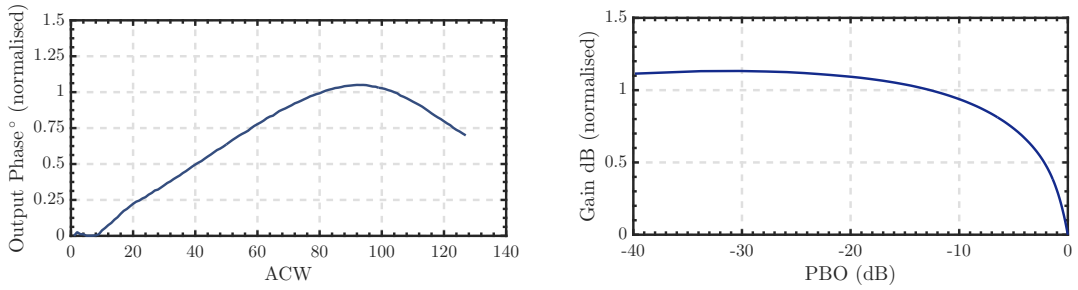


Figure 4.28: Drain (solid blue line) and system efficiency (solid red line) as a function of the ACW.

attained simulated peak power and efficiency are $P_{rf_{peak}} = 62\,\text{mW}$ and $\eta_{peak} = 43\%$, respectively. Moreover, the simulated second and third harmonics at full power are $P_{rf_2} = -51.4\,\text{dBm}$ and $P_{rf_3} = -25\,\text{dBm}$, which results in a fundamental to harmonic relation of $\Delta_{f_2} = 69.3\,\text{dB}$ and $\Delta_{f_3} = 42.9\,\text{dB}$, respectively. Furthermore, owing to no significant i_{DS} waveform *deformity* (evoke figure 4.26a), the driver chain width was not adapted.

Figure 4.28 portrays the evolution of both the system and drain efficiency in solid red and blue lines. As earlier declared, the accomplished peak drain efficiency was 43%, while the system efficiency (accounting for 25% clock generator plus implicit mixers) in peak power operation is 40%. The power consumption of the digital blocks varies from 2.65 mW when ACW= 0 to 9.5 mW under full power operation. Even though the power wasted in the drivers is substantially when correlated to the total amount of power delivered to the antenna, the final efficiency is arguably satisfactory.

That being said, it is now time to assess the static linearity. Figures 4.29a and 4.29b report the total amount of phase and gain (dB scale) variation, respectively. When compared with the results achieved with the ideal drivers (recall figures 4.20), we now attain less phase variation, while keeping approximately the same gain fluctuation. This indicates us that, besides the waveform distortion and the needed compensation mechanism employed, the transmitter can achieve essentially the same results as before, at expense of cramped increase in the total area.



(a) (b)

Figure 4.29: Figure (a) depicts the phase variation as a function of the ACW while figure (b) illustrates the gain variation as a function of PBO. Both measures are set normalised, as previously established.

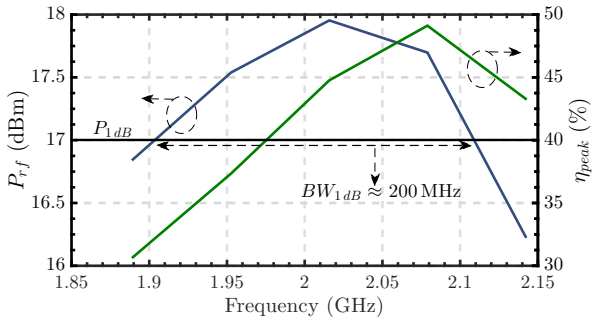


Figure 4.30: Drain efficiency (green solid curve) and output power (blue solid curve) as a function of frequency (ACW = 127)[27].

The performance over frequency was also verified, whose results can be perceived in figure 4.30. The $P_{1\,\mathrm{dB}}$ bandwidth is approximately 200 MHz, while the drain efficiency is kept in between 33% and 45%, reaching a peak efficiency of 48.8% at $f_c = 2.08\,\mathrm{GHz}$.

4.4 Conclusions

This chapter presented the proposed polar digital transmitter based in a reduced conduction angle DRAC topology. Theoretical foundations were presented as well as the main trade-offs between efficiency and achievable peak output power. Moreover, a compromise was made by selecting a conduction angle of 25%, while the supply voltage was also chosen to optimise both the efficiency and output power, without sacrificing the device performance.

The DRAC core was designed and optimised together with the π MNT. Second harmonic LC trap was employed, leading to improved efficiency, output power and linearity. Under these conditions, the proposed topology outputs 17.92 dBm while attaining 43% drain efficiency at $f_c = 2\,\mathrm{GHz}$. Moreover, a peak drain efficiency of 48.8% is also reported within the $\mathrm{BW}_{P_{1\,\mathrm{dB}}}$. The simulated PBO efficiency profile matches those observed in current state-of-the-art implementations, confirming then the typical class B style behaviour in PBO.

Considering full ACW excursion, the attained phase variation was 1.1°, while the gain variation is kept below 1.1 dB. The main cause of AM-AM degradation was identified as being the CLM effect. A theoretical foundation was derived and the simulation results between BSIM and verilog-A models as well as theoretical equation show an excellent match, corroborating then the proposed explanation. In addition, smooth profile of both AM-AM and AM-PM is reported, being reasonable to affirm that the DRAC presents considerably good linearity. Furthermore, the proposed topology could take advantage of advanced CMOS nodes in terms of power consumption. However, due to increased CLM, we should also expect AM-AM degradation.

[27] Both the peak drain efficiency and output power curves were simulated with low number of points, thereby not including $f_c = 2\,\mathrm{GHz}$.

Chapter 5

Towards High PBO Efficiency

Energy efficiency paradigm is compelling the global industry and scientific community to focus in new wireless transmitter solutions that require less power, smaller batteries and lower charging time. Therefore, highly efficient wireless transceivers are needed to endure the aforementioned requirements. Unfortunately, as previously identified, all-digital transmitters own sparse efficiency performance when operating at PBO. Recently, Doherty based all-digital transmitters have been successfully integrated in low power CMOS nodes (e.g. 65 nm) [21, 72], showing promising metrics. However, the achieved PBO efficiency enhancement profile does not show great correlation with the idealised Doherty operation. Moreover, the use of parallel combining matching network increases excessively the IC area [9]. Nevertheless, this work opened the way to wideband Doherty CMOS operation demonstrating an effective reconfigurable PBO efficient mixed-signal transmitter. Outphasing digital transmitters have already been explored, however demonstrating relatively low drain efficiencies [19, 41]. Reported DLM CMOS based works focus their approaches in analog centred techniques, while adopting considerably high supply voltages. Thus, their amenability to CMOS integration is harshly degraded. However, in [16] a 1-bit DLM transformer all-digital transmitter is introduced. Due to the use of two transformers the occupied IC area is considerably high. Nonetheless, a remarkable 60% increase in efficiency at 6 dB PBO is reported.

To tackle this century-old problem, we propose the use of discrete DLM in the context of all-digital transmitters. The method achieves multi-level discrete DLM without incurring in severe linearity losses. An optimisation algorithm is proposed and detailed in section 5.2. The approach guarantees minimum AM-PM distortion, leaving only the AM-AM profile (static DPD) correction to the BB. However, as a viable alternative, a mixed-signal AM-AM correction technique is also demonstrated in static conditions in section 5.3.1. In section 5.3.2, simulation results with all non-ideal elements are presented as well as the selected topology to implement the variable capacitance elements.

5.1 Dynamic Load Modulation

Dynamic load modulation appears as a promising solution to be integrated in digitally assisted transmitters. However, the majority of CMOS implementations found in literature are usually based in *analog* PA blocks, such as *linear* class B/AB [9, 17, 86, 87], imposing serious threats for sub-micrometer CMOS implementations.

The tunable matching network block comprises the heart of the DLM. Its efficiency and linearity performance are vital to the correct transmitter behaviour. Therefore, when addressing the MNT design and topology selection, this criteria must always be present. The double cascade L network [88] reveals itself as a promising solution to achieve the desired result. The π based network can also be used to accomplish effective DLM. In [17] Yu *et. al* presented a two-level switching scheme to achieve DLM. However, to achieve small phase variation high drain impedances are adopted, which limits the attained peak output power. Unfortunately, the two previous MNTs show lack of convergence in the proposed method when targeting multi-state DLM.

The shortly reviewed set of works as well as the ones presented in sub-section 3.2.2 indicates us that DLM is viable in CMOS nodes. Hereby, an opportunity exists concerning the exploration of this technique in context of DPA, where we could take advantage of sub-micrometer CMOS nodes strengths.

5.1.1 DLM Challanges: Design Perspective

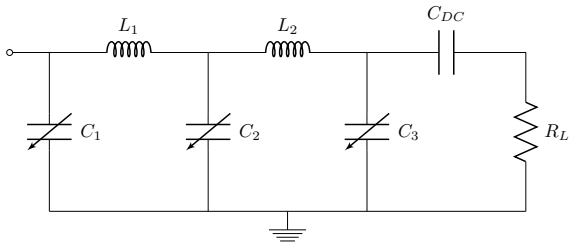


Figure 5.1: Double π MNT with variable capacitors.

To attain diminished phase variation and low losses in the LC based MNTs, state-of-the-art implementations resort to high drain impedance loads [9, 17, 86], which inevitably result in high supply voltages. Moreover, all reported CMOS implementations only achieve two-level DLM[1]. Using the π network as a TMNT not only imposes the adoption of low transformation ratios, but also the need for a considerably high supply voltage, condition that is undesirable in mobile devices targeting medium power (i.e. $17-25\,\text{dBm}$). Moreover, matching networks that only possess one or two tunable capacitors seem to limit the attained transformation ratio, thereby restraining

[1] In [15] it is proposed a SOI-CMOS based transmitter that employs multi-level DLM. However, no AM-AM nor AM-PM profiles are reported.

the PBO efficiency range[2]. Therefore, to mitigate the previously mentioned challenges, we propose the use of a double π tunable matching network, whose schematic is depicted in figure 5.1. To address multi-level DLM and, simultaneously, to diminish the phase variation (i.e. to attain linear AM-PM profile) the presented methodology is supported by an optimisation algorithm, whose description is delineated in the following section.

Before jumping into the MNT design, let us first define some basic notation. Let us assume that each solution can be represented in a matrix form, expressed as

$$S_k = \begin{bmatrix} C_{1_{R_1}} & C_{2_{R_1}} & C_{3_{R_1}} \\ C_{1_{R_2}} & C_{2_{R_2}} & C_{3_{R_2}} \\ \vdots & \vdots & \vdots \\ C_{1_{R_n}} & C_{2_{R_n}} & C_{3_{R_n}} \end{bmatrix} = \begin{bmatrix} S_{R_1} \\ S_{R_2} \\ \vdots \\ S_{R_n} \end{bmatrix} \tag{5.1}$$

where $C_{b_{R_n}}$ corresponds to the capacitance b of the solution n that provides the real load impedance R_n. Phase linearity should also be object of attention to guarantee minimum phase distortion. Considering that $H_n(j\cdot\omega) = I_o(j\cdot\omega)/I_i(j\cdot\omega)$, where $I_i(j\cdot\omega)$ corresponds to the input current source and $I_o(j\cdot\omega)$ to the current that flows through the antenna, we must ensure that the transfer function phase for each state is approximately identical, which can be stated as:

$$\angle H_n(j\cdot\omega_c) = \angle H_{n+1}(j\cdot\omega_c) \tag{5.2}$$

The transfer function can be inspected in appendix A.1. Furthermore, besides the phase linearity, we also need to guarantee that each impedance state, $Z_n(S_{R_n})$, is equal to

$$Z_n(S_{R_n}) = R_{d_n} + j\cdot X_{d_n} \approx R_{d_n} + j0 \tag{5.3}$$

being R_{d_n} the ideal resistance for a given PBO level. Defined this two prominent conditions, we are only left with selection of the inductors L_1 and L_2.

Assuming on-chip inductors would take us to impracticable efficiencies[3], consequently, wasting the DLM advantage. Moreover, in order to achieve reasonable efficiency with on-chip inductors, differential architectures and high optimum drain load impedances are usually employed. This in turn requires the usage of prohibitively high supply voltages. As an alternative, it is proposed here an approach relying on off-chip inductors. Unfortunately, at $f_c \geq 2\,\text{GHz}$, the required inductors values for π based MNT designs are relatively small[4] (e.g. 1 nH to 2 nH), which imposes additional design challenges due to the bond wire inductance. Therefore, to ameliorate the proposed proof-of-concept design, we will assume from now on that $f_c = 1\,\text{GHz}$, enabling then higher $L_{1,2}$ values.

[2] As previously affirmed, both the double L and π MNT have shown no convergence when applied in the procedure to be introduced in section 5.2.

[3] The attained peak efficiencies under these conditions would only go as high as 12% to 20%.

[4] Through simulation we verified that $L_1 = 1.5\,\text{nH}$ and $L_2 = 2\,\text{nH}$ would allow an implementation at $f_c = 2\,\text{GHz}$. However, this would require extra care in the simulations given that bond wire inductance presents $L_{bw} \approx 0.4\,\text{nH} - 0.8\text{nH}$.

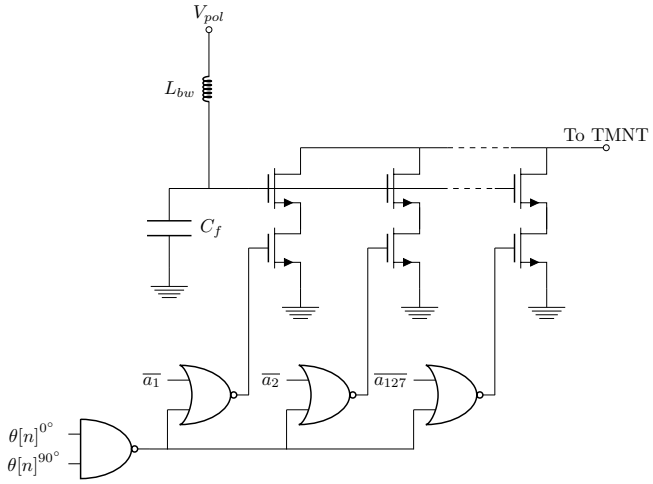


Figure 5.2: Proposed cascode based DRAC.

The all-digital transmitter presented in chapter 4 operates with $V_{DD} = 1.4\,\text{V}$ and requires an impedance transformation > 10. Thus, to alleviate the design constraints and reduce the MNT losses, we will consider from now on that the optimum peak power impedance is $R_{opt} = 10\,\Omega$. However, if we maintain the same unit cell structure, the output power is reduced. Therefore, to attain approximately the same output power as before, we will resort to a cascode unit-cell that operates with $V_{DD} = 2.2\,\text{V}$ and requires a polarisation voltage, V_{pol}. The schematic of the modified proposed architecture can be found in figure 5.2. The stacked transistor works as a voltage controlled current source, whereas the transistor at the bottom continuously changes its state from OFF and ON, presenting a given ON resistance, R_{ON}. This switching action imposes rapid voltage variations at the source of the top transistor, therefore, inducing current glitches[5]. To mitigate this undesired effect, a large capacitance, $C_f = 70\,\text{pF}$, is inserted between the top transistor gate and ground. Furthermore, performing the switching action in the bottom transistor eases the interface with the BB (clock converter and unit mixers), while incrementing the feed-through isolation. Moreover, adopting the cascode structure impacts positively the AM-AM profile due to its inherently higher output resistance, r_o.

5.2 Efficient Optimisation Algorithm: PSO-Based Approach

To address the design of the MNT diverse options can be followed. As previously stated, all the reported CMOS implementations only achieve two state DLM, condition that enables a somewhat simpler design. However, when targeting multi-level DLM to achieve deep PBO efficiency enhancement, the traditional approach is substantially demanding. Thus, developing a computationally efficient algorithm to tackle this problem seems a reasonable decision. Applying optimisation

[5]This current spikes appear between the source and gate of the top transistor due to the high $\frac{\partial V}{\partial t}$ that the NMOS capacitance experiences.

algorithms to solve and optimise electronic design flow is a well established approach [52], where usually genetic algorithms or its modified versions are employed.

Inspired by the social behaviour of animals, such as bird flocks, particle swarm optimisation (PSO) algorithm searches the solution space in a parallel like style, thus allowing excellent computation efficiency [89]. The basic principle is that each particle acts on its own with random movements, however, keeping track of its best position and accessing the shared information of the whole swarm (i.e. global best known position). Unlikely the evolutionary algorithms, PSO does not make use of evolutionary concepts (e.g. mutation or crossover) only relying on the co-operation principle. Due to its extreme simplicity, this algorithm can be easily fully implemented providing flexibility to the end user. Moreover, PSO based implementations allow the transition from single to multi-objective optimisation without requiring too much effort [89], condition that will enable future improvements to the current solution. Although we have adopted PSO to solve this design, other well-established optimisation algorithms could be used as well. Using mathematical notation, the algorithm can be described as follows

$$VEL[i] = K_1 \cdot (P_{BEST}[i] - POP[i]) + K_2 \cdot (G_{BEST} - POP[i]) \tag{5.4}$$

and

$$POP[i] = POP[i] + W \cdot VEL[i] \tag{5.5}$$

where $VEL[i]$, $POP[i]$ and $P_{BEST}[i]$ are the current velocity, position and personal best of the particle i, while G_{BEST} is the global best known position. Constants K_1 and K_2 values range between 1-4 and W is a inertia coefficient. In this design $K_1 = 1$ and $K_2 = 2$, while the inertia coefficient was chosen to vary between 0.1 and 0.4, with a non-linear relation between iterations. By applying inertia, a balance between space exploration and exploitation process is provided. Likewise, it also helps the convergence process in the early stage of the algorithm [90]. Obviously, to quantify each one of the solutions, i.e. S_K, we need to assess their performance with the fitness function. This function gives us feedback on how well is performing each solution, being similar to the typical so-called cost-function. In principle, by guaranteeing all the targeted impedance levels, the drain efficiency of the transmitter will be enhanced in PBO operation[6]. Consequently, minimising the AM-PM distortion will be our primary goal. Thus, the fitness function will assess the $\angle H_n(j \cdot \omega_c)$ variation between the impedance levels. To quantify this parameter numerous definitions can be used, such as variance, normalised mean square error or unbiased mean square error. In this procedure we adopted the unbiased mean square error, which is the unbiased estimator of the population variance and is defined as

$$MSE_u = \frac{\sum_{i=1}^{N} (\overline{S} - S_i)^2}{N-1} \tag{5.6}$$

where S_i is the $i-$th population sample, $\overline{S}$ is the mean of the population and N the population size. The algorithm was also tested with variance and normalised mean square error, always achieving

[6]This assumption is not always valid, since the transformation ratio within the double π MNT also contributes to the total power losses.

convergence without significant impact on computational time nor solutions. Therefore, any of the previous parameters could have been used.

Assuming that we intend to conduct the design for n different impedance levels, the algorithm needs to secure that both the restraints are met for all the n impedance values and the minimisation of the fitness function is performed. Thus, to address this problem we propose a *parallel* like search procedure. The algorithm is structured so that each impedance level that we pretend to achieve, R_{d_n}, has its own dedicated swarm. Hence, for N different impedances, we will have N swarms performing a parallel search. However, to select the best combination of capacitors that ensure the best fitness function value, we need to combine information between the swarms. Thus, local repository is introduced, which works as a *memory repository*. This repository is updated in each iteration and has a maximum user specified size. As soon as the maximum size is reached, the new combination of capacitances to enter the repository occupies the oldest one spot. However, to ensure convergence, the current global best solution, S_{GB}, is always preserved inside the repository. Accordingly, to find the global best solution, we perform a combination between all the stored particles and select the one that minimises the fitness function. Thus, the computational cost to calculate all the combinations for N_1 different number of solutions with a maximum repository size equal to N_2 is ${N_2}^{N_1}$. Therefore, the number of combinations increases exponentially with the wanted number of impedance levels. This indicates that a trade-off must be established to achieve convergence in a reasonable amount of time. Although not explore here, the presented algorithm could be structured so that it could make used of multi-core architectures, both for the swarm position update and the best global solution search.

To guarantee satisfactory drain efficiency, the input impedance of the matching network at the fundamental frequency must be solely real, while ideally providing short-circuits at higher order harmonics. Thus, these two conditions need to be included in the algorithm restraints. It is worthy to note that the current algorithm version do not maximises the attained drain efficiency. To include this condition, a multi-objective version of the proposed algorithm is required. The restraints in use are stated as

$$\begin{cases} R_{d_n} \cdot (1-P_1) \leq \Re\{Z_n\} \leq R_{d_n} \cdot (1+P_1) & : f = f_c \\ R_{d_n} \cdot P_2 \geq |\Im\{Z_n\}| & : f = f_c \\ \Re\{Z_n\} \leq P_3 & : f = 2 \cdot f_c \\ |Z_{n_{2f}}| \leq |Z_{n_f}| \cdot P_4 & : f = f_c \end{cases} \tag{5.7}$$

where the first condition ensures that the real part of the impedance is sufficiently close to the wanted value, while the second one assures that the imaginary part is close to zero. The third and fourth conditions are related to the frequency response at the second harmonic. The third ensures that the real part is below a given threshold, P_3, and the last guarantees that the ratio between the fundamental and second harmonic impedance magnitude is also kept below a defined value. Through simulation the constant values were determined to be $P_1 = 0.1$, $P_2 = 0.075$, $P_3 = 0.1$ and $P_4 = 1.25$.

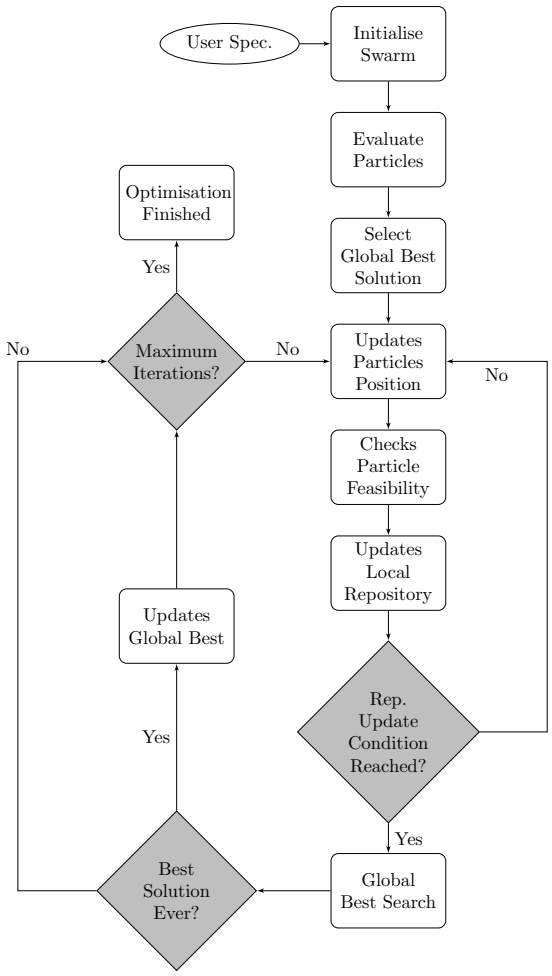


Figure 5.3: Proposed PSO based algorithm flowchart.

Figure 5.3 illustrates the high level flowchart of the proposed PSO based algorithm. It first takes as input the inductors specifications (L_1, Q_1, L_2, Q_2), the impedances that we pretend to achieve, the maximum number of iterations, the repository size and number of iterations to perform global best particle search. Then, all the particles for each one of the *sub-spaces*, i.e. swarms, must be initialised. The global best solution must be selected, only then we start the real optimisation process. From now one, every step updates the particles position and checks for their feasibility (restraints). If the restraints are not satisfied a penalty is added. As soon as the number of iterations to initialise the global search is reached, this process is initiated, performing combinations between all the particles contained in the local repository, updating then the global best solution. This process continues on and on, until the maximum number of iterations initially specified is achieved. A mutation operator was also employed to prevent convergence issues (e.g. avoiding being trapped in local minima) [91]. For a more detailed description, the set of MATLAB® files used to simulate the algorithm can be found in appendix B.1, guided by a short explanation.

5.2.1 Algorithm Evaluation

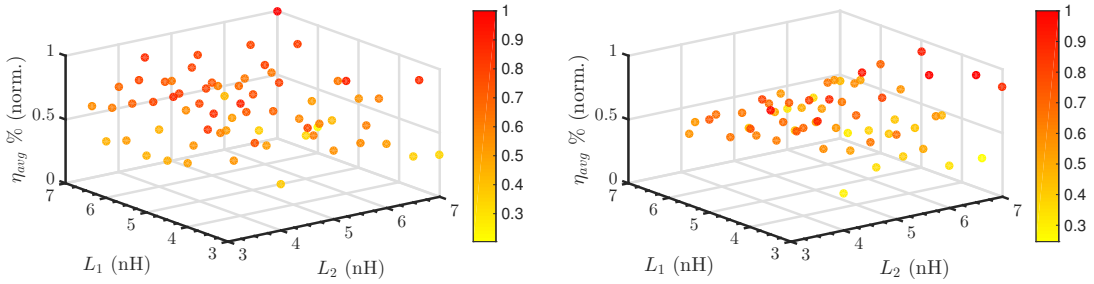


Figure 5.4: Average efficiency as a function of inductors L_1 and L_2 for: (a) package 0402 and (b) package 0201.

In order to validate the proposed approach, we firstly need to select L_1 and L_2 values. Based on CoilCraft inductor manufacturer and considering $Q_{bw} \approx 25$, we will run two sets of simulations where L_1 and L_2 are assorted between $L_{1,2} \in \{3\,\text{nH}\,;7\,\text{nH}\}$. It will also be assumed that the inductors values already account for the bond wire inductance (presumed to be $L_{bw} = 0.75\,\text{nH}$), being then the equivalent Q a function of Q_{ext} and Q_{bw}. The simulations will be carried out with inductors from package 0402 and 0201 (inch), where the corresponding quality factor of the total inductance, $L_{bw} + L_{ext}$, is presumed to vary between $25.1 - 44$ and $21 - 25.1$, respectively[7]. Figure 5.4 illustrates the simulation results assuming 3 impedance levels $R_1 = 10\,\Omega$, $R_2 = 20\,\Omega$ and $R_3 = 40\,\Omega$. The depicted average efficiencies are only assumed to be *true* if the three desired impedances were achieved while attaining the same input-output delay[8]. Moreover, η was calculated without the influence of the higher orders harmonics, being its purpose to serve as a mere FoM. Its calculation is based on linear principles, assuming an ideal current source imposing an ideal current like square-wave. Furthermore, the parasitics values are also included, being then possible to assess the transformation ratio effect on efficiency. Unfortunately, since the proposed topology is prone to harmonic content, their influence must be appraised. Left-sided figure is related to the package 0402 while the right-sided plot illustrates the package 0201. It is more than clear that by using the package 0402 a higher number of combinations leads to greater η_{avg}. This in turn provides higher flexibility at expense of a small increase in the total area. Moreover, the attained $\eta_{avg_{max}}$ is higher when using the 0402 package (higher Q_{ext}). Although the highest η values are generally found for $L_1 > L_2$, when accounting for the extra harmonic content we verify that the former condition leads to a stronger second harmonic in the drain voltage (lower C_1)[9], attaining lower efficiency and output power. Consequently, allowing a higher value of C_1

[7] This values were calculate using a linear regression with the lowest and highest external inductors quality factors. Afterwards, the equivalent Q was expressed accounting for the influence of the total bond wire inductance $2 \cdot L_{bw} \approx 1.5\,\text{nH}$ (i.e. it is assumed that the inductor is bonded back into the IC, as will be shortly illustrated).

[8] This condition was verified using the unbiased estimator of the population variance. Whenever this parameter present a value below a given threshold, the *true* condition is verified.

[9] In π based MNT this capacitance ideally short-circuits higher order harmonic content. Thus, if its value is sufficiently high, the transmitter should attain better performance.

mitigates the possible need for a second harmonic trap. Furthermore, low values of L_1 seem to attain higher drain efficiency[10]. Thus, the following set of simulations shall be conducted using inductors found in series 0402. $L_1 = 0.5\,\text{nH}$ will also be considered to investigate the algorithm and MNT performance under lower L_1 values.

Table 5.1: Inductors employed in the double π MNT.

Set	L_{ext_1}	Q_{ext_1}	L_{ext_2}	Q_{ext_2}	L_{bw}	Q_{bw}
1	1.914 nH	70.56	4.75 nH	62.5	1.5 nH	25
2	2.41 nH	63.12	4.75 nH	62.5	1.5 nH	25
3	0.50 nH*	30.73	2.41 nH	63.12	1.5 nH	25

* - Coilcraft inductor from package 0201.

Recalling the PSO based algorithm previously introduced, a set of MATLAB simulations will be carried out. Assuming the inductors values designated in table 5.1, the algorithm will try to find solutions that provide adequate performance for each one of the previously stated impedance values. Capacitors values are limited to $C_{1,2} \in [0;60\,\text{pF}]$ and $C_3 \in [0;30\,\text{pF}]$. It is worth noticing that the solution with the highest η_{avg} found in figure 5.4a, i.e. $L_1 = L_2 \approx 7\,\text{nH}$, is not considered here. Being the C_1 value considerably low (≈ 10 and $12\,\text{pF}$) a strong V_{ds_2} component will occur, thereby deteriorating the efficiency and output power[11]. Table 5.2 shows the solutions found by the algorithm as well as the algorithm theoretical drain efficiency. Capacitor C_1 was adjusted to account for the cascode output capacitance. As one can state, set 3 offers the best overall efficiency, however, also possessing the lowest C_1 value. This indicates that we should be expecting a higher second harmonic voltage component in opposition to the other two solutions.

Table 5.2: Capacitors values found by the algorithm for each one of the sets.

	Set 1				**Set 2**				**Set 3**			
$R_{opt}(\Omega)$	C_1 (pF)	C_2 (pF)	C_3 (pF)	η (%)	C_1 (pF)	C_2 (pF)	C_3 (pF)	η (%)	C_1 (pF)	C_2 (pF)	C_3 (pF)	η (%)
10	34.32	14.5	13.87	37	30.5	13.28	14.7	37.7	16.79	27.3	8.7	58.0
20	25.45	15.52	12.84	35	22.0	14.27	12.28	38.18	18.1	31.31	7.24	52.5
40	17.35	18.03	10.64	40.6	15.3	16.4	10.2	41.9	17.0	40.3	5.91	53

5.3 Simulation Results

Figure 5.5 portrays the final proposed digital transmitter architecture, already incorporating the double π TMNT. For the time being, the tunable capacitances will be considered ideal. Simulating the three sets in Cadence Virtuoso, we attained average efficiencies[12] of $\eta_1 = 37.3\%$, $\eta_2 = 34.3\%$ and $\eta_3 = 40.5\%$, while the transistors total width are $W_{T_1} = 890\,\mu\text{m}$, $W_{T_2} = 838\,\mu\text{m}$ and $W_{T_3} =$

[10] This was confirmed with simulations in Cadence SpectreRF environment. The exact causes of this behaviour were not object of study, but we suspect that it is related to a combination of both the transformation ratio within the MNT and the second harmonic influence.

[11] This situation was corroborated with simulations in Cadence SpectreRF.

[12] Calculated as the mean average of the peak efficiencies obtained in peak power and the two switching points.

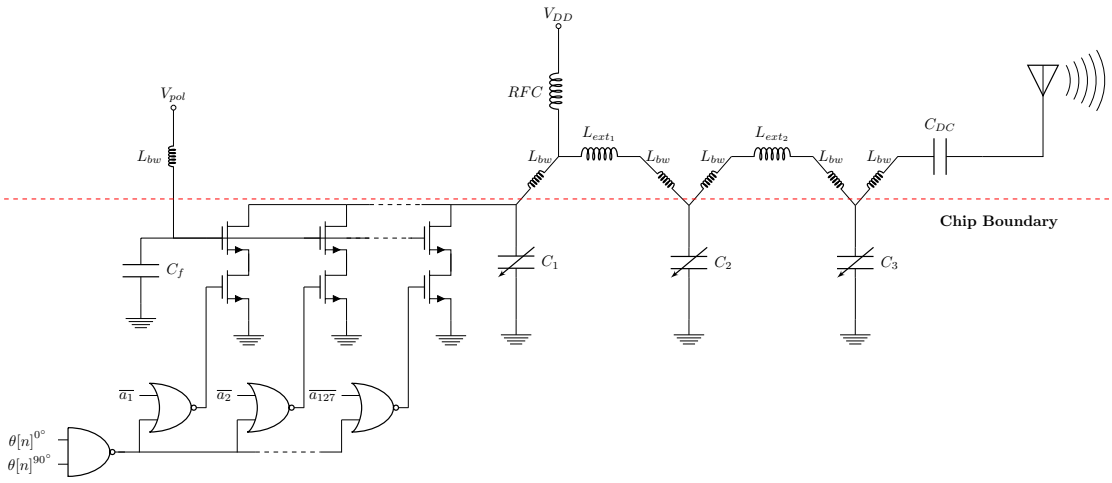
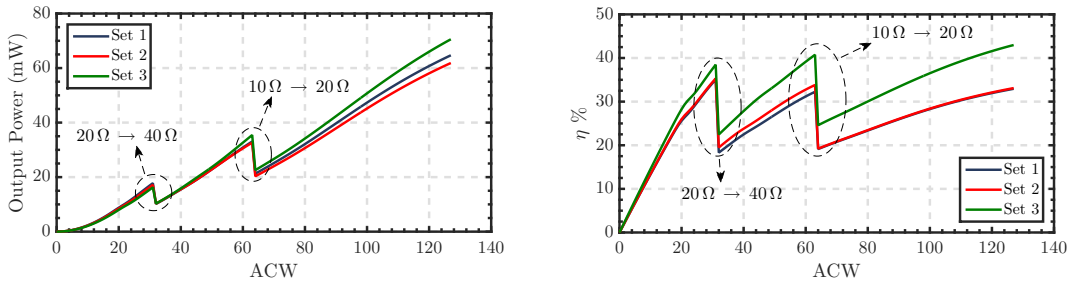


Figure 5.5: Proposed DRAC architecture with DLM.

711 µm[13]. Figure 5.6 portrays both the output power evolution and efficiency profiles for the 3 previously considered solutions. The achieved peak output power is $P_{rf_1} = 65\,\text{mW}$, $P_{rf_2} = 62\,\text{mW}$ and $P_{rf_3} = 70.5\,\text{mW}$. Despite the higher V_{ds_2} component, the set 3 outperforms the others two solutions, while demanding less area. Therefore, as already predicted by the algorithm FoM, set 3 presents best performance than the other two competitors.

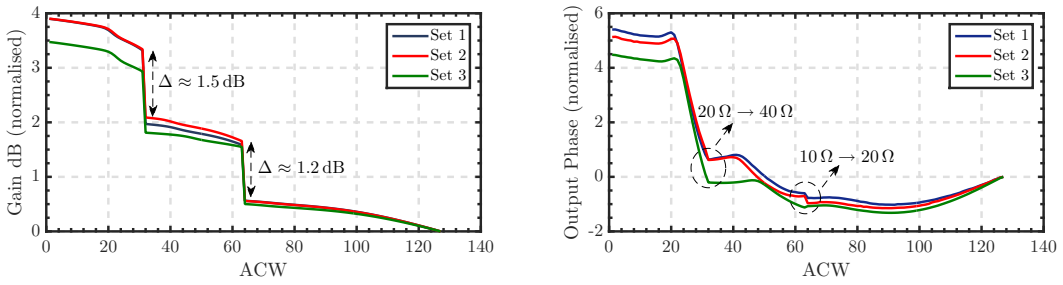
Figure 5.7 portrays the gain and phase variation as a function of ACW in the left and right sided figures, respectively. As already stated in chapter 5, adopting DLM to enhance PBO efficiency impairs the AM-AM system linearity. Figure 5.6a shows us the output power variation that occurs every time the MNT switches between the impedance levels. Whenever this switching action occurs, a large gain variation is introduced in the system, as stated in figure 5.7a. Although less severe, the same effect is possible to be observed in the phase evolution, where the phase variation (set 3) goes as high as 5.8°. Nevertheless, the phase and gain variation reported for set 3 are lower than in its counterparts. Regardless the AM-AM and AM-PM degradation, the attained PBO efficiency enhancement at 3 dB and 6 dB, i.e. at the switching points, is remarkably good.



(a) (b)

Figure 5.6: DLM effect for each one of the sets: (a) efficiency profile and (b) output power evolution.

[13]The maximum width was adjusted to guarantee a smooth AM-AM profile.



(a) (b)

Figure 5.7: DLM effect for each one of the sets: (a) gain variation and (b) phase evolution.

5.3.1 AM-AM Linearisation

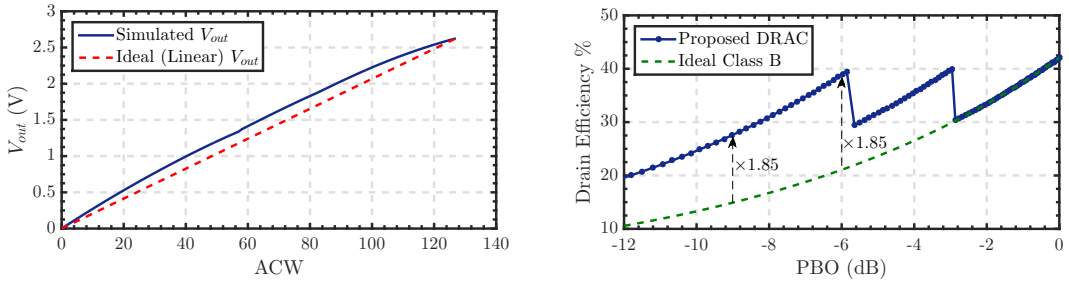
In [16] Ye *et al.* addressed the linearisation of a two level transformer based DLM by smoothing the AM response (BB domain). Since this work is being developed in the context of all-digital transmitters, adopting static DPD seems a reasonable choice. However, this approach has the downside of limiting the modulation accuracy by reducing the effective AM resolution (limits the BB interpolation) [16]. To overcome this issue, BB filtering and AM smoothing are performed. Analog based DLM designs [9, 18, 86] mitigate the AM-AM profile by dynamically adapting the PA biasing. Thus, dynamically compensating the unit current of each cascode unit, I_{unit}, might allow for a straightforward linearisation technique, without incurring in linearity losses.

Assuming that the output voltage is given by

$$V_{out} = 0.45 \cdot ACW \cdot I_{unit} \cdot R_{opt}(ACW) \tag{5.8}$$

it is easily seen that whenever the $R_{opt}(ACW)$ changes its value, an abrupt change in the output voltage is expected. However, if one allows a change in I_{unit} capable of balancing the drain resistance shift, a smoother characteristic should be attained. Whenever the tunable MNT switches between impedance levels, the region with efficiency enhancement presents the same output power as the points with higher ACW. Therefore, the linearisation must use this efficiency enhanced *region* to transmit the information. Thus, $I_{unit}(V_b(ACW))$[14] must be dynamically adjusted so that it achieves the desired compensation. Furthermore, by inspecting figure 5.7a we state that after each transition the evolution of the gain acquires a different profile (i.e. distinct slope). Hence, to achieve a continuous and smooth $V_{out}(ACW)$ profile we should also constraint the slope variation

[14] In here we use V_{pol} and V_b interchangeably to address the polarisation voltage applied to the cascode gate.



(a) (b)

Figure 5.8: Output voltage (a) and efficiency (b) after AM-AM linearisation.

of the output voltage, which is given by[15]:

$$\frac{\partial V_{out}(ACW)}{\partial ACW} = \begin{cases} 0.45\, I_{unit(V_{b_1})} R_1 & : ACW_2 < ACW \leq 127 \\ 0.45\, I_{unit(V_{b_2})} R_2 & : ACW_1 < ACW \leq ACW_2 \\ 0.45\, I_{unit(V_{b_3})} R_3 & : 0 \leq ACW \leq ACW_1 \end{cases} \tag{5.9}$$

Considering now ACW_1 and ACW_2, where $I_{unit_1}(V_{b_1})$, $I_{unit_2}(V_{b_2})$, R_1 and R_2 are the respective currents and impedances of each code word, we can state that the ideal conditions that guarantee no AM-AM linearity degradation are:

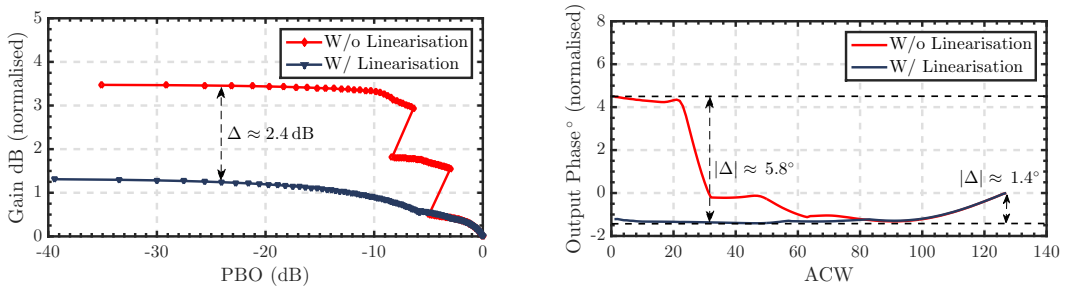
$$\begin{cases} V_{out}(ACW_1) = V_{out}(ACW_2) \\ \frac{\partial V_{out}(ACW_1)}{\partial ACW_1} = \frac{\partial V_{out}(ACW_2)}{\partial ACW_2} \end{cases} \quad \begin{cases} ACW_1 \cdot R_1\, I_{unit}(V_{b_1}) = ACW_2 \cdot R_2\, I_{unit}(V_{b_2}) \\ R_1\, I_{unit}(V_{b_1}) = R_2\, I_{unit}(V_{b_2}) \end{cases} \tag{5.10}$$

Thus, assuming that R_1 and R_2 are already defined as well as ACW_1 and ACW_2, V_{b_1} and V_{b_2} must be adjusted accordingly to ensure the same current ratio as R_1/R_2. This condition will ideally lead to no AM-AM distortion. Hence, adjusting the biasing voltage smooths the discontinuities and the slope of $\partial V_{out}/\partial ACW$ as well.

Figure 5.8 illustrates the output voltage and efficiency evolution under both DLM operation and AM-AM linearisation. The switching occurs now between $56-57$ and $81-82$, while the biasing voltage changes between 0.98 V, 1.17 V and 1.5 V, respectively. The $V_{out}(ACW)$ profile is considerably linear, exhibiting low degree of distortion. The observed distortion can be mainly attributed to the code dependent output impedance and the discrete nature of ACW[16]. Figure 5.8b presents us the PBO efficiency evolution. Considering the ideal class B operation, a remarkable efficiency enhancement of $\times 2.1/2.2$ is achieved at 6 dB and 9 dB, respectively. Additionally, even for deep PBO operation (i.e. 9 dB to 12 dB) the increment in efficiency stays above $\times 1.8$. Figure 5.9a illustrates the gain profile versus PBO, confirming then the effectiveness of the AM-AM linearisation. Figure 5.9b depicts now the phase evolution. Under AM-AM linearisation

[15] Despite the fact the DRAC operates in the discrete domain, expressing these conditions in the continuous case eases the representation.

[16] It complicates the exact matching conditions expressed in (5.10).



(a) (b)

Figure 5.9: Gain evolution as a function of the PBO (a) and phase evolution as a function of the ACW (b).

the phase profile is quite smoother, hence, achieving higher linearity. Moreover, the attained variation goes from $\approx 5.8°$ to $\approx 1.4°$, which further demonstrates the benefits of employ the AM-AM linearisation. Contrasting with the original situation, the $V_{out}(ACW)$ evolution is now kept approximately constant, condition that smooths the AM-PM profile.

Despite of this technique effectiveness in the AM-AM impairment, it usually relies on the use of off-chip dynamic supply voltage, burdening then the desired goal of a self-contained transmitter. Ideally, to take advantage of digital integration, techniques relying on digital control would be favourable. However, due to the presence of a relatively large capacitor at the cascode node (recall figure 5.5) employing current-mode techniques would limit the switching speed. Hence, voltage mode biasing must be used, where the biasing voltage would be digitally controlled. Hence, this type of linearisation can be suitable for mixed-signal integration. To decide between this mixed-signal technique or BB DPD, more variables must be taken into account, for instance additional power consumption, output noise or the technique effectiveness. This discussion is not addressed here by virtue of going beyond the scope of this dissertation.

5.3.2 Variable Capacitor

Variable capacitor presents it self as the key element to successfully build the intended dynamic MNT. The 130 nm process in use provides RF modelled MiM and metal-oxide-metal (MoM) capacitors as well as accumulation mode varactors. The selection of the right topology to implement the variable capacitance element needs to be deeply evaluated, since there are several crucial aspects involved here, namely occupied area, ON and OFF quality factors (Q_{ON} and Q_{OFF}), and linearity. Thus, the following sub-section is dedicated to a short review of several designs available as well as validating the best topology that meets our needs. All the following presented simulated results are derived from non-linear periodic-steady-state simulations (SpectreRF).

Varactors are widely employed in both DCOs and their analog counterparts [4] as part of the tunable capacitor element, considering that they usually present relatively high quality factors. Unfortunately, the effective capacitance at their terminals is a function of the actual voltage swing

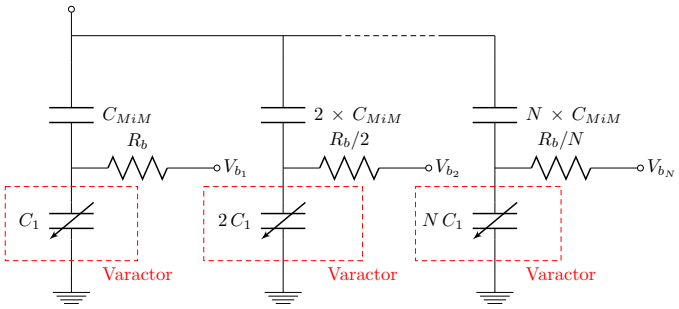


Figure 5.10: Tunable capacitor implementation based on MiM and accumulation mode varactor as proposed in [92].

plus dc biasing, which introduces non-linearities in the system that are highly undesirably when it comes to the design of highly linear RF front-ends.

Recently, several works proposed a variety of methods to overcome the non-linear behaviour of tunable capacitors either by using a combination of MiM and accumulation mode varactors, extra filtering or DPD. In [63] the author proposed the usage of a varactor along with two different matching networks that aimed to eliminate the extra harmonic content generated by the non-linear device (recall figure 3.9). The usage of two series matching network imposes the need of a higher number of passive devices, which leads to inherently higher losses, degrading de system efficiency. Chao *et al.* also presented in [25] a DPD scheme that intended to linearise the transmitter, solving then the non-linear behaviour through baseband control. Despite presenting good results, this approach makes even more complex the multi-mode transmitter implementation. In [92] the authors presented a CMOS based solution that combines MiM and accumulation mode varactors in order to achieve a satisfactory trade-off between tuning ratio and quality factor. Figure 5.10 depicts the basic schematic of the tunable element, which consists of a MiM capacitor stacked on the top of an accumulation mode varactor. By controlling the voltage applied to the bias resistor, R_b, between $+V_{DD}$ and $-V_{DD}$, it is possible to control the varactor region of operation, i.e. either in accumulation or inversion mode. However, the proposed solution only shows linear behaviour when the ac signal presents relatively small voltage swing. The desired ac voltage swing must not exceed a well defined range, otherwise the varactor enters in depletion region and presents an abrupt change in the capacitance, attaining non-linear operation. Furthermore, this solution is also impractical when we intend to implement large capacitances (e.g. $\geq 5\,\text{pF}$), since the MiM capacitor works as a bypass and needs to be much higher than the desired final capacitance value (typical rule of thumb dictates five to ten times larger).

MiM and MoM capacitors present extremely high linearity as well as high quality factors [93]. Although they are not as area efficient as varactors, which typically present $4-10\,\text{fF}/\mu\text{m}^2$ density versus $1-1.5\,\text{fF}/\mu\text{m}^2$ area density of MiM and MoMs (according to the foundry documentation), they appear as a more attractive solution to incorporate the variable capacitance element. Concerning the total occupied design area, this design will either exploit MiM capacitors with the highest density, i.e. $1\,\text{fF}/\mu\text{m}^2$ or MoM capacitors, which present $\approx 1.85\,\text{fF}/\mu\text{m}^2$ density. In order to access the topology with the best RF performance, both capacitors were simulated under RF

Table 5.3: Comparison of MiM and MoM capacitors provided by technology in use.

	Linearity ($\mathbf{I_{f_1}}$)$^{+}$	$\mathbf{I_{f_1}/I_{f_2}}$ (dB)*	**Capacitance**	**Quality Factor**$^{++}$	**Density** (fF/μm^2)
MiM	High	71 dB	3 pF	82	1
MoM	High	81.1 dB	3 pF	263	1.85

$^{+}$ - Obtained as fundamental current evolution as a function of sinusoidal voltage amplitude applied at capacitor terminals (1 GHz). Current shows no distortion with increasing voltage.
* - Ratio, defined as $20\log_{10}(I_{f_1}/I_{f_2})$, between fundamental and second harmonic current evolution for 3 V sinusoidal voltage amplitude at capacitor terminals (1 GHz).
$^{++}$ - Simulated using a sinusoidal voltage signal with 3 V amplitude (1 GHz).

voltage swing. Table 5.3 presents the measured features, such as linearity, harmonic generation and quality factor, for 3 pF MiM and MoM capacitors. The characteristic that best differentiates the two implementations is the attained quality factor at 1 GHz, which is clearly more favourable for MoM capacitors. Additionally, MoM capacitors do not need special masks in their fabrication process [94], which can lower the final production costs. Moreover, MoM based capacitor implementation is even more favourable for sub-micrometer nodes than MiM, since they can take advantage of technology shrinking, such as increasing number of metal layers and reduced space between metal lines, reducing even further the design area [93]. Being so, this design is going to explore the implementation of MoM based tunable capacitors.

Switched-capacitor array (SCA) appears as the most promising solution to achieve the desired goal [9, 69, 88] (recall figure 3.14). In order to accomplish a satisfactory quality factor as well as reliable device operation, great care must be taken when designing the SCA. As previously seen, MoM capacitors present a high quality factor, clearly indicating that its series resistance, R_{SC}, is remarkably small. Hence, the overall ON quality factor (Q_{ON}) of the switched capacitor will be dominated by the NMOS switching ON resistance [74], given by

$$R_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_T)} \tag{5.11}$$

where μ is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, $\frac{W}{L}$ the transistor aspect ratio and $V_{GS} - V_T$ the gate overdrive voltage (V_{OV}). To achieve the desired Q_{ON}, the transistor width must be set to satisfy the required R_{ON} that ensures the target quality factor, expressed as:

$$Q_{ON} = \frac{1}{\omega (R_{ON} + R_{SC}) C} \approx \frac{1}{\omega R_{ON} C} \tag{5.12}$$

However, as stated in [92], the switched capacitor also presents a finite quality factor while in their OFF state, mainly due to the substrate losses associated to the parasitic junction ac coupling. Moreover, while in OFF state the SC parasitic capacitance also needs to be taken into account when designing the complete SCA.

Other works, such as [37], [88] and [95], present enhanced techniques to implement CMOS based switches. As stated in [92, 95], triple well option minimises the OFF state losses as well as opens the way to implement body floating technique, which besides enhancing the power capabil-

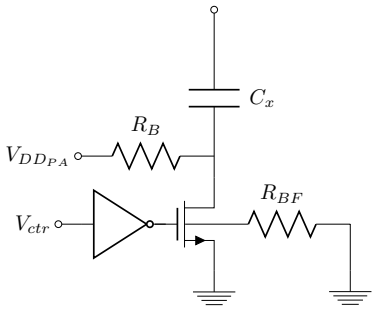


Figure 5.11: Switched-capacitor to be implemented in the proposed DLM architecture.

ity, also decreases the substrate coupling losses. Furthermore, body floating technique prevents the body to drain and source diffusion parasitic diodes to conduct. This aspect is essential since the drain voltage in the OFF state switch can become negative, which may cause the parasitic diode to conduct, increasing the losses, and ultimately, damaging the diffusion implants. Besides that, all the above works indicate that the SCA presents considerably good linearity[17] both in ON and OFF state.

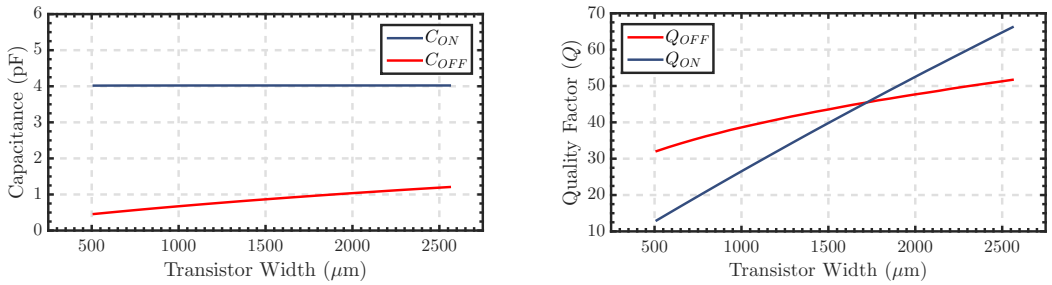
Figure 5.11 presents the selected approach that will be used to implement the SC. Thick gate NMOS transistor will be employed in order to sustain higher voltage swing without incurring in breakdown. This implementation was preferred over cascode or series divider topologies [37, 86] due to its higher simplicity and area saving. Unfortunately, since the BB works with 1.2 V, a level-shifter is required to interface with the SC [35]. For the time being, we will not address this implementation issue, which should present no major challenges. The driver will be considered a perfect inverter with zero resistance when switching between $V_{DD} = 2.2\,\mathrm{V}$ and ground. Furthermore, body-floating technique ($R_{FB} = 10\,\mathrm{k\Omega}$) will be adopted here to improve Q_{OFF}[18]. An additional resistance ($R_B = 20\,\mathrm{k\Omega}$) will be connected between V_{DD} and the transistor drain in order to fix the drain dc voltage. This in turn enhances the maximum voltage swing, preventing the turn-on of the parasitic drain-body diode. Whenever in the ON state this resistance presents negligible contribution to the dc total power consumption nor ac power dissipation[19].

Figure 5.12 depicts in the left the C_{ON} and C_{OFF} as a function of the total transistor width and in the right the ON and OFF quality factors, respectively. This design was conducted to achieve a $C_{ON} \approx 4\,\mathrm{pF}$. As a compromise between design area, complexity and driver requirements, we intend to achieve $Q_{ON} \approx 30$. In this range Q_{OFF} is always higher than Q_{ON}. Therefore, the total width will be chosen to satisfy $Q_{ON} \approx 30$, which is $W \approx 1100\,\mu\mathrm{m}$. Moreover, under the former conditions the SC attains a tuning ratio of ≈ 5.8. In the following set of simulations the tuning

[17] In fact, the linearity is dependent of the voltage swing. For the ON state there is almost no impact. However, when in the OFF state this condition needs to be assessed. Although not portrayed in this document, in the presented design, the voltage swing introduces no appreciable distortion.

[18] Although not depicted here, the Q_{OFF} improvement whenever we use resistances higher than $10\,\mathrm{k\Omega}$ is negligible. In fact, after $6\,\mathrm{k\Omega}$ the Q_{OFF} rapidly stabilizes, being quite insensible to the total width of the transistor. This was confirmed with Cadence Spectre PSS simulations.

[19] In OFF state, the resistor R_B will dissipate some amount of ac power. However, due to its high value the additional power loss is negligible and does not impacts the transmitter performance.



(a) (b)

Figure 5.12: ON and OFF width influence in: (a) total capacitance and (b) attained Q.

ratio will be assumed to vary between ≈ 5.8 and ≈ 6.0[20].

Considering nominal L_{bw} values, each one of the three different capacitors tanks was designed according the previously stated guidelines. However, the OFF state capacitance must not be neglected. Hence, in order to take into account its values, the problem can be stated as

$$\begin{bmatrix} C_{1_{HC}} \\ C_{1_{MC}} \\ C_{1_{LC}} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1/t_{tr} \\ 1 & 1/t_{tr} & 1/t_{tr} \end{bmatrix} \times \begin{bmatrix} C_{1_{P_1}} \\ C_{1_{P_2}} \\ C_{1_{P_3}} \end{bmatrix} \tag{5.13}$$

where $C_{1_{HC}}$, $C_{1_{MC}}$ and $C_{1_{LC}}$ represent the highest, intermediate and lowest C_1 capacitance values, while t_{tr} is the tuning ratio. $C_{1_{P_1}}$ is the fixed capacitance and $C_{1_{P_2}}$ and $C_{1_{P_3}}$ are the SCs. This procedure was also performed for capacitor tank C_2 and C_3. Table 5.4 presents the values for each one of the capacitors tank as well as the total transistor width. For tank 1 and 3 the tuning ratio was assumed to be $t_{tr} = 5.8$, while for tank 2 $t_{tr} = 6$. Obviously, this set os values does not take into account mismatch and other layout/fabrication issues that would affect the transmitter performance. Hence, to address this problem the capacitor tank could be partitioned into coarse and fine tuning, thus allowing BB digital control, similar as in a DCO [4]. Other issue that is not addressed here is the switching time, which is dependent of the driver size. Ideally, the switching action should be performed within the time that the DRAC is not conducting (i.e. during 75% of the period), ensuring less interference over the modulated signal. This indicates the need for synchronization between the RF phase modulated and switch control signals. In modern CMOS nodes this timing is fairly easy to perform [4]. Despite this subject being beyond the scope of this dissertation, this two identified issues should present no major problem in the implementation phase. The total active area occupied by the switches is $2084\,\mu m^2$, which represents only $0.002084\,mm^2$. The resistors[21] take less than $200\,\mu m^2$. Furthermore, the transistor area can be even lower if the drivers could switch between 0 and 3.3 V.

Assuming now the SCA previously presented, the proposed all-digital transmitter performance must now be evaluated. The switching points as well as the V_{pol} voltage values are kept the same as

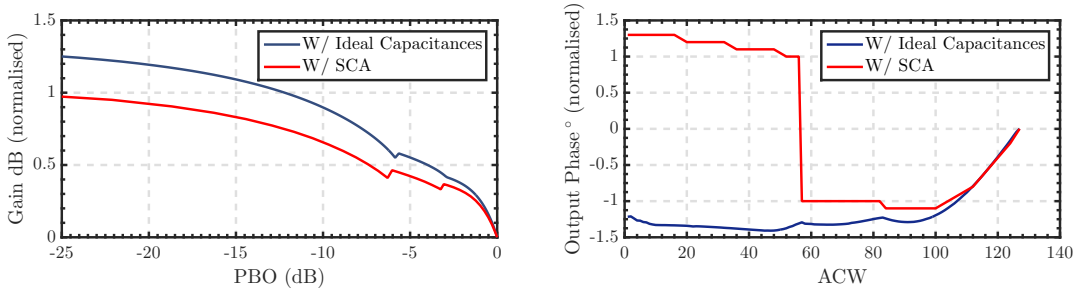
[20] This tuning ratio was verified trough simulation for low (≈ 3 pF) and high (≈ 8 pF) capacitance values, respectively.
[21] Resistors are performed with the high resistivity poly layer available in this process.

Table 5.4: Capacitors values found by the algorithm for each one of the tanks.

	Tank 1			**Tank 2**			**Tank 3**		
	$C_{1_{P_1}}$	$C_{1_{P_2}}$	$C_{1_{P_3}}$	$C_{2_{P_1}}$	$C_{2_{P_2}}$	$C_{2_{P_3}}$	$C_{3_{P_1}}$	$C_{3_{P_2}}$	$C_{3_{P_3}}$
C_{MoM} (pF)	16.52	0.275	1.35	24.7	4.85	10.87	5.55	1.62	1.76
NMOS Width (µm)	–	76.8	432	–	1368	3192	–	500	560

before. Figure 5.13 presents the gain and phase variation of the proposed transmitter, considering now non-ideal SCA. The left-sided figure portrays the gain variation, indicating that now we attain approximately less 0.3 dB when compared with the ideal capacitors case. However, observing the left-side graphic shows that the maximum phase variation under complete ACW excursion is now increased to $\approx 2.2^{\circ}$. Despite the verified small increase, the transmitter still attains considerably high static linearity.

Figure 5.14 illustrates the drain efficiency of the transmitter. The efficiency in peak power operation is lowered from 42.05% to 38.83%, while the output power is decremented from 70 mW to 65 mW. Moreover, the output power being radiated at the second and third harmonic are $P_{rf_2} = -25.94$ dBm and $P_{rf_3} = -50.64$ dBm, which results in $\Delta_{f_2} = 44.04$ dB and $\Delta_{f_3} = 68.77$ dB, respectively. Let us now analyse the PBO efficiency. The switching action of the TMNT presents peak efficiencies of 34.77% and 32.7%, against 39.95% and 39.48% with non-ideal and ideal SC, respectively. Through simulation we verified that the voltage swing at the switching points (i.e. ACW 56-57 and 81-82) is relatively away from the maximum admissible voltage swing. Hence, there is still room for improvements. The reported deviation is related to the simplified assumption we assumed when designing the SCA. Nevertheless, the efficiency enhancement at 3 dB, 6 dB and 9 dB is $\times 1.2$, $\times 1.6$ and $\times 1.6$ against the normalised class B operation[22]. Therefore, by applying manual tuning and a more strict SCA design approach, improvement of the overall performance is expected.



(a) (b)

Figure 5.13: Gain (a) and phase (b) variation profile under SCA.

[22] It is worthy to state that the class B is normalised-05-01 a 2016-08-08 to the peak efficiency of the transmitter with ideal SCA.

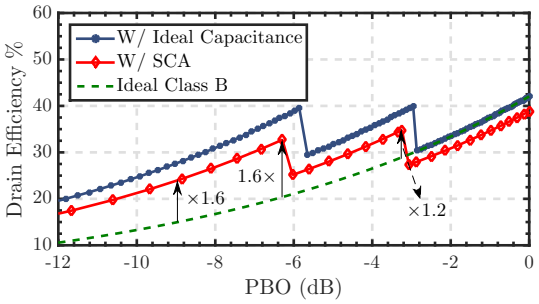


Figure 5.14: Drain efficiency comparison between ideal and non-ideal variable capacitors.

The simulations conducted in this chapter assumed $L_{bw} = 0.75\,\text{nH}$. Unfortunately, the bond wire inductance is known to be quite variable, only presenting a small fluctuations when the bonding is performed with specific machines. Therefore, it is imperative to assess the capability of the MNT to tolerate bond wire inductance variations. Hence, assuming the same external bond wires, the optimisation algorithm performance was tested under 25%, i.e. $L_{bw} = (1 \pm 0.25) \cdot 0.75\,\text{nH}$. All the corner cases were evaluated, resulting in 8 different scenarios. The algorithm shown convergence for all the considered cases. The output results were simulated[23] for the peak power operation, while the SCA was considered to be ideal. The attained peak power varied between 65 mW and 77 mW and the efficiency between 38% and 46%. Therefore, the proposed algorithm shows coverage for L_{bw} mismatch without excessive transmitter performance deterioration. Thus, by proper design and digital control, this approach can offer the possibility of adjusting the performance under process variations.

5.4 Conclusions

This chapter presented a discrete multi-level DLM topology that intends to enhance the PBO efficiency. To achieve the desired multi-level operation, an optimisation algorithm was introduced. The proof-of-concept transmitter was evaluated for 3-state DLM scenario. The reported peak output power and efficiency are 18.13 dBm and 38.83%, respectively. Furthermore, an efficiency enhancement over the idealised class B operation (normalised to ideal SCA operation) of $\times 1.2$ and $\times 1.6$ for 3 dB and $6/9$ dB, respectively, is attained. Therefore, the suitability to extend the PBO efficiency is demonstrated, showing promising metrics. These results indicate the possibility to extend even further the PBO efficiency enhancement range. To the best of the authors knowledge, this is the first CMOS all-digital transmitter reporting multi-level discrete DLM with minimum AM-PM distortion.

[23] The total transistor width was kept as $W_T = 711\,\mu\text{m}$.

Chapter 6

Conclusion

This dissertation discussed the concept and design of a reduced conduction angle switched-current source DRAC. To address the PBO performance, DLM was employed to achieve superior efficiency. Moreover, the conducted design ensures an easy interface with the BB domain. By implementing this in a circuit simulation environment, we achieved a truly digital compatible design, allowing effortless control of the proposed DPA. The following section details the dissertation outcome, while section 6.2 delineates different procedures and directions for future improvements.

6.1 Dissertation Outcomes

When targeting consumer electronics, low-power portable devices require low-cost solutions, nonetheless, still providing efficient performance. Hence, innovative solutions are on demand. By allowing seamless linear and efficient operation over a large dynamic range, multi-standard digital transmitters with enhanced performance can be successfully deployed. Thus, in this dissertation, a new DRAC topology based on a single ended SCS is introduced. A 25% duty-cycle is employed to allow, simultaneously, linear and efficient performance. However, the linearity is slightly degraded due to both CLM and soft-triode region alike. Nevertheless, the reported linearity is considerably satisfactory. Operating with $V_{DD} = 1.4\,\text{V}$ and considering $f_c = 2\,\text{GHz}$, the DRAC attained $P_{rf} = 17.92\,\text{dBm}$ and $\eta_{peak} = 43\%$. Moreover, the achieved bandwidth was $\approx$ 200MHz. A gain and phase variation of 1.1 dB and 1.1° are reported, respectively. Besides that, by resorting to digital capabilities of 130 nm CMOS node, a simple and low-power 25% duty-cycle clock converter and digital mixer are designed.

To mitigate the reported efficiency degradation in current-mode DPAs, we proposed a novel DLM methodology. To demonstrate the effectiveness of the delineated approach, a double π MNT is used. By resorting to external inductors, and relying on the support of an optimisation algorithm, a 3 state discrete DLM network is effectively simulated. Additionally, by constricting the input-output MNT delay, a arguably linear AM-PM static profile is achieved, while it is assumed that AM-AM amplitude non-linearity can be compensated recurring to non-expensive digital predistortion. The proof-of-concept design achieved a maximum output power of 18.13 dBm and a

peak efficiency of 38.83%. The efficiency enhancement at 3 dB, 6 dB, 9 dB and 12 dB PBO levels is $\times 1.2$, $\times 1.6$, $\times 1.6$ and $\times 1.6$, respectively, assuming the ideally normalised class B operation under a static MNT with ideal capacitance elements. Furthermore, the maximum gain variation over full dynamic range (DR$\approx$ 40 dB) is below 1.2 dB, while the phase variation is kept near 2.2°. By means of refining the designing methodology as well as resorting to manual tuning, the performance of the DRAC is expected to be enhanced.

As a result, the majority of the dissertation goals proposed in section 1.2 are accomplished. Additionally, the metrics drawn from this work demonstrate that multi-level DLM with minimum AM-PM distortion is viable in low power CMOS nodes.

6.2 Future Work

Despite the promising metrics, a more thorough analyses is mandatory. Firstly, an accurate model of the off-chip bond wire, PCB and inductors' interactions is needed. Secondly, the Q factor variation impact must be assessed as well. Although preliminary conclusions were drawn[1] using the proposed algorithm, a more precise evaluation must be conducted[2]. Thirdly, the layout should also be performed in order to verify the on-chip parasitics impact on the DRAC performance. Fourthly, the dynamic conditions of the DLM operation should be addressed as well. Finally, extending the efficiency enhancement to deeper PBO regions is an unquestionably attractive condition. As a result, incrementing the current solution to a higher number of states, e.g. 4 or 6 levels, could be the next step. In addition, another desired feature to be included in an all-digital transmitter is its ability to operate over a wide frequency range. Hence, addressing wideband frequency operation would open new possibilities for this topology. Consequently, the following guidelines can be used for prospective designs:

- Address the major implementations issues, such as layout, unforeseen parasitics' effects and AM-AM linearisation;
- Reformulation of the proposed algorithm to address wide frequency operation;
- Adapt the current DLM approach to support other digital architectures, for instance quadrature or outphasing digital transmitters;
- Deeply evaluate the PBO efficiency range operation;

[1] Although not presented in the previous chapters, the initial set of simulations indicate that we should expect no significant performance degradation for $\pm 25\%$ deviation around the nominal value.

[2] Obviously, this information must be aided by Cadence SpectreRF simulation results.

Appendix A

Appendix

A.1 Double π MNT Transfer Function

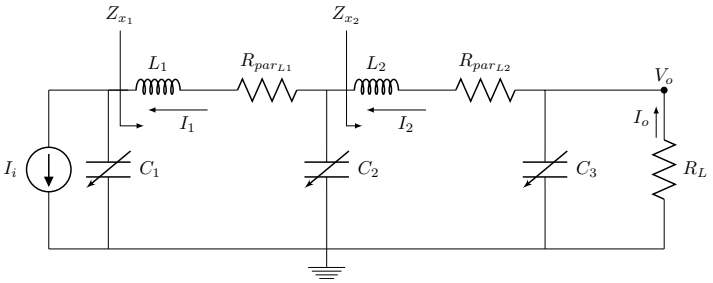


Figure A.1: Double π MNT with variable capacitors.

The relationship between the input current, I_i, and output current, I_o, can be easily calculated using the current divider principle. Current I_1 is defined as

$$I_1 = \frac{I_i X_{C_1}}{X_{C_1} + Z_{x_1}} \tag{A.1}$$

where the impedance is marked in figure A.1. The current I_2 is calculated in the same manner, leading to

$$I_2 = \frac{I_1 X_{C_2}}{X_{C_2} + Z_{x_2}} \tag{A.2}$$

where the impedance Z_{x_2} is also indicated in the same figure as previous. Finally, the output current is stated as

$$I_o = \frac{I_2 X_{C_3}}{X_{C_3} + R_L} \tag{A.3}$$

where X_{C_1}, X_{C_2} and X_{C_3} are the admittances of the impedance C_1, C_2 and C_3. Impedance Z_{x_2} is equal to

$$Z_{x_2} = \frac{j C_3 L_2 R_L \omega^2 + C_3 R_L R_{par_{L_2}} \omega + \omega L_2 - j R_L - j R_{par_{L_2}}}{R_L \omega C_3 - j} \tag{A.4}$$

while the impedance Z_{x_1} is defined as

$$Z_{x_1} = \frac{j C_2 L_1 Z_{x_2} \omega^2 + C_2 R_{par_{L_1}} Z_{x_2} \omega + \omega L_1 - j R_{par_{L_1}} - j Z_{x_2}}{Z_{x_2} \omega C_2 - j} \tag{A.5}$$

Thus, the transfer function can be defined as

$$H(j\omega) = \frac{I_o}{I_i} = \frac{X_{C_1} X_{C_2} X_{C_3}}{(Z_{x_1} + X_{C_1}) \cdot (Z_{x_2} + X_{C_2}) \cdot (X_{C_3} + R_L)} \tag{A.6}$$

where Z_{x_1} and Z_{x_2} are defined in (A.4)–(A.5). This procedure was adopted in the presented optimisation algorithm.

Appendix B

Appendix

B.1 Optimisation Algorithm Code

This chapter presents the algorithm detailed in the chapter 5. The body of the code is in the file `mainPSO.m`, where the PSO based search is performed. The restrainst check (feasibility) is verified by the file `restraintsCheck.m`. This function resorts to files `giniCoeffEval.m` and `phaseEval.m` to assist its undertaking. The memory update is conducted by the file `memoryHandler.m`, while the search for the best global solution is performed in `gBestSearch.m` . The FoM efficiency given by the algorithm is calculated in `MNT_Eff.m`, while the output-input phase relation is given by `transferFunctionPi_par.m`.

```
\\ mainPSO.m

%% MOPSO Matching Network

function mainMOPSO(L1, L2, maxItr, Rd, repSize, repUpdateStep, Q1, Q2)

% L1 is the first inductor
% L2 is the second inductor
% maxItr defines the maximum number of iterations
% repSize is the default size for the memory repository that is needed to
% cross check the data.
% Each Particle is comprosised by numSolutions

ind = 1;
strOut = sprintf('Output_BW_0_Lcomb_%d.txt',ind);

numVar = 3;                 % Number of variables of the MNT!
popSize = 100;              % Defines the size of population (Particles)
[~,dim] = size(Rd);
solDim = dim + 4;           % Rdesired complete lenght, taking into account
    the several needed fields
```

```
numDim = sum((Rd ~= 0)); % Defines the number of solutions per particle

if( numDim <= 0 )
disp('Array of the desired resistance values is not correct! It may
    contain zero number of elements!\n');
elseif( numDim > 8 )
disp('More that eight desired solutions is not acceptable!\n');
end

bw = [1]*2*pi*1e9; % Defines frequency spawn!
flagRep = ones(1,dim);   % Holds the oldest solution!

pBestWeight = 1.0;       % Personal best value importance
gBestWeight = 2.0;       % Global Best Value Importance
wmax = 0.4;              % Inertia values used to prevent fast attraction
    towards local minimums
wmin = 0.1;              % Minimum recommended value
var = 0;                 % Percetage by which inital boundaries are widen
    to ensure optimal space search
velocityParam = 1;       % Parameter by which velocity is divided
varginiReal = 0.1;       % Gini Coefficient for real part variation
varImpedance = 0.1;      % Coefficient that allows impedance variation
    around nominal value
unfeasibleThr = 20;      % After unfeasibleThr iterations, if some of the
    global solutions stays unfeasible, randomisation is done!
mutRateMax = 0.1;        % Defines the mutation rate; implemented to
    ensure diversity and avoid local minimums
mutRateMin = 0.01;

lbC1 = 0e-12;
ubC1 = 60e-12;
lbC2 = 0e-12;
ubC2 = 60e-12;
lbC3 = 0e-12;
ubC3 = 30e-12;

% Variables to be optimised

C1 = [lbC1, ubC1];
C2 = [lbC2, ubC2];
C3 = [lbC3, ubC3];

lbC1mut = lbC1*(1-var);
ubC1mut = ubC1*(1+var);
```

```
lbC2mut = lbC2*(1-var);
ubC2mut = ubC2*(1+var);

lbC3mut = lbC3*(1-var);
ubC3mut = ubC3*(1+var);

ubAll = [ubC1mut ubC2mut ubC3mut];
lbAll = [lbC1mut lbC2mut lbC3mut];

% Each Position should store 7 different values: C1 - C2 - C3 - GD -
% PhaseIn - PhaseOut - feasibilityFlag ---- 7 fields are needed!----

swarmPosition = zeros(popSize,numDim*7); % Creates position vector
swarmVelocity = zeros(popSize,numDim*7); % Creates velocity vector
swarmCurrCost = zeros(popSize,1); % Single Objective PSO
swarmPersonalCost = swarmCurrCost; % Cost of the Particle
swarm(:,1) = [1:1:popSize];     % Assigns numbers to each particle
swarmGlobalBestParticle = zeros(1,7*numDim);
memoryRepSize = repSize;        % Holds the total size of the repository
flagUpdate = zeros(1,solDim);  % Holds the flag that indicates the oldest
    solution in rep.


% Initialise positions
% -------------------------------------------------------------

for i = 0:numDim-1

swarmPosition(:,i*(7)+1) = lbC1mut + (ubC1mut-lbC1mut)*rand(popSize,1);
swarmPosition(:,i*(7)+2) = lbC2mut + (ubC1mut-lbC2mut)*rand(popSize,1);
swarmPosition(:,i*(7)+3) = lbC3mut + (ubC1mut-lbC3mut)*rand(popSize,1);
swarmPosition(:,i*(7)+4) = 0;
swarmPosition(:,i*(7)+5) = 0;
swarmPosition(:,i*(7)+6) = 0;
swarmPosition(:,i*(7)+7) = 0;

swarmGlobalBestParticle(i*(7)+1) = lbC1mut + (ubC1mut-lbC1mut)*rand;
swarmGlobalBestParticle(i*(7)+2) = lbC2mut + (ubC2mut-lbC2mut)*rand;
swarmGlobalBestParticle(i*(7)+3) = lbC3mut + (ubC3mut-lbC3mut)*rand;
swarmGlobalBestParticle(i*(7)+4) = 0;
swarmGlobalBestParticle(i*(7)+5) = 0;
swarmGlobalBestParticle(i*(7)+6) = 0;
swarmGlobalBestParticle(i*(7)+7) = 0;
```

```
end


for i = 1:popSize

[GD, phaseIn, phaseOut, flag] = restraintCheck(swarmPosition(i,:), bw,
    L1, L2, Rd, varImpedance, varginiReal, Q1, Q2);

for k = 0:numDim-1

swarmPosition(i,k*(7)+4) = GD(k+1);
swarmPosition(i,k*(7)+5) = phaseIn(k+1);
swarmPosition(i,k*(7)+6) = phaseOut(k+1);
swarmPosition(i,k*(7)+7) = flag(k+1);

end

end


% Selects leader
% ------------------------------------------------------

% Calculates costs and updates best personal known position!

for i = 1:popSize


[cost] = myCostFunction(swarmPosition(i,:));
swarmCurrCost(i) = cost;
swarmPersonalCost(i) = swarmCurrCost(i);
swarmPersonalBest(i,:) = swarmPosition(i,:);




end
memRepInitial = zeros(repSize,numVar*numDim);
[memoryRepUpdated, flagRep] = memoryHandler(swarmPosition, memRepInitial,
    repSize, flagRep, numDim, solDim, numVar);


sumInf = 0;
```

```
[GD, phaseIn, phaseOut, flag] = restraintCheck(swarmGlobalBestParticle,
    bw, L1, L2, Rd, varImpedance, varginiReal, Q1, Q2);

for k = 0:numDim-1

swarmGlobalBestParticle(k*(7)+4) = GD(k+1);
swarmGlobalBestParticle(k*(7)+5) = phaseIn(k+1);
swarmGlobalBestParticle(k*(7)+6) = phaseOut(k+1);
swarmGlobalBestParticle(k*(7)+7) = flag(k+1);

end


swarmGlobalBestCost = myCostFunction(swarmGlobalBestParticle);




% Initialises external repository
% ------------------------------------------------------
% Only needed in Multi-Objective Scenario


% Initialises velocity
% ------------------------------------------------------------


for i = 0:numDim-1

swarmVelocity(:,i*(7)+1) = (lbC1mut +
    (ubC1mut-lbC1mut)*rand(popSize,1))/velocityParam;
swarmVelocity(:,i*(7)+2) = (lbC2mut +
    (ubC1mut-lbC2mut)*rand(popSize,1))/velocityParam;
swarmVelocity(:,i*(7)+3) = (lbC3mut +
    (ubC1mut-lbC3mut)*rand(popSize,1))/velocityParam;

end


% Iteration Cycle
% ---------------------------------------------------------

itr = 0;
```

```
wInertia = wmax - (wmax - wmin)*itr/maxItr;
contMutGlobal = zeros(1,numDim);
itrGlobalSearch = 1;



while itr < maxItr

itr;
swarmGlobalBestCost;
swarmGlobalBestParticle;

%    sum((swarmPosition(:,7) == 1));
%    sum((swarmPosition(:,14) == 1));
%    sum((swarmPosition(:,21) == 1));

ID = fopen(strOut, 'w+');

for i = 0:numDim-1

Eff = MNT_Eff(swarmGlobalBestParticle(i*7+1:i*7+3), bw, L1, L2, Q1, Q2,
    i+1, Rd);
fprintf(ID, '%e %e %e %e %e %f %f %f %f %d\n',
    swarmGlobalBestParticle(i*7 + 1), swarmGlobalBestParticle(i*7 + 2),
    swarmGlobalBestParticle(i*7 + 3), L1, L2, swarmGlobalBestParticle(i*7
    + 4), swarmGlobalBestParticle(i*7 + 5), swarmGlobalBestParticle(i*7 +
    6),100*Eff, swarmGlobalBestParticle(i*7+7));

end
fclose(ID);

% Updates the position!
swarmPosition = swarmPosition + swarmVelocity;

% Checks restraints and calculates costs ---------------------------


% Calculates contraints, costs and checks boundaries violations
for i = 1:popSize

for k = 0:numDim-1

% Checks for boundary violation
if(swarmPosition(i,1+k*7) > ubC1mut)
swarmPosition(i,1+k*7) = ubC1mut;
```

```
elseif(swarmPosition(i,1+k*7) < lbC1mut)
swarmPosition(i,1+k*7) = lbC1mut;
end

if(swarmPosition(i,2+k*7) > ubC2mut)
swarmPosition(i,2+k*7) = ubC2mut;
elseif(swarmPosition(i,2+k*7) < lbC2mut)
swarmPosition(i,2+k*7) = lbC2mut;
end

if(swarmPosition(i,3+k*7) > ubC3mut)
swarmPosition(i,3+k*7) = ubC3mut;
elseif(swarmPosition(i,3+k*7) < lbC3mut)
swarmPosition(i,3+k*7) = lbC3mut;
end

end

[GD, phaseIn, phaseOut, flag] = restraintCheck(swarmPosition(i,:), bw,
    L1, L2, Rd, varImpedance, varginiReal, Q1, Q2);

for k = 0:numDim-1

swarmPosition(i,k*(7)+4) = GD(k+1);
swarmPosition(i,k*(7)+5) = phaseIn(k+1);
swarmPosition(i,k*(7)+6) = phaseOut(k+1);
swarmPosition(i,k*(7)+7) = flag(k+1);

end




end

% Updates Repository of Feasible Solutions!
[memoryRepUpdated, flagRep] = memoryHandler(swarmPosition,
    memoryRepUpdated, repSize, flagRep, numDim, solDim, numVar);



% Calculates costs and updates best personal known position!

for i = 1:popSize
```

```
[cost] = myCostFunction(swarmPosition(i,:));
swarmCurrCost(i) = cost;



if( (swarmCurrCost(i) < swarmPersonalCost(i)))
%pause;
% Only solutions that are feasible are accepted as personal
% best values!
for k = 0:numDim-1


if(swarmPosition(i,k*7+7) == 1)
swarmPersonalBest(i,(1+k*7):(7+k*7)) = swarmPosition(i,(1+k*7):(7+k*7));
end

end
swarmPersonalCost(i) = swarmCurrCost(i);

end


end

% Searches for the best Particle ever!!
allCheck = 0;
for k = 0:numDim-1

if(swarmGlobalBestParticle(k*7+7) == 1)
allCheck = allCheck + 1;
end

end

if(allCheck == numDim)

if( itrGlobalSearch == repUpdateStep )

[bestParticle, flagAssigned] = gBestSearch(swarmPosition,
    swarmGlobalBestParticle, memoryRepUpdated, numDim, bw, L1, L2, Rd,
    varImpedance, varginiReal, numVar, Q1, Q2);
swarmGlobalBestParticle = bestParticle;
swarmGlobalBestCost = myCostFunction(swarmGlobalBestParticle);
```

```
itrGlobalSearch = 0;

else
itrGlobalSearch = itrGlobalSearch + 1;
end

else
[bestParticle, flagAssigned] = gBestSearch(swarmPosition,
    swarmGlobalBestParticle, memoryRepUpdated, numDim, bw, L1, L2, Rd,
    varImpedance, varginiReal, numVar, Q1, Q2);

swarmGlobalBestParticle = bestParticle;

[GD, phaseIn, phaseOut, flag] = restraintCheck(swarmGlobalBestParticle,
    bw, L1, L2, Rd, varImpedance, varginiReal, Q1, Q2);

for k = 0:numDim-1

swarmGlobalBestParticle(k*(7)+4) = GD(k+1);
swarmGlobalBestParticle(k*(7)+5) = phaseIn(k+1);
swarmGlobalBestParticle(k*(7)+6) = phaseOut(k+1);
swarmGlobalBestParticle(k*(7)+7) = flag(k+1);

end


swarmGlobalBestCost = myCostFunction(swarmGlobalBestParticle);

end
```

```
% Updates the velocity


for i = 0:numDim-1

swarmVelocity(:,i*(numVar*2+1)+1) =
    wInertia*swarmVelocity(:,i*(numVar*2+1)+1).*rand(popSize,1) + ...
pBestWeight*(swarmPersonalBest(:,i*(numVar*2+1)+1) -
    swarmPosition(:,i*(numVar*2+1)+1)).*rand(popSize,1) + ...
```

```
gBestWeight*(swarmGlobalBestParticle(i*(numVar*2+1)+1).*ones(popSize,1) -
    swarmPosition(:,i*(numVar*2+1)+1)).*rand(popSize,1);

swarmVelocity(:,i*(numVar*2+1)+2) =
    wInertia*swarmVelocity(:,i*(numVar*2+1)+2).*rand(popSize,1) + ...
pBestWeight*(swarmPersonalBest(:,i*(numVar*2+1)+2) -
    swarmPosition(:,i*(numVar*2+1)+2)).*rand(popSize,1) + ...
gBestWeight*(swarmGlobalBestParticle(i*(numVar*2+1)+2).*ones(popSize,1) -
    swarmPosition(:,i*(numVar*2+1)+2)).*rand(popSize,1);

swarmVelocity(:,i*(numVar*2+1)+3) =
    wInertia*swarmVelocity(:,i*(numVar*2+1)+3).*rand(popSize,1) + ...
pBestWeight*(swarmPersonalBest(:,i*(numVar*2+1)+3) -
    swarmPosition(:,i*(numVar*2+1)+3)).*rand(popSize,1) + ...
gBestWeight*(swarmGlobalBestParticle(i*(numVar*2+1)+3).*ones(popSize,1) -
    swarmPosition(:,i*(numVar*2+1)+3)).*rand(popSize,1);

end



% Increments the counter, updates mutation rate and inertia

itr = itr + 1;
mutationRate = mutRateMax - (mutRateMax - mutRateMin)*itr/maxItr;
wInertia = wmax - (wmax - wmin)*itr/maxItr;


% Conts the number of cycles in each one of the possible GLOBAL solutions
% stays unfeasible
for k = 0:numDim-1

if(swarmGlobalBestParticle(k*7+7) == 0)
contMutGlobal(k+1) = contMutGlobal(k+1) + 1;
end

% If the count number exceeds a threshold, we should randomise it!
if(contMutGlobal(k+1) >= unfeasibleThr)

swarmGlobalBestParticle(k*(7)+1) = lbC1mut + (ubC1mut-lbC1mut)*rand;
swarmGlobalBestParticle(k*(7)+2) = lbC2mut + (ubC2mut-lbC2mut)*rand;
swarmGlobalBestParticle(k*(7)+3) = lbC3mut + (ubC3mut-lbC3mut)*rand;
```

```
contMutGlobal(k+1) = 0;

[GD, phaseIn, phaseOut, flag] = restraintCheck(swarmGlobalBestParticle,
    bw, L1, L2, Rd, varImpedance, varginiReal, Q1, Q2);

for k = 0:numDim-1

swarmGlobalBestParticle(k*(7)+4) = GD(k+1);
swarmGlobalBestParticle(k*(7)+5) = phaseIn(k+1);
swarmGlobalBestParticle(k*(7)+6) = phaseOut(k+1);
swarmGlobalBestParticle(k*(7)+7) = flag(k+1);

end


swarmGlobalBestCost = myCostFunction(swarmGlobalBestParticle);
end

end



% Performs random mutations
indMut = randperm(popSize, round(popSize*mutationRate));
sz = size(indMut);
indx = 1;
while(indx <= sz(2))

for i = 0:numDim-1

swarmPosition(indMut(indx), i*(7)+1) = lbC1mut + (ubC1mut-lbC1mut)*rand;
swarmPosition(indMut(indx), i*(7)+2) = lbC2mut + (ubC2mut-lbC2mut)*rand;
swarmPosition(indMut(indx), i*(7)+3) = lbC3mut + (ubC3mut-lbC3mut)*rand;

end
indx = indx + 1;

end







end
```

```
swarmGlobalBestParticle;




end
```

```
\\ gBestSearch.m

function [particleBest, assignedParticle] = gBestSearch(particleSwarm,
    swarmGB, memoryRepUpdated, numDim, bw, L1, L2, Rd, varImpedance,
    varginiReal, numVar, Q1, Q2)


[dimx, dimy] = size(particleSwarm); % Checks the matrix dimension
assignedParticle = zeros(dimy/7);
particleBest = zeros(1,dimy);
feas{1,(dimy/7)} = zeros(dimx, dimy);



for k = 0:(dimy/7-1)

if(swarmGB(k*7+7) == 0)

check(k+1) = 1;
feas{1,k+1} = particleSwarm((particleSwarm(:,k*7+7) == 1),:);



else

particleBest((k*7+1):(k*7+3)) = swarmGB((k*7+1):(k*7+3));
check(k+1) = 0;

end
```

```
end


if( (sum(check) > 0) )          % If sum(check) is greater than 0, then I
    need to check first for dym/7 feasible solutions!

% Searches for all feasibles!

for k = 0:(dimy/7-1)

if( ((1-isempty(feas{1,k+1})) == 1) && (check(k+1) == 1) ) % If exists
    one feasible, it will be assigned to the gBEST!
assignedParticle(k+1) = 1;
particleBest((k*7+1): (k*7+3)) = feas{1,k+1}(1,(k*7+1):(k*7+3));

else
assignedParticle(k+1) = 0;
particleBest((k*7+1): (k*7+3)) = swarmGB((k*7+1):(k*7+3));
end

end

else

% Complete Search Algorithm through combinations!
% This way efficient parallel search is performed!
loopForSize = ones(1,8);
loopFlag = zeros(1,8);

[dimx, dimy] = size(memoryRepUpdated);

for k = 0:(numDim-1)

%for b = 0:(dimx-1)

%val(1:dimx,1) = b+1;
if( isempty(memoryRepUpdated(:,(numVar*k+1):(numVar*k+3))) == 0)
feas{k+1} = memoryRepUpdated(:,(numVar*k+1):(numVar*k+3));

m = find(memoryRepUpdated(:,(numVar*k+1)) == 0);
if( isempty(m) == 1)
[loopForSize(k+1), ~] =
    size(memoryRepUpdated(:,(numVar*k+1):(numVar*k+3)));
loopFlag(k+1) = 1;
else
```

```
[loopForSize(k+1), ~] =
    size(memoryRepUpdated(:,(numVar*k+1):(numVar*k+3)));
loopForSize(k+1) = loopForSize(k+1) - numel(m);
loopFlag(k+1) = 1;
m = 0;
end
end

%end

end

% Adds the global best Particle to the Rep!
% This ensures that only solutions with lower cost that the
% current GB are added to the best known position!

for k = 0:(numDim-1)

feas{k+1}(loopForSize(k+1)+1,:) = swarmGB((k*7+1):(k*7+3));
loopForSize(k+1) = loopForSize(k+1) + 1;


end



dimensionComb = loopForSize(1);
for k = 2:numDim
dimensionComb = dimensionComb*loopForSize(k);
end

swarmComb = zeros(dimensionComb, numDim*7);

% Performs the necessary combinations!
ind = 1;
for a1 = 0:loopForSize(1)-1

for a2 = 0:loopForSize(2)-1

for a3 = 0:loopForSize(3)-1

for a4 = 0:loopForSize(4)-1

for a5 = 0:loopForSize(5)-1
```

```
for a6 = 0:loopForSize(6)-1

for a7 = 0:loopForSize(7)-1

for a8 = 0:loopForSize(8)-1

if( loopFlag(8) > 0 )

swarmComb(ind,:) = [feas{1}(a1+1,:), zeros(1,4), feas{2}(a2+1,:),
    zeros(1,4), feas{3}(a3+1,:), zeros(1,4), feas{4}(a4+1,:), zeros(1,4),
    feas{5}(a5+1,:), zeros(1,4), feas{6}(a6+1,:), zeros(1,4),
    feas{7}(a7+1,:), zeros(1,4), feas{8}(a8+1,:), zeros(1,4)];

elseif( loopFlag(7) > 0 )

swarmComb(ind,:) = [feas{1}(a1+1,:), zeros(1,4), feas{2}(a2+1,:),
    zeros(1,4), feas{3}(a3+1,:), zeros(1,4), feas{4}(a4+1,:), zeros(1,4),
    feas{5}(a5+1,:), zeros(1,4), feas{6}(a6+1,:), zeros(1,4),
    feas{7}(a7+1,:), zeros(1,4)];

elseif( loopFlag(6) > 0 )

swarmComb(ind,:) = [feas{1}(a1+1,:), zeros(1,4), feas{2}(a2+1,:),
    zeros(1,4), feas{3}(a3+1,:), zeros(1,4), feas{4}(a4+1,:), zeros(1,4),
    feas{5}(a5+1,:), zeros(1,4), feas{6}(a6+1,:), zeros(1,4)];

elseif( loopFlag(5) > 0 )

swarmComb(ind,:) = [feas{1}(a1+1,:), zeros(1,4), feas{2}(a2+1,:),
    zeros(1,4), feas{3}(a3+1,:), zeros(1,4), feas{4}(a4+1,:), zeros(1,4),
    feas{5}(a5+1,:), zeros(1,4)];

elseif( loopFlag(4) > 0 )

swarmComb(ind,:) = [feas{1}(a1+1,:), zeros(1,4), feas{2}(a2+1,:),
    zeros(1,4), feas{3}(a3+1,:), zeros(1,4), feas{4}(a4+1,:), zeros(1,4)];

elseif( loopFlag(3) > 0 )

swarmComb(ind,:) = [feas{1}(a1+1,:), zeros(1,4), feas{2}(a2+1,:),
    zeros(1,4), feas{3}(a3+1,:), zeros(1,4)];

elseif( loopFlag(2) > 0 )
```

```
swarmComb(ind,:) = [feas{1}(a1+1,:), zeros(1,4), feas{2}(a2+1,:),
    zeros(1,4)];

elseif( loopFlag(1) > 0 )

swarmComb(ind,:) = [feas{1}(a1+1,:), zeros(1,4)];

end

ind = ind + 1;


end
end
end
end
end
end
end
end



[dimxfinal, dimyfinal] = size(swarmComb);
costComb = zeros(1,dimxfinal);
% Performs the evaluation cicle!

for i = 1:dimxfinal

[GD, phaseIn, phaseOut, flag] = restraintCheck(swarmComb(i,:), bw, L1,
    L2, Rd, varImpedance, varginiReal, Q1, Q2);

for k = 0:numDim-1

swarmComb(i, k*(7)+4) = GD(k+1);
swarmComb(i, k*(7)+5) = phaseIn(k+1);
swarmComb(i, k*(7)+6) = phaseOut(k+1);
swarmComb(i, k*(7)+7) = flag(k+1);

end


costComb(i) = myCostFunction(swarmComb(i,:));
```

```
end




[~, ind] = min(costComb);
particleBest = swarmComb(ind,:);




end

end
```

```
\\ giniCoeffEval.m

%% Function that evaluates Gini Coefficient



function [realG] = giniCoeffEval(swarmPos, bw, L1, L2, Rdesired, var, Q1,
    Q2)



ratio = 0.075;
XC1 = 1./(j*bw*swarmPos(1));
XC2 = 1./(j*bw*swarmPos(2));
XC3 = 1./(j*bw*swarmPos(3));
XL1 = j*bw*L1;
XL2 = j*bw*L2;

Rpar1 = (bw*L1)/Q1;
Rpar2 = (bw*L2)/Q2;
Z1 = (XC3*50)./(XC3 + 50) + XL2 + Rpar2;
Z2 = (XC2.*Z1)./(XC2 + Z1) + XL1 + Rpar1;
Z3 = (XC1.*Z2)./(XC1 + Z2);

XC11 = 1./(j*2*bw*swarmPos(1));
XC22 = 1./(j*2*bw*swarmPos(2));
XC33 = 1./(j*2*bw*swarmPos(3));
XL11 = j*2*bw*L1;
```

```
XL22 = j*2*bw*L2;

Rpar1 = (2*bw*L1)/Q1;
Rpar2 = (2*bw*L2)/Q2;
Z11 = (XC33*50)./(XC33 + 50) + XL22 + Rpar2;
Z22 = (XC22.*Z11)./(XC22 + Z11) + XL11 + Rpar1;
Z33 = (XC11.*Z22)./(XC11 + Z22);



% Check Real and Imaginary parts values!
Rmean = mean(real(Z3));
maxImg = max(imag(Z3));
minImg = min(imag(Z3));



check1 = (Rdesired*(1-var) <= Rmean);
check2 = (Rmean <= Rdesired*(1+var));
check3 = (abs(minImg) <= Rdesired*ratio);
check4 = (abs(maxImg) <= Rdesired*ratio);
check5 = (max(real(Z33)) < 0.1);
check6 = (max(abs(Z33)./(max(abs(Z3)))) <= 1.25);
check7 = (max(imag(Z33)) <= 0);

if( ((check1 == 1) && (check2 == 1)) && (check4 == 1) && (check3 == 1) &&
    (check5 == 1) && (check6 == 1) && (check7 == 1))

realG = 0.01;


else
realG = 10; % Penalty


end






end
```

\\ memoryHandler.m

```
function [memoryRepUpdated, flagUpdated] = memoryHandler(swarm,
    memoryRep, repDim, flagRep, numDim, particleDim, numVar)


memoryRepUpdated = memoryRep;


for i = 0:numDim-1

solutions{i+1} = swarm((swarm(:,i*7+7) == 1),(i*7+1):(i*7+3));

end

% Solutions now holds the newest feasible solutions to enter the
% memoryRep!!

k = 1;
while ( k <= numDim )

sz = size(solutions{k});


if(sz(1) > 0)
% Data To Enter the Rep!!
solEnter = 1;

while(solEnter <= sz(1))


memoryRepUpdated(flagRep(k),(((k-1)*numVar) + 1):(((k-1)*numVar)+numVar))
    = solutions{k}(solEnter,1:3);


if(flagRep(k) == repDim)

flagRep(k) = 1;

else

flagRep(k) = flagRep(k) + 1;

end
solEnter = solEnter + 1;
```

```
end

end

k = k + 1;

end

flagUpdated = flagRep;


end
```

```
\\ MNT_Eff.m

function Eff = MNT_Eff(Caps, bw, L1, L2, Q1, Q2, indx, Ropt)

C1 = Caps(1);
C2 = Caps(2);
C3 = Caps(3);
[~,indy] = size(bw);
wc = bw(ceil(indy));
RL1 = (wc*L1)/(Q1);
RL2 = (wc*L2)/(Q2);
Rout = 50;
I_drain = (2.2-0.45)/(Ropt(indx));

XC1 = 1./(j*wc*C1);
XC2 = 1./(j*wc*C2);
XC3 = 1./(j*wc*C3);
XL1 = j*wc*L1;
XL2 = j*wc*L2;
Rpar1 = (wc*L1)/Q1;
Rpar2 = (wc*L2)/Q2;

%%% Current Divider!
Z1 = (XC3*50)./(XC3 + 50) + XL2 + Rpar2;
Z2 = (XC2.*Z1)./(XC2 + Z1) + XL1 + Rpar1;

Iout1 = (XC1*I_drain)/(XC1 + Z2);
Iout2 = (XC2*Iout1)/(XC2 + Z1);
IoutFinal = (XC3*Iout2)/(XC3+Rout);

Pout = 0.5*Rout*real(IoutFinal*conj(IoutFinal));
```

```
%%%


Pdc = 2.2*(I_drain/0.45)/4;


Eff = Pout/Pdc;
```

```
\\ myCostFunction.m

%% Function that evaluates costs



function cost = myCostFunction(pos)

[dimx, dimy] = size(pos);

diffPhaseIn = 0;
diffPhaseOut = 0;
diffGD = 0;
penalty = 0;
kpenalty = 10000;

% Defining the weight constants!


% Phase In (related to output flatness)
k2 = 10;        % Phase Out (related to phase discontinuities)
% Related to Group Delay likelihood

for i = 0:(dimy/7 - 1)

PhaseOut(i+1) = pos(6+i*7);
if( pos(i*7+7) == 1 )
penalty = penalty + 0;
else
penalty = penalty + 1;
end

end
```

```
meanPhaseOut = mean(PhaseOut);
msePhaseOut = sum(((meanPhaseOut-PhaseOut).^2))/(dimy/7 - 1);
cost = k2*msePhaseOut + penalty*kpenalty;



end
```

```
\\ phaseEval.m

%% Function that evaluates the Groud Delay and byy of each solution
    sub-set

function [GD, bbyOut, bbyIn] = phaseEval(swarmPos, bw, L1, L2, Q1, Q2)




XC1 = 1./(j*bw*swarmPos(1));
XC2 = 1./(j*bw*swarmPos(2));
XC3 = 1./(j*bw*swarmPos(3));
XL1 = j*bw*L1;
XL2 = j*bw*L2;

Z1 = (XC3*50)./(XC3+50) + XL2;
Z2 = (Z1.*XC2)./(Z1 + XC2) + XL1;
Z3 = (Z2.*XC1)./(Z2 + XC1);
phaseResponse = phase(Z3)*180/pi;

yPhase = transferFunctionPi_par(swarmPos(1), swarmPos(2), swarmPos(3),
    L1, L2, bw, Q1, Q2);


GD = +666;
bbyIn = 0;
bbyOut = yPhase*180/pi;




end
```

```
\\ restraintCheck.m

function [GD, phaseIn, phaseOut, flag] = feasibilityCheck(particle, bw,
    L1, L2, Rd, varImp, varginiReal, Q1, Q2)


sz = size(particle);

GD = zeros(1,sz(2));
phaseIn = zeros(1,sz(2));
phaseOut = zeros(1,sz(2));
flag = zeros(1,sz(2));
giniReal = zeros(1,sz(2));


for k = 0:sz(2)/7-1

[GD(k+1), phaseOut(k+1), phaseIn(k+1)] =
    phaseEval(particle((1+k*7):(3+k*7)), bw, L1, L2, Q1, Q2);
[giniReal(k+1)] = giniCoeffEval(particle((1+k*7):(3+k*7)), bw, L1, L2,
    Rd(1+k), varImp, Q1, Q2);

if( (giniReal(k+1) < varginiReal) && (GD(k+1) > 0) )

flag(k+1) = 1;    % Feasible Solution!

else

flag(k+1) = 0;    % Non-feasible Solution!

end


end




end
```

```
\\ transferFunctionPi_par.m

function phaseOut_Parasitics = transferFunctionPi_par(C1, C2, C3, L1, L2,
    w, Q1, Q2)
```

```
[indx,indy] = size(w);
wc = w(ceil(indy));
I_drain = 1;
Rout = 50;

XC1 = 1./(j*wc*C1);
XC2 = 1./(j*wc*C2);
XC3 = 1./(j*wc*C3);
XL1 = j*wc*L1;
XL2 = j*wc*L2;
Rpar1 = (wc*L1)/Q1;
Rpar2 = (wc*L2)/Q2;

Z1 = (XC3*50)./(XC3 + 50) + XL2 + Rpar2;
Z2 = (XC2.*Z1)./(XC2 + Z1) + XL1 + Rpar1;

Iout1 = (XC1*I_drain)/(XC1 + Z2);
Iout2 = (XC2*Iout1)/(XC2 + Z1);
IoutFinal = (XC3*Iout2)/(XC3+Rout);

phaseOut_Parasitics = phase(IoutFinal);
```

Bibliography

[1] "How the 'Internet of Things' will impact consumers, businesses, and governments in 2016 and beyond," http://www.businessinsider.com/how-the-internet-of-things-market-will-grow-2014-10, accessed: 2016-02-07.

[2] F. Ghannouchi, "Power amplifier and transmitter architectures for software defined radio systems," *IEEE Magazine of Circuits and Systems (CS'2010)*, vol. 10, no. 4, pp. 56–63, Nov 2010.

[3] "Samsung - F900 Washing Machine with ecobubble, 12 kg," http://www.samsung.com/uk/consumer/home-appliances/laundry/washing-machine/WF12F9E6P4W/EU, accessed: 2016-02-07.

[4] R. Staszewski, J. Wallberg, S. Rezeq, C.-M. Hung, O. Eliezer, S. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M.-C. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, "All-digital PLL and transmitter for mobile phones," *IEEE Journal of Solid-State Circuits (SSC'2005)*, vol. 40, no. 12, pp. 2469–2482, Dec 2005.

[5] P. Zampardi, "Will CMOS amplifiers ever Kick-GaAs?" in *IEEE Custom Integrated Circuits Conference (CICC'2010)*, Sep 2010, pp. 1–4.

[6] E. McCune, "A Technical Foundation for RF CMOS Power Amplifiers: Part 1: Key Power Amplifier Issues," *IEEE Solid-State Circuits Magazine (SSCM'2015)*, vol. 7, no. 3, pp. 81–85, Summer 2015.

[7] R. Staszewski, "Digital RF and digitally-assisted RF (invited)," in *2011 IEEE International Symposium on Radio-Frequency Integrated Technology (RFIT'2011)*, Nov 2011, pp. 9–16.

[8] "Simulating CDF for Peak to Average Power Ratio for OFDM," http://www.mathworks.com/matlabcentral/fileexchange/19190-simulating-cdf-of-peak-to-average-power-ratio-for-ofdm, accessed: 2016-02-07.

[9] Y. Yin, X. Yu, Z. Wang, and B. Chi, "An Efficiency-Enhanced Stacked 2.4-GHz CMOS Power Amplifier With Mode Switching Scheme for WLAN Applications," *IEEE Transactions on Microwave Theory and Techniques (MTT'2015)*, vol. 63, no. 2, pp. 672–682, Feb 2015.

[10] "IEEE 802.11a Standard," http://standards.ieee.org/getieee802/download/802.11a-1999.pdf, accessed: 2016-02-07.

[11] M. M. Hella and M. Ismail, *RF CMOS Power Amplifiers: Theory, Design and Implementation*. Springer Science & Business Media, 2006, vol. 659.

[12] S. Cripps, *RF Power Amplifiers for Wireless Communications*, ser. Artech House microwave library. Artech House, 1999.

[13] C. Doan, S. Emami, D. Sobel, A. Niknejad, and R. Brodersen, "Design considerations for 60 GHz CMOS radios," *IEEE Communications Magazine (CM'2004)*, vol. 42, no. 12, pp. 132–140, Dec 2004.

[14] A. Kavousian, D. Su, M. Hekmat, A. Shirvani, and B. Wooley, "A Digitally Modulated Polar CMOS Power Amplifier With a 20-MHz Channel Bandwidth," *IEEE Journal of Solid-State Circuits (SSC'2008)*, vol. 43, no. 10, pp. 2251–2258, Oct 2008.

[15] F. Carrara, C. Presti, F. Pappalardo, and G. Palmisano, "A 2.4-GHz 24-dBm SOI CMOS Power Amplifier With Fully Integrated Reconfigurable Output Matching Network," *IEEE Transactions on Microwave Theory and Techniques (MTT'2009)*, vol. 57, no. 9, pp. 2122–2130, Sep 2009.

[16] L. Ye, J. Chen, L. Kong, P. Cathelin, E. Alon, and A. Niknejad, "A digitally modulated 2.4GHz WLAN transmitter with integrated phase path and dynamic load modulation in 65nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC'2013)*, Feb 2013, pp. 330–331.

[17] X. Yu, M. Wei, Y. Song, Z. Wang, and B. Chi, "A PAPR-Aware Dual-Mode Subgigahertz CMOS Power Amplifier for Short-Range Wireless Communication," *IEEE Transactions on Circuits and Systems II (CS-II'2016)*, vol. 63, no. 1, pp. 44–48, Jan 2016.

[18] M.-S. Jeon, J.-L. Woo, S. Park, and Y. Kwon, "A Pulsed Dynamic Load Modulation Technique for High-Efficiency Linear Transmitters," *IEEE Transactions on Microwave Theory and Techniques (MTT'2015)*, vol. 63, no. 9, pp. 2854–2866, Sep 2015.

[19] M. Heidari, M. Lee, and A. Abidi, "All-Digital Outphasing Modulator for a Software-Defined Transmitter," *IEEE Journal of Solid-State Circuits (SSC'2009)*, vol. 44, no. 4, pp. 1260–1271, Apr 2009.

[20] S. Hu, S. Kousai, J. S. Park, O. Chlieh, and H. Wang, "Design of A Transformer-Based Reconfigurable Digital Polar Doherty Power Amplifier Fully Integrated in Bulk CMOS," *IEEE Journal of Solid-State Circuits (SSC'2015)*, vol. 50, no. 5, pp. 1094–1106, May 2015.

[21] Gaber, W.M. and Wambacq, P. and Craninckx, J. and Ingels, M., "A CMOS IQ Digital Doherty Transmitter using modulated tuning capacitors," in *IEEE Proceedings of European Solid-State Circuits (ESSCIRC'2012)*, Sep 2012, pp. 341–344.

[22] S. Hu, S. Kousai, and H. Wang, "A Broadband Mixed-Signal CMOS Power Amplifier With a Hybrid Class-G Doherty Efficiency Enhancement Technique," *IEEE Journal of Solid-State Circuits (SSC'2016)*, vol. PP, no. 99, pp. 1–16, Feb 2016.

[23] A. Ba, Y. H. Liu, J. van den Heuvel, P. Mateman, B. Busze, J. Gloudemans, P. Vis, J. Dijkhuis, C. Bachmann, G. Dolmans, K. Philips, and H. de Groot, "26.3 A 1.3nJ/b IEEE 802.11ah fully digital polar transmitter for IoE applications," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, Jan 2016, pp. 440–441.

[24] C. Sanchez-Perez, M. Ozen, C. Andersson, D. Kuylenstierna, N. Rorsman, and C. Fager, "Optimized Design of a Dual-Band Power Amplifier With SiC Varactor-Based Dynamic Load Modulation," *IEEE Transactions on Microwave Theory and Techniques (MTT'2015)*, vol. 63, no. 8, pp. 2579–2588, Aug 2015.

[25] H. Cao, H. Nemati, A. Tehrani, T. Eriksson, J. Grahn, and C. Fager, "Linearization of Efficiency-Optimized Dynamic Load Modulation Transmitter Architectures," *IEEE Transactions on Microwave Theory and Techniques (MTT'2010)*, vol. 58, no. 4, pp. 873–881, Apr 2010.

[26] B. A. W. Alireza Shirvani, *Design and Control of RF Power Amplifiers*, 1st ed. Kluwer, 2003.

[27] E. McCune, "A Technical Foundation for RF CMOS Power Amplifiers: Part 2: Power Amplifier Architectures," *IEEE Solid-State Circuits Magazine (SSCM'2015)*, vol. 7, no. 4, pp. 75–82, Fall 2015.

[28] J. T. Stauth and S. R. Sanders, "Energy Efficient Wireless Transmitters: Polar and Direct-Digital Modulation Architectures," Ph.D. dissertation, EECS Department, University of California, Berkeley, Feb 2009. [Online]. Available: http://www.eecs.berkeley.edu/Pubs/TechRpts/2009/EECS-2009-22.html

[29] S. Luschas, R. Schreier, and H.-S. Lee, "Radio frequency digital-to-analog converter," *IEEE Journal of Solid-State Circuits (SSC'2004)*, vol. 39, no. 9, pp. 1462–1467, Sep 2004.

[30] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 2004.

[31] M. Alavi, R. Staszewski, L. de Vreede, A. Visweswaran, and J. Long, "All-Digital RF I/Q Modulator," *IEEE Transactions on Microwave Theory and Techniques (MTT'2012)*, vol. 60, no. 11, pp. 3513–3526, Nov 2012.

[32] K. Waheed and R. Staszewski, "Digital RF Processing Techniques for Device Mismatch Tolerant Transmitters in Nanometer-Scale CMOS," in *IEEE International Symposium on Circuits and Systems (CS'2007)*, May 2007, pp. 1253–1256.

[33] P. Meher, J. Valls, T.-B. Juang, K. Sridharan, and K. Maharatna, "50 Years of CORDIC: Algorithms, Architectures, and Applications," *IEEE Transactions on Circuits and Systems I (CS-I'2009)*, vol. 56, no. 9, pp. 1893–1907, Sep 2009.

[34] H. Choi, Y. Lee, and S. Hong, "A Digital Polar CMOS Power Amplifier With a 102-dB Power Dynamic Range Using a Digitally Controlled Bias Generator," *IEEE Transactions on Microwave Theory and Techniques (MTT'2014)*, vol. 62, no. 3, pp. 579–589, Mar 2014.

[35] S.-M. Yoo, J. Walling, E. C. Woo, B. Jann, and D. Allstot, "A Switched-Capacitor RF Power Amplifier," *IEEE Journal of Solid-State Circuits (SCC'2011)*, vol. 46, no. 12, pp. 2977–2987, Dec 2011.

[36] T. Nakatani, D. Kimball, and P. Asbeck, "Techniques for Power Dynamic Range and Back-Off Efficiency Improvement in CMOS Digitally Controlled Polar Transmitters," *IEEE Transactions on Microwave Theory and Techniques (MTT'2016)*, vol. 64, no. 2, pp. 550–561, Feb 2016.

[37] M. Alavi, R. Staszewski, L. de Vreede, and J. Long, "A wideband 2 x 13-bit all-digital i/q rf-dac," *IEEE Transactions on Microwave Theory and Techniques (MTT'2014)*, vol. 62, no. 4, pp. 732–752, Apr 2014.

[38] C. Lu, H. Wang, C. Peng, A. Goel, S. Son, P. Liang, A. Niknejad, H. Hwang, and G. Chien, "A 24.7dBm all-digital RF transmitter for multimode broadband applications in 40nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC'2013)*, Feb 2013, pp. 332–333.

[39] W. Yuan, V. Aparin, J. Dunworth, L. Seward, and J. Walling, "A Quadrature Switched Capacitor Power Amplifier," *IEEE Journal of Solid-State Circuits (SSC'2016)*, vol. PP, no. 99, pp. 1–22, Jan 2016.

[40] H. Chireix, "High Power Outphasing Modulation," *Proceedings of the Institute of Radio Engineers (IRR'1935)*, vol. 23, no. 11, pp. 1370–1392, Nov 1935.

[41] P. Madoglio, A. Ravi, H. Xu, K. Chandrashekar, M. Verhelst, S. Pellerano, L. Cuellar, M. Aguirre, M. Sajadieh, O. Degani, H. Lakdawala, and Y. Palaskas, "A 20dBm 2.4GHz digital outphasing transmitter for WLAN application in 32nm CMOS," in *IEEE Solid-State Circuits (SSC'2012)*, Feb 2012, pp. 168–170.

[42] S. Cripps, *Advanced Techniques in RF Power Amplifier Design*, ser. Artech House microwave library. Artech House, 2002.

[43] X. Zhang, P. Asbeck, and L. Larson, *Design of Linear RF Outphasing Power Amplifiers*. Norwood: Artech House, 2003.

[44] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ, USA: Prentice-Hall, Inc., 1998.

[45] D. Kang, B. Park, C. Zhao, D. Kim, J. Kim, Y. Cho, S. Jin, H. Jin, and B. Kim, "A 34% PAE, 26-dBm output power envelope-tracking CMOS power amplifier for 10-MHz BW LTE applications," in *IEEE Microwave Theory and Techniques (MTT'2012)*, Jun 2012, pp. 1–3.

[46] E. Kaymaksut and P. Reynaert, "Dual-Mode CMOS Doherty LTE Power Amplifier With Symmetric Hybrid Transformer," *IEEE Journal of Solid-State Circuits (SSC'2015)*, vol. 50, no. 9, pp. 1974–1987, Sep 2015.

[47] J. Jeong, D. Kimball, M. Kwak, C. Hsia, P. Draxler, and P. Asbeck, "Wideband Envelope Tracking Power Amplifiers With Reduced Bandwidth Power Supply Waveforms and Adaptive Digital Predistortion Techniques," *IEEE Transactions on Microwave Theory and Techniques (MTT'2009)*, vol. 57, no. 12, pp. 3307–3314, Dec 2009.

[48] K. Rawat, M. Rawat, and F. Ghannouchi, "Compensating I-Q Imperfections in Hybrid RF/Digital Predistortion With an Adapted Lookup Table Implemented in an FPGA," *IEEE Transactions on Circuits and Systems II (CS-II'2010)*, vol. 57, no. 5, pp. 389–393, May 2010.

[49] W. Neo, Y. Lin, X. dong Liu, L. de Vreede, L. Larson, M. Spirito, M. Pelk, K. Buisman, A. Akhnoukh, A. de Graauw, and L. Nanver, "Adaptive Multi-Band Multi-Mode Power Amplifier Using Integrated Varactor-Based Tunable Matching Networks," *IEEE Journal of Solid-State Circuits (SSC'2006)*, vol. 41, no. 9, pp. 2166–2176, Sep 2006.

[50] H. Nemati, C. Fager, U. Gustavsson, and H. Zirath, "An Efficiency Optimized Controlling Scheme for Dynamic Load Modulation of Power Amplifiers," in *IEEE European Microwave Conference (EuMC'2008)*, Oct 2008, pp. 583–586.

[51] J.-S. Fu and A. Mortazawi, "Improving Power Amplifier Efficiency and Linearity Using a Dynamically Controlled Tunable Matching Network," *IEEE Transactions on Microwave Theory and Techniques (MTT'2008)*, vol. 56, no. 12, pp. 3239–3244, Dec 2008.

[52] K. Chen and D. Peroulis, "Design of Adaptive Highly Efficient GaN Power Amplifier for Octave-Bandwidth Application and Dynamic Load Modulation," *IEEE Transactions on Microwave Theory and Techniques (MTT'2012)*, vol. 60, no. 6, pp. 1829–1839, Jun 2012.

[53] C. Andersson, M. Ozen, D. Gustafsson, K. Yamanaka, E. Kuwata, H. Otsuka, M. Nakayama, Y. Hirano, I. Angelov, C. Fager, and N. Rorsman, "A packaged 86 W GaN transmitter with SiC varactor-based dynamic load modulation," in *IEEE European Microwave Conference (EuMC'2013)*, Oct 2013, pp. 283–286.

[54] C. Hoarau, N. Corrao, J.-D. Arnould, P. Ferrari, and P. Xavier, "Complete Design and Measurement Methodology for a Tunable RF Impedance-Matching Network," *IEEE Transactions on Microwave Theory and Techniques (MTT'2008)*, vol. 56, no. 11, pp. 2620–2627, Nov 2008.

[55] C. Fager, H. Cao, T. Eriksson, R. Jos, H. Nemati, A. Soltani, and H. Zirath, "High efficiency transmitter using varactor based dynamic load modulation," in *IEEE International Microwave Workshop Series (IMWS'2010)*, Feb 2010, pp. 1–4.

[56] H. Nemati, H. Cao, B. Almgren, T. Eriksson, and C. Fager, "Design of Highly Efficient Load Modulation Transmitter for Wideband Cellular Applications," *IEEE Transactions on Microwave Theory and Techniques (MTT'2010)*, vol. 58, no. 11, pp. 2820–2828, Nov 2010.

[57] A. Tehrani, H. Nemati, H. Cao, T. Eriksson, and C. Fager, "Dynamic load modulation of high power amplifiers with varactor-based matching networks," in *IEEE Microwave Theory and Techniques (MTT'2009)*, Jun 2009, pp. 1537–1540.

[58] H. Nemati, C. Fager, U. Gustavsson, R. Jos, and H. Zirath, "Design of Varactor-Based Tunable Matching Networks for Dynamic Load Modulation of High Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques (MTT'2009)*, vol. 57, no. 5, pp. 1110–1118, May 2009.

[59] H. T. Jeong, H. S. Lee, I. S. Chang, and C. D. Kim, "Efficiency enhancement method for high-power amplifiers using a dynamic load adaptation technique," in *IEEE Microwave Theory and Techniques (MTT'2005)*, Jun 2005, pp. 4 pp.–.

[60] M. El Din, B. Geck, I. Rolfs, and H. Eul, "A novel inverse class-D output matching network and its application to dynamic load modulation," in *IEEE Microwave Theory and Techniques (MTT'2010)*, May 2010, pp. 332–335.

[61] A. Mohamed, S. Boumaiza, and R. Mansour, "Novel reconfigurable fundamental/harmonic matching network for enhancing the efficiency of power amplifiers," in *IEEE European Microwave Conference (EuMC'2010)*, Sep 2010, pp. 1122–1125.

[62] L. Yue, T. Maehata, K. Totani, H. Tango, T. Hashinaga, and T. Asaina, "A novel tunable matching network for dynamic load modulation of high power amplifiers," in *IEEE European Microwave Conference (EuMC'2012)*, Oct 2012, pp. 707–710.

[63] F. Raab, "High-efficiency linear amplification by dynamic load modulation," in *IEEE Microwave Theory and Techniques (MTT'2003)*, vol. 3, Jun 2003, pp. 1717–1720 vol.3.

[64] K. Buisman, L. de Vreede, L. Larson, M. Spirito, A. Akhnoukh, Y. Lin, X. Liu, and L. Nanver, "Low-distortion, low-loss varactor-based adaptive matching networks, implemented in a silicon-on-glass technology," in *IEEE Radio-Frequency Integrated Circuits (RFIC'2005)*, Jun 2005, pp. 389–392.

[65] M. Sudow, H. Nemati, M. Thorsell, U. Gustavsson, K. Andersson, C. Fager, P.-A. Nilsson, J. ul Hassan, A. Henry, E. Janzen, R. Jos, and N. Rorsman, "SiC Varactors for Dynamic Load Modulation of High Power Amplifiers," *IEEE Electron Devices Letters (EDL'2008)*, vol. 29, no. 7, pp. 728–730, Jul 2008.

[66] H. Cao, C. Fager, T. Khan, A. Tehrani, and T. Eriksson, "Comparison of bandwidth reduction schemes in dynamic load modulation power amplifier architectures," in *IEEE Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC'2011)*, April 2011, pp. 1–4.

[67] W. Hallberg, D. Gustafsson, M. Ozen, C. Andersson, D. Kuylenstierna, and C. Fager, "A class-J power amplifier with varactor-based dynamic load modulation across a large bandwidth," in *IEEE Microwave Theory and Techniques Symposium (MTT-S'2015)*, May 2015, pp. 1–4.

[68] C. Andersson, D. Gustafsson, K. Yamanaka, E. Kuwata, H. Otsuka, M. Nakayama, Y. Hirano, I. Angelov, C. Fager, and N. Rorsman, "Theory and Design of Class-J Power Amplifiers With Dynamic Load Modulation," *IEEE Transactions on Microwave Theory and Techniques (MTT'2012)*, vol. 60, no. 12, pp. 3778–3786, Dec 2012.

[69] P. Sjoblom and H. Sjoland, "Measured CMOS Switched High-Quality Capacitors in a Reconfigurable Matching Network," *IEEE Transactions on Circuits and Systems II (CS-II'2007)*, vol. 54, no. 10, pp. 858–862, Oct 2007.

[70] A. Paidimarri, N. Ickes, and A. P. Chandrakasan, "A +10 dBm BLE Transmitter With Sub-400 pW Leakage for Ultra-Low Duty Cycles," *IEEE Journal of Solid-State Circuits (SSC'2016)*, vol. PP, no. 99, pp. 1–16, 2016.

[71] M. Park, M. H. Perrott, and R. B. Staszewski, "An Amplitude Resolution Improvement of an RF-DAC Employing Pulsewidth Modulation," *IEEE Transactions on Circuits and Systems I (CS-I'2011)*, vol. 58, no. 11, pp. 2590–2603, Nov 2011.

[72] H. Song and R. Gharpurey, "Digitally intensive transmitter employing RF pulse width modulation for IoT applications," in *Radio Frequency Integrated Circuits Symposium (RFIC'2015)*, May 2015, pp. 151–154.

[73] P. Reynaert and M. Steyaert, *RF Power Amplifiers for Mobile Communications*, ser. Analog Circuits and Signal Processing. Springer Netherlands, 2006. [Online]. Available: https://books.google.pt/books?id=g4mtb7yyImQC

[74] Y. Tsividis, *Operation and Modeling of the MOS Transistor*. New York, NY, USA: McGraw-Hill, Inc., 1987.

[75] L. Larcher, D. Sanzogni, R. Brama, A. Mazzanti, and F. Svelto, "Oxide Breakdown After RF Stress: Experimental Analysis and Effects on Power Amplifier Operation," in *2006 IEEE International Reliability Physics Symposium Proceedings (RPS'2006)*, March 2006, pp. 283–288.

[76] C. D. Presti, F. Carrara, A. Scuderi, P. M. Asbeck, and G. Palmisano, "A 25 dBm Digitally Modulated CMOS Power Amplifier for WCDMA/EDGE/OFDM With Adaptive Digital Predistortion and Efficient Power Control," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 7, pp. 1883–1896, July 2009.

[77] P. Davis and P. Rabinowitz, *Methods of Numerical Integration*, ser. Dover Books on Mathematics Series. Dover Publications, 2007.

[78] M. Albulet, *RF Power Amplifiers*, ser. Electromagnetics and Radar. Institution of Engineering and Technology, 2001.

[79] K. C. Lin, H. K. Chiou, P. C. Wu, W. H. Chen, C. L. Ko, and Y. Z. Juang, "2.4-GHz Complementary Metal Oxide Semiconductor Power Amplifier Using High-Quality Factor Wafer-Level Bondwire Spiral Inductor," *IEEE Transactions on Components, Packaging and Manufacturing Technology (CPMT'2013)*, vol. 3, no. 8, pp. 1286–1292, Aug 2013.

[80] S. Lee and S. Nam, "A CMOS Outphasing Power Amplifier With Integrated Single-Ended Chireix Combiner," *IEEE Transactions on Circuits and Systems II (CS-II'2010)*, vol. 57, no. 6, pp. 411–415, June 2010.

[81] H. J. Qian, J. O. Liang, and X. Luo, "Wideband Digital Power Amplifiers With Efficiency Improvement Using 40-nm LP CMOS Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 3, pp. 675–687, March 2016.

[82] K. K. Sessou and N. M. Neihart, "An Integrated 700-1200-MHz Class-F PA With Tunable Harmonic Terminations in 0.13 um CMOS," *IEEE Transactions on Microwave Theory and Techniques (MTT'2015)*, vol. 63, no. 4, pp. 1315–1323, April 2015.

[83] B. Francois and P. Reynaert, "A Fully Integrated Watt-Level Linear 900-MHz CMOS RF Power Amplifier for LTE-Applications," *IEEE Transactions on Microwave Theory and Techniques (MTT'2012)*, vol. 60, no. 6, pp. 1878–1885, June 2012.

[84] D. Chowdhury, C. D. Hull, O. B. Degani, Y. Wang, and A. M. Niknejad, "A Fully Integrated Dual-Mode Highly Linear 2.4 GHz CMOS Power Amplifier for 4G WiMax Applications," *IEEE Journal of Solid-State Circuits (JSSC'2009)*, vol. 44, no. 12, pp. 3393–3402, Dec 2009.

[85] H. Song and R. Gharpurey, "Digitally intensive transmitter employing RF pulse width modulation for IoT applications," in *Radio Frequency Integrated Circuits Symposium (RFIC'2015)*, May 2015, pp. 151–154.

[86] Y. Yoon, J. Kim, H. Kim, K. H. An, O. Lee, C. H. Lee, and J. S. Kenney, "A Dual-Mode CMOS RF Power Amplifier With Integrated Tunable Matching Network," *IEEE Transactions on Microwave Theory and Techniques (MTT'2012)*, vol. 60, no. 1, pp. 77–88, Jan 2012.

[87] K. Onizuka, S. Saigusa, and S. Otaka, "A 1.8GHz linear CMOS power amplifier with supply-path switching scheme for WCDMA/LTE applications," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb 2013, pp. 90–91.

[88] Y. Yoon, J. Kim, H. Kim, K. H. An, O. Lee, C. H. Lee, and J. S. Kenney, "A Dual-Mode CMOS RF Power Amplifier With Integrated Tunable Matching Network," *IEEE Transactions on Microwave Theory and Techniques (MTT'2012)*, vol. 60, no. 1, pp. 77–88, Jan 2012.

[89] C. A. C. Coello, G. T. Pulido, and M. S. Lechuga, "Handling multiple objectives with particle swarm optimization," *IEEE Transactions on Evolutionary Computation (TEC'2004)*, vol. 8, no. 3, pp. 256–279, June 2004.

[90] J. C. Bansal, P. K. Singh, M. Saraswat, A. Verma, S. S. Jadon, and A. Abraham, "Inertia Weight strategies in Particle Swarm Optimization," in *Third World Congress on Nature and Biologically Inspired Computing (NaBIC'2011)*, Oct 2011, pp. 633–640.

[91] Y. Gao and Z. Ren, "Adaptive particle swarm optimization algorithm with genetic mutation operation," in *Third International Conference on Natural Computation (ICNC 2007)*, vol. 2, Aug 2007, pp. 211–215.

[92] S. Kim and D. Im, "A High-Q Linear CMOS Digitally Controlled Accumulation-mode Varactor Array for Multiband RF Circuits," *Progress in Electromagnetic Research Symposium (PIERS'2015)*, vol. PP, pp. 2805–2808, 2015.

[93] D. Yang, Y. Ding, and S. Huang, "A 65-nm High-Frequency Low-Noise CMOS-Based RF SoC Technology," *IEEE Transactions on Electron Devices (ED'2010)*, vol. 57, no. 1, pp. 328–335, Jan 2010.

[94] B. Landgraf, "MOM Capacitance Measurements in a 130 nm CMOS Node," in *2015 Austrian Workshop on Microelectronics (Austrochip),*, Sept 2015, pp. 42–45.

[95] X. J. Li and Y. P. Zhang, "Flipping the CMOS Switch," *IEEE Microwave Magazine (MM'2010)*, vol. 11, no. 1, pp. 86–96, Feb 2010.