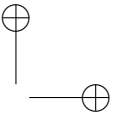
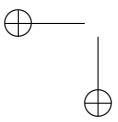


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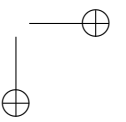


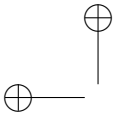
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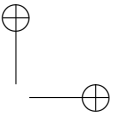


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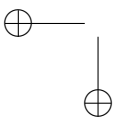


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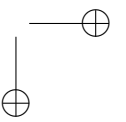


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Dense Electro-Photonic Integration
Based on Printing of Optical and High-Speed Electrical Interconnections

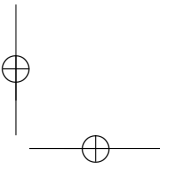
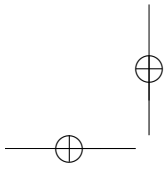
Elektro-fotonische integratie met hoge dichtheid
gebaseerd op het printen van optische en snelle elektrische verbindingen

Ahmed Elmogi

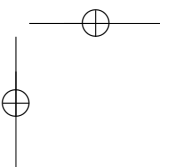
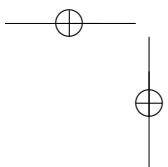
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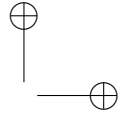
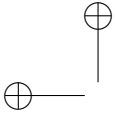


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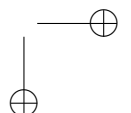
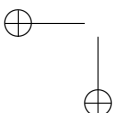
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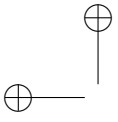
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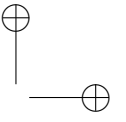
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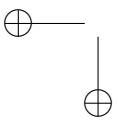


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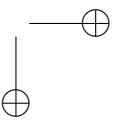


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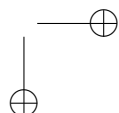
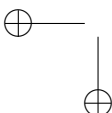


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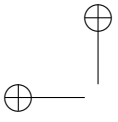
*Ghent, 5 July 2019
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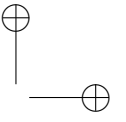
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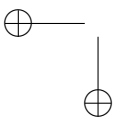


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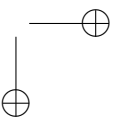


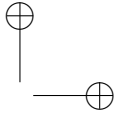
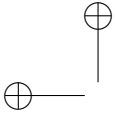
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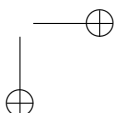
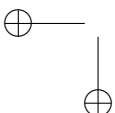
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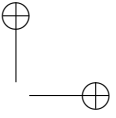
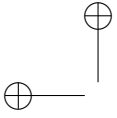
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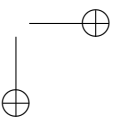
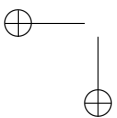
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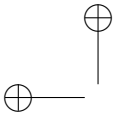
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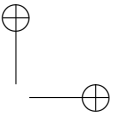
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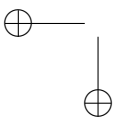


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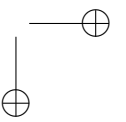


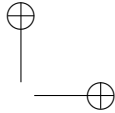
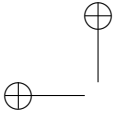
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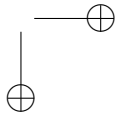
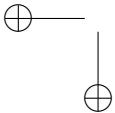
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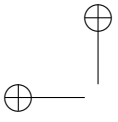
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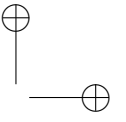
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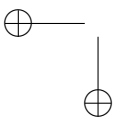


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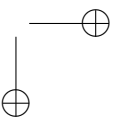


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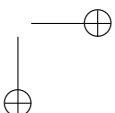
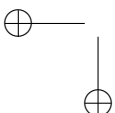




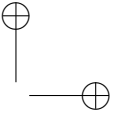
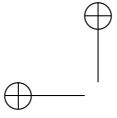
List of Acronyms



ADS	Advanced Design System
AJP	Aerosol Jet Printing
Al	Aluminum
AOD	Acoustic-optic Deflector
AOM	Acoustic-optic Modulator
AWG	Arrayed Waveguide Grating
BPM	Beam Propagation Method
BTB	Back to Back
BW	Bandwidth
CAD	Computer Aided Design
CAGR	Compound Annual Growth Rate
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
CTE	Coefficient of Thermal Expansion
3D	Three-Dimensional
2.5D	2.5 Dimensional
DCs	Data Centers
DFB	Distributed Feedback
DWL	Direct-write Lithography
DUT	Device under Test
EAM	Electro-absorption Modulator
EIC	Electronic Integrated Circuit
EO	Electro-Optical
ER	Extinction Ratio
FEM	Finite Element Method
FFE	Feed Forward Equalization
FDSOI	Fully Depleted Silicon-on-Insulator
GSG	Ground-Signal-Ground
IC	Integrated Circuit
IPA	Isopropyl Alcohol
IR	Infrared
IoT	Internet of Things
LD	Laser Diode
LDW	Laser Direct Writing



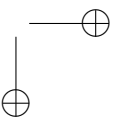
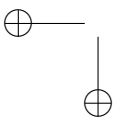
LRL	Line Reflect Line
LRM	Line Reflect Match
MFD	Mode Field Diameter
MMF	Multimode Fiber
NA	Numerical Aperture
NIR	Near Infrared
NP	Nanoparticle
NR	Non Return to Zero
OOK	On Off keying
PA	Pneumatic Atomizer
PAM	Pulse Amplitude Modulation
PCB	Printed Circuit Board
PD	Photo Diode
PDMS	Polydimethylsiloxane
PEB	Post Exposure Bake
PET	Polyethylene terephthalate
PET	Polyethylene terephthalate
PFA	PerfluoroAlkoxy
PGMEA	Propylene glycol methyl ether acetate
PIC	Photonic Integrated Circuit
PMMA	Poly Methyl Methacrylate
PWG	Polymer Waveguide
RF	Radio Frequency
RH	Relative Humidity
RI	Refractive Index
SCD	Single-crystalline diamond
Si	Silicon
SEM	Scanning Electron Microscope
SiWG	Silicon Waveguide
SOI	Silicon-on-Insulator
SMF	Single-mode fiber
SOLT	Short open Load Thru
SSC	Spot size converter
SSMF	Standard Single-mode fiber
TL	Transmission line
ToR	Top-of-Rack
TOV	Through-oxide Via
TRL	Thru Reflect Line
TSV	Through-silicon Via
UA	Ultrasonic Atomizer
UV	Ultraviolet
TEC	Thermo-electric Cooling
TOC	Thermo-Optic

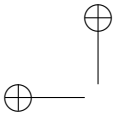


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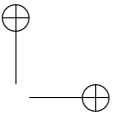
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TOC	Thermo-Optic Coefficient
VCSEL	Vertical Cavity Surface Emitting Laser
VNA	Vector Network Analyzer



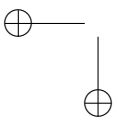


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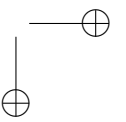


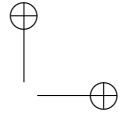
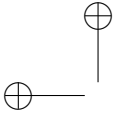
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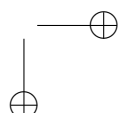
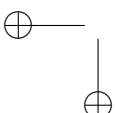


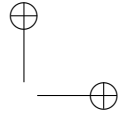
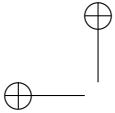


Samenvatting

In de voorbije decennia heeft de evolutie van het internet onze levens drastisch veranderd en verbeterd. Een enorme hoeveelheid informatie en een groot aantal diensten zijn in een oogwenk beschikbaar op het internet. Heden ten dage kunnen een groot autonome slimme toestellen met elkaar communiceren en gegevens uitwisselen via het Internet. Dit concept is tegenwoordig bekend als het internet der dingen, of ook Internet of Things (IoT) in het Engels. Om dit te realiseren zijn communicatienetwerken met een hoge doorvoercapaciteit nodig om onmiddellijk gegevens te actualiseren en te delen. Als een gevolg hiervan veroorzaakt het internet der dingen een nooit eerder geziene stroom internetverkeer. Alsof dit nog niet genoeg is veroorzaken de sociale netwerken, muziek- en videodiensten elke dag enorme hoeveelheden verkeer. Deze enorme hoeveelheid gegevens worden opgeslagen in wat tegenwoordig populair de cloud heet, maar wat in werkelijkheid niet meer is dan het alom bekende begrip datacenter (DC).

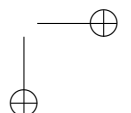
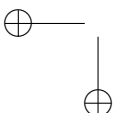
Om de exponentiële groei in capaciteit en snelheid van datacenters te kunnen blijven behouden zijn belangrijke verbeteringen noodzakelijk in elk aspect van de DCs. De verbindingen tussen DC servers en switches zijn een van de meest kritische aspecten, en hebben een directe impact op de snelheid van DC netwerken. Hierdoor is het noodzakelijk om innovatieve interconnectiemethodes te voorzien voor de communicatie tussen DC servers en switches, zowel in hetzelfde serverrek als tussen serverrekken onderling. Technologieën gebaseerd op optische verbindingen zijn een veelbelovende oplossing om in de noden naar groeiende capaciteit van DCs te voldoen. Gedurende het laatste decennium hebben optische verbindingen reeds hun potentieel in verband met hogesnelheidscommunicatie bewezen. Optische interconnectietechnologie is vooral gebaseerd op elektro-optische zend-ontvangers voor het versturen en ontvangen van gegevens. Multimode VCSEL-gebaseerde optische verbindingen hebben een ruim marktoverwicht in de datacenter-markt aangezien ze zeer goedkoop zijn op componentniveau (VCSEL en fotodiode). De vraag naar hogere gegevensoverdrachtcapaciteit zet meer druk op de verkopers en uitbaters van datacenters om nieuwe technologieën en aanpakken uit te proberen. Single-mode silicium fotonische DC interconnecties hebben het potentieel om het bandbreedte-afstand product te behalen dat nodig is voor datacenters van de toekomst. De 400 Gigabit Ethernetstandaard, gedefinieerd door de IEEE P802.3bs 400 GbE Task Force zal verschillende geavanceerde technologieën moeten gebruiken om elk individueel kanaal sneller te maken en onder-tussen een gelijkaardige poort-densiteit te behouden. Een van de grote uitdagingen voor datacenters van de toekomst is de integratie van elektronische en fotonische geïntegreerde





circuits (ICs, Integrated Circuits). De verpakking van fotonische ICs in het bijzonder is een van de meest cruciale uitdagingen die moeten aangepakt worden om echte massaproductie mogelijk te maken, aangezien deze een enorme impact heeft op de performantie en kost van het fotonische systeem.

Het werk dat wordt voorgesteld in deze scriptie spitst zich toe op de hybride integratie van elektronische en fotonische ICs, in het bijzonder op de elektrische koppeling (hogesnelheidsverbindingen) en de optische koppeling (verbinding van optische vezel naar IC). In deze scriptie hebben we twee procestechnologieën ontwikkeld om elektrische en optische verbindingen te maken voor de verpakking van fotonische circuits. De elektrische verbindingen worden geprint met Aerosol Jet Printing (AJP) technologie om de hogesnelheidsverbindingen tussen de optische en elektronische circuits te realiseren. De optische verbindingen zijn gebaseerd op single-mode (SM) polymeer golfgeleiders, die gerealiseerd worden met direct-write lithography (DWL, rechtstreeks geschreven lithografie). AJP technologie wordt gebruikt voor de hogesnelheidsverbindingen om zeer korte en rechte verbindingen tussen de fotonische en elektronische ICs (100-300 μm lang met een steek van 50 μm) te realiseren, waarbij dus de parasitaire inductantie voor hoge snelheid zend-ontvangers minimaal is. De technologie laat ook toe om de karakteristieke impedantie van de geprinte transmissielijnen (TL) af te stemmen door de afmetingen en tussenruimte te controleren, om zodoende TL aan elkaar aan te passen om reflecties en verzwakkingen van het signaal te minimaliseren. Voor dit aspect van het onderzoek werden verschillende zilver-inkten uitgetest met de AJP technologie, en op basis van de experimenten werd 1 type inkt geselecteerd. Het printproces werd verder geoptimaliseerd voor deze specifieke inkt. Hierna werden coplanaire TL ontworpen en op diverse substraten geprint met AJP. Vervolgens werd een proces ontwikkeld voor de elektro-optische verbinding. Verschillende optische zenders die gebaseerd zijn op de integratie van de elektronische driver ICs en fotonische ICs worden aangetoond op hoge snelheden, tot 60 Gb/s. De ontwikkelde samenstelling werd rechtstreeks vergeleken met de traditionele wire-bonded variant van dezelfde samenstelling, en op hoge frequenties was de performantie van de AJP samenstelling beter. Voor de optische verbindingen werd een proces ontwikkeld om single-mode polymeer golfgeleiders te fabriceren met twee verschillende materialen. Gebaseerd op de meting van de brekingsindex van de polymeren werden de benodigde afmetingen om single-mode te bereiken bij golflengtes van 1.31 μm en 1.55 μm berekend. De DWL belichtingsparameters werden geoptimaliseerd voor de kernmaterialen om een goede controle te verkrijgen over de afmetingen van de golfgeleiders, en de polymeer golfgeleiders werden gepatroneerd met deze optimale parameters. Daarnaast worden ook kruisingen tussen SM golfgeleiders gerealiseerd met de twee materialen, om een complexere routing mogelijk te maken. De gefabriceerde golfgeleiders werden gekarakteriseerd door de propagatieverliezen te meten met de cut-back methode zowel op 1.31 μm als op 1.55 μm . Vervolgens werd een proces ontwikkeld om adiabatische koppeling tussen DWL SM en SOI golfgeleiders aan te tonen. De SM polymeer golfgeleiders gedragen zich als spot size converters tussen single-mode fibers en SOI golfgeleiders. Het inkoppelverlies per facet werd gemeten en het adiabatische koppelverlies werd geschat.



Hoofdstuk 1 introduceert de achtergrond van de integratie van elektronica en fotonica en geeft de huidige stand van de techniek weer voor de verpakking van fotonische chips, inclusief de relevante uitdagingen.

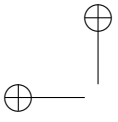
Hoofdstuk 2 presenteert de AJP technologie, inclusief de meest recente en relevante applicaties, in het bijzonder in het gebied van elektrische verbindingen en RF transmissielijnen. Experimenten met verschillende nanopartikel zilver-inkten en de optimalisatie van het printproces worden toegelicht. Vervolgens wordt ook het sinteren van de geprinte elektrische verbindingen getoond. Tot slot wordt de realisatie van coplanaire golfgeleider transmissielijnen aangetoond en vergeleken met simulaties.

Hoofdstuk 3 belicht het gebruik van AJP hogesnelheidsverbindingen om elektronische en fotonische geïntegreerde circuits met elkaar te verbinden om optische zenders voor gebruik in datacenters te ontwikkelen. Het proces om AJP-gebaseerde elektro-fotonische integratie te bekomen wordt beschreven. Vervolgens werd de functionaliteit van de procestechologie getest op daisy-chain testchips. Bijkomend werden ook $85^{\circ}C/85\% RH$ betrouwbaarheidstesten uitgevoerd om de betrouwbaarheid van de geprinte verbindingen te onderzoeken. Vervolgens wordt een vergelijking gemaakt met aerosol-geprinte verbindingen en traditionele wire-bonds. Tot slot worden verschillende hoge snelheid optische zender-samenstellingen aangetoond.

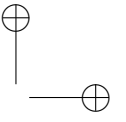
In hoofdstuk 4 worden optische verbindingen gebaseerd op SM polymeer golfgeleiders ontwikkeld met behulp van DWL. Twee systemen van optische materialen op basis van epoxy en siloxaan polymeren worden gebruikt. De dimensies nodig voor een single-mode golfgeleider voor beide materialen werd berekend met een numerieke mode solver. Vervolgens wordt het fabricageproces van de polymeer golfgeleiders beschreven. In het bijzonder wordt aandacht gegeven aan het DWL proces en de bijhorende optimalisatie van het patroneren van de kernmaterialen. De resultaten van de karakterisatie met behulp van cut-back metingen bij datacom golfengtes worden eveneens toegelicht.

In hoofdstuk 5 wordt een adiabatische koppeling tussen SOI golfgeleiders en de in dit werk ontwikkelde DWL polymeer golfgeleiders aangetoond. Het fabricageproces wordt in detail beschreven en de resultaten van de karakterisatie, inclusief de totale inkoppelverliezen en de adiabatische koppelverliezen.

Tot slot worden in hoofdstuk 6 de belangrijkste verwezenlijkingen en aanbevelingen voor toekomstig werk samengevat.

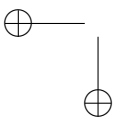


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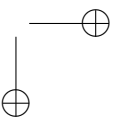


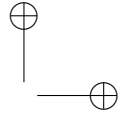
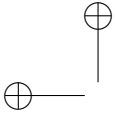
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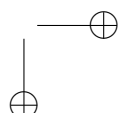
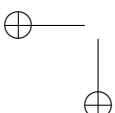




Summary

With the tremendous evolution in Internet over the past decades, nearly every aspect in our lives has entirely changed and significantly improved. The amounts of information and services that can be immediately accessed on the Internet are incredibly massive. Nowadays, huge numbers of autonomous smart devices can communicate with each other and exchange data through the Internet. This concept is known nowadays as Internet of things (IoT). As a result, IoT will require high throughput communication networks to ensure instantaneous data updates and exchange. Consequently, the amount of generated Internet traffic by IoT is unprecedented. Besides, social networks, music and video streaming services (Netflix, Amazon) generate enormous amount of data everyday. This huge amount of data needs to be stored using cloud services. The physical implementation of the cloud services is the data centers (DCs).

In order to sustain the exponential growth in capacity and performance for data centers (DCs), major improvements in every segment of the DCs are required. The routing interconnections between the DC servers and switches are one of the most critical segments that can have a direct impact on the performance of DC networks. Therefore, innovative interconnection schemes for communication between DC switches and servers (within rack & rack-to-rack) are essential. Optical interconnect based technology is a promising solution to address the growing capacity requirement of DC. Over the last decade, optical interconnects have proven their potential for high-speed data communication. The optical interconnect based technology mainly depend on the electro-optical transceivers for data transmission and detection. Multimode VCSEL-based optical links are widely dominating the data center market today because they are much cheaper on the component level (VCSEL and PD). However, the demand for higher data transmission capacity puts extra pressure on the data center vendors and operators to explore new technologies and approaches. Single-mode silicon photonics based DC interconnects have the potential to address the bandwidth-distance product requirements for future DCs. The 400 Gigabit Ethernet standard, which is defined by the IEEE P802.3bs 400 GbE Task Force, will need to utilize different advanced techniques to boost the single lane rate while maintaining a similar port density. One of the main challenges for future data centers communication is the integration between electronics and photonics ICs. Particularly, packaging of photonic integrated circuits (PICs) is one of the most critical challenges that still need to be addressed in order to enable true mass-market production. Photonic packaging highly impacts the performance and cost of the photonic system.



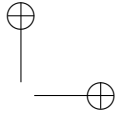
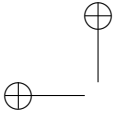
The work presented in this thesis focuses on hybrid integration of electronic and photonic ICs, particularly the electrical interface (high-speed interconnects) and the optical interface (fiber-to-chip coupling). In this thesis, we developed two process technologies to realize electrical and optical interconnects for photonic packaging. The electrical interconnects are realized using aerosol-jet printing (AJP) technology to print the high-speed interconnects between PIC and EIC. The optical interconnects are based on single-mode (SM) polymer waveguides, which are developed using direct-write lithography (DWL).

For the high-speed interconnects, AJP technology is used to print very short and straight electrical interconnects (100-300 μm) with a pitch of 50 μm between PIC and EIC, thus minimizing the parasitic inductance for high-speed transceivers. It also offers tuning the characteristic impedance of the printed transmission lines (TLs) by controlling their dimensions and spacing in order to design impedance-matched TLs, thus reducing signal reflections and attenuation. In this aspect, multiple silver ink materials are experimented with the AJP technology and one ink is selected based on the results of the experiments. The printing process is further optimized for this specific ink. Then, coplanar waveguide transmission lines are designed and fabricated by AJP on different substrates. Next, a process flow for electronic-photonic interconnection is developed. Different optical transmitters based on the integration of PICs and electronic driver ICs are demonstrated at high-speed up to 60 Gb/s. Furthermore, a direct comparison between the developed assembly using AJP and the wire-bonded assembly is performed. The AJP assembly showed better performance at high frequency.

As for the optical interconnects part, we developed a process to fabricate single-mode polymer waveguides using two different material systems. Based on the measurements of refractive indices of the polymer materials, the required single-mode dimensions are calculated at wavelengths of 1.31 μm and 1.55 μm . The DWL exposure parameters are optimized for the core materials to provide a good control for the waveguide dimensions. Then, the polymer waveguides are patterned at the optimum exposure parameters. Additionally, SM polymer waveguide crossings are also realized using the two materials to provide more complex routing. The characterization of the fabricated waveguides is performed by measuring the propagation losses using the cut-back method both at 1.31 μm and 1.55 μm . Next, A process flow is developed to demonstrate the adiabatic coupling between the DWL SM polymer waveguides and SOI waveguides. The SM polymer waveguides in this approach act as spot size converters (SSC) between SSMF and SOI waveguides. The insertion loss per facet is measured and the adiabatic coupling loss is estimated.

chapter 1 introduces the background on electronic-photonic integration and state-of-the-art solutions for photonics packaging including the relevant challenges.

In chapter 2, AJP technology is presented including the state-of-art applications particularly in the area of electrical interconnects and RF transmission lines. Experiments using different nanoparticle silver inks and the optimization of the printing process are also demonstrated. Next, sintering of the printed electrical interconnects is illustrated. Finally, the realization of coplanar waveguide transmission lines is demonstrated, and compared to simulations.

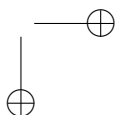
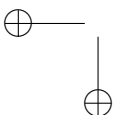


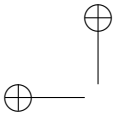
In chapter 3, the AJP high-speed interconnects are used to interconnect electronic and photonic ICs in order to develop optical transmitters for data center applications. The fabrication process flow for the AJP based electronic-photonic integration is described. Then, the functionality of the process technology is tested on daisy-chain test chips. In addition, 85°C/85% RH reliability test is performed in order to investigate the reliability of the realized printed interconnects. Next, a comparison between the aerosol-jet printed interconnects and the traditional bonding wires is provided. Finally, different high-speed optical transmitters assemblies are demonstrated.

In chapter 4, optical interconnects based on single-mode polymer waveguide are developed by direct-write lithography. Two optical material systems including epoxy and siloxane polymers are utilized. The cut-off single-mode waveguide dimensions are calculated for both the core materials using a numerical mode solver. Next, the fabrication process flow of the polymer waveguides is described. In particular, a focus is shed on the direct-write lithography process and the corresponding optimization for patterning the core materials. The characterization results of the fabricated waveguides are introduced including the cut-back measurements at datacom wavelengths.

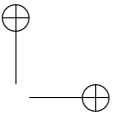
In chapter 5, an adiabatic coupling approach between SOI waveguides and the developed DWL polymer waveguides is demonstrated. The fabrication process flow is described in detail and the characterization results including the total insertion loss and the adiabatic coupling loss are presented.

Finally, in chapter 6, the main achievements and future work are summarized.



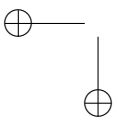


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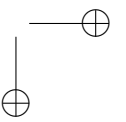


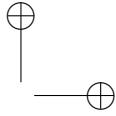
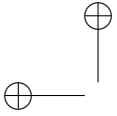
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Introduction

1.1. Background

With the tremendous evolution in Internet over the past decades, nearly every aspect in our lives has entirely changed and significantly improved. The amounts of information and services that can be immediately accessed on the Internet are incredibly massive. Nowadays, huge numbers of autonomous smart devices can communicate with each other and exchange data through the Internet. This concept is known nowadays as Internet of things (IoT). The Internet of Things (IoT) refers to the use of intelligently connected devices and systems to leverage data gathered by embedded sensors and actuators in machines and other physical objects [1]. These smart devices can be controlled remotely to allow direct integration with computer systems. One of the most popular examples of IoT are smart cities and smart homes. Fig. 1.1 shows a graphical representation for the IoT concept [2] in which it shows a simple example how the smart devices existing at home are connected to smartphones and computers. This example represents smart home which is one of the popular IoT applications. Fig. 1.2 shows a graphical representation of the potential IoT applications [3]. In smart retail, IoT shopping applications for instance could track the smartphone location and learn about person's shopping preferences. Companies will then use this data to feed individuals with special offers for their favorite shops and products. A shopping app could also link to a smart fridge, which would decide what food is needed (based on past consumption) and send the grocery list directly to a persons phone. In fact, it is entirely possible that a smart fridge could order products automatically without any human interaction. There are several other examples and applications for IoT which can result in a higher standard of living. In this context, IoT becomes immensely

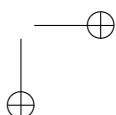
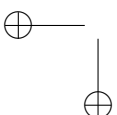




Figure 1.1: A graphical representation for the internet of things (IoT) concept [2]

important because it has the potential to deliver solutions that dramatically enhance every aspect of our life. It can improve energy, efficiency, security, health, education and many other aspects of people's daily life. For enterprises, IoT can also offer solutions that improve decision-making and productivity in industry, retail, agriculture and many other sectors. Already, IoT has realized the Internet sensory environment (temperature, pressure, vibration, light, moisture, stress), allowing us to become more proactive and less reactive [4]. In general, IoT can provide a higher quality of life for everyone. As a result, IoT will require high throughput communication networks to ensure instantaneous data updates and exchange. Consequently, the amount of generated Internet traffic by IoT is unprecedented. Besides, social networks, music and video streaming services (Netflix, Amazon) generate enormous amount of data everyday. This huge amount of data needs to be stored using cloud services. The physical implementations of the cloud services are the data centers (DCs).

1.2. Data centers

A data center is a huge infrastructure (size of a warehouse) that houses a massive number of computer systems interconnected together in a controlled environment. These computing resources include mainframes; web and applications servers, storage systems and equipped with highly-efficient power sources and cooling systems [5]. Fig. 1.3 shows the interior of a data center [6]. In data center networks, servers are mounted within separate racks and are interconnected to each other through top-of-rack (ToR) switch. These rack-level switches uplink connections to one or more cluster-level (or datacenter-level) Ethernet switches.



Figure 1.2: Potential Internet of things (IoT) applications [3]

This second-level switching domain can potentially span more than ten thousand individual servers. Fig. 1.4 shows the typical elements present in data centers [5]. Data centers require high capacity and high-speed interconnections to ensure efficient networking and immediate data accessibility in the cloud storage services. The unprecedented data growth has led to the development of large-scale public cloud data centers called hyper-scale data centers. According to Cisco's global cloud index, the amount of the annual global data traffic is estimated to be 20.6 Zettabytes (10^{21}) by 2021 [7]. This increase represents a 25% Compound Annual Growth Rate (CAGR). As a result, higher capacity data center networks are indispensable to cope with such massive data traffic in the coming years. Therefore, the hyper-scale cloud operators are increasingly dominating the cloud landscape. Giant corporations such as Google, Facebook, Amazon, and Microsoft use hyper-scale data centers to empower their cloud computing services. These hyper-scale data centers are predicted to grow from 338 in number at the end of 2016 to 628 by 2021 [7]. They will represent 53 % of all installed data center servers by 2021. In other words, they will account for 85 percent of the public cloud server installed base in 2021 and 87 % of public cloud workloads and compute instances.

1.3. Optical interconnects

In order to sustain the exponential growth in capacity and performance for data centers, major improvements in every segment of the DCs are required. The routing interconnections between the DC servers and switches are one of the most critical segments that can have a direct impact on the performance of the DC networks. Therefore, innovative interconnection schemes for communication between DC switches and servers (within rack &



Figure 1.3: An interior of a data center facility [6]

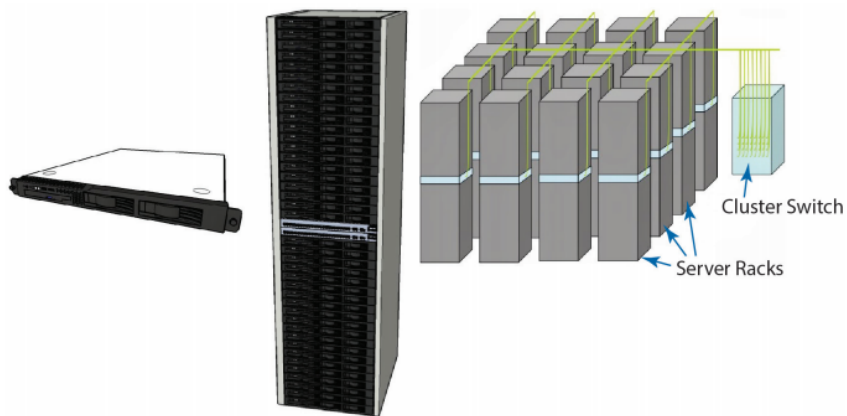


Figure 1.4: Sketch of the typical elements in warehouse-scale systems: 1U server (left), a rack with Ethernet switch (middle), and diagram of a small cluster with a cluster-level Ethernet switch/router (right) [5]

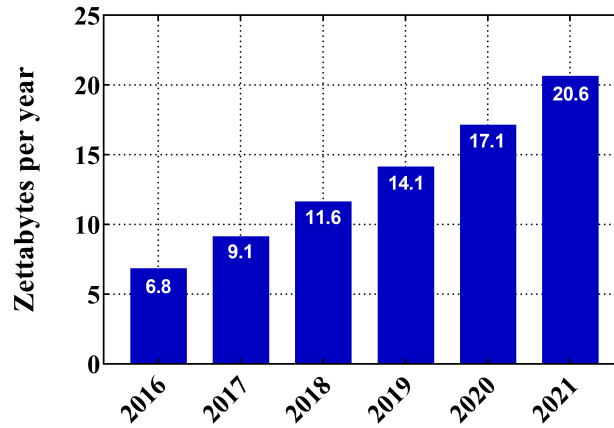


Figure 1.5: Cisco's prediction of the annual global data center traffic between 2016-2021 [7]

rack-to-rack) are essential. Optical interconnect based technology is a promising solution to address the growing capacity requirement of DC [8–11]. Over the last decade, optical interconnects have proven their potential for high-speed data communication [10]. The optical interconnect based technology mainly depends on the electro-optical transceivers for data transmission and detection. Multimode VCSEL-based optical links are widely dominating the data center market today because they are much cheaper on the component level (VCSEL and PD) [12]. The demand for higher data transmission capacity over long distances puts extra pressure on the data center vendors and operators to explore new technologies and approaches. Single-mode silicon photonics based DC interconnects have the potential to address the bandwidth-distance product requirements for future DCs [13, 14]. The 400 Gigabit Ethernet standard, which is defined by the IEEE P802.3bs 400 GbE Task Force, will need to utilize different advanced techniques to boost the single lane rate while maintaining a similar port density. One of the main challenges for future data centers communication is the integration between electronics and photonics ICs, which is the main focus of this thesis.

1.4. State-of-the-art electronic-photonic integration

Packaging of photonic integrated circuits (PICs) is one of the most critical challenges that still need to be addressed in order to enable true mass-market production [15–20]. Photonic packaging can significantly impact the performance and cost of the photonic system. The term "photonic packaging" refers to all the technical aspects related to the optical, electrical, thermal, and mechanical interfaces between the PIC and the outside world [21–26]. Fig.

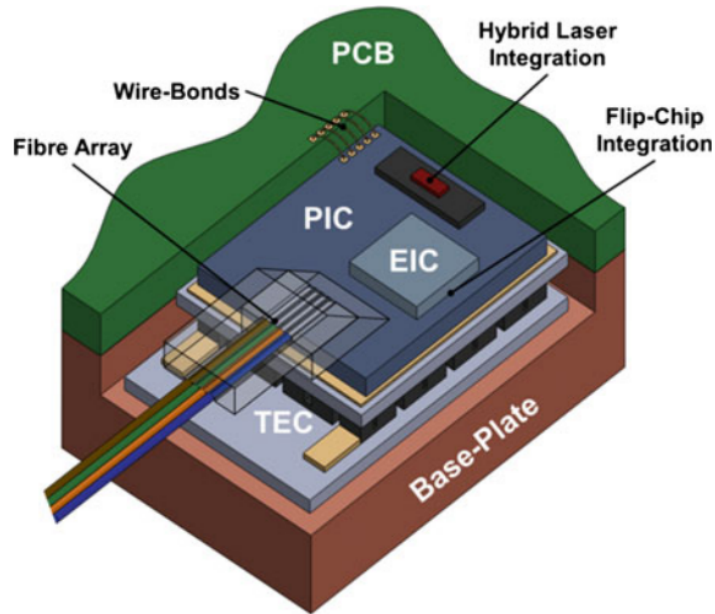
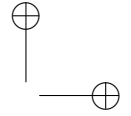
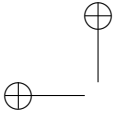


Figure 1.6: Schematic of the different elements covered by the photonic packaging of a Si-PIC wire-bonding for electrical contacting, fiber-arrays for optical packaging, flip-chip integration of an electronic-IC, hybrid integration of a laser source, and thermo-electric cooling (TEC) for temperature stabilization [27]

1.6 shows the key segments covered by photonic packaging [27]. This covers fiber-to-chip coupling, laser-source integration, chip assembly using wire-bonding, thermal management and flip-chip integration for efficient high-speed interconnections. Fiber-to-chip coupling is probably the most popular obstacle for photonic packaging. However, other issues such as electronic-photonics integration and thermal management also have a significant impact on the overall performance of the photonic device. In the context of this thesis, we will mainly focus on the electronic-photonics co-packaging particularly the electrical interface (high-speed interconnects) and the optical interface (fiber-to-chip coupling).

In real systems, photonic devices can not perform without interfacing electronics. Electronic ICs (EIC) and photonic ICs (PIC) need to be integrated together. There are different approaches for electronic-photonics integration in which electronic and photonic ICs are combined together. Fig. 1.7 shows different concepts for electronic-photonics integration [28].

- Side-by-side integration using wire bonding [29]. Although wire bonding technology is the most widely used method for electro-photonics co-packaging, it has limitations at high frequency applications due to the high parasitic inductance of the wires.



1.4 State-of-the-art electronic-photonic integration

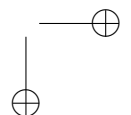
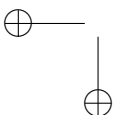
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- Flip chip: both the PIC and EIC are flip-chipped on an interposer.
- Vertical integration: the EIC is flip-chipped on the PIC and the electrical connections is realized using solder-ball-bumps or copper-pillar-bumps [22, 25, 30–32].
- 3D stacking: the PIC is mounted on the EIC and electric connections were realized using through-silicon-via (TSV) and in some cases through-oxide-via (TOV) [33].

Flip-chip and through-silicon via technologies are proven to be a good alternative to to the wire bonding technology particularly at high frequencies [34] as they replace the long wire (100-500 μm) with very short vertical microbump interconnects (10 μm), which minimize the effect of the parasitic inductances [35, 36]. However, those technologies are still less flexible and very expensive compared to the wire-bonding technology

- Monolithic integration of electronic and photonic functions onto a single chip is considered as the ultimate solution to provide a very tight electronic-photonic integration. Either CMOS electronic functionalities can be added on a photonic chip [23, 37, 38] or photonic functionalities can be added on a CMOS electronic chip [39–44]. However, this solution still has several challenges and obviously is not the best economic approach. On the other hand, hybrid integration of electronic and photonic ICs on two separate chips is still the most economic solution because it enables using different CMOS technology nodes for both PICs and EICs [45]. In other words, the fabrication tolerances of PICs can be realized by the 45 nm node on relatively low-cost 200 mm wafers, while high-performance cost-effective electronic-ICs (EIC) may require the 14 nm node on 300 mm wafers. The footprint of a PIC (10 – 30 mm^2) is typically larger than the EIC due to the large photonic segments such as arrayed waveguide gratings (AWG) and delay-lines besides the reserved space for Fiber-to-PIC coupling. This additional space for the PIC will be only for the least expensive CMOS node. Hence, separating the CMOS nodes will result in a significant reduction in the overall cost. [25].

Other electro-photonic packaging approaches have been reported by TU/e [46, 47] as shown in Fig. 1.8. In the first approach [46], a wet etching process is employed to create a 3D silicon interposer in which the electronic and photonic ICs are mounted and flip-chipped after electro-plating of the electrical traces. A 12-channel transmitter and receiver submodules are developed based on this approach at 10 Gb/s per channel. The second approach [47] is based on bonding the photonic chip face-up on the electronic IC. Then, a mechanical support is created at the PIC edge by reflowing a photoresist to form a ramp between the PIC and EIC. The electrical metallization was realized by electrical plating. The optical transmitter was demonstrated at 12.5 Gb/s. Although, those approaches provide a promising solution for electro-photonic integration, they lack the flexibility and low-cost advantages of other conventional technologies such as wire-bonding.



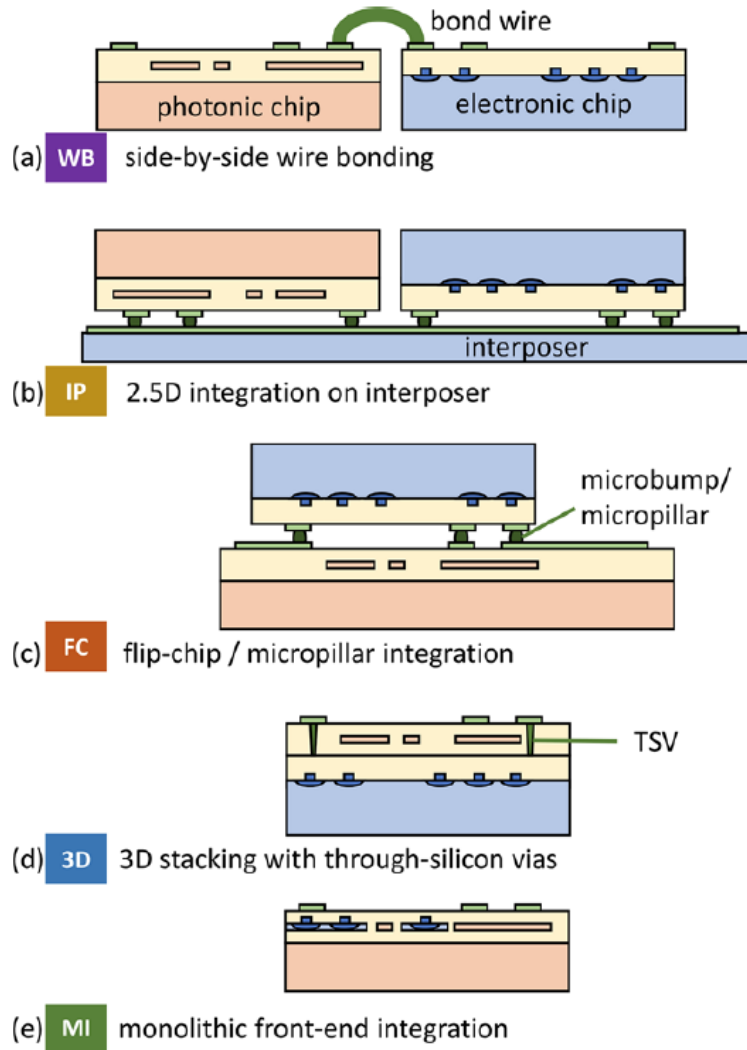


Figure 1.7: Different approaches for photonic-electronic integration [28]

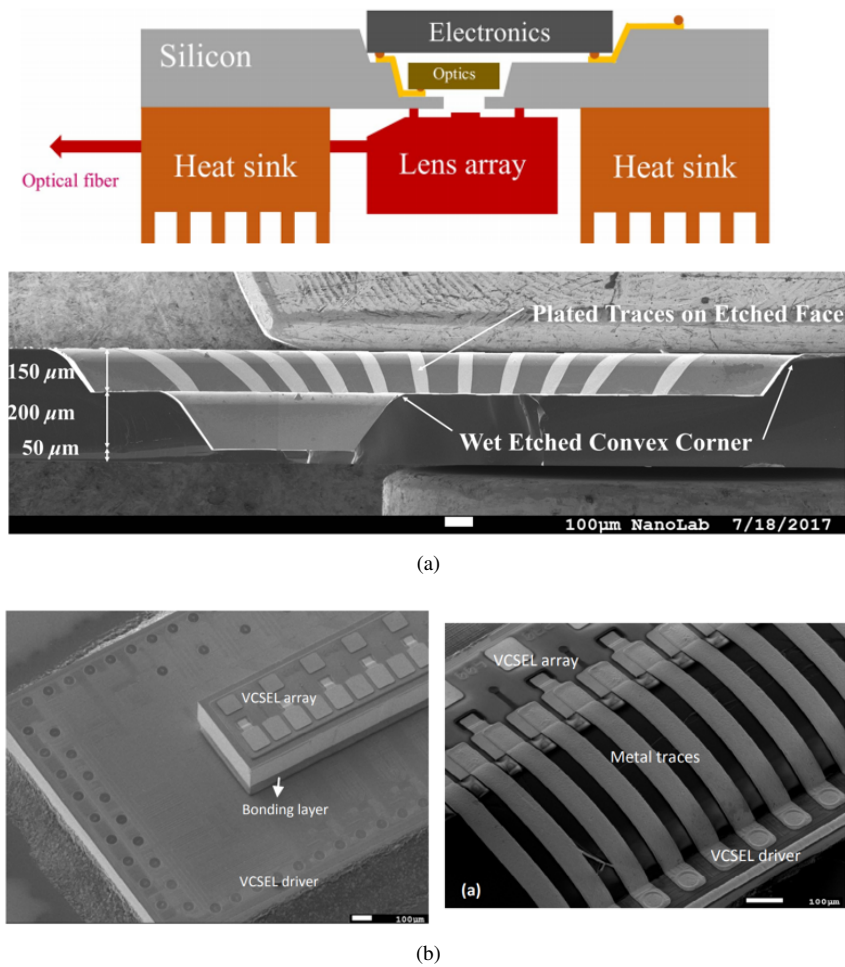
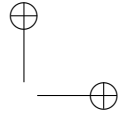
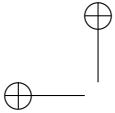


Figure 1.8: TU/e electro-photonic integration approaches (a) wet-etched silicon interposer approach (b) 3D stacking of PIC on EIC [46, 47]



1.5. Challenges for electronic-photonic integration

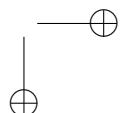
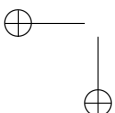
As discussed before, photonic packaging is crucial for the real mass market deployment of photonic devices. A lot of research in this area is ongoing in order to operate the photonic devices at high-speed and with very high bandwidth to meet the data rate requirements for datacom applications. The current challenges for photonic packages as mentioned before include fiber-to-chip coupling, electronic-photonic packaging, laser-source integration, and thermal management. In the context of this work we will only discuss the challenges for electronic-photonic integration including electrical interconnects and fiber-to-PIC coupling, which we are trying to overcome.

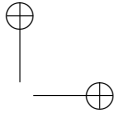
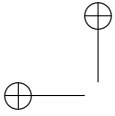
1.5.1. High-speed electrical interconnects

Electrical interconnects are considered one of the most prominent challenges for electronic-photonic integration. Typically, most of the photonic ICs are interfaced with the electronic ICs using traditional wire-bonding technology [48] owing to their flexibility and reliability. However, at high frequency, the bondwire itself can be a major problem due to the parasitic inductance induced by the wire and the longer the bondwire the higher the parasitic inductance. This parasitic inductance at high frequency will cause high reflections and losses and eventually will limit the bandwidth. To reduce parasitic induction effects, bondwires should be as short and straight as possible. Additionally from a design perspective, it is also difficult to control the wire loop shape and dimensions. An alternative solution could be to shift from round bondwires to ribbon wires [49]. This can provide more consistent loop profiles because of the ribbon wire's rectangular shape. In addition, the impedance and inductance at high frequencies is lower for ribbon wire, because of the large surface area with respect to the cross-sectional area, thus reducing the impact of the skin effect. Despite those advantages, ribbon bonding for RF applications is still very critical, and less flexible since wires can only be realized in one orientation. Therefore, new flexible low-cost methods are essential in order to realize electrical interconnects with the capability of tuning the dimensions and hence the characteristic impedance. In this case, electrical interconnects could be designed to support high bandwidth by developing impedance matched transmission lines to minimize reflections and signal attenuation.

1.5.2. Fiber-to-PIC coupling

Fiber-to-chip coupling is probably the most discussed obstacle in photonic packaging [50–54]. The main challenge is to couple the light from standard single-mode fibers (SSMF) and silicon photonic waveguides. SSMF has a mode field diameter of about $10.4 \mu\text{m}$ at a wavelength of 1550 nm while the silicon-on-insulator (SOI) waveguides has a typical cross section area of about $0.45 \mu\text{m} \times 0.22 \mu\text{m}$ [55]. This large MFD mismatch between SSMF and SOI waveguides causes relatively high coupling loss. Therefore, there has been a lot of research in this area to efficiently couple the light from SSMF to PIC.





There are mainly two approaches for coupling the light from SSMF to PIC; surface grating couplers and edge couplers.

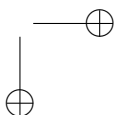
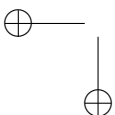
Grating couplers

Grating couplers consist of sub-wavelength periodic structures etched in the SOI platform, which diffracts the light from a near normally (typically around 10°) incident SSMF into the SOI waveguide as shown in Fig. 1.9 [56, 57]. The foot print of a typical grating coupler is about $10\ \mu\text{m} \times 10\ \mu\text{m}$, which is chosen to match the MFD of a SSMF. The most distinct advantage of grating couplers is that they enable wafer-level optical testing. This means they can be placed at any location on the wafer without requiring any additional post-processing such as dicing and polishing. They are also more alignment-tolerant than edge couplers [58]. However, they are sensitive to polarization and wavelength-dependent. Furthermore, from packaging perspective, fiber-to-PIC coupling in case of using a grating coupler will be challenging as attaching a fiber under a near-normal angle will create a bulky device with poor mechanical performance. To overcome this issue, an additional polishing process for the fiber facet [25, 59, 60] to create an angle of approximately 40° so that total internal reflection can be achieved to deflect the light onto the grating-coupler at the correct angle of 10° . In this case, the fiber can be packaged in the same PIC plane.

Edge couplers

The alternative approach to grating couplers is using edge couplers. Typically, edge couplers offer lower insertion loss than grating couplers. Edge coupler is already used in packaging of commercial laser-chips [61]. An edge coupler typically consists of an inverted taper (with a length of $100\text{-}300\ \mu\text{m}$) embedded in an integrated silicon nitride or silicon oxide-based spot size converter (SSC) as shown in Fig. 1.9 [17, 57, 62, 63]. The SSC can also be developed in a polymer waveguide using an additional post-processing [64, 65]. In this case the MFD of SSMF matches the mode of the SSC and the light is then adiabatically coupled to the SOI waveguide [51, 66]. Edge couplers are typically broadband and polarization tolerant unlike grating couplers. However, they require to be located at the PIC edge and hence they need post processing to create the coupling facet using dicing and polishing if necessary. As mentioned, the edge couplers approach is less alignment-tolerant compared to grating couplers. However, recent advances in edge couplers reported that a misalignment of $\pm 2\ \mu\text{m}$ for the SSC with respect to the inverted Si taper results in a penalty of about 1 dB [67].

Both edge and grating couplers approaches have their own advantages and drawbacks. Therefore, the application and the cost will determine which approach is chosen to meet the specific requirements defined by the application.



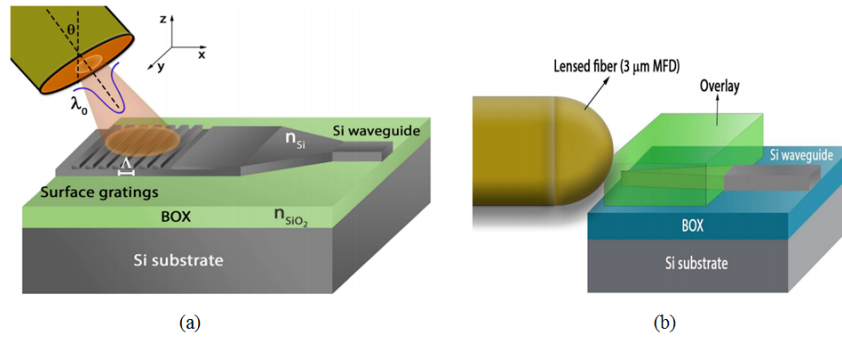


Figure 1.9: Schematic of the different approaches for fiber-to PIC coupling (a) surface grating couplers (b) edge couplers [57]

1.6. Scope of the thesis

The goal of this research is to enable the hybrid integration of electronic and photonic integrated circuits using flexible adaptive technologies. In this work, we developed two process technologies to realize electrical and optical interconnects for photonic packaging. The electrical interconnects are realized using aerosol-jet printing (AJP) technology to print the high-speed interconnects between PIC and EIC. The optical interconnects are based on single-mode (SM) polymer waveguides, which are developed using direct-write lithography (DWL). Fig. 1.10 shows the schematics of the developed approach to enable hybrid electronic-photonic integration. The two approaches for developing the electrical and optical interconnects are implemented on a separate interposer as illustrated in Fig. 1.10a and Fig. 1.10b. However, they might be combined on the same interposer as suggested in Fig. 1.10c.

1.6.1. AJP for electronic-photonic integration

AJP technology enables printing very short electrical interconnects (100-300 μm) with a pitch of 50 μm between PIC and EIC, thus minimizing the parasitic inductance for high-speed transceivers. It offers tuning the characteristic impedance of the printed transmission lines (TLs) by controlling their dimensions (width, thickness, and spacing) in order to design impedance-matched transmission lines, thus reducing signal reflections and attenuation. This feature can have a significant impact on the device performance. For example, in order to interconnect a traveling-wave electrode Mach-Zehnder modulator, it requires a 50 Ω transmission line to match its 50 Ω RF terminations [68]. Otherwise, the signal reflections will be relatively high. This 50 Ω transmission line can not be realized using wire bonding technology. The AJP technology can show great potential in such application where high resolution impedance-matched interconnects are required. Furthermore, it also enables printing 3D interconnections from chip to the interposer (PCB).

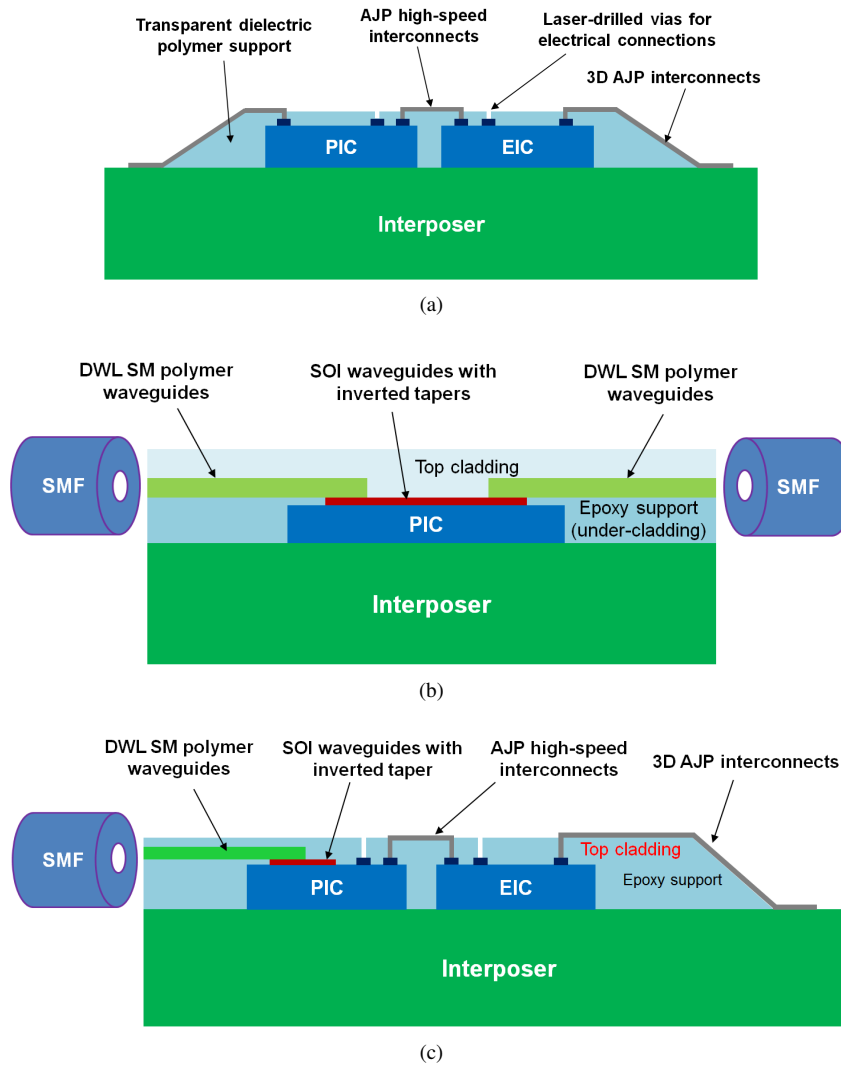


Figure 1.10: Schematics of the proposed approach for electronic-photonic integration (a) AJP approach for electronic-photonic interconnection (b) adiabatic spot size converter between DWL SM polymer waveguides and SOI waveguides (c) possible integration concept for combining both approaches

In this aspect, multiple silver ink materials are experimented with the AJP technology and one ink is selected based on the results of the experiments. The printing process is further optimized for this specific ink. Then, coplanar waveguide transmission lines are designed and fabricated by AJP on different substrates. Next, a process flow for electronic-photonic interconnection is developed. Different optical transmitters based on the integration of PICs and electronic driver ICs are demonstrated at high-speed up to 60 Gb/s. Furthermore, a direct comparison between the developed assembly using AJP and the wire-bonded assembly is performed. The AJP assembly showed better performance at high frequency.

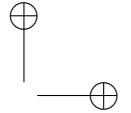
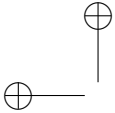
1.6.2. DWL of SM polymer waveguides for adiabatic coupling to SOI waveguides

As for the optical interconnects part, a process to fabricate single-mode polymer waveguides was developed using two different material systems. Based on the measurements of refractive indices of the polymer materials, the required single-mode dimensions are calculated at wavelengths of 1.31 μm and 1.55 μm . The DWL exposure parameters are optimized for the core materials to provide a good control for the waveguide dimensions. Then, the polymer waveguides are patterned at the optimum exposure parameters. Additionally, SM polymer waveguide crossings are also realized using the two materials to provide more complex routing for the optical interconnects. The characterization of the fabricated waveguides is performed by measuring the propagation losses using the cut-back method both at 1.31 μm and 1.55 μm . Next, a process flow is developed to demonstrate the adiabatic coupling between the DWL SM polymer waveguides and SOI waveguides. The SM polymer waveguides in this approach act as spot size converters (SSC) between SSMF and SOI waveguides. The insertion loss per facet is measured and the adiabatic coupling loss is estimated. The main advantage of this approach is that the SM polymer waveguides are extended from the PIC till the package and the polymer waveguides act as an optical fanout.

1.7. Thesis outline

In chapter 2, the aerosol-jet printing technology will be presented including the state-of-the-art applications particularly in the area of electrical interconnects and RF transmission lines. Experiments using different nanoparticle silver inks and the optimization of the printing process will also be demonstrated. Next, sintering and curing of the printed electrical interconnects will be illustrated. Finally, the realization of coplanar waveguide transmission lines will be demonstrated, and compared to simulations.

In chapter 3, the AJP high-speed interconnects will be used to interconnect electronic and photonic ICs in order to develop optical transmitters for data center applications. The fabrication process flow for the AJP based electronic-photonic integration will be described. Then, the functionality of the process technology is tested on daisy-chain test chips. In addition, 85°C/85% RH reliability test is performed in order to investigate the



reliability of the realized printed interconnects. Next, a comparison between the aerosol-jet printed interconnects and the traditional bonding wires will be provided. Finally, different high-speed optical transmitters assemblies will be demonstrated.

In chapter 4, optical interconnects based on single-mode polymer waveguide are developed by direct-write lithography. Two optical material systems including epoxy and siloxane polymers are utilized. The cut-off single-mode waveguide dimensions are calculated for both the core materials using a numerical mode solver. Next, the fabrication process flow of the polymer waveguides will be described. In particular, a focus will be put on the direct-write lithography process and the corresponding optimization of patterning the core materials. The characterization results of the fabricated waveguides will be introduced including the cut-back measurements at datacom wavelengths.

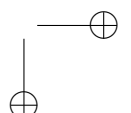
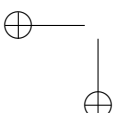
In chapter 5, an adiabatic coupling approach between SOI waveguides and the developed DWL polymer waveguides is demonstrated. The fabrication process flow will be described and the characterization results including the total insertion loss and the adiabatic coupling loss will be presented.

In chapter 6, the main achievements and future work are summarized.

1.8. Research dissemination

1.8.1. Papers published in an SCI-journal

- **Ahmed Elmogi**, Hannes Ramon, Joris Lambrecht, Peter Ossieur, Guy Torfs, Jeroen Missinne, Peter De Heyn, Yoojin Ban, Marianna Pantouvaki, Joris Van Campenhout, and Geert Van Steenberge, "Aerosol-Jet Printed Interconnects for 60 Gb/s CMOS Driver and Microring Modulator Transmitter Assembly," *IEEE Photonics Technology Letters* vol. 30, no. 22, pp. 1944-1947, 15 Nov.15, 2018, DOI: 10.1109/LPT.2018.2873056.
- **Ahmed Elmogi**, Wouter Soenen, Hannes Ramon, Xin Yin, Jeroen Missinne, Silvia Spiga, Markus-Christian Amann, Ashwyn Srinivasan, Peter De Heyn, Joris Van Campenhout, Johan Bauwelinck and Geert Van Steenberge, "Aerosol-Jet Printed Interconnects for 2.5D Electronic and Photonic Integration," *Journal of Lightwave Technology* vol. 36, no. 16, pp. 3528-3533, 2018, DOI: 10.1109/JLT.2018.2848699.
- Manuel Cao-Garca, **Ahmed Elmogi**, Marie-Aline Mattelin, Jeroen Missinne, Morten A. Geday, Jos M. Otn, Geert Van Steenberge, and Xabier Quintana, "All-organic switching polarizer based on polymer waveguides and liquid crystals," *Opt. Express* 26, 9584-9594 (2018), DOI: 10.1364/OE.26.009584.
- **Ahmed Elmogi**, Erwin Bosman, Jeroen Missinne and Geert Van Steenberge "Comparison of epoxy- and siloxane-based single-mode optical waveguides defined by direct-write lithography" *OPTICAL MATERIALS Elsevier*. Vol. 52. 2016. 26-31, DOI: 10.1016/j.optmat.2015.12.009.



1.8.2. Papers presented at international/national conferences

- **Ahmed Elmogi**, Andres Desmet, Jeroen Missinne, Hannes Ramon, Joris Lambrecht, Marianna Pantouvaki, Peter De Heyn, Joris Van Campenhout, Johan Bauwelinck, and Geert Van Steenberge, "Adaptive Patterning of Optical and Electrical Fan-out for photonic chip packaging" accepted for publication in ECTC 2019, Las Vegas, USA.
- Manuel Cao-Garca, **Ahmed Elmogi**, Jeroen Missinne, Morten A. Geday, Jos M. Otn, Xabier Quintana, Geert van Steenberge "All-organic integrated LC optical cross-connect" Conference on Liquid Crystals - Chemistry, Physics and Applications, 2018.
- **Ahmed Elmogi**, Wouter Soenen, Erwin Bosman, Jeroen Missinne, Silvia Spiga, M.-C. Amann, Johan Bauwelinck, and Geert Van Steenberge. Flexible hybrid integration of photonic and electronic chips using aerosol-jet printing. Annual Symposium of the IEEE Photonics Benelux Chapter, Proceedings. IEEE Benelux photonics Chapter, Delft, Netherlands, 2017.
- Jeroen Missinne, **Ahmed Elmogi**, Marie-Aline Mattelin, and Geert Van Steenberge "Flexible photonic sensors realized using printing technologies" 7th EOS topical meeting on optical microsystems 2017.
- Jeroen Missinne, Nuria Teigell Beneitez, Marie-Aline Mattelin, **Ahmed Elmogi**, Erwin Bosman, and Geert Van Steenberge, Polymer Micro- and Nanophotonic Sensors Realized Using Replication Technologies. In Proceedings Symposium IEEE Photonics Society Benelux, 183186. Gent, Belgium, 2016
- Jeroen Missinne, Anton Vasiliev, **Ahmed Elmogi**, Nuria Teigell Benítez. Erwin Bosman, Bram Van Hoe, and Geert Van Steenberge. "Bragg grating sensors in laser-written single mode polymer waveguides." *Procedia Engineering 120 (2015): 878-881.*

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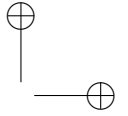
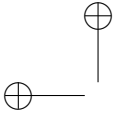
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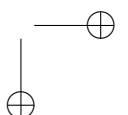
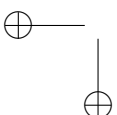
2

Aerosol-Jet printing of electrical interconnects

This chapter will focus on the application of aerosol-jet printing technology in developing electrical interconnects and RF transmission lines. The aerosol-jet printing technology and its applications will be introduced. In particular, we will focus on state-of-art high-speed RF transmission lines. Then, the AJP process will be explained in detail. Experiments using different nanoparticle silver inks and the optimization process will also be discussed. Next, sintering and curing of the printed electrical interconnects will be illustrated. Finally, the realization of coplanar waveguide transmission lines will be demonstrated, and compared to simulations.

2.1. Introduction

Transmission lines and electrical interconnects are indispensable elements in electronic systems. The electrical interconnects and passive elements occupy over 50% of the total area of the printed circuit boards. To a large extent, the total cost and the system performance are highly influenced by the technologies involved in realizing the electrical interconnects. Nowadays, the conventional technologies used for developing electrical interconnects typically require expensive and complex lithographic processes. They also lack the flexibility of processing on flexible substrates such as PET foil (Polyethylene terephthalate) and plastic substrates. Therefore, there is an increasing demand to develop electrical interconnects with new flexible technologies that can significantly reduce the



cost and sustain the accuracy and performance.

For high-speed electro-optical systems, low parasitic electrical interconnects are essential in order to enhance the bandwidth, decrease the power consumption, and improve the data signal transmission, thus improving the transceiver performance. In this chapter, we will present the aerosol-jet printing (AJP) technology and its application in developing high-speed interconnects and transmission lines. The AJP technology offers promising advantages in the area of realizing transmission lines. For example, the AJP technology enables tuning the characteristic impedance of the realized transmission lines. This means that the dimensions (width, thickness, & spacing) of the electrical interconnects can be tuned to achieve a desired characteristic impedance (e.g., $50\ \Omega$ to minimize signal reflections) or to obtain well-controlled parasitics (e.g. for bandwidth enhancement through inductive peaking), thus improving the transceiver performance. Therefore, the AJP technology is considered as a promising approach and a low-cost alternative solution to the conventional technologies in order to develop high-performance transmission lines.

2.2. State-of-the-art

Over the past years, additive manufacturing technologies have emerged as an alternative to the traditional subtractive technologies since they are cost-effective, flexible, environmentally-friendly and compatible with flexible substrates. Inkjet printing and AJP are two examples of the additive manufacturing technologies that showed promising potential in various applications. Inkjet printing [1] has emerged before AJP. As a result, inkjet printing has been extensively investigated in different research aspects especially in the field of printed electronics [2, 3]. In particular, inkjet printing has been widely employed in RF/microwave applications [4–9] including the realization of transmission lines [10–15]. However, inkjet printing still has limitations [16] related to printing high resolution features in addition to the limited range of the ink viscosity. Therefore, AJP technology was introduced to overcome the limitations of inkjet printing and offers additional promising features. A detailed comparison between the inkjet printing and AJP is reported in [17, 18]. AJP technology was developed by Optomec, Inc and the first generation of AJP system for printed electronics was commercially available since 2008. Since then, the AJP technology was explored in several applications. The AJP technology offers promising features over inkjet printing in terms of higher resolution, 3D printing capability, and a broader range of material viscosity.

The AJP technology was used to print the front side metallization for silicon and organic solar cells [19–21]. A thin-film transistor made using single-walled carbon nanotube was printed using AJP [22, 23]. Aerosol-jet printed sensors onto pre-packaged integrated circuits (ICs) were recently developed [24]. Furthermore, AJP technology has already been reported to enable 3D printed electronics such as resistors, capacitors, antennas, and sensors [25]. The most interesting application in the context of this dissertation is the development of electrical interconnects and transmission lines for high-speed RF interconnects. Hence, 3D multi-layer transmission lines were recently developed by

stacking multiple layers of polyimide and silver using a dual-printhead AJP system [26, 27]. Both the polyimide and silver layers were directly printed using aerosol-jet technology. The aerosol-jet printed transmission lines showed promising RF behavior up to 40 GHz. The loss of the stripline was reported to be 0.53 dB/mm at 40 GHz. Furthermore, coplanar waveguide (CPW) transmission lines were printed on a single-crystalline diamond (SCD) substrate using AJP [28]. The measured loss of the transmission lines is found to be 0.46 dB/mm at 40 GHz. The developed CPWs can be utilized for integrated high power RF electronic systems.

2.3. Aerosol-jet printing

AJP is an additive manufacturing technique (drop-on-demand) which allows depositing materials with a wide range of viscosities, directly on planar and non-planar surfaces, with micrometer resolution, and can deposit an extremely wide range of materials, including metallic inks and dielectrics. Fig. 2.1 shows the aerosol-jet system installed in the UGent cleanroom. The AJP technology offers the following features:

- AJP technology can deposit a wide range of material with different viscosities. The inks can have a viscosity ranging from 1 to 1000 cP, which is much wider with respect to other printing technologies such as inkjet printing.
- AJP can achieve a minimum line width of 10 μm and a thickness ranging from 100 nm to 5 μm per printing pass.
- The technology enables in-situ local laser sintering, which can be an essential requirement for flexible and low-temperature substrates.
- It offers 3D printing capability as the material particles (aerosol) exiting the printing nozzle remain focused over a distance up to 5 mm. Hence, the variable printing standoff distance enables printing on non-planar or curved surfaces.
- It achieves an alignment accuracy of $\pm 1\mu\text{m}$.

2.4. Aerosol-jet printing process

An aerosol is generally defined as a suspension of small particles in air or in another gaseous environment. The aerosol can be generated by a process called atomization, which is defined as the process of breaking up bulk liquids into droplets. Hence, the aerosol-jet process is simply based on creating an aerosol from a functional liquid ink by means of atomization, then transporting the aerosol to the deposition head and finally focusing the aerosol stream on the substrate by a nitrogen (N_2) flow. The technology supports two different atomizers for creating the aerosol: pneumatic atomizer (PA) & ultrasonic atomizer (UA). The viscosity of the ink and the type of solvents (low boiling point or high

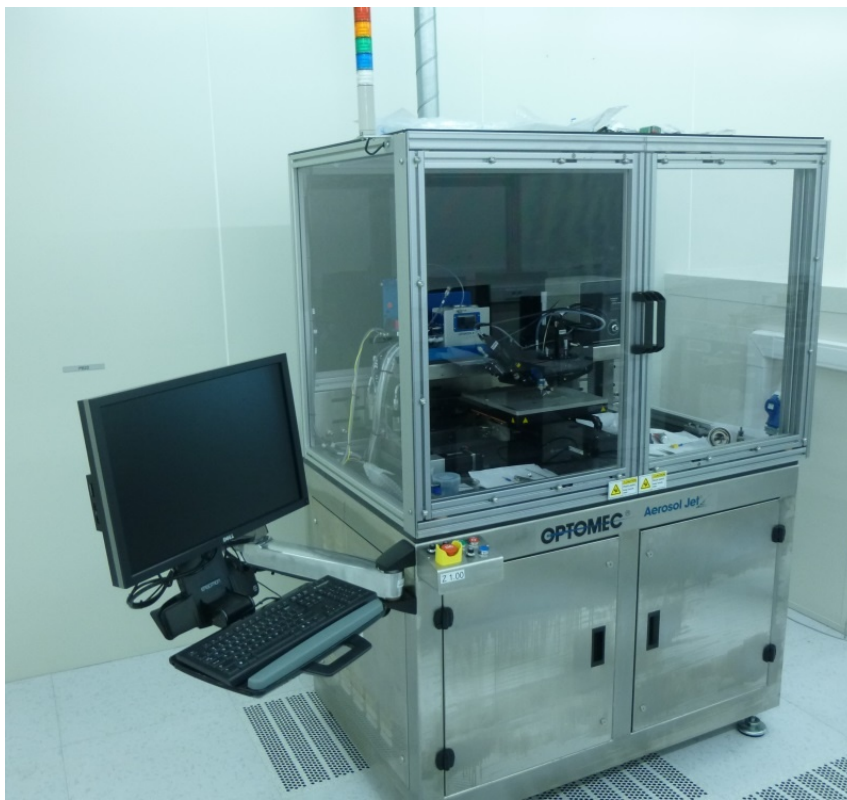


Figure 2.1: Aerosol-jet printer in UGent cleanroom

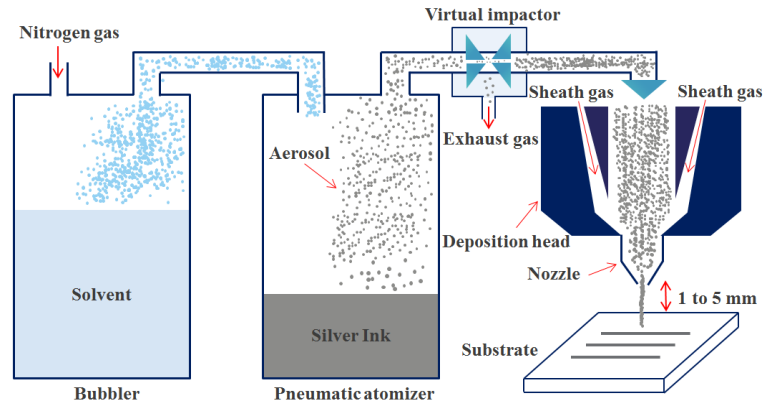


Figure 2.2: Aerosol-jet process with the pneumatic atomizer

boiling point) determine which atomizer can be used. Inks with low viscosity (1-20 cP) are used with the ultrasonic atomizer, while inks with higher viscosity (20-1000 cP) are used with the pneumatic atomizer. The main differences between the pneumatic and ultrasonic atomizers are summarized in table 2.1. In this work, we used both the pneumatic and ultrasonic atomizers to print silver inks on glass substrates.

2.4.1. AJP process with pneumatic atomizer

Fig. 2.2 shows the aerosol-jet printing setup using the PA. The silver ink was placed into the pneumatic atomizer in which the aerosol is generated. A bubbler containing a solvent was added to the setup to compensate the loss of solvent from the ink during the atomization process. Typically, the solvent with the highest volatility is placed in the bubbler. In this case the nitrogen flow entering the PA is wetted with the most volatile solvent in the ink. As a result, an aerosol of droplets between 1-5 μm in diameter is generated. Drops larger than about 5 microns cannot overcome the force of gravity and drop back into the ink and are recycled. Then, the aerosol is transported by the nitrogen stream to the deposition head. Before reaching the deposition head, the virtual impactor removes the excess air (exhaust gas) and increases the aerosol density. Within the deposition head, the aerosol is focused by a second N_2 flow called the sheath gas which surrounds the aerosol as an annular ring. The resulting high-velocity converging particle stream is deposited onto the substrate creating the very fine features. The aerosol stream exiting the nozzle remains focused over a working distance between 1-5 mm. This feature enables the 3D printing capability of the technology. The parameters that need to be optimized while using the pneumatic atomizer include the atomizer gas flow rate, sheath gas flow rate, exhaust gas flow rate, stage speed, substrate temperature, and the stand-off distance between the nozzle and substrate.

Table 2.1: Comparison between pneumatic and ultrasonic atomizers

Pneumatic atomizer	Ultrasonic atomizer
suitable for viscous inks (20-1000 cP)	suitable for low-viscous inks (1-20 cP)
with low vapor pressure (≤ 0.1 mmHg)	with high vapor pressure
and high boiling point ($> 180^\circ C$) solvents	and low boiling point solvents (volatile solvents)
particle size can be large (> 50 nm)	particle size should be small (< 50 nm)
requires an ink quantity of 30 ml	requires an ink quantity of 1 ml
can achieve a minimum feature of $20\ \mu\text{m}$	can achieve a minimum feature of $10\ \mu\text{m}$
minimum thickness of $3\ \mu\text{m}$ per pass	minimum thickness of $100\ \text{nm}$ per pass
example of materials: metallic inks (metal content $> 55\%$ wt)	example of materials: metallic inks (metal content $< 50\%$ wt)
UV curable polymers	aqueous and organic semiconductor inks

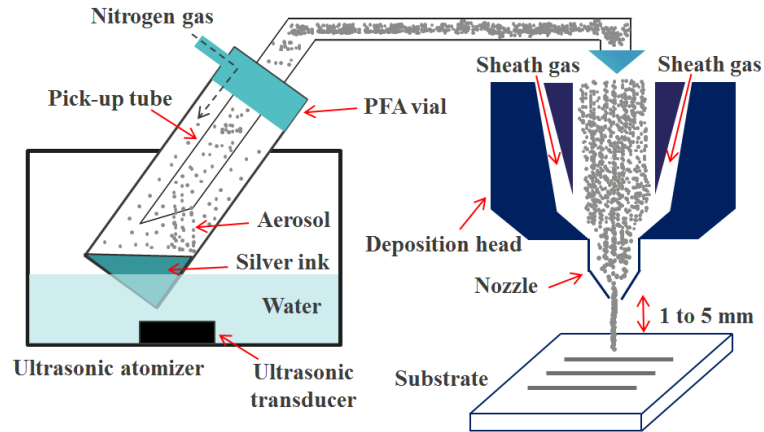


Figure 2.3: Aerosol-jet process with the ultrasonic atomizer

2.4.2. AJP process with ultrasonic atomizer

Fig. 2.3 shows the aerosol-jet printing setup using the UA. The silver ink was placed into a PFA vial (PerFluoroAlkoxy) in a water bath (coupling fluid) positioned above an ultrasonic transducer. The transducer vibrates at ultrasonic frequencies and produces perturbations that eject small droplets from the ink surface to form the aerosol. The ultrasonic energy is transferred through the water and the atomization vial to the ink. The Nitrogen flow is circulated in the vial containing the ink in order to facilitate creating the aerosol and to transport the generated aerosol to the deposition head. The parameters that need to be optimized while using the ultrasonic atomizer include the atomizer gas flow rate, sheath gas flow rate, ultrasonic power, stage speed, substrate temperature, and the stand-off distance between the nozzle and substrate. The position of the pick-up tube inside the the PFA vial is also very critical for creating very dense aerosol output.

2.5. Experiments with silver inks

There are different factors that should be considered before using the aerosol-jet technology such as the ink properties, substrate properties and printing resolution. The most important factor is the ink or the material properties that will be printed. Development of suitable inks or materials is one of the major challenges for additive manufacturing technologies in particular for AJP [29]. The developed inks for aerosol-jet printing require the capability of creating an aerosol from the liquid inks. In principle, metallic inks consist of metal nanoparticles, solvents, binding agents and adhesion particles. The developed inks should have good jetting properties. Additionally, the physical properties such as viscosity, surface tension and contact angle are critically important to ensure reliable printing process [30].

Moreover, the chemical properties of the inks should also be compatible with the printheads or nozzles [31]. The ink viscosity should be in a range between 1 to 1000 cP in order to enable atomizing the ink by generating an aerosol from the liquid ink. We used commercially-available metallic inks which are compatible with the aerosol-jet technology. The ink can be printed using either the ultrasonic or the pneumatic atomizer based on the viscosity and the solvents existed in the ink. In this work, we focused on silver inks that can be used as a conductive material for the electrical interconnects. We used different inks for both the ultrasonic and pneumatic atomizer.

We used three different silver inks from different suppliers, which are compatible with AJP. The first ink is a nanoparticle silver ink from UT dots and is commercially known as "UTDAg 40". The second ink is originally formulated in a Xerox research center in Canada and is commercially known as "xcm-nsPA". The third ink is a nanoflakes ink from Novacentrix and is known as "Metalon HPS030 AE1". Out of these 3 inks, the novacentrix ink is selected based on a number of printing experiments and it is more suitable for the final application for developing electrical interconnects at high-frequency applications. A further detailed process optimization for the selected ink "Novacentrix" will be presented in section 2.6. In this section, the experiments with the 3 different inks will be demonstrated.

2.5.1. UT dots silver ink

A silver nanoparticle ink from UT Dots (UTDAg 40) was used with the ultrasonic atomizer. The ink showed good printing quality on glass substrates. The achieved thickness of this ink was about 200 nm per pass while the stage speed was set at 3 mm/s. Since, the goal was to develop conductive traces with a thickness of a few micrometers, that required applying multiple passes in order to obtain a thicker trace. Fig. 2.4 shows the printed traces of the UT Dots silver ink on a glass substrate for printing single pass and multiple passes (6 passes). A thickness of 1.3 μm was achieved after stacking 6 passes. Additionally, Fig. 2.5 shows the profile optical measurements for the printed traces. However, the printing quality started to degrade after applying multiple passes. The width and the profile of the printed traces were also not uniform along the traces after applying 6 passes. Stacking more than 6 passes of this ink results in a bulging effect along the printed traces, thus degrading the quality. Hence, we stopped the activity with the UT Dots ink as the results were not suitable for the desired application.

2.5.2. Xerox silver ink

We tested another silver nanoparticle ink from Xerox called xcm-nsPA, which is originally developed for the pneumatic atomizer so that relatively thick traces can be printed from a single pass. The ink showed bad adhesion on glass substrates as shown in Fig. 2.6. Cracks were directly observed after printing on glass substrates. This can be attributed to the high surface energy of glass and the ink didn't adhere well to glass. This ink also contains low-boiling additives that tend to evaporate quickly leading to ink drying and causing

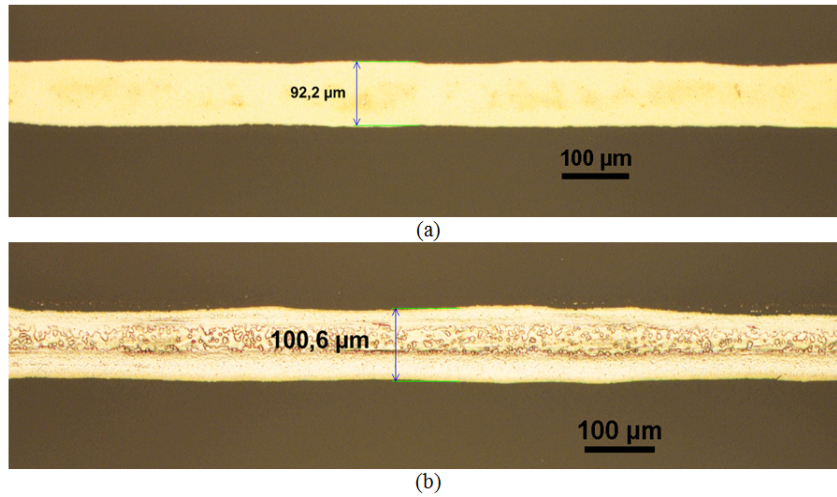


Figure 2.4: Aerosol-jet printed traces using UT dots nanoparticle silver ink (a) one pass printing (b) applying 6 printing passes

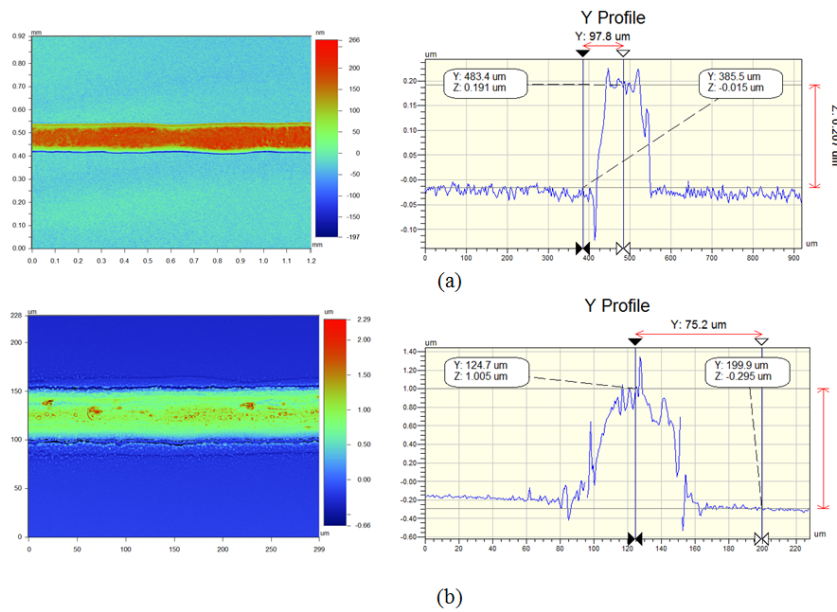


Figure 2.5: Optical profiler measurements (wyko) of the aerosol-jet printed traces using UT dots nanoparticle silver ink (a) one pass printing (b) applying 6 printing passes

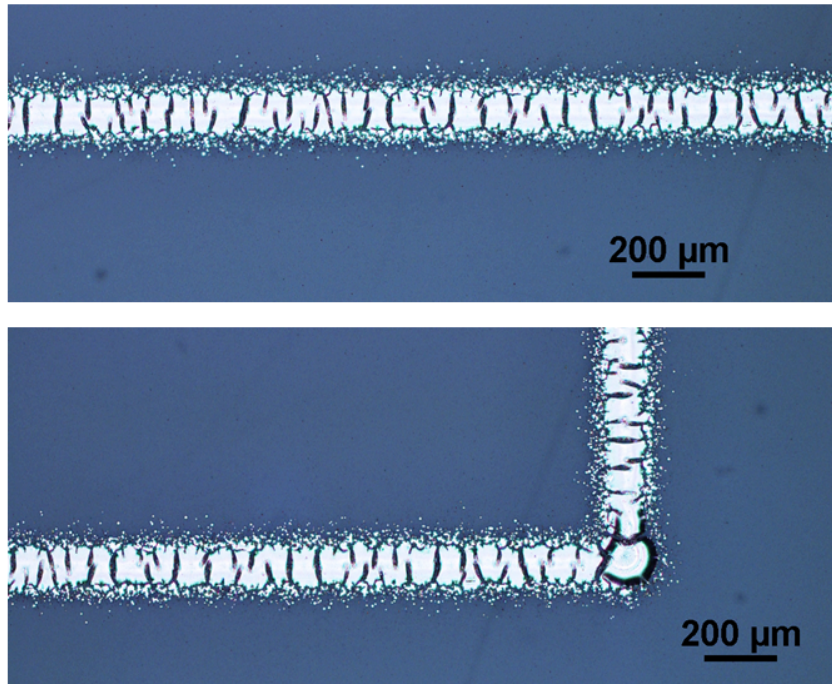


Figure 2.6: Aerosol-jet printed traces on glass substrate using Xerox nanoparticle silver ink

cracks directly after printing [32]. Significant amount of over-spray was also observed on the edges of the printed traces. Different substrates with lower surface energy such as PET foil were used in order to get rid of the resulting cracks. However, the micro-cracks and wrinkles still exist all over the printed traces as shown in Fig. 2.7 and it was not possible to completely remove the cracks even after testing different substrates and varying the process parameters. Plasma treatment was also employed to change the substrate surface energy but that didn't help as well. Therefore, the quick evaporation of the ink solvents is believed to be the main reason for the crack/wrinkles issue. So, the Xerox ink was also not ideal for our application of developing electrical interconnects to interconnect electronic and optical chips.

2.5.3. Novacentrix silver ink

Then we tested another silver nanoflakes ink from Novacentrix which is commercially known as "Metalon HPS030 AE1". It is a water-based ink and is mainly developed for AJP. The ink viscosity is about 187 cP and is compatible with the pneumatic atomizer. This ink showed promising results and much better printing quality compared to the previous

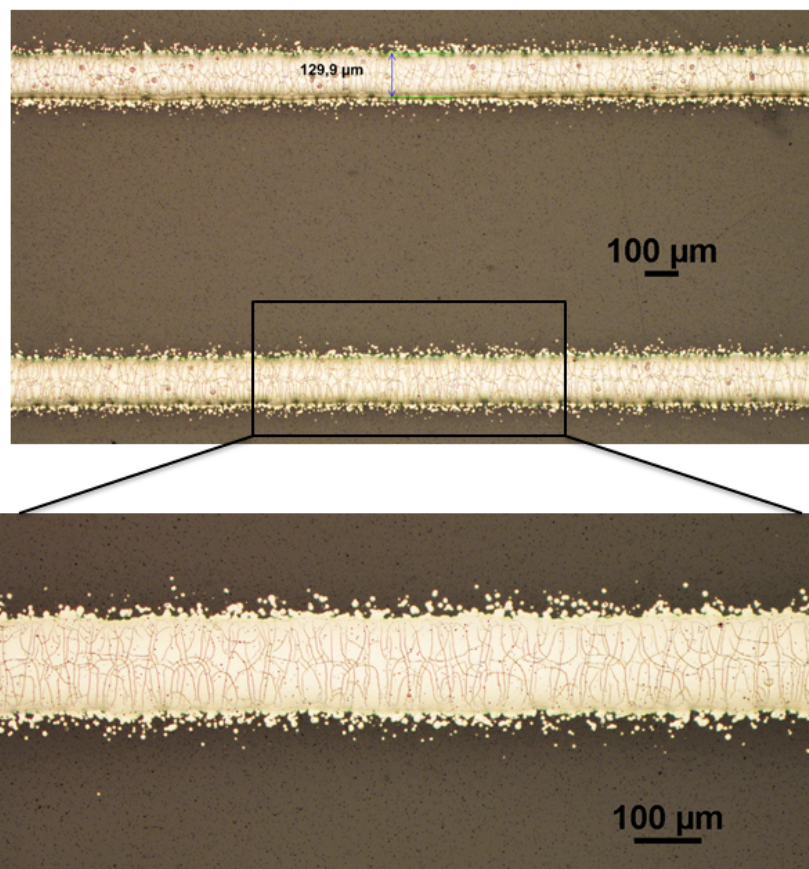


Figure 2.7: Aerosol-jet printed traces on PET foil using Xerox nanoparticle silver ink

inks. The ink also showed good adhesion and wetting properties on glass substrates. Fig. 2.8(a) shows the printed silver traces on a borosilicate glass substrate. The overspray is also very limited which allows printing traces very close to each other as illustrated in Fig. 2.8(b). The minimum line width was about $22\ \mu\text{m}$, which was achieved by increasing the sheath flow rate to 78 sccm to produce narrower traces as depicted in Fig. 2.8(c). However, increasing the sheath flow in order to reduce the line width may introduce an additional overspray induced by the high sheath flow and its effect on the very small aerosol particles. Fig. 2.8(d) shows the resulting surface profile measurements for the printed traces while fixing the stage speed at 3 mm/s. The resulting trace thickness is $3\ \mu\text{m}$ for single-pass printing. The profile of the printed traces is more uniform compared to the profile of the previous inks. Additionally, stacking multiple layers does not degrade the printing quality. Fig. 2.9 shows the printed traces for different numbers of passes. Hence, it was easy to obtain thick traces with a thickness of almost $10\ \mu\text{m}$ by printing 3 passes at a speed of 3 mm/s. Therefore, we continued using the Novacentrix ink for developing electrical conductive interconnects and all the AJP work in this thesis was done using this ink.

2.6. Aerosol-jet process optimization

The aerosol-jet process requires an optimization of multiple process parameters in order to sustain the print quality and achieve the desired structure dimensions (width, thickness, & spacing). The proper adjustment of the process parameters can ensure high printing quality and repeatable results. These parameters include pressure gas flow rates, printing speed, stage temperature, nozzle diameter and working distance. The pressure gas flow rates represent the carrier gas flow and the sheath gas flow. In case of using the pneumatic atomizer the carrier gas flow is the difference between the atomizer flow rate and the virtual impactor flow rate (exhaust flow), while for the ultrasonic atomizer there is no virtual impactor. Therefore, the carrier gas flow is the same as the atomizer flow rate. However, there is an additional process parameter for the UA which is the ultrasonic power. The ultrasonic power is responsible for creating a dense aerosol. Hence, it requires an accurate adjustment to obtain sufficient and continuous aerosol output. For each material, the process parameters need to be optimized and a process operation window needs to be defined depending on the ink properties. According to the results from section 2.5, the novacentrix inks showed the best performance among other inks and fulfilled the purpose of the final application. As a result, we optimized the process for this specific ink. Different pressure flow rates and sheath flow rates were applied to the pneumatic atomizer to investigate the printing quality for a wide range of the process parameters.

2.6.1. Influence of the focusing ratio on the line dimensions

The line geometry is determined by the ratio between the sheath and carrier gas flow rate, which is called the focusing ratio. The focusing ratio term was first introduced by Mahajan et al. [33], while printing high-aspect ratio lines using silver nanoparticle ink using the

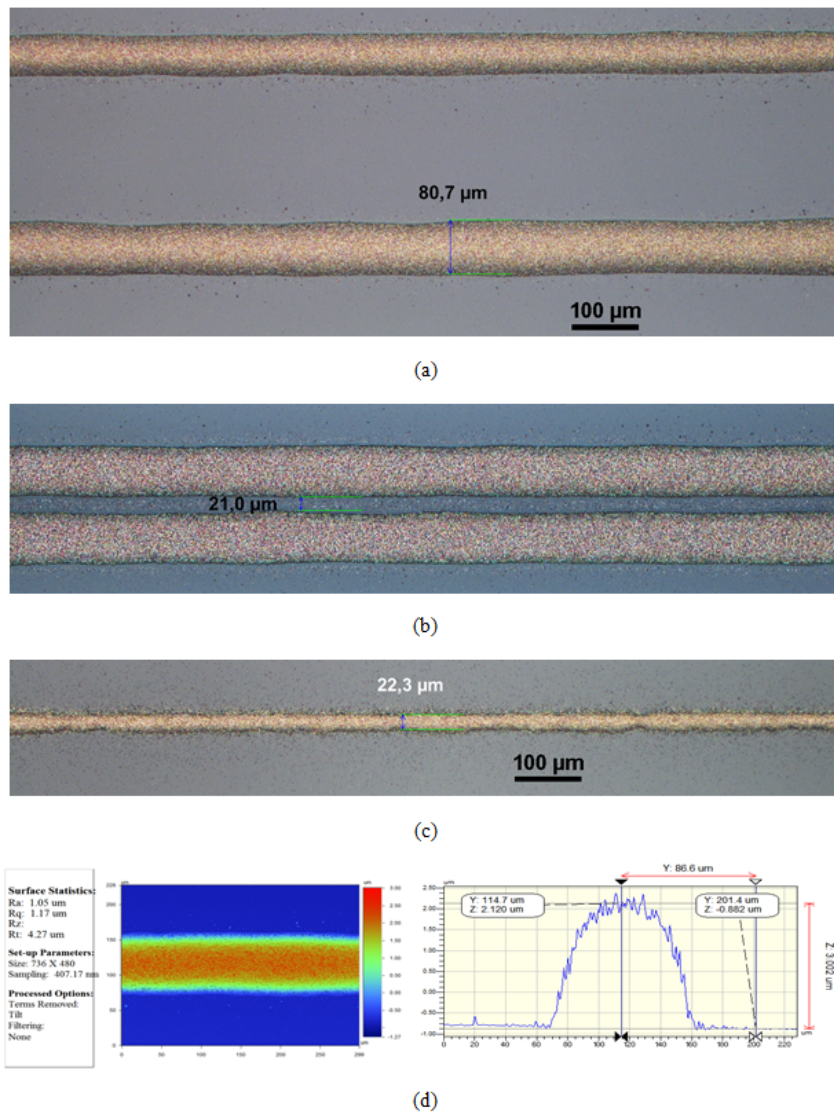


Figure 2.8: (a) Aerosol-jet printed traces on glass substrate using Novacentrix nanoflakes silver ink (b) Printing two traces with a spacing of 21 μm (c) Resulting trace after increasing sheath flow rate to 78 sccm (d) The profile measurements of the printed trace

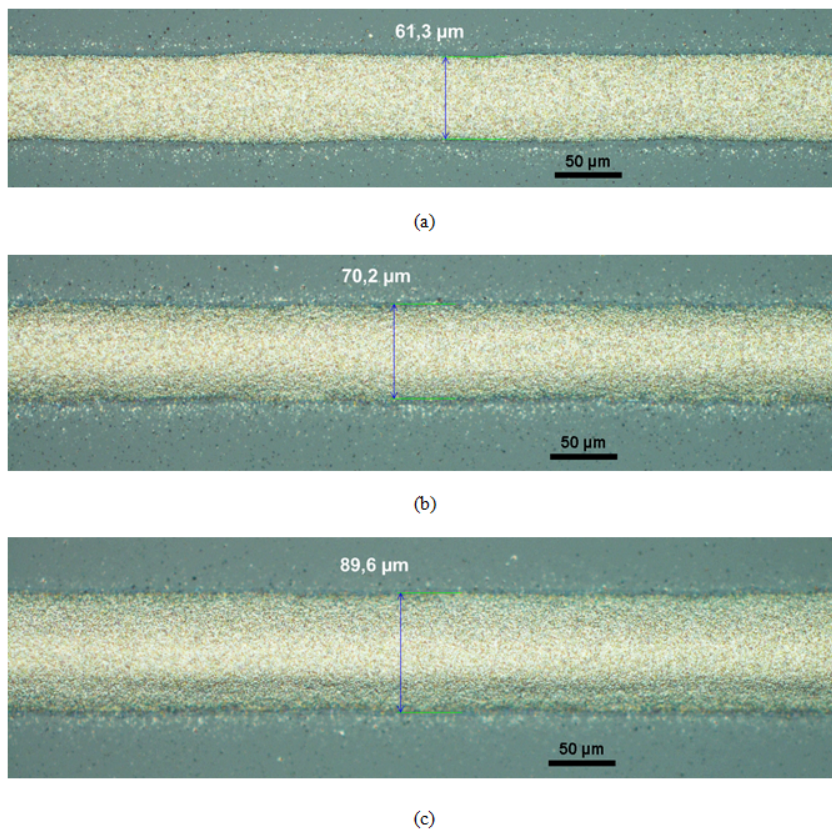


Figure 2.9: Aerosol-jet printed traces of Novacentrix ink for different printing passes (a) 1 pass (b) 2 passes (c) 3 passes

ultrasonic atomizer. The focusing ratio is given as follows:

$$Focusing\ ratio = \frac{Sheath\ gas\ flow\ rate}{Carrier\ gas\ flow\ rate} \quad (2.1)$$

In this work, we optimized the printing process for the Novacentrix nanoflakes ink (Metalon HPS030 AE1) with the pneumatic atomizer. The printing nozzle was kept at 3 mm from the substrate during the optimization process. The platen temperature was fixed at 60°C to limit the spreading of the ink after collision with the substrate and allow the solvents to partially evaporate after deposition. The stage speed was also fixed at 3 mm/s while changing the focusing ratio. The line width and thickness can also be influenced by the nozzle size. In principle, smaller nozzles enable printing finer features (i.e. 100 µm diameter). However, there is a pressure limitation for smaller nozzles due to the pressure buildup as the focusing ratio increases. This means that the smaller nozzles reach the pressure limitation at lower focusing ratios as compared to the larger nozzles. Hence, the 200 µm nozzle was used throughout the complete printing process in order to cover a wider range of the focusing ratio.

For a specific material at a certain carrier flow, the amount of the generated aerosol being transported from the atomizer to the print head remains fixed. Hence, this means a decrease in the line width corresponds to an increase in the line thickness. In general for each ink the pressure gas flows need to be optimized and hence the focusing ratio range can change from one ink to another depending on the properties of the ink. The line width increases as the focusing ratio decreases and vice-versa. Fig. 2.10 shows the effect of the focusing ratio on the line width and thickness. The focusing ratio was varied from 1.75 to 11.67. As a result, the printed line width decreased from 88 µm to 27 µm, while the thickness of the printed lines slightly increased from 1.88 µm to 2.68 µm. The sheath gas flow rate was set at 70 sccm and the carrier gas flow rate was varied from 6 sccm to 40 sccm in order to change the focusing ratio from 1.75 to 11.67. However, we can observe two different slopes in the curves in Fig. 2.10. At lower focusing ratio values (below 2.8), the slope is slightly higher which results in wider and thinner lines. This occurs because the carrier flow is relatively large with respect to the sheath flow which results in a higher aerosol output. Hence, the printed traces start to spread with a higher rate than the printed traces using a higher focusing ratio (above 2.8). It is also observed that the variations and repeatability of the printing process (especially the line width) highly depend on the focusing ratio. As the focusing ratio decreases (below 2.8), the variations in the line width can be significant ($\pm 8\ \mu\text{m}$), while if the focusing ratio exceeds 2.8 and gradually increases till 11.67, the variations also gradually decrease (below $\pm 5\ \mu\text{m}$) until it is almost negligible when the minimum feature size is reached.

2.6.2. Influence of the stage speed on the line dimensions

The line geometry can also be further controlled by the stage speed. Increasing the stage speed reduces both the line width and thickness and vice-versa. Fig. 2.11 shows the effect of the stage speed on the line width and thickness. The stage speed was varied from 1

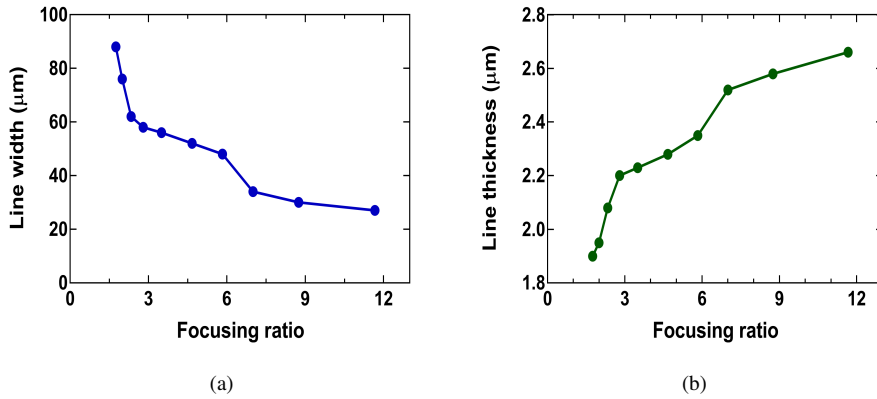


Figure 2.10: Effect of focusing ratio on line width (left) thickness (right)

mm/s to 10 mm/s while the focusing ratio was set at 2.8 (sheath flow of 70 sccm and carrier flow 25 sccm), the platen temperature was kept at 60°C and the standoff distance between the nozzle and the substrate was also fixed at 3 mm. At a stage speed from 1 mm/s to 3 mm/s, the line width decreased significantly from $142.3\ \mu\text{m}$ to $58.8\ \mu\text{m}$ respectively as the spreading was dominant in this speed range, while the thickness decreased from $4.6\ \mu\text{m}$ to $2.1\ \mu\text{m}$ respectively. At a stage speed from 4 mm/s to 10 mm/s, the line width decreased gradually from $58.3\ \mu\text{m}$ to $37.6\ \mu\text{m}$ respectively, while the thickness decreased from $1.9\ \mu\text{m}$ to $0.9\ \mu\text{m}$ respectively.

The thickness can also be increased by stacking multiple passes in order to achieve the required thickness. The width can slightly increase by applying multiple passes in particular for lower focusing ratios. Fig. 2.12 shows the relation between the number of printing passes and the corresponding line width and thickness for different focusing ratios. In this experiment, three different set of traces were printed; one set with one printing pass, the second with two passes and the third with three passes. Then, the thickness and the width were measured for the three different sets. The stage speed was fixed at 3 mm/s and focusing ratios of 2.8, 3.5 and 4.67 were used. The thickness increased linearly with the number of passes, while the width increased about 30% after applying three printing passes. Table 2.2 gives a summary for the resulting line dimensions for different sets of process parameters.

2.7. Sintering of silver inks

After printing, the inks need to be sintered and cured in order to make the printed traces conductive and evaporate the solvents. The sintering process also enables welding the metal nanoparticles together by removing all the solvents existing in the ink. Different sintering

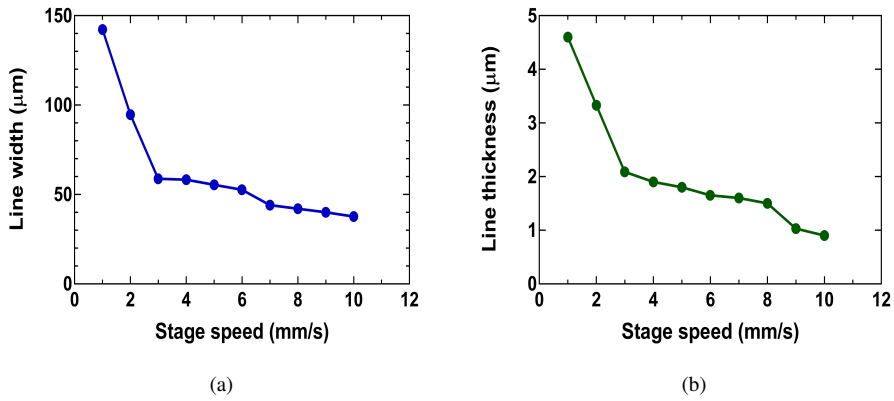


Figure 2.11: Effect of stage speed on line width (left) thickness (right)

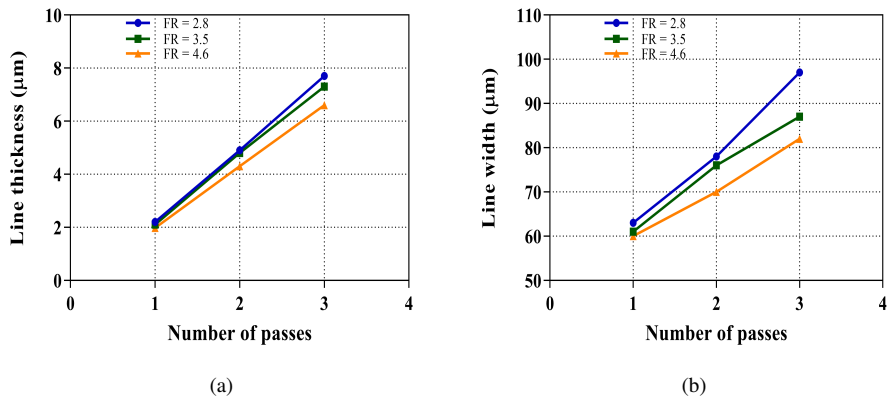


Figure 2.12: influence of stacking multiple passes on (a) trace thickness (b) trace width

Table 2.2: A summary of the resulting line dimensions for different set of process parameters

	Stage speed (mm/s)	Sheath gas flow (sccm)	Carrier gas flow (sccm)	Focusing ratio	number of passes (μm)	Resulting width (μm)	Resulting thickness
Line1	1	70	25	2.8	1	142	4.6
Line2	3	70	25	2.8	1	59	2.1
Line3	5	70	25	2.8	1	55	1.8
Line4	7	70	25	2.8	1	44	1.5
Line5	10	70	25	1.8	1	37	0.9
Line6	3	70	6	11.67	1	27	2.65
Line7	3	70	10	7	1	34	2.55
Line8	3	70	15	4.67	1	52	2.28
Line9	3	70	20	3.5	1	56	2.23
Line10	3	70	25	2.8	1	58	2.2
Line11	3	70	30	2.33	1	62	2.08
Line12	3	70	35	2	1	76	1.95
Line13	3	70	40	1.75	1	88	1.88
Line14	3	65	25	2.6	1	68	2.1
Line15	3	75	25	3	1	50	2.4
Line16	3	70	15	4.67	2	70	4.3
Line17	3	70	15	4.67	3	89	6.6
Line18	3	70	20	3.5	2	76	4.8
Line19	3	70	20	3.5	3	86	7.3
Line20	3	70	25	2.8	2	78	4.9
Line21	3	70	25	2.8	3	97	7.7

techniques (i.e. thermal, plasma, laser and photonic sintering) have been investigated for sintering nanoparticle inks deposited by inkjet printing [34]. Those sintering methods were investigated and evaluated based on different aspects such as the conductivity, adhesion, roll-to-roll compatibility, and temperature requirements. For example, oven sintering can achieve high conductivity and good adhesion properties, but it is not suitable for roll-to-roll fabrication and can not be used with flexible substrates (i.e. temperature sensitive substrates). On the other hand, laser and photonic sintering are recommended for temperature sensitive substrates. Laser and intense pulsed light (photonic) sintering have shown promising results for sintering a copper nanoparticle ink printed on polyimide substrates by achieving a conductivity of 20% of the bulk conductivity of the copper [35]. Moreover, intense pulsed light sintering in particular is compatible with roll-to-roll fabrication. In this work, we used oven sintering for curing the silver tracks as the printing process was performed on rigid substrates such as glass and PCB substrates. Additionally, the conductivity was required to be as high as possible so we sintered the printed traces thermally in the convection oven at 210°C . The resulting conductivity was found to be relatively higher than the laser-sintered traces. Fig. 2.13 shows the sheet resistance for laser sintered and thermally-sintered traces. The laser sintering process was performed using a picosecond laser at a wavelength of 1064 nm. The laser power was set at 700 mW and a frequency of 1 MHz with a pulse overlap of about 50% was utilized to sinter the silver tracks on the glass substrate. An ablation effect started to appear on the silver tracks if the power was set higher than 700 mW. So, the power was fixed at 700 mW as a threshold value. The oven-sintered interconnects showed a sheet resistance of $0.025\ \Omega$ per square, which is almost 10 times lower than the laser-sintered interconnects. Fig. 2.14 shows the sheet resistance for the printed traces after an oven sintering time of 1 and 3 hours at 210°C . The degree of sintering and conductivity of the printed traces are mainly influenced by the sintering temperature rather than the sintering time [36]. The higher the temperature, the shorter the time to reach the highest conductivity. That explains that the difference between the resulting sheet resistance of the printed traces for a sintering time of 1 and 3 hours is not significant. The Novacentrix ink (Metalon HPS030 AE1) is water-based nanoflakes ink and the welding process of the nanoflakes was inspected using scanning electron microscope before and after thermal sintering as illustrated in Fig. 2.15. The resistivity of the aerosol-jet printed tracks can be further reduced by adding carbon nanotubes (CNTs) with a certain weight to the silver nanoparticle ink [37]. The conductivity of the printed tracks is improved by 38% while adding 0.15wt% CNTs to the silver ink and no further improvement in the conductivity was observed while increasing the CNTs concentration. The authors believe that the reason behind the conductivity improvement is that the CNTs act as a bridge to connect the defects and the voids in the sintered silver tracks.

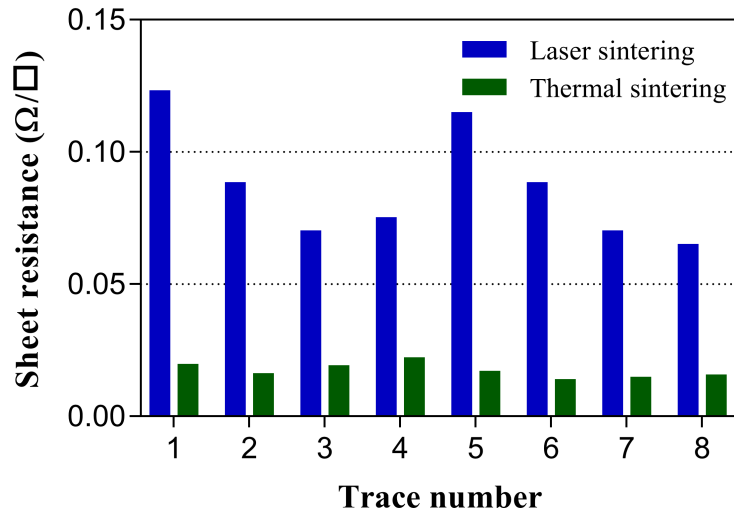


Figure 2.13: Resulting sheet resistance of the printed traces for laser and thermal sintering

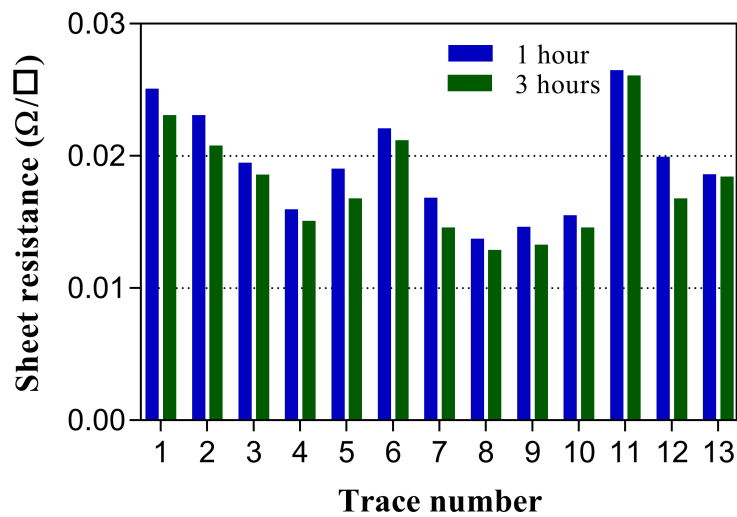
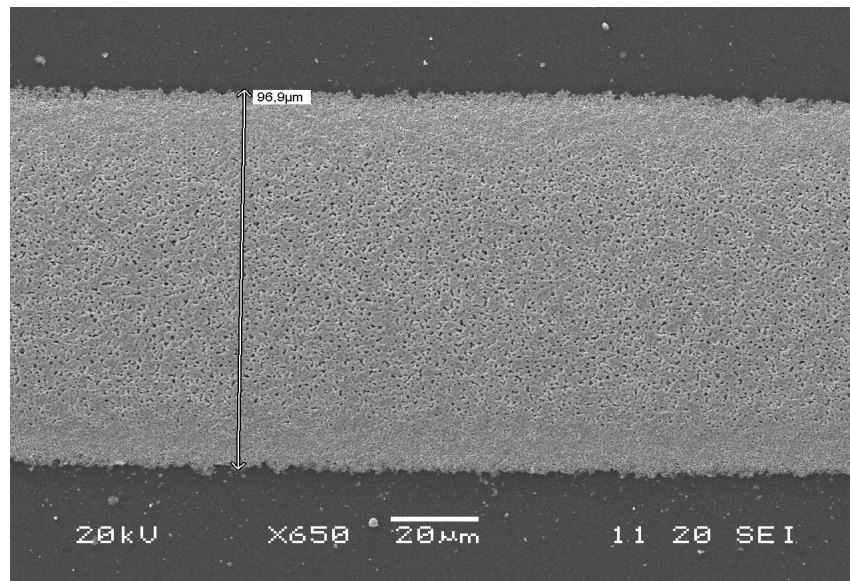
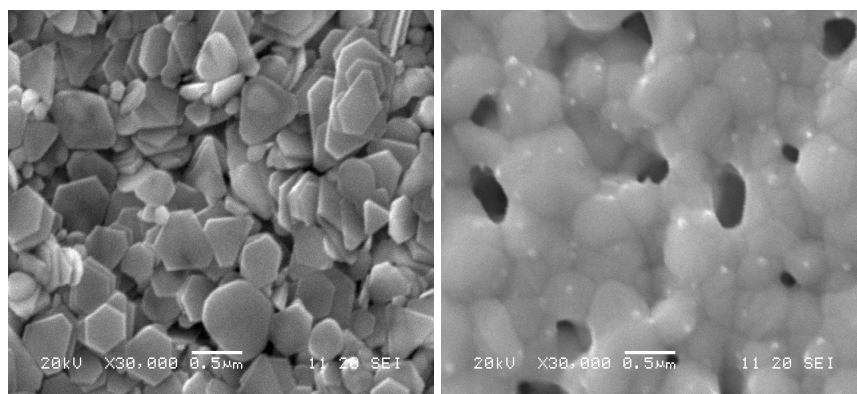


Figure 2.14: Resulting sheet resistance after Thermal sintering for 1 and 3 hours



(a)



(b)

(c)

Figure 2.15: SEM micrographs for the Novacentrix traces (a) before sintering (b) after sintering

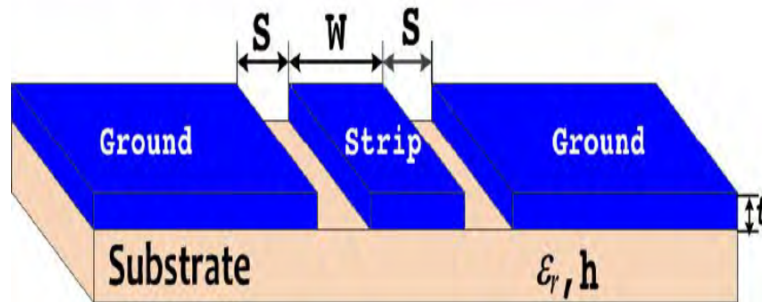


Figure 2.16: Coplanar waveguide cross section

2.8. Realization of coplanar waveguide transmission lines

We used AJP to print coplanar waveguide (CPW) transmission lines in order to investigate the electro-magnetic behavior of the aerosol-jet printed interconnects. The ground-signal-ground coplanar waveguide (GSG CPW) is one of the most commonly used and simplified transmission line structures in planar microwave circuit design. A CPW consists of a center conductor strip separated by a narrow gap from two ground planes on each side as illustrated in Fig. 2.16. The dimensions of the center conductor, the gap between the signal and ground planes, the thickness and permittivity of the substrate determine the effective dielectric constant, the characteristic impedance and the attenuation of the transmission line. The limitations of the AJP process were also considered in the realization of CPW structures as the most critical parameter to achieve is the gap between the signal and ground conductors. The minimum gap that can be achieved with the Novacentrix ink is about $25\ \mu\text{m}$. Hence, the gap was set at $35\ \mu\text{m}$ in the CPW design to ensure that it can be practically realized without causing a short or overlap between the signal and ground conductors.

2.8.1. Simulation of coplanar waveguide structures

The CPW dimensions were tuned using the Linecalc tool in the Advanced design system (ADS) software from Keysight technologies to match a characteristic impedance as close to $50\ \Omega$ as possible. The scattering parameters (S-parameters) including the transmission and reflection coefficients were obtained for the simulated CPWs over a frequency range up to 55 GHz. CPWs with different lengths (1, 2, 4, and 8 mm) were simulated. In this simulation the substrate is considered to be borosilicate glass and the corresponding permittivity was assigned in the simulation. The parameters of the simulated CPWs are given in table 2.3. Additionally, the CPWs were also simulated while an epoxy layer with a thickness of $200\ \mu\text{m}$ is applied on the borosilicate glass substrate. The influence of the

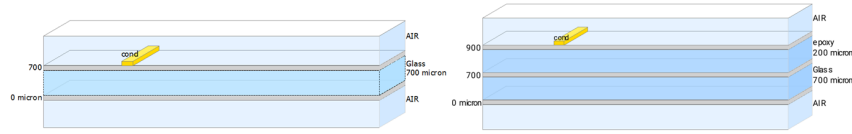


Figure 2.17: Coplanar waveguide models in ADS

Table 2.3: Simulated CPW parameters

Signal conductor width	90 μm
Gap between signal and ground conductors	35 μm
Conductor thickness	5 μm
Glass permittivity	4.8
Epoxy permittivity	3.5
Glass substrate thickness	700 μm
Glass tangent loss	0.02
Epoxy tangent loss	0.06

substrate dielectric properties for the two different substrates is investigated in terms of the attenuation (per millimeter) and the characteristic impedance of the coplanar waveguides. Fig. 2.18 shows the S-parameter simulation results for the coplanar waveguides on glass and epoxy substrates. The simulations show that the CPWs on glass substrate have an attenuation of 0.43 dB/mm at 50 GHz, while the CPWs on epoxy exhibit an attenuation of 0.63 dB/mm at 50 GHz. The CPWs on glass show lower loss per mm than the CPWs on epoxy as expected because the loss per millimeter depends on the dielectric tangent loss (tanD) of the substrate. The tangent loss for the epoxy material is higher than that for the glass material [38]. The values of the loss tangents for glass and epoxy materials are estimated to be 0.02 and 0.06 at 50 GHz respectively. That explains the slightly higher loss for the CPWs on the epoxy substrate. Additionally, the CPWs on the glass substrate exhibit a slightly lower reflection S_{11} than the CPWs on epoxy as illustrated in Fig. 2.18c and Fig. 2.18d

2.8.2. Aerosol-jet printing of coplanar waveguides

Based on the simulation results, CPWs autocad designs with the same dimensions were developed and loaded to the motion manager of the AJP system. Coplanar waveguide transmission lines with different lengths (1, 2, 4, 8 mm) were printed on a borosilicate glass, and on an epoxy layer with a thickness of 200 μm residing on a borosilicate glass. The used epoxy material is commercially known as Epotek OG142-112. Fig. 2.19 shows the AJP printed GSG CPWs with different lengths on a glass substrates. The CPWs were printed using the following process parameters; sheath flow = 70 sccm, atomizer flow = 1100 sccm, exhaust flow = 1075 sccm, stage speed = 3 mm/sec, print passes = 2, stand-off distance =

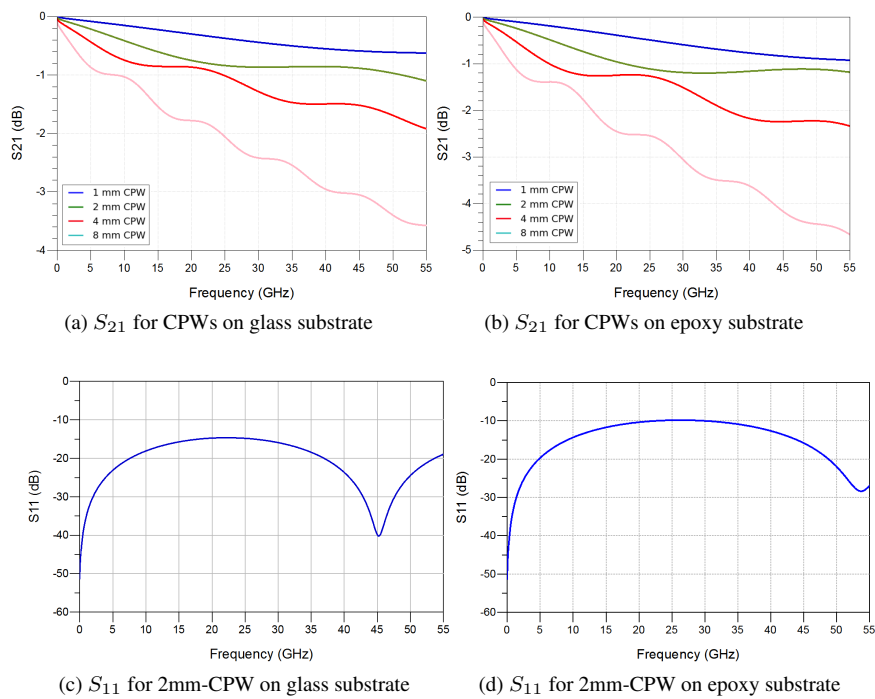


Figure 2.18: Transmission coefficient S_{21} and reflection coefficient S_{11} of the simulated CPWs

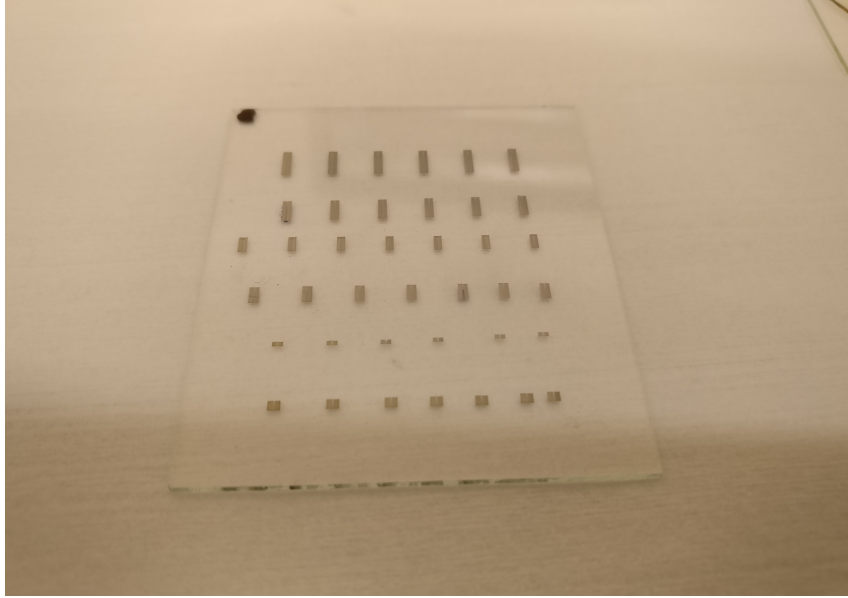


Figure 2.19: Aerosol-jet printed GSG CPW with different lengths on a glass substrate

3 mm, stage temperature = $60\text{ }^{\circ}\text{C}$. The dimensions of the printed CPW are summarized in table 2.4. The AJP CPWs have a width of $93\text{ }\mu\text{m}$, a gap of $36\text{ }\mu\text{m}$ between the ground and signal planes, and a thickness of $5.8\text{ }\mu\text{m}$ as illustrated in Fig. 2.20. Additionally, the surface roughness of the printed CPW structures is measured as illustrated in Fig. 2.20(b). The RMS roughness (R_{rms}) of the signal and ground planes is found to be about 390 nm and 310 nm respectively. The skin depth of the silver ink is calculated and found to be about 450 nm at 50 GHz [27, 39]. Moreover, 3D and 2D views of the CPW profile are illustrated in Fig. 2.20(c) and (d) respectively. Three samples of the printed CPWs and calibration standards with the same specifications were prepared to ensure the consistency of the measurements. The goal is to measure the loss per mm for the printed CPWs on glass and epoxy and extract the relative permittivity (ϵ_r) for both epoxy and glass substrates.

2.8.3. TRL calibration

The CPWs were then characterized by measuring the S-parameters including the transmission and reflection coefficients using a vector network analyzer (VNA). The characterization setup is shown in Fig. 2.21. In order to perform accurate measurements for the device under test (DUT), a calibration procedure needs to be performed to omit all the errors and non idealities introduced by the probes, cables, connectors and the VNA itself. The effect of these errors can be very significant with respect to the DUT. The calibration process helps to subtract those errors and obtain accurate results for the DUT. There are several

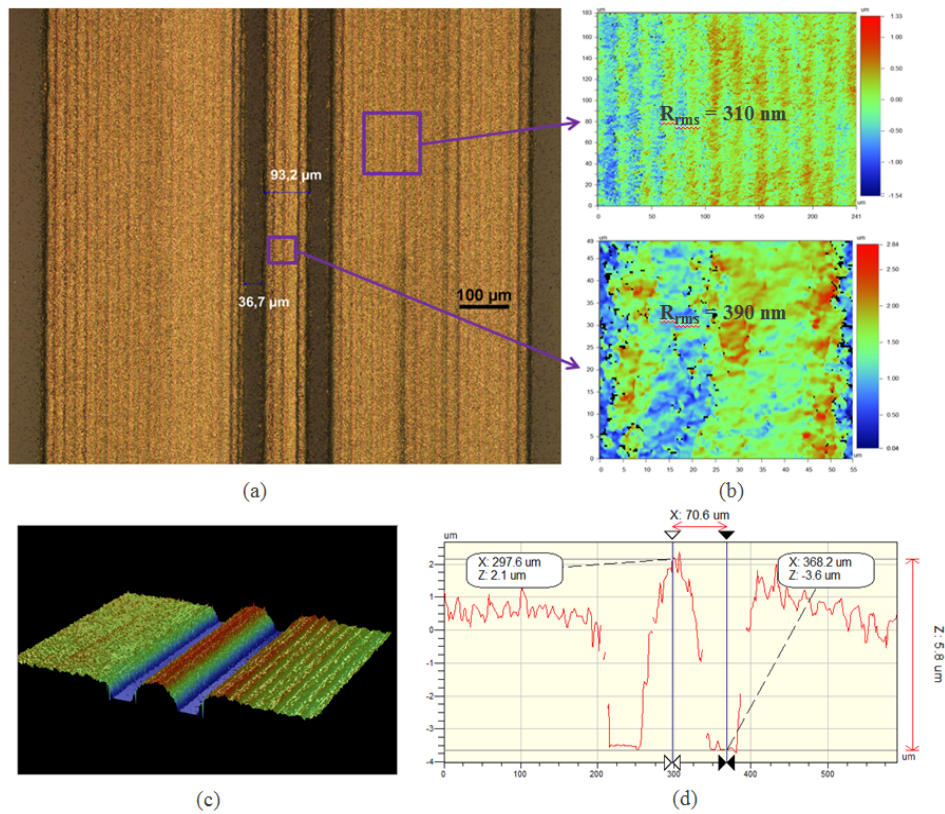
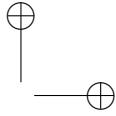
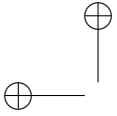


Figure 2.20: Aerosol-jet printed GSG coplanar waveguide(CPW)

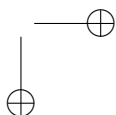
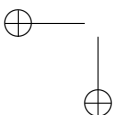
Table 2.4: Printed coplanar waveguide parameters

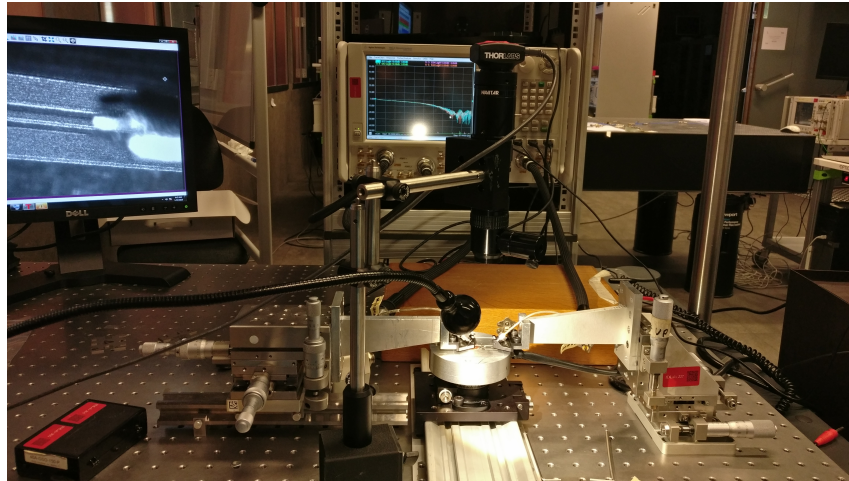
Signal conductor width	93 μm
Gap between signal and conductor planes	36 μm
Ground width	400 μm
Conductor thickness	5.8 μm
Substrate thickness	700 μm
Signal conductor RMS roughness	390 nm
Ground plane RMS roughness	310 nm



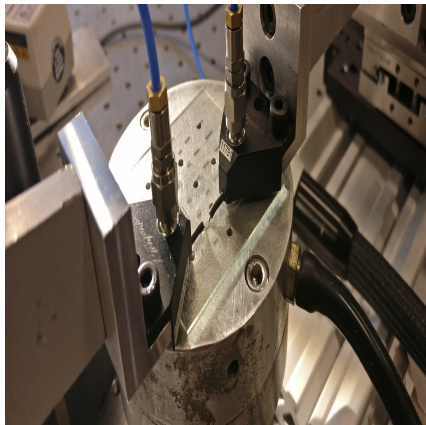
calibration techniques that can be used to de-embed the probes such as SOLT (short, open, load, thru) [40], TRL (Thru, reflect, line), LRL (line, reflect, line) [41, 42] and LRM (line, reflect, match) [43]. TRL calibration is considered as the most widely used and accurate method in microwave measurements [41, 44, 45]. TRL calibration requires including short, thru, reflect structures which are equal at both sides and a number of lines with different lengths in order to cover a broad frequency range as each line length covers a certain frequency band. The electrical length of the frequency range must be properly chosen so that the phase difference between the Thru and line at each frequency should be greater than 20° and less than 160° . A representation of the TRL calibration standards is shown in Fig. 2.22. The TRL calibration standards are required to be fabricated on the same substrate as the DUT. Therefore, Thru structures with a length of $400\ \mu\text{m}$, reflect structures and different line lengths (1, 2, 4, and 8 mm) are fabricated on the same substrate. The scattering parameters of the DUT were normalized with respect to the unknown characteristic impedance of the lines. The TRL calibration can either be carried out directly on the VNA or can be done offline using the python scikit-rf package [46]. The TRL calibration on the VNA requires defining a set of parameters for each line standard in order to perform the calibration process correctly. These parameters include the frequency range, characteristic impedance of the line standard, estimated delay and number of line standards. On the other hand, the TRL calibration using scikit-rf is implemented in python. It is open source software and all the source code is available online. It is more flexible approach to allow to modify the frequency range and avoid defining the required parameters per line standard for each frequency range as the software is responsible to handle this job. In this case, the frequency banding per line is not required and the scikit-rf package can easily manage the frequency range per line standard to improve the measurement accuracy.

In this work, we first used the TRL calibration on the VNA but that required to precisely define the exact values of the previously mentioned parameters in order to perform the calibration correctly. Otherwise, discontinuity effects appeared in the resulting measurements due to the inaccurate frequency banding per line standard. For example, Fig. 2.23 shows the resulting S_{11} measurements after offline TRL and VNA calibration. For the VNA TRL calibration, there is a discontinuity in S_{11} at 11.5 GHz due to the inaccurate frequency banding of two line standards during calibration. Therefore, the frequency banding needs to be defined accurately to avoid any discontinuity issues for the TRL calibrated results. In order to avoid the complexity of the frequency banding for multiple lines calibration, we tested the offline TRL calibration for the same samples. The transmission coefficient (S_{21}) results after offline TRL calibration are in agreement with the results from the VNA TRL calibration. Fig. 2.24 shows the measured transmission coefficient (S_{21}) for the AJP 8 mm-CPW on the glass substrate after VNA and offline TRL calibration. Therefore, we utilized the offline TRL calibration for the rest of the measurements in order to provide a simple, flexible, and faster characterization process compared to the VNA direct calibration.

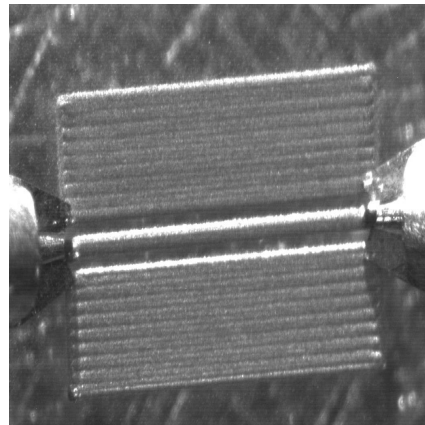




(a)



(b)



(c)

Figure 2.21: (a) Vector network analyzer (VNA) setup (b) Sample on vacuum chuck (c) 1mm-CPW probed by RF GSG probe

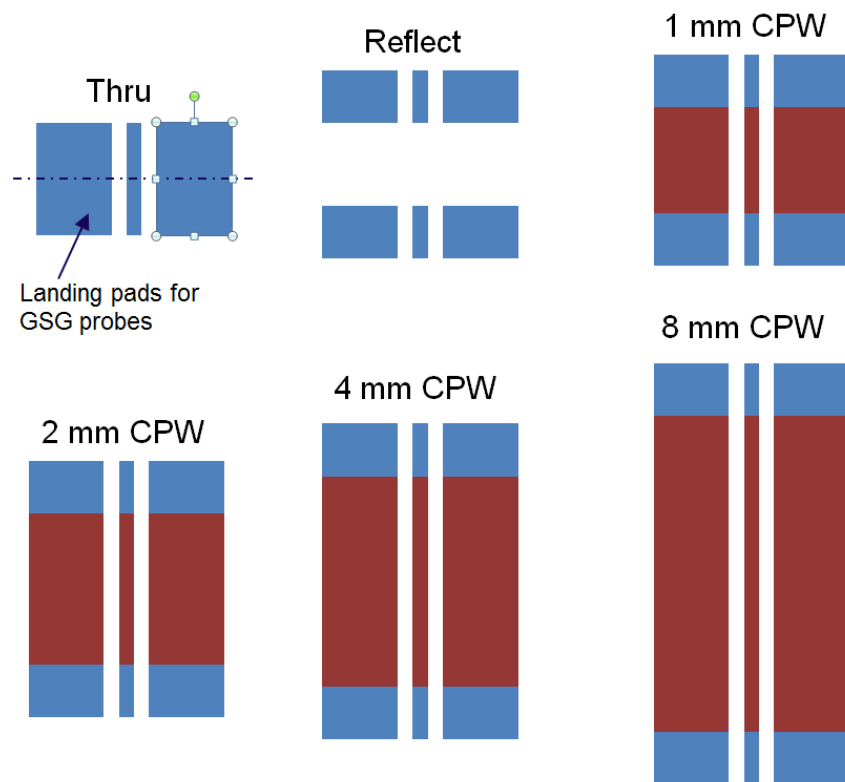
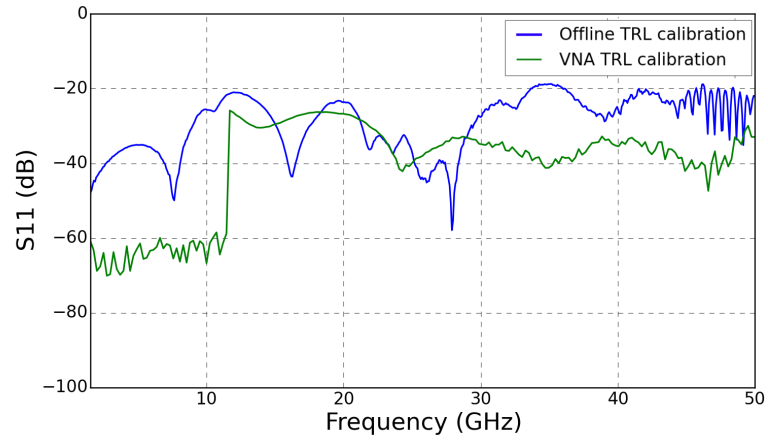
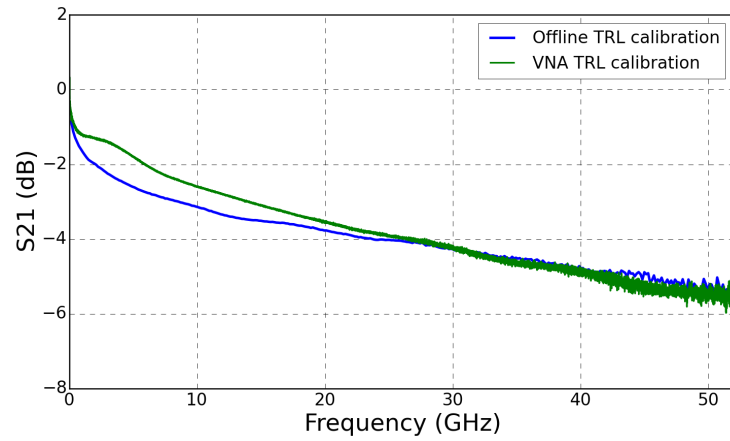
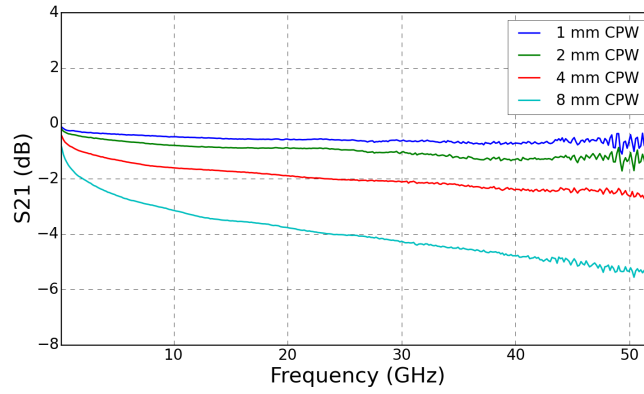


Figure 2.22: TRL calibration standards

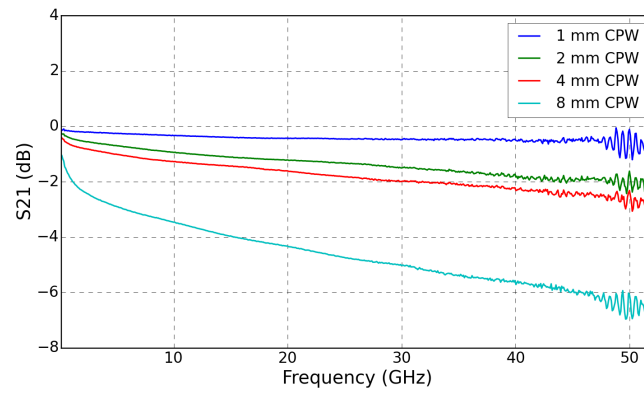
Figure 2.23: S_{11} measurements using TRL offline and VNA calibrationFigure 2.24: Measured S_{21} after TRL offline and VNA calibration

2.8.4. Characterization results

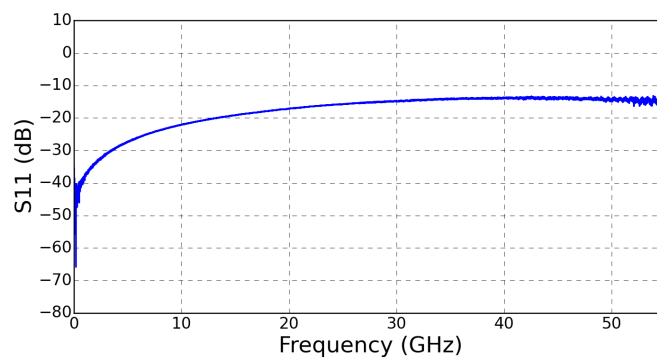
The characterization measurements were performed as follows; the frequency range was chosen and the cables were calibrated out using the Ecal SOLT on the VNA. The scattering parameters for all the TRL line standards (thru, reflect, different lines) were then measured for the same frequency range. The resulting .s2p files were processed by the scikit-rf package in python to perform the TRL offline calibration. Fig. 2.25 shows the measurements of the transmission coefficient (S_{21}) for the printed CPW on glass and epoxy after TRL calibration with respect to the line standard. The printed CPWs on glass and epoxy show low attenuation of about 0.57 dB/mm and 0.76 dB/mm at 50 GHz respectively. Similar CPW transmission lines fabricated using conventional lithography showed an attenuation around 0.3 dB/mm at 50 GHz [47]. The lower attenuation is mainly attributed to the higher conductivity of the sputtered or evaporated conductors with standard lithography. Therefore, a lot of research nowadays is invested to explore developing inks with higher conductivity. This will significantly improve the conductivity of the AJP interconnects. However, the losses of the aerosol-jet printed CPWs developed in this work are still acceptable for our application, which is targeting short transmission lines (few millimeters) and very short high-speed interconnects (100-300 μm). Based on S-parameters measurements, the relative permittivity for glass and epoxy materials was also extracted as a part of the scikit-rf calibration package as shown in Fig. 2.26. The values of the relative permittivity (ϵ_r) for glass and epoxy materials are found to be 4.8 and 3.5 at 50 GHz respectively. The resulting S-parameter measurements after TRL calibration are in agreement with the simulation results introduced in section 2.8.1.



(a)



(b)



(c)

Figure 2.25: (a) measured S_{21} for the printed CPWs on glass (b) measured S_{21} for the printed CPWs on epoxy (c) measured S_{11} for the printed 1 mm CPW on glass

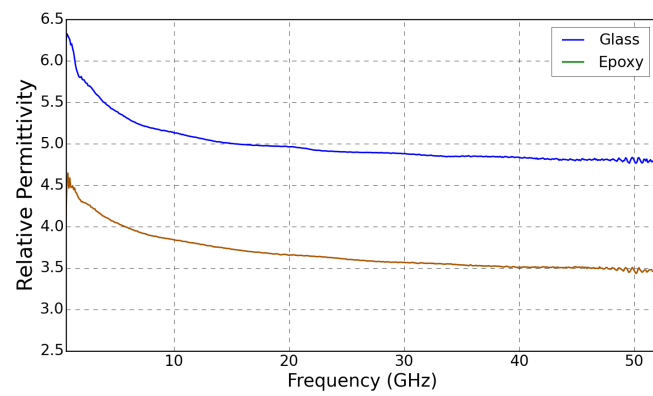


Figure 2.26: Extracted relative permittivity (ϵ_r) for glass and epoxy substrates

2.9. Conclusions

In this chapter, we presented the AJP technology to develop conductive electrical interconnects. The AJP technology offers promising features over the current additive manufacturing technologies. The AJP technology enables printing a broad range of materials including metallic inks and dielectric materials. With the help of the two atomizer systems (pneumatic and ultrasonic), different ink viscosities up to 1000 cP can be printed. Three silver nanoparticle inks have been explored by the AJP system. The novacentrix ink showed the best results in terms of the printing quality, desired geometry, substrate and the conductivity. The process optimization for this ink was investigated in detail. The line dimensions are determined by the focusing ratio, which is the ratio between the sheath flow rate and the carrier flow rate. The higher the focusing ratio, the narrower the lines and the higher the thickness and vice versa. The stage speed or the printing speed can also control the line dimensions. The higher the printing speed, the smaller the width and thickness of the printed traces. Moreover, multiple layers can be stacked in order to obtain a certain line thickness. In this case, the width may slightly increase as well.

After printing the silver interconnects, the samples were sintered in the convection oven at 210°C for 1 hour in order to evaporate the solvents and weld the silver nanoflakes together. Laser sintering was also explored for the printed interconnects. However, the oven-sintered traces showed much lower sheet resistance of $0.025\ \Omega$ per square than the laser-sintered traces. We also investigated the sintering time for the printed traces and it was found that the degree of sintering and conductivity of the printed traces were mainly influenced by the sintering temperature rather than the sintering time.

CPW transmission lines were finally realized in order to investigate the electro-magnetic behavior of the printed interconnects. CPWs with different lengths were first simulated in the ADS software from Keysight technologies. Based on the simulations, CPWs structures were aerosol-jet printed on glass and epoxy substrates. The transmission lines were characterized by measuring the scattering parameters including the transmission and reflection coefficients using VNA. In order to de-embed the probes and subtract the errors induced by the VNA and cables, offline TRL calibration using the python scikit-rf package was performed to obtain precise results for the transmission lines. The printed CPWs on glass and epoxy showed an attenuation of about $0.57\ \text{dB/mm}$ and $0.76\ \text{dB/mm}$ at 50 GHz respectively. The CPWs have a calculated characteristic impedance of $61\ \Omega$. This can be further improved towards $50\ \Omega$ for better matching by tuning the CPW dimensions. Furthermore, the values of the relative permittivity (ϵ_r) for glass and epoxy materials were extracted and valued as 4.8 and 3.5 at 50 GHz respectively.

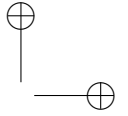
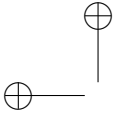
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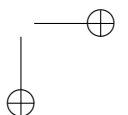
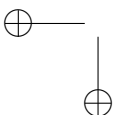
3

Electronic-photonic Integration using aerosol-jet printing

In the previous chapter, we focused on the aerosol-jet printing of electrical interconnects and transmission lines. In this chapter, we will use those printed high-speed interconnects to interconnect electronic and photonic ICs in order to develop optical transmitters for datacenter applications. The fabrication process flow for the AJP based electronic-photonic integration will be described in detail. Then, the functionality of the process technology is tested on daisy-chain test chips. In addition, a $85^{\circ}C/85\% RH$ test is performed in order to investigate the reliability of the realized printed interconnects. Next, a comparison between the aerosol-jet printed interconnects and the traditional bonding wires will be provided. Finally, different high-speed optical transmitter assemblies will be demonstrated.

3.1. Introduction

The increasing demand for high-performance optoelectronic devices largely rises from the need for the high-data rates across communication and transceiver systems. Packaging of photonic integrated circuits (PICs) is one of the most critical obstacles that still need to be addressed in order to enable true mass-market production for photonic systems. The performance and the overall cost of the electro-optical devices highly depend on how efficiently the electronic and photonic ICs are co-packaged. Hybrid integration of photonic and electronic functionalities on two separate chips is still the most economical approach to meet these demands. High-speed optical transceiver systems require low-parasitic



packaging technologies to sustain the massive increase in data rates for optical links. Wire bonding technologies are still the most widely used techniques for electronic and photonic assembly because of their flexibility and reliability. However, the wire bonding technology has some drawbacks which need to be considered such as the parasitic inductance of the wires and the difficulty to control the wire loop shape and dimensions. Shifting from round wire interconnects to ribbon wires can provide more consistent loop profiles, due to the ribbon wire's rectangular shape. In addition, the impedance and inductance at high frequencies is lower for ribbon wire, because of the large cross-sectional area and the large surface area, thus reducing the impact of the skin effect. Despite those advantages, ribbon bonding for RF applications is very critical, and less flexible since wires can only be realized in one orientation.

To meet these requirements, several reports were presented to enable hybrid integration of electronic and photonic chips for high-speed optical transceiver systems in which the wire bonding technology is replaced by a 3D stacking method [1, 2] via mounting the optoelectronic chips (vertical cavity surface emitting laser (VCSEL) or photodiode (PD) arrays) over the electronic chips (driver or transimpedance amplifier (TIA)). Flip-chip technology is proven to be a good alternative particularly at high frequencies as it replaces the long wire (100-500 μm) with very short vertical microbump interconnects (10 μm), which minimize the effect of the parasitic inductances. A flip-chip interconnection [3] was developed for an electro-absorption modulator integrated with a distributed feedback (EAM-DFB) laser array transmitter. A 12-channel optical transmitter and receiver sub-assembly was recently demonstrated at 10 Gb/s based on a wet etched silicon interposer for 3D embedding and connecting of optoelectronic dies and CMOS ICs [4]. However, those approaches are still less flexible compared to the wire-bonding technology. Therefore, new integration and automated packaging techniques which not only sustain higher operating frequencies, but also maintain the flexibility (in assembly) and reliability, are essential. In this context, we present a flexible packaging method to interconnect electronic and photonic dies based on aerosol-jet printing. AJP technology enables printing very short electrical interconnects between PIC and EIC (100-300 μm) with a pitch of 50 μm , thus minimizing the parasitic inductance for high-speed applications. It also offers high flexibility in tuning the characteristic impedance of the printed transmission lines (TLs) by controlling their dimensions and spacing in order to design impedance-mated TLs, thus reducing signal reflections and attenuation.

3.2. Fabrication process flow

The fabrication process flow for electronic and photonic integration is shown in Fig. 3.1. In order to interconnect the photonic and electronic chips by AJP, a mechanical polymer support was created to bridge the gap between the chips and subsequently the electrical interconnects were printed on top of this polymer support. The process flow can be described as follows. First, the chips were die-bonded to the PCB followed by an epoxy polymer dispensing (Epotek OG 142-112). The epoxy was locally dispensed on the chips

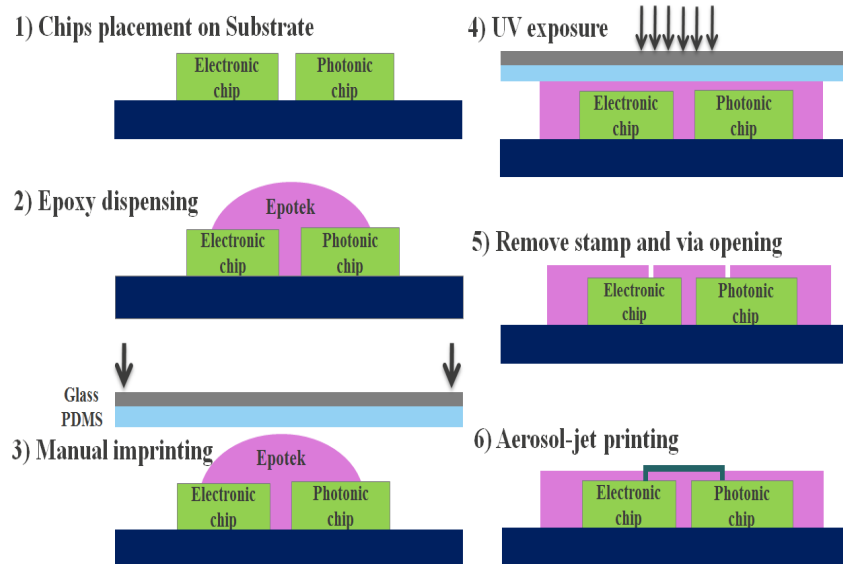


Figure 3.1: Fabrication process flow

by a fine needle. Next, a flat PDMS (Polydimethylsiloxane) stamp (50 μm PDMS layer residing on a borosilicate glass substrate) was gently pressed onto the dispensed epoxy. Then, the epoxy was cured using a UV lamp at $30 \text{ mW}/\text{cm}^2$ for 2 minutes. The stamp can be easily removed after UV exposure since the epoxy does not adhere to PDMS. Since, the polymer shrinks after UV exposure, the polymer imprinting step could be repeated a few times until uniform and sufficient coverage for the chips could be achieved. The thickness of the epoxy layer on top of the chips should be less than 10 μm , by applying a sufficient manual pressure during UV exposure. Next, vias were opened on the contact pads by excimer laser ablation. At last the electrical interconnects were precisely printed between the chips (pad-to-pad) using AJP. In order to ensure that the vias were completely filled, at least two printing passes (5 μm per pass) were applied to connect between the chips. The epoxy covering the electronic and photonic chips is transparent so that it would have no negative effect on the light coupling efficiency in or out of the photonic chips. The material properties of Epotek OG 142-112 are summarized in table 3.1. It is specifically developed as sealing and encapsulating adhesive for fiber optic and opto-electronic packaging solutions.

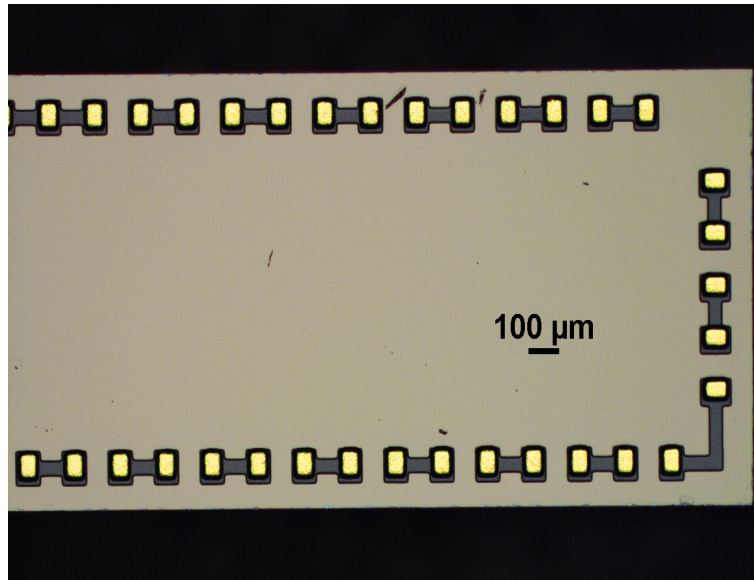
Table 3.1: Physical and optical characteristics of Epotek OG142-112

Parameter	Epotek OG142-112
Viscosity [cP]	1450 ± 250
Spectral transmission	$> 97\%$, 500-1660 nm
Weight loss [%]	0.27 % @ 200 °C
CTE (below T_g)	55 ppm/K
Refractive index	1.556 @ 589 nm
Glass transition temperature (T_g)	$> 90^\circ\text{C}$
Recommended cure	2 minutes @ 240-365 nm

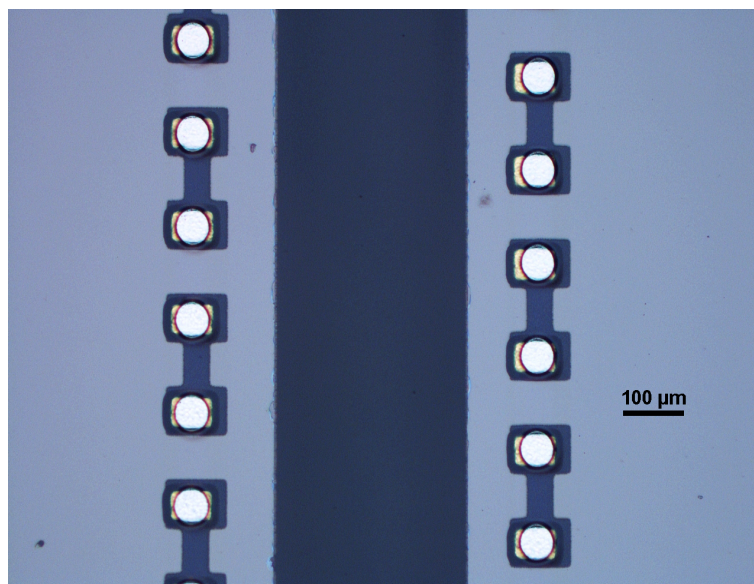
3.3. Interconnection between daisy-chain test chips

3.3.1. Interconnection description

In order to prove the concept and the functionality of the technology, we started the testing process using daisy-chain chips. The daisy chain chips have a thickness of 500 μm and they were Ni-Au plated. The goal is to interconnect two daisy-chain chips mounted face-up on a PCB by performing the process flow steps as discussed previously. Fig. 3.2 shows the daisy-chain chips used for testing the interconnection mechanism based on AJP. After creating the mechanical epoxy support, vias were opened for the two test chips by using excimer laser ablation through a circular mask with a diameter of 70 μm as shown in Fig. 3.2. The interconnection between the two daisy-chain chips was successfully realized by printing silver traces until the chain was closed and completed between the 300 μm -spaced test chips. The interconnects were printed at a stage speed of 3 mm/s. The sheath and carrier pressure gas flows were set at 70 sccm and 25 sccm respectively, which results in a focusing ratio of 2.8. The stand-off distance between the nozzle and the chips was fixed at 3 mm and the stage temperature was set at 60 °C. Fig. 3.3 shows pictures of the top and cross-section views for the AJP pad-to-pad interconnects between the test chips. The resulting printed interconnects have a width of about 50 μm and a thickness of 3 μm per pass. For a spacing of 300 μm between the test chips, the interconnect length (pad-to-pad) was about 550 μm and the resulting thickness was 5 μm after applying 2 passes. However, the interconnect length can be made much shorter if the chips were placed very close together. For instance, we also mounted two chips with a spacing of 50 μm , the interconnect length in this case was 300 μm and the thickness was 15 μm by applying 5 passes. Fig. 3.4 shows pictures of the top and cross-section views for the AJP interconnects while the spacing is set at 50 μm between the chips. The total length of the aerosol-jet printed tracks for the complete daisy-chain was about 7.5 mm and 30 vias were opened. The printed tracks have a resistance of around 6 Ω/mm .

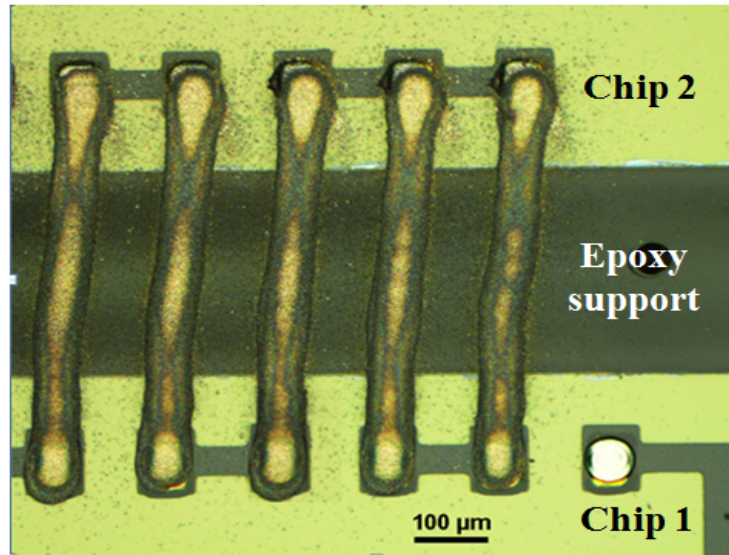


(a)

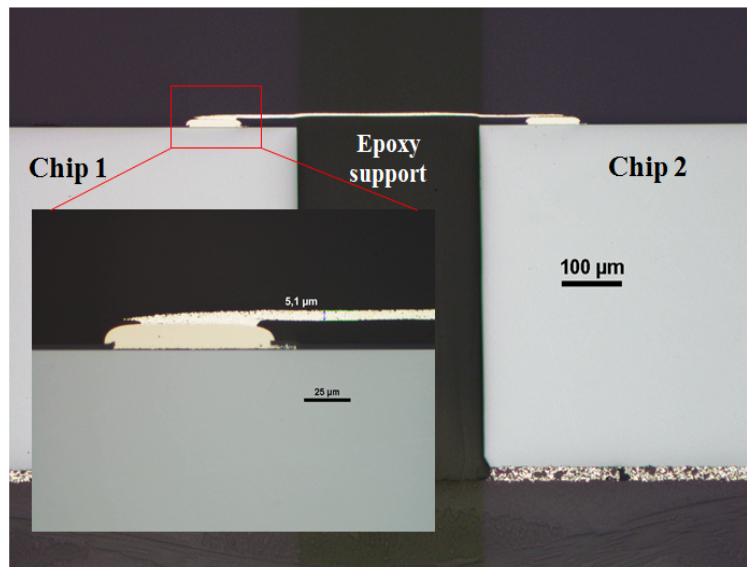


(b)

Figure 3.2: (a) Daisy-chain test chip (b) Test chips with a spacing of 300 μm after opening vias on the contact pads

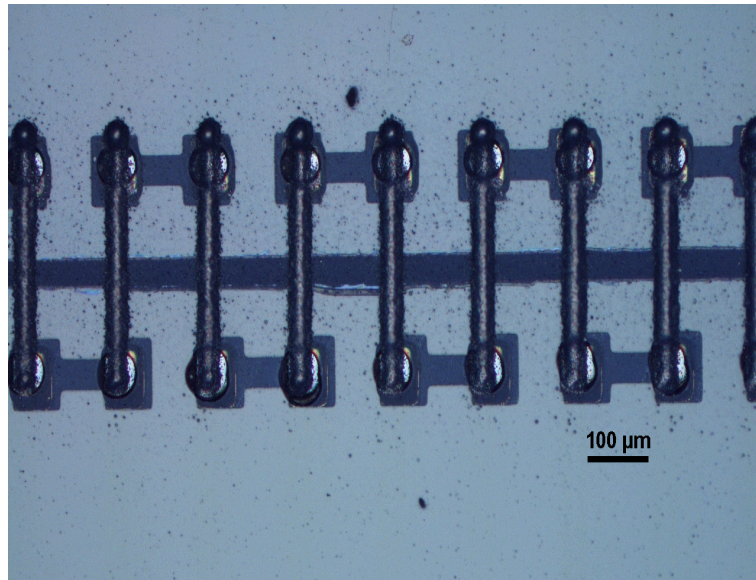


(a)

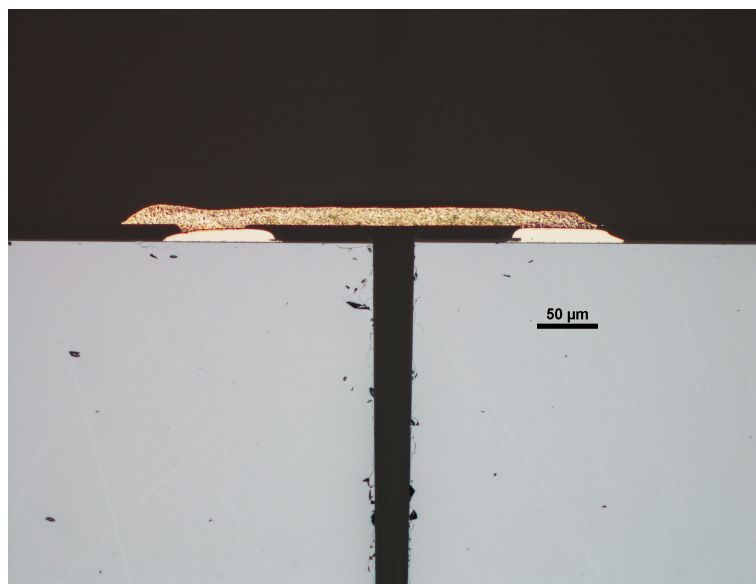


(b)

Figure 3.3: The aerosol-jet printed daisy chain interconnects between the test chips (a) top view (b) cross-section view



(a)



(b)

Figure 3.4: The aerosol-jet printed daisy chain interconnects between 50 μm -spaced test chips (a) top view (b) cross-section view

3.3.2. 85°C/85% RH reliability test

Reliability of optoelectronic systems are critically important in order to ensure the functionality of the system in different environmental conditions. Even if a system performs properly after fabrication, it could malfunction after a certain amount of time due to aging processes. The aging process is mostly induced by the continuous variation of the environmental conditions such as temperature and humidity. Therefore, we performed a standard 85°C/85% RH reliability test [5] to test the functionality of the AJP interconnection. During this test, the samples were exposed to an environment with a constant relative humidity of 85% at a fixed temperature of 85°C. Fig. 3.5 shows the evolution of running the 85°C/85% RH test for 700 hours. The AJP printed interconnects showed no failure or degradation even after running 85°C/85% RH tests for 700 hours. Afterwards, the test was stopped since no failure was observed. The reliability test was performed for 4 different daisy-chain links and the complete daisy-chain resistance was measured every 100 hours. Due to the fact that there is a polymer covering the chips, the sintering temperature for the samples was decreased from 210 °C to 150 °C to avoid any excessive difference in thermal expansion during heating due to CTE (coefficient of thermal expansion) mismatch of the different materials. The used epoxy has a CTE of 55 ppm/°C, while silicon substrates typically have a CTE of 2.6 ppm/°C and the CTE of pure silver is about 19 ppm/°C. Consequently, there is already a CTE mismatch between the three different materials. Hence, the sintering of the printed interconnects was done at 150 °C. As a result, the printed interconnects did not reach the maximum possible conductivity. Hence, the 85°C temperature of the test gradually contributed to evaporate the remaining solvents and increasingly joins the silver flakes in the printed traces. Therefore, the resistance was decreasing during the first 500 hours of the reliability test as shown in the graph until it stabilizes roughly after 500 hours. However, the sintering process could be achieved by using laser sintering as the thermal impact on the polymer is limited in this case and there will be no concern about CTE mismatch. But as discussed in chapter 2, the oven sintering resulted in a higher conductivity than laser sintering. That's why oven sintering was employed in this work. However, laser sintering using continuous laser or longer pulses can achieve better results than the picosecond laser employed in this research. A possible combination of laser and oven sintering can be interesting to test in order to reach the final conductivity of the printed interconnects. Moreover, a different epoxy material with low CTE could be used in order to match that of silicon and silver and in this case higher sintering temperature can be applied to further improve the conductivity of the electrical interconnects.

3.4. Electroless Ni-Au plating

Aluminum (Al) is the most widely used metalization for bond pads in ICs. However, Aluminum is only compatible with wire bonding packaging techniques and not ideal for other packaging solutions such as flip-chip. In our process, we print silver electrical interconnects between the Al bond pads of the chips. From the first experiments, we

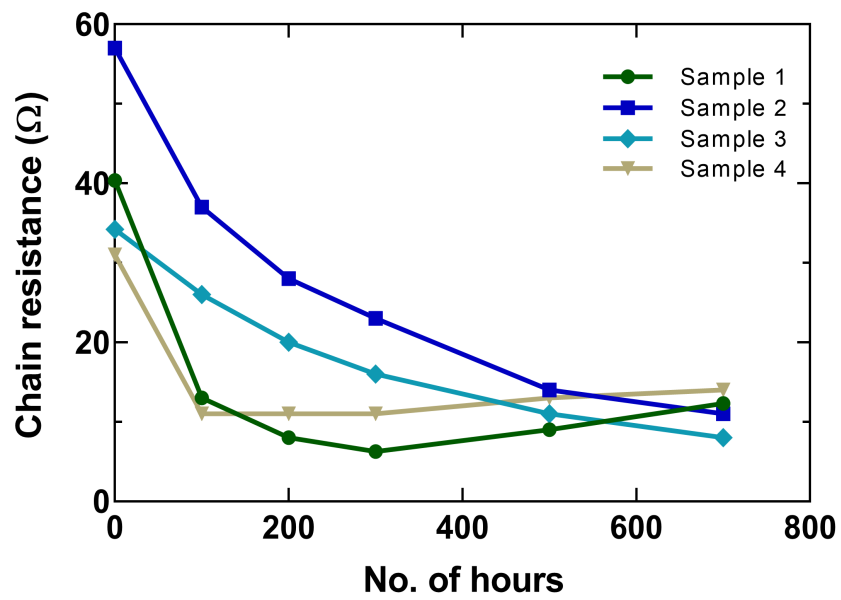
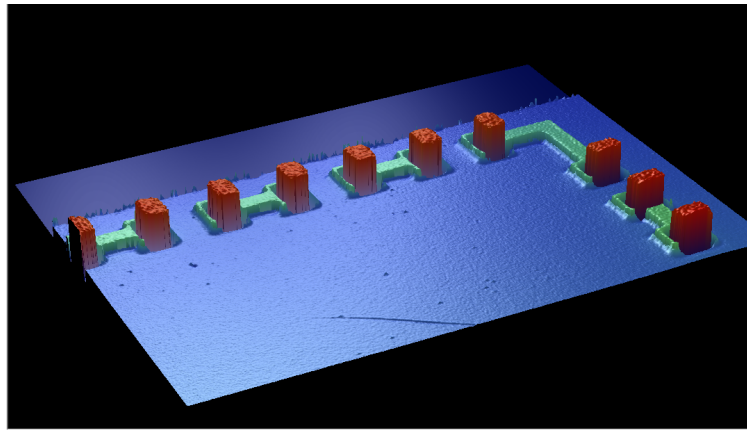
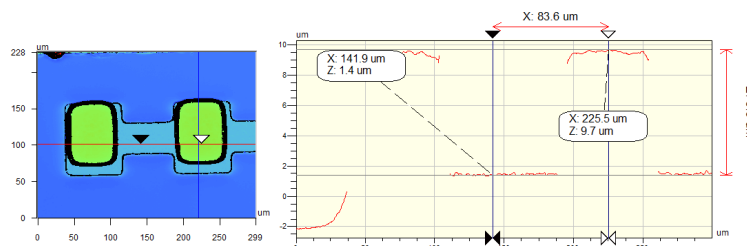


Figure 3.5: The effect of performing $85^{\circ}C/85$ RH reliability test for 700 hours on the daisy-chain resistance



(a)



(b)

Figure 3.6: Profile optical measurements for the Ni-Au bumps applied on a test chip (a) 3D view (b) 2D view

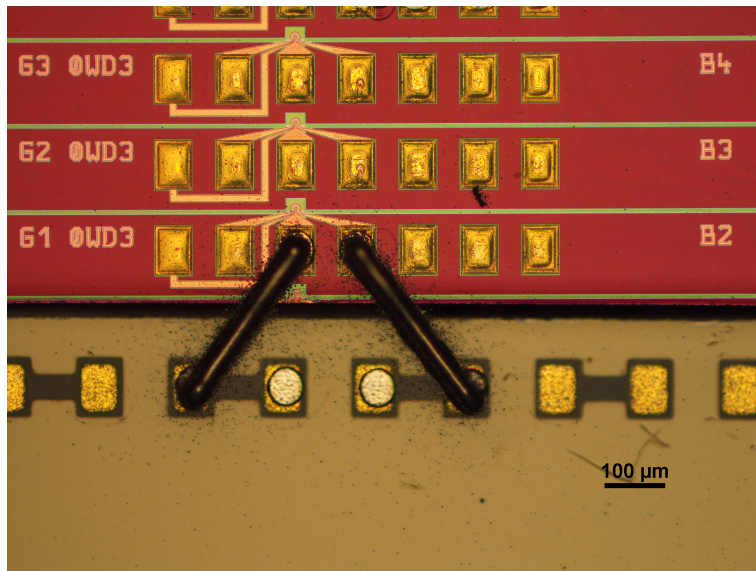
observed that the contact resistance between the printed silver interconnects and the Aluminum finished contact pads was relatively high. That occurred because the Aluminum-silver intermetallics have long-term reliability issues under high temperature and humidity conditions, thus causing high contact resistance [6–8]. Therefore, it was necessary to provide conventional aluminum bond pads with other metallic finishes to avoid the issues induced by silver-aluminum interfacial corrosion. Hence, the Al bond pads were plated with Ni-Au bumps using electro-less Ni-Au plating [9–11]. The Ni-Au bumps specify a typical nickel thickness between $3\ \mu\text{m}$ to $6\ \mu\text{m}$ and a flash of gold with a thickness of $100\ \text{nm}$. The thickness can definitely increase by using longer plating time. The daisy-chain test chips were electroless plated with Ni-Au bumps having a thickness of $8\ \mu\text{m}$. Fig. 3.6 shows 3D and 2D profile optical measurements for the Ni-Au bumps applied on test chip.

3.5. Comparison between bonding wires and aerosol-jet printed interconnects

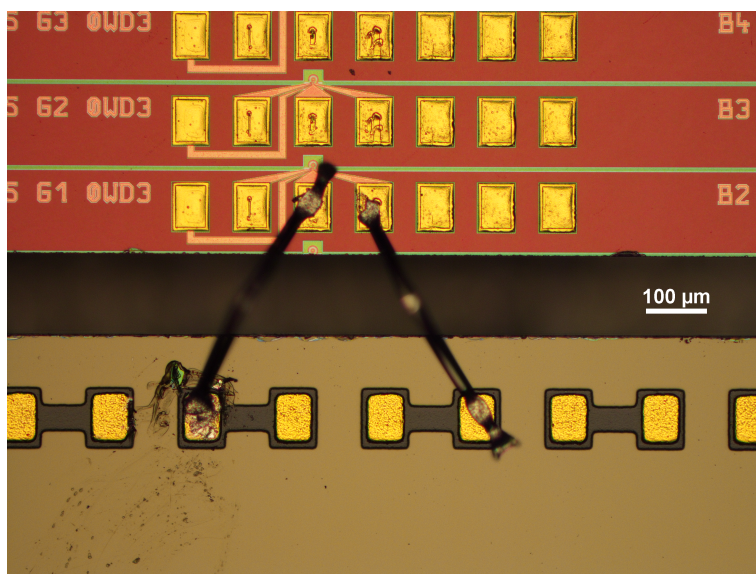
3.5.1. Assembly description

To compare the aerosol-jet interconnects with bonding wires, we developed two assembly schemes; one is interconnected by aerosol-jet printing and the other is wire-bonded. In this comparison, we test the interconnection to a microring modulator [12] separately, without a driver IC. Two versions of the modulator were available, one with 35 GHz 3-dB BW, and one with 46 GHz. For this comparison test, we used the one with a 3-dB BW of 35 GHz while we saved the higher BW ring modulators for the assembly in combination with a CMOS driver IC due to the limited numbers of the higher BW modulator chips. The microring modulator is developed by imec and a detailed description of the modulator is reported in [12]. Silicon microring modulators operating in depletion mode can provide low-voltage operation at high bit-rates, using small foot-print, at the expense of narrow optical bandwidth and the need for thermal control for wavelength stability. The microring waveguide incorporates a p-n junction formed by ion implantation of the silicon. In reverse bias, the carriers are depleted from the p-n junction in the microring waveguide, leading to refractive index and absorption changes in silicon. This results in shifting the ring resonance wavelength to longer wavelengths. In imec's silicon photonics platform, tungsten heaters are integrated in order to control the operating wavelength of the microring modulators upon temperature variations. In [12], the authors use a simplified model of the microring modulator in which it is considered as a low pass filter. The model of the microring modulator is shown in Fig. 3.10b, where C_1 and R_1 are the microring modulator capacitance and series resistance, and C_0 , C_2 and R_2 represent the parasitic pad capacitance and resistance. In order to achieve high modulation bandwidth, it is required to reduce the microring modulator quality factor (Q), as well as the resistance and the capacitance of the p-n junction. The Q-factor can be reduced by increasing the doping in the microring modulator and this will also result in reducing the resistance, but at the expense of increased capacitance. However, reducing the Q factor typically also reduces the extinction ratio and increases the insertion loss of the ring modulator. Hence, a trade-off exists between modulation bandwidth and modulator optical loss.

The developed assembly consists of a ring modulator interconnected to a silicon interposer (daisy-chain), which was realized using the two techniques. Fig. 3.7 shows the realized assemblies by AJP and wire bonding. The interposer has contact pads with a pitch of 150 μm . Hence, this required making the interconnection in both cases under an angle to enable probing the assembly with a 150 μm -pitch RF GS probe. The aerosol-jet interconnects were realized using the same procedure as discussed in section 3.2. For the aerosol-jet interconnection, it was possible to place the modulator and the interposer chips very close together. For the wire bonding interconnection, it was required to leave an additional gap of about 100 μm due to limitations of the used system in order to enable creating the wire loop.



(a)



(b)

Figure 3.7: (a) The microring modulator interconnected by aerosol-jet printing (b) the microring modulator interconnected by wire bonding

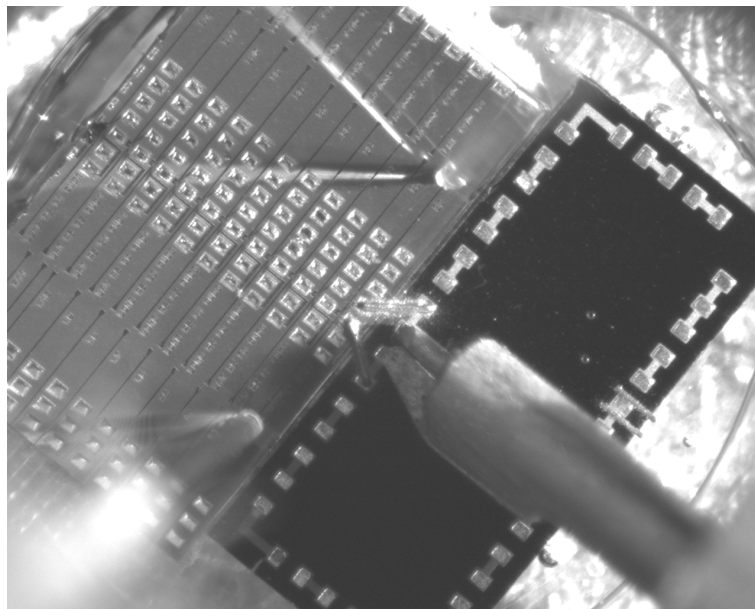


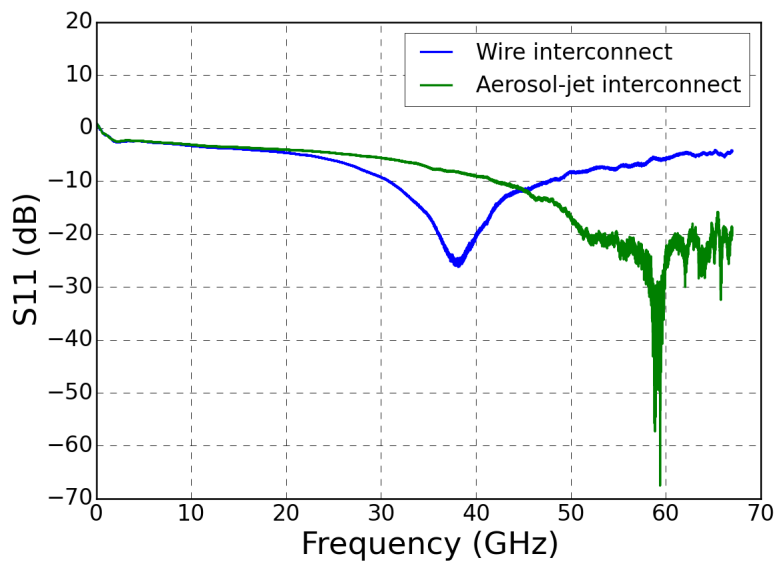
Figure 3.8: The assembly during S-parameter measurements

3.5.2. S-parameters measurements

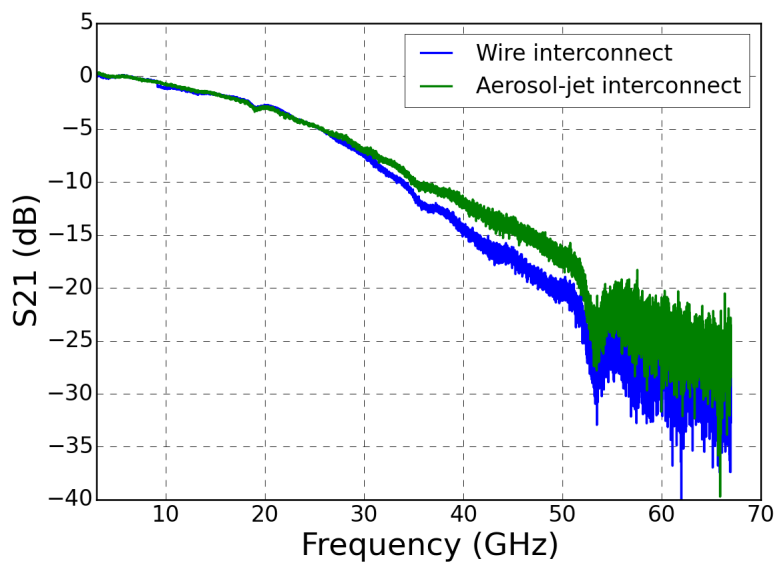
We measured the reflection coefficient (S_{11}) for the aerosol-jet and the bond wire interconnection using a VNA. Fig. 3.8 shows the sample during the S-parameter measurements. The reference plane of the S_{11} measurements was calibrated up to the probe tips using a calibration substrate (short, open, load). Fig. 3.9a shows the measured reflection coefficient (S_{11}) for both the aerosol-jet and wire interconnection with a ring bias voltage of 0 V.

The S_{11} measurements include the reflections from both the aerosol-jet and wire interconnects in addition to the 150 μm -long Al metallization of the silicon interposer. The reflection coefficient S_{11} started at 0 dB because it is modeled as a capacitor as shown in Fig. 3.10b so it is an open circuit at DC. It could also be interesting to print a termination resistor in parallel with the capacitive ring modulator to match it using AJP, which is not possible using wire bonding. The reflection coefficient S_{11} shows the same behavior up to 20 GHz for both the aerosol-jet and wire interconnection. However, at higher frequencies, the wire interconnection started to suffer from a resonance at 38 GHz and afterwards the S_{11} performance starts to degrade till it reaches -5 dB at 67 GHz. On the other hand, the aerosol-jet interconnection shows much better S_{11} performance as the frequency increases. The resonance frequency of the interconnect is situated at a much higher frequency of 59 GHz and the reflections remain below -20 dB until 67 GHz. The S_{11} measurements clearly reflect that aerosol-jet printed interconnects have less parasitic inductance than the wire interconnection. However, the resonance notch of the wire interconnect would be shifted to

a higher frequency if the bondwire was shorter. Although, the wire could be made shorter with other advanced systems, the capability of controlling the interconnect dimensions and creating an impedance-matched transmission line can be only achieved using AJP and it is not possible with conventional wire-bonding technologies. Additionally, the optical transmission coefficient S_{21} was measured for both the AJP interconnect and the wire interconnect as illustrated in Fig. 3.9b. The S_{21} measurements are normalized to 0 dB to remove the optical losses. Although the 3-dB BW for the ring modulator interconnected by AJP and wire-bonding is approximately the same around 20 GHz, the AJP interconnect shows higher transmission than the wire interconnect while increasing the frequency (at higher bit rates). For instance, the AJP interconnect achieves 4 dB higher transmission than the wire interconnect at 50 GHz. From the resulting S_{11} parameters and using the microring modulator model presented in [12], a simplified model of the AJP interconnects is fitted using advanced design system (ADS) software from Keysight technologies in order to provide a good estimate for the AJP interconnects in simulations in order to provide a good estimate for the AJP interconnects in simulations. The model includes an inductor, a series resistor, and a capacitor (L_{ajp} , R_{ajp} , and C_{ajp}) with the following values; 90 pH, 10 Ω , and 0.36 fF. The bondwire has a parasitic inductance of about 1nH/mm for a wire diameter of 25 μm . The microring modulator circuit model [12] is shown in Fig. 3.10b. The equivalent circuit model that was used to extract those values is illustrated in Fig. 3.10a. Additionally, as illustrated in chapter 2, the AJP technology enables realizing impedance-controlled interconnects with high reproducibility and high flexibility in characteristic impedance (e.g. a different Epotek or different line dimensions give different Z_0), whereas with bondwires, there are less possibilities to control the impedance of the interconnects. This is particularly interesting for 50 Ω -matched interfaces (e.g. a traveling-wave electrode Mach-Zehnder modulator), where the impedance mismatch introduced by the bondwires will give significant dips and/or peaking in S_{21} .

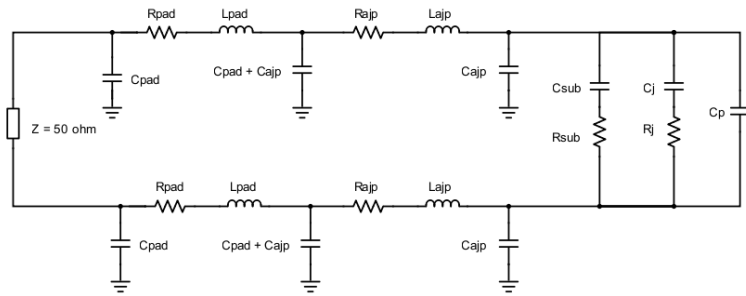


(a)

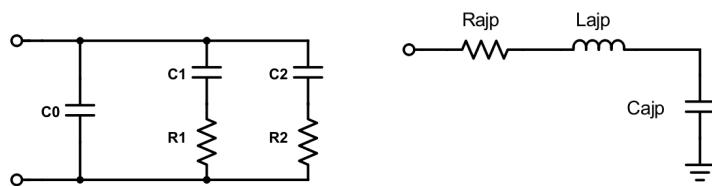


(b)

Figure 3.9: (a) measured S_{11} for the microring modulator with aerosol-jet and bondwire interconnects (b) measured S_{21} for the microring modulator with aerosol-jet and bondwire interconnects

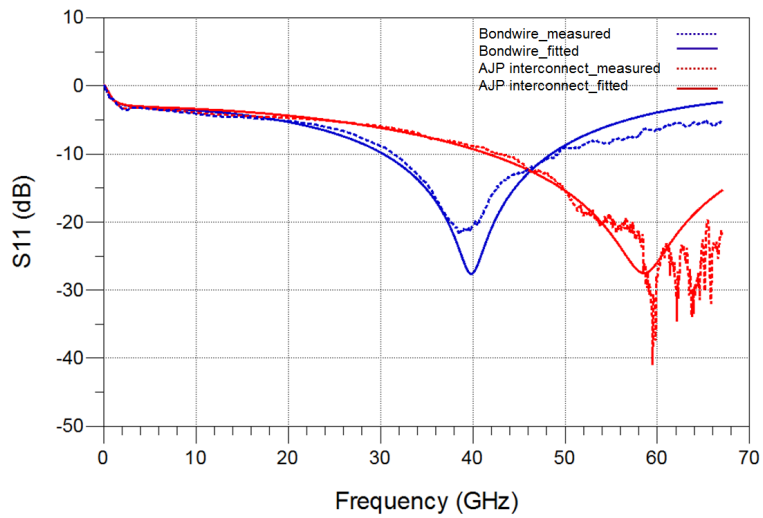


(a)



(b)

(c)



(d)

Figure 3.10: (a) Equivalent circuit model for developed assembly (b) microring modulator circuit model (c) AJP interconnect model (d) Fitting results

3.6. 4-channel VCSEL transmitter assembly

3.6.1. Introduction

VCSELs are considered one of the most widely used, efficient and low cost laser sources. They offer attractive advantages such as low threshold current, compact size, low power consumption, robustness and direct modulation. Since short-reach optical links are commonly employed in today's data center applications, short-wavelength VCSELs (850 nm) have been widely involved in developing optical links for short-reach interconnects [13–16]. An 850 nm VCSEL-based optical link has been demonstrated by IBM at a data rate up to 64 Gb/s over 57 meter of OM4 multimode fiber (MMF) using non-return-to-zero (NRZ) transmission [17]. Additionally, IBM demonstrated a NRZ directly modulated 850-nm VCSEL link operating at 71 Gb/s (back-to-back (BTB)) by integrating a BiCMOS driver with two-tap feed-forward equalization (FFE) and a VCSEL with a 3-dB modulation bandwidth of 26 GHz [18]. Other modulation formats based on multi-level modulation were explored in order to increase the transmission distance. For example, 4-level pulse amplitude modulation (PAM-4) was employed to transmit 40 Gb/s over 100 meter of OM4 MMF using a directly-modulated 850 nm VCSEL [19, 20]. Moreover, short-wavelength VCSEL based parallel interconnects have been developed by increasing the number of channels (VCSEL arrays) [4, 21–24].

The next generations of data centers are likely to use single-mode fiber based optical links for longer transmission distance and higher data rates up to 50 Gb/s and beyond. Long-wavelength VCSELs have a promising potential for long-reach data center intra-connects. Over the past years, a lot of research was conducted to enhance the high-speed modulation of long-wavelength VCSELs [25–29]. As a result, long-wavelength VCSEL links were extensively investigated for long-reach interconnects [30–35]. NRZ modulation of a 1.5 μm VCSEL link up to 56 Gb/s (BTB) and 50 Gb/s after a distance of 2 km was demonstrated [36]. PAM-4 single-mode VCSEL links have also been developed for long distance optical interconnects [37–41].

As mentioned previously, electrical interconnects between electronic and photonic chips are considered one of the main challenges for opto-electronic integration. Wire bonding technology is currently the most widely used technique for electro-photonic packaging. However, wire bonding is not suitable for high-frequency applications due to the high parasitic inductance induced by the wires. Consequently, this will limit the RF performance and cause high reflections and losses at high frequency. Therefore, we use the aerosol-jet printing technology to print the high-speed interconnects between the electronic and photonic dies as a replacement for the traditional bonding wires.

3.6.2. Assembly description

After developing the basic technology on test chips, we started applying the technology on functional chips. As a first demonstrator for the AJP packaging technology, we developed an optical transmitter assembly based on single-mode VCSELs and a BiCMOS electronic

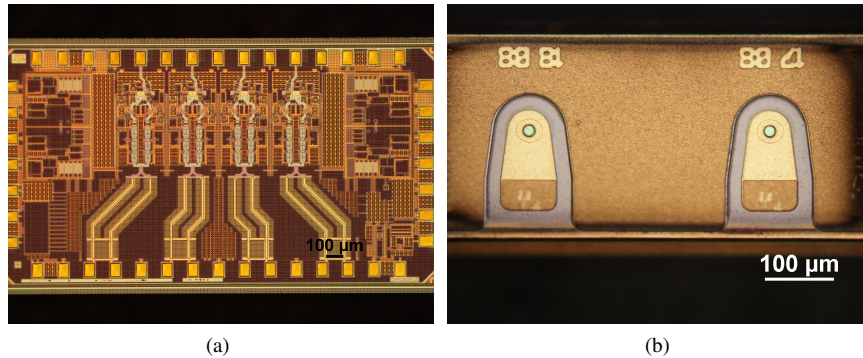
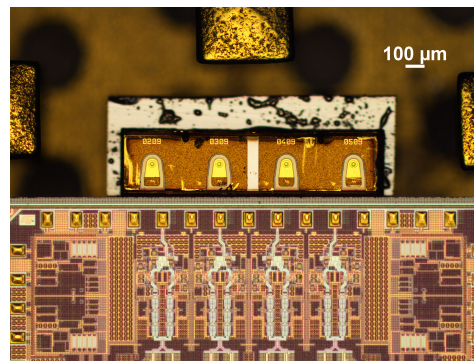


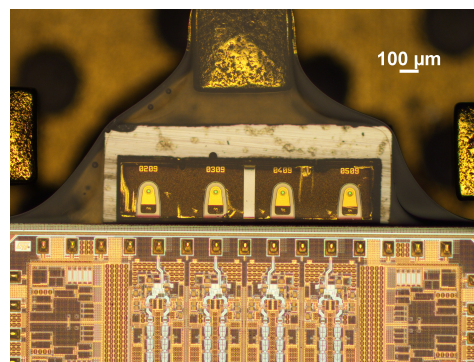
Figure 3.11: (a) The BiCMOS driver chip (b) A 1x2 VCSEL array

driver. The optical transmitter consists of a 4-channel driver and 4 single-mode VCSELs. The VCSELs emit at a wavelength of 1550 nm with a small signal bandwidth around 22 GHz. The VCSELs were developed by the Technical University of Munich (TUM) [27]. The driver chip was fabricated in a $0.13\ \mu\text{m}$ SiGe BiCMOS process [34] and can directly modulate a 4 common-anode VCSELs. The driver chip is developed by IDLab in UGent [PhD. Wouter Soenen]. The driver Al bond pads were plated with Ni-Au bumps using electroless plating to avoid the high contact resistance issue. Fig. 3.11 shows the pictures of the used BiCMOS driver chip after NiAu plating and the 1x2 VCSEL array. The thickness of the NiAu bumps was $3\ \mu\text{m}$. The VCSELs have gold contact pads and therefore did not require post processing. Since the driver chip has a thickness of $375\ \mu\text{m}$ and the VCSEL is $75\ \mu\text{m}$ -thick, the VCSELs were mounted on a silicon interposer with a thickness of $300\ \mu\text{m}$ in order to obtain the same height for all chips. Then, the chips were glued to the PCB using a non-conductive adhesive and decoupling capacitors were glued to the PCB using an electrically conductive adhesive. Next, the chips were covered with the transparent epoxy and vias were opened on the contact pads using the process described in section 3.2. Fig. 3.12 shows the assembly process steps from chip placement till via opening.

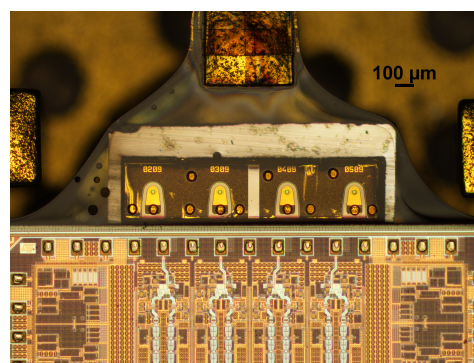
Finally, the high-speed interconnects were precisely printed from the driver chip to the VCSELs and also from the VCSELs anode to the decoupling capacitor. Fig. 3.13 shows the resulting assembly after printing the high-speed interconnects between the driver and VCSELs chips. The distance between the driver and the VCSELs was kept as short as possible by mounting the chips very close together to minimize the parasitics. This enabled making the interconnects from the driver to the VCSELs as short as $200\ \mu\text{m}$. The aerosol-jet printed interconnects have a width of $40\ \mu\text{m}$, a thickness of $15\ \mu\text{m}$ and a length of $200\ \mu\text{m}$. The other interconnects for providing the supply voltage for the driver chip were wire-bonded as the electrical DC connections have no effect on the high-speed performance of the assembly. However, a complete printed assembly is feasible if a ramp is created at the chip edges. In this case the interconnects would be printed up till the traces on the PCB.



(a)



(b)



(c)

Figure 3.12: Assembly process steps of the VCSEL transmitter (a) after chip placement (b) after polymer dispensing (c) after via opening

Fig. 3.14 shows the demonstrator of the 4-channel VCSEL transmitter. The VCSELs were biased at an average current of 8.7 mA for all the experiments. The light is coupled out of the VCSELs using lensed fibers. The measured optical eye-diagrams at 50 Gb/s for 3 channels are shown in Fig. 3.15. Channel 4 was damaged during the testing process.

3.7. Silicon photonics based optical transmitter assemblies

3.7.1. Introduction

Silicon photonic based optical transceivers are capable of achieving very high-speed data rates which make them a promising candidate for data center intraconnects. Silicon photonic modulators such as microring and electro-absorption modulators (EAM) [12, 42–46] have a small footprint and low capacitance, thus making those devices ideal for high-speed data center communication. Recently, a real time 100 Gb/s NRZ-OOK transmission has been demonstrated using GeSi EAM implemented on a silicon photonics platform [47, 48]. Additionally, an optical transmitter consisting of GeSi EAM and ultra low power fully differential SiGe BiCMOS driver was demonstrated at 70 Gb/s [49]. Furthermore, a low power optical transmitter based on a microring modulator and a CMOS inverter based driver IC was successfully demonstrated at 56 Gb/s [50].

Most of the reported silicon photonic optical transceivers are assembled using wire bonding technology. However, the next generations of optical transceivers for data center applications demand highly efficient packaging technologies with much lower parasitic inductance that can improve the bandwidth and sustain the massive increase in data rates for optical links. Therefore, we applied the AJP interconnection technology as a potential alternative for the traditional packaging technologies to assemble silicon photonic modulators in combination with a low-power CMOS driver IC to develop high-speed optical transmitters.

3.7.2. CMOS driver and electro-absorption modulator assembly

Imecs silicon photonics platform [12] was selected which includes many photonic devices including high-speed EAMs and microring modulators. The driver chip (provided by IDLab-UGent) was fabricated in a 28 nm fully depleted silicon-on-insulator (FDSOI) CMOS process [50]. Since the driver and the modulator chips have Al contact pads, they were electro-plated with NiAu bumps for the same reason as discussed in section 3.4. Since the driver chip has a thickness of 250 μm and the modulator is 500 μm -thick, the modulator chip was thinned-down to 250 μm to achieve the same height as the driver chip. The modulator, driver and decoupling capacitors were die-bonded to the PCB using an electrically conductive adhesive. The high speed interconnects were realized using the same printing process as described in section 3.2. The printed interconnects have a width of 45 μm , a thickness of 15 μm and a length of 300 μm . Fig. 3.16 shows the resulting

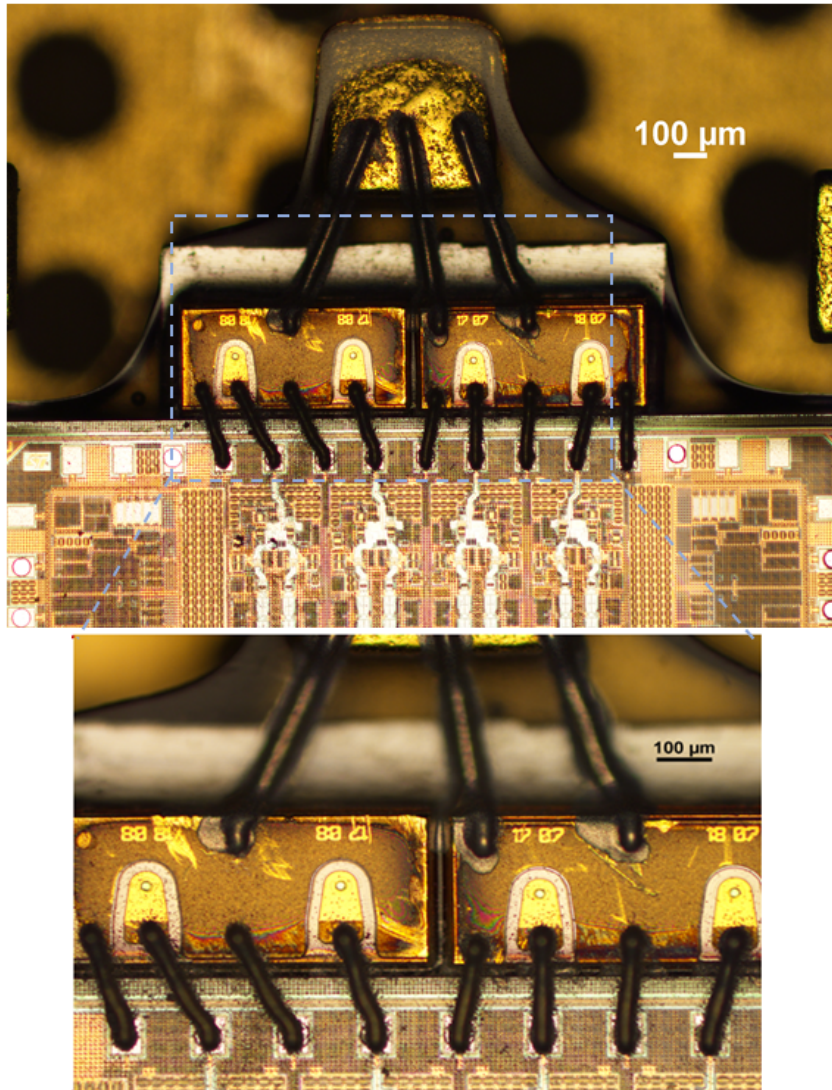


Figure 3.13: The assembly of the 4-channel driver IC and 4 single-mode VCSELs

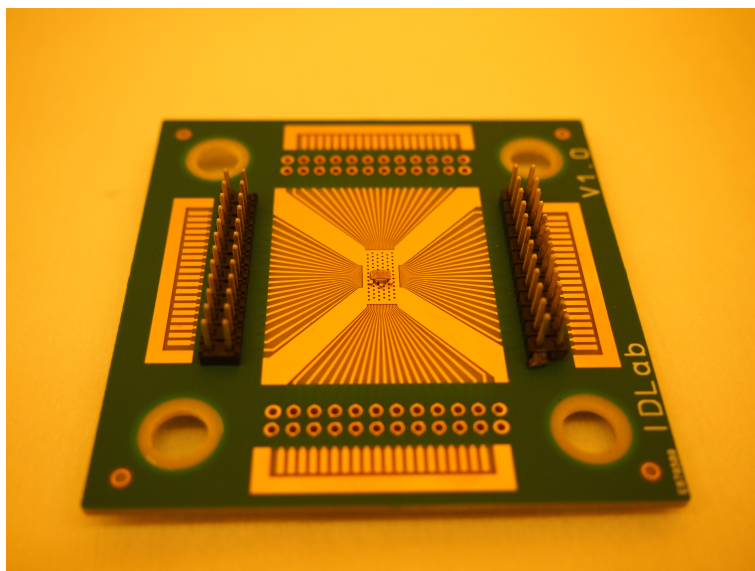


Figure 3.14: The 4-channel VCSEL optical transmitter demonstrator

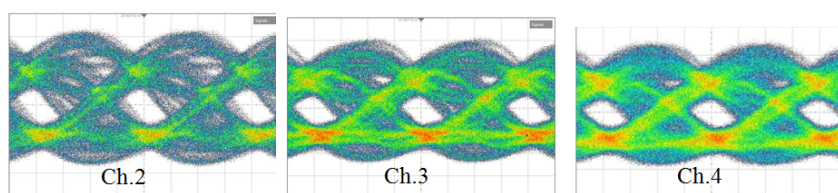


Figure 3.15: The measured back to back eye diagrams at 50 Gb/s for 3 channels

assembly of the EAM modulator and the driver. The light is coupled in and out of the EAM modulator by two grating couplers at 1560 nm. The measurement setup is illustrated in Fig. 3.17. The resulting back to back optical eye-diagrams are shown in Fig. 3.18 at 40 Gb/s, 50 Gb/s and 56 Gb/s. The eyes are clearly open even after transmission distances of 1 km and 2 km standard single-mode fiber as illustrated in Fig. 3.19 and Fig. 3.20. An extinction ratio (ER) of 2.83 dB was achieved while applying a drive voltage of $1 V_{pp}$. The driver uses an RC bias tee to reverse-bias the EAM to -0.8 V. The resulting ER is close to the value obtained in [12].

3.7.3. CMOS driver and microring modulator assembly

In this assembly, we used a C-band ring modulator with a 3-dB BW of 46 GHz fabricated using imecs silicon photonics platform [12]. The same driver chip from the EAM assembly was also used for the microring modulator [50]. The driver and the modulator chips were plated using NiAu electroless plating to avoid the interfacial corrosion between the silver AJP interconnects and the Al contact pads. The modulator die which is 500 μm -thick, was thinned-down to 250 μm to match the thickness of the driver chip. The high speed interconnects were also realized using the same printing process. Fig. 3.21 shows the resulting assembly of the ring modulator and the driver. The contact pads were opened using excimer laser ablation by projecting the laser beam through a circular mask with a diameter of 150 μm . The high-speed silver interconnects were printed from the CMOS driver to the ring modulator. The other contact pads for electrical DC connections were wire-bonded. Light was coupled into and out of the ring modulator by two grating couplers. Since no on-chip heaters were available to tune the resonance wavelength of the microring modulator, a tunable laser was used to find the optimal wavelength (1546.1 nm) for maximum eye opening. The laser power was set at 12 dBm and the power reaching the microring is about 6 dBm due to the grating coupler losses. Fig. 3.22 shows the measured back-to-back optical eye-diagrams at 50 Gb/s, 56 Gb/s and 60 Gb/s. The eyes are clearly open even after transmission distances of 1 km and 2 km SSMF as illustrated in Fig. 3.23 and Fig. 3.24. The overshoot in the rising edge of the realized assembly is minimized compared to the wire-bonded assembly [50]. An ER of 4.63 dB was achieved while applying a drive voltage of $1 V_{pp}$. The resulting ER is higher than the value obtained in [50] using bonding wires. The measured optical insertion loss at this ER is about -11 dB.

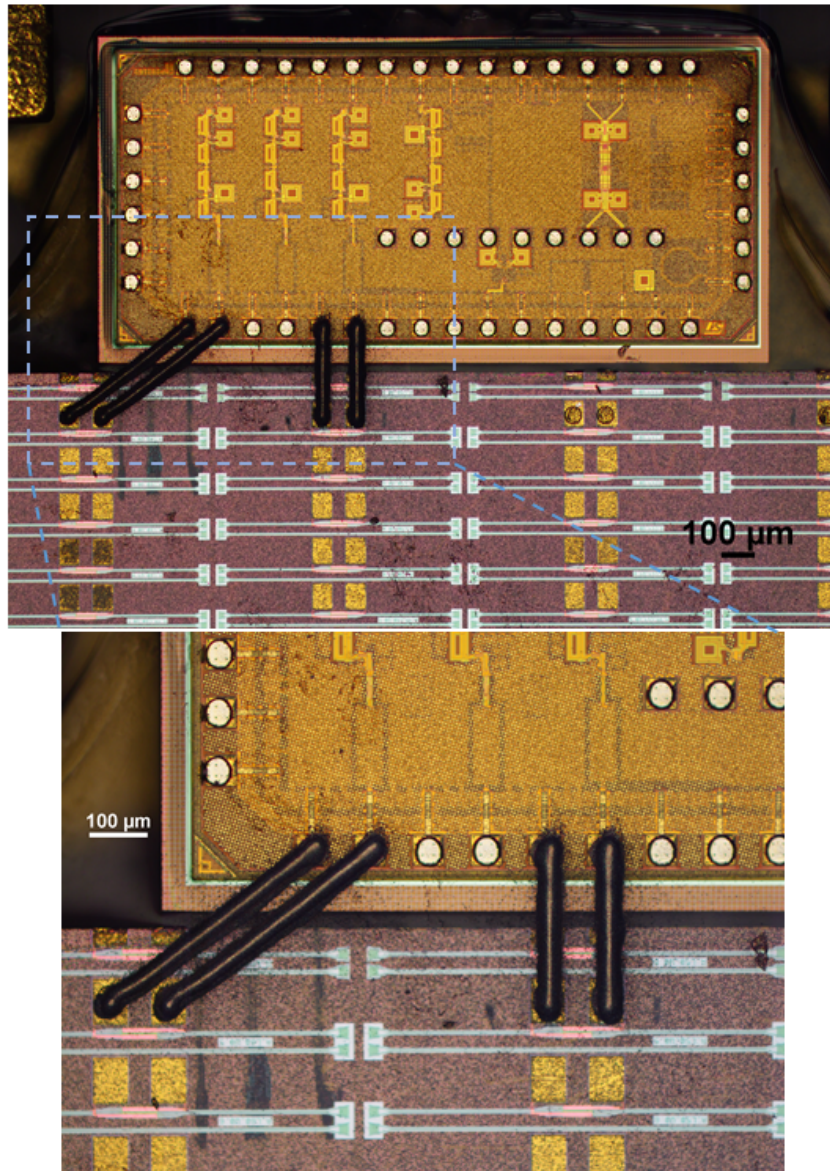


Figure 3.16: The assembly of the EAM modulator and CMOS driver interconnected by AJP

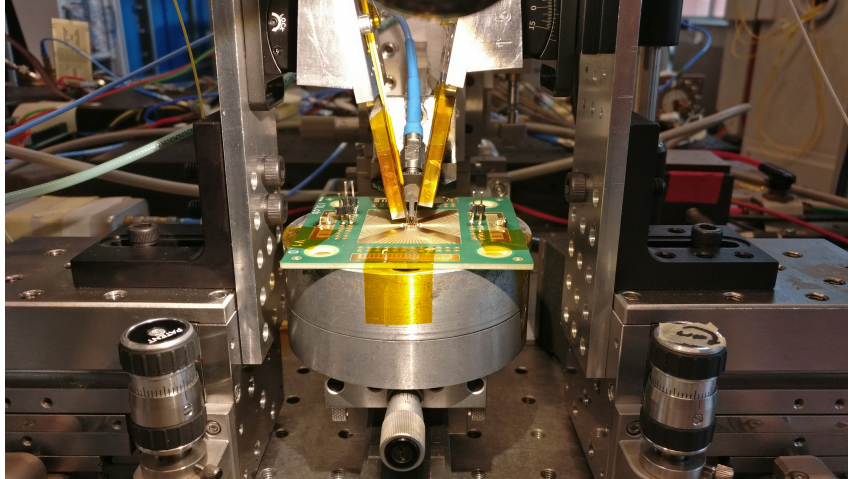


Figure 3.17: The high-speed characterization setup

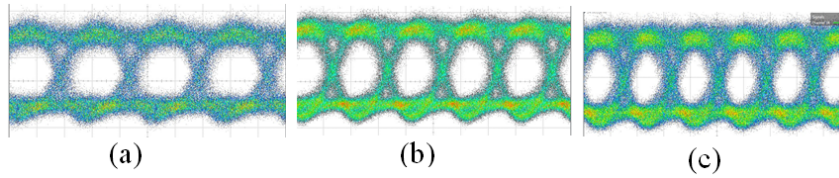


Figure 3.18: The measured back to back eye diagrams (a) 40 Gb/s, (b) 50 Gb/s, and (c) 56 Gb/s

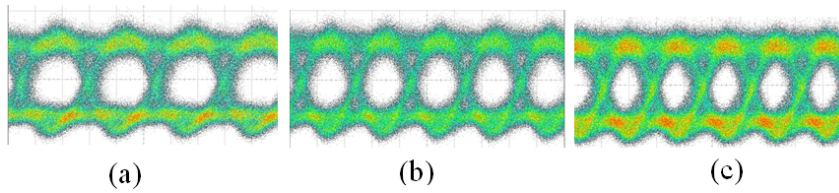


Figure 3.19: The measured eye diagrams after 1 km of SSMF fiber (a) 40 Gb/s, (b) 50 Gb/s, and (c) 56 Gb/s

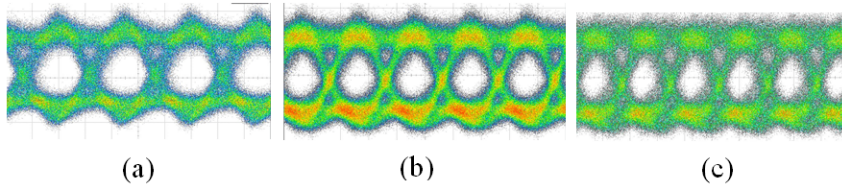


Figure 3.20: The measured eye diagrams after 2 km of SSMF fiber (a) 40 Gb/s, (b) 50 Gb/s, and (c) 56 Gb/s

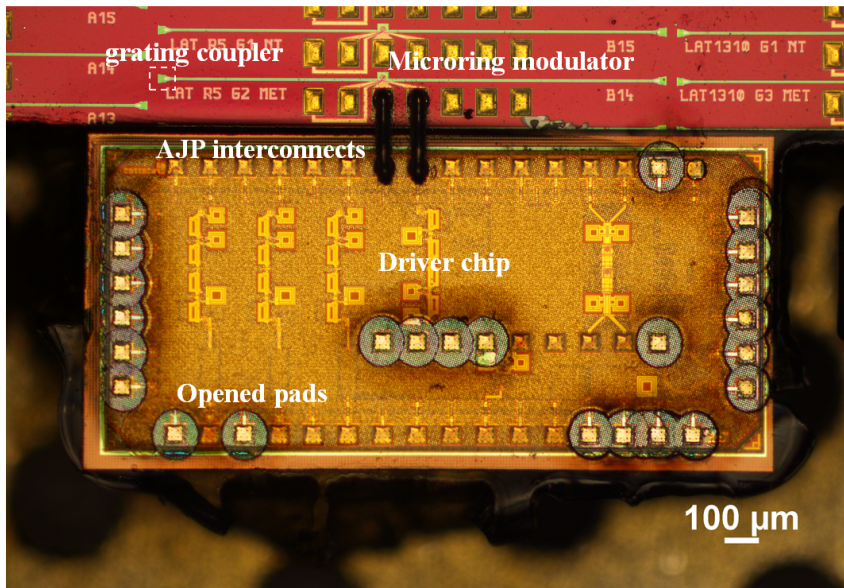


Figure 3.21: The assembly of the microring modulator and CMOS driver interconnected by AJP

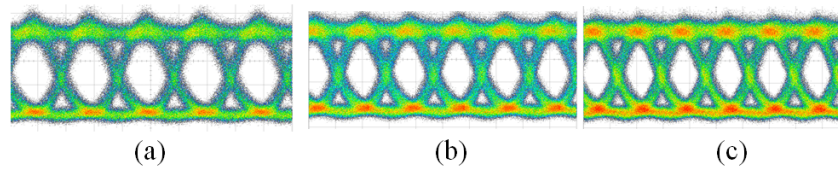


Figure 3.22: The measured back to back eye diagrams (a) 50 Gb/s, (b) 56 Gb/s, and (c) 60 Gb/s

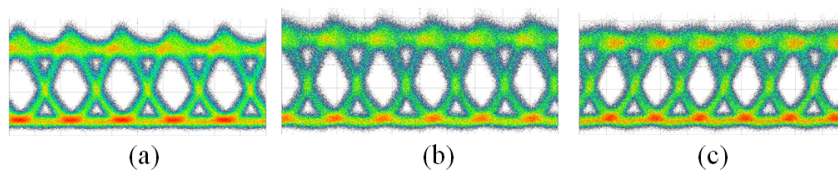


Figure 3.23: The measured eye diagrams after 1 km of SSMF fiber (a) 50 Gb/s, (b) 56 Gb/s, and (c) 60 Gb/s

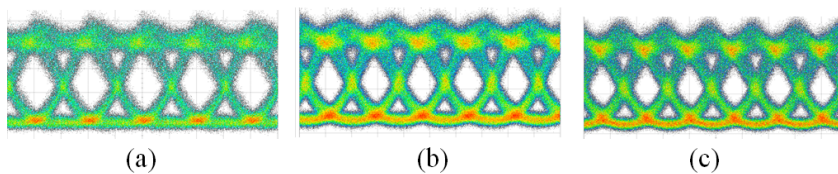


Figure 3.24: The measured eye diagrams after 2 km of SSMF fiber (a) 50 Gb/s, (b) 56 Gb/s, and (c) 60 Gb/s

3.8. Conclusions

In this chapter, we demonstrated a flexible face-up 2.5D packaging technique for hybrid electronic-photonic integration as a potential alternative for the wire-bonding technology. It is well known the bonding wires suffer from high parasitic inductance particularly at high frequency. The proposed technology is capable of printing very short high-speed interconnects (down to 100 μm) with the freedom to tune the characteristic impedance for better impedance matching and lower reflections. The high-speed interconnects between electronic and photonic IC dies were printed using aerosol-jet technology. The fabrication process flow was discussed in detail. The technology was tested first on daisy-chain test chips and the interconnection between the test chips was successfully realized. Then, a standard 85°C/85% RH reliability test was performed to investigate the long term functionality of the realized AJP interconnection. After running the reliability test for 700 hours, no failure or degradation was observed.

Afterwards, the aerosol-jet printed interconnects were benchmarked with the traditional bonding wires. Two assemblies were developed; one is interconnected by aerosol-jet printing and the other is wire-bonded. The measured reflection coefficient (S_{11}) of the aerosol-jet printed interconnects showed an increase in resonance frequency of 20 GHz compared to Al bonding wires. This reflects that AJP interconnects have less parasitic inductance than the wire interconnection. Additionally, the optical transmission coefficient showed 4 dB higher transmission than the wire interconnect at 50 GHz. The advantage of the AJP interconnects is that the characteristic impedance can be flexibly tuned while this option is not possible for the bond-wires. Besides, the length of the AJP printed interconnects can be very short and the effect of the parasitic inductance will be very limited compared to the bond-wires.

At last, the technology was applied on functional chips. A 4-channel VCSEL transmitter consisting of 4 single-mode VCSELs and a BiCMOS driver IC was successfully demonstrated at 50 Gb/s. Additionally, the technology was also successfully applied on silicon photonic chips. An assembly of EAM and a CMOS driver IC was realized and clear open eye diagrams were obtained at 40 Gb/s, 50 Gb/s, 56 Gb/s even after 2 km of SSMF. Moreover, an assembly of a microring modulator and the same CMOS driver IC was also developed and clear open eye diagrams were successfully obtained at 50 Gb/s, 56 Gb/s, and 60 Gb/s after 2 km of SSMF. The realized optical transmitters can be exploited in long and short-reach data center intraconnect optical links.

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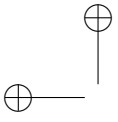
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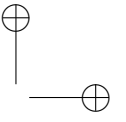
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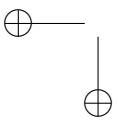


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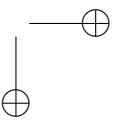


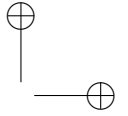
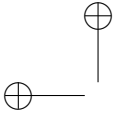
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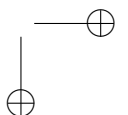
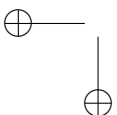
4

Direct-write lithographic (DWL) patterning of single-mode polymer waveguides

In the previous chapter, we focused on the development of electrical interconnects for high-speed optical transmitters. This chapter will handle the realization of optical interconnects based on single-mode polymer waveguide using direct-write lithography. Two optical material systems including epoxy and siloxane polymers will be presented. The cut-off single-mode waveguide dimensions will then be calculated for both the core materials using a numerical mode solver. Next, the fabrication process flow of the polymer waveguides will be described in detail. In particular, a focus will be put on the direct-write lithography process and the corresponding optimization of patterning the core materials. The characterization results of the fabricated waveguides will be introduced including the cut-back measurements at datacom wavelengths. At last, single-mode polymer waveguide crossings will also be realized and characterized.

4.1. Introduction

Optical interconnects are a promising candidate to meet the demand for the data centers scaling up and overcome the limitations of electrical interconnects for short and long distance communications. Optical interconnects via polymer waveguides [1–3] have attracted considerable attention owing to the processing flexibility on different substrates (PCB,



glass, silicon, etc.), scalability (large area manufacturing compatibility), cost efficiency and high coupling efficiency to optical fibers and integrated optoelectronic chips such as vertical cavity surface emitting lasers (VCSELs) and photodiodes [4–6]. Particularly, single-mode polymer waveguides are a promising candidate for communication between integrated photonic chips and single-mode optical fibers (SMFs) on the package and board level. Additionally, they provide enhanced functionalities such as light routing, power splitting, and optical (de-)multiplexing. Furthermore, they can be integrated with the emerging silicon photonics technology as spot size converters via low-loss adiabatic coupling [7]. Various optical polymer materials have been developed for the fabrication of optical waveguides [8, 9]. The waveguide materials criteria are mainly determined by a number of properties such as low absorption loss in the near infrared (NIR) for datacom applications, large-area processability, low-cost due to process compatibility with established PCB manufacturing, and reliability during manufacturing and system operation. The material physical properties also determine which fabrication technique is employed to develop the optical waveguides. Several fabrication techniques have been reported for single-mode polymer waveguides such including mask photolithography [10], reactive-ion etching [11], UV imprinting [12, 13], and laser ablation [14, 15]. In this chapter we will focus on the fabrication and characterization of single-mode polymer waveguides defined by direct-write lithography (DWL).

The optical waveguide is a structure that allows confining and guiding light across its boundaries. It consists of two materials; core and cladding, in which the core material exhibits higher refractive index than the cladding materials so that the light can propagate in the core layer by total internal reflection (TIR). Several kinds of optical waveguides exist and are sorted according to the following criteria: number of modes (single-mode or multimode), geometry (planar, strip, ridge, or fiber waveguides), refractive index distribution (step or gradient index). The light can be confined in one direction (slab waveguide) or two directions (rectangle waveguide) and in this case the light propagates in a perpendicular direction to the structure cross-section. In this dissertation, we target developing step-index single-mode rectangle waveguides. Fig. 4.1 shows a schematic of a rectangle waveguide where the refractive index of the core material is chosen to be higher than the cladding to achieve TIR and the light propagates across the Z-direction.

4.2. Optical waveguide materials

Polymer waveguide materials offer several advantages such as cost-effectiveness, flexibility, ease in processing and device fabrication. Different types of polymer materials have been explored to realize optical waveguides such as acrylate [16], epoxy [17], polyimides [18], Polydimethylsiloxane (PDMS) [19], siloxane [20], and fluorinated polymers [21]. Each polymer type has its own advantages and disadvantages depending on the material properties and the desired application. For the optical waveguides developed in this thesis, the material choice is decided based on following characteristics:

- Low optical absorption (intrinsic loss)

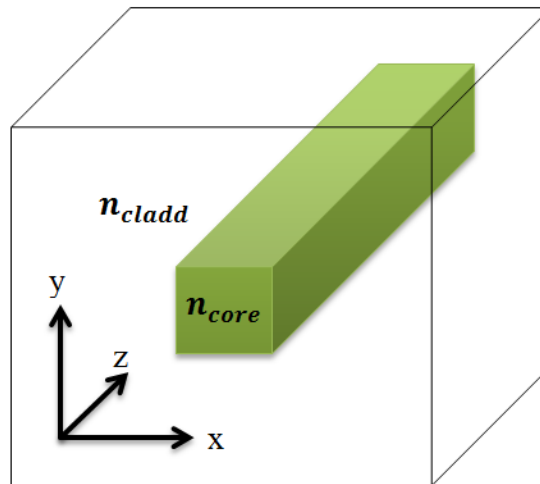


Figure 4.1: A schematic of a rectangular strip waveguide

- Processing flexibility including large-area scalability, high-volume production, manufacturing compatibility with printed circuit boards (PCBs), and compatibility with different waveguide fabrication technologies particularly direct-write lithography (DWL)
- Low viscosity materials: the main goal is to fabricate single-mode waveguides, which have a typical core thickness of about $5\ \mu\text{m}$. So, the requirement of having low and medium viscosity materials is essential so that thin layers can be achieved particularly for the core material.
- Refractive index tuning capability: one important feature of the polymer waveguide materials is that the refractive index can be easily tuned according to the desired application. For single-mode waveguides, sometimes it is required to reduce the index contrast between the core and cladding materials in order to increase the cut-off core size and thus providing some tolerance during the fabrication process as well as relaxed alignment during light coupling from single-mode fibers to the waveguides.
- Integration capability with lasers and photo-detectors as well as silicon photonics technology

For optical interconnects in telecoms applications, the optical loss at the near infrared (NIR) range is considered the most important material characteristics. The optical absorption loss in polymer materials is predominantly attributed to the bond vibrations induced by the C-H and O-H groups. Most polymer materials exhibit high absorption at the near

infrared bands due to the high bond vibrations (C-H & O-H bonds) over this range. As for the visible range, the bond vibrations are much less. Hence, this will result in a lower absorption. An effective way to reduce the intrinsic absorption loss is to design polymers in which the highly absorbing C-H groups are replaced with fluorocarbon groups (C-F) [22]. Fluorinated polymers exhibit very low absorption loss in the NIR band as their C-F molecular bonds exhibit very low vibrational absorption in this range. The lowest loss polymer waveguides in the near-infrared was reported for fluorinated acrylates [23] fabricated by indirect photolithography (0.04 dB/cm at 1.31 μm and 0.05 dB/cm at 1.55 μm wavelength).

In this dissertation, two material systems (epoxy and siloxane) were selected for which commercially available formulations exist and both are compatible with the DWL process. These polymer materials are specifically designed for the fabrication of optical waveguides and they show good thermal stability, high mechanical robustness and excellent reliability in high humidity environments.

4.2.1. Siloxane material

The siloxane-based system is commercially known as LightLink™(MicroChem) having a cladding and a core version (XP-6701A LightLink™core and XP-07423A LightLink™cladding with 65 % solids weight in PGMEA). Tze Yang Hin et al. reported the refractive index measurements of the LightLink™core at 847 nm [24]. According to our measurements, the relative refractive index contrast between both versions is 2.3 % at 1.55 μm ($n_{\text{clad}} = 1.473$ and $n_{\text{core}} = 1.507$). A relative index contrast of about 1% was targeted to enable the realization of single-mode waveguides (both at 1.31 μm and 1.55 μm) with a core size not smaller than 4 μm x 4 μm ; providing an efficient coupling to standard single-mode fibers. Therefore, the index contrast was reduced by using an appropriate mixture of the core and cladding materials as the waveguide cladding. The relative index contrast decreased to 1.06% by increasing the cladding index to 1.491. The mixing process is performed as follows; the core and cladding materials were blended with ratios of 55%:45% respectively and stirred for 2 hours at room temperature. Then, the material mix was left to rest for 1 day to remove the mixing induced air bubbles. Finally, the refractive indices of the LightLink™cladding, core and mix were measured using spectroscopic ellipsometry as shown in Fig. 4.2.

4.2.2. Epoxy material

The selected epoxy-based system is commercially known as EpoClad/EpoCore (Microresist Technology); and is available in different versions with different viscosities. This offers flexibility in the waveguide dimensions according to the desired application. In this work, we used the Epocore 5 version optimized for achieving a core thickness around 5 μm and we also used a higher viscosity version for the cladding material (EpoClad 50). The EpoCore/EpoClad materials show high flexibility and precision in the fabrication process. The material can be patterned using standard photolithography, direct-write lithography

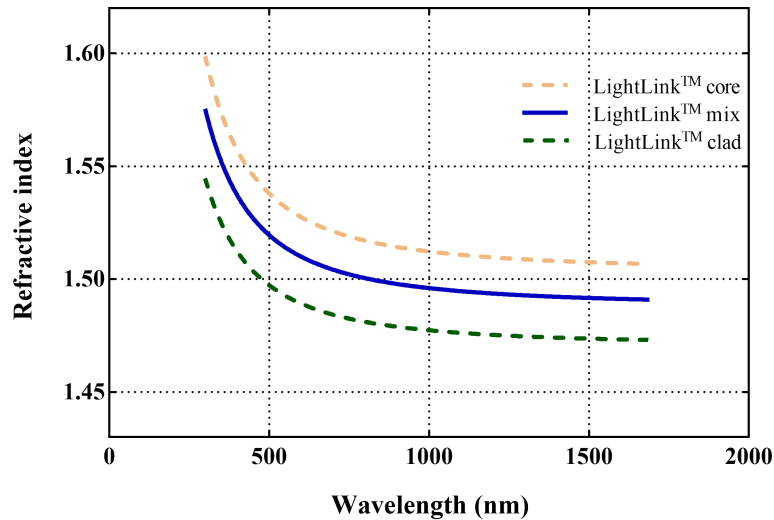


Figure 4.2: The refractive index as a function of the wavelength for the siloxane (LightLink™) materials

and UV imprinting. The refractive index can also be tuned by mixing the core and cladding materials. However, the optical intrinsic loss at a wavelength of 850 nm is 0.2 dB/cm, which is higher than other low-loss polymers. The relative refractive index contrast is 0.465 % at 1.55 μm ($n_{\text{clad}} = 1.570$ and $n_{\text{core}} = 1.577$). The refractive indices curves of the cured EpoCore and EpoClad materials are plotted using Cauchy's equation provided by the datasheet from Microresist Technology [25] as depicted in Fig. 4.3. This low index contrast enables the fabrication of waveguides with relaxed single-mode dimensions.

4.3. Calculation of cut-off single-mode dimensions

Several techniques are used to simulate waveguide structures such as beam propagation method (BPM) [26], finite-element method (FEM) [27], transfer matrix [28], and eigenmode expansion method [29]. We used a numerical mode solver from Lumerical to simulate the waveguide structures. Based on the refractive index measurements for both polymer material systems, the influence of various parameters on the waveguide mode profiles were simulated using Lumerical (Mode solutions) to ensure the single mode operation at a wavelength of 1.31 μm and 1.55 μm . The refractive indices of the polymer materials were used as inputs for the simulations in order to determine the maximum single-mode core size. The graph in Fig. 4.4 shows the relation between the cut-off single-mode core size

Table 4.1: The main characteristics of LightLink™ materials

Parameter	LightLink™
Core refractive index @ 1550 nm	1.507
Cladding refractive index @ 1550 nm	1.473
Spectral sensitivity [nm]	Broadband, 365 nm
Coefficient of Thermal Expansion (ppm/°C) (by DMA, 50°C Hold 10 min, ramp 10°C/min to 350°C)	135-140
Optical loss [dB/cm] @ 850 nm	~ 0.05 dB/cm
Glass transition temperature	166°C

Table 4.2: The main characteristics of EpoCore and EpoClad materials

Parameter	EpoCore/EpoClad
Core refractive index @ 1550 nm	1.577
Cladding refractive index @ 1550 nm	1.57
Spectral sensitivity [nm]	Broadband, 365 nm
Volume shrinkage [%]	<3 %
CTE (20-100 °C) [ppm/K]	~ 50
dn/dT (589 nm) [10 ⁻⁴ /K]	~0.5-0.7
Optical loss [dB/cm] @ 850 nm	~ 0.2 dB/cm
Thermal stability	up to 230°C
Glass transition temperature	180°C

and the relative index difference between the core and cladding materials for single mode operation at 1.31 μm and 1.55 μm . For this simulation, the index of the cladding material was selected to be 1.53 (average value of EpoClad and LightLink™ cladding refractive indices). It is clear that for a certain index contrast there is a corresponding maximum core size for single mode operation (cut-off core size) and the higher this index contrast, the smaller this cut-off core size. The relative index contrast for the epoxy system at 1.31 μm and 1.55 μm is almost the same and corresponds to 0.465%. For the siloxane system (after mixing), the relative index contrast is 1.06% at 1.31 μm and 1.55 μm . The resulting cut-off core sizes for the EpoCore waveguides corresponded to 6.2 μm and 7.6 μm at 1.31 μm and 1.55 μm respectively, while the cut-off core sizes for LightLink™ waveguides (with mixing) corresponded to 4.2 μm and 5.1 μm at 1.31 μm and 1.55 μm respectively. Moreover, it is obvious that the cut-off core size for LightLink™ increased to 4.2 μm and 5.1 μm (with mixing) instead of 2.7 μm and 3.2 μm (relative index contrast of 2.3% without mixing) at 1.31 μm and 1.55 μm respectively. This slight increase in the cut-off core size after reducing the index contrast of the LightLink™ materials was necessary in order to provide a sufficient tolerance in the fabrication and characterization processes of the single-mode LightLink™ waveguides.

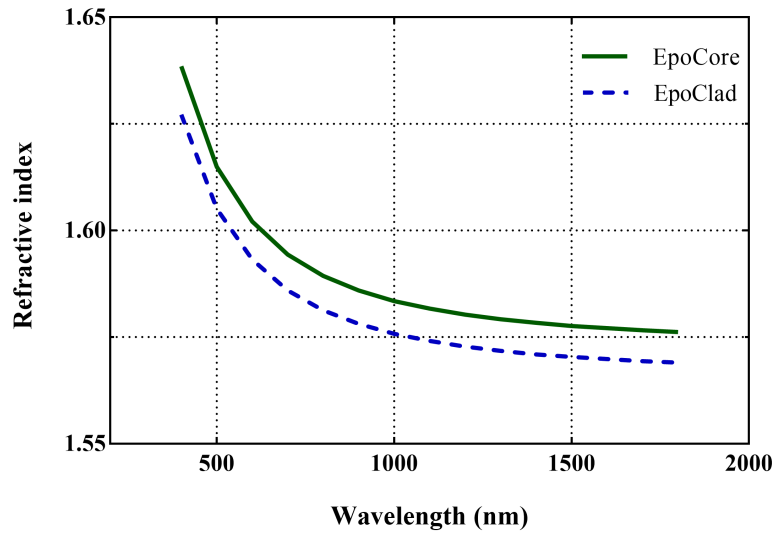


Figure 4.3: The refractive index as a function of the wavelength for EpoCore and EpoClad materials

4.4. Fabrication process flow

The process flow of the waveguide fabrication is illustrated in Fig. 4.5 and is described in detail in this section. The optimized process parameters for the fabricated waveguides using both material systems are also given in table. 4.3.

4.4.1. Substrate preparation

Different types of substrates can be used as the carrier interposer for the polymer materials since polymers exhibit good adhesion and wetting properties on wide range of substrates. In this work, we used silicon as the carrier substrate owing to simple processing, low surface roughness and compatibility with standard semiconductor process. Additionally, cross sections with smooth facets can be easily created for the fabricated waveguides by dicing or cleaving. The silicon substrate is chemically cleaned by rinsing in acetone for 2 minutes, IPA (Isopropyl Alcohol) for 2 minutes and then in DI water for 2 minutes and finally the substrate is dried on a hotplate at $150^{\circ}C$ for 15 minutes.

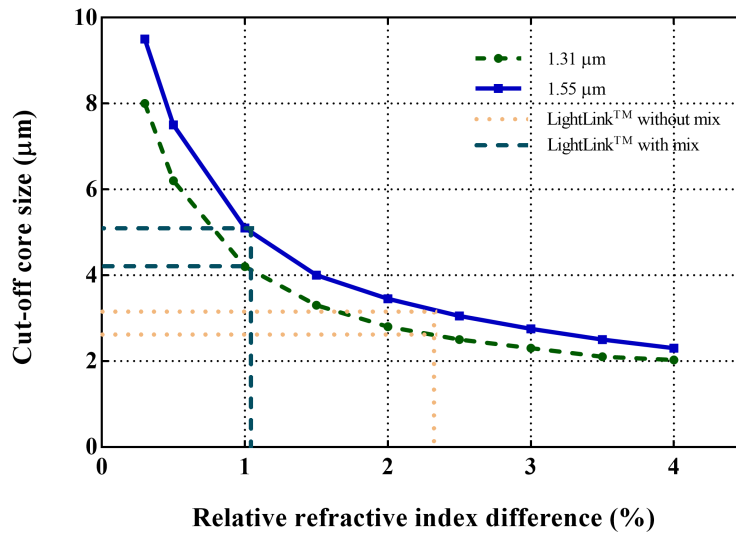


Figure 4.4: The cut-off single-mode core size as a function of the relative index difference. The cut-off core sizes of EpoCore waveguides with a relative index contrast of 0.465 % are 6.2 μm and 7.6 μm at 1.31 μm and 1.55 μm respectively while for LightLink™(with mixing) with a relative index contrast of 1.06 % are 4.2 μm and 5.1 μm at 1.31 μm and 1.55 μm respectively

4.4.2. Spin coating lower cladding

The lower-cladding is applied by means of spin coating where the material is uniformly spread over the complete surface of the substrate to achieve a thickness of 20 μm . The cladding layer is then pre-baked on a hotplate to evaporate the solvents. Next the under-cladding layer is UV cured by flood exposure using mask aligner SET MG1410. Post-exposure bake is then followed in order to complete the photo-reactions and cross-linking initiated during the UV exposure. Finally, hard bake is performed in the convection oven as the final step to provide a thermal stability for the cladding layer and enhance the material adhesion to the substrate.

4.4.3. Core layer definition

The core layer is then spin-coated followed by pre-baking to remove the solvents and reach the full UV-sensitivity. The pre-baked core layer is patterned by direct-write lithography (DWL-66FS from Heidelberg instruments) using a continuous UV laser (Genesis CX STM-Series from Coherent, $\lambda = 355 \text{ nm}$) and then post-baked in order to finalize the cross-

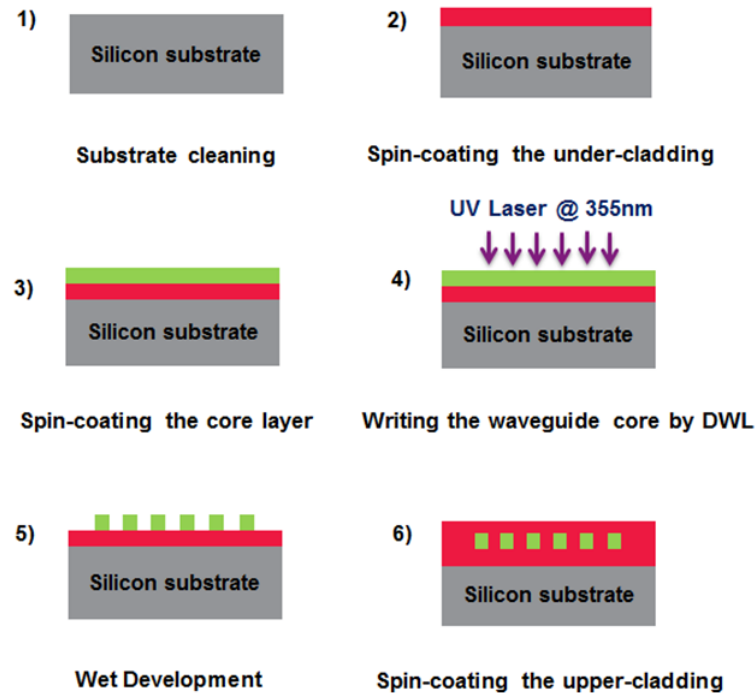


Figure 4.5: The process flow illustrating the most important waveguide fabrication steps

linking initiated during UV-exposure. The core layer is then developed in an appropriate developer to remove the unexposed parts and maintain the exposed structures.

Direct-write lithography (DWL)

Direct-write lithography DWL is a mask-less technique which enables high-resolution direct patterning of photo-sensitive materials. In contrast to the conventional photolithographic technologies and imprinting techniques, DWL does not require expensive masks and the design can be flexibly modified or changed via the CAD software interface integrated with the DWL tool. The structures are directly-written by scanning a UV-laser beam over the surface of the photosensitive material according to the designed pattern. Therefore, it represents a very convenient approach for fast prototyping in research environments, where the designs need to be frequently modified or entirely changed. However, it can not be compared with the photolithographic technologies in terms of the high throughput and the mass production. But, with the continuous improvement in laser technologies, the writing speed increases significantly and consequently the fabrication speed. Moreover, three-dimensional (3D) micro- and nano- fabrication [30, 31] can be

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Table 4.3: A summary of the optimized process parameters for the waveguide fabrication

Process step	Epoxy system		Siloxane system	
	EpoClad	EpoCore	LightLink™ cladding	LightLink™ core
Spin coating	4500 rpm for 60 s → 20 μm	3000 rpm for 30 s → 5 μm	500 rpm for 40 s → 20 μm	4700 rpm for 60 s → 5 μm
Soft bake	5' @ 50 °C then 5' @ 90°C and then 10' @ 120°C	2' @ 50°C then 4' @ 90°C	5' @ 90°C	4' @ 90°C
UV exposure	1' flood exposure at 10 mW/cm ²	DWL patterning at 334 mW/cm ²	2' flood exposure at 10 mW/cm ²	DWL patterning at 240 mW/cm ²
Post exposure bake	15' @ 85°C	2' at 50°C + 4' at 85°C	5' at 90°C	3' @ 90°C
Wet development	-	45'' in mr-Dev 600 then 1' rinse in IPA	-	10'' in xp-3636 LightLink™ developer followed by 1' DI rinse
Hard bake	1 hour @ 120°C	1 hour @ 120°C	1 hour @ 140°C	1 hour @ 140°C

realized using laser-direct writing, which is not possible using standard photo-lithographic techniques. Therefore, the laser-direct writing technologies have been involved in many applications [32–36].

Amongst all the reported single-mode technologies, DWL has been selected in this work as the most promising approach for the waveguide definition. Laser direct writing of polymer waveguides has been widely investigated over the last years [37–39]. In this thesis, we used a laser direct-writing system DWL 66FS (from Heidelberg instruments). The DWL 66fs system installed in UGent cleanroom is shown in Fig. 4.6. This technique is utilized for the waveguide fabrication so that it can provide a precise control over the dimensions and minimize the surface roughness of the patterned single-mode polymer waveguides. In addition, this technique is mask-less and flexible; which allows rapid prototyping in contrast to conventional mask-based photolithographic approaches; in which a mask has to be designed first and fabricated before waveguides can be produced. It can also be used to define very high resolution features (down to 0.6 μm line-width) over comparatively

large planar areas (up to 300 mm x 300 mm). Moreover, this method has the property of adaptive focusing which enables the laser writing head to change the focus adaptively according to the deformations of the substrate. This property is essential in particular while developing waveguides on polymer and hybrid substrates such as printed circuit boards (PCBs). It also has sub-micron alignment accuracy ($\pm 0.25 \mu\text{m}$).

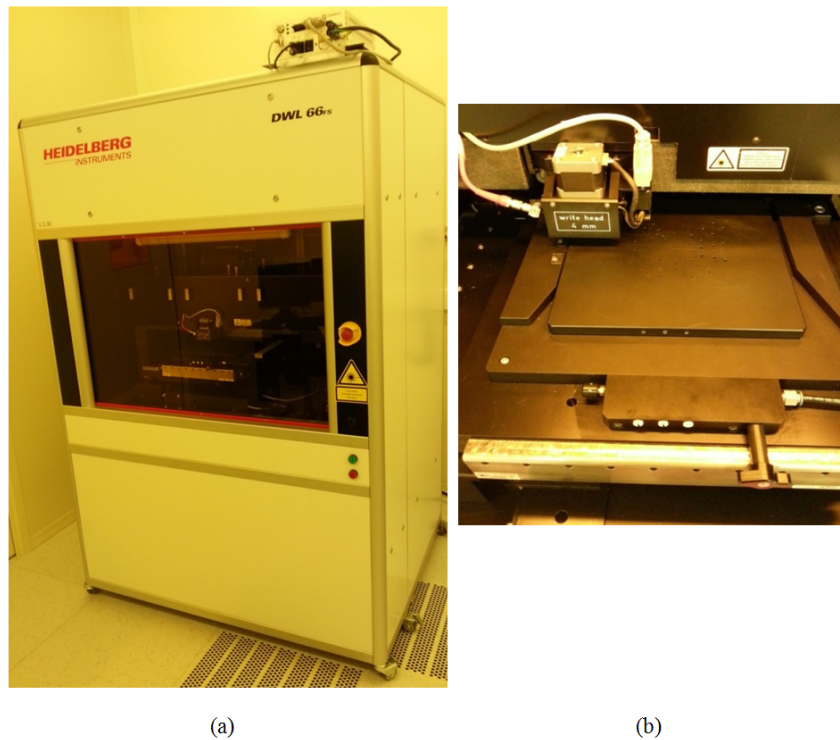


Figure 4.6: (a) The DWL system in UGent-imec cleanroom (b) The DWL system stage

The DWL system uses acoustic-optic modulators (AOM) to adjust the laser intensity, and acoustic-optic deflectors (AOD) to scan the beam as shown in Fig. 4.7. During the exposure, the substrate is fixed on the stage by a vacuum and the stage moves in the x-y plane. Its position is constantly monitored by an interferometer system with a resolution of 10 nm. There are two write heads available with a certain focal length for the DWL system; 4 mm & 40 mm. But in this work, the 4-mm write head is mainly used in order to achieve small features for the single-mode waveguides. The 40-mm write head can define structures with minimum a line width of $10 \mu\text{m}$. But it can write at a speed of $416 \text{ mm}^2/\text{minute}$, which is much higher speed compared to the 4-mm write head ($10 \text{ mm}^2/\text{minute}$). Table 4.4 gives more details of the main features for both the 4 mm and 40 mm write heads. The write head uses an air-gauge to monitor N_2 pressure change, which

Direct-write lithographic (DWL) patterning of single-mode polymer waveguides

then sends a feedback to the lens piezo actuators to perform the auto-focusing. During a scan, the design patterns are divided into stripes along Y-axis, each stripe contains 100 pixels. The stage moves along Y-axis to finish exposing one stripe, then steps in X-axis to start exposing the next stripe. The exposed stripes are then stitched together to form the final pattern.

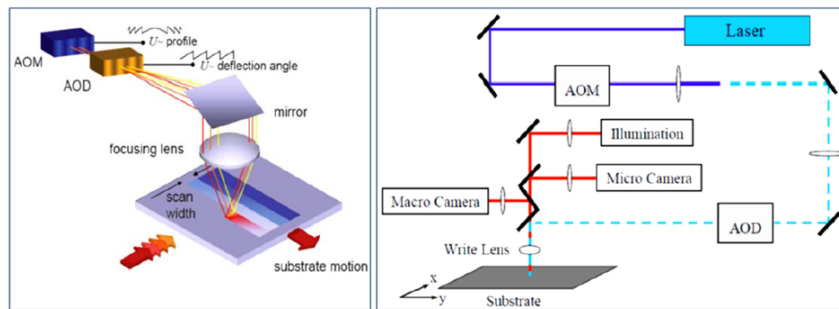


Figure 4.7: DWL writing strategy (source:Heidelberg instruments)

Table 4.4: The main specifications of the 4 mm and 40 mm write heads of DWL system

Parameter	4 mm- write head	40 mm- write head
Address grid (nm)	100 nm	500 nm
Minimum feature size (μm)	0.6 μm	10 μm
Write speed ($\text{mm}^2/\text{minute}$)	10	416
Edge roughness (3σ , nm)	80 nm	280 nm
Critical dimension (CD)		
uniformity (3σ , nm)	100 nm	880 nm
Alignment accuracy (3σ , μm)	$\pm 0.25 \mu\text{m}$	$\pm 2 \mu\text{m}$

Optimization of core materials using DWL

Since the goal is directed towards the fabrication of single-mode waveguides with a width around 5 μm for both LightLink™ and EpoCore materials, the highest resolution DWL write head with the focal length of 4 mm was used in order to achieve the desired width and minimize the roughness of the waveguide structures. The optimum exposure parameters need to be determined in order to precisely achieve the required dimensions for the cut-off single-mode core size. Therefore, the laser writing process was optimized by performing an exposure matrix for the core materials. This matrix is produced by writing test structures with different fluences and focus heights. The outcome of this matrix is the optimum exposure fluence for each material. The effect of the exposure fluence on the waveguide

width for the LightLink™core and EpoCore materials is shown in Fig. 6. The optimum exposure fluence was determined by matching the width of the fabricated waveguide with the original design. When the nominally 5 μm waveguide in the design was considered as a reference, the optimum exposure fluences were found to be 240 mJ/cm² and 334 mJ/cm² for the LightLink™core and EpoCore materials respectively.

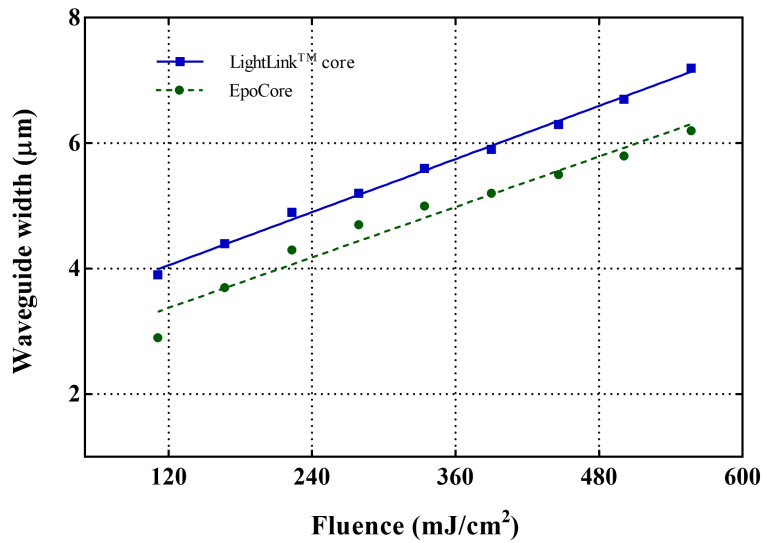


Figure 4.8: The effect of the exposure fluence on the waveguide width (5 μm target width)

4.4.4. Spin coating top cladding

Finally, the upper-cladding is applied with a similar process as for the lower-cladding to form the complete waveguide stack. For the EpoCore materials, air plasma treatment was employed before spin-coating the top cladding (EpoClad) as there was a wettability issue, in which the top cladding layer was shrinking at the edges during soft-bake. Therefore an air plasma-treatment step was necessary to avoid this issue. A final baking step was performed in the convection oven.

4.5. Fabrication results

Fig. 4.9 shows the scanning electron micrographs of the patterned epoxy (EpoCore) and siloxane (LightLink™core) waveguides defined at the optimized parameters. The SEM analysis demonstrates the high surface quality and smooth sidewalls for the patterned

waveguides. Cross-sectional views for the fabricated waveguides are also shown in Fig. 4.10. It is clear that the Epoxy waveguides have a sharp rectangular shape while the siloxane waveguides have a rounded profile. Moreover, non-contact optical profiler measurements (Wyko NT3300) have been performed to quantify the surface roughness of the bottom and top cladding layers as illustrated in Fig 4.11. The RMS roughness values (measured on an area of $0.92 \times 1.2 \text{ mm}^2$) for the EpoClad and LightLink™ cladding were around 3.5 nm and 1.6 nm respectively.

4.6. Characterization of the laser direct written waveguides

The performance of the fabricated optical waveguides is determined by measuring the propagation loss per centimeter (dB/cm). This gives an indication how much the light will be attenuated while propagating through the waveguides. The propagation loss includes the influence from other three different losses; absorption (intrinsic) loss, scattering loss, and radiation loss. The intrinsic absorption loss is a characteristic of the polymer material itself and it is dominated by the vibrational absorption of molecular bonds as explained in section 4.2. The scattering loss is caused by the imperfections and defects introduced during the waveguide fabrication processes and the losses can be reduced by further optimization during the fabrication. The scattering loss are categorized into intrinsic extrinsic loss. The intrinsic loss results from the inhomogeneities and non-uniformities of the material itself. As for the extrinsic loss, it is caused by the impurities such as dust, bubbles, voids and cracks in the polymer waveguides. None of the fabricated waveguides showed visual voids or cracks since the samples are processed under cleanroom conditions to minimize the effect of impurities. The extrinsic scattering loss is also highly influenced by the waveguide surface roughness. The higher the surface roughness, the higher the scattering loss and consequently the propagation loss. As illustrated in section 4.5 the surface roughness of the fabricated waveguides is minimized since the high-resolution DWL system was employed for the definition of the core layers.

4.6.1. Optical measurements setup

Fig. 4.12a shows the optical characterization setup, which is used to measure the propagation losses of the realized single-mode waveguides. Two motorized XYZ stages (Newport) with sub-micron precision mounted on a vibration-isolated workstation were used to control the position of the input and output fibers while the sample was fixed using a vacuum chuck. The X, Y and Z-movements have been done automatically with a remote motion controller. The X & Y axes of the Newport stages have a travel range up to 10 cm, while the Z-axis can travel up to 2.5 cm. A microscope camera (Dino-lite microscope) was used to monitor the position of the input and output optical fibers. Laser diode sources (QDFBLD-1300-10 & QDFBLD-1550-5 from QPhotonics) operating at 1310 nm and 1550 nm respectively were used as the light sources. Temperature controller and a Newport laser

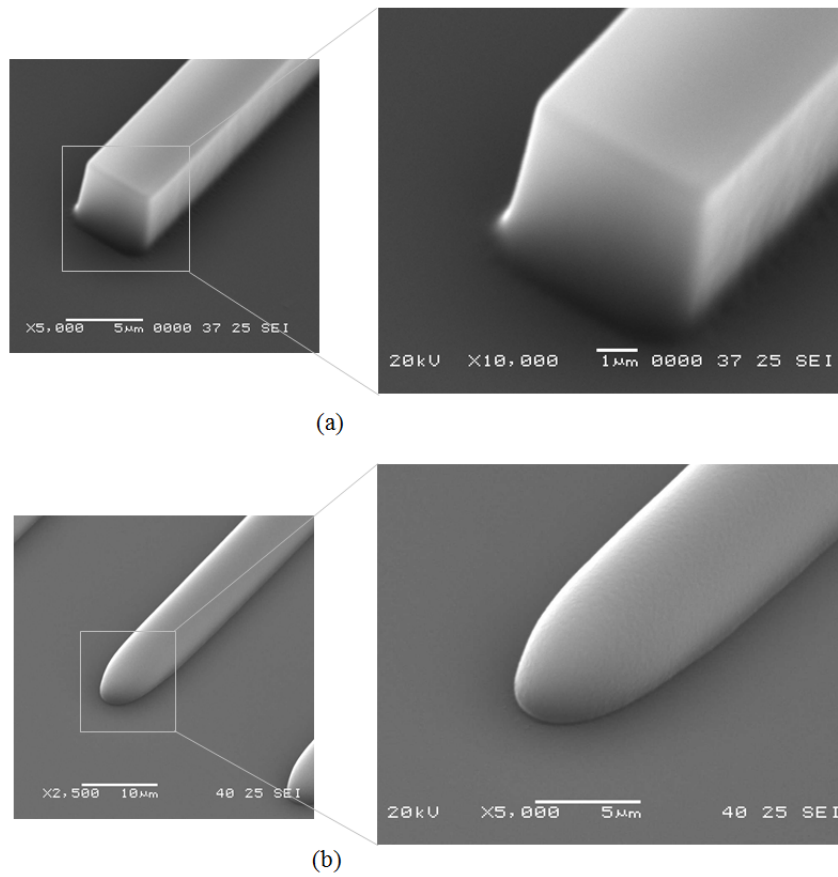
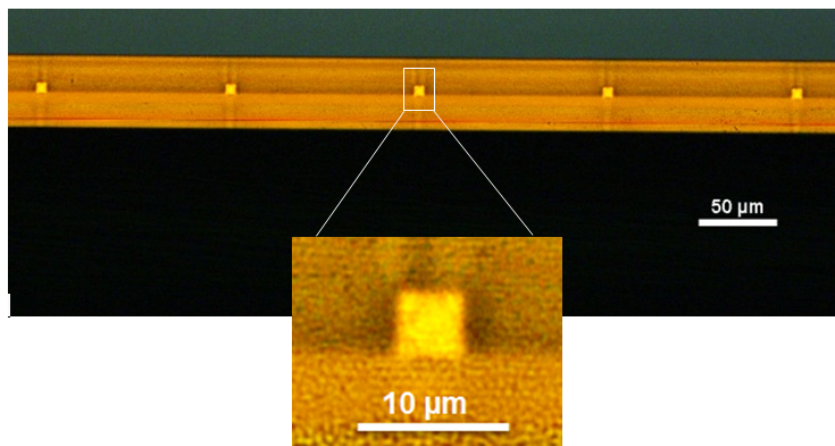


Figure 4.9: Scanning electron microscope (SEM) micrographs of the patterned core by DWL: (a) Epoxy (EpoCore), (b) Siloxane (LightLink™core)



(a)

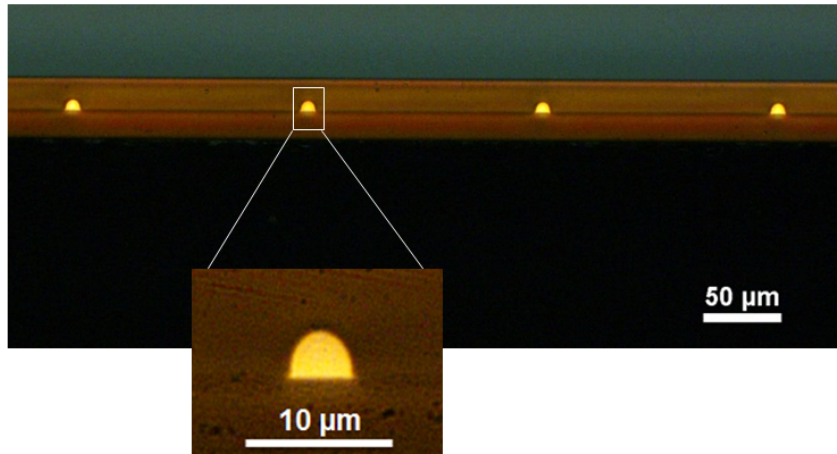
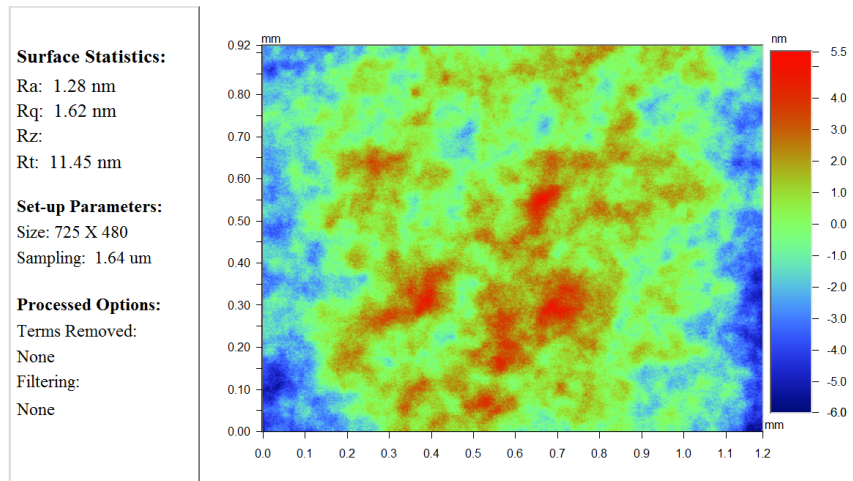
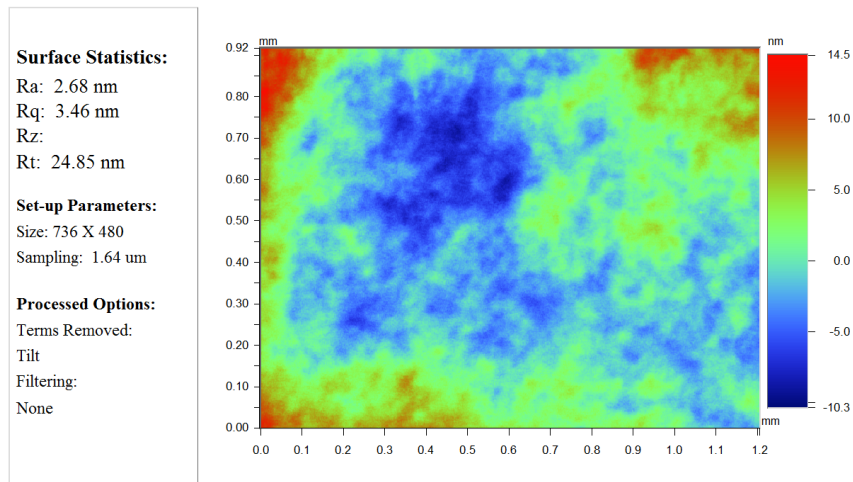


Figure 4.10: Cross-sectional view of the fabricated waveguides: (a) Epoxy (EpoCore), (b) Siloxane (LightLink™core)

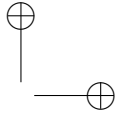
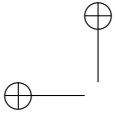


(a)



(b)

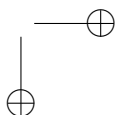
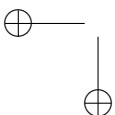
Figure 4.11: Roughness measurements using Wyko optical profiler (a) LightLink™ cladding (b) EpoClad

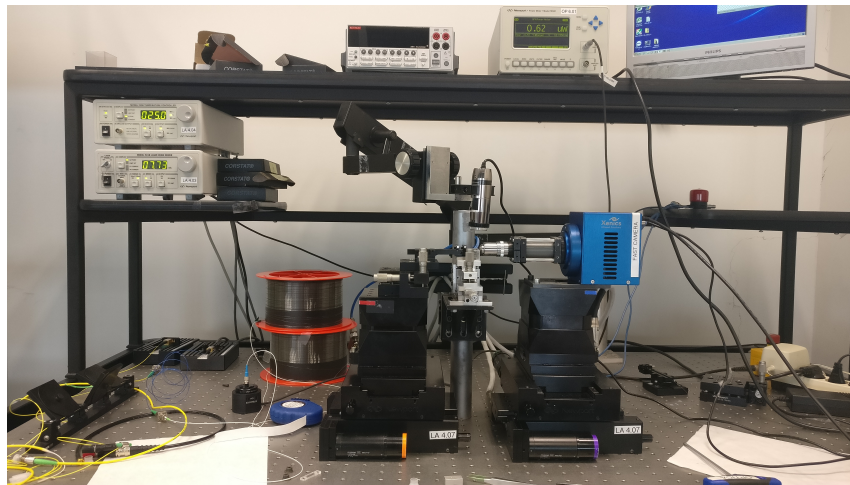


diode driver were interfaced to the laser diode sources in order to control the temperature and the transmitted optical power. The in-coupling optical fiber is connected to the laser source and aligned with the waveguides at one side and the light is coupled out of the waveguides on the other side by the out-coupling, which is then connected to a Newport photodiode and power meter to measure the received optical power. The alignment process is done as follows; the in-coupling fiber is aligned with the in-coupling facet of the waveguide and Xenics IR camera is mounted at the out-coupling side. The input fiber is actively aligned using the XYZ stage remote unit until clear light spot is seen on the IR camera as shown in Fig 4.12c. The input fiber is kept untouched and the IR camera is removed and replaced by the output fiber. Active alignment is performed again for the out-coupling fiber until the highest power was detected by the power meter. Once the two sides were aligned and the power was measured, the connectors were kept untouched. Then the input and output fibers were moved simultaneously by the remote unit (150- μm pitch) to record the optical power for multiple waveguides.

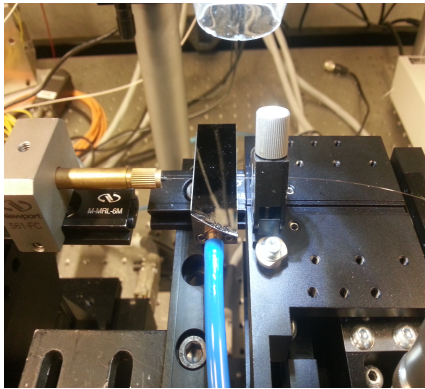
4.6.2. Cut-back measurements

The waveguide propagation losses were determined using the cut-back method. According to the determined single-mode dimensions at wavelengths of 1.31 μm and 1.55 μm , $5 \times 5 \mu\text{m}^2$ epoxy waveguides and $4 \times 4 \mu\text{m}^2$ siloxane waveguides were prepared for the optical characterization measurements. A cleaved standard single-mode fiber (SMF-28 fiber) was aligned at the input and 50/125 μm multimode fiber (numerical aperture 0.2) was mounted at the output side to facilitate light collection. The transmitted optical power was measured both at 1.31 μm and 1.55 μm . A sample with 5 cm-long waveguides was fabricated on a silicon wafer for this loss measurement. The end-facets were created by dicing the sample using a wafer dicer (Disco DAD322) at a translational speed of 1 mm/sec and blade rotational speed of 10000 rpm. The cutback measurements were performed both for the epoxy and siloxane waveguides. For each sample length, 10 waveguides were measured and the average loss was calculated. The fiber-to-fiber transmitted power was set as a reference for the measurements. The graphs corresponding to the cut-back measurements are shown in Fig. 4.13. For the epoxy-based system, the average propagation losses are 0.49 ± 0.07 dB/cm and 2.23 ± 0.05 dB/cm at 1.31 μm and 1.55 μm respectively. For the siloxane-based system, the average propagation losses are 0.34 ± 0.04 dB/cm and 1.36 ± 0.02 dB/cm at 1.31 μm and 1.55 μm respectively. The measurements were performed without using an index matching fluid at the input and output facets of the waveguides. The coupling loss between the optical fiber and the waveguide has a value between 1 to 1.5 dB per facet. This loss is caused by different factors such as reflections (air-polymer), facet roughness, mode field diameter and NA mismatches. The high propagation loss of the fabricated waveguides in particular the epoxy waveguides is mainly attributed to the high material absorption at 1.31 μm and 1.55 μm . The main advantage of the developed technology is the adaptive approach employed in the patterning process using DWL. Other waveguide materials with low absorption (e.g. fluorinated polymers) at 1.31 μm and 1.55 μm and DWL-compatibility could be a promising solution for chip-to-chip optical

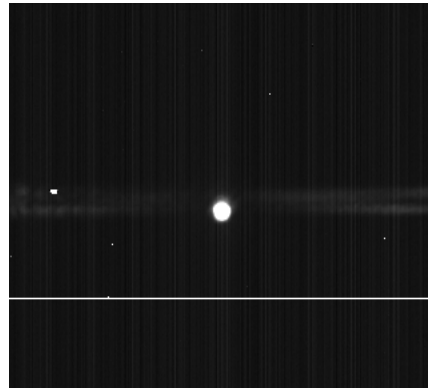




(a)

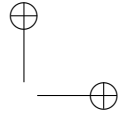
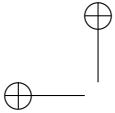


(b)



(c)

Figure 4.12: (a) The optical characterization setup (b) Close-up view on the sample during light coupling (c) IR camera picture of the light coupled in the waveguide

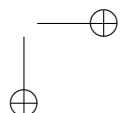
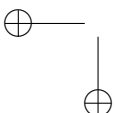


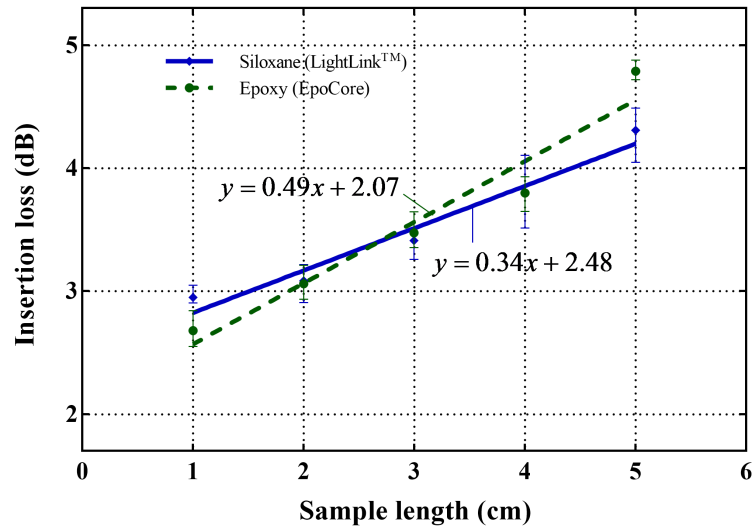
interconnects in datacom applications.

Based on the results above, clear differences can be observed between the epoxy and siloxane based single-mode waveguides. Since the epoxy materials exhibit a higher optical absorption compared to siloxane materials (both at 1.31 μm and 1.55 μm), it was anticipated that the propagation loss of the epoxy-based waveguides is higher. However, there are additional parameters to consider when evaluating the waveguide performance. The roughness of the waveguide sidewalls, for instance also influences the propagation loss. Although a very low roughness was observed for both types of waveguides (since a high resolution direct-write system was employed), intrinsic material differences are involved. EpoCore, which has a similar chemistry compared to SU-8 (also epoxy-based), is a very high resolution resist allowing definition of very fine structures: the shape of the final structures is almost completely defined during UV-illumination and subsequent baking steps virtually do not alter this shape. Therefore, the material is sensitive to leaving rough sidewalls when lower quality UV-patterning would be applied. For the siloxane materials, the degree of polymerization is lower after UV-exposure: during subsequent baking and developing steps reflowing and rounding of the structures is observed. This has a very positive effect on the waveguide smoothness, but makes the fabrication process more sensitive to parameter variations. On the other hand, high resolution resists are needed when reproducible (for example square) waveguide dimensions are required. This is the case when other functional structures such as directional couplers, splitters or ring resonators are needed since they require accurate dimensions and well-defined gaps between waveguides. Using epoxy, a minimum feature size and feature spacing of 600 nm was possible and this was mainly limited by the direct-write lithography system used. Using siloxane, the minimum spacing between adjacent structures was found to be around 12 μm as structures with spacing below 12 μm would start to overlap. In conclusion, if low-loss single-mode waveguides are required without complex routing, siloxane waveguides show better performance; if the optical chip contains more complex optical functionality and propagation loss is less important, the use of epoxy waveguides is more advantageous.

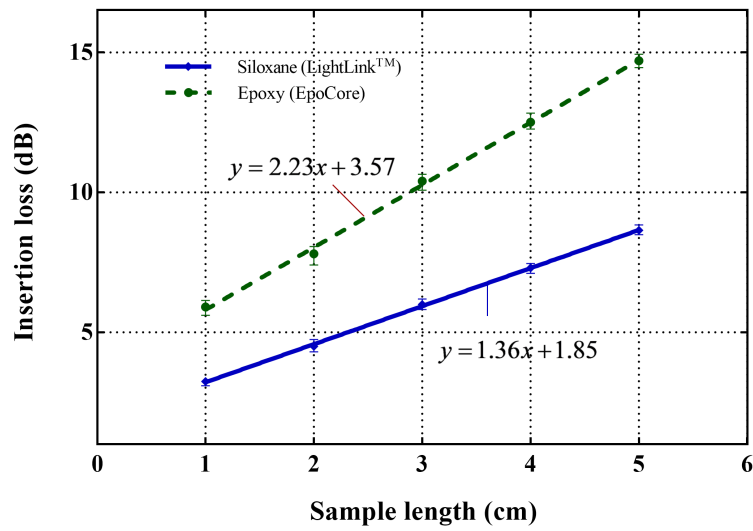
4.7. Polymer waveguide crossings

Realization of complex waveguide structures is essential so that different geometric configurations can be provided to meet the required optical routing functions and layouts for electro-optical printed circuit boards (EO-PCB) [40]. The design of these complex optical interconnections increases routing functionalities, saves area on EO-PCB, minimize link lengths and enable advanced on-board topologies. Waveguide crossings are one example of these structures that can facilitate an optimized routing of the optical waveguide circuitry. Considerable research has been conducted on multimode polymer waveguide crossing over the past years [41–46]. Generally, when a waveguide intersects with another, the propagating light will experience a variation in modal distribution at the crossing intersection and some of the optical power might be coupled to radiation modes and might eventually be lost or cause a crosstalk to the adjacent and crossing waveguides. However, the lost





(a)

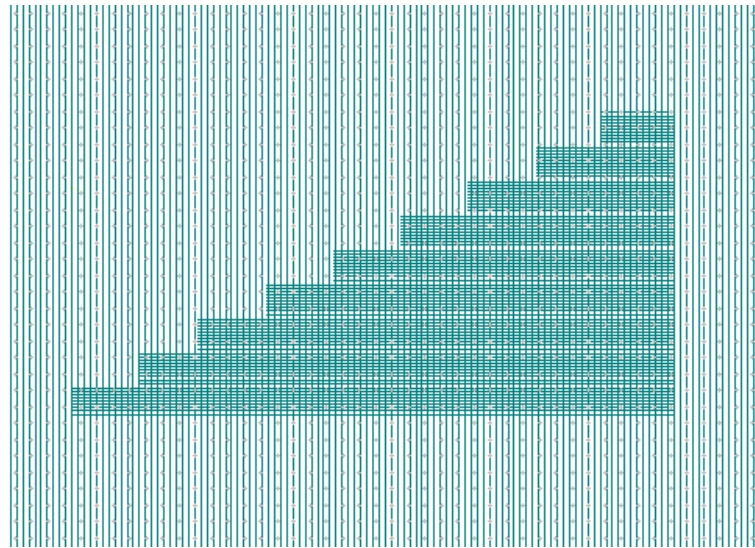


(b)

Figure 4.13: Results of the cut back measurements: (a) Epoxy (EpoCore) and siloxane (LightLink™) waveguides at 1.31 μm; (b) Epoxy (EpoCore) and siloxane (LightLink™) waveguides at 1.55 μm

optical power is not necessarily high particularly for 90° crossings. The optical loss per crossing and the crosstalk depends on the crossing angle between the waveguides [47–49]. The crosstalk induced in the intersecting polymer waveguide crossings is reported to be below the sensitivity of the power meter (-40 dB) at 850 nm [50]. However, it has also been reported that crosstalk in the adjacent parallel waveguides increases while increasing the number of crossings. The worst crosstalk values obtained from the waveguides with 100 crossings were of the order of -25 dB [20]. The reported crosstalk values are claimed to be sufficiently low for on-board interconnections.

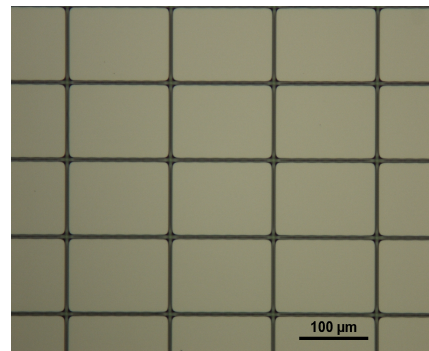
The development of single-mode polymer waveguide crossings is very limited in the literature since most of the investigated research was focused on multimode polymer waveguide crossings. Therefore, in this dissertation, we exploited the flexibility of the high-resolution DWL technique to pattern single-mode polymer waveguide crossings using the two material systems, targeting datacom wavelengths. Fig. 4.14a shows the waveguide crossings schematic CAD design. It consists of 20 mm-long straight waveguides with an increment of 10 crossings every 1.5 mm. The idea is to couple the light in the waveguides where the crossings exist and measure the excess optical loss while increasing the number of crossings. Fig. 4.14b and 4.14c show the fabricated EpoClad/EpoCore LightLink™ crossings. The transmitted power through the straight waveguide without any crossings is set as a reference. Then, the transmitted power through the waveguide crossings were measured while varying the number of crossings between 10 and 80. The excess loss was plotted as a function of the number of crossings. The linear regression of these plotted values yields the loss per crossing. Fig. 4.15 shows the results of the excess optical loss for both types of the waveguide crossings (LightLink™ & EpoCore) at 1.31 μm and 1.55 μm . For the EpoClad/EpoCore system, the average losses per crossing are 0.026 dB/crossing and 0.025 dB/crossing at 1.31 μm and 1.55 μm respectively. For the LightLink™ system, the average losses per crossing are slightly higher, i.e. 0.049 dB/crossing and 0.028 dB/crossing at 1.31 μm and 1.55 μm respectively. This can be explained as the core dimensions at 1.31 μm are closer to multimode behavior (higher index contrast than epoxy) and higher order modes can be excited causing this slightly higher loss.



(a)

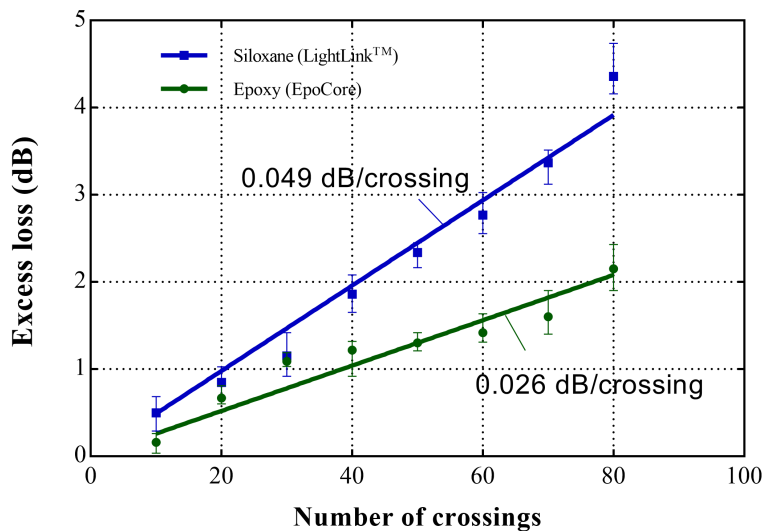


(b)

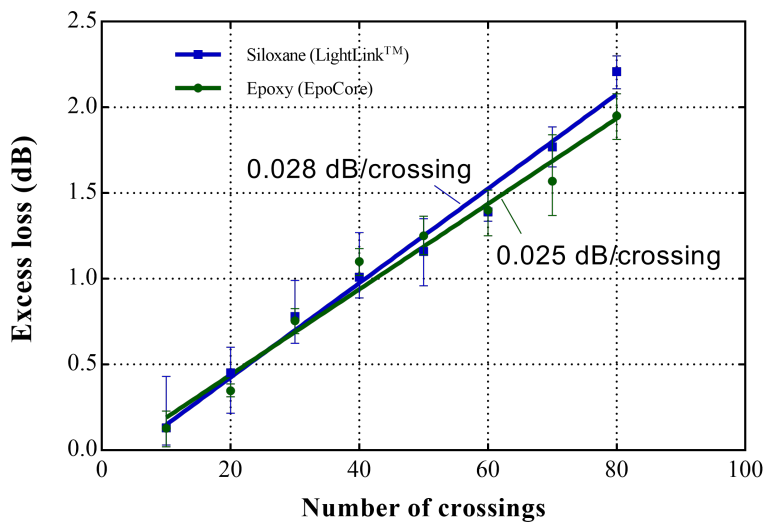


(c)

Figure 4.14: (a) The CAD design of the waveguides crossings (b) the laser-written EpoCore waveguide crossings (c) the laser-written LightLink™ crossings



(a)



(b)

Figure 4.15: Results of the excess loss per crossing (a) Epoxy (EpoCore) and siloxane (LightLink™) waveguides at 1.31 μm; (b) Epoxy (EpoCore) and siloxane (LightLink™) waveguides at 1.55 μm

4.8. Conclusions

In this chapter, we developed single-mode polymer waveguides by direct-write lithography (DWL) method. Two polymer materials including epoxy and siloxane were used for the realization of the optical waveguides. The siloxane material is commercially known as LightLink™ and the epoxy material known as EpoCore/EpoCLad. The refractive indices of those polymer materials were measured by ellipsometry. Based on the refractive index measurements, the single-mode cut-off core size was calculated using a numerical mode solver (Lumerical) for both materials at 1.31 μm and 1.55 μm. The resulting cut-off core sizes for the EpoCore waveguides corresponded to 6.2 μm and 7.6 μm at 1.31 μm and 1.55 μm respectively, while the cut-off core sizes for LightLink™ waveguides corresponded to 5.1 μm and 4.2 μm at 1.31 μm and 1.55 μm respectively.

After determining the waveguide dimensions, the polymer waveguides were fabricated on a silicon substrate. The waveguide stack consists of a lower cladding with a thickness of 20 μm, a core cross section area of 5 x 5 μm² (EpoCore) and 4 x 4 μm² (LightLink™) and a top cladding with a thickness of 20 μm. The core layers were directly patterned by DWL system. The optimum exposure parameters were determined in order to precisely achieve the required dimensions for the cut-off single-mode core size. An exposure matrix is produced for each core material by writing test structures with different fluences and focus heights. The outcome of this matrix is the optimum exposure fluence for each material. The resulting optimum exposure fluences were found to be 240 mJ/cm² and 334 mJ/cm² for the LightLink™ core and EpoCore materials respectively. The fabricated polymer waveguides showed high surface quality and smooth sidewalls.

The developed polymer waveguides were then characterized by measuring the propagation losses. The cut-back method was employed to measure the propagation loss of the polymer waveguides. Sample with 5 cm-long waveguides were prepared on a silicon wafer for this loss measurement. For each sample length (from 5 cm down to 1 cm), 10 waveguides were characterized by measuring the transmitted optical power and the average loss was calculated. For the epoxy-based system, the average propagation losses are 0.49 ± 0.07 dB/cm and 2.23 ± 0.05 dB/cm at 1.31 μm and 1.55 μm respectively. For the siloxane-based system, the average propagation losses are 0.34 ± 0.04 dB/cm and 1.36 ± 0.02 dB/cm at 1.31 μm and 1.55 μm respectively. Moreover, single mode polymer waveguides crossings were developed and the excess optical loss per crossing was measured. For the EpoClad/EpoCore system, the average losses per crossing are 0.026 dB/crossing and 0.025 dB/crossing at 1.31 μm and 1.55 μm respectively. For the LightLink™ system, the average losses per crossing are slightly higher, i.e. 0.049 dB/crossing and 0.028 dB/crossing at 1.31 μm and 1.55 μm respectively.

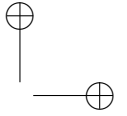
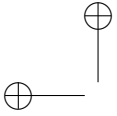
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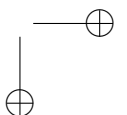
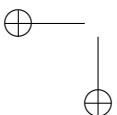


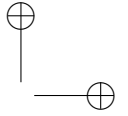
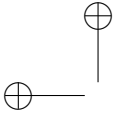
124 **Direct-write lithographic (DWL) patterning of single-mode polymer waveguides**

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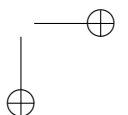
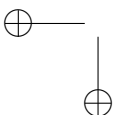
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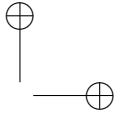
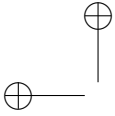
Adiabatic coupling between DWL polymer waveguides and SOI waveguides

In the previous chapter, we focused on the realization of single-mode polymer waveguides using direct-write lithography (DWL). These waveguides can be used for chip-to-chip interconnects and can also be integrated with silicon photonics as spot size converters. In this chapter, we will present an adiabatic coupling approach between SOI waveguides and the developed DWL polymer waveguides. The fabrication process flow will be discussed in detail and the characterization results including the total insertion loss and the adiabatic coupling loss will be presented. The proposed adiabatic solution can also be integrated with the electronic-photonic packaging approach using AJP as discussed in chapter 3. Hence, the electrical interconnects can be realized for the optical chip in case if the SOI chip includes electrical functionalities, which is the case in a real system where the photonics need to integrate with electronics. Therefore, both optical and electrical interconnects can be combined on the same platform.

5.1. Introduction

With the tremendous development in silicon photonics [1, 2], high quality ultra compact photonic integrated circuits (PICs) can be developed with extremely high-precision and yield, leveraging microelectronic CMOS fabrication facilities. One key advantage of SOI platform is the strong optical confinement exploiting the silicon high refractive index, enabling ultimate miniaturization of the photonic chips. However, optical coupling between





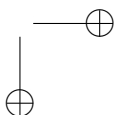
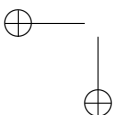
126 **Adiabatic coupling between DWL polymer waveguides and SOI waveguides**

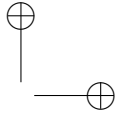
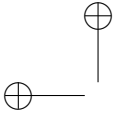
the photonic chips and the outside world is one of the most significant challenges [3, 4] particularly for high-index-contrast silicon-on-insulator (SOI) waveguides because the silicon waveguide has a sub-micron size, consequently there is a huge mismatch between the SOI waveguide mode and the standard optical fiber mode, leading to high coupling loss. Therefore, there has been extensive research on efficient coupling to SOI waveguides. A number of solutions have been proposed [5] for coupling the light between the optical fiber and silicon waveguides. These coupling solutions can be divided into in-plane and out-of-plane, depending on whether the optical fiber is positioned in the same plane with the photonic chip or not. The most common in-plane and out-of-plane couplers are mainly the inverse tapers and diffraction gratings respectively.

The out-of-plane couplers are based on diffraction gratings, in which the propagating light in the waveguide is scattered by the grating. The scattered light is then coupled to an optical fiber placed in the vertical plane; either in a perpendicular position or under an angle (typically around 10°) with respect to the normal of the photonic chip. The grating couplers can also diffract the incident light from an optical fiber (placed under an angle or vertically) in a particular direction (i.e. the propagation direction of the waveguide) depending on the phase matching condition. Several vertical [6–12] and angle-diffracted grating couplers [13–20] have been demonstrated to improve the coupling efficiency out of or into silicon waveguides. Although the out-of-plane couplers can be placed anywhere on the chip without the need of facet polishing and are compatible with wafer-scale optical testing, they are wavelength and polarization-dependent due to the resonant nature of grating couplers.

Therefore, other interesting approaches for in-plane edge couplers have been investigated based on adiabatic coupling between low index waveguides and silicon waveguides. Inverse tapers based couplers was first demonstrated for coupling light between optical fibers and semiconductor lasers [21]. The concept was then applied to couple light between optical fibers and silicon waveguides by using intermediate waveguide with low index contrast as spot-size converters [22–28]. In couplers based on inverse tapers, the light from the optical fiber is first coupled to an intermediate waveguide with a mode size matching that of a standard optical fiber. This requires the intermediate waveguide to possess a lower index contrast (e.g. polymer waveguide) in order to match the mode of the optical fiber. An inverse-taper is then introduced inside the polymer waveguide in which the inverse taper starts with a very narrow width so that the fundamental mode is not coupled to its core but instead it couples to the polymer waveguide since the polymer waveguide mode matches the mode of the optical fiber. The silicon taper starts to gradually widen till the fundamental mode is adiabatically coupled to the silicon waveguide.

Recently, IBM has developed an integration approach based on adiabatic optical coupling between Si waveguides and single-mode polymer waveguides [29]. This approach is shown in Fig 5.1 and can be described as follows: a silicon photonic chip with tapered Si waveguides is flip-chip bonded onto single-mode polymer waveguide processed on a separate carrier as shown Fig. 5.1a. In this case, the cores of the silicon and the polymer waveguides are brought together into a direct physical contact or in a very close proximity as demonstrated in Fig. 5.1b. The reported insertion loss per facet is about 3.5 dB at 1310





nm. The adiabatic coupling approach is based on processing the polymer waveguides directly on the SOI chip. The SOI chip is mounted in a face-up position and then embedded in an epoxy layer. Next, the polymer waveguides are directly patterned using direct-write lithography (DWL).

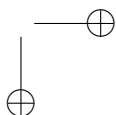
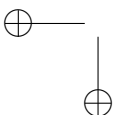
5.2. Adiabatic optical coupling

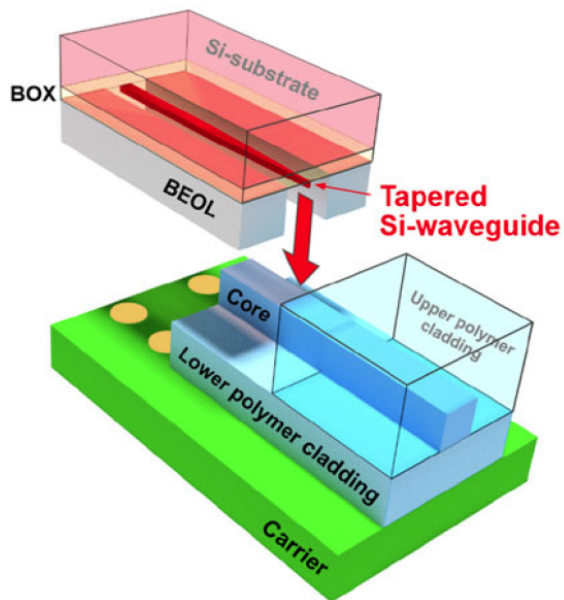
In adiabatic coupling, the geometries of tapered Si waveguide are gradually changed so that the fundamental propagating mode could not transfer the optical power to any higher order or radiation modes. Fig. 5.2a shows the schematic of the adiabatic coupling approach using polymer waveguides as a spot-size converter between SM fibers and Si waveguides. For coupling from an optical fiber to Si waveguides, the optical mode of the optical fiber is almost matched with the mode of the polymer waveguide and hence the light is coupled in the polymer core till the Si taper tip. In the taper, the width is horizontally widened in order to convert the effective index gradually from that of the polymer mode to that of the Si waveguide, resulting in a confined mode in the Si waveguide. The opposite approach occurs during the coupling from Si waveguide to an optical fiber. The inverse taper is gradually narrowed so that the waveguide effective index is reduced by narrowing the Si waveguide width, which results in expanding the mode till it couples to the polymer waveguide and eventually matching the mode of optical fiber. Fig. 5.2b shows the cross section view for the adiabatic coupling approach between polymer waveguides and Si waveguides.

The adiabatic coupling principle has been previously investigated in order to explore the adiabaticity criterion. In order to enable the adiabatic coupling, there is an adiabaticity condition [30] to avoid power transfer from the fundamental mode to the next undesired modes. The adiabatic coupling condition is determined by the following formula for the taper length (L):

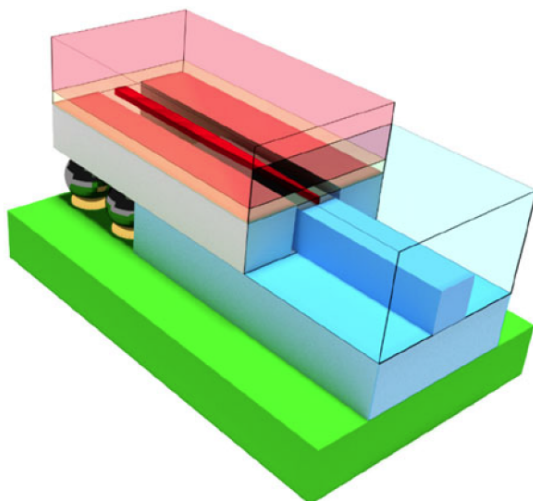
$$L \gg \frac{2\pi}{\beta_1 - \beta_2} \quad (5.1)$$

where β_1 and β_2 are the propagation constants of the fundamental mode and the next local mode (closest mode that the light could couple to) respectively. This condition requires that the taper length should be much larger than the coupling length between the fundamental mode and the next local mode in order to avoid power transfer to higher or radiation modes. Hence, if the adiabaticity condition in eq. 5.1 is satisfied, this will ensure that the fundamental mode will propagate adiabatically with approximately a negligible loss. Otherwise, there will be a significant coupling loss to the second optical mode, leading to a lossy taper. Therefore, the taper dimensions were selected to ensure that the adiabatic coupling condition is satisfied. The design and simulations of the taper and SOI chip used in this work are part of the PhD of Andres Desmet. We used those chips to demonstrate the adiabatic coupling approach based on polymer waveguides as spot size converters. Fig. 5.3 gives the dimensions of the used Si taper. The taper has a length of 1.5 mm and the taper



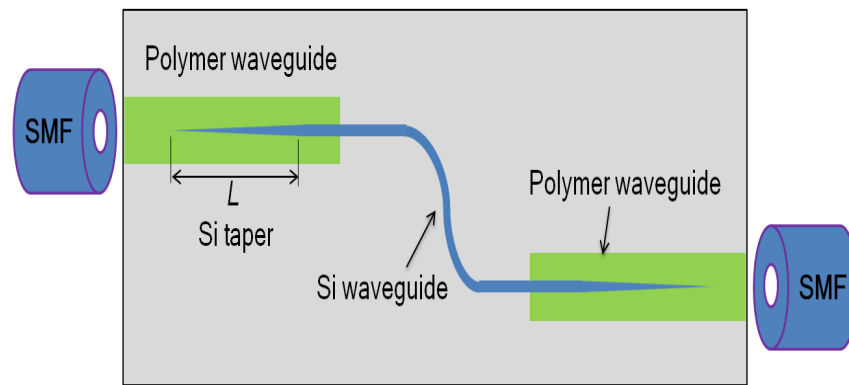


(a)

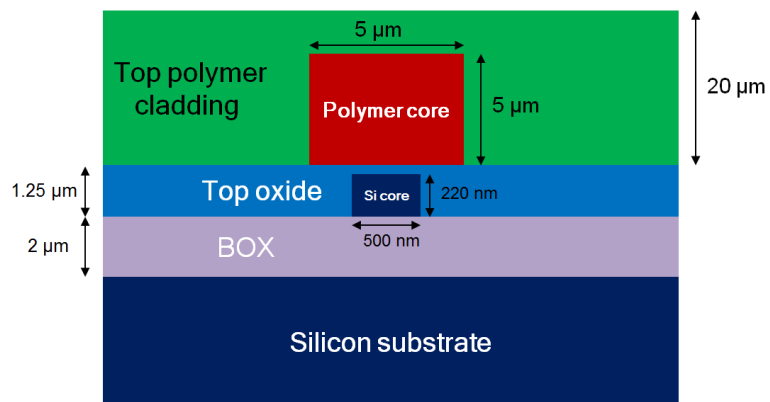


(b)

Figure 5.1: IBM adiabatic coupling approach (a) flip-chip bonding of Si-photonics chip onto PWG on carrier (b) physical contact between the tapered SiWG and PWG enables adiabatic optical coupling [29]



(a)



(b)

Figure 5.2: The schematic of the adiabatic coupling approach (a) top view (b) cross section view

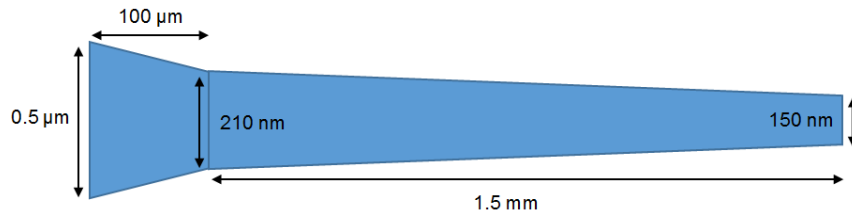


Figure 5.3: Schematic illustrating the dimensions of the Si taper

width gradually varies from 210 nm to 150 nm over the length. While, the Si waveguide has a width of 0.5 μm and height of 220 nm.

5.3. Fabrication process flow

In order to experimentally realize the adiabatic coupling approach, we process the polymer waveguides on the same SOI chip after embedding SOI chip in an epoxy layer. The fabrication process flow for the adiabatic coupling approach is shown in Fig. 5.4. The goal is to embed the SOI chip in a flat epoxy surface so that polymer waveguides can be directly defined by direct-write lithography (DWL). The process flow is described as follows; the SOI chip is attached in a flipped position to a PDMS stamp (50 μm PDMS layer residing on a borosilicate glass). An epoxy polymer (Epotek OG142-112) is then dispensed on the back side of the SOI chip. The epoxy will flow at the sides of SOI chip but will not reach the top surface of the SOI chip since the top side is protected by the PDMS layer. Another borosilicate glass substrate is pressed onto the dispensed polymer to create a flat uniform surface. Next, the polymer is cured using a UV lamp at 30 mW/cm^2 for 2 minutes by illuminating from the backside of the glass substrate. The PDMS stamp is then removed after UV exposure since the epoxy does not adhere to PDMS. In this case, the SOI chip is embedded in an epoxy layer with a flat surface which has the same thickness or slightly higher as the SOI chip. By following the DWL fabrication process illustrated in chapter 4, single-mode polymer waveguides are directly patterned on the SOI chip embedded in the epoxy layer. First, an EpoCore layer with a thickness of about 5 μm was spun on the sample after treating the surface with oxygen plasma to ensure good wettability and adhesion properties and hence create a uniform polymer core layer. The EpoCore layer is then directly exposed by DWL. The core layer in this case is required to be aligned with respect to the Si waveguide. Next, an EpoCLad layer with a thickness of 20 μm is applied on top of the core layer. The requirement of creating a flat epoxy surface is essential particularly at the edges of the SOI chip so that polymer waveguides can cross through the edge of the SOI chip without having any cuts or interruptions in the waveguide structures. The epoxy can also behave in this case as an under-cladding for the EpoCore waveguides. In this approach, the single-mode polymer waveguides are extended from the PIC till the package and they act as an optical fanout.

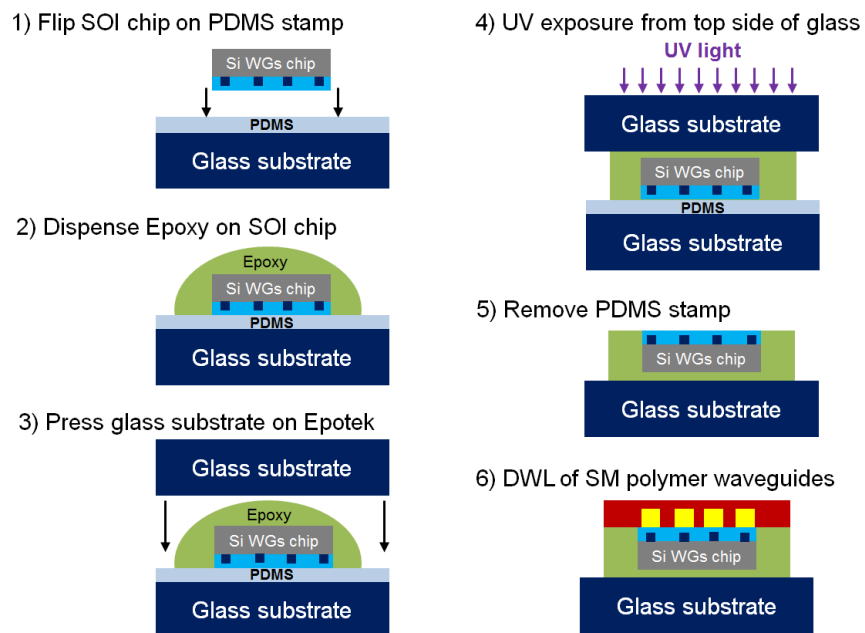


Figure 5.4: Fabrication process flow for the adiabatic coupling approach

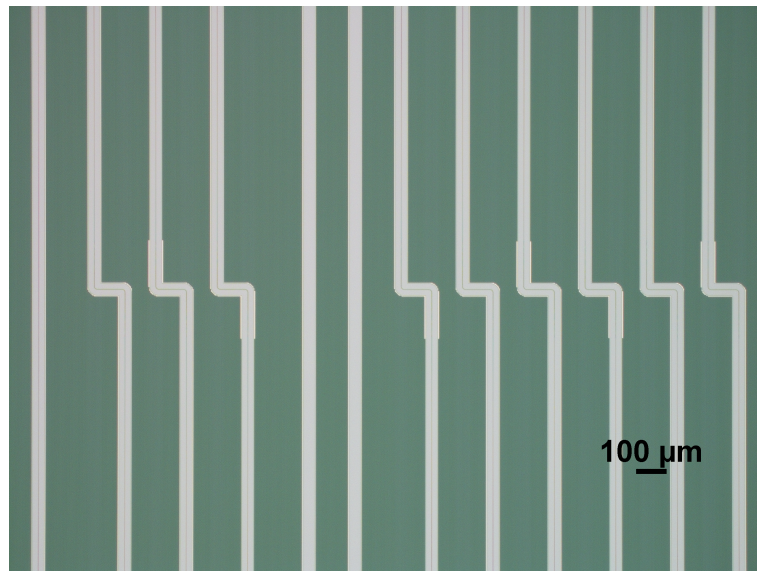


Figure 5.5: A microscope picture of the SOI chip

5.4. Fabrication results

The SOI chip used in this work to demonstrate the adiabatic coupling between polymer and Si waveguides is shown in Fig. 5.5. It includes S-bends Si waveguides with a length of about 4 mm. The Si waveguides are defined in a region in which the silicon is etched. This region has a width of $50\ \mu\text{m}$ and the whole area around is covered with silicon and there is a distance of about 500 nm between the beginning of the region and the start of the Si waveguides. Therefore, the polymer waveguides cannot be longer than the region length as the light will leak to the silicon outside the region boundaries. In this case the length of the polymer waveguides will be about 4 mm. The polymer waveguides were directly patterned by DWL at both sides of the Si waveguides so that the light can be coupled in and out of the Si waveguides. Fig. 5.6 shows the laser direct written polymer waveguides at both sides of the S-bend Si waveguides. In general, the DWL can pattern structures with a high alignment accuracy of about $\pm 0.25\ \mu\text{m}$. However, in some cases if the write-head is dismantled and assembled back, this will result in an offset which needs to be compensated in order to perform the alignment process correctly. The fabricated polymer waveguides have a width of $6\ \mu\text{m}$ and a thickness of $5.6\ \mu\text{m}$. An offset of $2\ \mu\text{m}$ was observed in the lateral direction of the DWL polymer waveguides with respect to the SOI waveguides. On the same SOI chip there were empty straight stripes where there were no Si waveguides. These stripes were utilized to pattern straight waveguides in order to provide a reference for the adiabatically coupled waveguides as shown in Fig. 5.6.

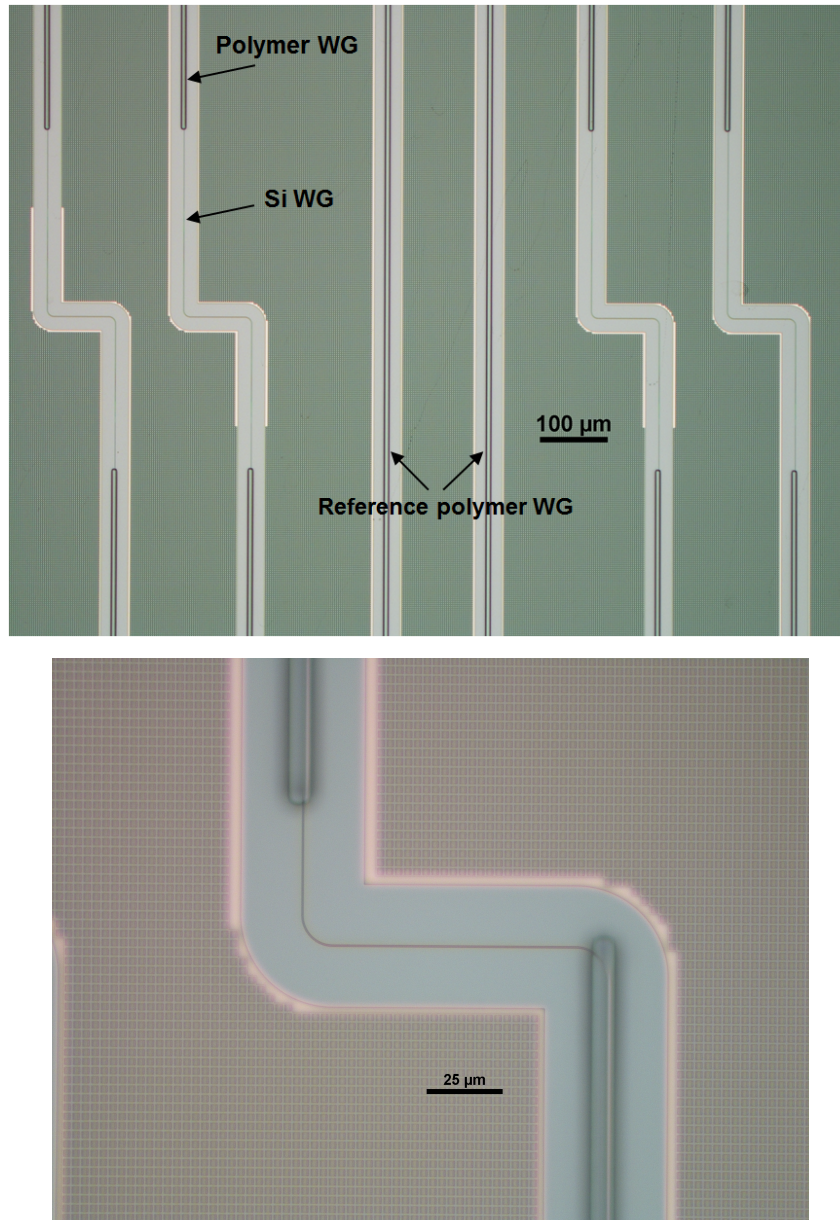
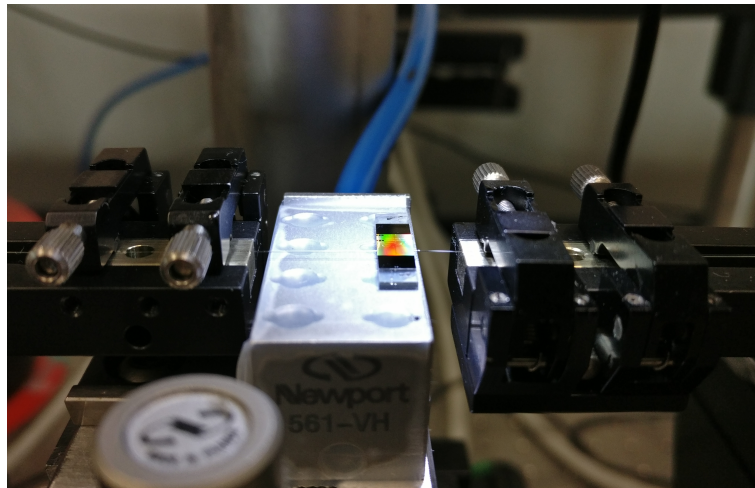


Figure 5.6: Laser direct written polymer waveguides on the Si waveguides

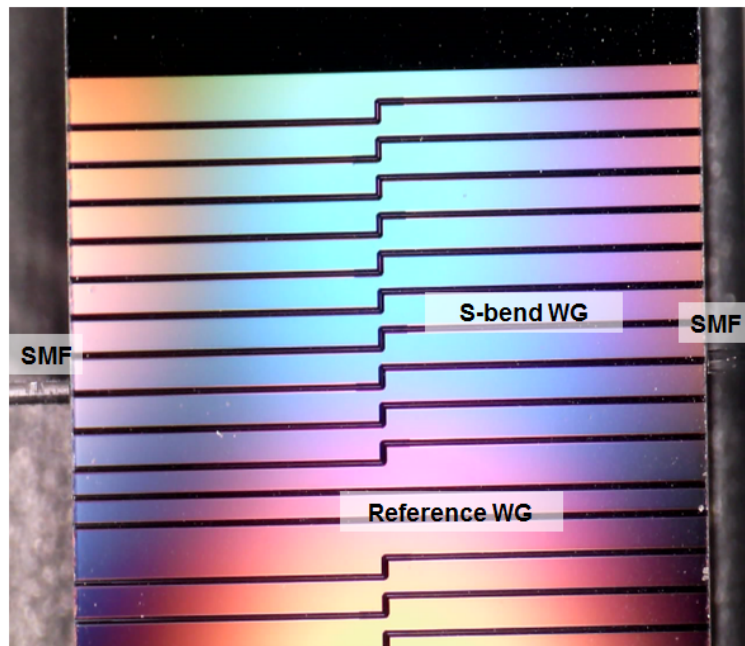
5.5. Characterization results

The facets of the fabricated samples were created by mechanical dicing using a blade dedicated for glass substrates since the SOI chip is embedded in polymer and residing on a glass substrate. The samples were diced at a feed speed of 1 mm/s and blade rotation speed of 10000 rpm. A sample with a length of 4 mm was prepared for the loss measurements. The sample is mounted on the vacuum chuck. Laser diode sources (QDFBLD-1300-10 & QDFBLD-1550-5 from QPhotonics) operating at 1310 nm and 1550 nm respectively were used as the light sources. The light is coupled from a standard single-mode fiber (SMF-28) at 1310 nm and 1550 nm to the polymer waveguides from one side and the light is captured by Xenics IR camera at the out-coupling side. Fig. 5.8a shows the IR camera picture of the coupled light in the reference polymer waveguide (PWG), while fig. 5.8b shows the IR picture of the adiabatically coupled light from the PWG to SiWG then to PWG again. We can see that the IR profile for the reference PWG has a very clear light spot with a minimal scattered light around the waveguide core. For the IR picture of the adiabatically coupled light from the in-coupling PWG to the SiWG then to out-coupling PWG, there is a scattered light next to the detected light spot due to the uncoupled light in the S-bend and it propagates in the cladding layer instead. The region where light scatters is the 100 μm -spacing between the two branches of the S-bend. Once the in-coupling fiber is aligned, the IR camera is replaced with the out-coupling fiber. An index matching liquid was used at the waveguide end facets in order to minimize the coupling loss. The fiber-to-fiber transmitted power was set as a reference for the insertion loss measurements. We measured the total insertion loss (SMF-PWG-SiWG-PWG-SMF) both at 1310 nm and 1550 nm. Table 5.1 gives a summary of the measurement results. The total insertion loss was found to be 9.2 dB and 9.6 dB at 1310 nm and 1550 nm respectively. Hence, the insertion loss per facet corresponds to 4.6 dB and 4.8 dB at 1310 nm and 1550 nm respectively. For the 4 mm-long reference polymer waveguides, an insertion loss of 2.7 dB and 3 dB was measured at 1310 nm and 1550 nm respectively. As presented in 4, the propagation loss of the EpoCore waveguides is about 2.2 dB/cm. The standard SOI waveguide loss developed by photonics research group (PRG-UGent-imec) is found to be about 2.7 dB/cm at 1550 nm [31]. If we also assume that the propagation length of the straight PWG and the (PWG-SiWG-PWG) S-bend is almost the same, we can deduce that the propagation loss in the (PWG-SiWG-PWG) S-bend is approximately the same as in the reference PWG. Therefore, if we subtract the insertion loss of the reference PWG from the total insertion loss (SMF-PWG-SiWG-PWG-SMF), this corresponds to the total adiabatic coupling loss (2 facets). The total adiabatic coupling loss (PWG-SiWG-PWG) in this case is 6.5 dB and 6.6 dB at 1310 nm and 1550 nm respectively. Hence, the adiabatic coupling loss per facet (PWG-SiWG or SiWG-to-PWG) corresponds to 3.25 dB and 3.3 dB at 1310 nm and 1550 nm respectively.

Despite the previous results, we believe that there is still some room for optimization. The resulting adiabatic coupling loss can be further reduced by tuning the dimensions of the polymer waveguide to achieve higher optical coupling. Additionally, the influence of the alignment accuracy between the DWL polymer waveguides and SOI waveguides



(a)



(b)

Figure 5.7: (a) a picture of the sample on the measurement setup (b) a microscope picture of the sample during the measurement process

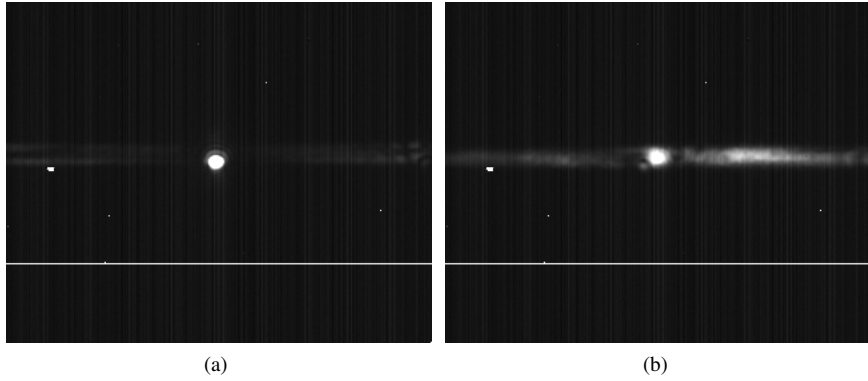
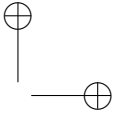
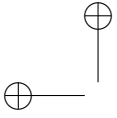


Figure 5.8: IR camera pictures (a) the reference polymer waveguide (b) the adiabatic coupling (PWG to Si WG to PWG)

can be further investigated. We believe that the alignment accuracy of the DWL polymer waveguides can still be improved by compensating the offset in the lateral direction. However, it has been reported that an additional optical loss due to an offset of $2\ \mu\text{m}$ is limited to about 1 dB [29]. Furthermore, the taper design can be further optimized by determining the optimum taper dimensions to suit the adiabatic coupling approach using polymer waveguides as spot size converters. In this case, the effective refractive indices of the used polymer waveguide materials will be considered in the taper design simulations to ensure high coupling efficiency between polymer and SOI waveguides.

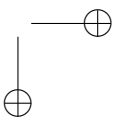
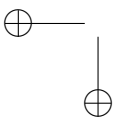
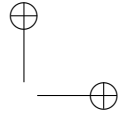
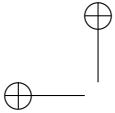


Table 5.1: A summary of the measurement results for the adiabatic coupling between polymer and Si waveguides

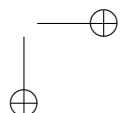
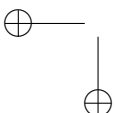
Type of optical loss	Optical loss at 1310 nm	Optical loss at 1550 nm
Fiber-to-fiber total insertion loss (SMF-PWG-SiWG-PWG-SMF)	9.2 dB	9.6 dB
Insertion loss per facet (SMF-PWG-SiWG)	4.6 dB	4.8 dB
Insertion loss (reference straight PWG)	2.7 dB	3 dB
Total adiabatic coupling (PWG-SiWG-PWG)	6.5 dB	6.6 dB
Adiabatic coupling loss per facet (PWG-SiWG or SiWG-PWG)	3.25 dB	3.3 dB



5.6. Conclusions

In this chapter we presented an adiabatic coupling approach to couple the light between polymer and Si waveguides. The adiabatic coupling approach has the advantage of being wavelength and polarization tolerant unlike other approaches which are based on surface grating couplers (wavelength and polarization sensitive). The proposed approach is based on matching the mode of the optical fiber with the mode of the Si waveguide by using polymer waveguides as low index waveguide which match the mode of standard optical fibers. This also requires introducing an inverse Si taper before the beginning of the Si waveguide in order to gradually match the propagating mode in the polymer waveguide with the mode of the Si waveguide. Polymer waveguides with cross section area of $6\ \mu\text{m} \times 5.6\ \mu\text{m}$ were aligned with respect to the Si waveguides and directly patterned using direct-write lithography as discussed in the previous chapter. The insertion loss per facet was measured to be 4.6 dB and 4.8 dB at 1310 nm and 1550 nm respectively. The adiabatic coupling loss between the polymer waveguide and the Si waveguide is found to be about 3.25 dB and 3.3 dB at 1310 nm 1550 nm respectively. The insertion loss can be further improved by tuning the dimensions of the polymer waveguides, improving the alignment accuracy, and optimizing the taper design for higher optical coupling.

This approach is also compatible with the electro-photonics integration using aerosol-jet printing presented in chapter 3. First, the optical and electronic chips will need to be embedded in an epoxy layer as discussed in the previous process flow. The polymer waveguides are then directly defined on the optical chip to act as spot size converter based on adiabatic coupling. If the optical chips include electrical functionalities, the aerosol-jet printing is then used to interconnect the electronic ICs and the optical chips after opening vias for the contact pads on both optical and electronic chip. Therefore, it is possible to combine both electrical interconnects and polymer waveguides on the same platform.



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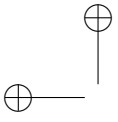
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Adiabatic coupling between DWL polymer waveguides and SOI waveguides

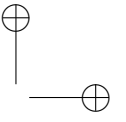
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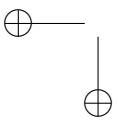


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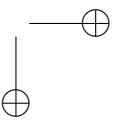


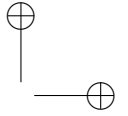
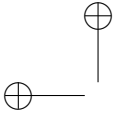
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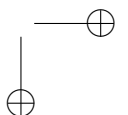
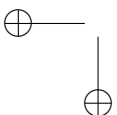
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Conclusions and future work

6.1. Main achievements

Throughout this dissertation, different technologies were described to enable flexible hybrid integration of photonic and electronic chips. This dissertation focused on two key objectives to develop a flexible electronic-photonic integration platform. The first objective of this work is to develop a flexible interconnection scheme between photonic and electronic ICs in order to find a potential alternative to replace the conventional bond wires that cause high parasitic inductance at high frequencies. In this aspect, we explored the aerosol-jet printing as key technology to develop high-speed electrical interconnects. With the capabilities of the AJP technology, electrical interconnects and transmission lines with controlled dimensions and characteristic impedance are successfully printed. Hence, this can provide better impedance matching and lower signal reflections and attenuation at high frequency compared to wire bonding technology.

In order to achieve this objective, several silver nano-particle inks were experimentally tested with the AJP in order to determine the best performing ink. Based on the experimental results, one ink (Novacentrix Metalon 030AE1) is selected and further experiments were undergone to optimize the process parameters and provide a good control over the dimensions for the printed interconnects. It was found that the geometry of the AJP interconnects highly depend on the focusing ratio, which is the ratio between the sheath flow rate and the carrier flow rate. The higher the focusing ratio, the lower the line width and the higher the thickness and vice versa. The printing speed also determines the dimensions of the printed structures. The width and the thickness of the printed lines are inversely proportional to the printing speed. The thickness can also be increased by applying multiple printing



passes till the desired thickness is obtained. Two different sintering methods including thermal and laser sintering were also investigated for the printed silver interconnects. Next, coplanar waveguide transmission lines were printed on glass and epoxy substrates in order to study the electro-magnetic behavior of the printed interconnects. The RF performance of the printed transmission lines is investigated by measuring the scattering parameters (S-parameters) including transmission and reflection coefficients. The measured S-parameters are in agreement with the simulation results performed using ADS software from Keysight technologies. The printed CPWs on glass and epoxy showed an attenuation of 0.57 dB/mm and 0.76 dB/mm at 50 GHz respectively.

The research is then directed towards the application of the AJP technology in the assembly process of photonic and electronic ICs. However, applying a printing technology like AJP in the assembly of photonic chips can be very challenging particularly if the PICs are placed face-up. Typically, PICs have light coupling locations such as surface grating couplers and any misalignment or process variations during printing can result in covering these locations with printed materials (e.g. silver ink) and eventually causing PICs malfunction. Therefore, the printing process was properly optimized to suit this application. A process flow for electronic-photonic interconnection was developed, primarily to create a transparent dielectric support between PIC and EIC so that the electrical interconnects can be printed on top afterwards. In this case the PIC and EIC are somehow embedded in this dielectric support and the thickness of the transparent epoxy layer above the chips should not be large in order to facilitate opening vias for the contact pads and to provide an efficient light coupling into and out of the photonic chips. The proof of concept of the AJP interconnection was proven first on daisy-chain test chips. Additionally, 85°C/85% RH reliability test was performed on the test chips to investigate the functionality of the AJP interconnects under different environment conditions. The AJP printed interconnects showed no failure or degradation even after running 85°C/85 RH tests for 700 hours.

Afterwards the AJP interconnection was applied on functional chips. Three different optical transmitters were successfully demonstrated at high-speed. The first demonstrator represents a 4-channel VCSEL transmitter which consists of 4 long-wavelength VCSELs and 4-channel BiCMOS electronic driver. This optical transmitter was demonstrated at 50 Gb/s. The second optical transmitter consists of electro-absorption modulator (EAM) and CMOS driver. Clear open eye diagrams were obtained at 56 Gb/s even after a transmission distance up to 2 km of SSMF. The third optical transmitter is based on microring modulator and CMOS driver and it was successfully demonstrated up to 60 Gb/s and clear open eye diagrams were also obtained at 60 Gb/s after a transmission distance up to 2 km of SSMF. Furthermore, a direct comparison between the AJP interconnection and the traditional Al bondwires was also demonstrated. The measured reflection coefficient (S_{11}) of the AJP interconnects showed an increase in resonance frequency of 20 GHz compared to Al bond wires. This indicates that AJP interconnects have less parasitic inductance than the bondwire. Additionally, the optical transmission coefficient (S_{21}) of AJP interconnect showed 4 dB higher transmission than the wire interconnect at 50 GHz. From this comparison, a circuit model for the AJP interconnect was fitted so that it can be included in the circuit simulations phase in order to predict the behavior and to improve

the circuit design in advance.

The second key objective is developing a technology to fabricate single-mode polymer waveguides using direct-write lithography. Two commercially-available optical materials including epoxy (EpoCore/EpoClad) and siloxane (LigthLink™) have been utilized to realize the polymer waveguides. The refractive index of the core and cladding materials were measured by spectroscopic ellipsometry. The cut-off core size was then calculated using Lumerical (mode solutions) to ensure the single mode operation at a wavelength of 1.31 μm and 1.55 μm . A process flow for the waveguide fabrication has been developed to realize the waveguides on silicon substrates. The laser direct writing process was optimized for both core materials in order to accurately control the waveguide core size, thus ensuring single-mode operations. The optimum exposure parameters including fluence and defocusing were determined for both core materials. The fabricated polymer waveguides showed high surface quality and smooth sidewalls. Then, 5 cm-long waveguide samples with cross section area of about $5 \times 5 \mu\text{m}^2$ were prepared for the characterization process. The propagation losses were measured using the cut-back method. For the epoxy-based system, the propagation losses are 0.49 ± 0.07 dB/cm and 2.23 ± 0.05 dB/cm at 1.31 μm and 1.55 μm respectively. For the siloxane-based system, the average propagation losses are 0.34 ± 0.04 dB/cm and 1.36 ± 0.02 dB/cm at 1.31 μm and 1.55 μm respectively. Afterwards, the realized DWL polymer waveguides were integrated with silicon photonics. As known, coupling light to SOI waveguides can be very challenging due to the large mode mismatch between SSMF and Si waveguides. Hence, the polymer waveguides were used as spot size converter between SSMF and SOI waveguides based on adiabatic optical coupling. The SSMF mode in this case matches the mode of the polymer waveguide and the mode is then gradually transferred to the Si inverted taper which is introduced inside the polymer waveguide. In this context, a process flow was developed to realize the adiabatic coupling by processing the DWL polymer waveguides on the same SOI chip after embedding SOI chip in an epoxy layer. This required that the DWL polymer waveguide were accurately aligned to the SOI waveguides. The adiabatic coupling approach was successfully demonstrated and the insertion loss per facet was measured and found to be 4.6 dB and 4.8 dB at 1310 nm and 1550 nm respectively.

6.2. Outlook and future perspectives

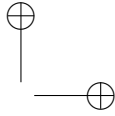
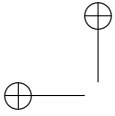
Throughout this thesis, we have developed a flexible technology platform for electronic-photonics integration by realizing both electrical and optical interconnects. However, there are still some aspects that can be further optimized in order to improve the system performance. For the AJP electrical interconnects introduced in chapter 2, we used nanoflakes silver ink as a material for the printed interconnects. However, the conductivity can be further improved by using nanoparticle silver inks with higher metal content. Optimization of the sintering process can also increase the conductivity of the AJP interconnects. Although, laser sintering was not successful with the novacentrix ink due to the relatively large nanoflake size (average size of about 140 nm), it can have a significant effect on

nanoparticle inks which have a typical particle size between $\sim 10\text{-}100$ nm. However, a combination of laser and thermal sintering could be investigated in order to achieve the maximum possible conductivity for the printed interconnects. From an economic perspective, potential copper inks could be used to decrease the overall cost. Moreover, other dielectric materials with low dielectric constant (k) can be used instead of the epoxy material (Epotek OG142-112) utilized in this work, thus improving the RF performance of the printed interconnects and transmission lines. For example, one potential material could be PTFE (Polytetrafluoroethylene) which has a relatively low dielectric constant of 2.2.

In the current process for the AJP interconnection introduced in chapter 3, the dielectric material covering the gap between the photonic and electronic ICs was applied by manual dispensing using a fine needle. However, the dielectric polymer material can be printed by AJP. There are already some polymer materials such as SU-8 and polyimide which are compatible with AJP technology and it has been already reported in the literature to use AJP for printing polyimide material for multilayer transmission lines. In this case, the dielectric material will be only deposited at the required locations (i.e. only between PIC & EIC) without the need of covering the whole chips with the dielectric material. As a result, the laser drilling step for opening vias will not be required since there is not polymer covering the contact pads. For the AJP system with full features, there is a dual deposition system and a UV laser attached to the deposition head for local sintering. In this case, one deposition system is dedicated for metallic conductive inks and the other is for dielectric materials. The process sequence will be as follows; (i) the polymer material is printed using the dielectric deposition system (ii) the UV laser is directly used to cure the printed polymer dielectric material (iii) the silver conductive interconnects are subsequently printed using the deposition system dedicated for metallic inks. By following this sequence, the manual imprinting and vias opening steps will be eliminated from the process flow presented in chapter 3. This will make the process flow much shorter and enable a much higher throughput of the overall assembly. Furthermore, the AJP process can be further optimized to print the metallic interconnects (silver or copper) from the EICs and PICs to the electrical traces on the printed circuit board (PCB). Therefore, this will require creating a ramp at the chip edges which will be feasible to realize using dielectric deposition by AJP.

It would be very interesting to show the advantage of using AJP to interconnect a traveling-wave electrode Mach-Zehnder modulator, since it requires a $50\ \Omega$ transmission line to match its $50\ \Omega$ RF terminations. With the AJP tuning capability, $50\ \Omega$ transmission line can be printed. Furthermore, 3D printed interconnections from the chip to the interposer (PCB) can be also realized but this will require some optimization to create a polymer support ramp from the chip to the interposer, which can be printed using AJP as well.

The throughput of AJP technology can not be compared yet with the traditional subtractive lithographic processes for mass-production application. However, there is much ongoing research to boost the throughput of the technology by increasing the number of deposition heads in the same system and to increase the print speed. A single deposition head can print over 5000 interconnects with a length of 1.5 mm at 1 hour and it can operate up to 12 hours before ink refill. An automated ink refill can extend the operation time up to 24

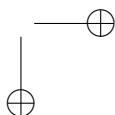
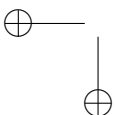


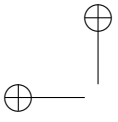
hours. AJP systems with 5 deposition heads have been already manufactured for printed electronics applications in particular for printing smartphone antennas.

In this thesis, we focused on realizing electro-optical assemblies at the transmitter side. However, the research could be extended to the receiver side and we can apply our packaging approach to interconnect photodiode (PDs) and trans-impedance amplifiers (TIAs) to develop optical receiver assembly. Eventually, all the work could be integrated together and the complete optical transceiver can be demonstrated.

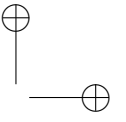
For adiabatic coupling between polymer and SOI waveguides discussed in chapter 5, the insertion loss can be further reduced by tuning the dimensions of the polymer waveguides, improving the DWL alignment accuracy, and optimizing the taper design for higher optical coupling. Additionally, low loss polymer materials such as fluorinated acrylates could be used to produce ultra low loss waveguides (0.05 dB/cm at 1550 nm) as discussed in section 4.2 in chapter 4

As discussed in the introduction in chapter 1, it would be very interesting to demonstrate both AJP interconnection and the adiabatic coupling approaches on the same interposer. This will require to design a suitable PIC with edge couplers and electrical functionalities on the same chip. But, only PICs with grating couplers and electrical functionalities were available during this work. In any case, the two approaches can be integrated on the same platform. This will require the PIC and EIC to be embedded in an epoxy layer. The polymer waveguides are then defined by DWL on the PIC chips to act as an optical fanout based on adiabatic coupling. Finally, The electrical interconnects are subsequently printed between PIC and EIC using AJP.



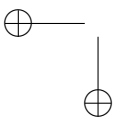


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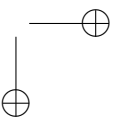


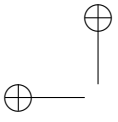
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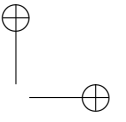


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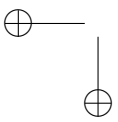


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