Origin of the Negative Differential Resistance in the output characteristics of a picene-based Thin-Film Transistor

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***Abstract*—In this work, we have fabricated and studied p-type picene thin-film transistors. Although the devices exhibited good electrical performance with high field-effect mobility (up to 1.3 $cm^2/V \cdot s$) and on/off ratios above 10^5, the output electric characteristics of the devices exhibited a Negative Differential Resistance for higher drain-source voltage. Finally, a possible explanation for this phenomenon is developed.**

***Index Terms*—OTFT, NDR, Organic semiconductors, non ideal output**

I. Introduction

Thin-Film Transistors based on organic semiconductors (OTFT) is one of the key device in modern electronics. Organic compounds incorporate semiconducting materials often based on π-conjugated bonds that are mechanically compatible with flexible substrates, opening a new fan-out opportunity for emerging applications. Examples span from healthcare-monitoring devices, electronic newspapers, flexible displays, and flexible radio frequency identification tags.

However, almost all electronic devices used in daily life are based on inorganic semiconductors, like, silicon, gallium arsenide, indium phosphate, etc. Most of this inorganic Field Effect Transistors (FET) owned their place on the market due to their high operating speed, and environmentally stable and everlasting performance. In order to make OTFT appealing to future industry, technical issues related to structures, materials, models, operating principle, fabrication and *device performance parameters* have to be solved [3].

When moving in this direction one can observe that the electrical outputs obtained from OTFTs often deviates from the expected transistor behaviour [1]. These non-ideal performance leads to variability on the resulting *transistor parameters*.

One of the irregularities often observed in OTFTs is the presence of Negative Differential Resistance (NDR) in the saturation region of the output curve of the device, i.e. an increase in drain-source voltage (V_{DS}) results in a decrease in drain-source current (I_{DS}) for a fixed gate-source voltage (V_{GS}). Understanding the origin of the NDR effect could provide guidelines for interpreting this particular non-ideality usually found in high mobility OTFTs, and give new design rules for the manufacturing of devices with higher reliability.

Finally, we have fabricated OTFTs based on p-type picene semiconductor. Electrical characterization of the devices showed a marked NDR effect in the saturation region of the output $I_{DS}(V_{DS})$ curve. An explanation of the physical origin of the observed negative differential resistance is described by taking into account the effect of the V_{DS} on the gate voltage, and the geometry of the device.

II. Experimental

We fabricated the OTFTs using the inverted-staggered (top contact) structure shown schematically in Figure 1. The substrate consisted of a thermally oxidized silicon wafer with a thickness of 120 nm for the SiO_2 dielectric. A polystyrene (PS) layer of 30 nm was deposited by spin-coated on top of the SiO_2 dielectric layer in order to improve the crystallinity of the

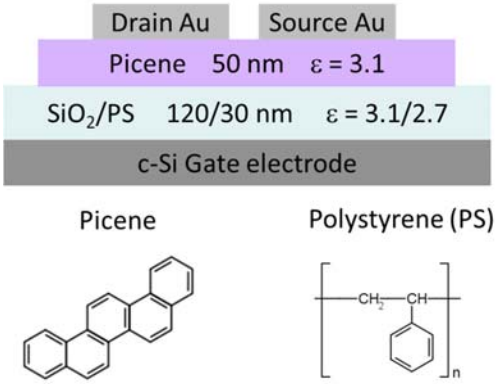

Figure 1 (Top) Scheme of the fabricated TFT based on picene. Thicknesses and permitivitty values of the picene and dielectric layer are showed. (Bottom) Chemical structure of the picene and polystyrene molecule.

picene thin-film layer. Therefore, the capacity of the insulator (SiO_2/PS) per unit area was 20 $nF \cdot cm^{-2}$. picene and PS

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compounds, purchased from Sigma–Aldrich, were used without further purification. The active picene layer (50 nm) was deposited in a vacuum system with base pressure below 10^{-6} mbar and the sublimation temperature was regulated near to 135 °C to maintain a stable deposition rate around 0.5 Å/s. After picene deposition, the samples were transferred to a different vacuum chamber used to evaporate metallic contacts. The drain and source gold electrodes were defined by means of a metallic shadow mask, with a channel length (L) and width (W) of 50µm and 600 µm, respectively. The fabricated OTFTs were electrically characterized in air and under vacuum conditions (10^{-1} mbar) using an Agilent 4156C parameter analyser.

The charge carrier mobility (μ) and the threshold voltage (V_{th}) were estimated in the saturated region by using the following equation:

$$I_D = \frac{W\, C_{ox}\mu}{2L}(V_{GS} - V_{th})^2$$

where W and L are the channel width and length, respectively, and C_{ox} is the capacitance of the dielectric per unit area.

Figure 2 shows the transfer and the saturation characteristics of the device, showing an excellent p-type behaviour. From the saturation curve (inset of Figure 2) the carrier field-effect mobility and threshold voltage were estimated.

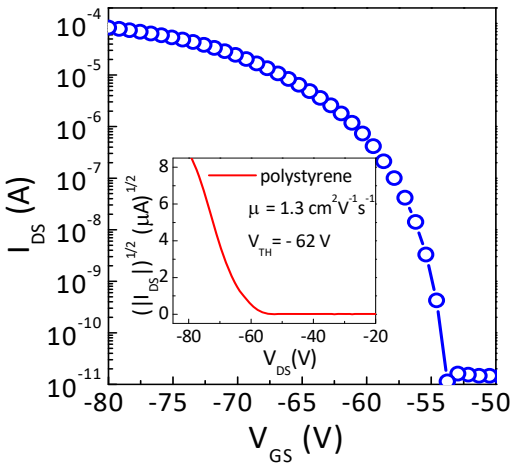

Figure 2. Transfer characteristics. (Inset) Saturation characteristcics, from which the field-effect mobility and Threshold voltage are estimated

Plotted in Figure 3 one can observe the output current obtained from the picene TFT. When a low V_{DS} is applied, one can see that the current does not scales linearly with the applied voltage. This probably indicates a crowding effect near the contact as a result of a poor carrier injection at the electrodes. For higher V_{DS} values we would expect a saturation of the I_{DS} on a functional transistor. Instead, as seen in Figure 3 the current output starts to decrease as the voltage increases. This phenomenon is usually named as negative differential resistance (NDR) regime, and appears for V_{DS} voltages values higher than $V_{DS\text{-}SAT}$.

The origin of this NDR effect is yet unclear. A possible

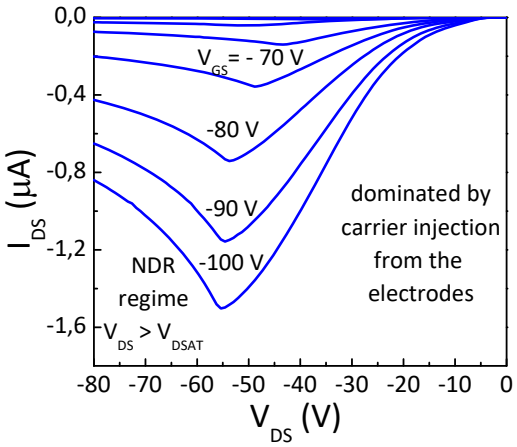

Figure 3. Output characteristics of the picene-based TFT. NDR effect is observed for V_{DS} voltages higher than V_{DSAT}

explanation could be argued based on the geometry of the transistor and the different values of the dielectric constants of the semiconductor and insulator.

The variation of I_{DS} upon the application of V_{DS} is usually explained by the change of the accumulated charge at the semiconductor/dielectric interface induced by the application of V_{GS} (field-effect phenomenon). Consequently, the applied V_{GS} controls the *electrical resistance* of the channel and therefore the I_{DS} [1].

Nevertheless, one can understand the FET by analysing the relative energy level position of the different elements involved in the device. Therefore, the electrical output of a TFT can be understood from the position of the Fermi level of the drain, source and semiconductor [2]. First, when the device is in equilibrium, Fermi level must be equal everywhere. The external application of a V_{DS} will split away the Fermi level of the drain and source electrodes ($E_{F1} - E_{F2} = -\,q \cdot V_{DS}$).

In order to drive the system again into equilibrium, carriers (holes in our picene TFT) will flow between source and drain electrodes through available electronic states at the semiconductor. In this view the flow of carriers will be motivated by an external potential gradient that allows carriers on one electrode to reach a lower energetic state available on the other electrode, thus, filling the electronic states until Fermi level of the electrodes reach once again equilibrium conditions ($E_{F1} = E_{F2}$). In this picture, the external applied voltage (V_{DS}) maintains the electrodes Fermi levels separated, continuously pulling the system out of equilibrium, and eventually yielding a continuous carrier flow between both electrodes; as carriers keep trying to drive the system back into equilibrium forced by the external voltage applied onto the Drain.

However in order to obtain a true picture of the device one must include the available conducting energy states inside the semiconductor, as the device current (I_{DS}) or the carriers flow will be limited by the amount of available states (Density-of-States (DOS)) in the semiconductor, between the energy window defined between the Fermi levels of the electrodes, i.e. $E_{F1} - E_{F2}$.

In the particular case of a p-type semiconductor, like picene,

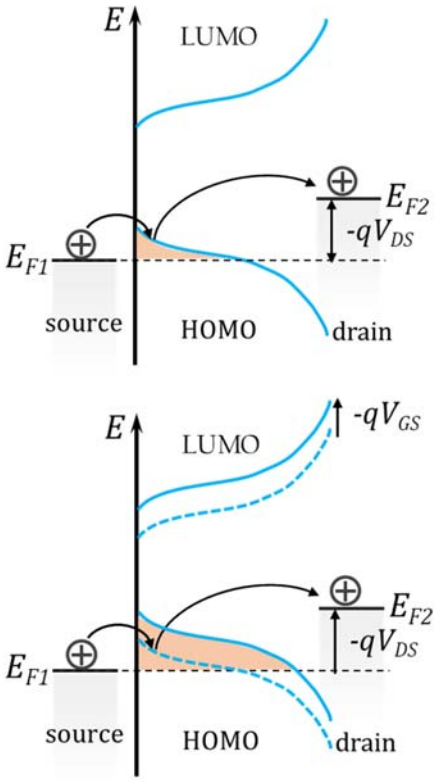

Figure 4. (Top) Schematic representation of the energy levels of the source, drain and DOS of the p-type picene TFT. (Bottom) Application of negative V_{GS} voltage shifts down the picene DOS, increasing the number of available states.

these electronic states will be located around the HOMO level of semiconductor (HOMO corresponds to the High Occupied Molecular Orbital of the semiconductor). One can see in Figure 4 (top) a schematic representation of the energy levels of the source and drain electrodes and the difference obtained in terms of the location of the Fermi level upon the application of negative V_{DS} (applied to the drain with respect to the source). The window of available conduction states of the semiconductor between source and drain Fermi levels has been coloured on the schematic DOS of the semiconductor. It looks intuitive from this picture that a higher applied V_{DS} results in a larger I_{DS} . The saturation of the output in this model is understood from the limited amount of available states in the semiconductor. This means that when V_{DS} is larger than $V_{DS\text{-}SAT}$ there are no more available conducting states in the semiconductor and the rate of carriers that flow through the semiconductor will remain equal, regardless of an increase in external voltage.

Let us examine the situation when a voltage is applied to the gate with respect to the source (Figure 4 (down)). In this case the negative V_{GS} changes the potential in the semiconductor channel displacing its Fermi level upwards. The displacement of the Fermi level of the semiconductor will pull all electronic states up in energy. Therefore, an increase in V_{GS} triggers an increase of DOS between the Fermi levels of the electrodes.

Since Fermi levels of the source and drain remains unaffected (V_{DS} has not changed) the increase of DOS between $E_{F1} - E_{F2}$ yields an increase in I_{DS}, as shown in Figure 4b.

In conclusion, increasing V_{GS} results in more electronic states available in the channel for conduction, and therefore an increase of the Drain Source current.

Furthermore, the existence of a threshold gate voltage (V_{th}) as the voltage needed to turn the transistor *on* can be explained by the energy difference between the equilibrium Fermi level of the semiconductor ($E_{SC} = E_{F1} = E_{F2}$) and the lowest available empty electronic state of the semiconductor, that in the case of p-type semiconductor corresponds to the HOMO conduction edge.

Finally, since from this model one can describe the working principle of a TFT, we believe that this model can be used to provide an explanation of the NDR effect that appears at higher V_{DS} voltages on the output characteristic of our picene devices.

It is important to point out that our TFT structure is quite symmetrical from the point of view of the active and dielectric layer. This means that the thicknesses of the picene and the dielectric layers lie on the same order of magnitude. Furthermore, dielectric constants of the picene and the SiO2/PS layers have similar values. This particular situation has strong impact on the device performance. In particular, the application of a V_{DS} splits the Fermi levels of the source and drain electrodes apart, as previously commented, but because of the geometric location of the electrodes and the channel as well as the existing symmetry between dielectric and semiconductor layer, the voltage applied also affects the position of the DOS of the semiconductor. Which in this case it would affect it by displacing it in the opposed direction of V_{GS}. We can describe this interaction on a first term approximation by use of a function $\alpha(V_{GS}, V_{DS})$ that describes the relation between gate and drain voltage and saturation current as a function of the applied V_{DS}.

$$I_D = \frac{W\, C_{ox}\mu}{2\mathrm{L}}(V_{GS} - \alpha(V_{GS}, V_{DS}) \cdot V_{DS} - V_{th})^2$$

In this expression the NDR term is introduced as mathematical representation of the V_{DS} dependant reduction of the DOS in the semiconductor obtained in the picene device when the effect of V_{DS} becomes comparable to the effect of V_{GS} on the semiconductor Fermi level location. This effect is more prominent in the saturation region, when the channel pinch-off has already happened.

I. Conclusion

The existence of Negative Differential Resistance measured in picene-based thin-film transistors is explained by taking into account the geometry of the device and the permittivity of both, active and dielectric layer. The application of a large drain-source voltage counteracts the charge accumulation effect generated by the gate-source voltage near the drain contact (i.e it displaces the DOS of the semiconductor in the opposite direction of an external V_{GS}), thereby *reducing* the number of

available states in the channel and progressively decreasing the I_{DS} current.

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