Fault Tolerant Multilevel Inverter Topologies with Energy Balancing Capability: Photovoltaic Application

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Approval Sheet

This thesis entitled "Fault Tolerant Multilevel Inverter Topologies with Energy Balancing Capability: Photovoltaic Application" by Madhukar Rao A is approved for the degree of Doctor of Philosophy from IIT Hyderabad.

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Dedicated to My Parents….

Abstract

The continuous increase in energy demand and depletion of conventional resources motivates the research towards the environment friendly renewable energy sources like solar and wind energy. These sources are best suitable for rural, urban and offshore locations, because of easy installation, less running cost and ample resources (sun light and wind). The remote locations are mostly islanded in nature and far away from technical expertise in case of troubleshooting. This motivates the research on development of fault tolerant converters. These fault tolerant converters increases the reliability, which provides the continuous power supply to critical loads. From the last few decades, the integration of multilevel inverters with renewable energy systems is also increasing because of advantages like, improved power quality, total harmonic distortion (THD) and reduced output filter size requirement. Employing conventional multilevel inverters for increasing the number of voltage levels increases the device count and isolated DC sources. As a result probability of semiconductor switch failure is more and energy balancing issue between sources, which in-turn degrades the reliability and performance of the inverter. The majority of conventional multilevel inverter topologies cannot address energy balancing issues between multiple photovoltaic (PV) sources, which may need because of partial shading, hotspots, uneven charging and discharging of associated batteries etc. If energy sharing not addressed effectively, the batteries which are connected to the shaded or faulty PV system will discharge faster which may cause total system shutdown and leads to under-utilization of healthier part of the system. To address these issues, fault tolerant multilevel inverter topologies with energy balancing capability are presented in this thesis.

The major contributions of the proposed work are

- Single phase and three phase fault tolerant multilevel inverter topologies.

- Energy balancing between sources and dc off set minimization (or batteries) due to uneven charging and discharging of batteries for five-level inverter.
- Extending the fault tolerance and energy balancing for higher number of voltage levels.

The first work of this thesis is focused to develop fault tolerant single phase and three phase multilevel inverter topologies for grid independent photovoltaic systems. The topologies are formed by using three-level and two-level half bridge inverters. The topology fed with multiple voltage sources formed by separate PV strings with MPPT charge controllers and associated batteries. Here the topologies are analyzed for different switch open circuit and/or source failures. The switching redundancy of the proposed inverters is utilized during fault condition for supplying power with lower voltage level so that critical loads are not affected.

In general, the power generation in the individual PV systems may not be same at all the times, because of partial shading, local hotspots, wrong maximum power point tracking, dirt accumulation, aging etc. To address this issue energy balancing between individual sources is taken care with the help of redundant switching combinations of proposed five-level inverter carried out in second work. Because of partial shading the associated batteries with these panels will charge and discharge unevenly, which results voltage difference between terminal voltages of sources because of SOC difference. The energy balance between batteries is achieved for all operating conditions by selecting appropriate switching combination. For example during partial shading the associated battery with low SOC is discharged at slower rate than the battery with more SOC until both SOC's are equal. This also helps in minimization of DC offset into the ac side output voltage. The mathematical analysis is presented for possible percentage of energy shared to load by both the sources during each voltage level.

The third work provides single phase multilevel inverter with improved fault tolerance in terms of switch open circuit failures and energy balancing between sources. Generally multilevel inverters for photovoltaic (PV) applications are fed

with multiple voltage sources. For majority of the multilevel inverters the load shared to individual voltage sources is not equal due to inverter structure and switching combination. This leads to under-utilization of the voltage sources. To address this issue optimal PV module distribution for multilevel inverters is proposed. Mathematical analysis is carried out for optimal sharing of PV resources for each voltage source. The proposed source distribution strategy ensures better utilization of each voltage source, as well as minimizes the control complexity for energy balancing issues. This topology requires four isolated DC-sources with a voltage magnitude of Vdc/4 (where Vdc is the voltage requirement for the conventional NPC multilevel inverter). These isolated DC voltage sources are realized with multiple PV strings. The operation of proposed multilevel single phase inverter is analyzed for different switch open-circuit failures.

All the presented topologies are simulated using MATLAB/Simulink and the results are verified with laboratory prototype.

Nomenclature

Abbreviations

SOC	**:** State of Charge
PV	**:** Photovoltaic
THD	**:** Total Harmonic Distortion
MPPT	**:** Maximum Power Point Tracking
SVPWM	**:** Space Vector Pulse Width Modulation
MLI	**:** Multilevel Inverter
NPC	**:** Neutral Point Clamped
FC	**:** Flying Capacitor
DER	**:** Distributed Energy Resource
PCB	**:** Printed Circuit Board
IGBT	**:** Insulated Gate Bipolar Transistor
MOSFET	**:** Metal Oxide Semiconductor Field Effect Transistor
TRAIC	**:** Triode for alternating current
SVC	**:** Space Vector Control
SHE	**:** Selective Harmonic Elimination
SPWM	**:** Sinusoidal Pulse Width Modulation
LED	**:** Light Emitting Diode
FPGA	**:** Field Programmable Gate Array
VHDL	**:** VHSIC Hardware Description Language
PD	**:** Phase Disposition
POD	**:** Phase Opposition Disposition
DSPACE	**:** Digital Signal Processing and Control Engineering
Symbols	**: Definitions**
F1, F2	**:** Fuse
Vr	**:** Space vector
$\mathbf{V_{\alpha}, V_{\beta}}$	**:** Two dimensional space vectors
$\mathbf{V_{AO}, V_{BO}, V_{CO}}$	**:** Three phase voltages
$\mathbf{I_{sa}}$	**:** PV module output current
$\mathbf{V_{sa}}$	**:** PV module output voltage

$\mathbf{N_P}$	**:** Number of parallel connected cells
$\mathbf{N_S}$	**:** Number of series connected cells
$\mathbf{R_s}$	**:** Series resistance
$\mathbf{R_{sh}}$	**:** Shunt resistance
$\mathbf{I_{ph}}$	**:** Light generated current
$\mathbf{I_{sat}}$	**:** Reverse saturation current
A	**:** Ideality factor
K	**:** Boltzmann's constant
T	**:** Cell temperature
Q	**:** Electronic charge
Vm	**:** Modulating signal
Vtri	**:** Triangular signal
$\mathbf{m_a}$	**:** Modulation index
$\mathbf{f_m}$	**:** Modulation signal frequency
$\mathbf{f_s}$	**:** Switching frequency
M1, M2	**:** Relays
$\mathbf{V_{dc\text{-}min}}$	**:** Minimum battery voltage
$\mathbf{S_{f1}}$, $\mathbf{S_{f2}}$	**:** Switch fault signal
$\mathbf{V_{1a}}$, $\mathbf{V_{1b}}$, $\mathbf{V_{1c}}$	**:** Higher voltage level for a, b, c phases
$\mathbf{V_{2a}}$, $\mathbf{V_{2b}}$, $\mathbf{V_{2c}}$	**:** Middle voltage level for a, b, c phases
E	**:** Energy transferred to load
$\boldsymbol{E_{V_{1a}}}$, $\boldsymbol{E_{V_{1b}}}$, $\boldsymbol{E_{V_{1c}}}$	**:** Energy transferred to load during higher voltage level
$\boldsymbol{E_{V_{2a}}}$, $\boldsymbol{E_{V_{2b}}}$, $\boldsymbol{E_{V_{2c}}}$	**:** Energy transferred to load during middle voltage level
$\boldsymbol{V_{avg}}$	**:** Average output voltage

Contents

Chapter 1

Introduction

1.1 Importance of renewable energy system

The demand for renewable energy systems is growing day by day because of continuous increase in energy demand, increase of global economy, rapid industrialization and population growth. In addition, the effects of fossil fuel energy sources like world climate changes (greenhouse gas emissions), which may leads to serious health issues of humans. The early day challenges like, uncertainty and high initial installation cost are limiting the efficient utilization of all renewable energy sources. The tremendous growth in harvesting technology, easy installation, reduced costs, low environmental impact, and recent developments in semiconductor fabrication technology has considerably reduced the initial cost and brought the renewable energy sources back to focus [1].

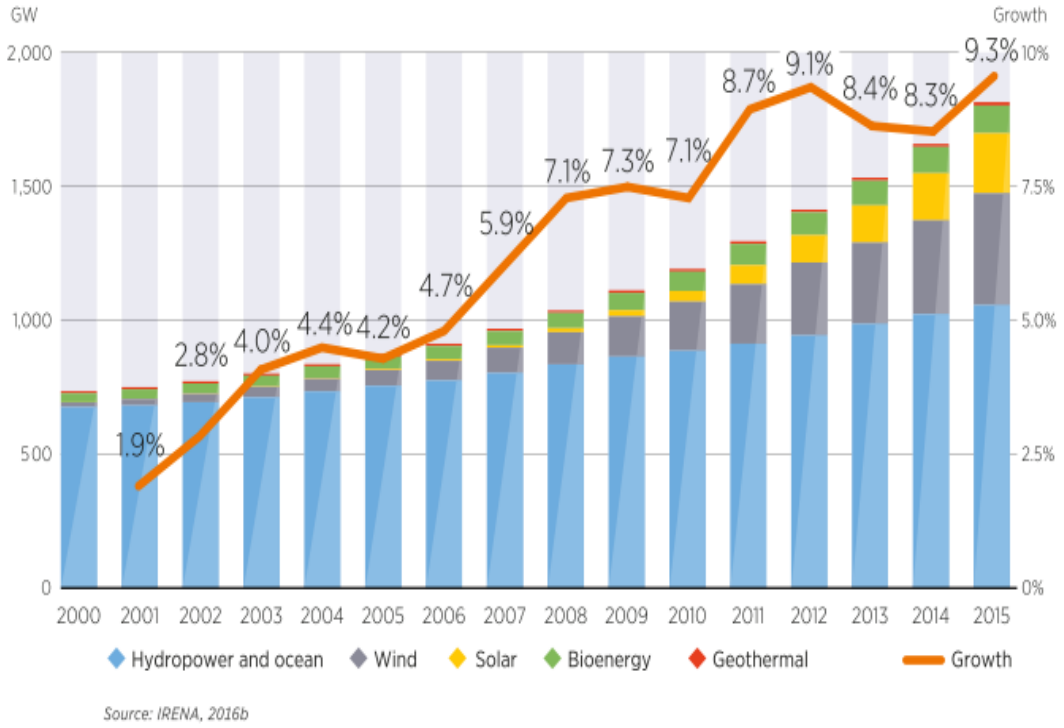

Fig.1.1 Renewable power capacity and annual growth rate, 2000-2015[2]

The annual growth rate of renewable power capacity from 2000 to 2015 is shown in Fig.1.1 [2]. The renewable power generating capacity is exceeded 1,811GW and accounted for more than 28% of global capacity by the end of 2015. Among these renewable energy sources, the share of solar Photo voltaic (PV) is increasing rapidly because of environmental friendly, available of abundant of sunlight and easy installation (at rooftop of houses). The rapid growth rate of solar PV global capacity by country/region from 2005 to 2015 is observed in Fig.1.2 [3].

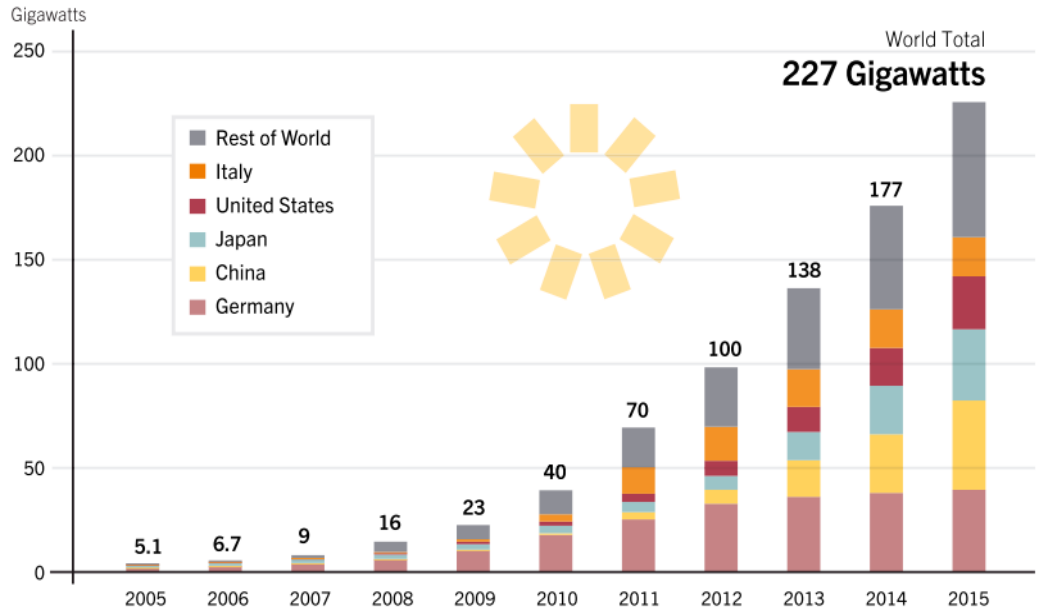

Fig. 1.2 Solar PV global capacity, by country/region 2005-2015 [3]

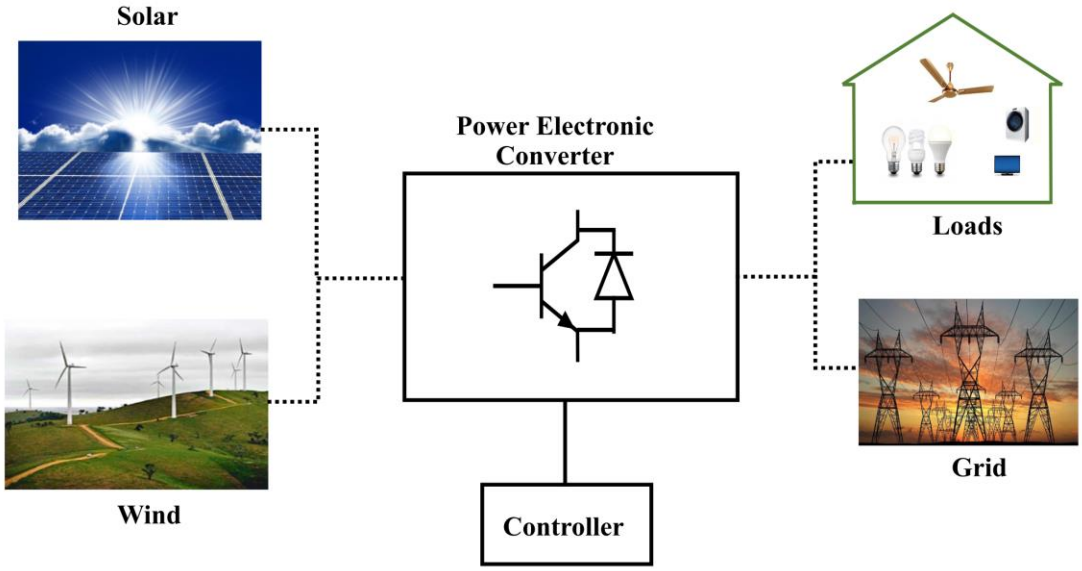

Fig.1.3 Power converter as interface between renewable energy source and load and/or grid

1.2 Importance of power electronic converters for renewable energy system

Power electronic converter plays an important role for conversion of renewable source energy to standardized form of electricity, as shown in Fig.1.3. The power converter uses semiconductor devices to perform switching action to achieve desired conversion strategy [4]. Therefore efficient design of power converter is needed to ensure good power quality and reliability. The dc output of the renewable energy sources like solar energy is converted into ac in a two stage process [5], [6] and [7], which is depicted in Fig.1.4. The first stage is to boost or buck the output voltage of the PV array and to extract maximum power from it using a suitable MPPT technique, with the help of a dc to dc converter. Second stage is for converting to ac by using inverter. Generally, the two stage process uses a two level inverter which will introduce considerable harmonic content along with the fundamental voltage. These harmonics increases loss in the system, which reduces the system efficiency. To improve the efficiency of the total solar system the two stage conversion process is reduced to a single stage process using three-phase boost inverter with SVPWM as explained in [8] and [9]. But, here also relatively the harmonics in the output voltage is high. There are many methods are available to improve the THD of output voltage, of which multilevel inverter is one of the option.

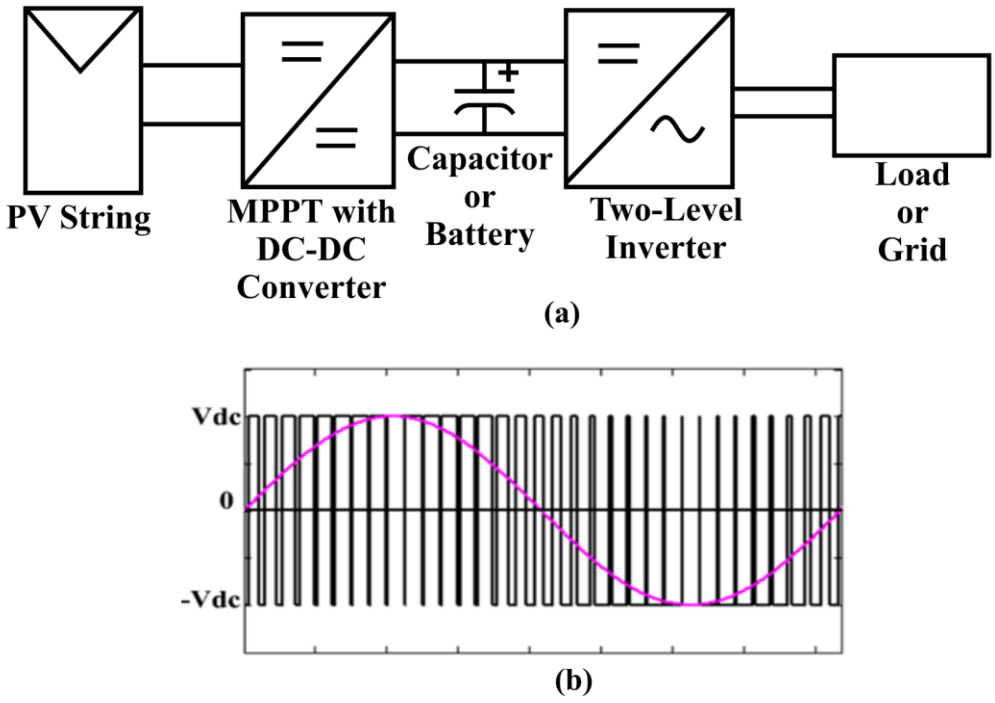

Fig.1.4 (a) Two stage conversion process of PV generation system. (b) Load Output voltage

1.3 Introduction to multilevel inverters (MLI)

Conventional multilevel inverters are introduced to improve the harmonic profile of output voltage [10], [11]. Multilevel inverter technology has been widely used in PV applications, because of its improved output voltage quality, better harmonic performance, less voltage stress on power electronic devices and etc. [12], [13]. The basic concept of multi-level inverters is, connecting power electronic switches in series/parallel along with more number of DC sources to synthesize the staircase waveform. The basic conventional multilevel inverter topologies are diode clamped (Neutral point clamped), flying capacitor and Cascaded H-bridge multilevel inverters [B1].

1.3.1 Diode Clamped multilevel inverter or neutral point clamped inverter (NPC)

The multilevel inverter topology for induction motor drives is proposed in the year 1981 [14] by Nabae, Takahashi and Akagi. The five-level diode clamped multilevel inverter with separate sources is shown in Fig.1.5.

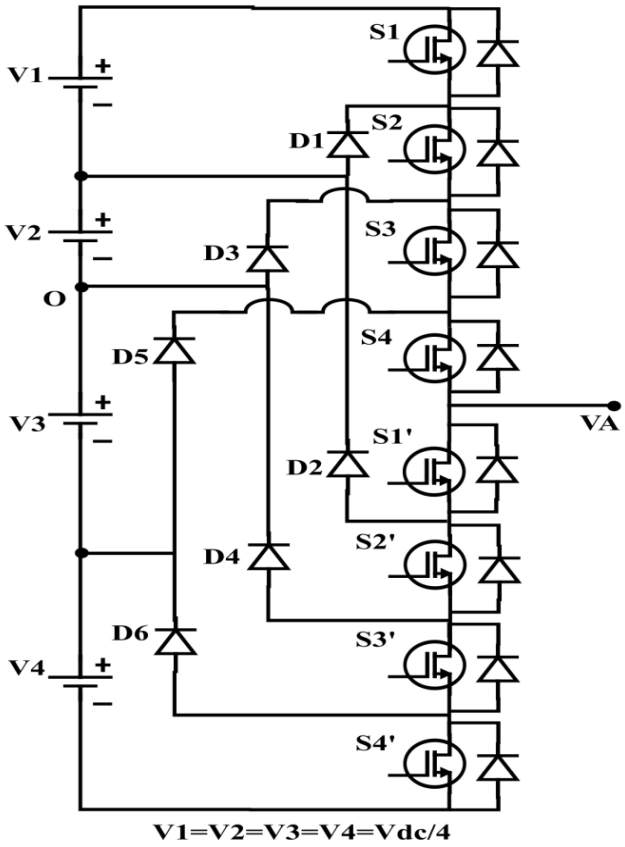

Fig.1.5 Topology of Single leg of five-level NPC inverter

Table 1.1
Switching combination for generating five-level output voltage

Switches in on	Output Voltage Level
S1, S2, S3, S4	$+\frac{V_{dc}}{2}$
S2, S3, S4, S1’	$+\frac{V_{dc}}{4}$
S3, S4, S1’,S2’	0
S4, S1’,S2’,S3’	$-\frac{V_{dc}}{4}$
S1’,S2’,S3’,S4’	$-\frac{V_{dc}}{2}$

The diode clamped multilevel inverter consists of dc bus capacitors, switches and clamping diodes. For an n-level inverter the number of dc bus capacitors required are (n-1), number of clamping diodes is (n-1)*(n-2) and 2(n-1) switches. The voltage across each dc bus capacitor is Vdc/ (n-1). The five-level output voltage is generated using switching combination given in Table 1.1. The drawback of diode clamped inverter is, it requires more number of clamping diodes. The reliability issues of this inverter are increases as the number of voltage levels increases because of more number of devices. In case of isolated voltage sources (instead of capacitors) the power balancing is an issue due to unequal load sharing. If a fault occurs in any one of the middle switch, it is difficult to operate the inverter.

1.3.2 Flying capacitor multilevel inverter (FCMLI)

The flying capacitor multilevel inverter is introduced by T.A Meynard and H.Foch in the year 1992 [15]. Flying capacitor multilevel inverter is derived from diode clamped multilevel inverter topology. Here the diodes are replaced with series connected flying capacitors. N-level FCMLI inverter requires (n-1) dc bus capacitors, 2(n-1) switching devices and (n-1)*(n-2)/2 clamping capacitors. The single leg of five-level flying capacitor multilevel inverter is shown in Fig.1.6. The five-level output voltage is generated using switching combination given in Table 1.2. This topology does not require any clamping diodes, but it requires more number of capacitor banks. These capacitor bank voltages should be controlled within allowable voltage ripple. Here redundant switching states are possible for middle voltage levels. But, it doesn’t have fault tolerance if any one of the switch fails.

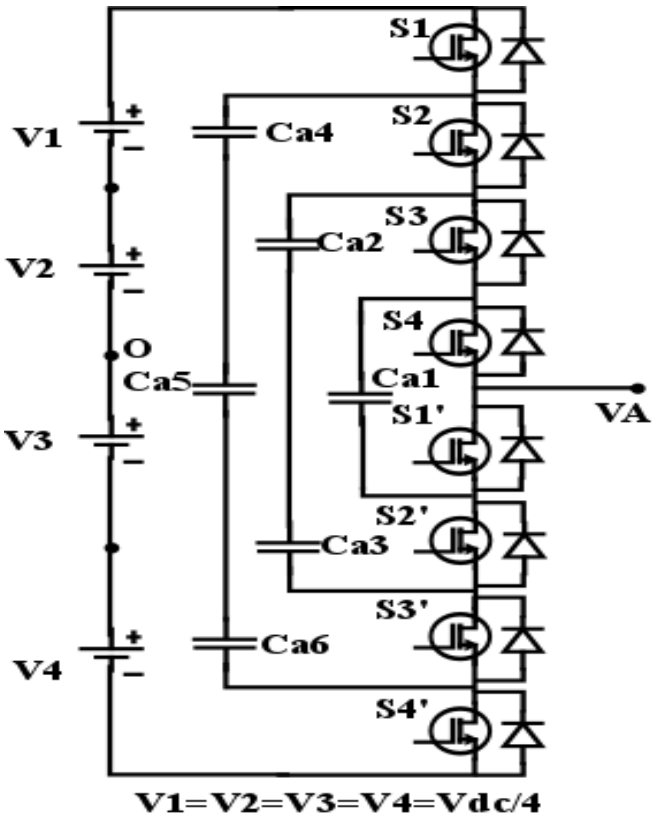

Fig.1.6 Topology of Single leg of five-level FC multilevel inverter

Table 1.2
Switching combination for generating five-level output voltage

Switches in on	Output Voltage Level
$S1, S2, S3, S4$	$+\frac{V_{dc}}{2}$
$S1, S2, S3, S1'$	$+\frac{V_{dc}}{4}$
$S1, S2, S2', S4'$	$+\frac{V_{dc}}{4}$
$S1, S3', S4, S3$	$+\frac{V_{dc}}{4}$
$S1, S2, S1', S2'$ (or) $S3, S4, S3', S4'$ (or) $S1, S3, S1', S3'$ (or) $S1, S4, S2', S3'$	0
$S1, S1', S2', S3'$	$-\frac{V_{dc}}{4}$
$S4, S2', S3', S4'$	$-\frac{V_{dc}}{4}$
$S3, S1', S3', S4'$	$-\frac{V_{dc}}{4}$
$S1', S2', S3', S4'$	$-\frac{V_{dc}}{2}$

1.3.3 Cascaded H-bridge multilevel inverter

. Cascaded multilevel inverter is another popular topology for high-power medium voltage drives [16]-[18], because it doesn't have capacitor voltage unbalancing issues. The five-level cascaded multilevel inverter requires less number of components than the diode clamped and flying capacitor MLI's, as shown in Fig.1.7. The disadvantage of cascaded H-bridge multilevel inverter is as the number of levels increases, it requires more number of isolated dc sources. The five-level output voltage is generated using switching combination given in Table 1.3. Because of switching redundancies, the five-level cascade H-bridge topology has fault tolerant capability if any one of the switch fails. During fault it can able to generate three-level output voltage using redundant switching combinations. But, it has no fault tolerance capability if any leg of the H-bridge cell fails. As the number of voltage levels increases the components required for the topology increases and also the control complexity to control semiconductor devices and reliability issues increases.

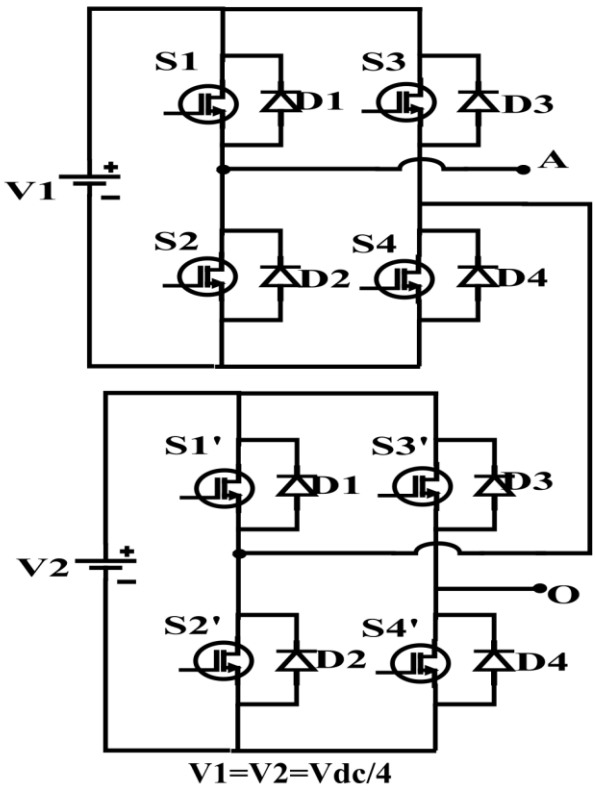

Fig.1.7 Five-level cascade H-bridge multilevel inverter

Table 1.3
Switching combination for generating five-level output voltage

Switches in on	Output Voltage Level
$S1, S4', S1', S4$	$+\frac{V_{dc}}{2}$
$S1, S4', S2', S4$	$+\frac{V_{dc}}{4}$
$S1, S1', S3', S4$	$+\frac{V_{dc}}{4}$
$S1', S4, S2, S4'$	$+\frac{V_{dc}}{4}$
$S1, S3, S2', S4'$	0
$S1, S3, S1', S3'$	0
$S2, S4, S2', S4'$	0
$S2, S4, S1', S3'$	0
$S3, S2', S4', S2$	$-\frac{V_{dc}}{4}$
$S3, S1', S3', S2$	$-\frac{V_{dc}}{4}$
$S3', S2, S4, S2'$	$-\frac{V_{dc}}{4}$
$S3, S2', S3', S2$	$-\frac{V_{dc}}{2}$

1.3.4 Inverter topologies with reduced number of switches

In literature many multilevel inverter topologies with reduced number of components for achieving higher number of voltage level is presented [19]. In Fig.1.8 five-level inverter topology is presented for multistring distributed energy resources (DER), it requires six semiconductor devices where as conventional multilevel inverter topologies requires eight semiconductor devices. Thereby it requires less number of driver circuit and components compared to conventional multilevelinverter topologies. If any one of the switch fails, this topology doesn't has the fault tolerance capability.

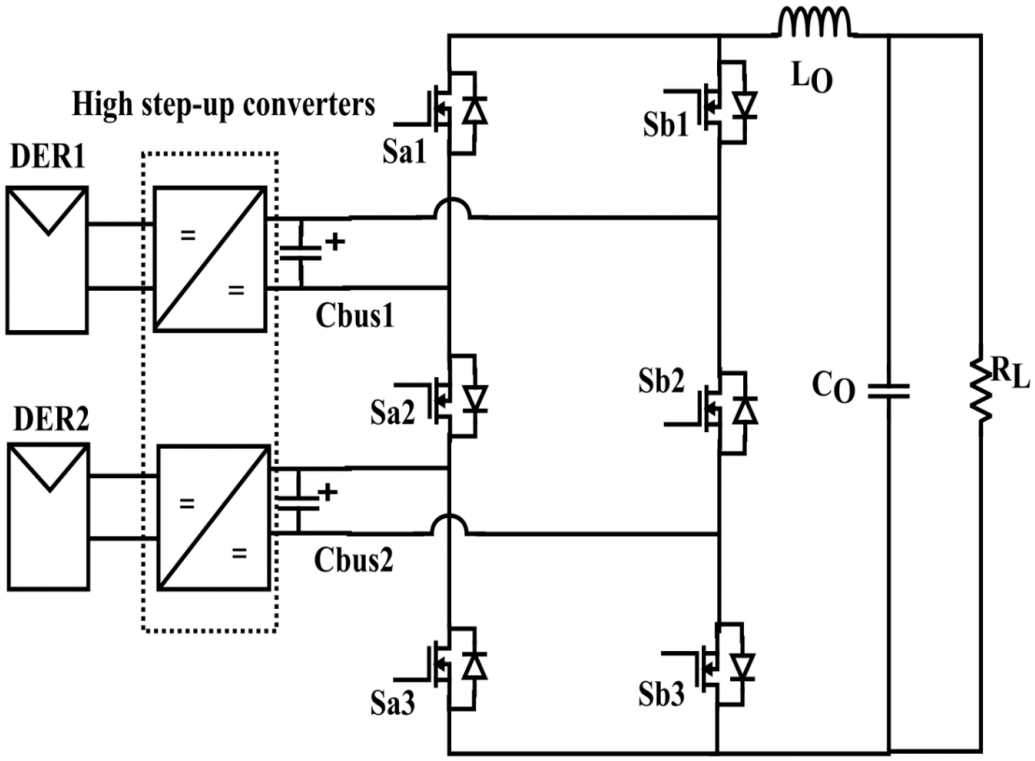

Fig.1.8 Single phase multistring five-level inverter topology [19]

The single phase five-level inverter topologies are proposed in [20], [21] with less number of components as compared to conventional five-level inverter topologies. The five-level inverter topology presented in [20] is formed by one H-bridge cell and two extra switches connected between sources, as shown in Fig.1.9. However, this topology is unable to generate output voltage at load under H-bridge switch failures. Another interesting five-level inverter topology is presented in [21], which is formed by one H-bridge cell, one unidirectional switch and bidirectional switch shown in Fig. 1.10. The bidirectional switch has capable of conducting current and blocking voltage in both directions. This bidirectional switch is currently available in markets as a module. This module requires only one isolated power supply instead of two for the gate driver. The topology requires same number of gate drive circuits as the topologies presented in Fig. 1.8 and Fig.1.9. But, it also has no fault tolerance if any switch of the H-bridge cell fails.

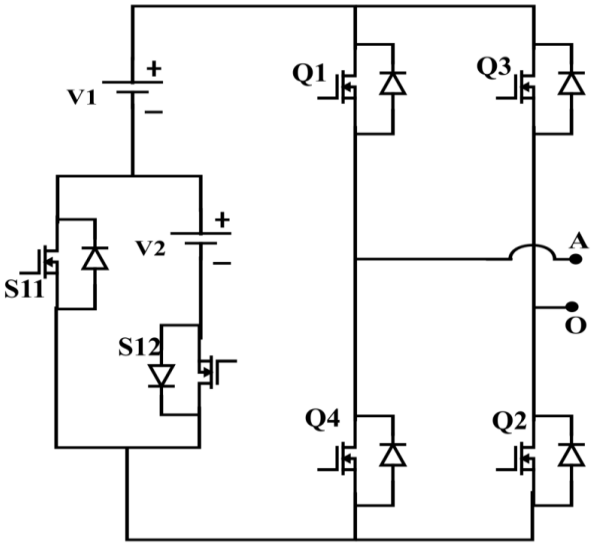

Fig 1.9 Single phase five-level inverter configuration [20]

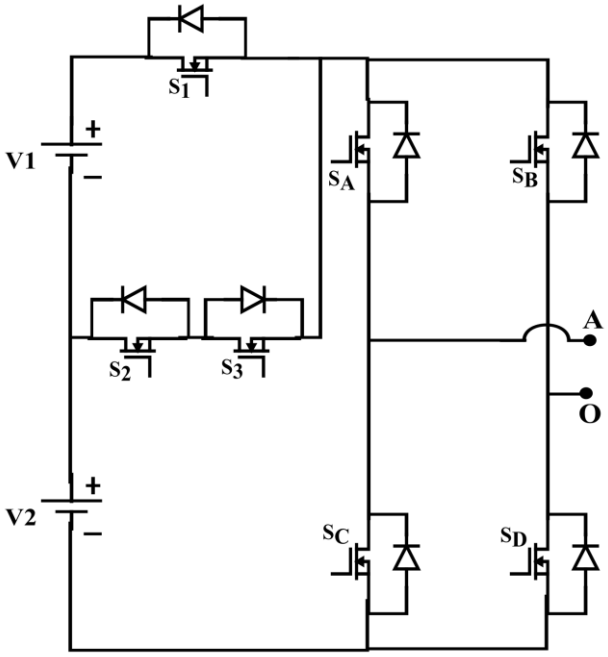

Fig 1.10 Single phase five-level inverter configuration [21]

1.4 Importance of fault tolerant multilevel inverter for stand-alone PV system

The 2010 international energy agency report says that around the world still 1.4 billion people without accesses to electricity even though with the continuous improvement in energy sector [22]. This strongly supports the need of stand-alone renewable generation system to those people and also for areas which are far away from grid and remote locations. Generally, multilevel inverters requires more

semiconductor devices to improve the harmonic profile of output voltage, if any fault occurs in these stand-alone power converters i.e. semiconductor switches and/or source failure leads to total shutdown of the system. These locations are far away from technical expertise in case of trouble shooting and have to operate at least some of the important loads. This brings in need of fault tolerant converter for islanded PV generation system.

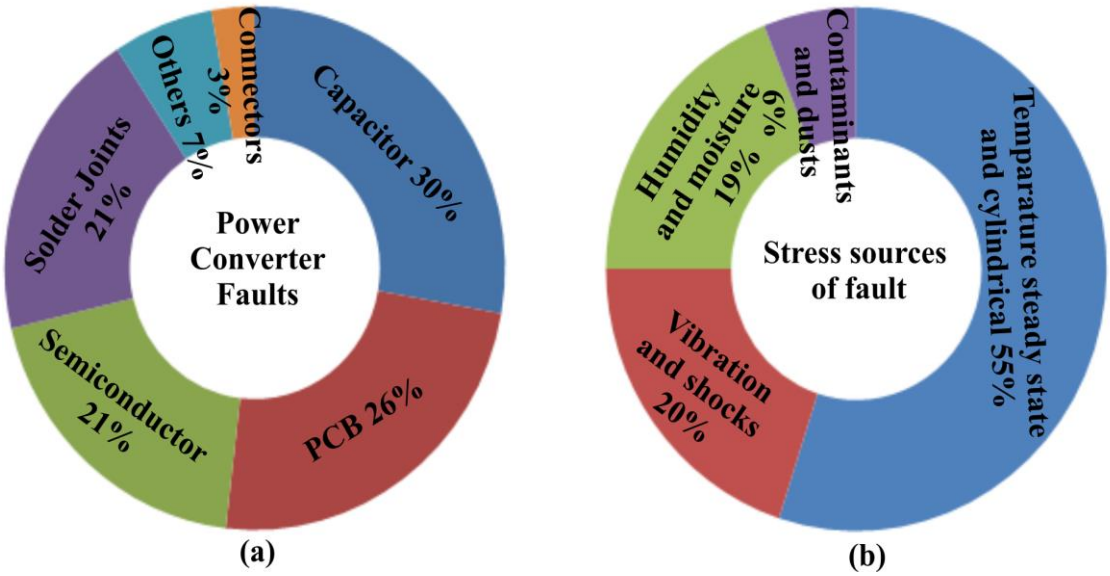

Fig.1.11 (a) Distribution of faults in power converter (b) Stress sources of fault [26]

1.4.1 Fault tolerant multilevel inverter configurations

The necessity and importance of reliability of power converters are discussed in [23], [24], [B6]. Generally, inverter failures occur due to semiconductor device failure, gate driver failure and PCB failures [25]. The percentage of different type of failures in power converter and sources of failure is shown in Fig.1.11 [26]. The semiconductor device failure is mainly because of short circuit and open circuit fault. The causes of short circuit fault are over voltage, high temperature and wrong gate voltage. This short circuit fault leads to abnormal current flow in power converter, which causes the serious damage to other parts of power converter with in very short time. Several reasons for open circuit fault are gate drive fault, lifting and cracking of bonding wires in IGBT modules due to thermal cycling. Compared to short circuit fault the open circuit fault cannot cause serious damage to power converter. Hence, fault detection techniques and control of fault tolerance are needed in power

electronic systems [27]. The different methods for detection of short circuit and open circuit faults and fault tolerant strategies are presented. The different open circuit fault and short circuit fault methods along with their comparison are presented in Table 1.4 and Table 1.5.

Table 1.4 [26]

Comparison of Different Open circuit fault Methods

Methods	Effectiveness	Diagnosis Time	Considered Parameters	Implementation Effort	Tuning Effort	Additional Hardware
Current vector shape method [28-32]	Poor at small current	Within Two fundamental Periods	3-Phase currents	Low	Medium	Not required
Slope of space vector's trajectory methods [32], [33]	Poor at small current	Average two fundamental periods	3-phase currents	Low	High	Not required
Direct average current method [34], [35]	Poor at small current	Within 1.5 fundamental Periods	3-phase currents	Low	Medium	Not required
Modified normalized average current method [34], [36]	Good	Within 1.5 fundamental Periods	3-phase currents	Low	Low	Not required
Method based on switching function model [37]	Good	Fast but not defined	Switch voltage, signal	Medium	Low	Required
Lower switch voltage measuring method [38]	Good but the location cannot be identified	Approximately 2.7ms	Lower switch voltage	Medium	Low	Required

Table 1.5 [26]

Comparison of Different short circuit fault Methods

Method	Reliability	Considered Parameters	Implementation Effort	Turn-off	Remarks
Desaturation detection method [39]-[41]	Medium	Collector voltage	Low	Abrupt	Device turn-off not assured
di/dt feedback control method [42], [43], [44]	Medium	Device current	High	soft	Stray inductance difficult to control
Gate voltage monitoring method [45], [46]	Low	Gate voltage	Low	abrupt	Requires complex circuitry
Gate voltage comparison method [47],[48],[49]	Low	Gate voltage	Low	soft	Requires complex circuitry
Current mirror method [42]	Medium	Device current	Low	Abrupt	Expensive
Protection using snubber and clamped circuit [50]	Low	Device voltage	High	N/A	Expensive
Protection by slow turn-off of IGBT [50]	Low	Gate voltage	High	soft	Requires complex circuitry

The different techniques for fault detecion are presented to isolate the system from fault but not much literature is presented to operate the system after post fault conditions to continue the operation of the essential loads.

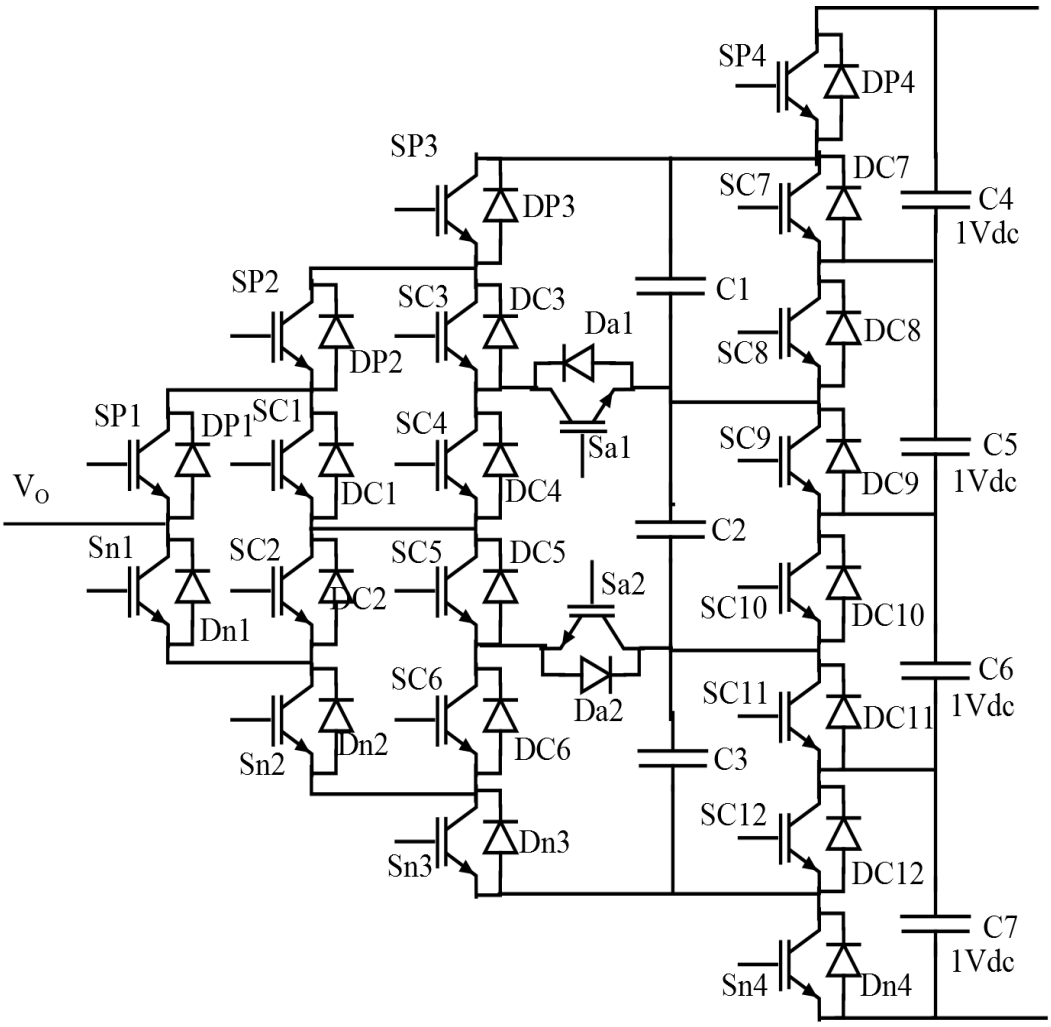

Fig. 1.12 Five-level inverter topology with fault tolerant ability [51]

In [51], a fault tolerant topology is presented for improving the reliability of the system, as shown in Fig. 1.12. The advantage of this topology is to maintain same number of output voltage levels during fault condition. The fault tolerance is achieved by using redundant states of the voltage states that is by modifying the control signal. However, it requires more number of semiconductor devices to make fault tolerant system. The topology uses 22 semiconductor devices (conventional five-level requires 8 semiconductor devices) for five-level fault tolerant operation. In [52], fault tolerant topology for grid connected PV application using coupled Scott transformer is proposed. In normal condition the topology operates with less number of switches, but during fault it requires additional leg to replace the faulty switch. Different fault tolerant topologies for neutral point clamped (NPC) and three phase two level inverter are shown in Fig.1.13 and Fig. 1.14 [53-55]. To provide open

circuit fault tolerance in three-level NPC inverter the clamping diodes are replaced with extra switches, as shown in Fig.1.13 (a). The purpose of these switches is to provide redundant switching states to provide fault tolerance, when any switch of one leg fails. Fig.1.13 (b) shows NPC with triac connected between neutral point of the sources and midpoint of NPC leg. The purpose of this TRIAC is to connect the faulty leg to the neutral point of the converter under open circuit switch faults.

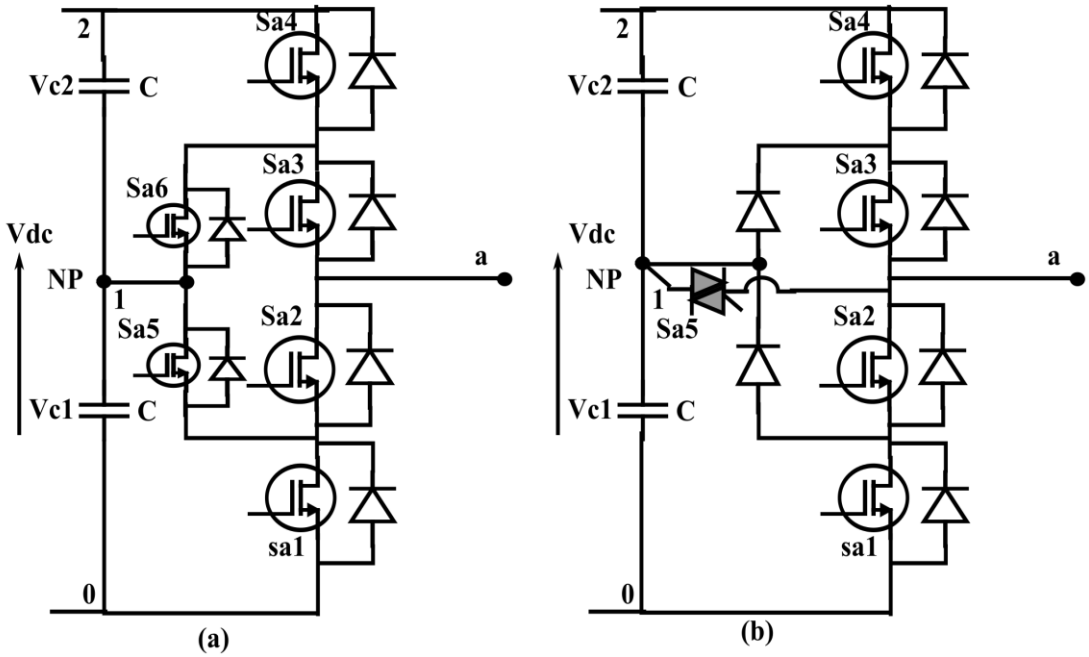

Fig. 1.13 NPC Fault tolerant converter leg (a) Solution I [53], (b) Solution II [54]

The four-leg three phase two-level inverter topology is shown in Fig. 1.14 (a). It requires two additional IGBTs, three TRIACs, and six fast-acting fuses. The fourth leg is inoperative for normal operation. The purpose of TRIAC is to isolate the faulty- leg as well as for connecting the fourth leg under fault condition. If a short-circuit fault occurs in any switch of the leg A, the fuses F1 and F2 will blow when the complementary switch turns ON. The requirement for selecting the power device is that the integral current square of the fuses and must be less than the tolerable value of the power switch. Because the faulty leg is replaced by the fourth leg, it must be controlled as if it were the isolated faulty leg. Therefore, space vector modulation (SVM) modification is not required. Fig. 1.14 (b) shows the four-leg

inverter circuit after a fault has occurred in phase A. The disadvantages of these topologies are using extra circuitry to make the system fault tolerant.

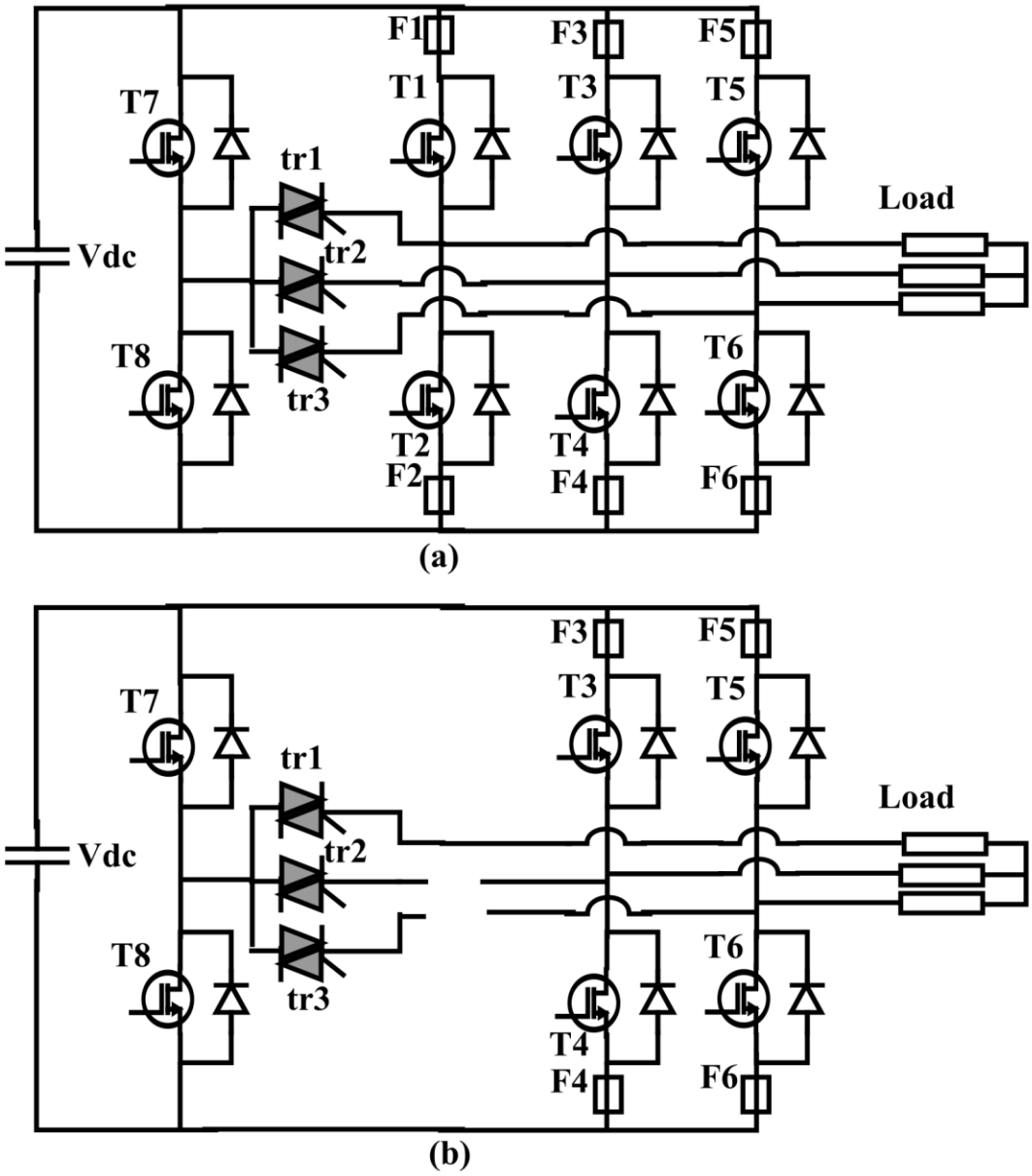

Fig. 1.14 (a) Fault tolerant solution for three phase two level inverter (b) Three phase two-level inverter after post fault [55]

1.5 Energy Balancing issue of Multilevel inverters for Stand-alone Photovoltaic systems

The block diagram of multilevel inverter with multiple PV strings with MPPT charge controller and associated batteries are shown in Fig. 1.15. The multilevel

inverters like diode clamped and cascaded H-bridge multilevel inverters are more popular for PV applications [56-58]. But, there may be a chance of energy unbalance between sources due to partial shading of PV panels and/or switching selection to generate multilevel voltages. A case study is explained for five level diode clamped inverter is shown in Fig.1.5 with four separate sources with equal power rating. Assume each source as separate PV string with battery backup. If there is partial shadow on any one of the PV string the corresponding batteries will charge and discharge unevenly. The battery with low state of charge (SOC) will dry out faster and causes total system shutdown, this leads to underutilization of healthier components. Another issue with diode clamped multilevel inverter is unequal share of load energy by sources. The switching combination to generate five level voltages is given in Table 1.6. From this table, it is observed that the sources V2, V3 are supplying more energy to load during Vdc/2 and Vdc/4 voltage level compared to V1 and V4. To avoid this issue, the energy balancing between sources has to be explored.

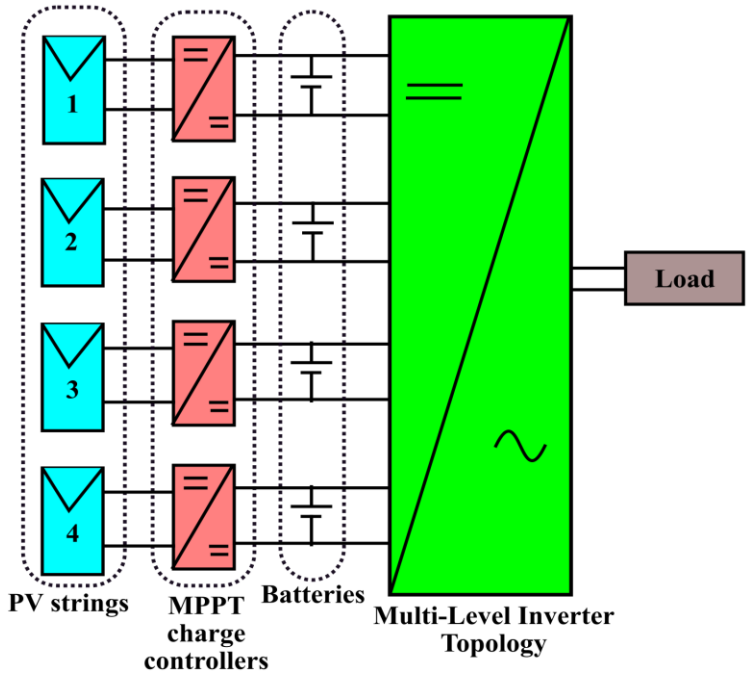

Fig.1.15 Multilevel inverter fed with multiple sources

Table 1.6

Switching sequence to generate five-level output voltage

Voltage level	S1	S2	S3	S4	S1’	S2’	S3’	S4’	Sources chosen
Vdc/2	1	1	1	1	0	0	0	0	V1, V2
Vdc/4	0	1	1	1	1	0	0	0	V2
0	0	0	1	1	1	1	0	0	0
-Vdc/4	0	0	0	1	1	1	1	0	V3
-Vdc/2	0	0	0	0	1	1	1	1	V3, V4

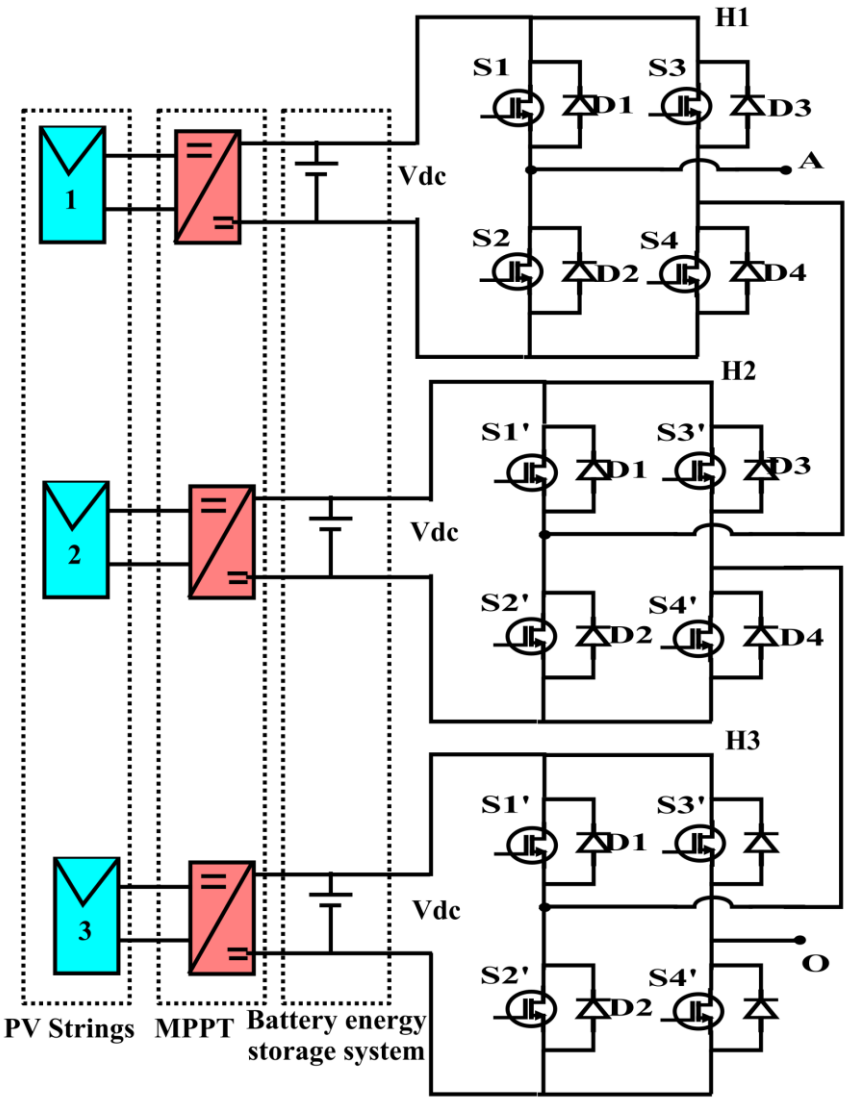

Fig.1.16 Block diagram of seven-level cascade H-bridge inverter [59]

Similar to the diode-clamped MLIs, the cascaded H-bridge inverters has limitations in terms of energy balancing issues. The energy balancing issue is addressed for seven-level cascade H-bridge inverter by using switching redundancies of H-brides in three fundamental cycles [59]. The seven-level cascade H-bridge inverter with three separate PV strings, MPPT converter and associated batteries is shown in Fig. 1.16. The gating pulses for the 7-level inverter are generated using in-phase disposition level shifted carrier pulse width modulation. The gating pulse for the each H-bridge is generated by comparing modulating signal with corresponding carrier signals. On rotation basis cyclically the pulses are applied to each H-bridge, so that the energy supplied to load by individual H-bridge is equal in three fundamental cycles. But, there is small dc voltage offset injected into ac output voltage side because of small difference in battery terminal voltage. This dc voltage offset causes saturation of transformer and other inductive loads.

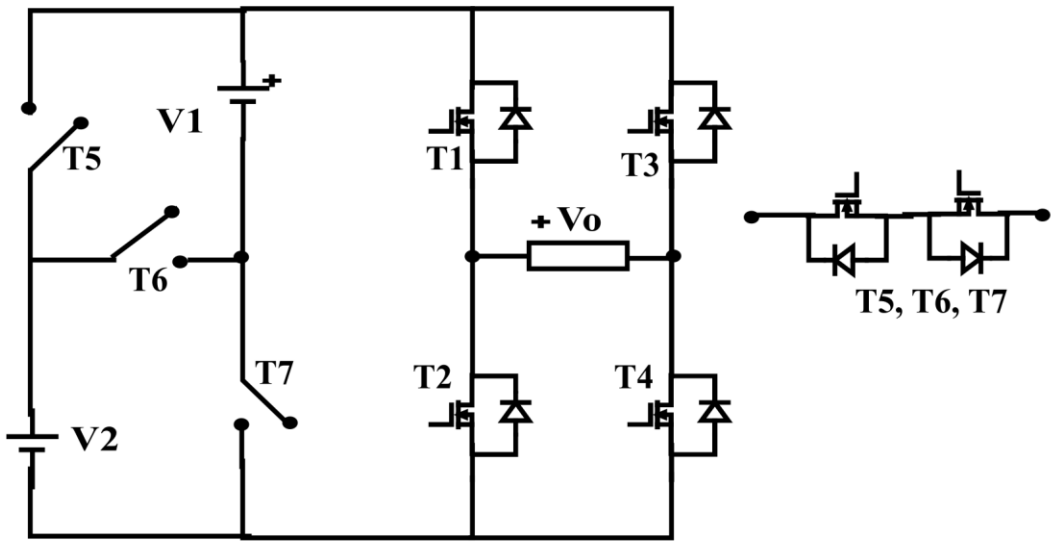

Fig.1.17 Five-level inverter topology

Fig.1.17 represents the five-level topology, which is realized by using Marx inverter structure and H-bridge. T1, T2, T3 and T4 are the H-bridge switches and T5, T6 and T7 are semiconductor switches in the Marx inverter structure [60]. T5, T6 and T7 Switches used are bidirectional to avoid their undesirable switching, short circuiting of the source and to maintain constant output voltage levels [61]. The

bidirectional switches present in this topology has low ON state voltage drop and it requires only one gate driver circuit. Considering the dc link capacitor to be charged by same rating distributed energy source, average voltage of V1 and V2 is same. The look up table for modulation scheme is shown in Table 1.7. Since both the sources deliver power to same load in alternate cycle, average value of source current for two cycles is same for both sources. Total power delivered to the load is equally distributed by both the sources in two fundamental cycles and hence power balancing among the sources is achieved. However, this topology takes two fundamental cycles to balance the power between sources and also the issues related to voltage balancing of DC sources is not addressed.

Table 1.7

Look up table for modulation scheme

V1+V2	T1, T4, T6
V1	T1, T4, T7
0	T1, T3
-V1	T2, T3, T7
-(V1+V2)	T2, T3, T6
V1+V2	T1, T4, T6
V2	T1, T4, T5
0	T2, T4
-V2	T2, T3, T5
-(V1+V2)	T2, T3, T6

1.6 Pulse Width Modulation Strategies

The modulation methods are classified based on switching frequency used for multilevel inverters, which are shown in Fig.1.18 [62], [63]. The fundamental switching modulation methods are Space vector modulation (SVM) and selective harmonic elimination (SHE) method [64], [65]. The high switching frequency modulation methods are space vector pulse width modulation (SVPWM) and sinusoidal pulse width modulation (SPWM) methods [66], [67].

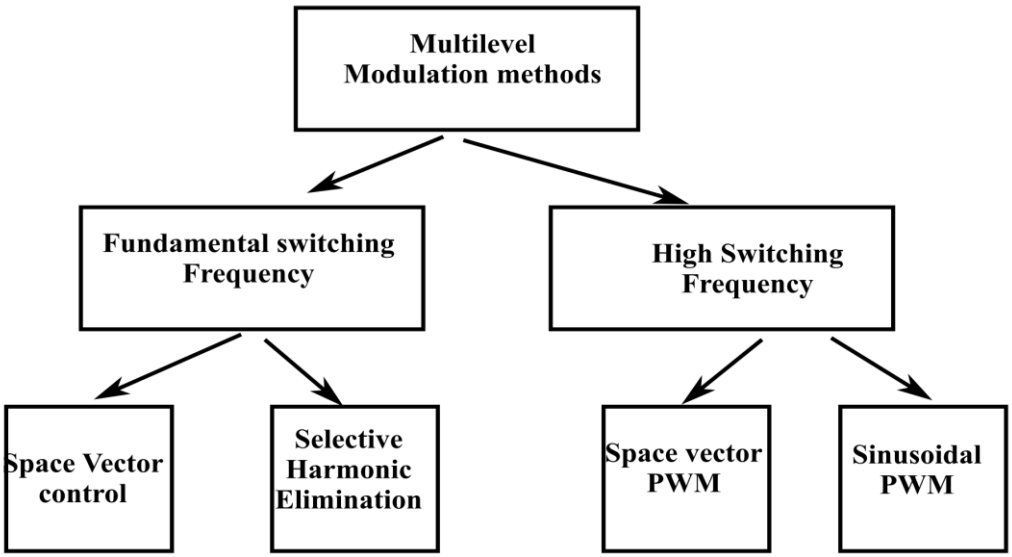

Fig.1.18 Multilevel Inverter Modulation methods

Space vector modulation (SVM) is one of the preferred real-time modulation techniques and is widely used for digital control of voltage source inverters [68], [B2].The operating status of the switches in the two-level inverter can be represented by switching states. Each pole voltage in a two-level inverter can independently assume two values namely 0 and Vdc .There are eight possible combinations of switching states in the two-level inverter which are the switching states of the inverter given as V1 (+--), V2 (++-), V3 (-+-), V4 (-++), V5 (--+), V6 (+-+), V7 (---), V8 (+++) which is depicted in Fig.1.19. In Fig. 1.19, the symbols '+' and '-' respectively indicate that the top switch and the bottom switch in a given phase leg are turned on.

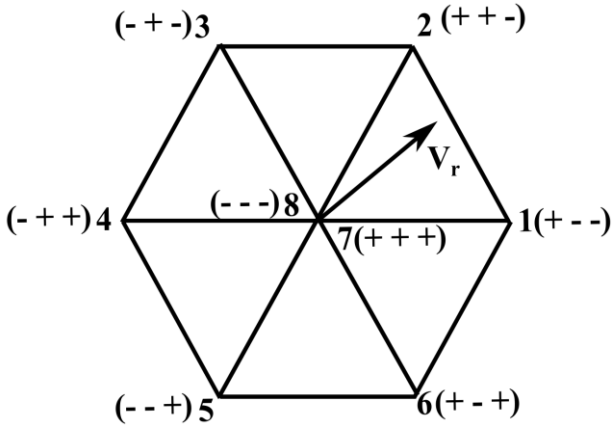

Fig. 1.19 voltage space vector diagram of three phase two level inverter

Space vector (V_r) is nothing but a resultant representation of all three phase voltage phasors given as [B3], [B4]

$$V_r = V_{AO} + V_{BO}e^{j120^0} + V_{CO}e^{j240^0} \tag{1.1}$$

The two dimensional representation of space vector is represented as

$$V_r = V_\alpha + jV_\beta \tag{1.2}$$

The relation between $V_\propto$, V_β and instantaneous phase voltages given as (1.3) and inverse transformation represented in (1.4).

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{AO} \\ V_{BO} \\ V_{CO} \end{bmatrix} \tag{1.3}$$

$$\begin{bmatrix} V_{AO} \\ V_{BO} \\ V_{CO} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & 0 \\ -\frac{1}{3} & \frac{1}{\sqrt{3}} \\ -\frac{1}{3} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{1.4}$$

From the Fig.1.19 (voltage space vector diagram), it can be observed that, all the three poles of the inverter are connected to the same node for voltage vectors V7 and V8. Therefore, it is effectively shorting the load that results no transfer of power between the dc-link and the load. Hence, V7 and V8 are known as zero voltage vectors. In case of the remaining six vectors, power gets transferred between the dc-link and the load. Therefore, these voltage vectors (V1, V2, V3, V4, V5, and V6) are known as active voltage vectors.

Sinusoidal carrier pulse width modulation technique is very popular method for industry applications for generating multilevel output voltage [69-71]. The three different carrier pulse width modulation techniques for generating odd number of voltage levels are alternative phase opposition and disposition, phase opposition disposition and in-phase disposition pwm technique [B5]. In this carrier pulse width modulation technique sinusoidal reference signal is compared with triangular carrier signal to generate pulses to the semiconductor switches. The three different carrier

modulation techniques for generating five level output voltage is shown in Fig.1.20. Here the modulating signal is compared with four triangular carriers to generate five-level output voltage across load.

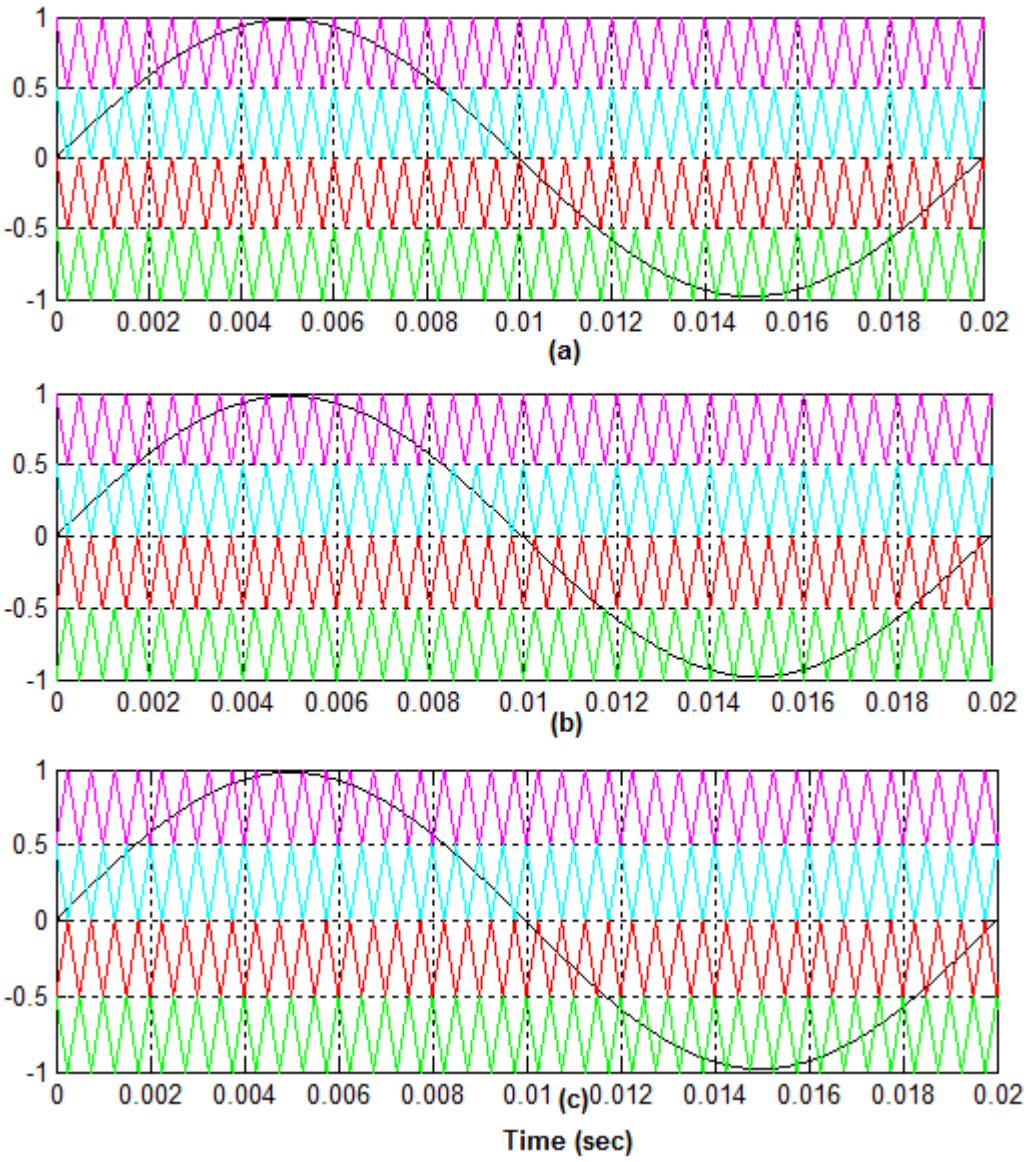

Fig. 1.20 Different carrier pwm techniques (a) In phase disposition (b) Phase opposition (c) Alternate phase opposition disposition

1.7 Scope of the thesis

This thesis presents different fault tolerant multilevel inverter topologies (fault tolerance for different switch open circuit faults and source failures) with energy balancing techniques for off-grid PV applications. In literature many multilevel

inverters with fault tolerance are presented, but these topologies have limitations in terms of more semiconductor devices and source failure conditions are not discussed. Moreover, the energy balancing issues due to the unequal load sharing or partial shading of PV panels and the issues related to dc-offset minimization are need to be explored.

In chapter one, importance of renewable energy sources and the advantages of multilevel inverters over two-level inverter is presented. The operation of five-level conventional NPC and FC multilevel inverters are explained, but these MLIs are suffers from fault tolerance and capacitor voltage balancing issues. If a source or switch fails in these topologies complete system has to be shutdown. For improving the reliability of system many fault tolerant MLI topologies are presented in the literature. The energy balancing issue of multilevel inverters for stand-alone PV systems is discussed.

In second chapter, fault tolerant single phase five-level inverter for off-grid PV applications formed by using two-level T-type half bridge inverter and three level diode clamped inverter is presented. The proposed topology has a fault tolerant capability for switch open-circuit fault or source fault or complete leg fault. This topology is extended to three phase system. This topology is modified for improving the reliability, which is formed by full bridge with two bidirectional switches. The fault tolerant operation is extended to dual inverter configuration fed to open end transformer. All these topologies are analyzed for different switch open circuit faults and source failures.

In chapter three, the energy balancing issues of the single-phase and three-phase five-level inverters during partial shading of PV panels are addressed. In these topologies the load is supplied by two separate PV strings with associated batteries. Mathematical analysis is presented for calculating the energy associated with each voltage level. In addition, the energy supplied by individual source is adjusted according to the availability of energy at individual source. The dc-off set issue is also addressed in this chapter by controlling the SOC of the batteries.

In fourth chapter, a nine level inverter with optimal PV panel distribution is presented. The energy associated with each individual source is analyzed for different possible switching combinations of this inverter. Based on this analysis proper switching combination is selected for distributing the PV panels according to the input voltage variations. The nine-level inverter topology is modified to improve the reliability and also the equal load sharing between sources is presented.

All the above presented topologies are simulated using MATLAB/SIMULINK and tested on a laboratory prototype.

Chapter 2

Fault Tolerant Multilevel Inverter Topologies

2.1 Introduction

As discussed above the off-grid PV generation system is a preferable choice for electrification option for geographically remote areas and islands which are far from the grid [72]. The faults in these systems such as source and switch failure may cause overall system shut down and take longer time to recover. These issues bring in the need of fault-tolerant converters for PV generation systems to provide continuous power to essential loads. It is known that majority of conventional multilevel inverters [10] and [11] are with limited switching redundancy lead to incompetent in addressing the issues like fault tolerant. To address some of the aforementioned issues, many multilevel inverter topologies are presented in literature with reduced number of devices for PV generation systems and drive applications [74]–[77]. Where these topologies proposed by reducing the switch count compared to conventional MLI's, but the problem of reliability in fault condition is not addressed. The survey of fault-tolerant techniques for three-phase two-level and multilevel inverters is discussed in [78].

To address the above issues, in this chapter single phase and three phase five level inverters are presented for remote and offshore PV applications. These topologies are having two equal separate PV strings rated half of the total power rating as compared to single centralized PV inverter. Advantage of having two separate PV strings are reduced switch rating as the total dc link voltage is divided in to half. These inverter configurations are realized by using two-level half bridge inverter, three-level diode clamped inverter and T-type full bridge inverter. This fault tolerance is also extended to open end winding concept of dual inverter

configuration. In case of open circuit fault or source failure condition, the faulty switch or source is bypassed by using redundant switching combinations.

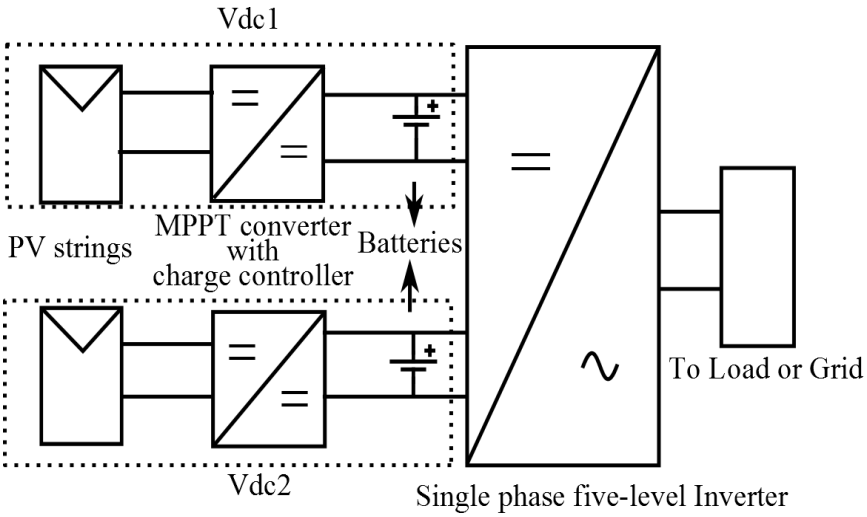

Fig. 2.1 The proposed fault tolerant single phase five-level inverter

2.2 Fault tolerant single phase and three phase five-level inverter

The block diagram of the proposed fault tolerant single phase five-level inverter circuit is shown in Fig.2.1. The configuration consists of two separate PV strings, MPPT converter with charge controller and associated batteries forming two DC links for the proposed five-level inverter, which are rated at half of the total power rating. The PV array consists of modules which has series and parallel connected cells is modelled using equation (1) [79]. The maximum power is tracked using perturb and observe algorithm given in [80].

$$I_{sa} = N_p I_{ph} - N_p I_{sat}\left\{\exp\left(\frac{V_{sa}}{N_s K_o} + \frac{I_{sa} R_s}{N_p K_o}\right) - 1\right\} - \frac{1}{R_{sh}}\left(\frac{V_{sa}}{N_s} + \frac{I_{sa} R_s}{N_p}\right) \quad (2.1)$$

Where I_{sa}, V_{sa} are module output voltage and current, each module has N_p, N_s parallel and series connected cells. R_s, R_{sh} are series and shunt resistances. I_{ph} is light generated current and I_{sat} is cell reverse saturation current. $K_o = AKT/q$, Where *A* is ideality factor, *K* is Boltzmann's constant, *T* is cell temperature and q is electronic charge.

The proposed five-level inverter configuration is formed by connecting a three-level neutral-point-clamped inverter to one side of the load, and the other side of the load is connected with a two-level half-bridge inverter depicted in Fig.2.2. The

bidirectional switch Sx5 is connected between the neutral point of two sources and the single leg of the half-bridge inverter.

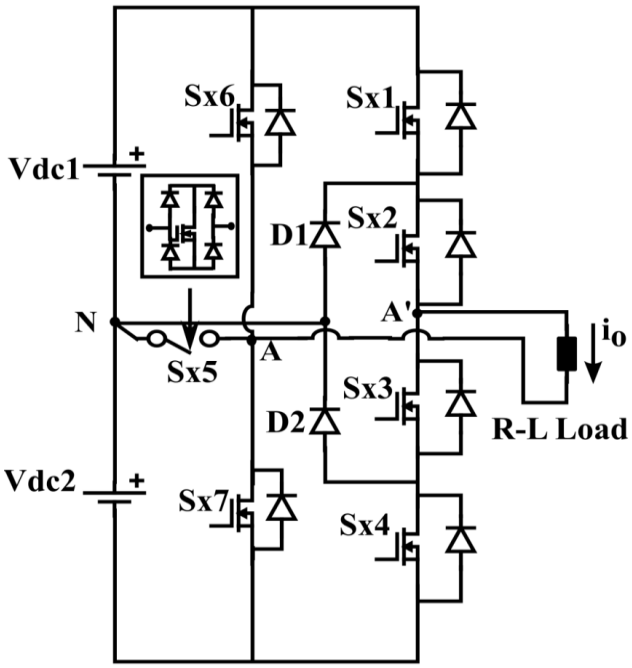

Fig. 2.2 The proposed fault tolerant single phase five-level inverter

For better understanding, the topology is supplied by two equal dc links Vdc1 and Vdc2, respectively. It is known that a leg of a three-level inverter is capable of generating voltage levels of Vdc1, 0, and − Vdc2; similarly, the two-level half bridge inverter can generate two voltage levels with magnitudes of Vdc1 and − Vdc2. As a result in combining both, the total effective voltage across the load will have a total of five voltage levels with magnitudes of +(Vdc1 + Vdc2), Vdc1, 0, − Vdc2, and − (Vdc1 + Vdc2). If two dc links are balanced to be of equal magnitude Vdc1 = Vdc2 = 0.5Vdc, then it will generate five voltage levels +Vdc, +0.5Vdc, 0, − 0.5Vdc, and − Vdc like the conventional multilevel inverter. The switching combination for five-level voltage generation and direction of current during each voltage level is given in Table 2.1 and illustrated in Fig. 2.3 (a)–(j). The switch Sx5 provides switching redundancy for voltage levels 0.5Vdc , 0, and − 0.5Vdc which can help in the energy sharing between two sources due to partial shading on one side of the PV panels which is discussed in next chapter. The same configuration is extended to three-phase operation with fault tolerance shown in Fig.2.4. The three phase fault tolerant multilevel inverter schematic is shown in Fig.2.4. The inverter structure is formed by

combining three phase two-level inverter, three-level neutral point clamped inverter and bidirectional switches. The inverter is fed with two individual DC links which consists of PV strings with MPPT charge controller and associated batteries. The total rated power is divided into halve among two PV strings. The configuration has a common connection point 'N' between sources Vdc1 and Vdc2. The bidirectional switches are connected between common connection point and two-level inverter as depicted in Fig.2.4. Phase A of two-level inverter and A' of diode clamped inverter are connected to three phase transformer winding A-A' to generate five-level voltage as shown in Fig.2.4. Similarly other phases are connected between B-B' and C-C'. The secondary side of transformer is connected in star to supply three phase or single phase loads.

The additional advantage of bidirectional switch Sx5 is to continue the operation of the inverter as three level in case of switch or source failure, which is discussed in detail at the later part of this section. From the proposed converter, it can be observed that the maximum voltage rating of the switching devices Sx1–Sx5 is 0.5Vdc, and for Sx6 and Sx7 is Vdc. In Table 2.1, if SxA = 1 switch is on, SxA = 0 switch is off, where A = 1, 2. . . 7., x refers to a, b, c phases.

Table 2.1

Switching combination for Five-level operation

Voltage levels	Sx1	Sx2	Sx3	Sx4	Sx5	Sx6	Sx7
Higher voltage level $(+V_{dc})$	1	1	0	0	0	0	1
Middle voltage level $(+0.5V_{dc})$	0	1	1	0	0	0	1
Zero level(0)	0	1	1	0	1	0	0
	0	0	1	1	0	0	1
	1	1	0	0	0	1	0
Middle voltage level $(-0.5V_{dc})$	0	1	1	0	0	1	0
Higher voltage level $(-V_{dc})$	0	0	1	1	0	1	0

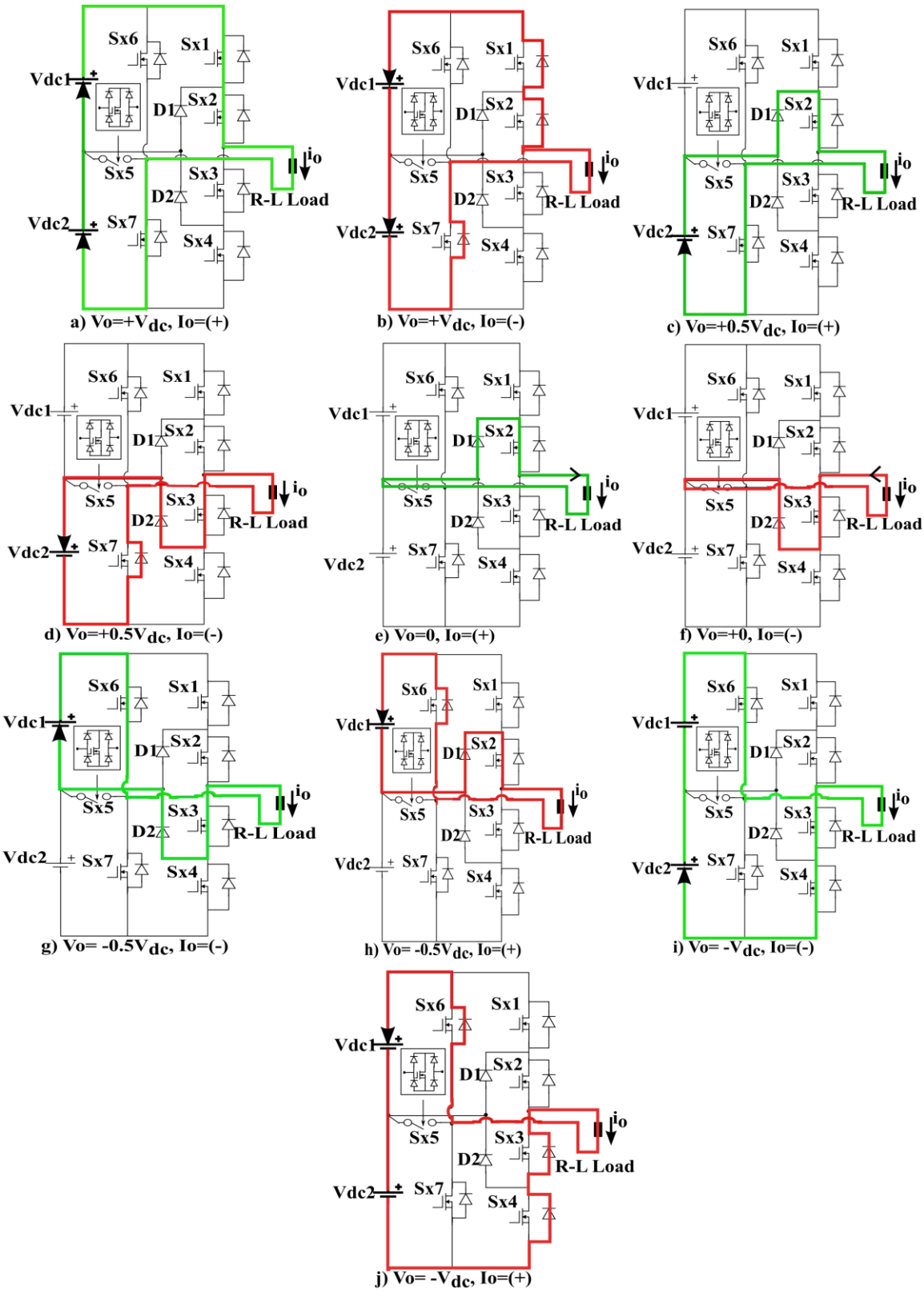

Fig. 2.3 Current direction and working state of each voltage level

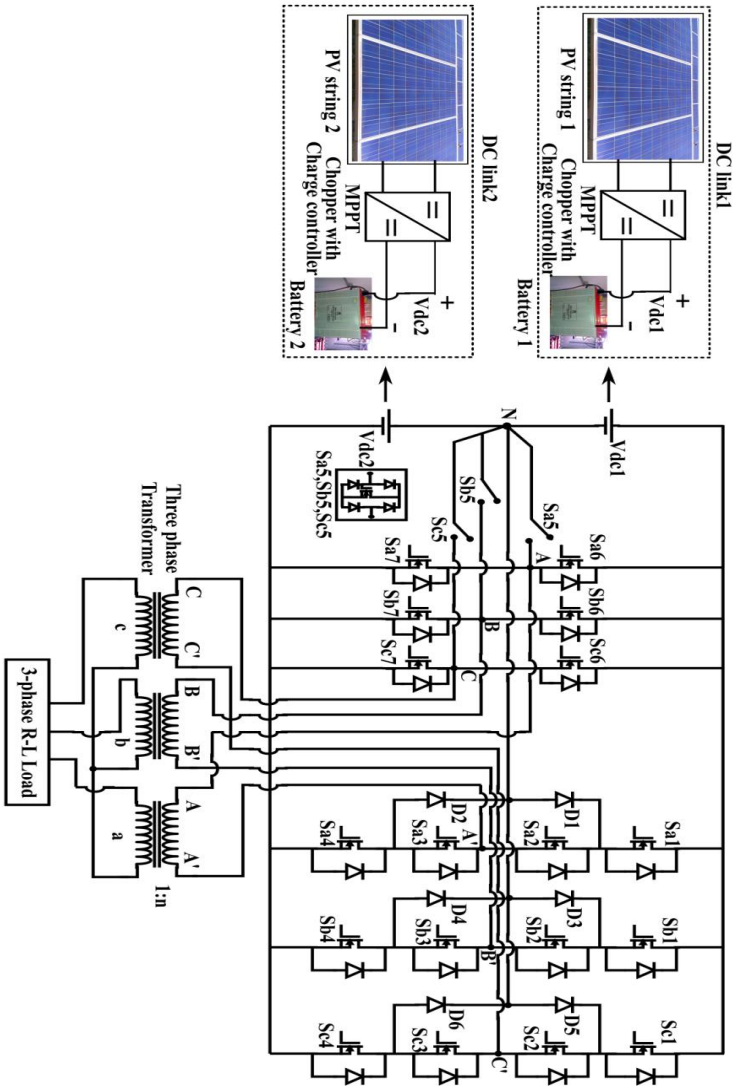

Fig. 2.4 Proposed 3-phase fault tolerant five-level inverter configuration

2.2.1 Fault analysis of five-level inverter

Generally, inverter failures are mainly due to semiconductor switch, source and driver circuit failures. The semiconductor switch failure may be open circuit or short circuit fault. In proposed configuration any one of the source short or open circuit fault, and/or switch open-circuit fault (Sx1, Sx4, Sx6 and Sx7) failure are considered. In this topology middle switching devices (Sx2, Sx3) failure is also possible by replacing clamping diodes D1, D2 with two extra switches. The possible switching combination for failure of source and/or switch is given in Table 2.2.

In case of failure (source or switch) only one source will be active and the total power supplied by the source is half at half of the rated voltage, therefore to

avoid the overloading on inverter load management is suggested. During fault the topology will be operated as three-level inverter and the output voltage is maintained at rated value by using the center tap transformer at the load side as shown in Fig.2.5. Whenever fault occurs control signal will be given to relays S8 and S9 such that the primary turns of the transformer reduces to half and maintains the volt/turn ratio constant which results rated voltage at secondary side of transformer. In some of the applications like electronic gadgets and LED's have the capability to operate at wide range of voltage variations i.e., at below half of the rated voltage which avoids the use of center tap transformer at the secondary side.

Table 2.2
Switching Combination To Generate Three-Level Voltage During Fault

Case-I Vdc2 Source open or short circuit fault and/or Sx4 or/and Sx7 Switch Open fault							
Voltage levels	Sx1	Sx2	Sx3	Sx4	Sx5	Sx6	Sx7
$+0.5V_{dc}$	1	1	0	0	1	0	0
0	0	1	1	0	1	0	0
$-0.5V_{dc}$	0	1	1	0	0	1	0
Case-II Vdc1 Source open or short circuit fault And/or Sx1 or/and Sx6 Switch Open fault							
$+0.5V_{dc}$	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0
$-0.5V_{dc}$	0	0	1	1	1	0	0
Case-III (Sx6 and Sx7 Open circuit fault)							
$+0.5V_{dc}$	1	1	0	0	1	0	0
0	0	1	1	0	1	0	0
$-0.5V_{dc}$	0	0	1	1	1	0	0

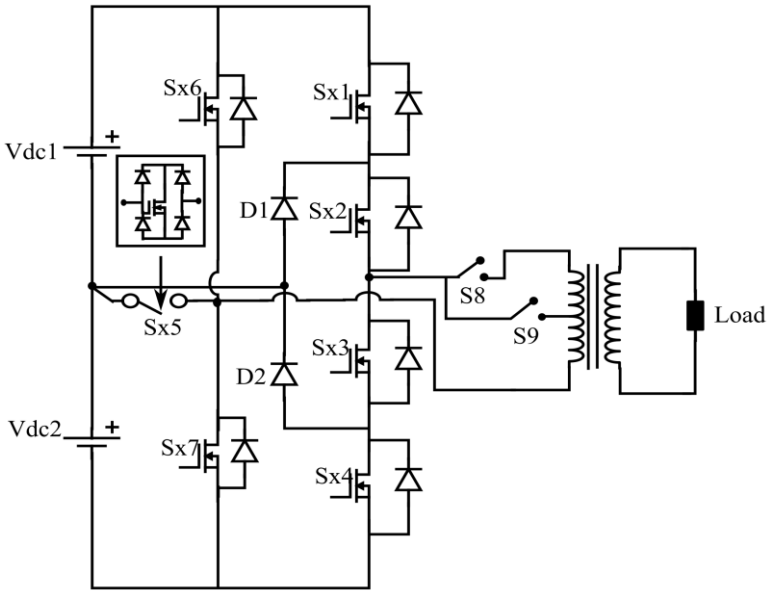

Fig. 2.5 The proposed fault tolerant single phase five-level inverter with center tap transformer

2.2.2 Pulse width modulation technique (PWM) and comparison with single phase five-level inverters

The gating pulses are produced to generate five-level voltage using phase disposition carrier pulse width modulation as shown in Fig.2.6. When the modulating signal (sine wave) (Vm) is compared with upper triangular wave (Vm>Vtri1) and lower triangular wave (Vm<Vtri4) higher voltage levels ($V_{dc}, -V_{dc}$) are generated using switching Table 2.1. If modulating signal compare with middle triangles (Vm>Vtri2, Vm<Vtri3) middle voltage levels ($0.5V_{dc}, -0.5V_{dc}$) are generated which has redundancy in switching selection using Table 2.2. Zero voltage level is generated using minimum switching combination given in Table 2.1. In case of fault the modulating wave will become half and compare with two inner carriers (Vtri2 and Vtri3). The corresponding three level voltages are generated using Table 2.2.

The number of components for proposed topology is compared with five-level neutral point clamped, flying capacitor, H-bridge multilevel inverters, and topology presented in [51] as shown in Table 2.3. The topology presented in [51] has fault tolerance for six clamping devices (Sc1-Sc6) open fault but it requires total of 22 semiconductor devices for fault tolerance. But, the proposed topology requires 7 switches and has fault tolerance for maximum of four device failure (Sx6, Sx7, D1 and D2). From Table 2.3 it is clear that the proposed topology requires less number of switches and clamping diodes than conventional topologies.

Table 2.3
Number of Components for Single Phase Five-Level Inverter

Type of Components	Number of components required				
	In Conventional Topologies			Topology Proposed in [51]	In Proposed topology
	NPC	Flying capacitor	H-bridge		
Main switches	8	8	8	22	7
Main diodes	8	8	8	22	10
Clamping diodes	12	0	0	0	2
DC bus capacitors/ Isolated supplies	4	4	2	1	2
Flying capacitors	0	6	0	7	0
Switch open circuit fault capability	No	No	Yes	Yes	Yes
Source failure capability	No	No	Yes	No	Yes

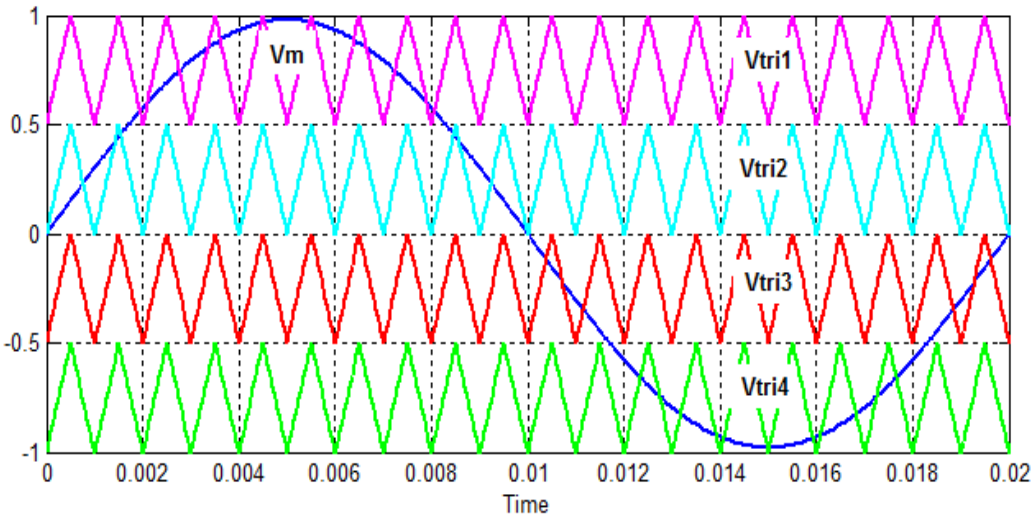

Fig. 2.6 Phase disposition carrier pulse width modulation technique

2.2.3 Single phase five-level inverter Results and Discussion

A. Simulation Results

The proposed fault tolerant single phase five-level inverter is simulated using MATLAB/Simulink for R-L load at rated output voltage of 120V rms. The parameters for single phase five-level inverter are given in Table 2.4.

Table 2.4
Parameters for Simulation and Laboratory Prototype

Rated battery voltage (Lead acid)	$Vdc1 = Vdc2 = 96V$
Rated output voltage	120V
Modulating wave frequency	$f_m = 50Hz$
Switching frequency	$f_s = 1kHz$
Modulation index	$m_a = 0.9$
Load Resistance, inductance values	$R = 78\Omega, L = 50mH$

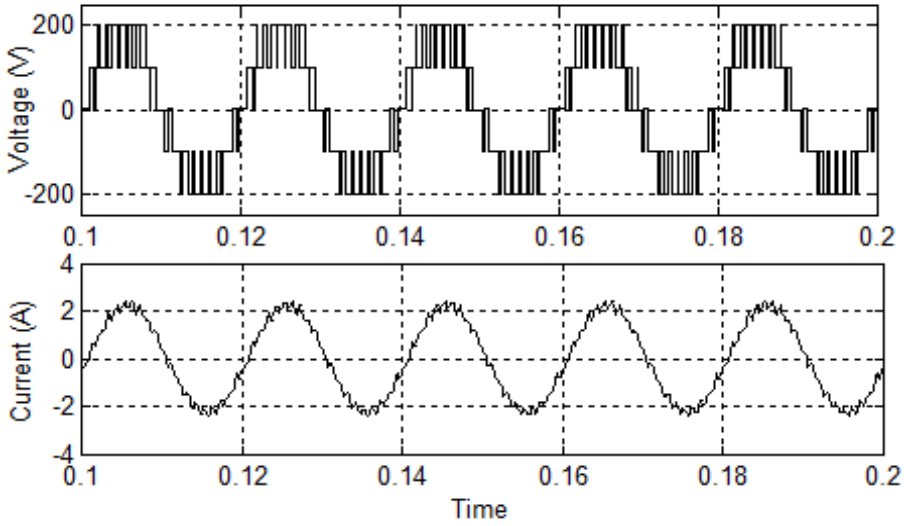

Fig. 2.7 Output voltage (upper trace) and current (bottom trace) waveforms of five-level inverter

The five-level output voltage waveforms across the load and current through the load are shown in Fig. 2.7 for a modulation index of 0.9. Fig. 2.7 clearly shows five voltage levels and nearly sinusoidal load current waveform. In Fig. 2.8, after 0.15 s, the fault is created, and the voltage transition from five level to three-level is shown and also demonstrates that the voltage and current magnitudes are reduced. The rated output voltage of the inverter is maintained by using a primary center tap single-phase transformer, and the corresponding waveforms are observed in Fig. 2.9. From this figure, after 0.17 s, the fault is created, and the conversion of the voltage waveform from five level to three-level with the same magnitude can be observed.

The magnitude of the current waveform is reduced by suggesting proper load management to avoid overloading on the inverter, which is observed from Fig.2.9. At the time of fault, the primary turns of the transformer become half by using the combination of S8 and S9 relays and maintain the volt/turn ratio constant, which results to rated voltage at the secondary side of the transformer.

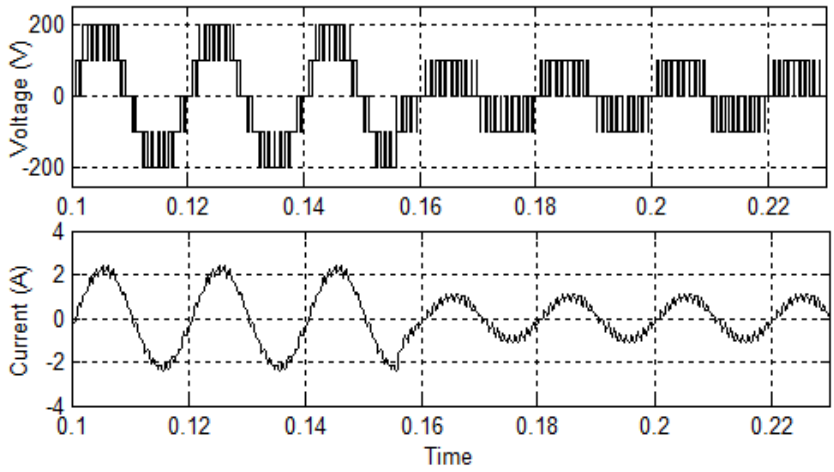

Fig. 2.8 Output voltage and current waveforms of proposed inverter due to Vdc2 source failure

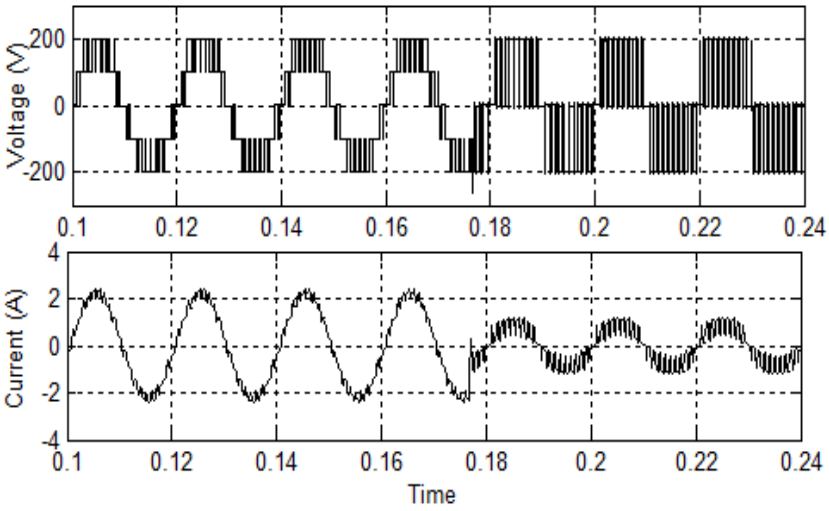

Fig. 2.9 Output voltage and current waveforms with transformer due to Vdc2 source failure

B. Experimental Results

The proposed fault tolerant single phase five-level inverter is tested using laboratory prototype with lead acid batteries for R-L load. The control and PWM schemes are implemented using dSPACE 1104 real time controller. A delay of 2μs is provided between the complimentary switches using external deadband circuit.

In Fig.2.10 upper trace shows five-level output voltage and bottom trace shows current through load during normal operation. Fig.2.11 clearly shows the conversion of five-level output waveform to three-level with reduced voltage magnitude and current during Vdc2 source failure. Fig.2.12 shows the five-level to three-level output voltage and current waveforms during source Vdc2 failure. The rated output voltage of inverter is maintained by proper combination of relays S8, S9 connected primary side of center tap transformer. Fig.2.12 shows the magnitude of output voltage is remain unchanged and proper load management is suggested to avoid overloading on inverter.

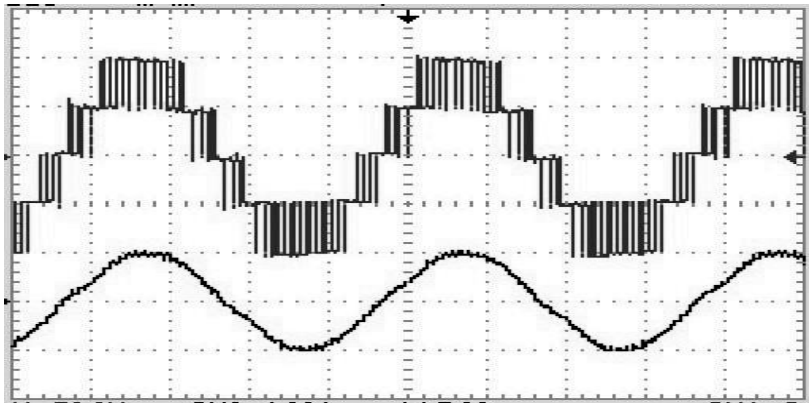

Fig. 2.10 Five level output voltage (upper trace) and current (bottom trace) waveforms of proposed inverter [Y-axis 100v/div, 2A/div; X-axis 5msec/div]

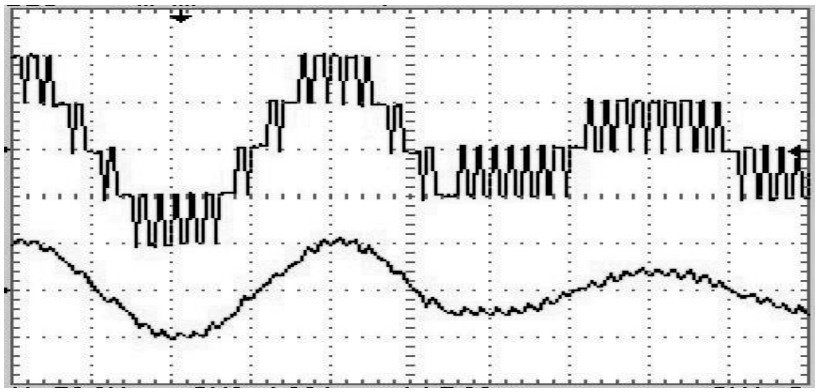

Fig. 2.11 Output voltage (Upper trace) and current (lower trace) waveforms of proposed inverter during Vdc2 source failure [Y-axis 100v/div, 2A/div; X-axis 5msec/div]

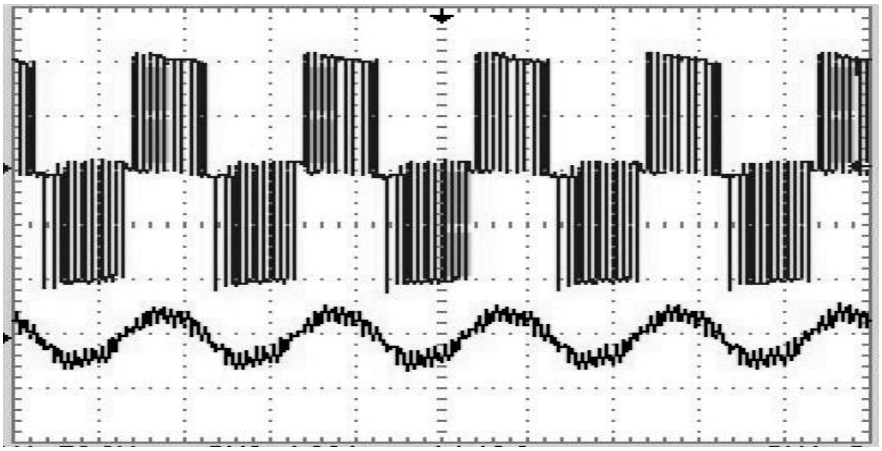

Fig. 2.12 Output voltage (Upper trace) and current (lower trace) waveforms of proposed inverter during Vdc2 source failure with transformer [Y-axis 100v/div, 2A/div; X-axis 10msec/div]

2.2.4 Three phase five-level inverter Results and Discussion

A. Simulation Results

The Matlab simulation parameters for proposed configuration are given in Table 2.5. PV array and maximum power point tracking is modelled using reference given in [79], [80]. In Fig.2.13, the upper two traces are pole voltage of two-level inverter and three-level diode clamped inverter during normal mode of operation. The middle trace shows the induced five-level voltage across primary side winding of three phase transformer. The bottom two traces are line voltage and load current waveforms at load side.

Table 2.5

Parameters for Simulation

Rated Lead acid battery voltage	$Vdc1 = Vdc2 = 96V$
Modulating signal frequency	$f_m = 50Hz$
Switching frequency	$f_s = 2kHz$
Modulation index	$m_a = 0.9$
Load Resistance, inductance values	$R = 150\Omega, L = 40mH$

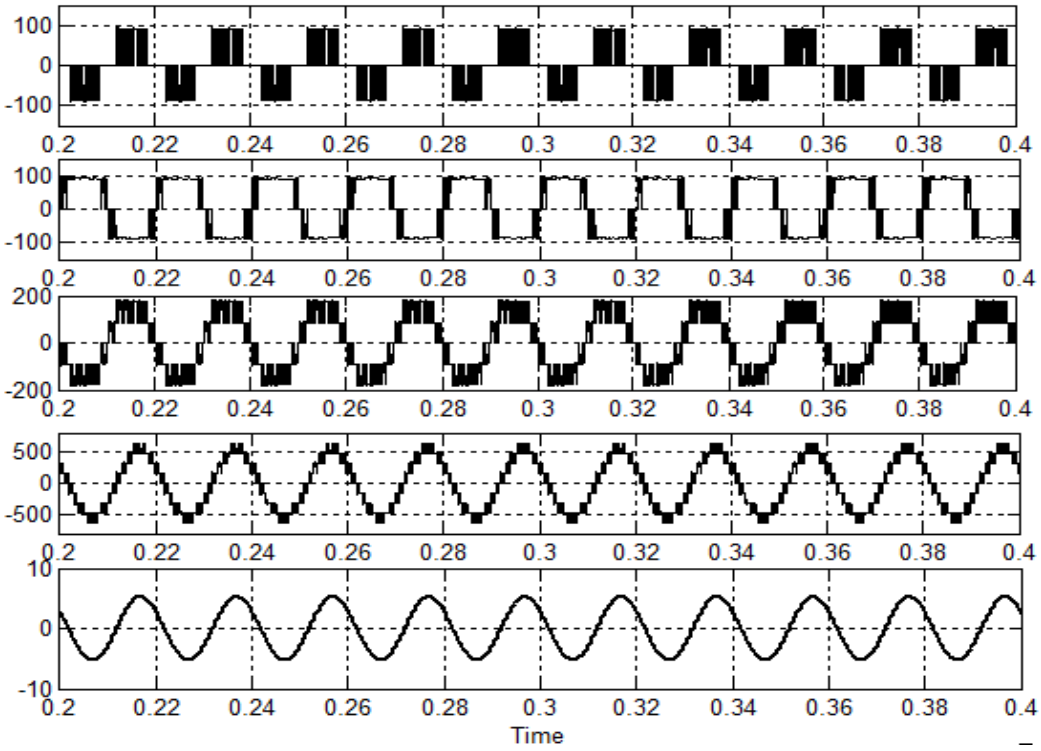

Fig.2.13 Pole voltage of two-level (V_{AN}) and diode clamped inverter ($V_{A'N}$), induced five-level voltage ($V_{AA'}$), line voltage and load current waveforms

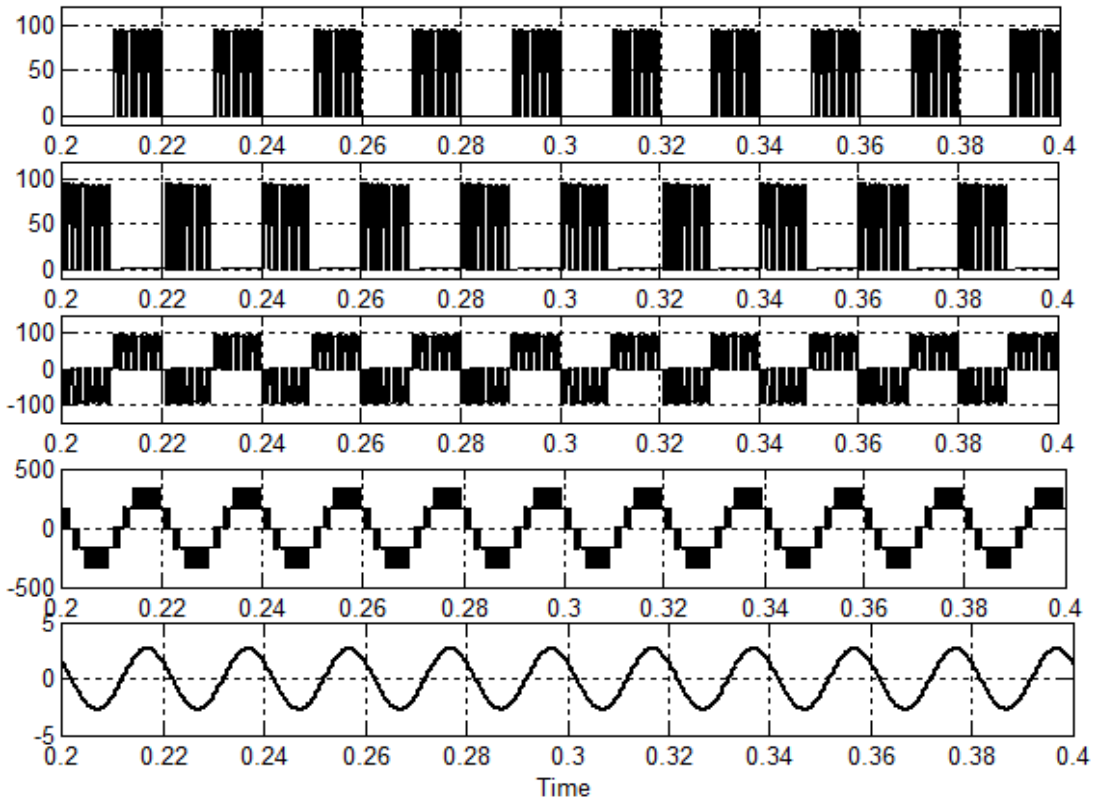

Fig. 2.14 Pole voltage of two-level (V_{AN}) and diode clamped inverter ($V_{A'N}$), induced five-level voltage ($V_{AA'}$), line voltage and load current waveforms during energy sharing mode of operation.

Fig. 2.14 shows the waveforms during fault tolerant mode of operation. The upper two traces are pole voltage of two-level inverter and three-level diode clamped inverter. The middle trace shows the induced three-level voltage across primary side winding of three phase transformer. The bottom two traces are line voltage and load current waveforms at load side.

B. Experimental Results

The prototype is tested with lead acid batteries of terminal voltage rating is 48V.The gating pulse for the proposed laboratory prototype is generated using Xilinx SPARTAN-6 (XC6SLX9) FPGA board programed in VHDL. A delay of 2.5μs is provided between the complimentary devices using dead band circuit. Fig.2.15 (a) shows five-level voltage and pole voltages during normal operation. The phase voltage across load and current through load are shown in Fig. 2.15 (b). During fault the three-level voltage across primary winding of transformer and pole voltages of two-level inverter and three-level diode clamped inverter are depicted in Fig.2.16 (a) and (b).

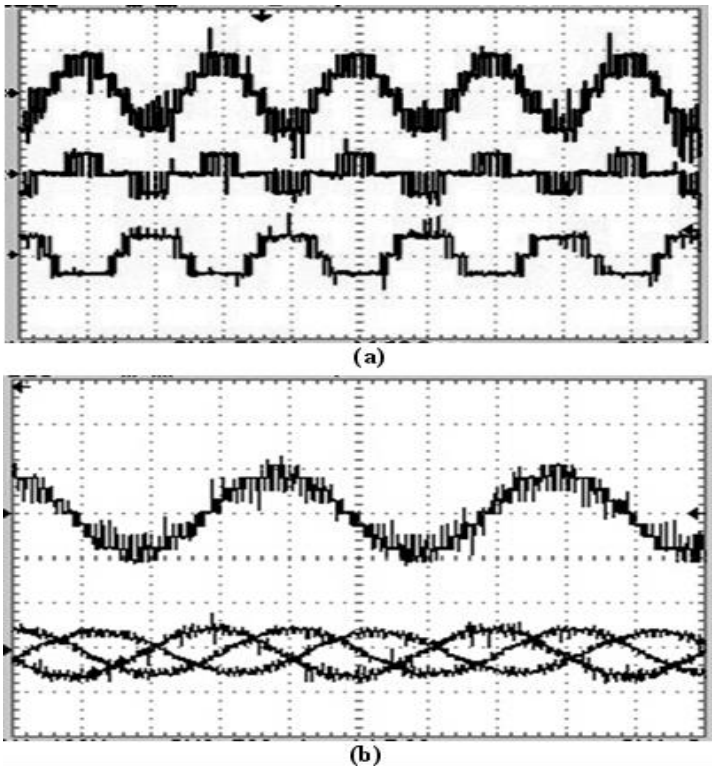

Fig. 2.15 (a) Induced five-level voltage ($V_{AA'}$) and pole voltages during normal operation ($V_{A'N}$, V_{AN}) (b) Line voltage and load current waveform. [Y-axis 100V/div, 200V/div 1A/div; X-axis 5ms,10ms/div]

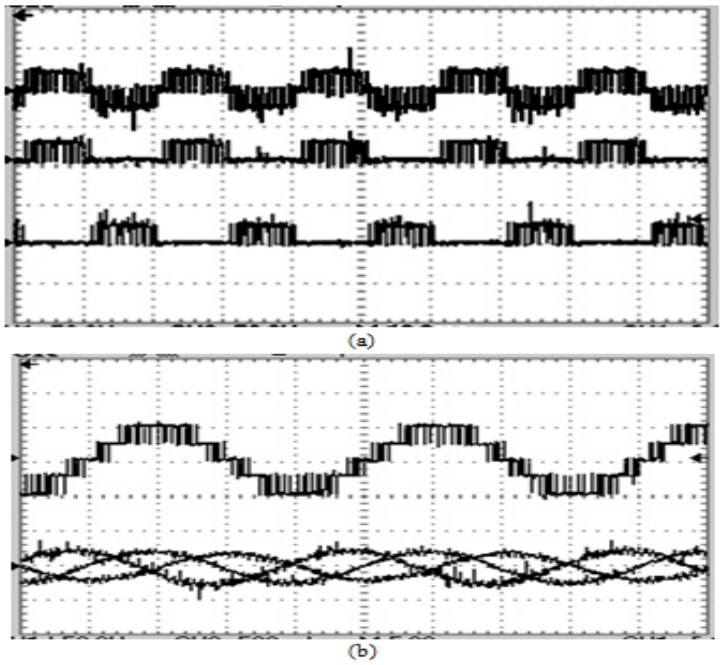

Fig. 2.16 (a) Induced three-level voltage ($V_{AA'}$) and pole voltages during fault operation ($V_{A'N}$, V_{AN}). (b) Line voltage and load current waveform. [Y-axis 100V,50V 1A/div; X-axis 10msec, 5ms/div]

2.3 Improved single phase five-level inverter Topology

An improved single phase fault tolerant five level inverter configuration is formed by single phase full bridge inverter (S1, S2, S3, S4) and two bidirectional switches (S5, S6) shown in Fig.2.17. The full bridge inverter capable of generating +(Vb1+Vb2), 0 and –(Vb1+Vb2). Bidirectional switch S5 or S6 will generate +0.5Vb1 and -0.5Vb2 using full bridge configuration. The given topology assumes Vb1=Vb2=0.5V_{dc}. The combination of full bridge inverter and switch S5 or S6 will capable to generate five level output voltage (+V_{dc}, +0.5V_{dc}, 0, -0.5V_{dc}, - V_{dc}) is shown in Table 2.6. The bidirectional switch S5, S6 helps in continue the inversion during faults and also paves way for power sharing between sources. The maximum voltage rating of the switches S1-S4 is V_{dc} and for S5-S6 is 0.5 V_{dc}. In Table 2.6, 1 indicates switch is ON, 0 indicates switch is OFF.

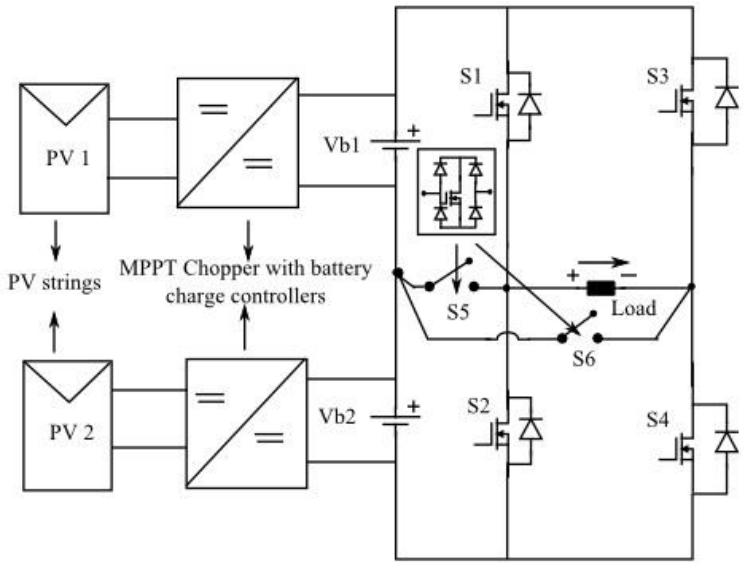

Fig.2.17 Proposed fault tolerant single phase five level inverter

Table 2.6
Switching combination for Five-level operation

Voltage levels	S1	S2	S3	S4	S5	S6
Higher voltage level ($+V_{dc}$)	1	0	0	1	0	0
Middle voltage level ($+0.5V_{dc}$)	0	0	0	1	1	0
Zero voltage level (0)	1	0	1	0	0	0
	0	1	0	1	0	0
Middle voltage level ($-0.5V_{dc}$)	0	0	1	0	1	0
Higher voltage level ($-V_{dc}$)	0	1	1	0	0	0

2.3.1 Fault analysis of Improved single phase five-level inverter

The malfunctioning of inverters is mainly due to open and/or short circuit fault of sources, switch and associated driver circuit. The proposed configuration has capability to continue its operation for open circuit switch faults and open or short circuit fault of sources. During normal operation the inverter will generate five level output voltage based on the switching combinations given in Table 2.6. In case of failure, the five-level inverter will continue the operation as three-level inverter with half of total power rating and reduced voltage magnitude

using switching combination mentioned in Table 2.7. To compensate the reduction in voltage magnitude for the critical loads requiring rated voltage, a primary center tap transformer is connected at the load side. At the time of fault the inverter is connected to the half of the primary winding there by the turns ratio is doubled at the secondary side and voltage magnitude is maintained constant.

Table 2.7
Switching Combination for Different Failure Cases to Generate Three Level Voltage

Vb2 source open and/or short or S2, S4 switch open fault						
Voltage levels	S1	S2	S3	S4	S5	S6
$+0.5V_{dc}$	1	0	0	0	0	1
0	1	0	1	0	0	0
$-0.5V_{dc}$	0	0	1	0	1	0
Vb1 source open and/or short or S1, S3 switch open fault						
Voltage levels	S1	S2	S3	S4	S5	S6
$+0.5V_{dc}$	0	0	0	1	1	0
0	0	1	0	1	0	0
$-0.5V_{dc}$	0	1	0	0	0	1
S3 and S4 switch open fault						
Voltage levels	S1	S2	S3	S4	S5	S6
$+0.5V_{dc}$	1	0	0	0	0	1
0	0	0	0	0	1	1
$-0.5V_{dc}$	0	1	0	0	0	1
S1 and S2 switch open fault						
Voltage levels	S1	S2	S3	S4	S5	S6
$+0.5V_{dc}$	0	0	0	1	1	0
0	0	0	0	0	1	1
$-0.5V_{dc}$	0	0	1	0	1	0

2.3.2 Results and Discussion

A. Simulation Results

The proposed fault tolerant single phase five-level inverter is simulated using MATLAB/SIMULINK for normal and fault operation. The simulation parameters are given in Table 2.8. The different carrier pulse width modulation (PWM)

techniques like phase disposition (PD) PWM, phase opposition disposition (POD) PWM and alternate phase opposition disposition PWM are presented for multilevel inverters to generate multilevel output voltage [81]. The gating pulses for proposed fault tolerant single phase five-level inverter is generated using phase disposition carrier pulse width modulation discussed in previous section 2.2.6.

Table 2.8
Simulation Parameters

Rated battery terminal voltage (Lead acid)	$Vb1 = Vb2 = 96V$
Modulating wave frequency	$f_m = 50Hz$
Switching frequency	$f_s = 1050Hz$
Modulation index	$m_a = 0.9$
Load Resistance, inductance values	$R = 20\Omega, L = 40mH$

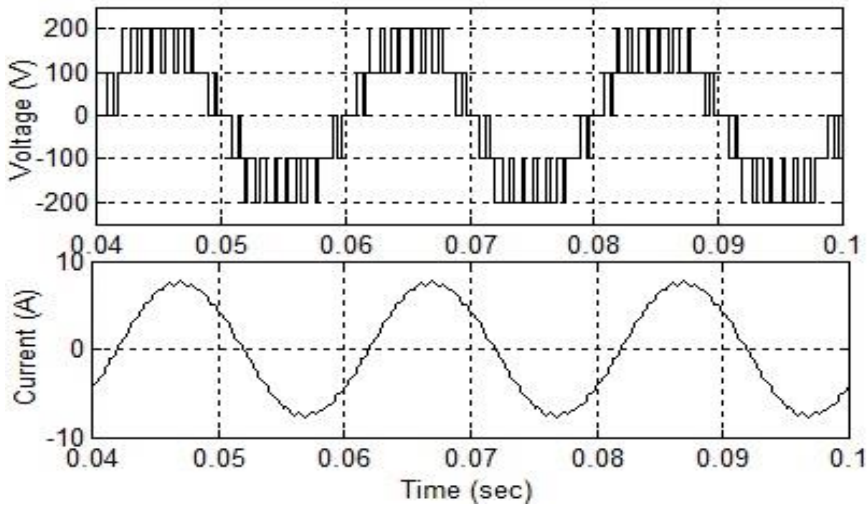

Fig. 2.18 Output voltage (upper trace) and current (bottom trace) waveforms of five-level inverter.

The Fig.2.18 clearly shows the five level output voltage across load and current through load for R-L load. From Fig.2.19 it can be observed that the distortion of load voltage and current waveforms during switch S3 open circuit fault. The Fig.2.20 shows waveforms during fault clearance by using redundant switching states as explained in the previous section. The inversion of five level output voltage to three-level at 1.277 sec with reduced magnitude.

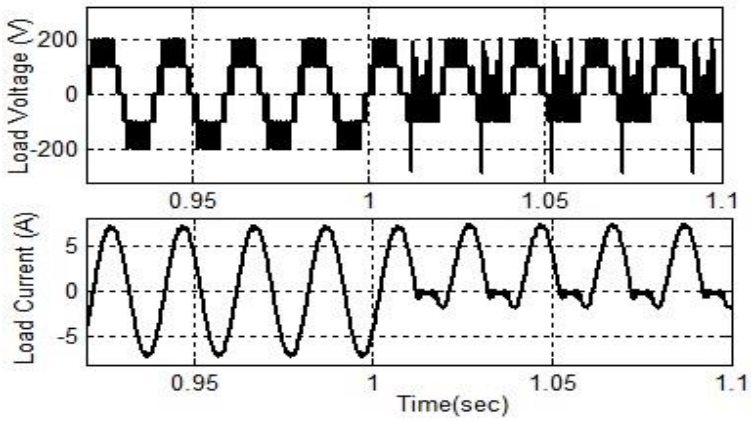

Fig. 2.19 Output voltage (upper trace) and current (bottom trace) waveforms of five-level inverter during switch S3 open circuit fault.

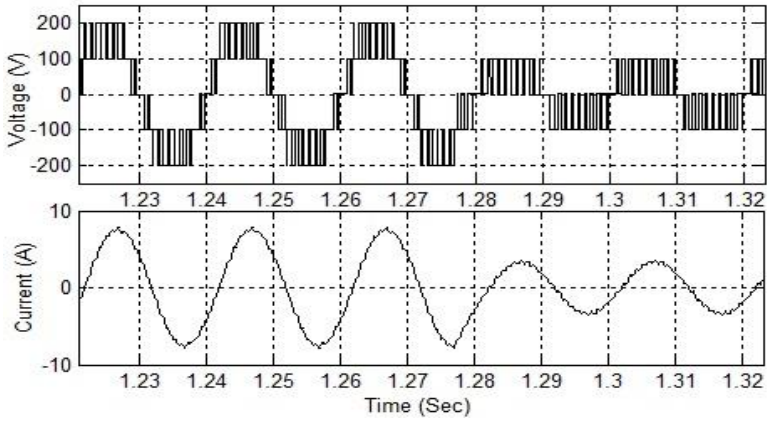

Fig. 2.20 Output voltage and current waveforms of proposed inverter after clearing switch S3 open circuit fault.

Fig.2.21 shows magnitude of three-level voltage is maintained constant as five-level by connecting a center tap transformer at the load side. The current waveform magnitude shows that over loading on inverter is avoided by disconnecting some of the unimportant loads.

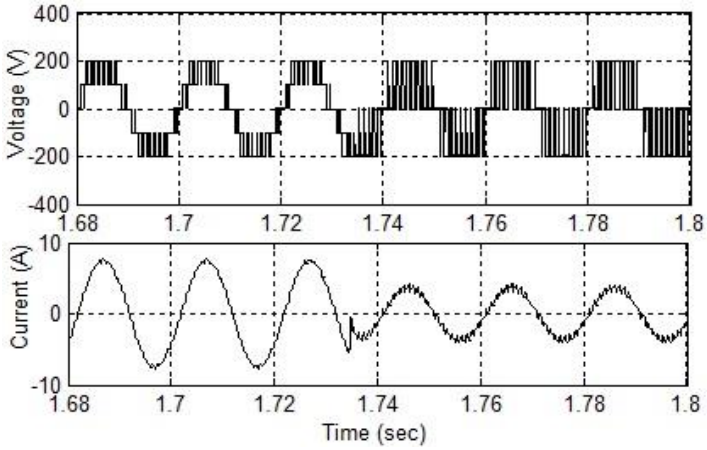

Fig. 2.21 Output voltage and current waveforms with transformer due to Vb2 source failure

B. Experimental Results

The laboratory prototype is tested with lead acid batteries with R-L load. The control technique is implemented using dSpace 1104. A delay of 2μsec is provided between complementary switches. Fig. 2.22 clearly shows the five-level output voltage and current waveform through load. Fig.2.23 shows the output voltage and current through load during switch S3 open circuit fault. From Fig.2.23 it can be observed that conversion of five-level voltage to three-level and magnitude of voltage and current waveform is reduced to half. Fig.2.24 shows the output voltage and current waveform with a center-tap transformer at the load side during fault. From Fig. 2.24 it can be observed that the magnitude of output voltage is maintained constant as in normal condition.

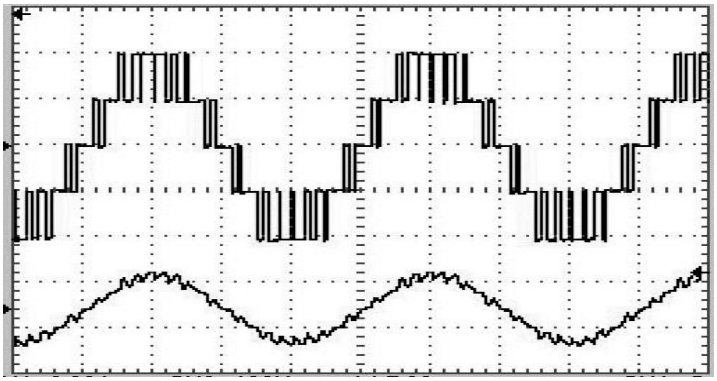

Fig. 2.22 Output voltage (upper trace) and current (bottom trace) waveforms of five-level inverter [Y-axis 100V/div, 2A/div; X-axis 5msec/div]

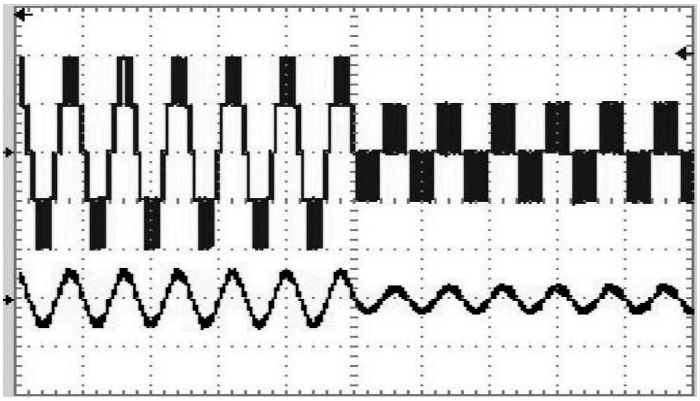

Fig. 2.23 Output voltage (upper trace) and current (bottom trace) waveform of five-level inverter during S3 open circuit fault [Y-axis 100V/div, 2A/div; X-axis 20msec/div].

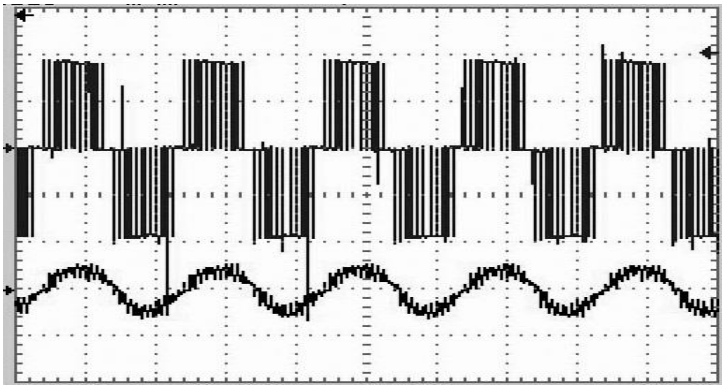

Fig. 2.24 Output voltage (upper trace) and current (bottom trace) waveform of five-level inverter with center tap transformer during switch S3 open circuit fault [Y-axis 100V/div, 1A/div; X-axis 10msec/div]

2.4 Fault tolerant Dual Inverter Configuration

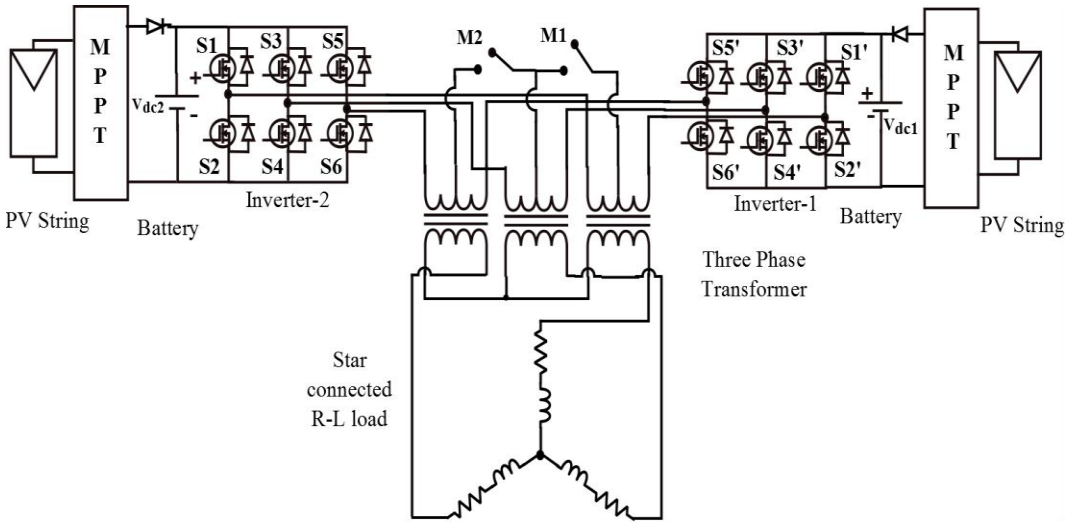

Fig.2.25 The proposed fault tolerant PV generation system.

The proposed islanded mode PV generation system consists of a two three phase two level inverters. These two inverters are supplied by two isolated PV strings with associated battery and MPPT technique. The primary windings of a three phase transformer (center tapped) are connected between the poles of dual inverters. Center tapings on primary are connected through relays as shown in Fig. 2.25. Both the two level inverters are controlled in such a way that the primary sees a three level voltage profile under normal operating condition. The required control is achieved using decoupled SVPWM method which is explained in detail in later part of this section. The secondary winding of the three phase transformer is

connected in star so that either three phase or single phase load can be supplied by the proposed system.

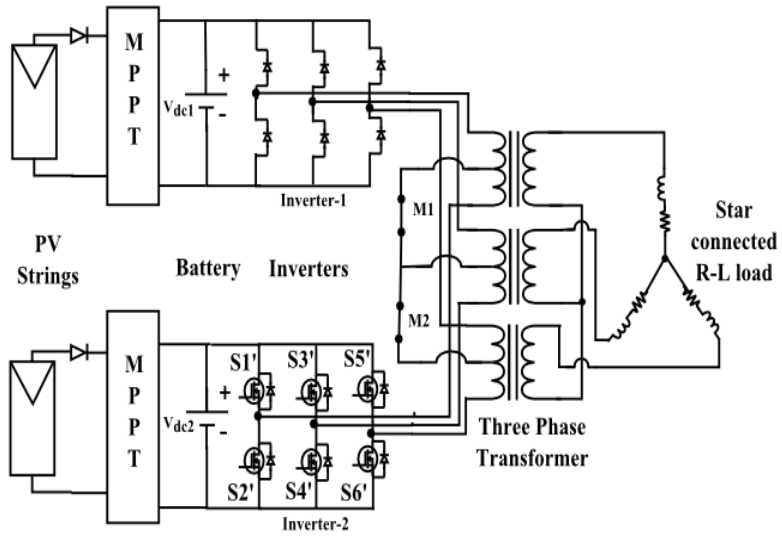

Fig. 2.26 Proposed system under fault condition

2.4.1 Fault analysis of Dual inverter configuration

In the proposed generation system mainly there are two possibilities of fault which will cause the overall system failure. One of the PV string may fail to provide the required dc link voltage due to partial shading of panels or due to some fault in corresponding MPPT block. The second possibility of fault is inverter failure because of fault in any of the switch, which can be easily detected from the driver circuit of the inverter. The semiconductor switch failures are because of short circuit or open circuit fault. In this configuration switch open circuit fault and source failure are considered. In case of fault in one of the PV string and/or the corresponding inverter, continuous system operation can still be ensured by a simple fault tolerant technique using relays. Whenever the fault occurs in any one part of the system the relays Ml and M2 are actuated by a control signal. Closure of these relays shorts the center tapings of primary windings, which in turn connects half of the primary windings in star across the healthy side inverter. The circuit under fault condition is shown in Fig. 2.26. So the volt per turn of the three phase transformer is still maintained constant as only half of the primary winding is supplied by the healthy side inverter. This arrangement effectively doubles the turn's

ratio of the three phase transformer and maintains the output voltage of the system unaltered even under fault condition.

Gate pulses for the faulty side inverter are removed to make it inoperative during fault time, which in turn avoids the magnetic locking of core. As remaining half of the primary winding is still on the same core, the voltage induced in it due to the healthy side inverter may circulate a reverse current through anti-parallel diodes. This will tries to energize the battery of faulty side inverter which is undesirable. To avoid this problem the battery associated to the faulty inverter should be disconnected, which in turn blocks the reverse current under fault condition. As the healthy side inverter is rated for half of the system rating it should not be overloaded during fault condition. To avoid overloading some of the loads are scheduled to be off during fault time.

2.4.2 Control Scheme Description

Gating pulses for the proposed fault tolerant PV generation system are generated using decoupled space vector PWM method for equal DC link voltages [82]. The total space vector reference V_r is decided depending upon the output voltage requirement. The total space vector reference V_r is divided into two smaller reference vectors V_{r1} and V_{r2} as shown in Fig.2.27. These V_{r1} and V_{r2} are the individual reference voltage space vectors for inverter 1 and inverter 2 respectively. Smaller reference vectors V_{r1} and V_{r2} are computed in the control scheme using values of battery output voltages V_{dc1} and V_{dc2} as given by equations (2.2) and (2.3) .By using decoupled space vector PWM method V_{r2} is generated 180^0 out of phase with V_{r1} which in turn makes the pole voltages of the two inverters to have 180^0 phase difference. As a result a three level voltage profile is seen by the primary of three phase transformer under normal operating conditions [83].

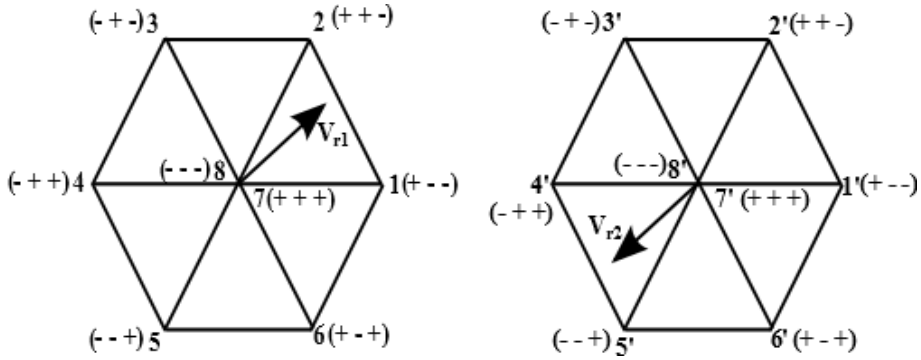

Fig. 2.27 Individual space vector references

$$V_{r1} = V_r \left(\frac{V_{dc1}}{V_{dc1} + V_{dc2}} \right) \tag{2.2}$$

$$V_{r2} = V_r \left(\frac{V_{dc2}}{V_{dc1} + V_{dc2}} \right) \tag{2.3}$$

$V_{dc\text{-}min}$ is the minimum battery voltage below which battery will not give any backup. If any one of battery voltage reduces below $V_{dc\text{-}min}$ due to failure of any one of the PV string, corresponding inverter is made inoperative by removing gate pulses to that inverter. At the same time a control signal is made high to actuate relays M1 and M2. As a result each half of the primary windings gets connected in star across the healthy side inverter and transformer turns ratio becomes double. So the generating system continues to work at same output voltage with reduced power rating. The control scheme is so designed that under fault condition V_{r1} or V_{r2} made equal to $V_r/2$ and not calculated according to equation (2.2) and (2.3). The same control can be expected even in case of the inverter switch failure. S_{f1} and S_{f2} are the switch failure signals obtained from the driver circuit of the inverters. The switch failure signals S_{f1} and S_{f2} are given to the control scheme for generating a control signal to close relays M1 and M2. The complete control scheme is represented as a block diagram as shown in Fig. 2.28.

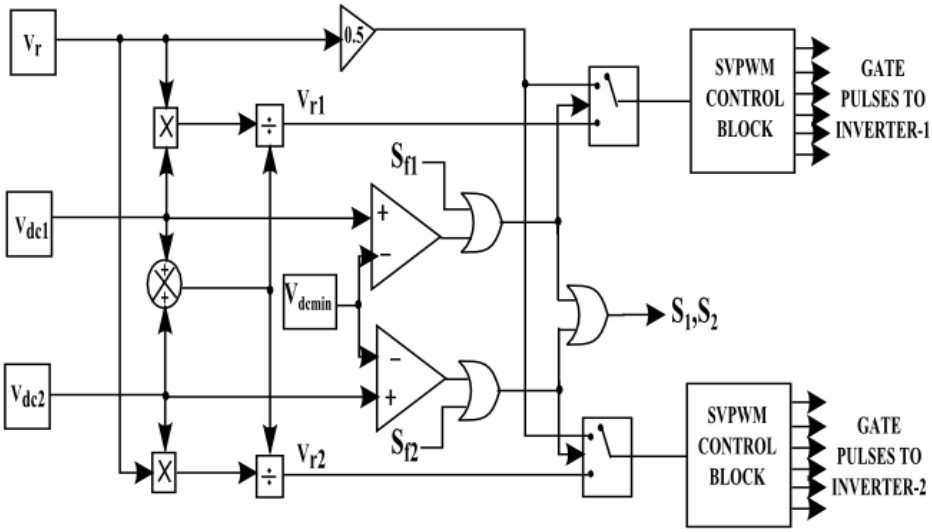

Fig. 2.28 Proposed Control Scheme

2.4.3 Results and Discussion

A. Simulation Results

The proposed system is simulated in MATLAB/SIMULINK. The PV array and maximum power point tracking is modelled using reference given in [79], [80]. Under good solar irradiation the PV string through MPPT block supplies both inverter and the battery. Battery backup will supply the inverter whenever irradiation is low. A 3.2 KW PV generation system is simulated with two inverters supplying half of the total rated power. Each inverter is supplied by separate DC link and MOSFET's ratings are chosen accordingly. A three phase transformer having center tapings at the primary with turn 's ratio of 1:6 is used for the proposed system.

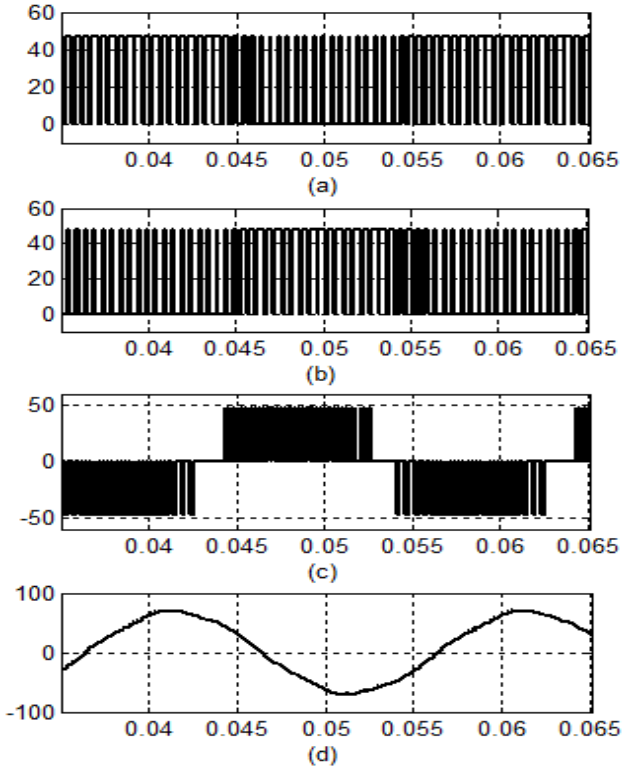

Fig. 2.29 Voltage and current waveforms of dual inverter configuration during normal condition (a) Inverter-1 pole voltage (b) Inverter-2 pole voltage (c) Pole to pole voltage of the inverter-1 [X-axis: time(sec), Y-axis: voltage(V)] (d) The current drawn by the primary of open ended transformer from dual inverters[X-axis: time(sec), Y-axis: current(A)]

Simulation results presented in this section verifies the performance of the proposed PV generation system under normal and fault condition. Output voltage

waveform on the secondary of the three phase transformer clearly shows that magnitude of output voltage is unaltered under fault condition but there is a transition from three level to two level. Output current waveform ensures that none of the dual inverter is over loaded. Inverter output waveforms under normal condition are shown in Fig. 2.29. The two level inverter pole voltages which are 180^0 out of phase are shown in Fig. 2.29(a) and Fig. 2.29(b).The inverter pole to pole voltage having a three level voltage profile is shown in Fig. 2.29(c). The presence of common mode voltages in the inverter output voltage cannot establish any current in the primary windings of the transformer as the dc links of each inverter are isolated [30]. The same can be observed from Fig. 2.29(d) which shows the line current of each inverter.

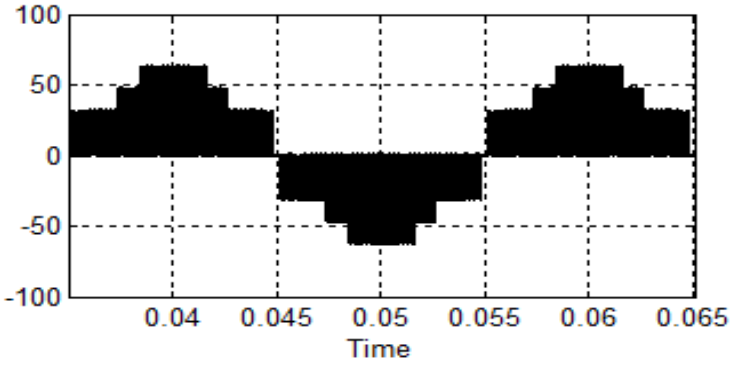

Fig. 2.30 Three level voltage induced in the open-ended primary winding of the transformer [X-axis: time(sec), Y-axis: voltage(V)]

Fig. 2.30 shows that three level voltage seen by the primary winding of the three phase transformer under normal condition. From this figure, relatively high dv/dt switching is observed as compared to other pulse width modulation techniques. The healthy side inverter will work independently under fault condition because of decoupled SVPWM with minimum control complexity. When a fault occurs three level voltage transists to two level voltage as only healthy inverter is working under fault as shown in Fig. 2.31 (a). Fig.2.31 (b) shows healthy inverter current waveform during fault condition, because of suggested load management no overload as happend. Fig. 2.31 (c) indicates no operation of the faulty side inverter under fault condition. The secondary side current wave form is shown in Fig.2.32 (a). which ensures the safe operation of proposed system under fault condition.

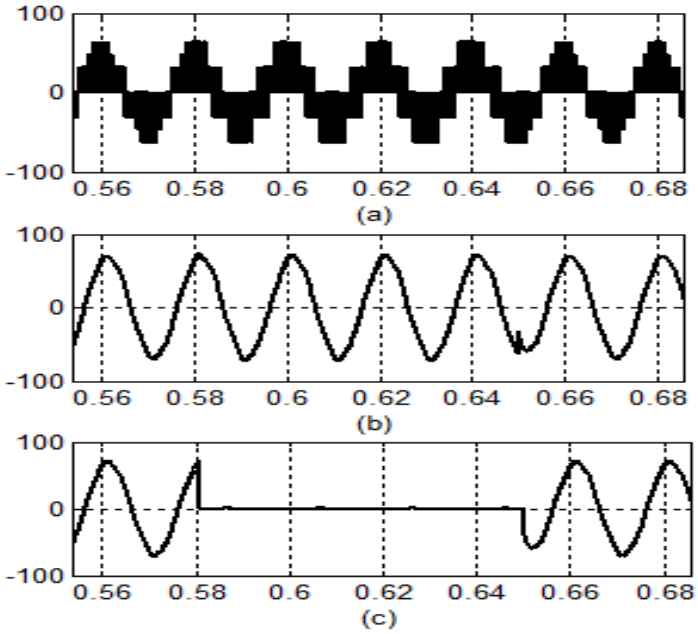

Fig. 2.31 Voltage and current waveforms during Fault condition (a) Dual inverter output voltage (b) Line current of inverter-2(Healthy inverter) (c) Line current of inverter-1[X-axis: time(sec), Y-axis: Voltage(V), current(A)]

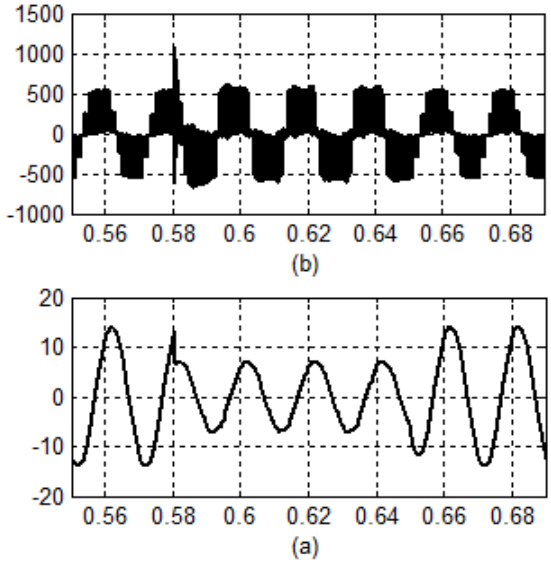

Fig. 2.32 Transformer secondary side current and voltage waveform under normal and fault condition (a) secondary side current wave form [X-axis: time(sec), Y-axis: current(A)] (b) secondary side voltage waveform [X-axis: time(sec), Y-axis: voltage(V)]

The transformer secondary side voltage waveform is shown in Fig. 2.32 (b) (very low value of leakage inductance is selected to show the effects of PWM switching and fault tolerant capability of the proposed circuit). Fig. 2.33 (a) shows the normalized harmonic spectrum of the dual inverter output voltage waveform under normal

operation. As the inverters in the proposed system are switched at 2 kHz, first order center band harmonics are expected at 40 time's fundamental frequency.

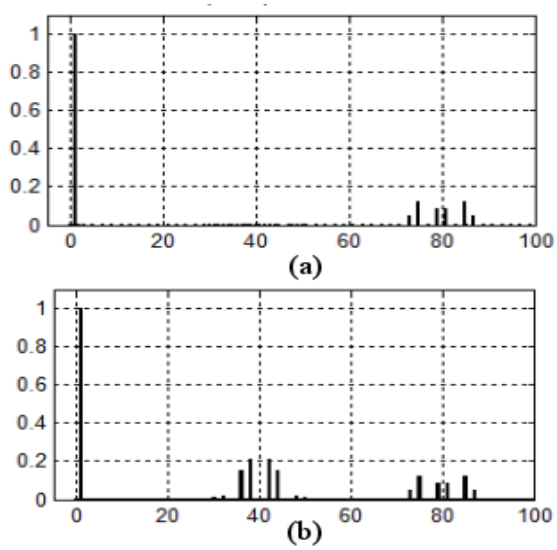

Fig. 2.33 The normalized harmonic spectrum of the voltage waveform (a) under normal operation (b) Under fault condition. [X-axis: Harmonic order, Y-axis: normalised harmonic magnitude]

But the dual inverters are controlled using decoupled SVPWM; thereby the first center band harmonics will cancel and appear at 80 times of fundamental frequency (50Hz) and this can be observed from Fig. 2.33 (a). Fig. 2.33 (b) indicates the normalized harmonic spectrum of output voltage under fault condition. Here the first center band harmonics can be observed at 40 times of fundamental frequency. This is because the output voltage is two-level as only healthy side inverter will be supplying the generation system.

B. Experimental Results

The gating pulse for the proposed laboratory prototype is generated with a switching frequency of 2 kHz using XILINX SPARTAN-6 (XC6SLX9) FPGA board programed in VHDL. A delay of 2.5μs is provided between the complimentary devices using dead band circuit. The two DC source voltages are considered as 48V. The pole voltages of inverter 1 and 2 are depicted in Fig.2.34, which are180^0 out of phase. The three-level induced voltage at the primary side of transformer and current waveform of two inverters are shown in Fig. 2.35.

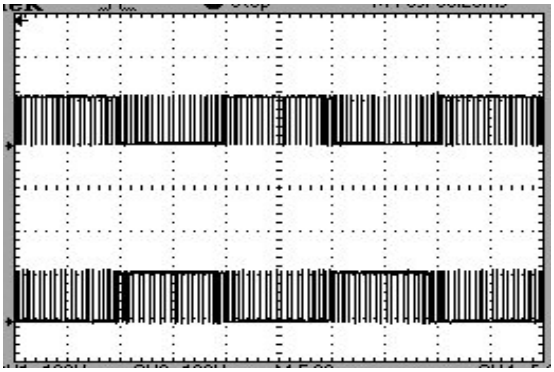

Fig. 2.34 pole voltages of inverter 1 and 2 [Y-axis 50V/div; X-axis 5msec/div]

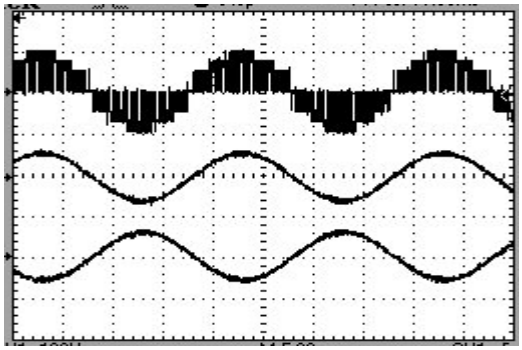

Fig. 2.35 Three-level induced voltage at primary side of transformer and inverter 1 and 2 currents [Y-axis 100V/div, 2A/div; X-axis 5msec/div]

The voltage across load and three phase currents through load are depicted in Fig. 2.36. The inverter 2 primary side induced voltage and current through transformer during inverter 1 failure is shown in Fig. 2.37. The two-level output voltage can be observed from Fig.2.37 only healthy inverter will operate during fault. The voltage across load and three phase currents are shown in Fig. 2.38. From this figure, it can be observed the magnitude of load voltage is same as normal condition.

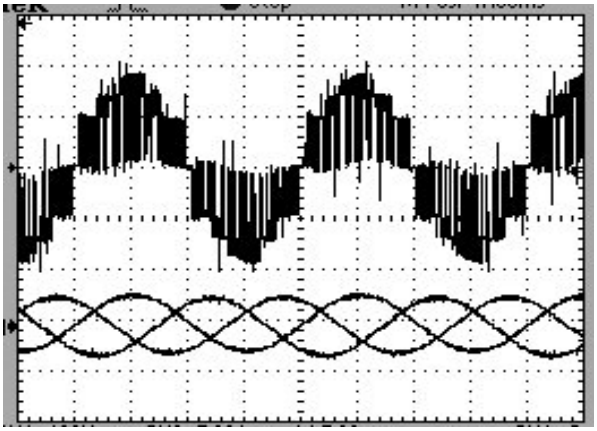

Fig. 2.36 Load voltage and three phase currents [Y-axis 100V/div, 2A/div; X-axis 5msec/div]

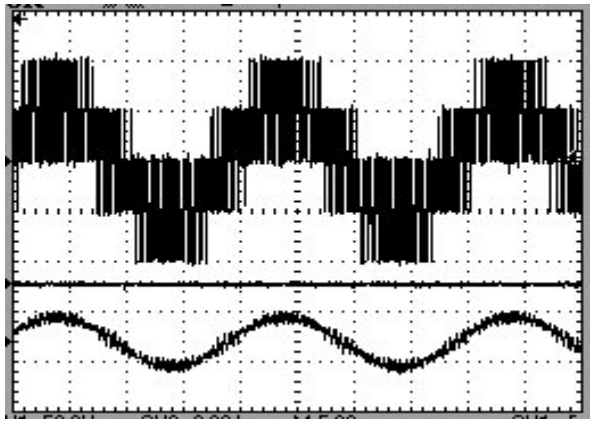

Fig. 2.37 Inverter 2 Primary side induced voltage and current through transformer [Y-axis 50V/div, 1A/div; X-axis 5msec/div]

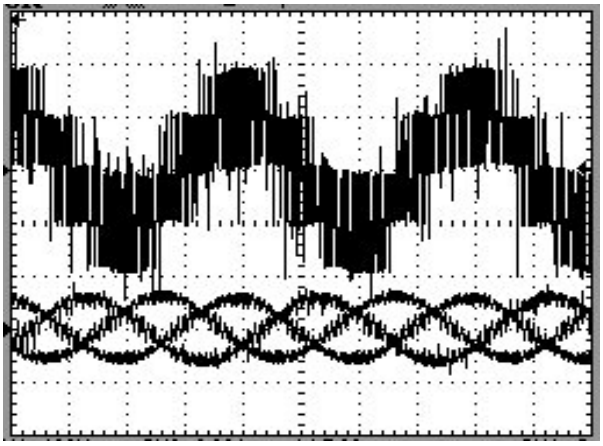

Fig. 2.38 Load voltage and three phase currents [Y-axis 50V/div, 2A/div; X-axis 5msec/div]

2.5 Conclusion

In this chapter different fault tolerant single phase and three phase multi-level inverter topologies are proposed for off grid PV applications. The proposed topologies are simulated using MATLAB/SIMULINK and then verified the results with laboratory prototype. Phase disposition carrier based pulse width modulation and decoupled SVPWM are adapted for generating multi-level output voltage across load. In case of any one of the switch open circuit fault and/or source failure happen, then the faulty switch or source is bypassed with the help of redundant switching combinations. The rated voltage is maintained during fault condition with the help of transformer. In these configurations, there is no capacitor voltage balancing issues and also requires less number of active switches compared to conventional NPC and flying capacitor inverters.

These fault tolerant multilevel inverters are fed with two separate PV sources with associated batteries has energy balancing problem due to partial shading or hotspots on any one of the PV string. In the following chapter a simple technique is presented for balancing the energy between two sources.

Chapter 3

Energy Balancing of Single Phase and Three Phase Five-level Inverter

3.1 Introduction

The block diagram of the multilevel inverter fed with two separate PV strings is shown in Fig. 3.1. It is known that, there will be energy sharing issue between the two sources because of partial shading and/or hotspots of PV panels. Due to this, the associated batteries will have difference in charging and discharging cycles which may lead to unequal SOC (state of charge) in the batteries. This difference in SOC's may lead to underutilize the system in critical conditions. Also, this difference in SOC of batteries creates small voltage variation at the battery terminals. This causes lower order sub-harmonic injection into AC side, which may cause for saturation of transformer and other inductive loads.

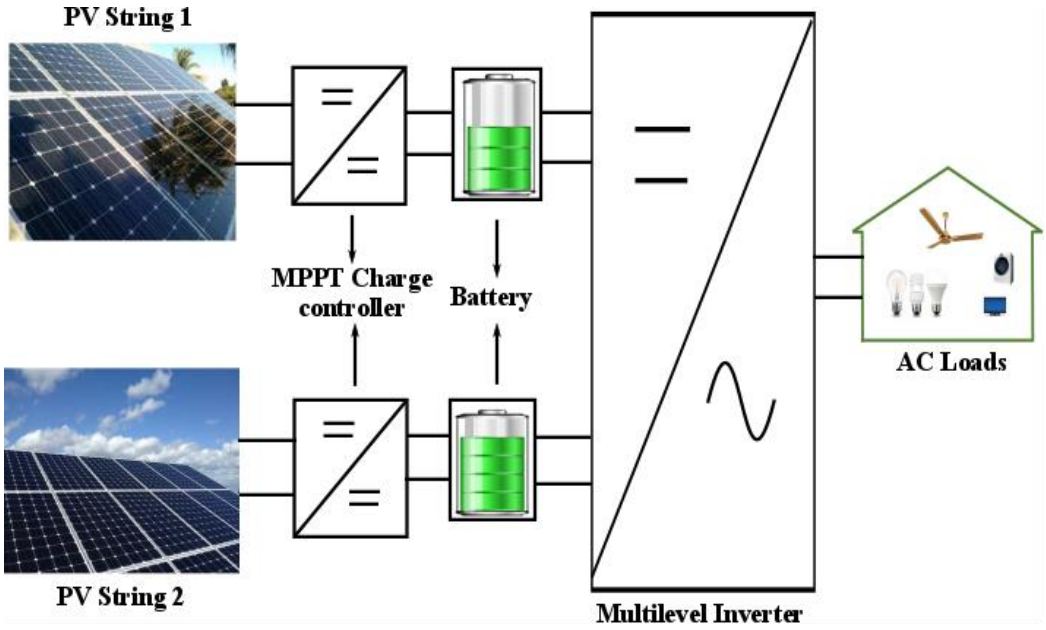

Fig.3.1 PV generation system under partial shaded condition

To address the above issues, in this chapter single phase and three phase five level inverter is presented for remote and offshore PV applications. The topologies are having two equal separate PV strings rated half of the total power rating as compared to single centralized PV inverter. Here the energy balancing between sources is achieved by using the available redundant switching combinations of middle voltage levels. The mathematical analysis for energy supplied during each voltage level and boundary conditions are presented.

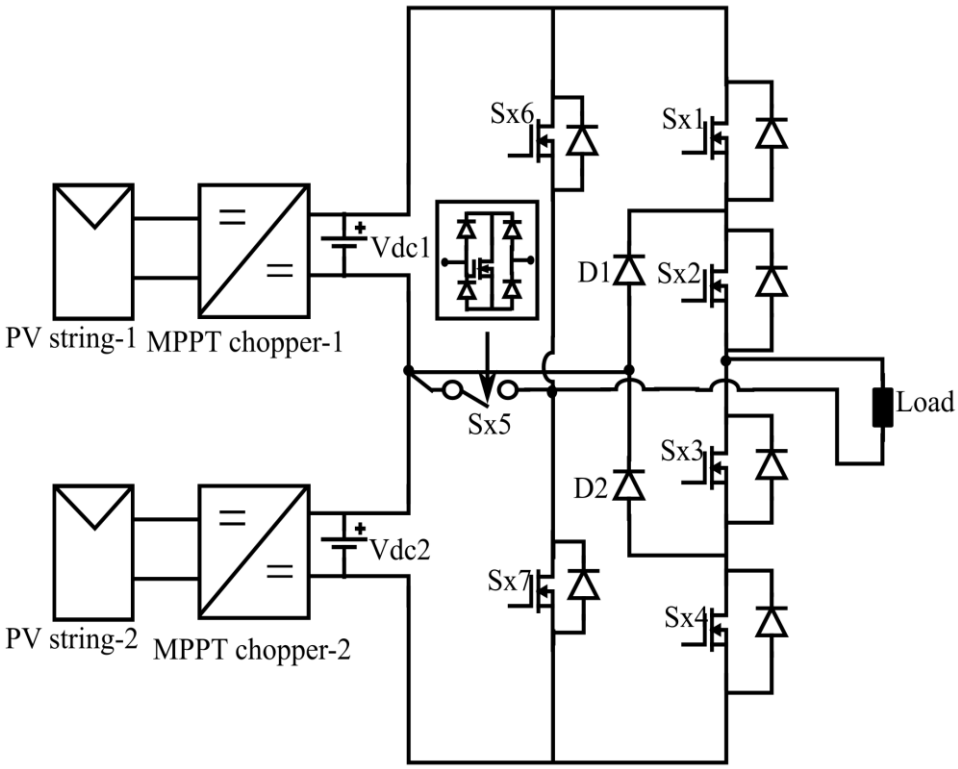

Fig. 3.2 Block diagram of single phase five-level inverter

3.2 . Energy balancing of single phase and three phase five-level Inverter due to partial shading

The proposed fault tolerant single phase and three phase five-level inverter is shown in Fig.3.2 and Fig.3.3. The inverter configuration is fed with two separate PV strings which are rated half of the total power rating, along with associated maximum power point tracking (MPPT) converter and batteries. The PV module is modelled using series and parallel connected PV cells using the model given in [79] based on

equation (2.1). The maximum power is tracked using perturb and observe algorithm proposed in [80].

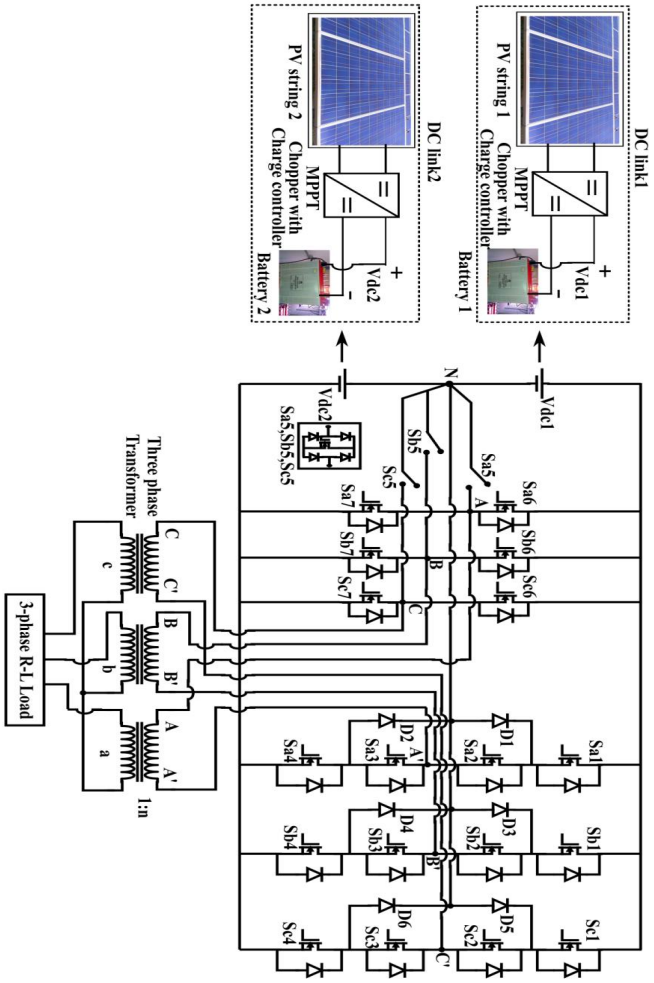

Fig. 3.3 Schematic of fault tolerant three phase multilevel inverter configuration.

The causes of partial shading are shadow of clouds, trees, electrical poles and shadow of one panel on other panel. The partial shading on any of the PV string causes reduction in power and leads to uneven charging/discharging of associated batteries that results in unequal SOC. Generally, in any island PV generation system, the load will take the energy more time from batteries compared to solar panels [84]. If the batteries continue to operate with uneven state of charges, the battery with low SOC dry out faster and causes overall system shutdown which in turn leads to underutilization of other battery. This issue can be reduced at all operating conditions by using the redundant switching combinations of middle voltage levels. The SOC of batteries is calculated based on voltage level [85].

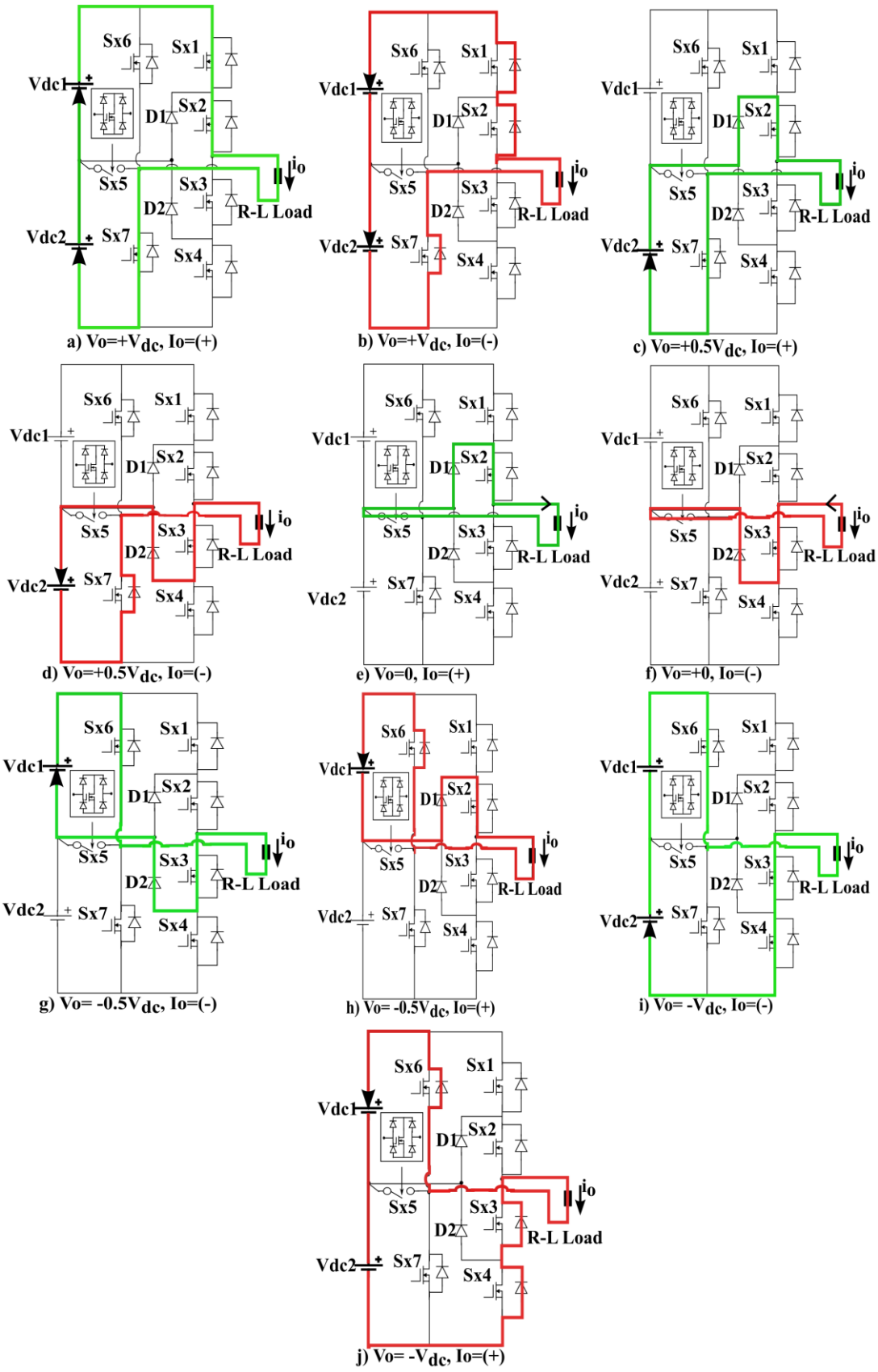

Fig.3.4 Current direction and working state of each voltage level

An effective energy balancing technique to balance the charging/discharging of batteries in case of uneven SOC's is derived using the redundant switching states of middle voltage levels of the proposed converter. During higher voltage level ($+V_{dc}$ and $-V_{dc}$) both the sources are connected in series to generate the required voltage level, which can be noticed from Fig.3.4 (a) and Fig.3.4 (i). Whereas for middle voltage levels ($+0.5V_{dc}$ and $-0.5V_{dc}$) by using switching redundancy given in Table 3.1, the load can be connected in parallel with the higher SOC. The possible percentage of energy share by both source during each voltage level is derived below.The switching combination for energy balancing between sources in case of partial shading is given in Table 3.1.

Table 3.1

Switching sequence during energy balancing

Levels of Voltage	Sx1	Sx2	Sx3	Sx4	Sx5	Sx6	Sx7
Higher Voltage ($+V_{dc}$)	1	1	0	0	0	1	0
0 (Zero level)	0	1	1	0	0	0	1
Higher Voltage ($-V_{dc}$)	0	0	1	1	1	0	0
Case I (source -V1)							
Middle Voltage($+0.5V_{dc}$)	1	1	0	0	0	0	1
0 (Zero level)	1	1	0	0	1	0	0
Middle Voltage ($-0.5V_{dc}$)	0	1	1	0	1	0	0
Case II (source-V2)							
Middle Voltage ($+0.5V_{dc}$)	0	1	1	0	0	1	0
0 (Zero level)	0	0	1	1	0	1	0
Middle Voltage ($-0.5V_{dc}$)	0	0	1	1	0	0	1

3.2.1 Calculation of Energy transferred to load by individual source

The five-level output voltage with only positive half cycle is shown in Fig. 3.5(a). The areas correponding to individual voltage level for single phase is shown in Fig. 3.5(b). Because of halfwave symmetry the calculations are considered only for halfcycle of fundamental waveform. The voltage waveform from 0 to θ and $(\pi - \theta)$ to π corresponding to middle voltage level and zero voltage level. The voltage waveform θ to $(\pi - \theta)$ is combination of higher $(V_{1a} = V_{dc})$ and middle $(V_{2a} =$

$V_{dc}/2$) voltage levels. In Fig. 3.5(b) from θ to $(\pi-\theta)$ the amount of area corresponding to each pulse of the higher level (V_{dc}) pulsating voltage waveform has same area below V_{2a} ($V_{dc}/2$)voltage level also. Hence Fig. 3.5(b) represents area A1 corresponding to V_{dc} voltage level and area A2 corresponding to $V_{dc}/2$ voltage level.

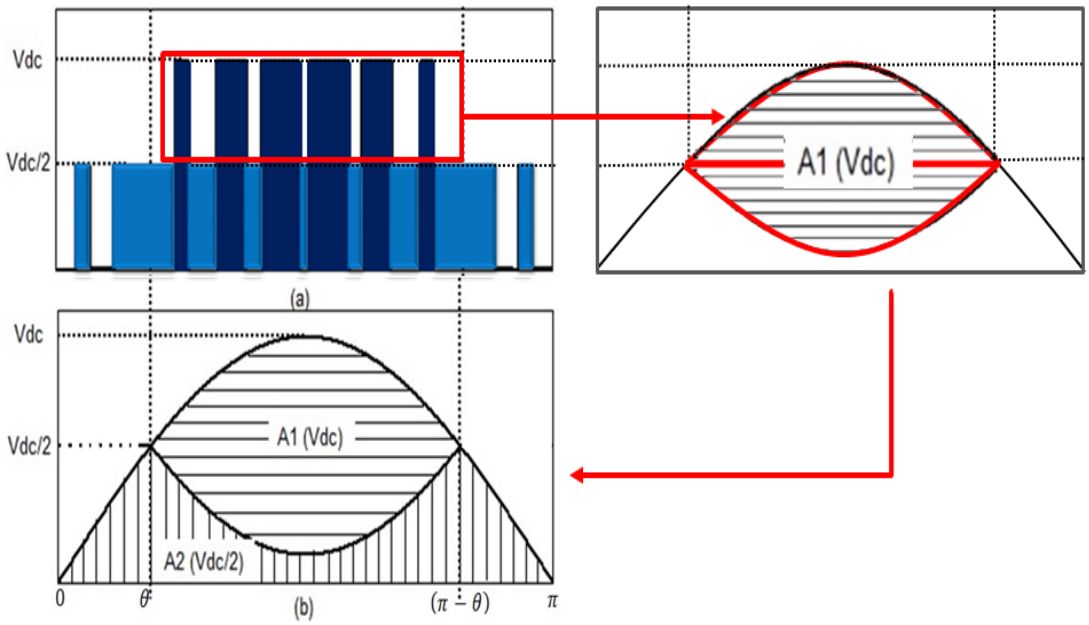

Fig.3.5 (a) Positive half cycle of fivelevel output voltage waveform. (b) Positive half cycle of fundamental voltage waveform with different areas

From Fig. 3.5(b) the instantaneous voltage from 0 to π given as $V = V_m \sin(\omega t)$

$V(x)$ is the fundamental voltage above $V_{dc}/2$ voltage level that is from θ to $(\pi-\theta)$ given as (3.1)

$$V(x) = \left\{ V_m \sin(\omega t) - \left(\frac{V_{dc}}{2} \right) \right\} \tag{3.1}$$

The fundamental voltage for higher voltage level and middle voltage level can be expressed as V_{1a} and V_{2a}

The fundamental voltage corresponding to higher voltage level (V_{1a}) can be expressed in (3.2)

$$V_{1a} = 2V(x) = 2\left\{ V_m \sin(\omega t) - \left(\frac{V_{dc}}{2} \right) \right\} \tag{3.2}$$

The fundamental voltage for middle voltage level (V_{2a}) is shown in equation (3.3)

$$V_{2a} = \left(V - V_{1a}\right)$$

$$V_{2a} = \left\{V_m \sin(\omega t) - 2\left[V_m \sin(\omega t) - \left(\frac{V_{dc}}{2}\right)\right]\right\} \tag{3.3}$$

Let us assume instantaneous current (i_a) as

$$i_a = I_m \sin(\omega t - \phi) \tag{3.4}$$

From equation (3.4) ϕ is power factor angle.

The angle θ can be calculated using equation (3.5)

$$\theta = \sin^{-1}\left(\frac{1}{2m_a}\right) \quad \text{where } \left\{\left(m_a V_{dc} \sin\theta\right) = \frac{V_{dc}}{2}\right\} \tag{3.5}$$

m_a =modulation index, V_{dc} is total dc voltage

The energy transfered (E_a) to load can be expressed as

$$E_a = \int_0^{\pi} V_j i_a dt \tag{3.6}$$

From (3.6) the voltage 'V_j' can be expressed as

$$E_a = \int_0^{\pi} \left(V_{1a} + V_{2a}\right) i_a dt$$

$$E_a = \int \left(V_{1a} i_a\right) dt + \int \left(V_{2a} i_a\right) dt$$

$$E_a = E_{V_{1a}} + E_{V_{2a}} \tag{3.7}$$

From (3.7) $E_{V_{1a}}$, $E_{V_{2a}}$ are the energies corresponding to V_{dc}, $V_{dc}/2$ voltage level is obtained from (3.2), (3.3) and (3.4) is given below

$$E_{V_{1a}} = \int_{\theta}^{\pi-\theta} 2\left\{V_m \sin(\omega t) - \left(\frac{V_{dc}}{2}\right)\right\} * I_m \sin(\omega t - \phi) d\omega t \tag{3.8}$$

After solving equation (3.8)

$$E_{V_{1a}} = \left(V_m I_m \cos\left(\phi\right)\right) * \left\{\left(\pi - 2\theta\right) + \sin\left(2\theta\right)\right\} - \left\{2V_{dc} I_m \cos\left(\phi\right)\cos\left(\theta\right)\right\} \tag{3.9}$$

$$E_{V_{2a}} = \int_{0}^{\pi} \left(V_m I_m \sin\left(\omega t\right)\right) * \sin(\omega t - \phi) d\omega t - \int_{\theta}^{\pi-\theta} 2\left\{V_m \sin(\omega t) - \left(\frac{V_{dc}}{2}\right)\right\} * I_m \sin(\omega t - \phi) d\omega t \tag{3.10}$$

After solving equation (3.11)

$$E_{V_{2a}} = \left(V_m I_m \cos\left(\phi\right)\right) * \left\{\left(\frac{\pi}{2}\right) - \left(\pi - 2\theta\right) - \sin\left(2\theta\right)\right\} + \left\{2V_{dc} I_m \cos\left(\phi\right)\cos\left(\theta\right)\right\} \tag{3.11}$$

The maximum possible percentage of energy transfered to load during each voltage level can be derived using (3.9) and (3.11) is obtained below and shown in Fig.3.6 for different modulation index varies from 0.1 to 1 and for given switching pattern.

$$\%E_{V_{2a}} = \left[\frac{E_{V_{2a}}}{E_{V_{1a}} + E_{V_{2a}}}\right] * 100 \tag{3.12}$$

$$\%E_{V_{1a}} = \left[\frac{E_{V_{1a}}}{E_{V_{1a}} + E_{V_{2a}}}\right] * 100 \tag{3.13}$$

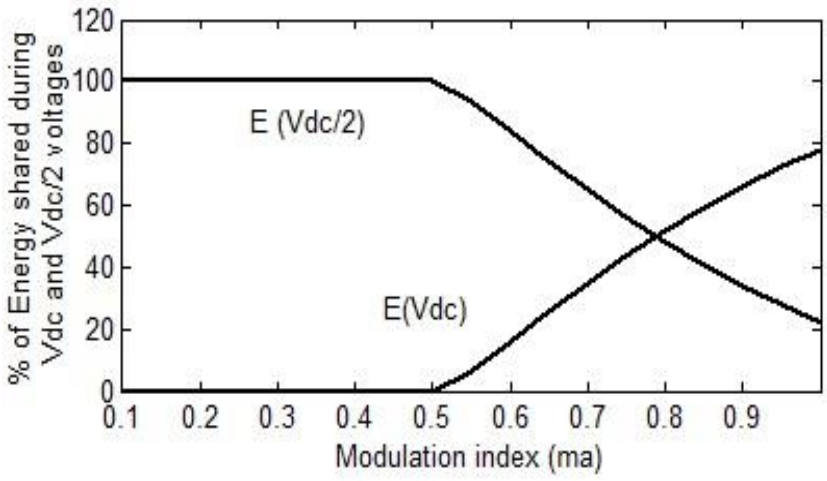

Fig.3.6 The possible percentage of energy shared to load by higher and middle voltage levels for different modulation index.

From equations (3.12), (3.13) and Fig. 3.6, it is noticed that the energy balancing between two sources depends on modulation index. The same advantage is effectively used to balance the SOC's of two batteries irrespective of input source

variations and output load conditions. The energy balancing between sources is explained for modulation index $m_a = 0.9$ using a case study given below. The possible percentage of energy supplied to load by higher voltage level (V_{dc}) is 66.15% of total energy, for middle voltage level ($V_{dc}/2$) is 33.85% of total energy, and zero energy for zero voltage level in a fundamental cycle (calculated using equation (3.12) and (3.13)). In normal condition the switching combinations are selected using Table 3.1 such that, both the sources will supply equal amount of energy to the load. In case of unbalance in SOC of batteries, appropriate switching combinations are selected given in Table 3.1 to minimize the difference in SOC. Generally, in higher voltage level (V_{dc}) both the sources are connected in series to supply the load, which results equal energy share during this voltage level (i.e. 33.07%). Therefore, the redundancy in lower voltage level ($V_{dc}/2$) is appropriately selected such that, the load will be connected to higher SOC source at this voltage level to reduce the difference in SOC. As discussed above the energy transferred during the middle voltage level is 33.85%. Therefore the maximum possible energy share of 33.85% in middle voltage level can be transferred to higher SOC source. Effectively, this result in energy share of 33.07% to lower SOC source and 66.93% to higher SOC source. The maximum possible energy shared by higher SOC source depends on area of middle voltage level.

Similarly for three phase operation the areas of individual voltage levels are shown in Fig. 3.7(c). The equations of the other two phases are given as follows

$$E_b = E_{V_{1b}} + E_{V_{2b}} \tag{3.14}$$

$$E_c = E_{V_{1c}} + E_{V_{2c}} \tag{3.15}$$

Where as for b and c phases the angles are

$$\theta_b = -\left(\frac{2\pi}{3}\right) + \sin^{-1}\left(\frac{1}{2m_a}\right),\ \theta_c = -\left(\frac{4\pi}{3}\right) + \sin^{-1}\left(\frac{1}{2m_a}\right)$$

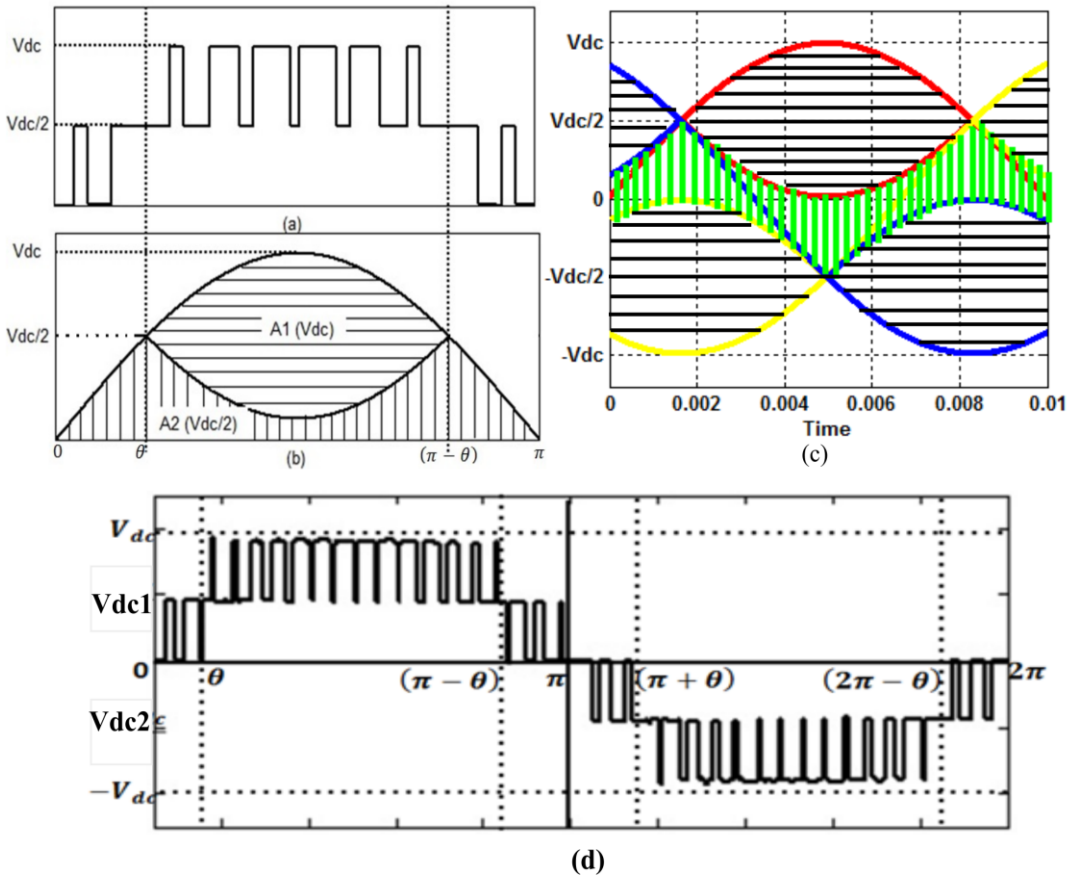

Fig. 3.7 a) Five-level output voltage in positive half cycle (b) Fundamental voltage in positive half cycle (c) Three phase fundamental voltage in positive half cycle. (d) Induced five-level voltage at primary side of transformer.

$$E_{V_{1b}} = \begin{Bmatrix} (V_{mb}I_{mb}) * \left\{ (\pi - 2\theta_b)\cos(\phi) + \cos(2\theta_b)\sin\left(\phi + \frac{\pi}{3}\right) \right\} \\ -\left\{ 2V_{dc}I_{mb}\cos\left(\phi + \frac{\pi}{3}\right)\cos(\theta_b) \right\} \end{Bmatrix} \tag{3.16}$$

$$E_{V_{2b}} = \left\{ \left(\frac{\pi}{2}\right) V_{mb}I_{mb}\cos(\phi) \right\} - E_{1b} \tag{3.17}$$

$$E_{V_{1c}} = \begin{Bmatrix} (V_{mc}I_{mc}) * \left\{ (\pi - 2\theta_c)\cos(\phi) + \cos(2\theta_c)\sin\left(\phi + \frac{2\pi}{3}\right) \right\} \\ -\left\{ 2V_{dc}I_{mc}\cos\left(\phi + \frac{4\pi}{3}\right)\cos(\theta_c) \right\} \end{Bmatrix} \tag{3.18}$$

$$E_{V_{2c}} = \left\{ \left(\frac{\pi}{2} \right) V_{mc} I_{mc} \cos(\phi) \right\} - E_{V_{1c}} \tag{3.19}$$

The total energy transferred to load $E = E_a + E_b + E_c$ (3.20)

The percentage energy transferred to load during higher voltage level (E_{V1})

$$\%E_{V1} = \left[\frac{E_{V_{1a}} + E_{V_{1b}} + E_{V_{1c}}}{E} \right] * 100 \tag{3.21}$$

The energy percentage transferred to load during middle voltage level (E_{V2})

$$\%E_{V2} = \left[\frac{E_{V_{2a}} + E_{V_{2b}} + E_{V_{2c}}}{E} \right] * 100 \tag{3.22}$$

For fundamental cycle the percentage of energy share by each source during normal operation given as

$$\%E_{Vdc1} = \left(\frac{\%E_{V_{dc}}}{2} \right) + \left(\frac{\%E_{-V_{dc}}}{2} \right) + \left(\%E_{V_{dc}/2} \right) \tag{3.23}$$

$$\%E_{Vdc2} = \left(\frac{\%E_{V_{dc}}}{2} \right) + \left(\frac{\%E_{-V_{dc}}}{2} \right) + \left(\%E_{-V_{dc}/2} \right) \tag{3.24}$$

For fundamental cycle the percentage of energy share by individual source during partial shading given as (Here Vdc1 is at higher SOC than Vdc2 and vice versa)

$$\%E_{Vdc1} = \left(\frac{\%E_{V_{dc}}}{2} \right) + \left(\frac{\%E_{-V_{dc}}}{2} \right) + \left(\%E_{V_{dc}/2} \right) + \left(\%E_{-V_{dc}/2} \right) \tag{3.25}$$

$$\%E_{Vdc2} = \left(\frac{\%E_{V_{dc}}}{2} \right) + \left(\frac{\%E_{-V_{dc}}}{2} \right) \tag{3.26}$$

3.2.2 DC offset minimisation

During partial shading of panels the associated batteries will charge and discharge differently due to this there is small voltage variation between battery terminals. Because of this voltage difference there is small dc offset is introduced in to the ac side output voltage. This issue can be addressed by using bidirectional

switches between neutral point and two-level inverter. These bidirectional switches will provide multiple switching combinations for middle voltage level generation.

For better understanding typical five level pole voltage waveform as shown in fig.3 (d). From this it can be noticed that, higher voltage magnitudes will be equal (i.e. Vdc which is equal to Vdc1+Vdc2), whereas the lower voltage magnitudes will be Vdc1 in positive half cycle and –Vdc2 in the negative half cycle. So if Vdc1 and Vdc2 are not equal, the average voltage at the output will not be zero. Which indicates that, if the batteries are not maintained at the same voltage will introduce an DC voltage offset value at the inverter output voltage.

The above issue can be addressed by sensing the battery terminal voltages, if there is difference in terminal voltages then redundant switching combinations for middle voltage level generation will be effectively used until the both SOC's are in allowable limit. For example Vdc1 is greater than Vdc2 then middle voltage levels generated using case I switching combinations shown in Table 3.1, in other event case II switching combination will be used.

3.3 Control Scheme

The control of the charge balance between batteries and the selection of switching combination are explained in the flowchart given in Fig. 3.8. Vdc1 and Vdc2 are two battery SOC's from the charge controller. From the flowchart, it can be noticed that, if it is within specified limits, then five-level voltages are generated using Table 2.1. If the difference in SOC is more or less than the limit, then an appropriate switching combination is selected using Table 3.1 using case I and II. The inverter pulses are generated using phase disposition PWM which is discussed in chapter 2.

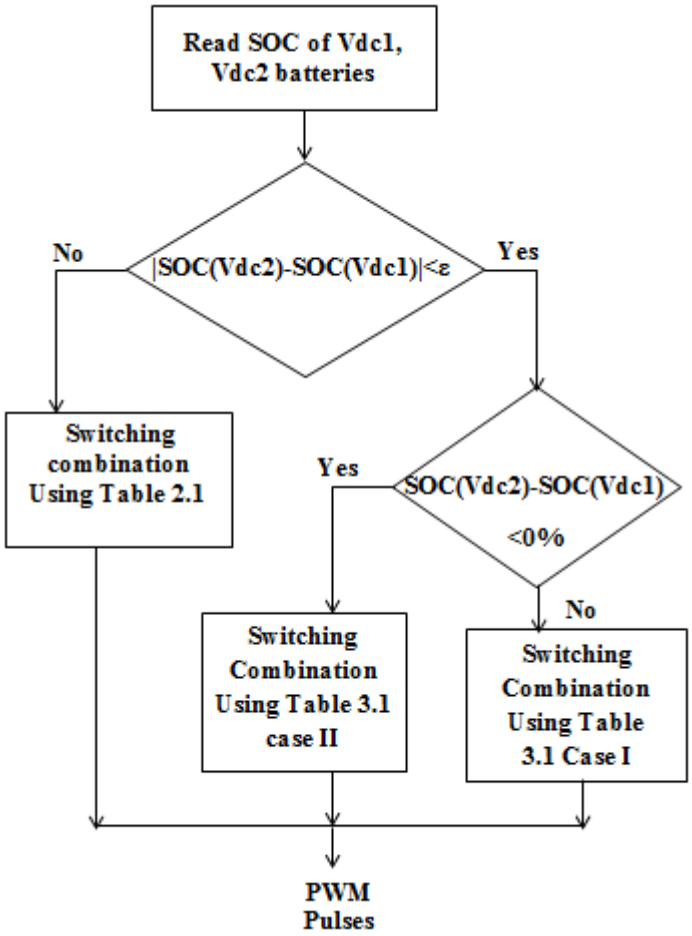

Fig.3.8 Control scheme flow chart for selecting switching combination

3.4 Results and Discussion

A. Simulation results of single phase five level inverter

The simulation parameters of single phase five-level inverter for energy balancing are given in Table 3.2. To evaluate the energy balancing capability of the proposed topology, both the batteries has charged to unequal SOC levels (i.e. first batteries associated to Vdc1 is kept at 60% and the other battery is at 80%). As discussed in the previous section, proposed energy balancing control scheme is used to minimize the difference in SOC's of both batteries, which can be seen from Fig.3.9 and 3.10. From these figures, it can be observed that the battery which is associated with voltage source Vdc2 is discharging faster compared to the other battery. During this operation, the average power dissipation by each source

measured as 33.6% and 66.4% respectively. These percentages are supporting with the previous section derivations.

Table 3.2
Parameters for simulation and laboratory prototype

Rated battery voltage (Lead acid)	$Vdc1 = Vdc2 = 96V$
Rated output voltage	120V
Modulating wave frequency	$f_m = 50Hz$
Switching frequency	$f_s = 1kHz$
Modulation index	$m_a = 0.9$
Load Resistance, inductance values	$R = 78\Omega, L = 50mH$

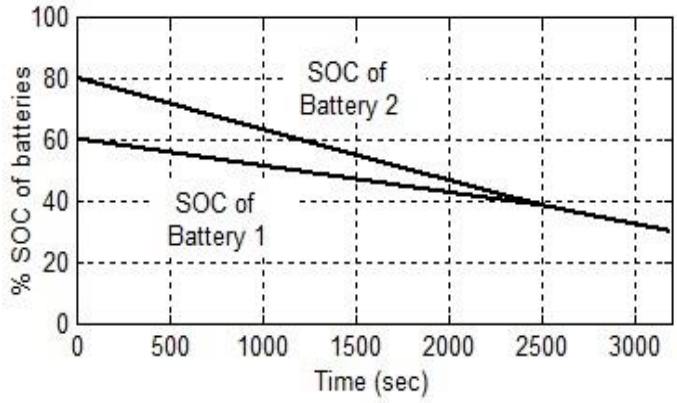

Fig. 3.9 Discharge characteristic of batteries for different SOC's [Y-axis % SOC of batteries; X-axis 500sec/div]

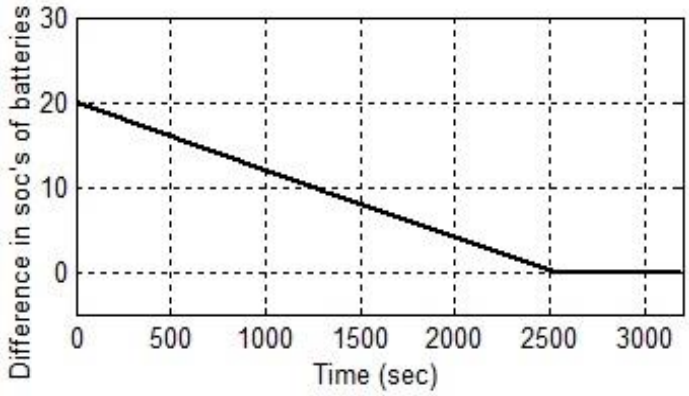

Fig. 3.10 Difference in SOC of batteries 1 and 2 [Y-axis Difference in SOC of batteries; X-axis 500sec/div]

B. Simulation results of three phase five-level inverter

The proposed three phase five-level inverter for islanded PV generation system is simulated using MATLAB/Simulink. The PV array and maximum power point tracking is modelled using reference given in [79], [80]. The parameters for simulation are given in Table 3.3.

Table 3.3

Parameters for Simulation

Rated Lead acid battery voltage	$Vdc1 = Vdc2 = 96V$
Modulating signal frequency	$f_m = 50Hz$
Switching frequency	$f_s = 2kHz$
Modulation index	$m_a = 0.9$
Load Resistance, inductance values	$R = 150\Omega, L = 40mH$

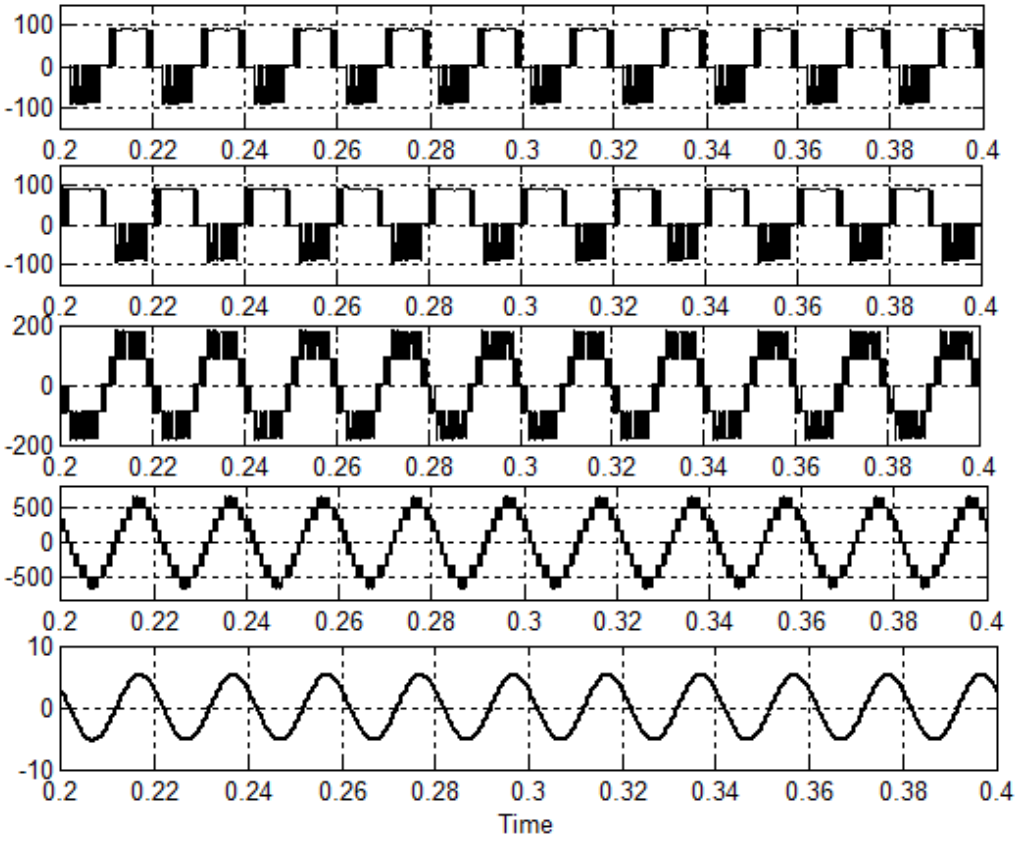

Fig. 3.11 Pole voltage of two-level and clamped inverter, induced five-level voltage, line voltage and load current waveforms During Energy balancing mode diode.

Fig.3.11 shows the waveforms during energy balancing mode of operation. The upper two traces are pole voltage of two-level inverter and three-level diode clamped inverter. The middle trace shows the induced five-level voltage across primary side winding of three phase transformer. The bottom two traces are line voltage and load current waveforms at load side.

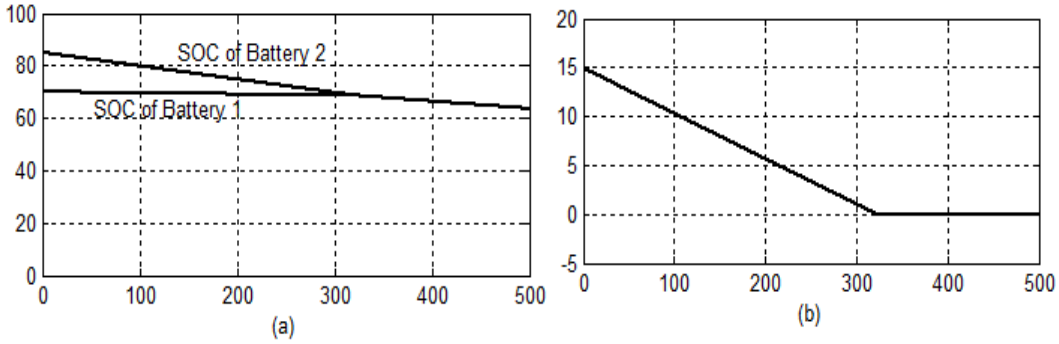

Fig. 3.12 (a) Discharge characteristic of batteries during energy balancing (b) Difference in SOC of batteries

The energy sharing between two batteries is shown in Fig. 3.12 (a). The percentage state of charge (SOC) of batteries 1 and 2 are 70% and 85%. If there is difference in SOC of batteries then the battery which is having more SOC is discharged more by slightly changing switching sequence there by the DC offset can be minimized and also battery SOC are balanced . Compared to single phase system the battery balancing is three times faster in three phase system. The difference in SOC of batteries is shown in Fig. 3.12 (b).

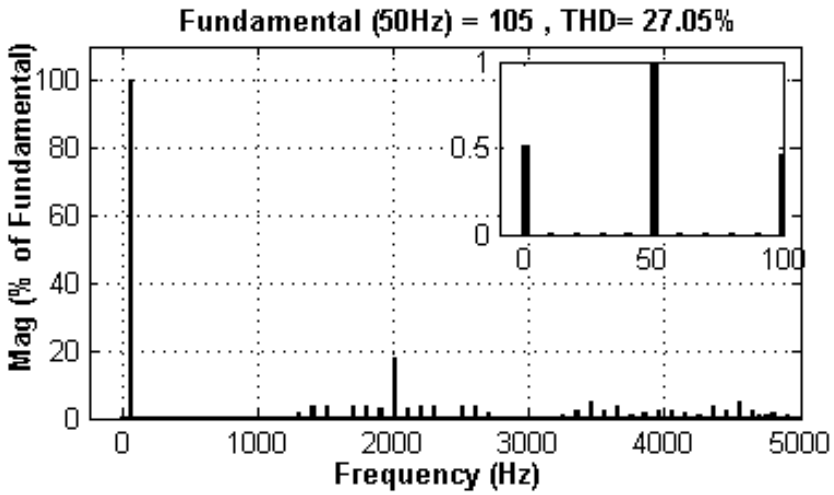

Fig.3.13 Harmonic spectrum of output voltage with dc-offset

During partial shading of PV panels the associated batteries will charge and discharge unevenly. Due to this, there is SOC difference between batteries which introduces a small dc-offset into ac side output voltage. Fig.3.13 gives the THD spectrum of the output voltage, because of the dc-offset harmonics present at the zero frequency. This dc offset is minimized by switching the middle voltage levels with single source which is having more SOC, as shown in Fig.3.14.

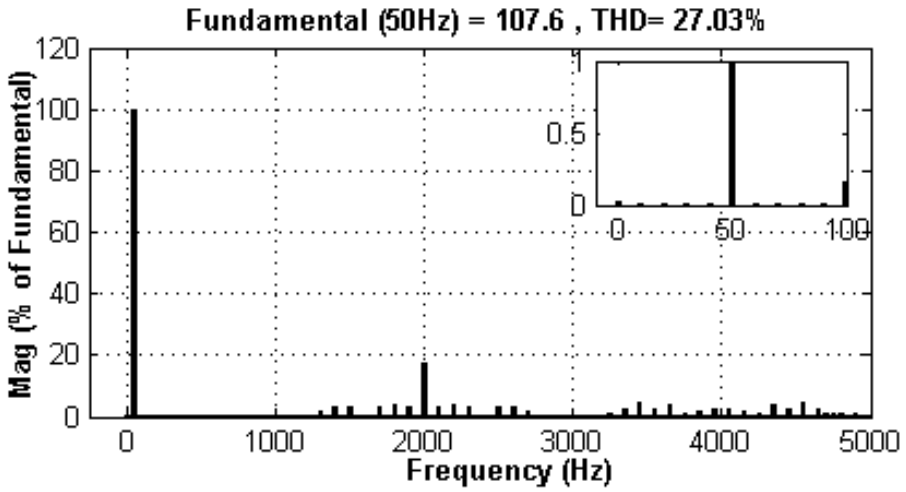

Fig. 3.14 Harmonic spectrum of output voltage without dc-offset

3.5 Conclusion

In this chapter the energy balancing of single phase and three phase five-level inverter for off-grid PV generation system is presented. By using the redundancy switching of the middle voltage levels, energy balancing is achieved between batteries and also the dc voltage offset is minimized. The battery which is having more SOC will supply more energy to load until both the SOC of batteries are equal. The mathematical analysis for energy supplied by individual voltage levels and sources is presented. The simulation results show the effectiveness of proposed technique.

In this chapter the energy balancing of multilevel inverter fed with two separate PV sources is discussed but, for higher number of sources is not discussed. The following chapter discusses the energy balancing by distributing the PV panels among the sources optimally.

Chapter 4

An Optimal Source distribution Strategy for Multilevel Inverters with Improved Reliability: Photovoltaic Application

4.1 Introduction

Diode clamped, cascade H-bridge multilevel inverter fed with multiple PV strings and MPPT control of individual PV strings improves the efficiency of the system [86-88]. In these inverters the stability control of PV generation system is discussed for different irradiation, temperature changes and mismatch of PV strings. Many multilevel inverters topologies are discussed for renewable energy applications with reduced number of semiconductor devices [89-94]. These multilevel inverters use equal ratings of voltage sources to supply energy to load. However, the equivalent loading of each sources over a complete fundamental cycle are quite different which leads to underutilization of voltage sources. On the other hand, in the equal rating battery integrated off-grid PV system, due to uneven loading of sources, the state of charge (SOC) of batteries will be different. This mismatch of power supplied to load by the sources leads to poor utilization of source. In literature [95], a battery charge balance control schemes for cascade multilevel inverter discussed using duty cycle based rotation of pulses. However, the total harmonic distortion by using these methods is high. This issue is addressed in [59] for cascaded seven-level H-bridge inverter by rotation of pulse width modulation based gating pulses to each H-bridge module, so that the power can be balanced in three fundamental cycles. Though the power is balancing in three fundamental cycles there is a chance of small dc offset injection into ac side because of battery terminal voltage difference. In [96] a nine-level cascade multilevel inverter with two bidirectional switches is presented but energy sharing issues of sources are not discussed. In [97], a novel DC power control

for cascade H-bridge multilevel inverter is presented. Although it has addressed the mismatch in dc side power generation, but the issues like load sharing effect on individual sources is not discussed.

The above issues are addressed in this chapter by distributing PV modules for individual voltage sources based on the loading as well as average operating modulation index. The proposed source distribution scheme is discussed in a multilevel inverter fed with four separate PV sources with maximum power point charge controller and corresponding batteries. The mathematical analysis is carried out for energy supplied by sources in each voltage level as well as energy contribution of each sources over a complete fundamental cycle. Based on mathematical analysis PV panels are distributed among four sources as well as corresponding battery ratings are decided.

4.2 Calculation of energy transferred during each voltage level

In a multilevel inverter, the energy supplied from source to load only during active voltage state (non-zero voltage magnitude) which has multiple voltage levels. The aggregate energy associate with each voltage level is quite different for a specific modulation index (m_a). However the energy associated with a particular voltage level is same for different multilevel inverter topologies with same number of voltage levels. A case study to calculate the energy transferred to load during each voltage-level of nine-level inverter with four individual sources is presented.

4.2.1 Calculation of energy associated with each voltage level

The positive half cycle of a standard nine-level pulsating output voltage waveform is shown in Fig.4.1 (a). Because of half wave symmetry of the output voltage waveform, the calculations are carried out for positive half cycle. Fig. 4.1(b) shows the area corresponding to each voltage level, where θ_1 to θ_6 are the angles corresponding to duration of different voltage-levels.

From Fig.4.1 the instantaneous fundamental voltage waveform from o to π given as

$$V_{fun} = V_m \sin(\omega t)$$

Vdc, 3Vdc/4, Vdc/2, Vdc/4 are the voltage levels indicated as V_k, V_n, V_o, V_p.

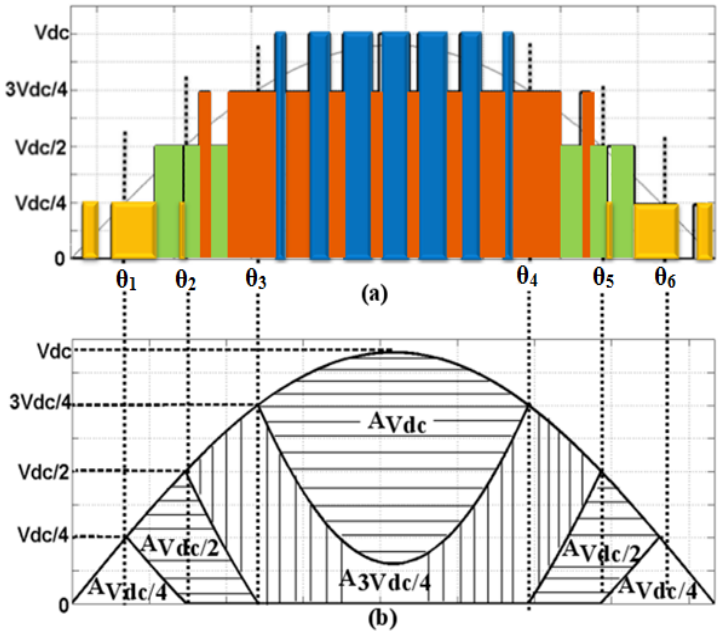

Fig. 4.1 (a) Positive half cycle of pulsating nine-level voltage waveform (b) Area corresponding to different voltage-levels

The fundamental voltage V_k indicates Vdc voltage level in the region θ_3 to θ_4 given as

$$V_k = 4\left\{V_m \sin(\omega t) - \left(\frac{3V_{dc}}{4}\right)\right\} \tag{4.1}$$

The fundamental voltage V_n indicates 3Vdc/4 voltage level in the region θ_2 to θ_5 expressed as

The 3Vdc/4 voltage level in the region θ_3 to θ_4 given as

$$V_a = \left(V_{fun} - V_k\right)$$

The 3Vdc/4 voltage level in the region θ_2 to θ_3 given as

$$V_b = 3\left(V_{fun} - \left(\frac{V_{dc}}{2}\right)\right)$$

The 3Vdc/4 voltage level in the region θ_4 to θ_5 is same as θ_2 to θ_3

$$V_n = \left(V_a + 2V_b\right) \tag{4.2}$$

The fundamental voltage V_o indicates Vdc/2 voltage level in the region θ_1 to θ_6 given as

The Vdc/2 voltage level in the region θ_2 to θ_3 expressed as

$$V_c = \left(V_{fun} - V_b\right)$$

The Vdc/2 voltage level in the region θ_1 to θ_2 given as

$$V_d = 2\left(V_{fun} - \left(\frac{V_{dc}}{4}\right)\right)$$

The Vdc/2 voltage level in the region θ_2 to θ_3 is same as θ_4 to θ_5 similarly for θ_1 to θ_2 same as θ_5 to θ_6

$$V_o = \left(2V_c + 2V_d\right) \tag{4.3}$$

The fundamental voltage V_p indicates Vdc/4 voltage level in the region 0 to θ_2 and θ_6 to π given as

The Vdc/4 voltage level in the region θ_1 to θ_2 given as

$$V_e = \left(V_{fun} - V_d\right)$$

The Vdc/4 voltage level in the region 0 to θ_1 expressed as

$$V_f = V_{fun}$$

The Vdc/4 voltage level in the region 0 to θ_1 is same as θ_6 to π similarly θ_1 to θ_2 is same as θ_5 to θ_6

$$V_p = \left(2V_f + 2V_e\right) \tag{4.4}$$

The load current is given as $i = I_m \sin(\omega t - \phi)$, where ϕ is power factor angle

The angle θ_1-θ_6 depends on modulation index m_a and the angle can be calculated as

$$\left(m_a V_{dc} \sin\theta_1\right) = \frac{V_{dc}}{4}$$

$$\theta_1 = \sin^{-1}\left(\frac{1}{4m_a}\right),\ \theta_2 = \sin^{-1}\left(\frac{1}{2m_a}\right),\ \theta_3 = \sin^{-1}\left(\frac{3}{4m_a}\right)$$

$$\theta_4 = \pi - \sin^{-1}\left(\frac{3}{4m_a}\right) = \pi - \theta_3,\ \theta_5 = \pi - \sin^{-1}\left(\frac{1}{2m_a}\right) = \pi - \theta_2$$

$$\theta_6 = \pi - \sin^{-1}\left(\frac{1}{4m_a}\right) = \pi - \theta_1$$

E_{V_k},E_{V_n},E_{V_o}, E_{V_p} are the energies corresponding to Vdc, 3Vdc/4, Vdc/2, Vdc/4 voltage levels can be derived using equation (4.1)-(4.4).

The energy transferred during V_k voltage level given as

$$E_{V_k} = \int_{\theta_3}^{\pi-\theta_3} V_k id\omega t \tag{4.5}$$

After solving equation (4.5) the energy transferred to V_k voltage level given as

$$E_{V_k} = \left\{ \begin{array}{l} \left(2V_m I_m\right) * \left\{ \left(\pi - 2\theta_3\right)\cos\left(\phi\right) + \dfrac{\sin\left(2\theta+\phi\right)}{2} + \dfrac{\sin\left(2\theta-\phi\right)}{2} \right\} - \\ \left\{ 3V_{dc} I_m \left[\cos\left(\theta_3+\phi\right) + \cos\left(\theta_3-\phi\right) \right] \right\} \end{array} \right\} \tag{4.6}$$

The energy transferred during V_n voltage level given as

$$E_{V_n} = \left\{ \int_{\theta_2}^{\theta_3} V_b id\omega t + \int_{\pi-\theta_3}^{\pi-\theta_2} V_b id\omega t + \int_{\theta_3}^{\pi-\theta_3} V_a id\omega t \right\} \tag{4.7}$$

The solution of equation (4.7) the energy transferred to V_n voltage level given as

$$E_{V_n} = \left\{ \begin{array}{l} \left(1.5V_m I_m\right) * \left\{ \left(\theta_3 - \theta_2\right)\cos\left(\phi\right) - \dfrac{\sin\left(2\theta_3-\phi\right)}{2} + \dfrac{\sin\left(2\theta_3+\phi\right)}{2} \right\} + \\ \left\{ 1.5V_{dc} I_m \left[\cos\left(\theta_3-\phi\right) - \cos\left(2\theta_2-\phi\right) \right] \right\} + \\ \left(1.5V_m I_m\right) * \left\{ \left(\theta_3 - \theta_2\right)\cos\left(\phi\right) + \dfrac{\sin\left(2\theta_2+\phi\right)}{2} - \dfrac{\sin\left(2\theta_3+\phi\right)}{2} \right\} + \\ \left\{ 1.5V_{dc} I_m \left[\cos\left(\theta_3+\phi\right) - \cos\left(\theta_2+\phi\right) \right] \right\} + \\ \left(1.5V_m I_m\right) * \left\{ \left(\pi - 2\theta_3\right)\cos\left(\phi\right) + \dfrac{\sin\left(2\theta_3+\phi\right)}{2} + \dfrac{\sin\left(2\theta_3-\phi\right)}{2} \right\} - E_{V_k} \end{array} \right\} \tag{4.8}$$

The energy transferred during V_o voltage level given as

$$E_{V_o} = \left\{ \int_{\theta_1}^{\theta_2} V_d id\omega t + \int_{\pi-\theta_2}^{\pi-\theta_1} V_d id\omega t + \int_{\theta_2}^{\theta_3} V_c id\omega t + \int_{\pi-\theta_3}^{\pi-\theta_2} V_c id\omega t \right\} \tag{4.9}$$

$$E_{V_o}=\left\{\begin{array}{l}(V_mI_m)*\left\{(\theta_2-\theta_1)\cos(\phi)-\frac{\sin(2\theta_2-\phi)}{2}+\frac{\sin(2\theta_1-\phi)}{2}\right\}+\\ \left\{1.5V_{dc}I_m\left[\cos(\theta_2-\phi)-\cos(\theta_1-\phi)\right]\right\}+\\ (V_mI_m)*\left\{(\theta_2-\theta_1)\cos(\phi)+\frac{\sin(2\theta_1+\phi)}{2}-\frac{\sin(2\theta_2+\phi)}{2}\right\}+\\ \left\{0.5V_{dc}I_m\left[\cos(\theta_2+\phi)-\cos(\theta_1+\phi)\right]\right\}-\\ (V_mI_m)*\left\{(\theta_3-\theta_2)\cos(\phi)+\frac{\sin(2\theta_3-\phi)}{2}+\frac{\sin(2\theta_2-\phi)}{2}\right\}-\\ \left\{0.5V_{dc}I_m\left[\cos(\theta_3-\phi)-\cos(\theta_2-\phi)\right]\right\}-\\ (V_mI_m)*\left\{(\theta_3-\theta_2)\cos(\phi)-\frac{\sin(2\theta_2+\phi)}{2}-\frac{\sin(2\theta_3+\phi)}{2}\right\}-\\ \left\{0.5V_{dc}I_m\left[\cos(\theta_3+\phi)-\cos(\theta_2+\phi)\right]\right\}\end{array}\right\} \tag{4.10}$$

The energy transferred during V_p voltage level given as

$$E_{V_p}=\left\{\int_0^{\theta_1}V_f id\omega t+\int_{\pi-\theta_1}^{\pi}V_f id\omega t+\int_{\theta_1}^{\theta_2}V_e id\omega t+\int_{\pi-\theta_2}^{\pi-\theta 1}V_e id\omega t\right\} \tag{4.11}$$

$$E_{V_p}=\left\{\begin{array}{l}(0.5V_mI_m)*\left\{\theta_1\cos(\phi)-\frac{\sin(2\theta_1-\phi)}{2}-\frac{\sin(\phi)}{2}\right\}+\\ (0.5V_mI_m)*\left\{\theta_1\cos(\phi)+\frac{\sin(2\theta_1+\phi)}{2}+\frac{\sin(\phi)}{2}\right\}-\\ (0.5V_mI_m)*\left\{(\theta_2-\theta_1)\cos(\phi)-\frac{\sin(2\theta_2-\phi)}{2}+\frac{\sin(2\theta_1-\phi)}{2}\right\}-\\ \left\{0.5V_{dc}I_m\left[\cos(\theta_2-\phi)-\cos(\theta_1-\phi)\right]\right\}-\\ (0.5V_mI_m)*\left\{(\theta_2-\theta_1)\cos(\phi)-\frac{\sin(2\theta_2+\phi)}{2}+\frac{\sin(2\theta_1+\phi)}{2}\right\}-\\ \left\{0.5V_{dc}I_m\left[\cos(\theta_2+\phi)-\cos(\theta_1+\phi)\right]\right\}\end{array}\right\} \tag{4.12}$$

The total energy transferred to load during positive half cycle given as

$$E=E_{V_k}+E_{V_n}+E_{V_o}+E_{V_p} \tag{4.13}$$

Similarly it is same for negative half cycle also

The percentage of energy transfer during each voltage level can be calculated as follows

$$\%E_{V_i} = \%E_{-V_i} = \left[\frac{E_{Vi}}{E_{V_k} + E_{V_n} + E_{V_o} + E_{V_p}} \right] * 100 \tag{4.14}$$

Where i= k, n, o, p

The energy associated with each voltage level for various modulation index values is shown in Fig.4.2. From this figure, it can be observed that the percentage of energy transferred to load during each voltage level is different.

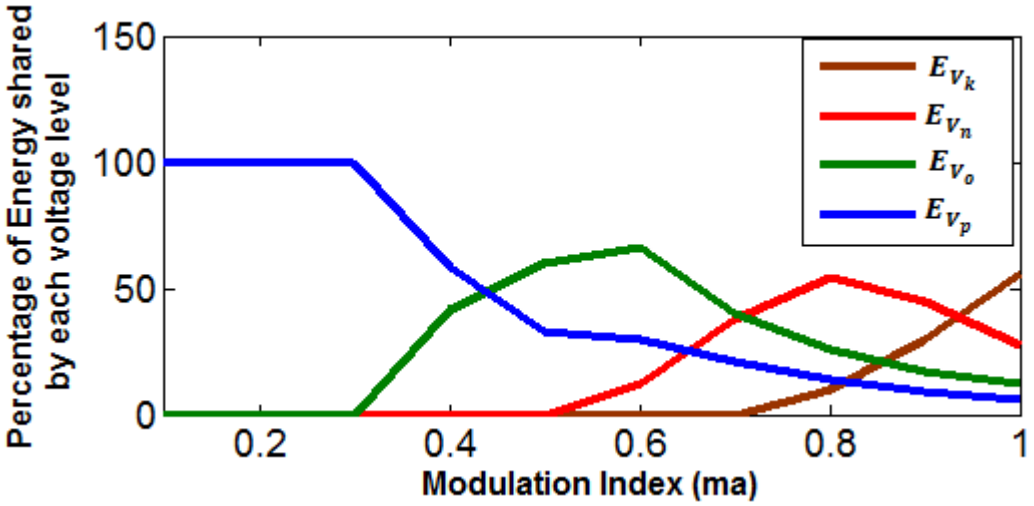

Fig. 4.2 Percentage of energy shared during each voltage level with different modulation index.

The percentage of energy shared during each voltage-level is depicted in Fig.4.2 is same for any multilevel inverter. The energy supplied to load by each source is different according to inverter topology structure and switching combination. To validate this proposed scheme a case study is presented using nine-level inverter topology with four separate sources [97].

4.2.2 Multilevel inverter configuration with equal source distribution

The multi-level inverter configuration given in [97] fed with four individual PV strings with MPPT charge controller and associated batteries which are rated equally as shown in Fig.4.3 The total number of PV modules are divided as N1, N2, N3, N4 (N1=N2=N3=N4=n/4, where n is total number of PV panels). The nine-level voltage generation is possible with equal voltage (V1=V2=V3=V4=Vdc/4) rating of sources using multiple switching combinations due to redundancy of the topology. Table 4.1

and 4.2 gives the two possible switching combinations for different voltage levels and corresponding voltage source combination.

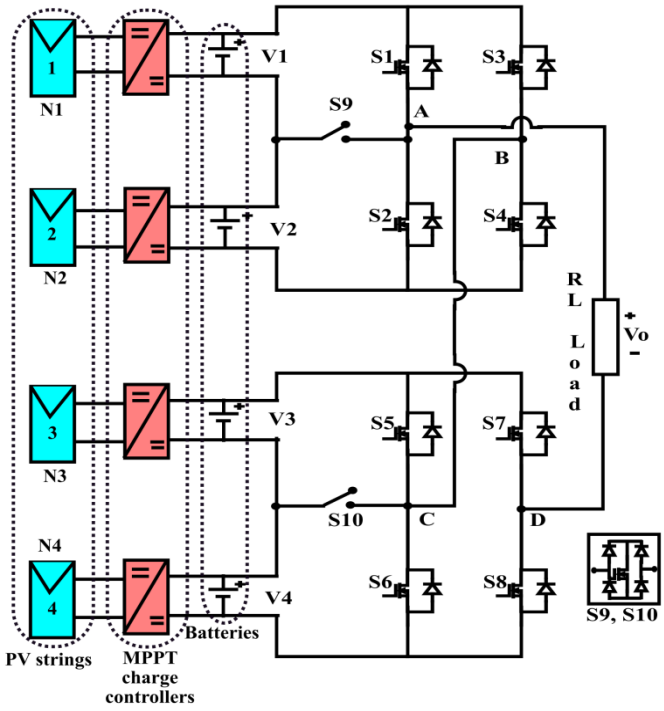

Fig. 4.3 Block diagram of multi-string single phase multilevel inverter system with four PV sources.

From Table 4.1, it can be observed that the sources V3 and V4 are supplying energy to load for all the voltage levels except Vdc/4 and –Vdc/4 respectively. Whereas V1 is supplying energy to load for Vdc, -Vdc and -3Vdc/4 voltage levels. The source V2 is supplying energy to load for Vdc, -Vdc and 3Vdc/4 voltage levels. Due to this, the loading is different on each voltage source which causes the corresponding batteries charge and discharge unequally which is shown in Fig.4.4. From this figure, it can also be observed that two set of batteries are charging equally compared to other two batteries. If the systems continuous to operate with unequal state of charge (SOC), the batteries with low SOC will dry out faster and causes total system shutdown and leads to underutilization of healthy sources. This issue is avoided by arranging the PV panels based on equivalent energy supplied to load by each source with various modulation indexes is discussed in later part of this section.

Table 4.1
Switching combination for nine-level operation
(V1=V2=V3=V4=V_{DC}/4)

Voltage levels	Switching sequence	Corresponding Sources
Vdc	S1,S8,S5,S4	V1,V2,V3,V4
3Vdc/4	S9,S4,S5,S8	V2,V3,V4
Vdc/2	S2,S4,S5,S8	V3,V4
Vdc/4	S2,S4,S10,S8	V4
0	S2,S4,S6,S8	0
-Vdc/4	S10,S2,S4,S7	V3
-Vdc/2	S2,S4,S7,S6	V3,V4
-3Vdc/4	S3,S6,S7,S9	V1,V3,V4
-Vdc	S2,S3,S6,S7	V1,V2,V3,V4

Table 4.2
Switching combination for nine-level operation
(V1=V2=V3=V4=V_{DC}/4)

Voltage levels	Switching sequence	Corresponding Sources
Vdc	S1,S8,S5,S4	V1,V2,V3,V4
3Vdc/4	S9,S8,S5,S4	V2,V3,V4
Vdc/2	S5,S2,S4,S8	V3,V4
Vdc/4	S10,S4,S2,S8	V4
0	S2,S4,S5,S7	0
-Vdc/4	S3,S5,S7,S9	V1
-Vdc/2	S3,S5,S7,S2	V1,V2
-3Vdc/4	S3,S10,S7,S2	V1,V2,V3
-Vdc	S3,S6,S7,S2	V1,V2,V3,V4

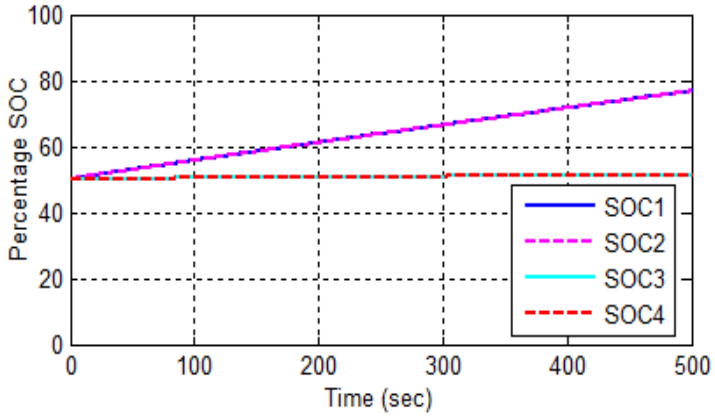

Fig. 4.4 Charging characteristics of each battery supplying with equal power rating PV sources.

4.3 Multilevel inverter configuration with optimized PV panel distribution

From the earlier discussion, the energy supplied to the load by the individual sources are unequal. To address this issue, the panels are distributed among four sources according to percentage energy sharing of each source. The percentage energy shared to load is calculated for fundamental cycle using equations (4.15)-(4.18). The source combinations for generating nine-level voltage are given in Table 4.1 and 4.2. Table 4.1 considered as worst switching combination for distribution of PV panels.

$$\%E_{V1}=\left(\frac{\%E_{V_k}}{4}\right)+\left(\frac{\%E_{-V_n}}{3}\right)+\left(\frac{\%E_{-V_k}}{4}\right) \tag{4.15}$$

$$\%E_{V2}=\left(\frac{\%E_{V_k}}{4}\right)+\left(\frac{\%E_{V_n}}{3}\right)+\left(\frac{\%E_{-V_k}}{4}\right) \tag{4.16}$$

$$\%E_{V3}=\left(\frac{\%E_{V_k}}{4}\right)+\left(\frac{\%E_{V_n}}{3}\right)+\left(\frac{\%E_{V_o}}{2}\right)+\left(\frac{\%E_{-V_n}}{3}\right)+\left(\frac{\%E_{-V_o}}{2}\right)+\left(\%E_{-V_p}\right)+\left(\frac{\%E_{-V_k}}{4}\right) \tag{4.17}$$

$$\%E_{V4}=\left(\frac{\%E_{V_k}}{4}\right)+\left(\frac{\%E_{V_n}}{3}\right)+\left(\frac{\%E_{V_o}}{2}\right)+\left(\frac{\%E_{-V_n}}{3}\right)+\left(\frac{\%E_{-V_o}}{2}\right)+\left(\%E_{V_p}\right)+\left(\frac{\%E_{-V_k}}{4}\right) \tag{4.18}$$

Fig.4.5 shows the percentage of energy shared to load by each source at different modulation index using equations (4.15)-(4.18). From Fig.4.5, it is observed that up to modulation index 0.5 sources V3, V4 are alone supplying energy to the load (V1, V2 also can supply energy alone up to 0.5 modulation index by using redundancy

switching of the topology). As the modulation index increases the energy supplied to load by individual sources are changing. The modulation index cannot be chosen less than 0.75 because for the rated output voltage, the dc bus voltage has to be increased which reduces the proper utilization of resources. To get the regulated output voltage an appropriate range of modulation index is chosen.

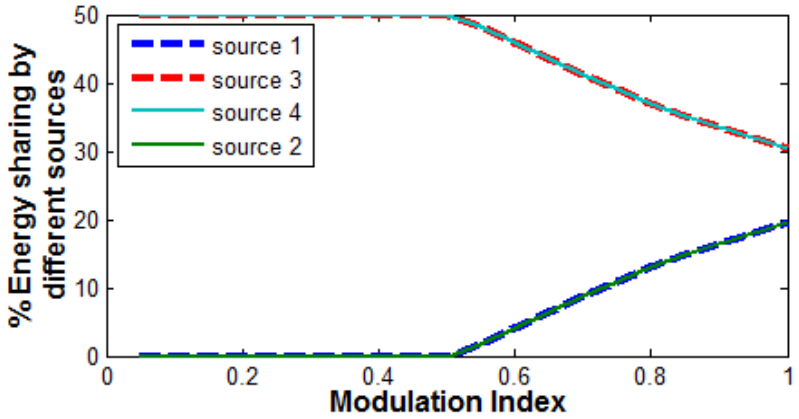

Fig. 4.5 Percentage of energy transferred to load by each source with different modulation index.

For the switching combination presented in Table 4.2, the energy shared by different sources for various modulation index values is depicted in Fig.4.6. From this figure, it can be noticed that at modulation index 0.62, all voltage sources share equal load energy. In this case, the percentage of energy shared to load by different sources is almost constant after 0.85 modulation index. Switching combination presented in Table 4.2 is preferable when the input side voltage fluctuations are more.

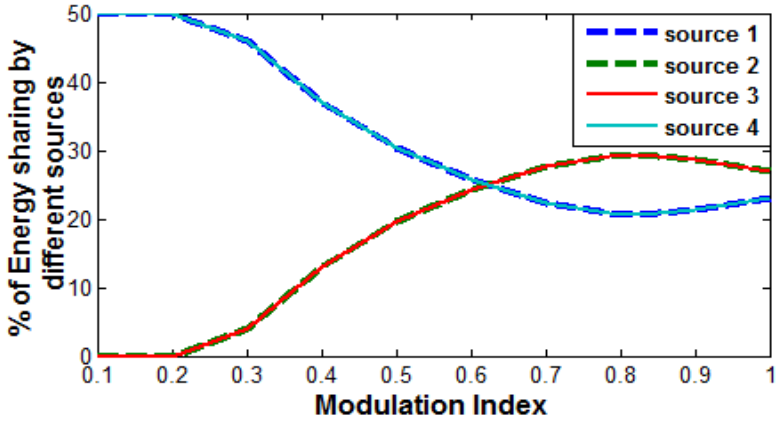

Fig. 4.6 Percentage of energy transferred to load by each source with different modulation index.

For distributing the PV modules among four sources the average operating modulation index of given topology chosen as 0.86. From Fig.4.5, the sources V1,

V2 are sharing 15% (N1=N2=15% of total number of panels) of total PV power individually. Similarly, each sources V3, V4 share 35% (N3=N4=35% total number of panels) of total PV power. The battery rating is chosen according to each individual source, the charging characteristics of each battery are shown next section. Whereas, from Fig.4.6 for modulation index 0.86 the sources V1, V4 each one is sharing 20% and V2, V3 sources share 30% of total PV power.

4.4 Results and discussion

A. Simulation Results

The single phase multilevel inverter is simulated using MATLAB/Simulink. The PV modules are optimally distributed using Fig. 4.5 and Fig. 4.6 for different switching combinations given in Table 4.1 and 4.2. The simulation parameters are given in Table 4.3. The PV string is formed by using series and parallel connection of modules. The photovoltaic module is modelled using [79], which consists of series and parallel cells. Perturb and observe algorithm is adopted to track maximum power [80]. The gating pulses for nine-level inverter are generated using phase disposition carrier pulse width modulation as shown in Fig.4.7. The Table 4.4 gives the switching logic for generating nine-level output voltage across the load.

Table 4.3
Simulation Parameters

	Specifications for Table I Switching Combination	Specifications for Table II Switching Combination
Irradiation	850W/m^2	850W/m^2
PV String 1 and 2 maximum power	300W, 300W	400W, 600W
PV String 3 and 4 maximum power	700W , 700W	600W, 400W
Each Lead acid battery terminal voltage (for simulation)	40V	40V
Load Active power	1400W	1400W
Fundamental frequency	60Hz	60Hz
Modulation Index	0.86	0.86
Switching Frequency	2.3kHz	2.3kHz

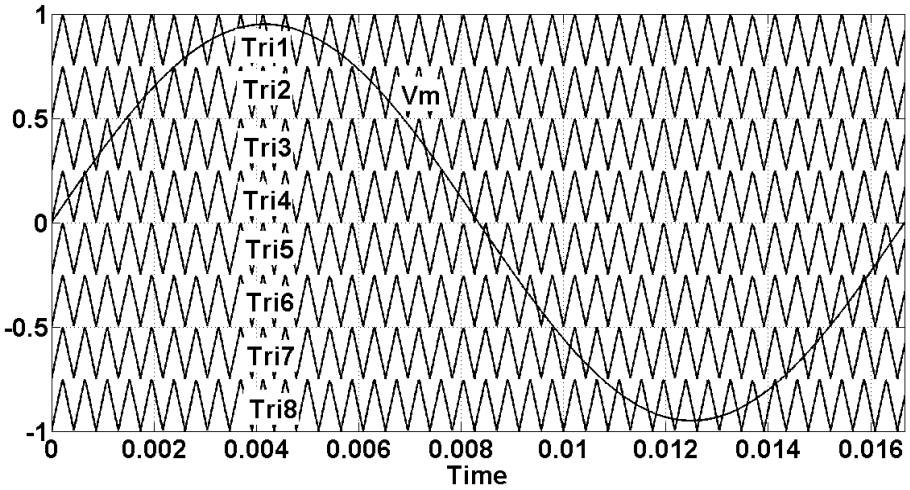

Fig. 4.7 Carrier Pulse width modulation for Nine-level voltage generation

Table 4.4

Comparison of Modulating and Carrier Signal to Generate Nine-Level Voltage

Comparison	Voltage level
Vm > Vtri1	Vdc
Vtri2 < Vm < Vtri1	4Vdc/3
Vtri3 < Vm < Vtri2	Vdc/2
Vtri4 < Vm < Vtri3	Vdc/4
Vtri5 < Vm < Vtri4	0
Vtri6 < Vm < Vtri5	-Vdc/4
Vtri7 < Vm < Vtri6	-Vdc/2
Vtri8 < Vm < Vtri7	-4Vdc/3
Vm < Vtri8	-Vdc

The current waveform of each source is shown in Fig.4.8 for the switching combination given in Table 4.1. The upper two traces shows the currents of corresponding sources V1, V2 and lower two traces are currents associated with V3, V4 sources. The mean value currents of sources V1, V2 are 5A each and for V3, V4 are 12A each. The sources V1, V2 each is sharing 15% energy to load whereas V3, V4 sources are supplying 35% each as shown in Fig.4.8.

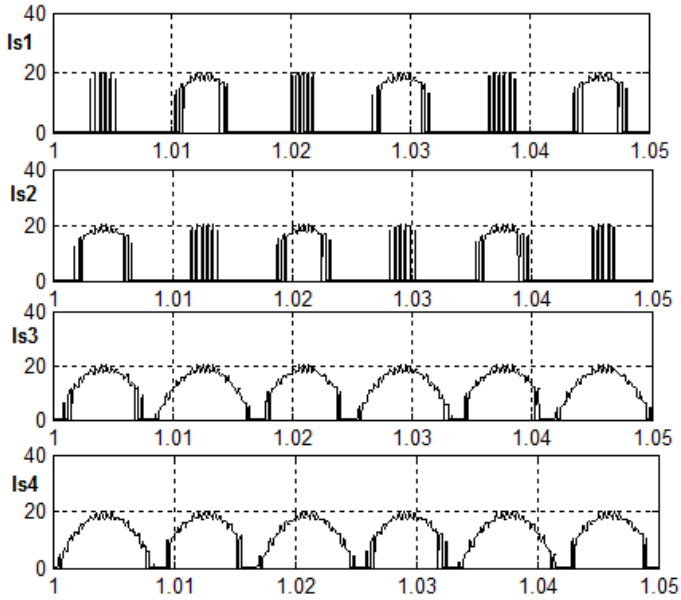

Fig. 4.8 Individual source currents for switching Table 4.1 [Y-axis 20A/div, X-axis 0.01sec/div]

Fig.4.9 depicts the current waveform of four sources for the switching combination given in Table 4.2. From Fig.4.9, it is clearly observed that the currents of V1, V4 (upper trace, lower trace) are same and currents of V2, V3 are equal (middle traces). The mean value of V1, V4 currents are 6.8A and V2, V3 are 9.8A. From Fig.4.9 it is clear that sources V1, V4 each is sharing 20% energy to load whereas V2, V3 sources are supplying 40% each.

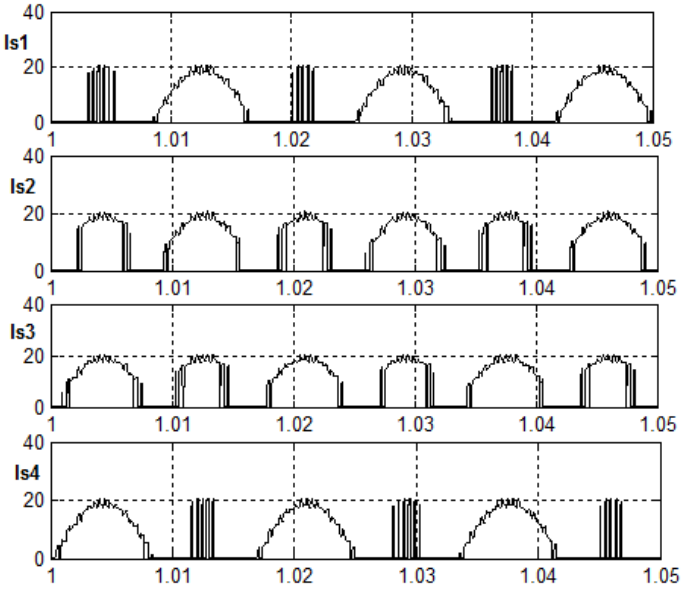

Fig. 4.9 Individual source currents for switching Table 4.2 [Y-axis 20A/div, X-axis 0.01sec/div]

The charging characteristics of each battery are shown in Fig.4.10 after distribution of panels. From Fig.4.10 it can be observed all the batteries are charging at same rate.

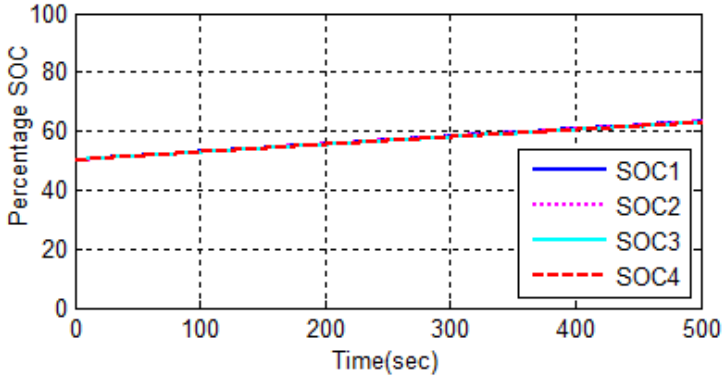

Fig. 4.10 Charging characteristics of each battery after rearrangement of solar panels

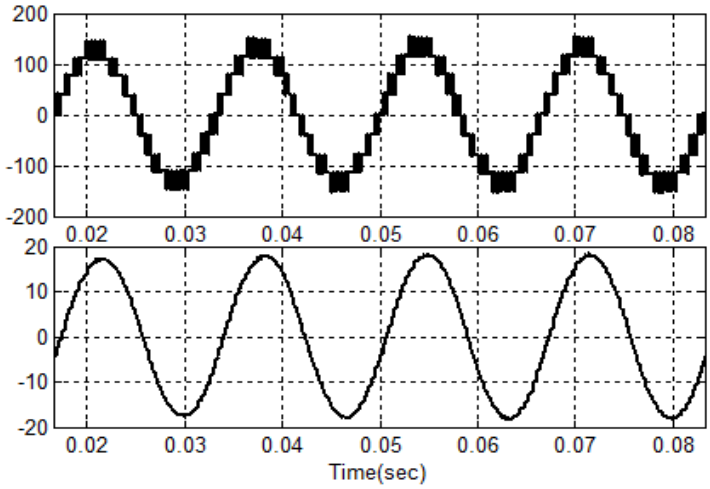

Fig. 4.11 Nine-level output voltage and load current waveform with symmetrical voltage sources [Y-axis: Voltage]

The nine-level output voltage and load current waveforms are shown in Fig.4.11. Then nine-level voltage is generated using switching sequence given in Table 4.1 for symmetrical voltage sources.

B. Experimental Results

The laboratory prototype is developed and tested using DC sources. The voltage rating of each source is 40V. For evaluation of experimental prototype Spartan6 FPGA controller used for generating pulses to inverter switches. A dead band circuit is used to provide delay of 2.5μs for complementary switches. The switching

frequency and modulation index used are same as simulation results. The input currents of each source are shown in Fig.4.12 for switching combination given in Table 4.1. In this figure, upper two traces represent the V1, V2 source currents and lower traces represent the V3 and V4 source currents. The mean value of V1, V2 source currents are less than the V3, V4 source currents. From Fig.4.12, it can be observed that the energy supplied to load by individual sources is different because of inverter structure and switching sequence. The source currents for switching combination mentioned in Table 4.2 are shown in Fig.4.13. From this figure, the energy supplied to load by sources V1, V4 are equal where as V2, V3 are same. The nine level output voltage across load and current waveform through load are depicted in Fig. 4.14.

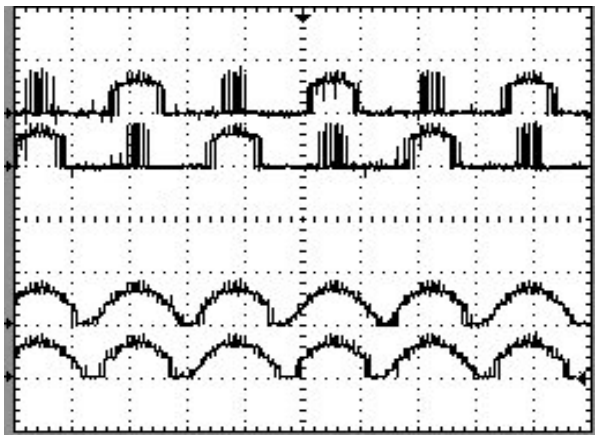

Fig. 4.12 Current waveforms of each source for switching Table 4.1 (Upper trace: V1, V2 source currents, lower trace: V3,V4 source currents) [Y-Axis 2A/div; X-axis 5msec/div]

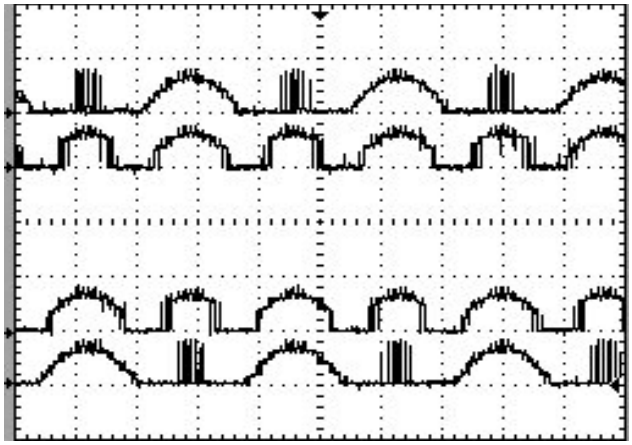

Fig. 4.13 Current waveforms of each source for switching Table 4.2 (Upper trace: V1, V2 source currents, lower trace: V3,V4 source currents) [Y-Axis 2A/div; X-axis 5msec/div]

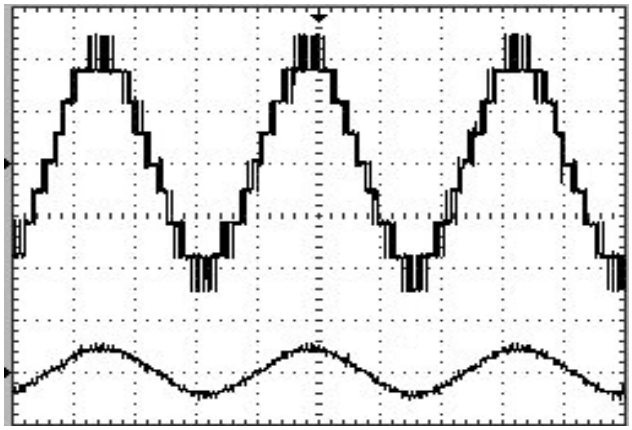

Fig. 4.14 Nine-level output voltage and load current waveform with symmetrical voltage sources [Y-axis 50v/div, 2A/div; X-axis 5msec/div]

4.5 Improved Fault tolerant nine-level inverter configuration

In the above discussed multilevel inverter configuration, if any leg of the full bridge fails then it is difficult to operate. To improve the fault tolerant capability two extra switches S9, S10 are introduced as shown in Fig. 4.15. To divide the PV panels equally among four sources a switching combination is presented and validated using simulation and experimental results.

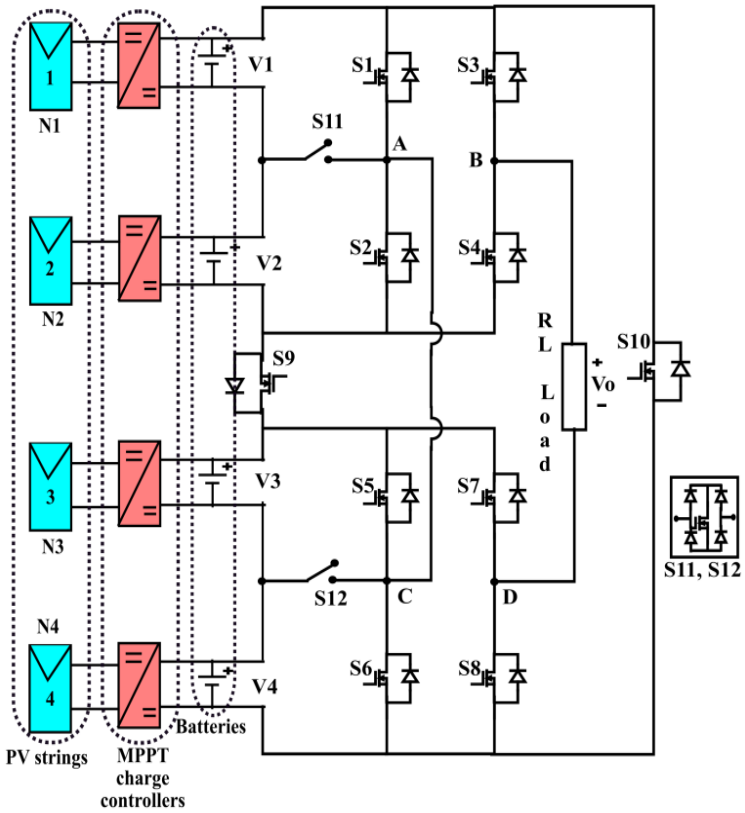

Fig 4.15 Proposed nine-level inverter topology

The block diagram of nine-level single phase inverter is shown in Fig.4.15. The topology is formed by using two full bridge inverter structures (S1-S4 and S5-S8), two bidirectional switches (S11, S12) and switches S9 and S10 are connected between sources shown in Fig.4.15. The available switching combination to generate nine-level output voltage is given in Table 4.5. The voltage rating of semiconductor switches are S1-S8 is Vdc/2 and S9, S10 are Vdc and S11, S12 is Vdc/4. Here the switches S9, S10, S11 and S12 provide redundant switching combinations for fault tolerant operation and energy sharing between sources.

Table 4.5

Switching Sequence for Nine-Level Operation

Voltage levels	Possible number of switching combinations
Vdc	S3,S8,S9 (or) S3,S8,S5,S2
3Vdc/4	S3,S8,S12,S2 (or) S5,S11,S3,S8
Vdc/2	S3,S7,S9 (or) S9,S4,S8 (or) S3,S8,S6,S2 (or) S5,S2,S4,S8 (or) S5,S1,S3,S8 (or) S3,S7,S5,S2 (or) S3,S8,S12,S11
Vdc/4	S3,S7,S5,S11 (or) S3,S8,S6,S11 (or) S12,S2,S4,S8 (or) S12,S1,S3,S8
0	S3,S10,S8 (or) S4,S9,S7 (or) S2,S4,S5,S7
-Vdc/4	S11,S5,S7,S4 (or) S11,S6,S8,S4 (or) S7,S4,S2,S12 (or) S7,S3,S1,S12
-Vdc/2	S7,S3,S10 (or) S10,S8,S4 (or) S7,S4,S2,S6 (or) S7,S3,S1,S6 (or) S1,S5,S7,S4 (or) S1,S6,S8,S4 (or) S11,S12,S7,S4
-3Vdc/4	S7,S4,S11,S6 (or) S1,S12,S7,S4
-Vdc	S10,S7,S4 (or) S1,S6,S7,S4

4.5.1 Distribution of PV panels equally among four sources

To distribute the PV panels equally among four sources the switching combination and corresponding source selection is given in Table 4.6. This table also gives the logic for generating nine level output voltage across the load.

Table 4.6
Switching Combination for Nine-Level Operation
(V1=V2=V3=V4=Vdc/4)

Voltage levels	Switching sequence	Corresponding Sources
Vdc	S3,S8,S5,S2 or S3,S8,S9	V1,V2,V3,V4
3Vdc/4	S3,S8,S12,S2	V1,V2,V4
Vdc/2	S5,S1,S3,S8 or S9,S4,S8	V3,V4
Vdc/4	S12,S1,S3,S8	V4
0	S1,S3,S6,S8	0
-Vdc/4	S7,S3,S1,S12	V3
-Vdc/2	S7,S3,S1,S6 or S7,S3,S10	V3,V4
-3Vdc/4	S7,S4,S1,S12	V1,V2,V3
-Vdc	S7,S4,S1,S6 or S10,S7,S4	V1,V2,V3,V4

The panels are distributed among four sources according to percentage energy sharing of each source. The percentage energy shared to load is calculated for fundamental cycle using equations (4.19)-(4.22). The divisions $1/4^{th}$,$1/3^{rd}$, ½ are because for higher level 4 sources are equally sharing the energy for Vdc voltage level.

$$\%E_{V1}=\left(\frac{\%E_{V_k}}{4}\right)+\left(\frac{\%E_{V_n}}{3}\right)+\left(\frac{\%E_{-V_n}}{3}\right)+\left(\frac{\%E_{-V_k}}{4}\right) \tag{4.19}$$

$$\%E_{V2}=\left(\frac{\%E_{V_k}}{4}\right)+\left(\frac{\%E_{V_n}}{3}\right)+\left(\frac{\%E_{-V_n}}{3}\right)+\left(\frac{\%E_{-V_k}}{4}\right) \tag{4.20}$$

$$\%E_{V3}=\left(\frac{\%E_{V_k}}{4}\right)+\left(\frac{\%E_{V_o}}{2}\right)+\left(\frac{\%E_{-V_n}}{3}\right)+\left(\frac{\%E_{-V_o}}{2}\right)+\left(\%E_{-V_p}\right)+\left(\frac{\%E_{-V_k}}{4}\right) \tag{4.21}$$

$$\%E_{V4}=\left(\frac{\%E_{V_k}}{4}\right)+\left(\frac{\%E_{V_n}}{3}\right)+\left(\frac{\%E_{V_o}}{2}\right)+\left(\frac{\%E_{-V_o}}{2}\right)+\left(\%E_{V_p}\right)+\left(\frac{\%E_{-V_k}}{4}\right) \tag{4.22}$$

Fig.4.16 shows the percentage of energy shared to load by each source at different modulation index using equations (4.19)-(4.22). From Fig.4.16 up to modulation index 0.5 sources V3, V4 are alone supplying energy to the load (V1, V2 also can supply energy alone up to 0.5 modulation index by using redundancy switching of the topology). As the modulation index increases the energy supplied to load by individual sources are changing. The modulation index cannot be chosen less than 0.75 because for the rated output voltage, the dc bus voltage has to be increased which reduce the proper utilization of resources. From Fig.4.16, it can be observed that from 0.82 to 1 modulation index the energy shared to load by each source is equal. To get the regulated output voltage an appropriate range of modulation index is chosen.

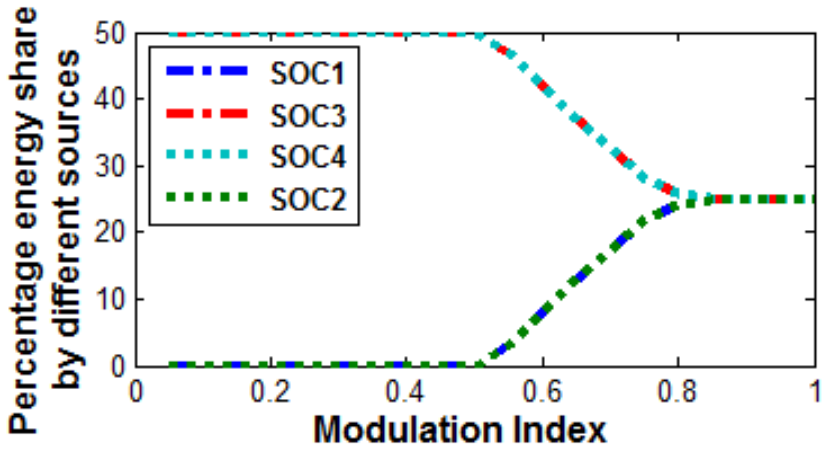

Fig. 4.16 Percentage of energy transferred to load by each source with different modulation index.

4.5.2 Fault analysis of proposed topology

The topology with symmetrical sources has analyzed for different open circuit switch failures. The different fault detection techniques for IGBT failure are given in [23]. In this chapter the fault detection techniques are not considered only possible output voltage levels for different open circuit switch faults are considered. Table 4.7 shows the possible number of voltage levels for different switch open circuit failures. During fault, the output voltage is generated by bypassing the faulty switch using redundant switching states given in Table 4.5. From Table 4.7, it can be observed the proposed topology capable of maintaining same nine-level output voltage as normal operation. But, for some of the fault (open circuit fault of S3 or S4 or S7 or S8) the

five-level output voltage generated with half of the rated voltage. This can be applicable for some of the loads which can be operated at wide range of voltages like led lights, electronic gadgets, etc.

Table 4.7
Proposed Nine-Level Topology for Different Switch Failures

Possible voltage levels	Different Switch failures
Nine-Level voltage	S1 and S2 or S5 and S6 or S9 and S10 or S11 or S12
Five-level voltage	S3 or S4 or S7 or S8 or S9, S10, S11, S12

4.5.3 Control scheme

The gating pulses for nine-level inverter are generated using phase disposition carrier pulse width modulation as shown in Fig.4.17. The modulating signal (Vm) is compared with eight carrier (triangular wave) signals (Tri1 to Tri8) and corresponding pulses are given to the switches to achieve nine-level output voltage using switching combination given in Table 4.6. In the event of switch open circuit fault the five-level voltage is generated by comparing the carrier signal Tri3 to Tri6 with modulating signal.

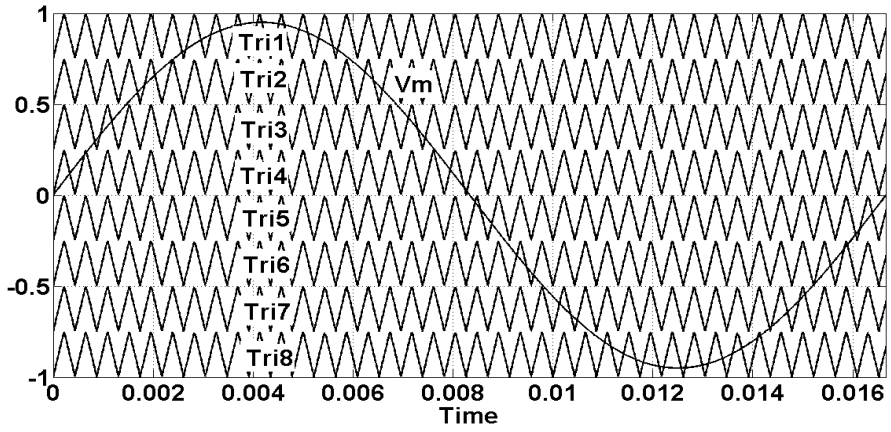

Fig.4.17 Carrier Pulse width modulation

4.5.4 Results and Discussion

A. Simulation Results

The single phase multilevel inverter is simulated using MATLAB/Simulink. The PV modules are equally distributed among four sources using switching combinations given in Table 4.6. The simulation parameters are given in Table 4.8. The PV string

is formed by using series and parallel connection of modules. The photovoltaic module is modelled using [79], which consists of series and parallel cells. Perturb and observe algorithm is adopted to track maximum power [80]. The current waveform of each source is shown in Fig.4.18 for the switching combination given in Table 4.6. The upper two traces shows the currents of corresponding sources V1, V2 and lower two traces are currents associated with V3, V4 sources. The mean values of all currents are equal to 10A. The Fig.4.18, it is clear that all sources V1, V2, V3, and V4 each is sharing 25% energy to load.

Table 4.8
Simulation Parameters

Irradiation	850W/m^2
PV String 1 and 2 maximum power	500W, 500W
PV String 3 and 4 maximum power	500W , 500W
Each Lead acid battery terminal voltage (for simulation)	40V
Load Active power	1400W
Fundamental frequency	60Hz
Modulation Index	0.95
Switching Frequency	2.3kHz

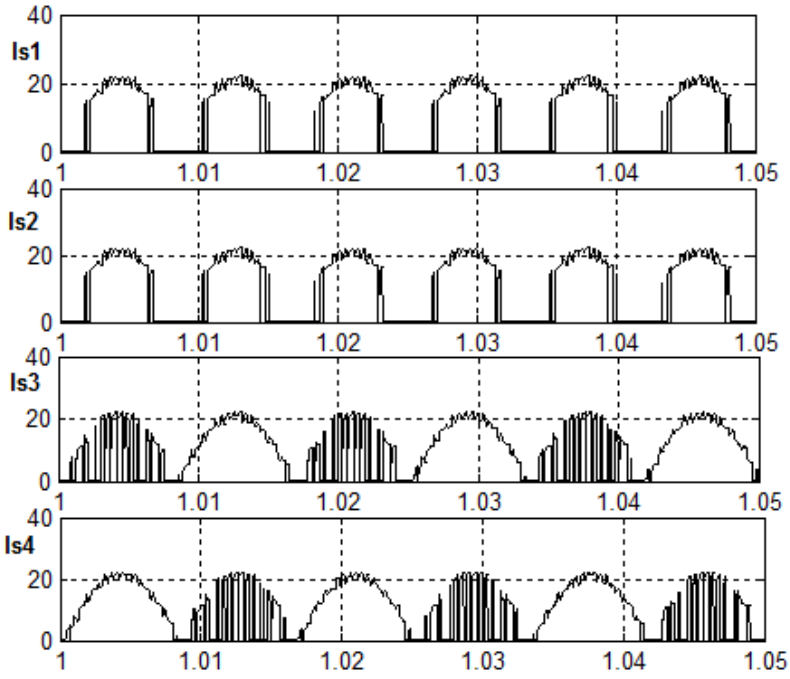

Fig. 4.18 Individual source currents [Y-axis: Current in Ampere, X-axis: Time in sec]

The nine-level output voltage across load and load current waveform are shown in Fig.4.19 for modulation index of 0.95. All batteries are charging and discharging at same rate which can be observed from Fig. 4.20.

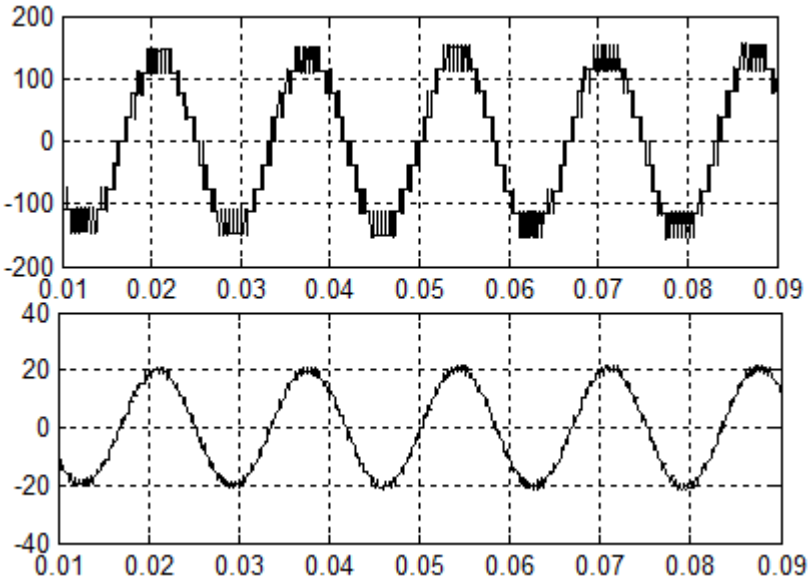

Fig. 4.19 Nine-level output voltage and load current waveforms [Y-axis 100v/div, 20A/div; X-axis 0.01sec/div]

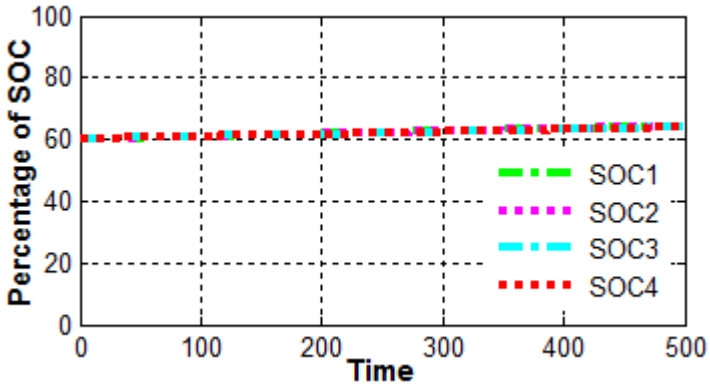

Fig. 4.20 Charging characteristics of batteries

The topology has fault tolerant capability for different switch open circuit faults which is discussed in previous section. Fig.4.22 (a) gives five-level output voltage with same voltage magnitude as normal operation during the switches S9, S10, S11 and S12 open circuit fault. Fig. 4.22 (b) shows the voltage across full bridges.

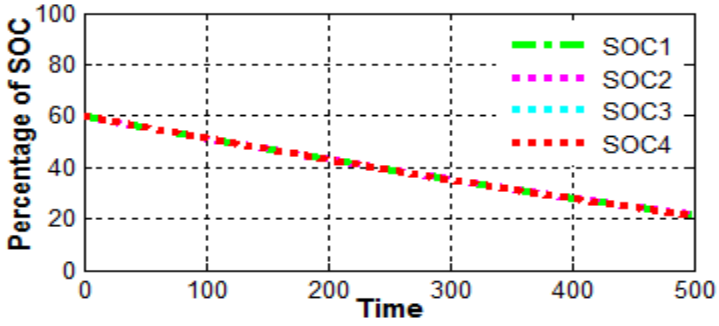

Fig. 4.21 Discharge characteristics of batteries

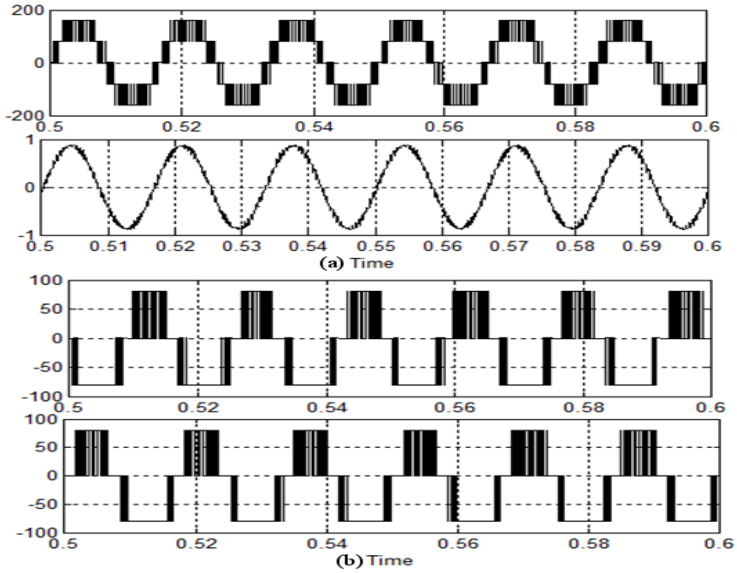

Fig.4.22 Simulation results (a) Five level output voltage and current through load during S9-S12 switch open-circuit fault (b) Two full bridge mid-point voltages during switch failure.

B. Experimental Results

The laboratory prototype is developed and tested using DC sources. The voltage rating of each source is 40V. For evaluation of experimental prototype SPARTAN6 FPGA controller used for generating pulses to inverter switches. A dead band circuit is used to provide delay of 2.5µs for complementary switches. The switching frequency and modulation index used are same as simulation results. The input currents of each source is shown in Fig.4.23 for switching combination given in Table 4.6, upper two traces shows V1, V2 source currents and lower traces are V3 and V4 source currents**.** The nine-level output voltage and current through load are shown in Fig. 4.24. The five-level output voltage during S9-S10 switch open circuit failure is shown in Fig.4.25 (a). The voltage across full bridge is shown in Fig. 4.25(b).

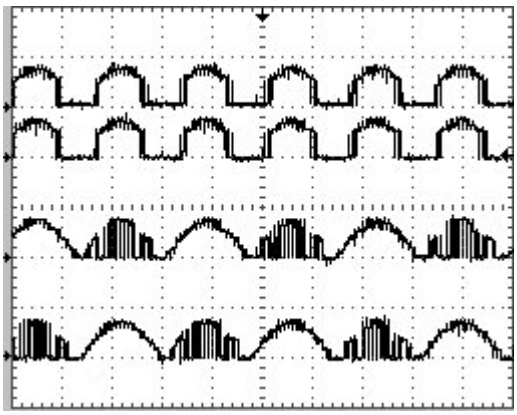

Fig. 4.23 Individual source currents [Y-axis 20A/div, X-axis 0.01sec/div]

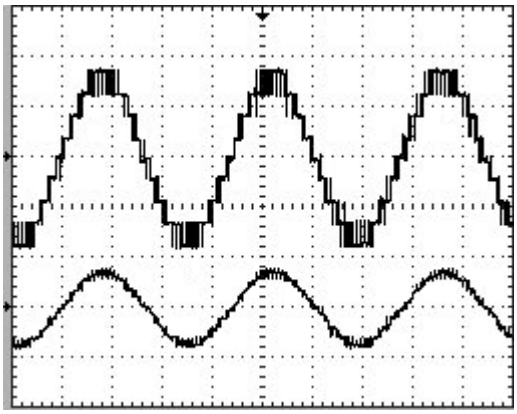

Fig. 4.24 Nine-level output voltage and load current waveforms [Y-axis 100v/div, 2A/div; X-axis 0.01sec/div]

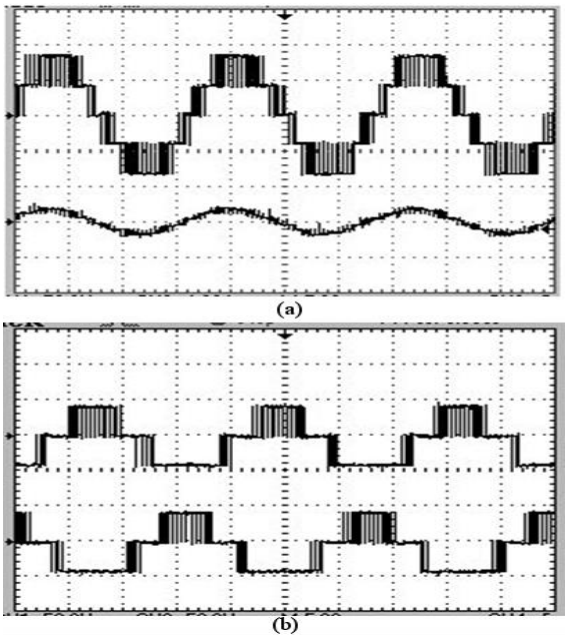

Fig.4.25 Experimental results (a) Five level output voltage and current through load during S9-S10 switch open-circuit fault (b) Two full bridge mid-point voltages during switch failure. [Y-axis 50V/div, X-axis 5msec/div]

4.6 Conclusion

In this chapter, an optimized source distribution scheme for a nine-level inverter fed with four PV sources is presented. The PV modules are divided based on equivalent load demand and average operating modulation index. Similarly, battery ratings are decided based on the modified rating of the sources which ensures better source utilization. The detailed mathematical analysis has been carried out for effective loading of individual sources for nine-level inverter. To improve the fault tolerance capability of the conventional cascaded T-type 9-level inverter is modified by adding two extra switches. The switching redundancy of the modified inverter during open circuit switch failure conditions is helps to supply the power with or without changing the voltage levels. The results show the ability of proposed topology working under normal and fault conditions. Simulation of the proposed scheme has been carried out in MATLAB Simulink. Experimental validation has been done with the help of laboratory prototype.

Chapter 5

Overview and Future Scope of the thesis

5.1 Overview of the thesis

This thesis mainly focused on fault tolerant multilevel inverter configurations with energy balancing capability for off-grid PV applications. The aim of these fault tolerant multilevel inverters is to provide continuous power supply to essential loads under fault operation. In literature different fault identification techniques are presented for inverters but to continue the operation after isolation of fault not much discussed. Also few papers addressed the load energy sharing problem between sources of multilevel inverters for photovoltaic application.

In chapter 2, single phase and three phase fault tolerant multilevel inverter topologies are presented and examined for various switch open circuit fault and/or source failures. These topologies are formed by combining three-level neutral point clamped inverter, two-level half bridge inverter, bidirectional switches and full bridge t-type inverter. The fault tolerance is achieved by using the redundant switching states of middle voltage levels of multilevel inverter.

The energy balancing between sources is achieved for the five-level inverter fed with two separate PV sources due to partial shading and/or hotspots in chapter 3. Because of partial shading the associated batteries with these panels will charge and discharge unevenly and creates voltage difference between terminal voltages of sources because of SOC difference. The energy balance between batteries is achieved for all operating conditions by selecting appropriate switching combination. For example the battery with low SOC is discharged at slower rate than the battery with more SOC until both SOC's are equal. This also helps in minimization of DC offset

into the ac side output voltage. The mathematical analysis is presented for possible percentage of energy shared to load by both the sources.

In chapter 4, single phase multilevel inverter with improved reliability in terms of switch open circuit failures and energy balancing between sources. The topology requires four isolated DC-sources; these isolated DC voltage sources are realized with multiple PV strings with associated batteries. The investigations for load energy sharing between sources for different switching combinations are presented for a nine-level inverter. An optimal distribution of PV panels for different switching combination based on mathematical analysis is presented. The operation of proposed multilevel single phase inverter is analyzed for different switch open-circuit failures.

All the above topologies are simulated using Matlab Simulink and experimentally verified. The pwm pulses are generated using FPGA based XILINX Spartan-6 XC6SLX9 board, dSPACE controller. The experimental prototype pictures are shown in Fig. 5.1 to Fig. 5.2. The 5KW off-grid generation system with lead acid batteries and charge controllers are shown in Fig.5.3 and Fig.5.4. The VHDL program for PWM signal generation is given in APPENDIX-I.

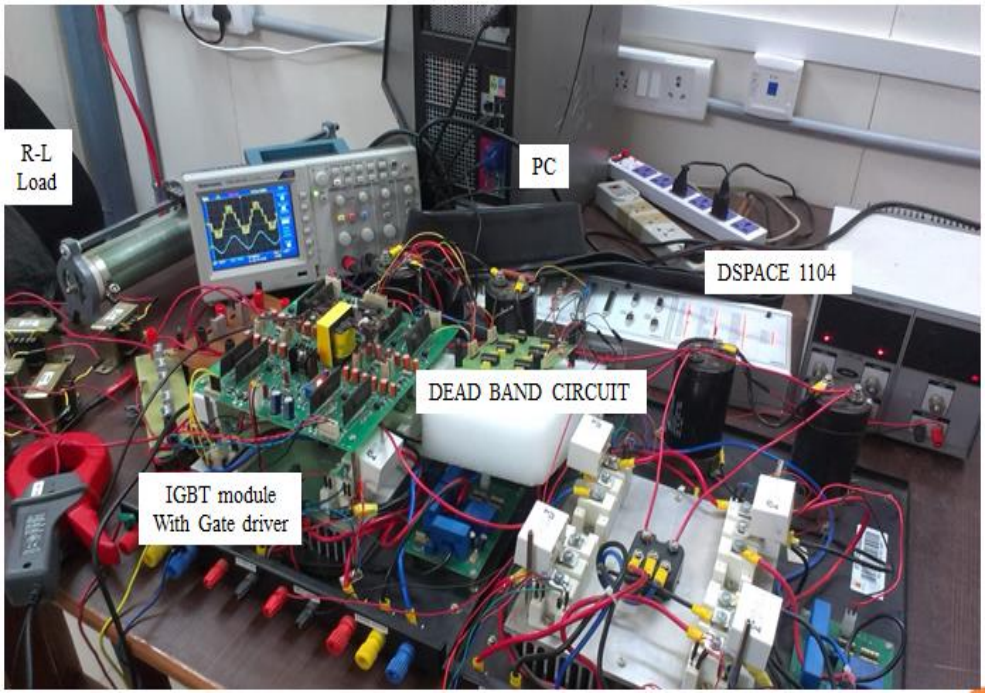

Fig.5.1 Laboratory prototype fault tolerant five-level inverter

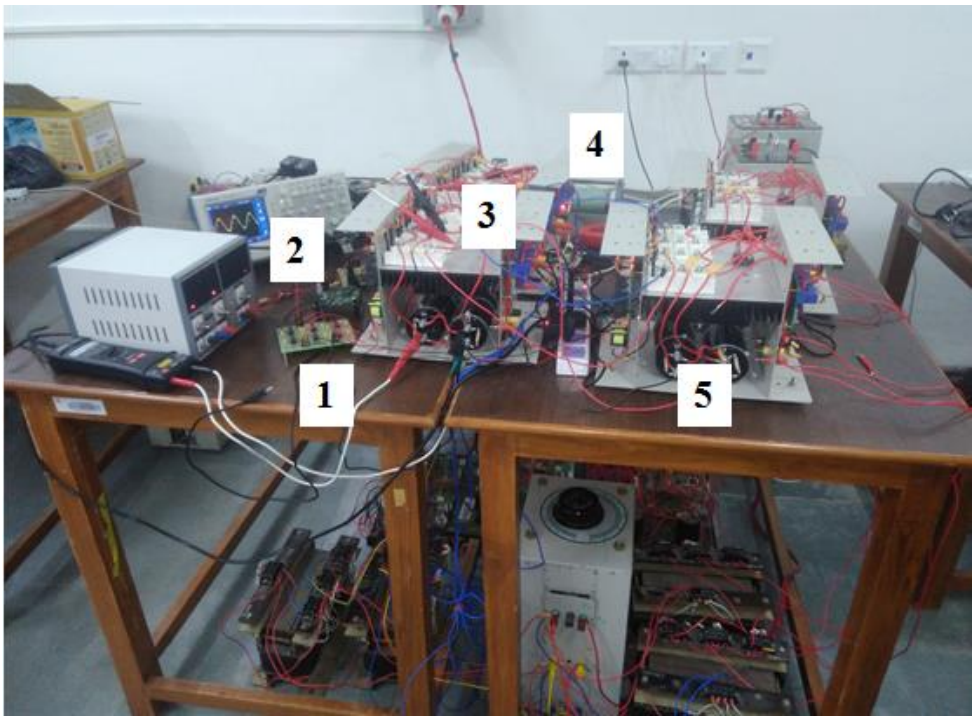

Fig.5.2 Laboratory prototype fault tolerant Nine-level inverter 1) Dead band circuit 2) FPGA controller 3)IGBT Modules with Gate driver 4)R-L Load 5) Rectifier circuit

Fig.5.3 5KW off-grid PV generation system

Fig.5.4 Lead acid batteries with charge controllers

5.2 Suggestions for future scope

The fault tolerant multilevel inverter topologies for off grid PV generation system are presented. These topologies are analyzed for different switch open circuit faults this can be further extended for analyzing various short circuit faults, improving of output voltage magnitude under fault condition and also for grid integration.

In chapter 3 and 4 the energy balancing issues of five-level and nine-level inverter are discussed. Mathematical analysis is given for energy transferred to load by each source for five level and nine-level inverter configurations fed with symmetrical voltage sources in a fundamental cycle. This can be further analyzed for ‘n’ number of voltage levels and asymmetrical voltage sources. These concepts can be extended for electric vehicle and induction motor drives applications.

Appendix-I

VHDL Program for Implementing Five-level Carrier SPWM

```
library ieee;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;   --try to use this library as much as possible.
entity fivelevel is
port (clk :in  std_logic;
    pwm1 : out std_logic;
     pwm2 : out std_logic;
     pwm3 : out std_logic;
     pwm4 : out std_logic;
     pwm5 : out std_logic;
     pwm6 : out std_logic;
     pwm7 : out std_logic;
     pwm8 : out std_logic;
     pwm9 : out std_logic;
     pwm10 : out std_logic;
     pwm11 : out std_logic;
     pwm12 : out std_logic;
     pwm13 : out std_logic;
     pwm14 : out std_logic;
     pwm15 : out std_logic;
     pwm16 : out std_logic;
     pwm17 : out std_logic;
     pwm18 : out std_logic;
```

```
        pwm19 : out std_logic;
        pwm20 : out std_logic;
        pwm21 : out std_logic
            );
end fivelevel;
architecture Behavioral of fivelevel is
signal a : integer range 0 to 3600:=0;
signal b : integer range 0 to 3600:=3200;
signal c : integer range 0 to 3600:=2800;
signal d : integer range 0 to 3600:=2400;
signal e : integer range 0 to 3600:=2000;
signal f : integer range 0 to 3600:=1600;
signal g : integer range 0 to 3600:=1200;
signal h : integer range 0 to 3600:=800;
signal i : integer range 0 to 3600:=400;
signal sine1 : integer range -2047 to 2047:=0;
signal sine4 : integer range -2047 to 2047:=0;
signal sine7 : integer range -2047 to 2047:=0;
signal s1 : integer range -2047 to 2047:=0;
signal s2 : integer range -2047 to 2047:=0;
signal s3 : integer range -2047 to 2047:=0;
signal s4 : integer range -2047 to 2047:=0;
signal s5 : integer range -2047 to 2047:=0;
signal s6 : integer range -2047 to 2047:=0;
signal tring1 : integer :=0;
signal tring2 : integer :=0;
signal btrig : integer :=0;
signal btrig1 : integer :=0;
signal btrig2 : integer :=0;
signal btrig3 : integer :=0;
signal btrig4 : integer :=0;
signal btrig5 : integer :=0;
```

```
signal btrig6 : integer :=0;
signal btrig7 : integer :=0;
signal btrig8 : integer :=0;
signal btrig9 : integer :=0;
signal z :integer :=0;
signal y :integer :=150;
signal x :integer :=120;
signal w :integer :=0;
signal v :integer :=0;
signal clk_out : std_logic:='0';
signal a1 : std_logic:='0';
signal a2 : std_logic:='0';
signal a3 : std_logic:='0';
signal a4 : std_logic:='0';
signal a5 : std_logic:='0';
signal a6 : std_logic:='0';
signal a7 : std_logic:='0';
signal a8 : std_logic:='0';
signal a9 : std_logic:='0';
signal a10 : std_logic:='0';
signal a11 : std_logic:='0';
signal a12 : std_logic:='0';
signal a13 : std_logic:='0';
signal a14 : std_logic:='0';
signal a15 : std_logic:='0';
signal a16 : std_logic:='0';
signal a17 : std_logic:='0';
signal a18 : std_logic:='0';
signal a19 : std_logic:='0';
signal a20 : std_logic:='0';
signal a21 : std_logic:='0';
signal a22 : std_logic:='0';
```

```
  signal a23 : std_logic:='0';
  signal a24 : std_logic:='0';
  signal count : integer range 0 to 5555 :=0;
  signal clk_out1 : std_logic:='0';
  signal count1 : integer range 0 to 5555 :=0;
  signal j : integer range 0 to 180:=0;
  signal k : integer range 0 to 180:=90;
  type memory_type1 is array (0 to 180) of integer range -2047 to 2047;
type memory_type is array (0 to 3600) of integer range -2047 to 2047;
```

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```
   signal b : integer range 0 to 3600:=1200;
   signal b1 : integer range 0 to 3600:=3000;
   signal c : integer range 0 to 3600:=2400;
   signal c1 : integer range 0 to 3600:=600;
   signal sine11 : integer range -2047 to 2047:=0;
   signal sine12 : integer range -2047 to 2047:=0;
   signal sine21 : integer range -2047 to 2047:=0;
   signal sine22 : integer range -2047 to 2047:=0;
   signal sine31 : integer range -2047 to 2047:=0;
   signal sine32 : integer range -2047 to 2047:=0;
   signal atrig : integer :=0;
   signal btrig : integer :=0;
   signal z :integer :=0;
   signal Vst :integer :=1023;
   signal clk_out : std_logic:='0';
   signal count : integer range 0 to 5555 :=0;
   signal clk_out1 : std_logic:='0';
   signal count1 : integer range 0 to 5555 :=0;
   type memory_type is array (0 to 3600) of integer range -2047 to 2047;
   signal sine : memory type :=
  (0,1,3,5,7,8,10,12,14,16,17,19,21,23,25,26,28,30,32,33,35,37,39,41,42,44,46,
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,207,205,204,202,200,198,197,195,193,191,190,188,186,184,183,181,179,17
7,176,174,172,170,169,167,165,163,161,160,158,156,154,153,151,149,147,1
46,144,142,140,138,137,135,133,131,130,128,126,124,123,121,119,117,115,
114,112,110,108,107,105,103,101,99,98,96,94,92,91,89,87,85,83,82,80,78,76
,74,73,71,69,67,66,64,62,60,58,57,55,53,51,50,48,46,44,42,41,39,37,35,33,32
,30,28,26,25,23,21,19,17,16,14,12,10,8,7,5,3,1,0,-1,-3,-5,-7,-8,-10,-12,-14,-
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```
42,-41,-39,-37,-35,-33,-32,-30,-28,-26,-25,-23,-21,-19,-17,-16,-14,-12,-10,-8,-
7,-5,-3,-1,0);
begin
process (clk)
begin
if (rising_edge(clk)) then
if (count= 139)then
clk_out <= not (clk_out);
count <= 0;
else
count <= count+1;
end if;
if (count1= 555/8)then
clk_out1 <= not (clk_out1);
count1 <= 0;
else
count1 <= count1+1;
end if;
end if;
end process;
process(clk)
begin
 if(rising_edge(clk_out)) then
sine1 <= sine(a);
sine4 <= sine(d);
sine7 <= sine(g);
a <= a+ 1;
d <= d+ 1;
g <= g+ 1;
if(a = 3599) then
a <= 0;
end if;
```

```
if(d = 3599) then
d <= 0;
end if;
if(g = 3599) then
g <= 0;
end if;
end if;
end process;
process(clk)
begin
if(rising_edge(clk_out)) then
if(sine1 > sine4 and sine1 > sine7) then
  max1 <= sine1;
    if (sine4 > sine7)then
       min1 <= sine7;
      else
      min1 <= sine4;
 end if;
    elsif(sine4 > sine1 and sine4 > sine7) then
       max1<= sine4;
        if (sine1 > sine7)then
        min1 <= sine7;
        else
        min1 <= sine1;
    end if;
    elsif(sine7 > sine1 and sine7 >sine4) then
        max1 <= sine7;
        if (sine1 > sine4)then
        min1 <= sine4;
        else
        min1 <= sine1;
    end if;
```

```
end if;
end process;
process(clk)
begin
if(rising edge(clk_out1)) then
z <= z+1;
y <= y+1;
x <= x+1;
w <= w+1;
v <= v+1;
j <= j + 1;
k <= k + 1;
--l <= l + 1;
--m <= m + 1;
--n <= n + 1;
--o <= o + 1;
if(j = 179) then
j <= 0;
end if;
if(k = 179) then
k <= 0;
end if;
if (x <= 90) then
btrig2 <= x*6;
elsif ((x >=90) and (x<=(180))) then
btrig2 <= (180-x)*6;
elsif (x>=180) then
x<= 0;
end if;
btrig3 <= -btrig2;
btrig1 <=(btrig2+540);
btrig4 <=(btrig3-540);
```

```
end if;
end process;
process(clk)
begin
 if(rising_edge(clk_out1)) then
  if (sine1 > btrig1) then
  a1 <= '1';
  else
  a1 <='0';
  end if;
    if (sine1 <= btrig1) then
  a2 <= '1';
  else
  a2 <='0';
  end if;
    if (sine1 > btrig2) then
  a3 <= '1';
  else
  a3 <='0';
  end if;

  if (sine1 <= btrig2) then
   a4 <= '1';
   else
   a4 <= '0';
   end if;
   if (sine1 > btrig3) then
   a5 <= '1';
   else
   a5 <= '0';
   end if;
   if (sine1 <= btrig3) then
```

```
  a6 <= '1';
  else
  a6 <= '0';
  end if;
  if (sine1 > btrig4) then
  a7 <= '1';
  else
  a7 <= '0';
  end if;
  if (sine1 <= btrig4) then
  a8 <= '1';
  else
  a8 <= '0';
  end if;
 if (sine4 > btrig1) then
  a9 <= '1';
  else
  a9 <='0';
  end if;
 if (sine4 <= btrig1) then
  a10 <= '1';
 else
  a10 <='0';
 end if;
if (sine4 > btrig2) then
  a11 <= '1';
 else
  a11 <='0';
 end if;
  if (sine4 <= btrig2) then
    a12 <= '1';
  else
```

```
   a12 <= '0';
  end if;
  if (sine4 > btrig3) then
   a13 <= '1';
  else
   a13 <= '0';
  end if;
  if (sine4 <= btrig3) then
   a14 <= '1';
  else
   a14 <= '0';
  end if;
  if (sine4 > btrig4) then
   a15 <= '1';
  else
   a15 <= '0';
  end if;
  if (sine4 <= btrig4) then
   a16 <= '1';
  else
   a16 <= '0';
   end if;
if (sine7 > btrig1) then
   a17 <= '1';
  else
   a17 <='0';
  end if;
if (sine7 <= btrig1) then
  a18 <= '1';
else
  a18 <='0';
end if;
```

```
if (sine7 > btrig2) then
  a19 <= '1';
 else
  a19 <='0';
end if;
 if (sine7 <= btrig2) then
    a20 <= '1';
 else
    a20 <= '0';
 end if;
 if (sine7 > btrig3) then
   a21 <= '1';
 else
   a21 <= '0';
 end if;
 if (sine7 <= btrig3) then
   a22 <= '1';
 else
   a22 <= '0';
 end if;
 if (sine7 > btrig4) then
   a23 <= '1';
 else
   a23 <= '0';
 end if;
 if (sine7 <= btrig4) then
   a24 <= '1';
 else
   a24 <= '0';
   end if;
   pwm1 <= a1 or (a2 and a3) or (a4 and a5);
   pwm2 <= a1 or (a2 and a3) or (a4 and a5);
```

```
    pwm3 <= (a6 and a7) or a8;
    pwm4 <= (a6 and a7) or a8;
    pwm5 <= (a2 and a3) or (a6 and a7);
    pwm6 <= (a4 and a5) or a8;
    pwm7 <= a1;
    pwm8 <= a9 or (a10 and a11) or (a12 and a13);
    pwm9 <= a9 or (a10 and a11) or (a12 and a13);
    pwm10 <= (a14 and a15) or a16;
    pwm11 <= (a14 and a15) or a16;
    pwm12 <= (a10 and a11) or (a14 and a15);
    pwm13 <= (a12 and a13) or a16;
    pwm14 <= a9;
    pwm15 <= a17 or (a18 and a19) or (a20 and a21);
    pwm16 <= a17 or (a18 and a19) or (a20 and a21);
    pwm17 <= (a22 and a23) or a24;
    pwm18 <= (a22 and a23) or a24;
    pwm19 <= (a18 and a19) or (a22 and a23);
    pwm20 <= (a20 and a21) or a24;
    pwm21 <= a17;
       end if;
    end process;
end Behavioral;
```

VHDL PROGRAM FOR DECOUPLED SVPWM

```
library ieee;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;  --try to use this library as much as possible.
entity dual1 is
port (clk :in  std_logic;
      pwm1 : out std_logic;
      pwm2 : out std_logic;
      pwm3 : out std_logic;
      pwm4 : out std_logic;
      pwm5 : out std_logic;
      pwm6 : out std_logic;
      pwm7 : out std_logic;
      pwm8 : out std_logic;
      pwm9 : out std_logic;
      pwm10 : out std_logic;
      pwm11 : out std_logic;
      pwm12: out std_logic
);
end dual1;
architecture Behavioral of dual1 is
signal a : integer range 0 to 3600:=0;
signal d : integer range 0 to 3600:=2400;
signal g : integer range 0 to 3600:=1200;
signal sine1 : integer range -2047 to 2047:=0;
signal sine4 : integer range -2047 to 2047:=0;
```

```
signal sine7 : integer range -2047 to 2047:=0;
signal sv1 : integer range -2047 to 2047:=0;
signal sv4 : integer range -2047 to 2047:=0;
signal sv7 : integer range -2047 to 2047:=0;
signal s1 : integer range -2047 to 2047:=0;
signal s2 : integer range -2047 to 2047:=0;
signal s3 : integer range -2047 to 2047:=0;
signal max1 : integer :=0;
signal min1 : integer :=0;
signal max2 : integer :=0;
signal min2 : integer :=0;
signal max3 : integer :=0;
signal min3 : integer :=0;
signal tring1 : integer :=0;
signal tring2 : integer :=0;
signal btrig : integer :=0;
signal btrig1 : integer :=0;
signal btrig2 : integer :=0;
signal btrig3 : integer :=0;
signal btrig4 : integer :=0;
signal btrig5 : integer :=0;
signal btrig6 : integer :=0;
signal btrig7 : integer :=0;
signal btrig8 : integer :=0;
signal btrig9 : integer :=0;
signal z :integer :=0;
signal y :integer :=0;
signal x :integer :=0;
```

```
signal w :integer :=0;
signal v :integer :=0;
signal clk_out : std_logic:='0';
signal a1 : std_logic:='0';
signal a2 : std_logic:='0';
signal a3 : std_logic:='0';
signal a4 : std_logic:='0';
signal a5 : std_logic:='0';
signal a6 : std_logic:='0';
signal a7 : std_logic:='0';
signal a8 : std_logic:='0';
signal a9 : std_logic:='0';
signal a10 : std_logic:='0';
signal a11 : std_logic:='0';
signal a12 : std_logic:='0';
signal a13 : std_logic:='0';
signal a14 : std_logic:='0';
signal a15 : std_logic:='0';
signal count : integer range 0 to 5555 :=0;
signal clk_out1 : std_logic:='0';
signal count1 : integer range 0 to 5555 :=0;
signal j : integer range 0 to 180:=0;
signal k : integer range 0 to 180:=90;
type memory_type1 is array (0 to 180) of integer range -2047 to 2047;
type memory_type is array (0 to 3600) of integer range -2047 to 2047;
 signal sine : memory type :=
( same as previous program);
          begin
```

```
process (clk)
begin
if (rising_edge(clk)) then
if (count= 555/4)then
clk_out <= not (clk_out);
count <= 0;
else
count <= count+1;
end if;
if (count1= 555/16)then
clk_out1 <= not (clk_out1);
count1 <= 0;
else
count1 <= count1+1;
end if;
end if;
end process;
process(clk)
begin
if(rising_edge(clk_out)) then
sine1 <= sine(a);
sine4 <= sine(d);
sine7 <= sine(g);
a <= a+ 1;
d <= d+ 1;
g <= g+ 1;
if(a = 3599) then
a <= 0;
end if;
if(d = 3599) then
d <= 0;
end if;
```

```
if(g = 3599) then
g <= 0;
end if;
end if;
end process;
process(clk)
begin
if(rising_edge(clk_out)) then
if(sine1 > sine4 and sine1 > sine7) then
  max1 <= sine1;
    if (sine4 > sine7)then
       min1 <= sine7;
      else
      min1 <= sine4;
 end if;
    elsif(sine4 > sine1 and sine4 > sine7) then
       max1<= sine4;
        if (sine1 > sine7)then
        min1 <= sine7;
        else
        min1 <= sine1;
    end if;
    elsif(sine7 > sine1 and sine7 >sine4) then
        max1 <= sine7;
        if (sine1 > sine4)then
        min1 <= sine4;
        else
        min1 <= sine1;
    end if;
end if;
sv1 <= sine1+(-(max1+min1)/2);
sv4 <= sine4+(-(max1+min1)/2);
```

```
sv7 <= sine7+(-(max1+min1)/2);
end if;
end process;
process(clk)
begin
if(rising_edge(clk_out)) then
s1 <= -sv1;
s2 <= -sv4;
s3 <= -sv7;
end if;
end process;
process(clk)
begin
if(rising_edge(clk_out1)) then
z <= z+1;
y <= y+1;
x <= x+1;
w <= w+1;
v <= v+1;
tring1 <= trig1(j);
tring2 <= -trig1(k);
j <= j + 1;
k <= k + 1;
if(j = 179) then
j <= 0;
end if;
if(k = 179) then
k <= 0;
end if;
if (z <= 45) then
btrig <= z*28;
elsif ((z > 45) and (z<=90)) then
```

```
btrig <= (90-z)*28;
elsif ((z > 90) and (z<=135)) then
btrig <= -(z-90)*28;
elsif ((z > 135) and (z<=180)) then
btrig <= -(180-z)*28;
elsif (z>=180) then
z<=0;
end if;
--sixty degree triangle---
if (y <= 45) then
btrig1 <= y*66;
elsif ((y > 45) and (y<=90)) then
btrig1 <= (90-y)*66;
elsif ((y > 90) and (y<=135)) then
btrig1 <= -(y-90)*66;
elsif ((y > 135) and (y<=180)) then
btrig1 <= -(180-y)*66;
elsif (y>=180) then
y<=0;
end if;
--120 degree triangle--
if (x <= 45) then
btrig2 <= x*40;
elsif ((x > 45) and (x<=90)) then
btrig2 <= (90-x)*40;
elsif ((x > 90) and (x<=135)) then
btrig2 <= -(x-90)*40;
elsif ((x > 135) and (x<=180)) then
btrig2 <= -(180-x)*40;
elsif (x>=180) then
x<=0;
end if;
```

```
if (w <= 51) then
btrig9 <= w*10;
elsif ((w < 51) and (w<=-51)) then
btrig9 <= (-51+w)*10;
elsif (w>=-51) then
w<=51;
end if;
btrig4 <= (btrig9 + 357);
btrig5 <= (btrig9 + 714);
btrig7 <= -(btrig9 + 351);
btrig8 <= -(btrig9 + 714);
if (x <= 90) then
btrig6 <= (45-x)*22;
elsif ((x > 90) and (x<=(180))) then
btrig6 <= -(135-x)*22;
elsif (x>180) then
x<= 0;
end if;
btrig3 <= -btrig6;
end if;
end process;
process(clk)
begin
  if(rising_edge(clk_out)) then
  if (sv1 > btrig) then
  pwm1 <= '1';
  else
  pwm1 <='0';
  end if;
    if (sv4 > btrig) then
  pwm2 <= '1';
  else
```

```
pwm2 <='0';
end if;
  if (sv7 > btrig) then
pwm3 <= '1';
else
pwm3 <='0';
end if;
  if (s1 > btrig1) then
 pwm5 <= '1';
 else
 pwm5 <= '0';
 end if;
 if (s2 > btrig1) then
 pwm6 <= '1';
 else
 pwm6 <= '0';
 end if;
 if (s3 > btrig1) then
 pwm7 <= '1';
 else
 pwm7 <= '0';
 end if;
        pwm4 <='0';
        pwm8 <='0';
        pwm9 <='0';
        pwm10 <='0';
        pwm11 <='0';
        pwm12 <='0';
      end if;
 end process;
end Behavioral;
```

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Journals:

1. Madhukar Rao A and K. Sivakumar, "A Fault-Tolerant Single-Phase Five-Level Inverter for Grid-Independent PV Systems," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7569-7577, Dec. 2015.

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1. Madhukar Rao A and K. Sivakumar, "DC Offset Minimization of Three phase Multilevel Inverter Configuration for Photovoltaic Applications under Fault and Partial Shading Conditions", IET power electronics. (**Accept with major revision**)
2. Madhukar Rao A, Parth sarathi and K. Sivakumar, "An Optimal Source distribution Strategy for Multilevel Inverters: Photovoltaic Application", IET power electronics.

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1. A. Madhukar Rao, B. S. Umesh and K. Sivakumar, "A fault tolerant dual inverter configuration for islanded mode photovoltaic generation system," in *Proc. IEEE IFEEC,* pp. 816-821, 2013 Tainan, Taiwan.
2. A. Madhukar Rao and K. Sivakumar, "Five level single phase inverter scheme with fault tolerance for islanded photovoltaic applications," in *Proc. IEEE ICITEE* pp. 194-199, 2015 Chiang Mai, Thailand.
3. A Madhukar Rao , Manoranjan Sahoo and K Sivakumar, "A Three phase Five-Level Inverter with Fault Tolerant and Energy Balancing Capability for Photovoltaic Applications" in *proc.* PEDES, Kerala, Dec.14-17, 2016.

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1. Madhukar Rao A, Manoranjan Sahoo, B Prathap, K Sivakumar, "Multilevel Inverter Configuration for Multistring Photovoltaic Applications with Improved Reliability".