Multi-Subband Ensemble Monte Carlo simulations of scaled GAA MOSFETs

L. Donetti*, C. Sampedro, F.G. Ruiz, A. Godoy, F. Gamiz

Departamento de Electrónica and CITIC, Universidad de Granada, 18071 Granada, Spain.

Abstract

We developed a Multi-Subband Ensemble Monte Carlo simulator for non-planar devices, taking into account two-dimensional quantum confinement. It couples self-consistently the solution of the 3D Poisson equation, the 2D Schrödinger equation, and the 1D Boltzmann transport equation with the Ensemble Monte Carlo method. This simulator was employed to study MOS devices based on ultra-scaled Gate-All-Around Si nanowires with diameters in the range from 4 nm to 8 nm with gate length from 8 nm to 14 nm. We studied the output and transfer characteristics, interpreting the behavior in the sub-threshold region and in the ON state in terms of the spatial charge distribution and the mobility computed with the same simulator. We analyzed the results, highlighting the contribution of different valleys and subbands and the effect of the gate bias on the energy and velocity profiles. Finally the scaling behavior was studied, showing that only the devices with $D = 4$ nm maintain a good control of the short channel effects down tho the gate length of 8 nm.

Keywords: Gate-all-around MOSFET, nanowire, Monte Carlo simulation, multi-subband, short-channel effects.

1. Introduction

Non-planar MOS transistors with multiple gates represent the most promising solution to the ultimate scaling of CMOS technology [1] because of their superior immunity to short channel effects. Indeed, they are not only a possible future option under scrutiny, but they have already entered mass production [2, 3]. When the size of a device reaches the nanometric scale, quantum effects play an important role; quantum confinement is relevant for reduced lateral size (*i. e.* in the direction perpendicular to transport) and even more so in non-planar structures where confinement is two-dimensional. An approximately correct electron distribution taking into account quantum confinement can be obtained with corrections to the classical potential, employing algorithms which, however, need proper calibration for each considered structure and crystal orientation (see for example [4, 5]). As a consequence, to properly take into account quantum confinement effects in the cross section of the device it is necessary to solve the Schrödinger Equation (SE). The Multi-Subband Ensemble Monte Carlo (MS-EMC) approach employs the semi-classical Monte Carlo (MC) method to solve the Boltzmann transport equation, coupled with the solution of the SE in the perpendicular direction. The MC method, compared to common transport framework such as Drift-Diffusion, takes directly into account non-equilibrium carrier transport. On the other hand, compared to full quantum approaches, MC allows a simpler implementation of scattering mechanisms and a relatively reduced computational effort.

In this work, we describe an MS-EMC simulator for 3D devices developed by our group, and show the possibilities it offers by studying the scaling properties of ultimate Gate-All-Around (GAA) MOS transistors with ultra-thin Si nanowires. Section 2 is devoted to the description of the simulator, while in the following one (Section 3) we define devices under study and report the obtained results and insights into the device behavior. Finally, conclusions are drawn in Section 4

2. Simulator description

To model a non-planar device, such as GAA MOSFETs, we employ a simulator based on the MS-EMC approach. This method has been widely and successfully employed for the simulation of planar semiconductor devices [6, 7, 8, 9], and only recently it has been applied to 3D devices [10, 11]. The simulator is based on the space-mode approach [12], where the SE is solved in several cross sections perpendicular to the transport direction z, for each considered conduction band valley. In this way, the eigen-energies, $E_{\nu,i}(z)$, and the wave functions, $\xi_{\nu,i}(x, y, z)$, are obtained for different values of z along the device, where ν and i are the valley and subband indices, respectively. After that, the energy levels are corrected for the effects of non-parabolic band structure as described in [13] while wave functions are left uncorrected.

Carrier transport is simulated through the MC method: once electrons are assigned to a subband (specified by its valley ν and index i), its motion is restricted to one dimension in the z direction and the driving force is computed employing the derivative of subband energy levels, that is $F = -\partial E_{\nu,i}(z)/\partial z$. Then, as usual in the MC scheme, the subband population, $n_{\nu,i}(z)$ is computed by counting the simulation particles in subband ν, i at different cross sections. By multiplying the population by the corresponding distribution function $|\xi_{\nu,i}(x, y, z)|^2$, the total

*Corresponding author
Email address: donetti@ugr.es (L. Donetti)

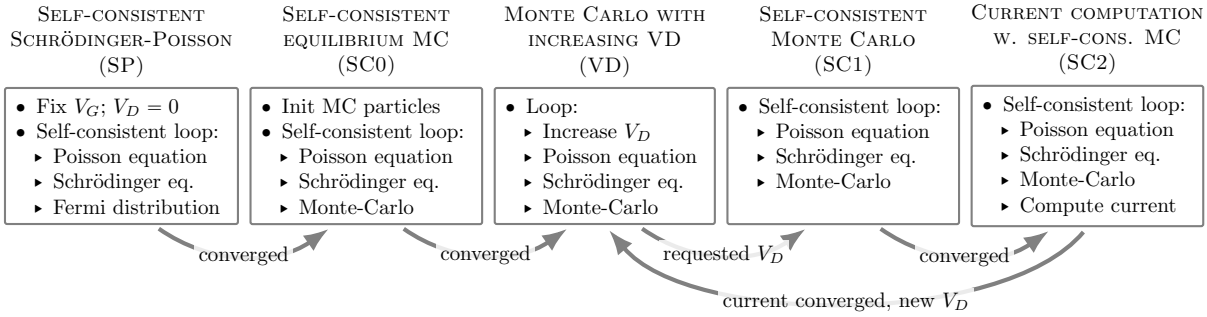

Figure 1: Simulation scheme for a given value of V_G.

electron density is obtained. The resulting charge density is employed in the 3D Poisson Equation (PE), which is solved in a loop with the SE and the MC simulation in order to achieve a self-consistent solution. To improve the stability and the convergence properties of the self-consistent loop, the non-linear PE is employed [14].

For the simulation, the device structure is described employing a 3D finite element mesh with tetrahedral elements. Because of the need to discretize the SE in different cross sections, this 3D mesh is constructed by extruding a 2D triangular mesh. The finite element mesh allows a good representation of complex geometries (e.g. round nanowires, rounded corners, leaning sidewalls in FinFETs) and a natural formulation of the equations (PE, SE) near material boundaries. The MC simulation includes carrier scattering by acoustic and optical phonons [15], taking into account Pauli exclusion principle [16]. To improve the MC statistics, especially in the sub-threshold regime, we employ a variance reduction technique based on non-uniform super-particle weight [17]. Here the weight is computed according to the total energy of the particle injected into the device through the contacts, as in the following equation:

$$w(E) = w_0\left(1 + \exp\left(q\frac{E - E_F}{2k_BT}\right)\right)^{-1} \tag{1}$$

where E_F is the Fermi energy (known at source and drain contacts where electrons are injected), k_B is the Boltzmann constant, T is absolute temperature, and w_0 a normalization constant, chosen and updated during the simulation in order to obtain a given number of (super-)particles. Notice that the expression of Equation (1) is similar to the Fermi-Dirac distribution function with an added factor $1/2$ in the exponent and a normalization factor.

The general simulation strategy for a given value of the gate bias V_G is shown in the diagram of Figure 1. The algorithm starts with $V_D = 0\,\mathrm{V}$ and a self-consistent solution of SE and PE in equilibrium (without transport) is found, employing a predictor-corrector method [18]. This allows the initialization of the MC simulator employing the electron density given by the equilibrium Fermi-Dirac distribution for each subband. Then a loop with the MC simulation and the solution of PE and SE is started. In a first phase (SC0), the drain bias V_D is kept equal to 0 V while a self-consistent solution is obtained. Then, a second phase is started (VD), in which the boundary conditions at the drain are changed increasing the voltage by a small ΔV_D step in each iteration of the loop, until the desired value of V_D is reached. After that, the boundary conditions are kept fixed and the MC-PE-SE loop (SC1) is repeated until the variation of the potential between one iteration and the following becomes lower than the prescribed tolerance, that, is when a self-consistent solution is obtained. Once this is achieved, the simulator starts computing the current (SC2) and an estimation of the corresponding statistical error, until the latter is below a specified threshold or a maximum number of iterations is reached. Then, the procedure is repeated from the VD stage with the following target value of the drain voltage.

Alternatively, it is possible to compute the low-field mobility, μ_n, by a similar procedure. Only the channel of the device is considered and small values of a uniform electric field are applied in the longitudinal direction. As in the full device simulation, an equilibrium self-consistent state with $V_D = 0\,\mathrm{V}$ is first obtained. Then, different small values of the drift electric field, F, are applied by shifting the subband energy levels, while an infinite channel length is emulated by employing periodic boundary condition. Finally, mobility is extracted by fitting the obtained values of the velocity, v_n with the linear relation $v_n = \mu_n F$.

To improve the performance of the simulator, a high level of parallelism is employed. In the MC code, the independent super-particle flights are simulated in a parallel fashion through the use of `OpenMP`; particular care is needed for synchronization to inject and remove particles at contacts and to gather particle statistics. On the other hand, specialized and optimized sparse matrix parallel routines are employed for the solution of the PE and the SE.

3. Results

We simulate GAA field-effect transistors based on cylindrical Si nanowires with channel along the ⟨100⟩ direction, with diameter D ranging from 4 nm to 8 nm. The coordinate reference system is chosen so that the x and y axes are in the cross section plane and the z axis is in the transport direction. The gate oxide (SiO_2) thickness is $T_{ox} = 1\,\mathrm{nm}$. The channel is considered undoped ($N_A = 1 \times 10^{13}\,\mathrm{cm}^{-3}$) and a midgap metal is assumed for the gate (with work function 4.56 eV).

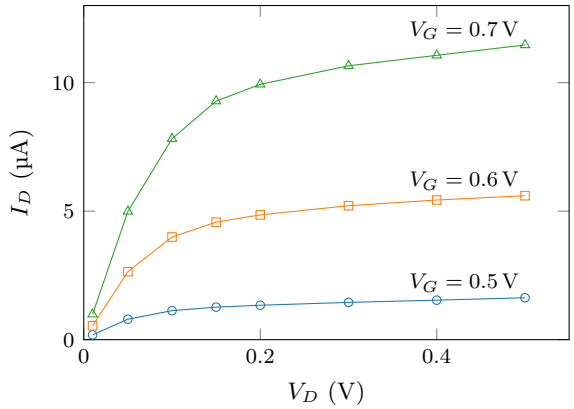

Figure 2: I_D-V_D curves for the device with $D = 8\,\mathrm{nm}$ and $L_G = 14\,\mathrm{nm}$.

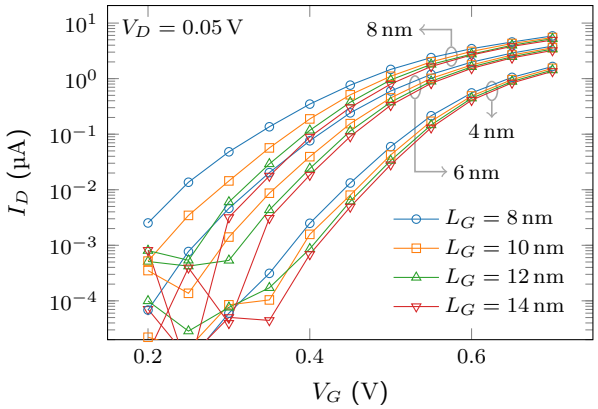

Figure 3: I_D-V_G curves for all simulated devices.

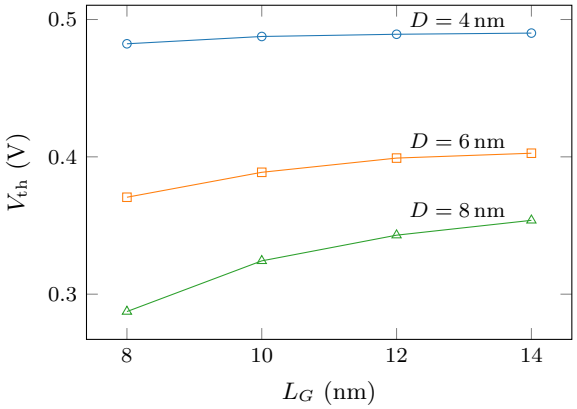

Figure 4: Threshold voltage V_{th} (computed at $V_D = 50\,\mathrm{mV}$) as a function of gate length L_G, for different values of nanowire diameter D.

The source and drain doping density is $N_{SD} = 1 \times 10^{20}\,\mathrm{cm}^{-3}$, with an underlap of $L_{sp} = 2\,\mathrm{nm}$ and Gaussian distribution with $\sigma = 0.8\,\mathrm{nm}$. The simulated devices have gate length L_G ranging from 14 nm down to 8 nm, while the total length of the source and drain regions, including extensions, is $L_{SD} = 14\,\mathrm{nm}$ each. As stated in Section 2, we employ a 3D mesh obtained by extrusion of a 2D mesh, as the latter is used to discretize the SE in the cross sections. This 2D mesh makes use of a variable number of triangles depending on the nanowire diameter: the minimum is ~ 1500 for $D = 4\,\mathrm{nm}$ and the maximum is ~ 3500 for $D = 8\,\mathrm{nm}$. The mesh spacing in the transport direction is finer in the channel region ($\Delta z_{\mathrm{min}} = 0.5\,\mathrm{nm}$) and gradually grows in the source and drain regions (up to $\Delta z_{\mathrm{max}} = 2\,\mathrm{nm}$). The number of nodes and tetrahedra in the full 3D mesh is approximately 32 500 and 182 500, respectively, for the smallest considered device; 98 000 and 560 000 for the largest one. All simulations have been performed at $T = 300\,\mathrm{K}$.

Figure 2 shows the simulated output characteristics of the largest device, with diameter $D = 8\,\mathrm{nm}$, and gate length $L_G = 14\,\mathrm{nm}$. Figure 3 shows the simulated transfer characteristics for all the considered devices: as expected the current is larger for nanowires with wider cross section and for shorter gate length. The statistical noise inherent to the MC method is greatly suppressed, thanks to the variance-reduction technique employed in the simulator: current fluctuations can be observed only for I_D values smaller than 1 nA. In any case the residual statistical noise in the I_D-V_G curve gives rise to larger fluctuations in the second derivative of I_D with respect to V_G: therefore we cannot locate the threshold voltage V_{th} with the maximum of $\partial^2 I_D / \partial V_G^2$. Therefore, we extract V_{th} by employing a fixed value of I_D. To take into account the difference in the gate length of the considered devices, we employ $I_{D,\mathrm{th}}(L_G = 14\,\mathrm{nm}) = 0.08\,\mu\mathrm{A}$ for the longest device and scale it inversely with L_G; that is $I_{D,\mathrm{th}}(L_G) = 0.08\,\mu\mathrm{A} \times (14\,\mathrm{nm}/L_G)$. The results are shown in Figure 4. The obtained values of V_{th} are larger for $D = 4\,\mathrm{nm}$ for all cannel lengths, due to quantum confinement. Moreover, a strong V_{th} roll-off is observed for the wider nanowires with $D = 6\,\mathrm{nm}$ or $D = 8\,\mathrm{nm}$, while only a small drift of V_{th} is present in the case of $D = 4\,\mathrm{nm}$.

If we restrict our analysys to the longest devices (i.e. with $L_G = 14\,\mathrm{nm}$) and plot the drain current vs. the gate voltage overdrive, $V_G - V_{\mathrm{th}}$, the curves corresponding to devices with different diameters collapse (see Figure 5) except for very large applied biases. This means that the behavior of I_D below the threshold voltage and slightly above it is independent of the diameter. To investigate this fact, we plot in Figure 6 the linear electron density n_{inv}, that is the charge density integrated in a cross section near the middle of the channel, versus the gate voltage overdrive. Only very small differences can be observed for values of $V_G - V_{\mathrm{th}}$ larger than approximately 0.2 V, indicating that linear density does not depend on the nanowire diameter D. This, in turn, means that the average spatial charge density must be inversely proportional to the cross-section area, for the same gate overdrive. Such behavior can be explained by considering the spatial charge distribution, n, along a cross section in the middle of the gated region as it is shown in Figure 7. In narrow nanowires, such as those considered in this paper, the charge concentration is almost always peaked around the center of the nanowire, as shown in Figure 7 (a), (b), and (c): for $V_G = V_{\mathrm{th}} + 0.2\,\mathrm{V}$ the shape of the electron distribution is very similar, with increasing width and decreasing peak concentration as the diameter grows from 4 nm to 8 nm. Only for the widest device ($D = 8\,\mathrm{nm}$) and larger gate bias ($V_G = V_{\mathrm{th}} + 0.3\,\mathrm{V}$) the maximum value of n is located at a position different from

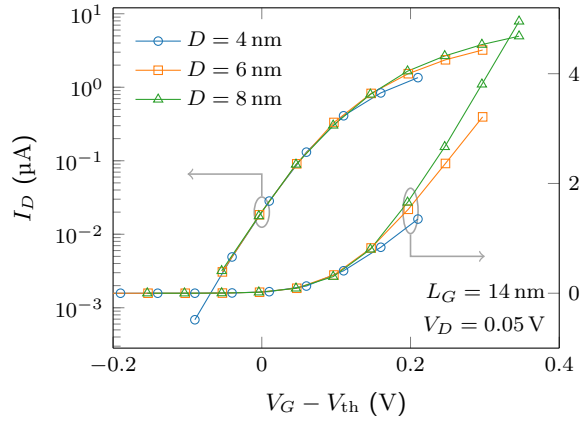

Figure 5: Drain current I_D as a function of gate overdrive $V_G - V_{\text{th}}$ for devices with $L_G = 14$ nm.

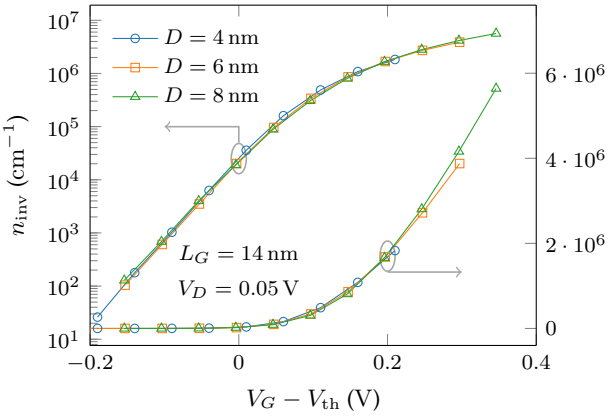

Figure 6: Linear electron density n_{inv} in the middle of the channel as a function of gate overdrive.

the geometrical center of the nanowire. In particular, due to the anisotropy of the Si conduction band valleys, four maxima appear along the x and y axes.

If we compare Figures 5 and 6, however, we can notice that the differences among the I_D curves for a gate overdrive larger than 0.1 V are larger than the differences in the n_{inv} curves. Therefore, the differences in the drain current cannot be attributed exclusively to the inversion charge and must stem from other causes. To shed light on this issue we also computed the mobility, μ_n, shown in Figure 8. Here, we can observe that μ_n is severely degraded for decreasing D, which justify the residual differences in the I_D curves.

The simulator also allows for measuring and comparing internal quantities such as, for example, those related to the subband profiles and populations. In a ⟨100⟩ nanowire with circular cross section, the six equivalent Δ valleys of Si conduction band split into nonequivalent sets. With our choice of coordinates, the doubly degenerate Δ_x and Δ_y valleys, present their longitudinal direction in the cross-section plane. For both valleys, the confinement masses are $m_l = 0.926\, m_0$ in one direction and $m_t = 0.19\, m_0$ in the perpendicular one (where m_0 is the free electron mass): due to the symmetry of the circular shape,

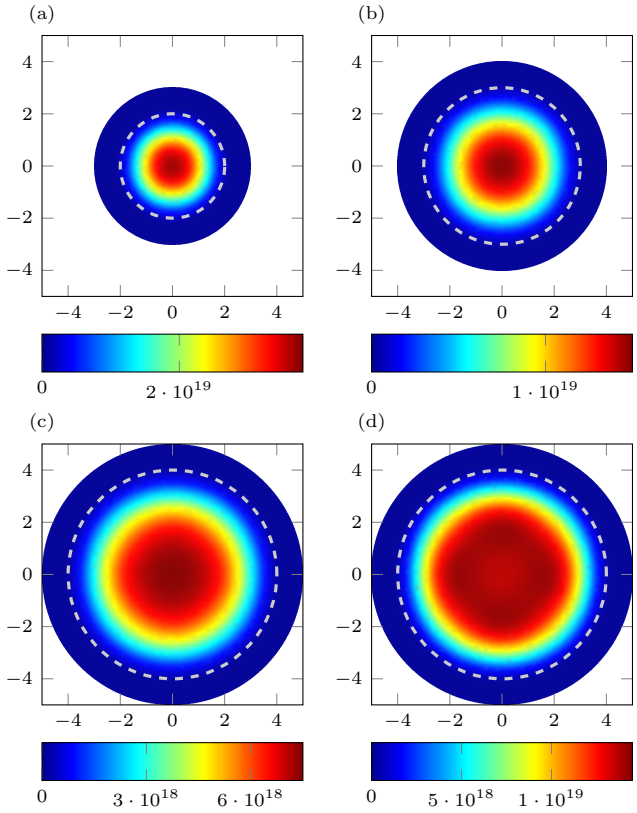

Figure 7: Electron density in the middle of the channel for $V_G = V_{\text{th}} + 0.2$ V and $D = 4$ nm (a), $D = 6$ nm (b), $D = 8$ nm (c); $V_G = V_{\text{th}} + 0.3$ V and $D = 8$ nm (d). The dashed line indicates the Si/SiO_2 interface. Units of dimensions in the cross sections are nm while the units of electron density are cm^{-3}.

the corresponding energy levels are equal, with wave functions with different symmetry axes. On the other hand, the Δ_z valleys with their longitudinal effective mass along the transport direction give rise to subbands with higher energy: in this case the confinement effective mass is isotropic in the cross-section plane and equal to m_t. Figure 9 shows the energy profiles of the two lowest subbands of each valley for the largest device, with $D = 8$ nm and $L_G = 14$ nm. Notice that, as explained before, the lowest energy subband corresponds to the Δ_x and Δ_y valleys. However, the confining potential is different inside the channel and in the source and drain regions, so that the subband with second lower energy belongs to different valleys according to the position z. Moreover, since in the Δ_z valleys the transport mass is larger than in the Δ_x and Δ_y valleys (m_l vs. m_t), the population of the corresponding subbands can be larger even if the energy levels are higher, as shown in Figure 10. Here we can see that the population of the first subbands of Δ_x, Δ_y and Δ_z are approximately equal in the gated region.

We now turn to the analysis of the profiles as a function of the gate voltage V_G, in the same device ($D = 8$ nm, $L_G = 14$ nm). Figure 11 shows the fundamental subband energy, $E_{x,1}$ (or, equivalently, $E_{y,1}$), the total linear electron density, n_{inv}, and the average electron velocity in the transport direction, $\langle v_z \rangle$, as a function of the position z along the channel, for $V_D = 0.05$ V and different values of V_G. In the subband profile (Fig-

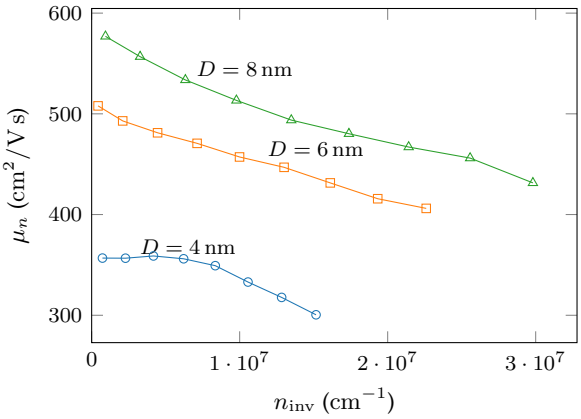

Figure 8: Phonon limited electron mobility for Si GAA nanowires as a function of inversion charge n_{inv} for different values of nanowire diameter D.

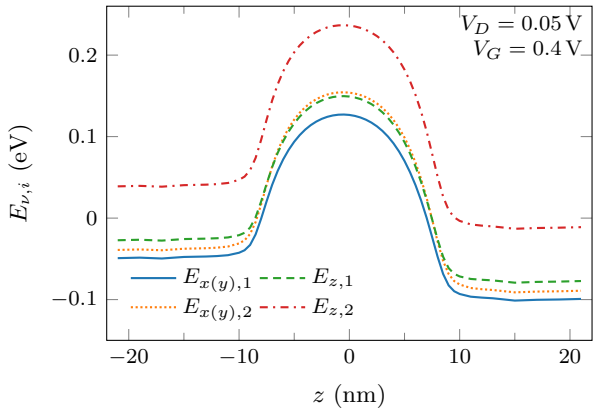

Figure 9: Energy profile of the first two subbands of each valley for the device with $D = 8$ nm and $L_G = 14$ nm. Subbands of Δ_x and Δ_y valleys have the same energy due to the symmetry of the cross-section.

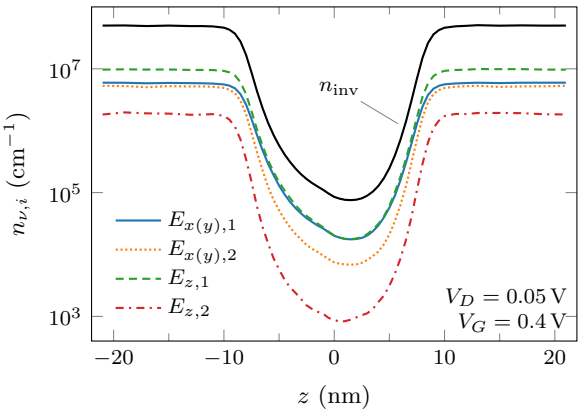

Figure 10: Population of the first two subbands of each valley for the device with $D = 8$ nm and $L_G = 14$ nm. Subbands of Δ_x and Δ_y valleys have the same population due to the symmetry of the cross-section. The black solid curve indicates the total electron density.

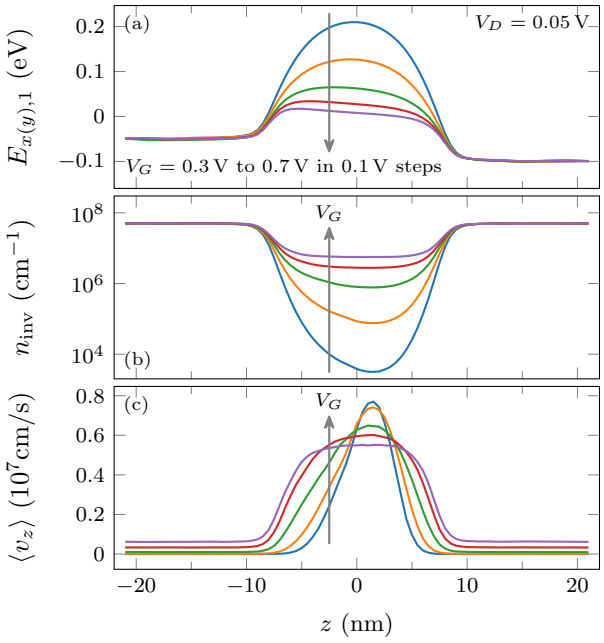

Figure 11: Fundamental subband profile (a), electron density (b), and average electron velocity in the transport direction (c) as a function of position along the device, for $V_D = 0.05$ V and different values of V_G. All curves correspond to the device with $D = 8$ nm, $L_G = 14$ nm.

ure 11(a)), we can see that the maximum energy (that is the peak of the source-to-drain barrier) is located in the center of the device in the sub-threshold regime (for $V_G = 0.3$ V) and gradually moves towards the source end of the channel as V_G increases. This displacement is also associated with a change in the shape of the profile inside the channel: rounded for small V_G and almost straight for high V_G, sloped towards the drain. In the n_{inv} curve (Figure 11(b)), we can notice that, even in sub-threshold regime (when the electron density in the channel is four orders of magnitude smaller than in the source and drain), the profile is very smooth, and the statistical noise produced by the MC method is kept under control thanks to the aforementioned variance reduction technique. Next, the shape of the curves presents a trend similar to the one observed in the subband profile, in the sense that the shape gets more flat when the gate bias increases. However, there is a noticeable difference: the position of the minima in the sub-threshold regime does not correspond to the center of the channel but it is displaced towards the drain. The position of such minima corresponds to maxima of the velocity curves Figure 11(c), as the current is constant in the whole device in a stationary state. As expected, in the channel region the average velocity is higher than in the source/drain regions, because of the reduced electron density. In general, the average velocity increases for larger values of V_G, following the increase of the drain current. However, this trend is reversed in a small region inside the channel, around the position of the average velocity maximum: the peak velocity decreases for increasing V_G.

We can also check the correct implementation of the scattering mechanisms and of the Pauli exclusion principle as mentioned in section 2, by analyzing the carrier distribution as a

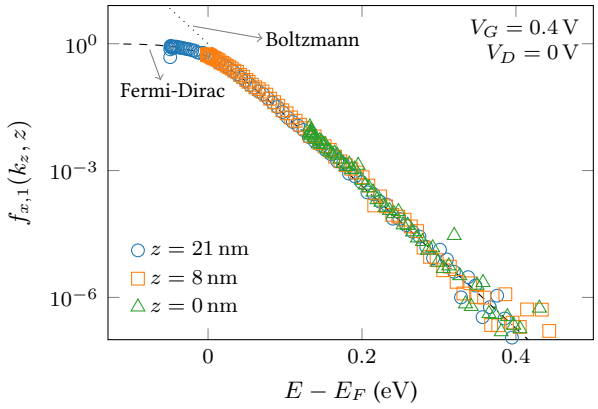

Figure 12: Occupation function for electrons in the lowest energy subband as a function of energy at different z positions, for the device with $D = 8\,\mathrm{nm}$ and $L_G = 14\,\mathrm{nm}$. Boltzmann and Fermi-Dirac distribution are also plotted for comparison.

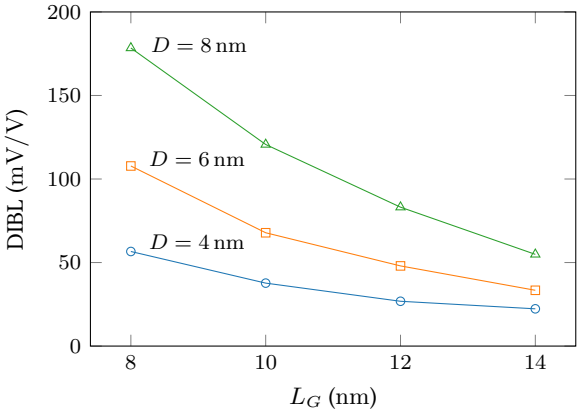

Figure 13: DIBL, computed employing $V_D = 0.05\,\mathrm{V}$ and $V_D = 0.5\,\mathrm{V}$, as a function of the gate length for different values of nanowire diameter.

function of energy. To be able to compare to an analytical expression we consider the equilibrium case, with $V_D = 0\,\mathrm{V}$. In this case, there exists a constant Fermi level, E_F, in the whole device, aligned with the Fermi level of source and drain, and the energy distribution of electrons must follow the Fermi-Dirac distribution. To implement the Pauli exclusion principle, the electron distribution function is computed by particle counting for every subband and every device cross-section, obtaining the function $f_{v,i}(k_z, z)$. Then, to perform a comparison with the Fermi-Dirac distribution we compute $f_{v,i}(E, z) = f_{v,i}(k_z(E), z) + f_{v,i}(-k_z(E), z)$, where $k_z(E)$ is the positive value of wave-vector k_z corresponding to the total energy E for subband v, i. In Figure 12, we show $f_{x,1}(E, z)$, the distribution function of the fundamental subband (the first subband of Δ_x valley) as a function of energy at three different positions: in the center of the channel ($z = 0\,\mathrm{nm}$), just outside the channel towards the drain region ($z = 8\,\mathrm{nm}$), and in the drain region near the contact ($z = 21\,\mathrm{nm}$). The result show that Fermi-Dirac distribution is correctly reproduced.

Finally, we turn to the analysis of the short channel effects (SCEs) in the simulated devices and their dependence on the

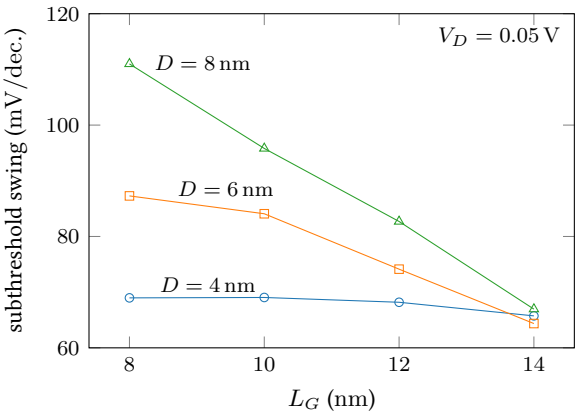

Figure 14: Sub-threshold swing as a function of gate length for different values of nanowire diameter.

gate length L_G. We can expect the narrower devices to possess better electrostatic control of the channel, especially for larger gate lengths. However, the MS-EMC simulator allows us to obtain quantitative results which properly take into account lateral quantum confinement. A first indication of the SCEs is given by the Drain Induced Barrier Lowering (DIBL), a measure of the variation of the threshold voltage shift caused by the drain bias: $\mathrm{DIBL} = \left|V_{\mathrm{th@VD2}} - V_{\mathrm{th@VD1}}\right|/(V_{D2} - V_{D1})$. In this case, the DIBL values shown in Figure 13 are computed employing the following drain voltage values: $V_{D1} = 0.05\,\mathrm{V}$ and $V_{D2} = 0.5\,\mathrm{V}$. In the figure, we can observe that for $D = 4\,\mathrm{nm}$ the DIBL hardly increases for decreasing L_G, with a largest value as small as $58\,\mathrm{mV/V}$ for the shortest device ($L_G = 8\,\mathrm{nm}$). For the nanowires with with $D = 6\,\mathrm{nm}$ and $D = 8\,\mathrm{nm}$, gate length scaling produces a larger increase of the DIBL, which exceeds $100\,\mathrm{mV/V}$ at $L_G = 8\,\mathrm{nm}$ and $L_G = 10\,\mathrm{nm}$, respectively.

Similar conclusions can be drawn by observing the sub-threshold swing (SS), represented in Figure 14. The longest devices, with $L_G = 14\,\mathrm{nm}$, show the same SS value for every D (within the numerical accuracy): $\mathrm{SS} \simeq 65\,\mathrm{mV/dec.}$, which is close to the ideal MOSFET limit at room temperature. However, the scaling behavior is quite different: while the narrowest device keeps SS values lower than $70\,\mathrm{mV/dec.}$ for all the considered gate lengths, the device with $D = 8\,\mathrm{nm}$ shows a linear increase reaching $\mathrm{SS} \simeq 110\,\mathrm{mV/dec.}$ at $L_G = 8\,\mathrm{nm}$.

4. Conclusion

This paper describes a numerical simulator that solves in a self-consistent way the 3D Poisson equation, the 2D Schrödinger equation, and the 1D Boltzmann transport equation through the Ensemble Monte Carlo method. This software can be used to study the static characteristics of ultra-scaled MOSFET devices, also in the sub-threshold region thanks to the implementation of a variance reduction technique based on variable superparticle weights. It also allows us to inspect the carrier distribution, taking into account quantum confinement effects, and to compare the phonon limited mobility and drain current including the short-channel and high-field effects, both computed

with the MC method.

We applied this simulator to narrow Si nanowire MOSFETs with reduced gate length. We correlated the differences in the curves above threshold with the different shape of the charge distribution in the cross section of the device and with the mobility degradation for small diameters. We analyzed the electron density and velocity distribution inside the channel of the device as a function of the applied gate bias. Finally we studied the short channel effects and we found that the narrowest cylindrical devices with $D = 4$ nm can keep a good electrostatic control down to $L_G = 8$ nm.

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