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# High Efficiency High Step-up Isolated DC-DC Converter for Photovoltaic Applications

Chang Wang<sup>1</sup>, Mingxiao Li<sup>1</sup>, Ziwei Ouyang<sup>1</sup>, Gang Wang<sup>2</sup>

<sup>1</sup> Department of Electrical Engineering, Technical University of Denmark, Kongens Lyngby, Denmark, [zo@elektro.dtu.dk](mailto:zo@elektro.dtu.dk)

<sup>2</sup> Institute of Electrics, Chinese Academy of Science, Beijing, China

**Abstract**—A high efficiency and high step-up isolated DC-DC converter with a new topology configuration for photovoltaic (PV) application is proposed in this paper. This converter consists of a Zero-Voltage-Switching (ZVS) and Zero-Current-Switching (ZCS) current-fed push-pull converter as a DC transformer dealing with most of power and an active clamp flyback (ACF) converter as a regulator with considerable high efficiency within a large conversion range. The two converters are constructed with the input-parallel-output-series (IPOS) structure. The input-parallel connection is able to share the large input current as well as reduce the current ripple, while the output-series connection is used to increase the output voltage gain. A 400 V / 400 W experimental prototype with an input voltage range of 24 V - 32 V is built. The maximum efficiency reaches at 95.1%. The experimental result validates the correctness of the analysis and proves the feasibility of the proposed topology for the photovoltaic applications.

**Keywords**—High step-up dc-dc converter, photovoltaic, ZVC/ZCS current-fed push-pull, active clamp flyback, input-parallel-output-series.

## I. INTRODUCTION

High level dc voltages are needed in many applications such as telecommunication equipment with travelling wave tube (TWT) which is used in communication satellite [1]. Since the power for satellite dragged from the PV panels plays an important role and the output voltage of a PV module is usually low and unregulated which is 24 V - 32 V in our case. A front-end dc-dc converter is needed to boost and regulate the PV voltage to dc interface voltage which is 400 V in our case [2]. The design consideration of high step-up converter according to the specification includes many aspects such like high efficiency, low electro-magnetic interference (EMI), reduction in mass, volume and cost, long lifetime and reliability, etc. Among which efficiency and EMI are priority.

Theoretically the conventional boost converter with extreme duty cycle can be employed due to its simple structure. However, it results in large current ripple, high switching and conduction loss, high voltage stress on semiconductors and EMI problems [3][4][5]. Many publications focus on high step-up voltage gain and high efficiency [3]. Multistage solutions increase the number of components which add to the increase in complexity and cost, also decrease the efficiency

by transferring the power through more stages [1]. Converters with coupled inductors are simple and more flexible solutions. But the leakage energy induces high voltage stress, large switching losses and severe EMI problems [6]. Switched-capacitor can achieve high voltage gain but many switches are needed which require many driving circuits [7]. The Quasi-Z source network was applied in [8] and [9], they provide a high voltage gain but with high voltage stress for semiconductors. Some interleaving structure was introduced in [2], [4], [5], but they added the difficulty in control circuit.

A one-stage isolated DC-DC converter with high voltage gain and high efficiency is proposed in this paper. The topology configuration is composed of two converters connected with input-parallel-output-series (IPOS) structure. One of which is a ZVC/ZCS current-fed push-pull realizing soft switching both in switch-on and switch-off moments, resulting in a maximum efficiency and lowest EMI. Due to the main switches are working in turns, the push-pull converter is able to deal with a higher power compared with other single switch converters. Also, the traditional symmetric structure and performing stages of push-pull converter gives a lower voltage stress on each semiconductor. Another part is an active clamp flyback (ACF) converter which is operated under discontinuous conduction mode (DCM). The ACF converter working as a buck-boost converter is able to regulate the output voltage. It can also realize ZVS and reach highest efficiency with maximum power distributed.

## II. PROPOSED TOPOLOGY AND SPECIFICATIONS

The proposed input-parallel-output-series (IPOS) structure topology is shown in Fig.1. The top part is a ZVC/ZCS current-fed push-pull converter. It works under a fixed switching frequency 500 kHz and fixed voltage transfer ratio 1:12. The push-pull converter deals with most power of the whole system. The bottom part is an active clamp flyback (ACF) converter. It works in both buck and boost modes according to the variation of the input voltage. The switches  $S_3$  and  $S_4$  work under the ZVS due to the DCM mode and the active clamp characteristics. The ACF dealing with a small portion of power is to regulate the output voltage, playing a role of the control circuit. The parameter design of the ACF converter aims to obtain the highest efficiency when it handles the largest power. The specifications are shown in TABLE I. The power distribution under the two extreme working conditions with different input voltages is shown in TABLE II. With the

variation of input voltage, the output voltage of push-pull converter varies in a large range due to the fixed high conversion ratio. The ACF converter varies its conversion ratio by changing the duty cycle to stabilize the output voltage.

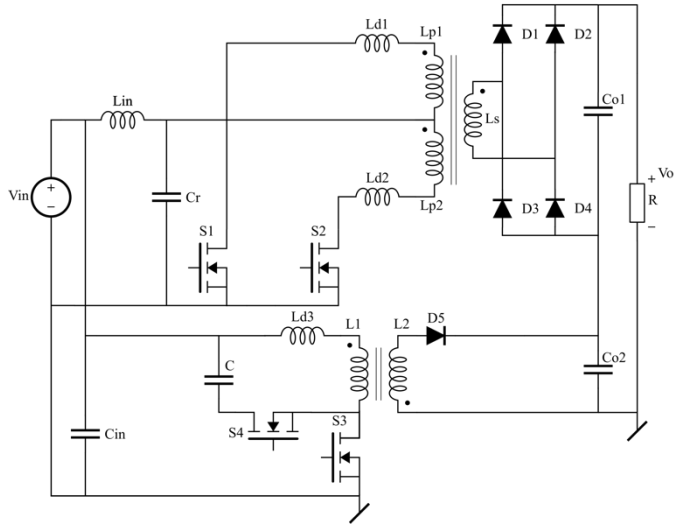


Fig.1. Input-parallel-output-series(IPOS) Topology

TABLE I. SPECIFICATIONS

Symbol	Quantity	Value
$V_{in}$	Input voltage	24 V ~ 32 V
$V_o$	Output voltage	400 V
$P$	Output power	100 W ~ 400 W
$D$	Duty cycle of main switches	0.4
$f_s$	Switching frequency	500 kHz

TABLE II. TWO EXTREME WORKING CONDITIONS

Symbol	Quantity	Min Value	Max Value
$V_{in}$	Input voltage	24 V	32 V
$P$	Output power	400 W	400 W
$G_{pp}$	Push-pull voltage gain	12	12
$V_{opp}$	Push-pull output voltage	288 V	384 V
$P_{pp}$	Push-pull output power	288 W	384 W
$G_f$	ACF voltage gain	4.67	0.5
$V_{of}$	ACF output voltage	112 V	16 V
$P_f$	ACF output power	112 W	16 W

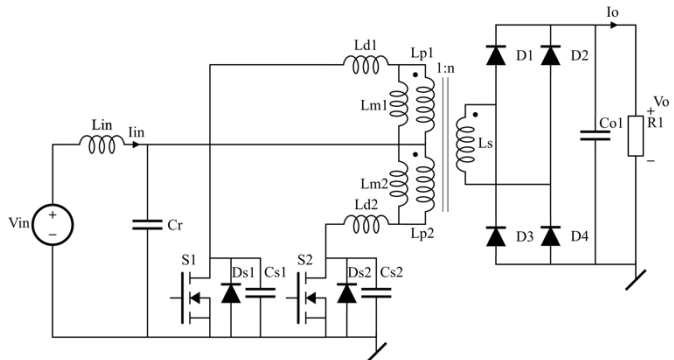


Fig.2. ZVS/ZCS Current-fed Push-pull

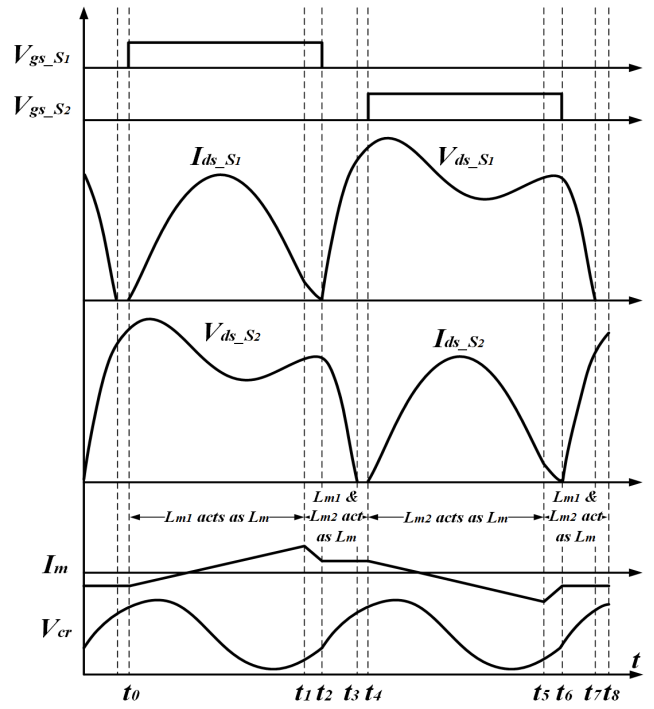


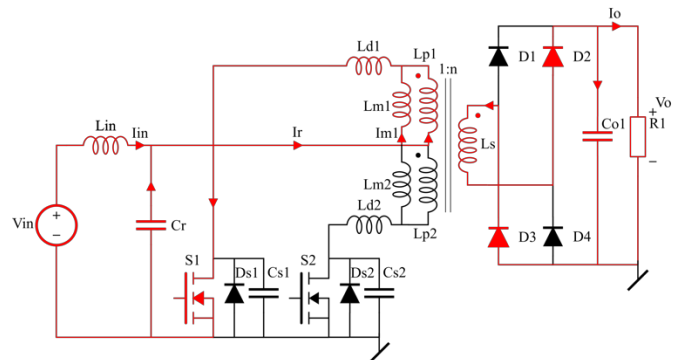
Fig.3. Main Theoretical Waveforms of 8 Stages

### III. ZVS/ZCS CURRENT-FED PUSH-PULL CONVERTER

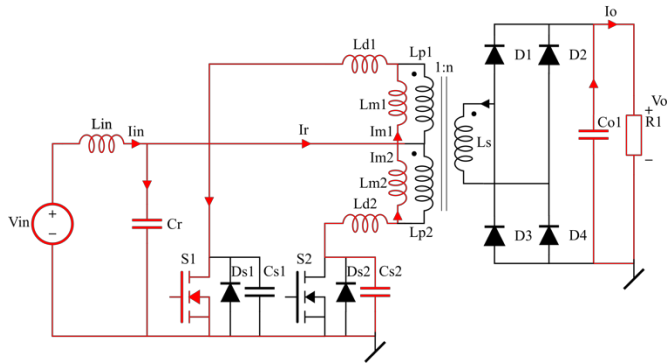
#### A. Proposed Circuit and Operation Principles

The ZVS/ZCS current-fed push-pull converter is shown in Fig.2. There are 8 operation stages during one period and the main theoretical waveforms are shown in Fig.3.

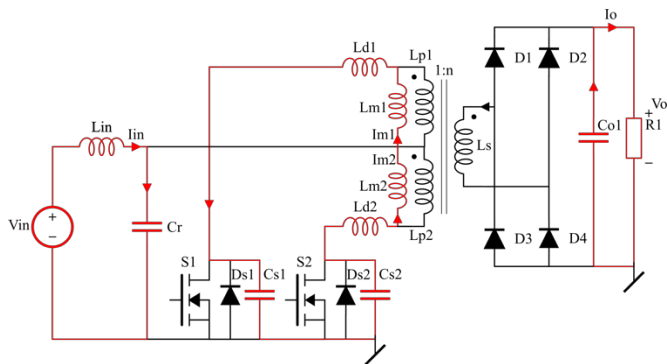
**Stage 1 [ $t_0-t_1$ ]:** When the switch  $S_1$  is turned on, the current flows through the primary winding  $L_{p1}$  to transfer the energy to the secondary part. The voltage on  $L_{p1}$  is clamped by the output voltage. And the resonance current  $I_r$  going through the switch's drain-source is resonated between the leakage inductance  $L_{d1}$  and the resonance capacitor  $C_r$ . The parasitic capacitance of the transformer joins the resonance but it's negligible due to the small value compared with  $C_r$ . The input inductor  $L_{in}$  also joins the resonance but it's negligible due to the large value compared with leakage inductance  $L_{d1}$ . The magnetizing inductance  $L_{m1}$  of transformer is charged and the magnetizing current  $I_{m1}$  is rising linearly. At the end of this stage ( $t_1$ ),  $I_r$  and  $I_{m1}$  intersect to a certain value  $I_{mmax}$ , where energy transferred from the primary winding to the secondary winding stops.



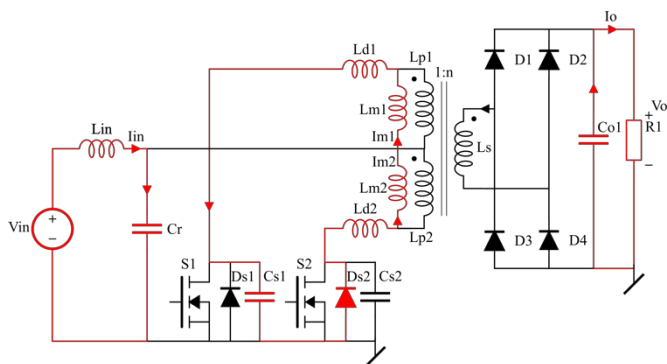
**Stage 2 [ $t_1-t_2$ ]:** At the moment of  $t_1$ , the magnetizing current  $I_{m1}$  begins to decrease at the meantime  $I_{m2}$  begins to increase. Due to the Kirchhoff's current law (KCL), the resonance current  $I_r$  equals to the difference between  $I_{m1}$  and  $I_{m2}$ . Due to the transformer flux balance relation, at the end of this stage ( $t_2$ ),  $I_{m1}$  and  $I_{m2}$  intersect to a medium value which is around half of  $I_{mmax}$ . The resonance current  $I_r$  decreases to the zero, the switch  $S_1$  is turned off under ZCS. The period of this stage is relatively short and can be regarded as a transient.



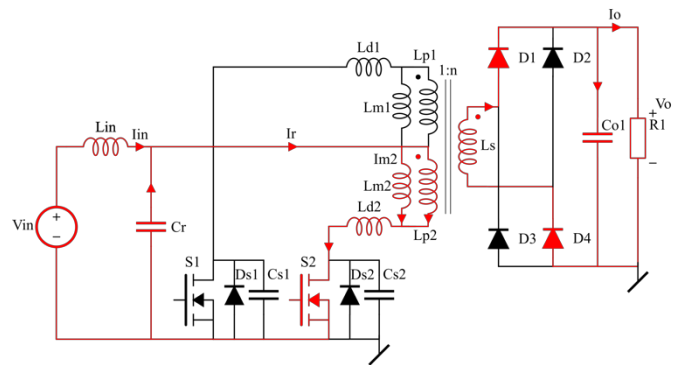
**Stage 3 [ $t_2-t_3$ ]:** After the resonance is finished, the magnetizing currents  $I_{m1}$  and  $I_{m2}$  remain to charge the parasitic capacitance of switch  $C_{s1}$  and discharge the  $C_{s2}$ . Thus, the voltage on the switch  $S_1$  is charged to around twice of the resonant capacitor voltage, the voltage on the switch  $S_2$  reduces to zero if the magnetizing inductance value  $L_m$  is selected appropriately.



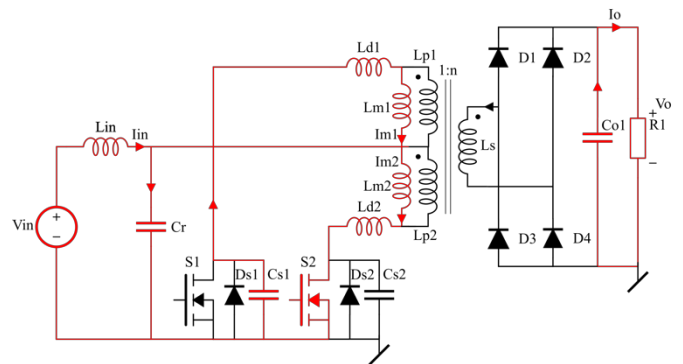
**Stage 4 [ $t_3-t_4$ ]:** After the parasitic capacitance  $C_{s2}$  of the switch  $S_2$  is fully discharged, the  $S_2$  is turned on immediately when the body diode of the  $S_2$  is forward biased. At the end of this stage,  $S_2$  is turned on under ZVS.



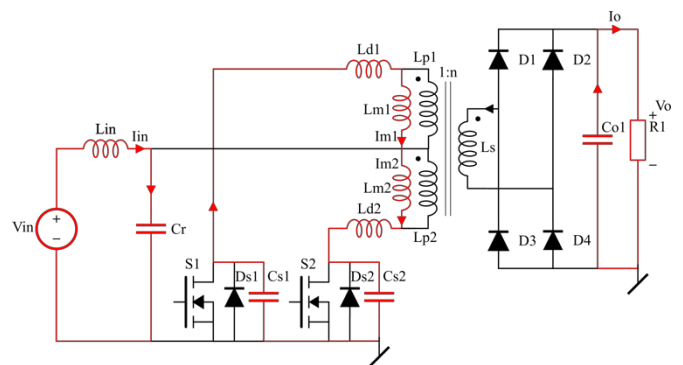
**Stage 5 [ $t_4-t_5$ ]:** Similar as Stage 1.



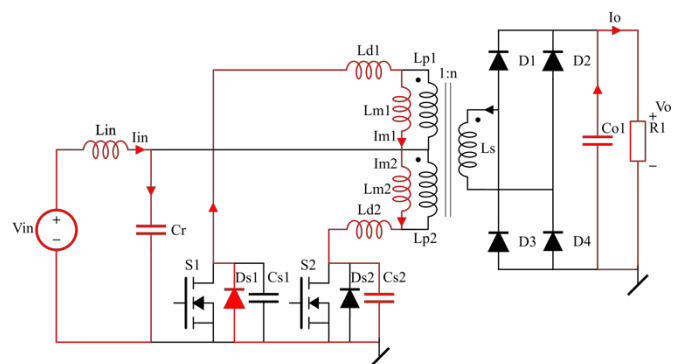
**Stage 6 [ $t_5-t_6$ ]:** Similar as Stage 2.



**Stage 7 [ $t_6-t_7$ ]:** Similar as Stage 3.



**Stage 8 [ $t_7-t_8$ ]:** Similar as Stage 4.



## B. Circuit Analysis

### a) ZCS Realization

The analyses of main switch drain-source current in stage 1 and stage 2 (stage 5 and stage 6) are needed to realize the ZCS for main switches. It can be written as two parts, one part is the resonance current  $I_r$  in sinusoidal waveform [10], the other one is the magnetizing current  $I_m$  in linear waveform. A point of the intersection is described by the value of  $I_{mmax}$ .

$$I_r = \left[ \sqrt{\frac{L_{in} \cdot (C_r + C_p)}{L_r \cdot (L_{in} + L_r)}} \cdot (V_{cr(t_0)} - V_n) - \frac{1}{L_{in} + L_r} \cdot \sqrt{\frac{L_{in} \cdot L_r \cdot (C_r + C_p)}{L_{in} + L_r}} \cdot (V_{in} - V_n) \right] \cdot \sin(\omega_r \cdot t) + \frac{V_{in} - V_n}{L_{in} + L_r} \cdot t + \frac{I_{in}(t_0) \cdot L_{in}}{L_{in} + L_r} \cdot (1 - \cos(\omega_r \cdot t)) \quad (1)$$

where the input inductor  $L_{in}$  should be designed to provide small input current ripple, here taking 10% ripple for design,

$$L_{in} = \frac{D \cdot V_{in}}{0.1 I_{inavg} \cdot f_s} \quad (2)$$

the resonance inductor  $L_r$  is leakage inductance of the transformer:  $L_r = L_{d1} = L_{d2}$ ; the equivalent parasitic capacitor  $C_p$  of windings:  $C_p \ll C_r$ ; the resonant capacitor voltage:  $V_{cr(t_0)} = V_{in}$ ; the input current:  $I_{in(t_0)} = I_{inavg}$ ; the clamping voltage on windings:  $V_n = V_o \cdot N_p / N_s$ ; the resonant frequency  $\omega_r$  is tuned by choosing the proper  $C_r$  to enable the switch off when the resonance current just reaches to the zero. Thus, it can minimize the current root mean square (RMS) value to enable a lower conduction loss and also reduce the circulating loss,

$$\omega_r = \sqrt{\frac{L_{in} + L_r}{L_{in} \cdot L_r \cdot (C_r + C_p)}} \quad (3)$$

Other parameters such as the input voltage  $V_{in}$ , output voltage  $V_o$ , the turns ratio  $n$ , the duty cycle  $D$ , the average input current  $I_{inavg}$ , and the switching frequency  $f_s$  are fixed and can be derived from the specification. During stage 1 and stage 5, the magnetizing current can be expressed as below,

$$I_m = I_m(t_0) + \frac{V_n}{L_m} \cdot t_1 \quad (4)$$

where  $L_m$  is magnetizing inductance and  $I_m(t_0) = -\frac{1}{2} I_{mmax}$ . Giving us the maximum value of magnetizing current  $I_{mmax}$  at the moment  $t_1$ ,

$$I_{mmax} = -\frac{1}{2} I_{mmax} + \frac{V_n}{L_m} \cdot t_1 \quad (5)$$

smaller  $L_m$  gives a higher value of  $I_{mmax}$ , thus leading longer time period of stage 2 and stage 6, which is not conducive to the realization of ZCS. Maximum value of magnetizing current  $I_{mmax}$  below 15% of peak value of resonance current  $I_r$  can be regarded as suitable choice. which gives us  $I_{mmax} \leq 4A$ . Therefore, one minimum limit of  $L_m$  can be described,

$$L_{mmin} = \frac{2}{3} \cdot \frac{V_n}{I_{mmax}} \cdot t_1 \quad (6)$$

### b) ZVS Realization

The analysis of charging and discharging of parasitic capacitance  $C_s$  of the switch during state 3 and state 7 are needed to realize the ZVS.

$$V_{ds1(t)} = \frac{1}{C_{s1}} \int_{t_2}^{t_3} \frac{1}{2} \cdot I_{m1} \cdot dt$$

$$V_{ds2(t)} = 2 \cdot V_{cr(t_1)} - \frac{1}{C_{s2}} \int_{t_2}^{t_3} \frac{1}{2} \cdot I_{m2} \cdot dt \quad (7)$$

where the resonance capacitor voltage:  $V_{cr(t_1)} = V_{in}$ . Due to a short time period of  $t_2-t_3$  or  $t_6-t_7$ , it is assumed that magnetizing current  $I_{m1}$  or  $I_{m2}$  keeps constant during this period. The energy stored in the magnetizing inductance  $L_{m1}$  or  $L_{m2}$  must be sufficient to cause a voltage swing across the switch equal to twice of the center tap voltage [11],

$$L_m \cdot \left(\frac{I_{mmax}}{2}\right)^2 = C_s \cdot (2V_{in})^2 \quad (8)$$

where:  $I_{mmax} = -\frac{1}{2} I_{mmax} + \frac{V_n}{L_m} \cdot t_1$ , larger  $L_m$  gives a smaller energy stored in the magnetizing inductance which is not conducive to the realization of ZVS. Therefore, one maximum value for  $L_m$  can be described,

$$L_{mmax} \cdot \left(\frac{1}{3} \cdot \frac{V_n}{L_{mmax}} \cdot t_1\right)^2 = 4C_s \cdot V_{in}^2 \quad (9)$$

The range of  $L_m$  can be described,

$$\frac{2V_n \cdot t_1}{3I_{mmax}} \leq L_m \leq \frac{t_1^2}{36C_s} \quad (10)$$

after the selection of components, the calculation can be done for the above range:  $4.3 \mu\text{H} \leq L_m \leq 14.8 \mu\text{H}$ . The  $L_m$  is chosen to be  $6 \mu\text{H}$  in this case.

### C. Magnetics Design

For turns ratio is 1:12, 1 turn is used for the primary winding, and 12 turns for the secondary windings to minimize the winding losses and parasitic capacitances [12]. The magnetic core material 3F36 is chosen for 500 kHz frequency. To produce sufficient  $L_m = 5 \mu\text{H}$  in one single turn, the core type E58\_11\_38 is chosen to provide  $5.4 \mu\text{H/turn}^2$ . The  $L_d$  value is aimed to be minimized in transformer design in order to provide considerable low value for the resonance circuit [13]. Thus, interleaving structure is adopted for this case [14], shown in Fig.4 (Here for simplicity only one part of the primary windings is considered due to the symmetric working states). Two 1-turn primary windings are connected in parallel to share the large primary current and thus reducing the winding loss. Two 6-turns secondary windings are laid symmetrically one both sides of the primary windings which are connected in series to form 12 turns. 3-D Finite Element Analysis (FEA) is carried out in order to verify the analysis and design. The simulation result shows leakage inductance  $L_d$  is  $30 \text{ nH}$ . The small value proves the feasibility of the partially interleaving structure. The transformer parameters are shown in TABLE III.

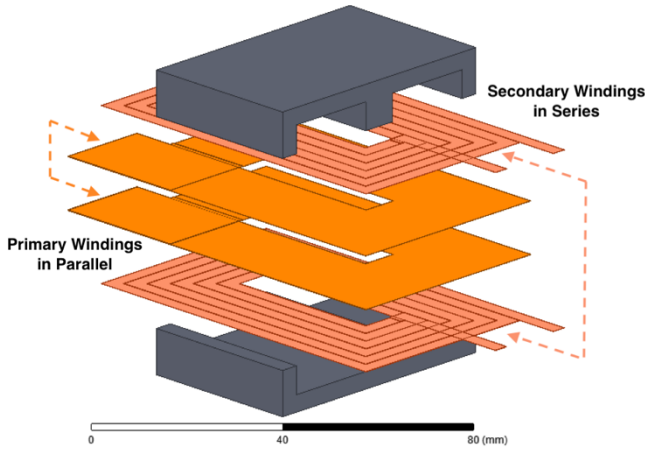


Fig.4. Interleaving Structure

TABLE III. TRANSFORMER PARAMETERS

Quantity	Parameters
Core type / material	E58_11_38 / 3F36
Pri-winding category	Planar PCB winding copper winding
Structure of pri-winding	1 turn / 2* 1 turn in parallel / 2 windings
Geometry of pri-winding	210 mm(L)*21.8 mm(W)*70 um(T)
Sec-winding category	Silk covered stranded copper litz wire
Structure of sec-winding	12 turns / 2*6 turns in series / 1 winding
Geometry of sec-winding	802 mm(L)*15 strands*0.2mm(D)

#### D. Losses Calculations

##### a) Conduction Loss

Leakage inductance may be affected by some aspects such as the manufacturing precision of magnetic components. Considering the uncertainty of the leakage inductance, a pair of calculation with a range of leakage inductance value is carried out and plotted in MATLAB with the corresponding RMS values of resonance current shown in Fig.5. The total conduction loss of two switches  $S_1$  and  $S_2$  can be calculated,

$$P_{con} = 2I_{RMS}^2 \cdot R_{on} = 0.76 \text{ W} \quad (11)$$

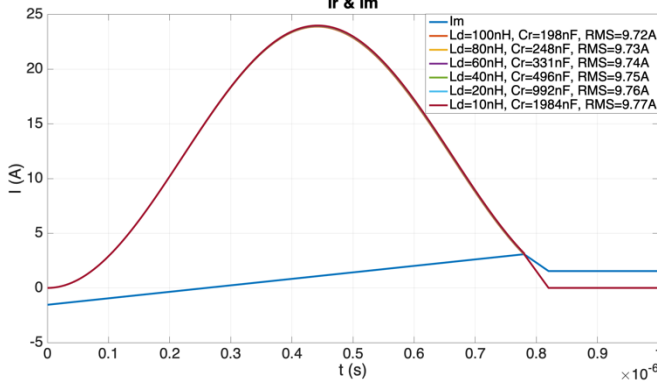


Fig.5. Resonance Current and Magnetizing Current in MATLAB

##### b) Winding Loss

Based on Dowell's assumptions and the general field solutions for the distribution of current density in a single layer, the ac resistance of  $m^{th}$  layer is derived as [12],

$$\frac{R_{ac,m}}{R_{dc,m}} = \frac{\xi}{2} \left[ \frac{\sinh \xi + \sin \xi}{\cosh \xi - \cos \xi} + (2m-1)^2 \cdot \frac{\sinh \xi - \sin \xi}{\cosh \xi + \cos \xi} \right] \quad (12)$$

where  $\xi = h/\delta$ ,  $h = 70 \mu\text{m}$  is the copper thickness for the PCB windings and  $\delta = 0.075/\sqrt{f_s}$  is the skin depth in conductor, and  $m$  is defined as a ratio in,

$$m = \frac{F(h)}{F(h) - F(0)} \quad (13)$$

where  $F(0)$  and  $F(h)$  are the magneto-motive force (MMF) at the limits of a layer [15], as shown in Fig.6.

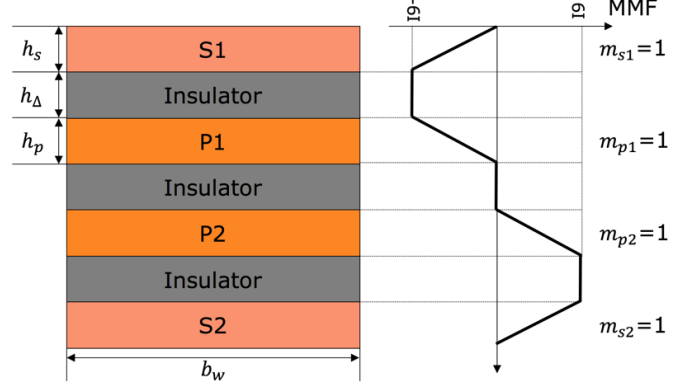


Fig.6. MMF Distribution

For either part of primary windings which are connected in parallel. The  $R_{ac,p}/R_{dc,p}$  ratio can be calculated according to (12). And DC resistance:  $R_{dc,p} = \rho \cdot l/A$ , where  $\rho = 2.3 \cdot 10^{-8} \Omega \cdot \text{m}$  is the resistivity of copper at  $100^\circ\text{C}$ ,  $l$  and  $A$  are the length and cross section area of the wire which can be calculated based on the geometry of the core.

So AC resistance can be calculated:  $R_{ac,p} = \frac{R_{ac,p}}{R_{dc,p}} \cdot R_{dc,p}$ ,

for both primary windings the winding loss is,

$$P_{priwind} = 2I_{RMS}^2 \cdot R_{ac,p} \quad (14)$$

for two 6-turns secondary windings which are connected in series. With the similar calculation method as mentioned above, the secondary part winding loss is,

$$P_{secwind} = 2 \left( \frac{I_{RMS}}{12} \right)^2 \cdot R_{ac,s} \quad (15)$$

the total winding loss is:  $P_{wind} = P_{priwind} + P_{secwind}$ .

##### c) Core Loss

Steinmetz equation is used for calculating core loss,

$$P_v = K \cdot f_s^\alpha \cdot \left( \frac{\Delta B}{2} \right)^\beta \quad (16)$$

where  $K, \alpha, \beta$  are constants provided by the core manufacturer. And  $\Delta B$  is the peak-to-peak flux density which can be calculated from Faraday's law,

$$\Delta B = \frac{V_n \cdot \Delta t}{N \cdot A_e} \quad (17)$$

where  $N$  is the number of turns,  $A_e$  is the effective area of the core. The core loss can be calculated:

$$P_{core} = P_v \cdot V_e \quad (18)$$

where  $V_e$  is effective volume of the core.

## IV. BUCK-BOOST ACTIVE CLAMP FLYBACK CONVERTER

### A. Proposed Circuit and Operation Principles

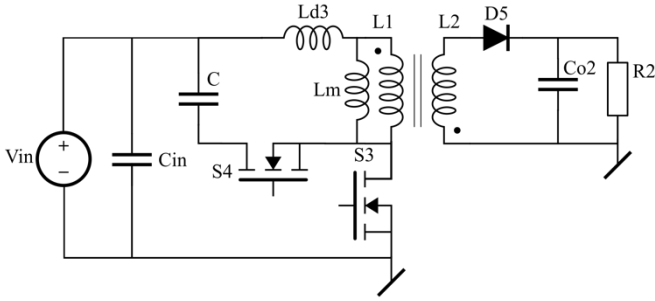


Fig.7. Active-clamp Flyback(ACF) Converter

The active-clamp flyback circuit is shown in Fig.7. An active clamp flyback converter is used to regulate the output voltage, which is connected with the push-pull converter in parallel in primary side and in series in secondary side as shown in Fig.1. Considering the input voltage at its minimum value, the ACF should transfer the maximum power. On the other hand, it transfers the minimum power at the maximum input voltage. The ACF should be designed to reach high efficiency under the maximum power, because it affects the total system efficiency more than the circumstance under the minimum power.

In traditional flyback converters, the main switch suffered from a large voltage spike and ringing due to leakage inductance when it turns off. In addition, the transformer for flyback converter is a coupled inductor. No flux cancellation can be achieved and interleaving strategy cannot be used to reduce the AC resistance. Consequently, tradition flyback converter suffers from larger winding loss at high frequency[16].

For the ACF converter, the energy stored in the leakage inductance is utilized to achieve the ZVS. No voltage spike and ringing occur to the main switch. More importantly, the reverse primary current reduces the magnetic field strength and the total winding loss can be reduced by applying interleaving winding layout [16]-[18]. Besides, discontinuous conduction mode (DCM) is more preferable since the small leakage inductance can be easily integrated into the transformer.

### B. Design Considerations for ACF

#### a) Clamp Capacitor

The turn-off current on auxiliary switch and secondary rectifier are small if the half resonant period formed by clamp capacitor  $C$  and leakage inductance  $L_d=L_{d3}$  is close to the turn-off time of the main switch. However, the primary RMS current increases with the smaller clamp-capacitor. On the other hand, the larger clamp capacitor  $C$  means smaller primary RMS current while larger turn-off current on auxiliary switch and secondary rectifier [19]. Therefore, the selection of clamp capacitor should be based on the converter total power loss. In this design, conduction loss is dominant because primary winding and switches suffers from large conduction current. The large clamp capacitor is selected to minimize the conduction power loss.

#### b) Turns Ratio

Both winding loss and core loss should be considered for the transformer turns ratio selection. ML91S has been proved to be an excellent material for high frequency transformer design [20], which is used for the transformer magnetic core. The flux density for the magnetic core can be calculated as,

$$B_{peak} = \frac{V_{in} \cdot D \cdot T_s}{2N_p \cdot A_e} \quad (19)$$

where  $D$  is the duty cycle of the main switch;  $T_s$  is switching period;  $N_p$  is the number of turns of primary winding.

Traditionally, the core loss is calculated by  $P_{core} = P_v \cdot V_e$ , where  $V_e$  is the volume of the core and  $P_v$  is calculated by Steinmetz's equation:  $P_v = K_c \cdot f_s^\alpha \cdot B_{peak}^\beta$ . where three quantities  $K_c$ ,  $\alpha$  and  $\beta$  can be calculated from relationship curve between unit volume core loss and flux density given in the datasheet of magnetic material.

In this case, winding loss is dominant. A trade-off is made between core loss and winding loss. 100 mT is determined to be the peak flux density for the magnetic core and the corresponding turns ratio is 2:4.

#### c) Magnetizing Inductance

This converter is built to operate under DCM. The reverse magnetizing current helps to achieve ZVS. The magnetizing inductance can be designed smaller than the critical value between the DCM and CCM. Usual methods can be used to determine this critical value. The parameters for the designed ACF is  $L_m = 2 \mu\text{H}$ ,  $L_r = 56 \text{ nH}$ ,  $C_r = 1.04 \mu\text{F}$ .

## V. EXPERIMENT RESULTS

The photo of experimental prototype is shown in Fig.8. The tested parameters from Precision Impedance Analyzer Agilent 4294A for the designed push-pull are shown in Fig.9 and Fig.10 which accounts for the value:  $L_m = 6.4 \mu\text{H}$ ,  $L_d = 53.0 \text{ nH}$ ,  $R_{ac} = 9.7 \text{ m}\Omega$ . The small value of leakage inductance further proves the correctness of interleaving structure. Also, the value of magnetizing inductance and AC resistance is in reasonable range. Thus, the resonance capacitor  $C_r$  is tuned to be 547 nF to performs the best waveforms.

The main switch  $I_{ds}$  and  $V_{ds}$  waveforms for full power with 24 V and 32 V input voltage are shown in Fig.11 and Fig.12. As we can see from the figures, the main switches of push-pull converter are operating under both ZVS and ZCS.

With 24 V input voltage, the ACF converter reaches its maximum power 112 W under full power condition. So optimal operating point of ACF converter is aimed for 24 V input voltage where the efficiency is shown in Fig.13. The efficiency of push-pull converter is shown in Fig.14. The corresponding losses breakdown for 24 V input voltage under full power condition is shown in Fig.15 where the winding loss is calculated from the experimental result of AC resistance  $R_{ac}$  and other losses are calculated from theoretical analyses. The efficiency of the whole system is shown in Fig.16.

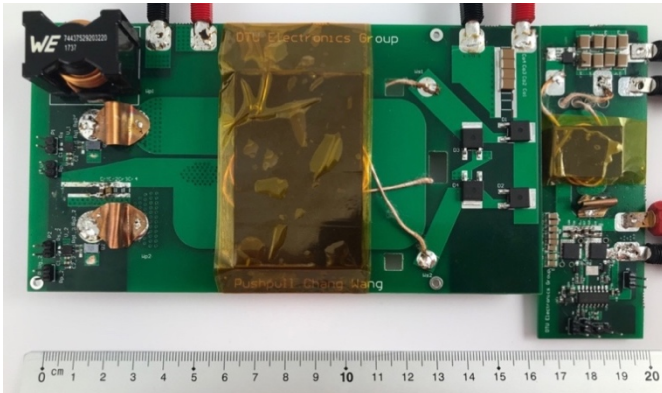


Fig.8. Photo of Experimental Prototype

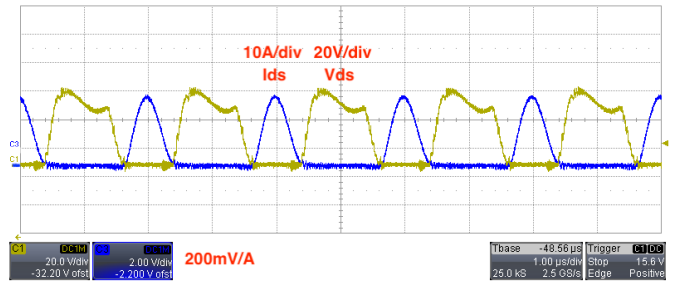


Fig.11. Main Switch Waveforms of 24 V Input

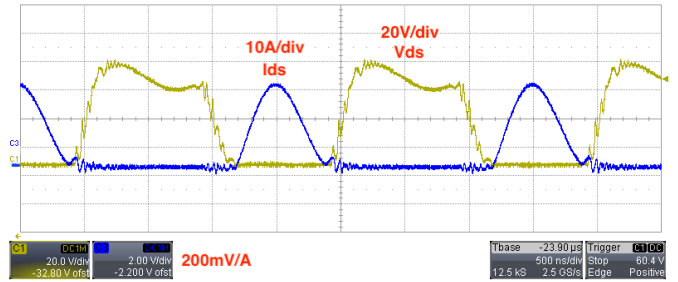


Fig.12. Main Switch Waveforms of 32 V Input

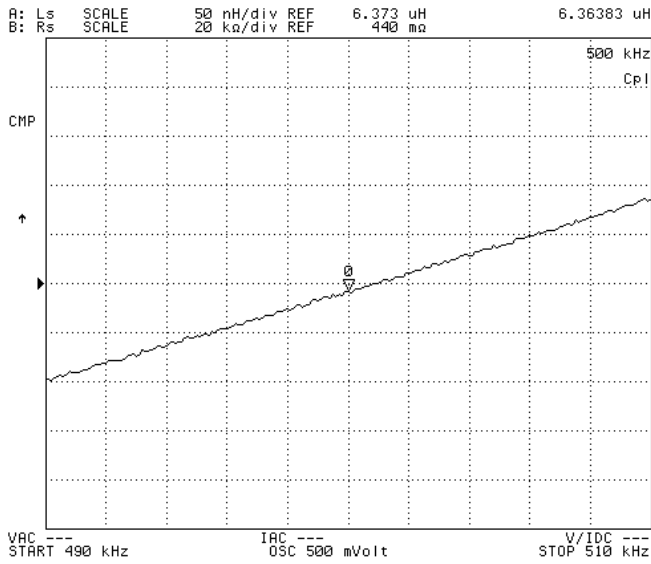


Fig.9. Tested Magnetizing Inductance  $L_m$

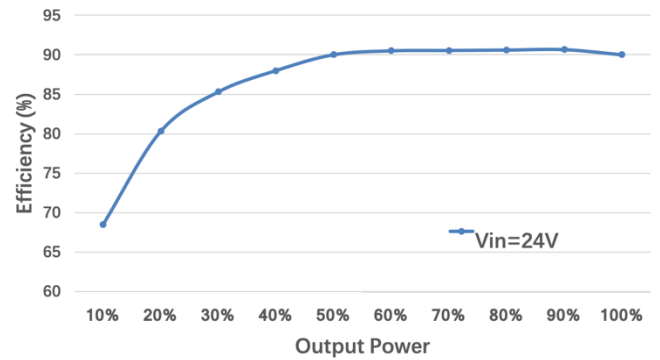


Fig.13. ACF Converter Efficiency Curve

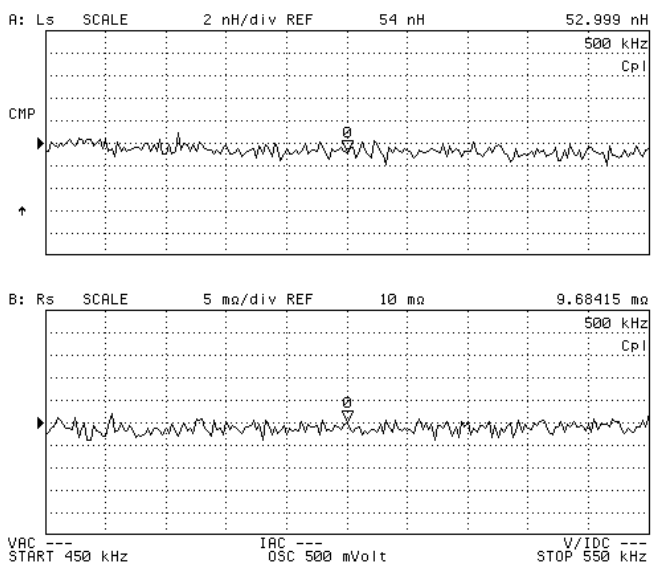


Fig.10. Tested Leakage Inductance  $L_d$  and AC Resistance  $R_{ac}$

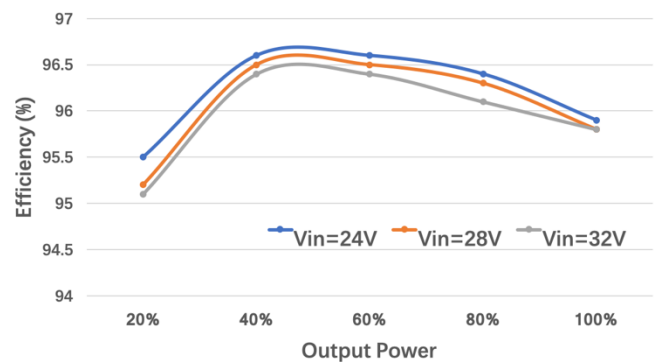


Fig.14. Current-fed Push-pull Converter Efficiency Curve



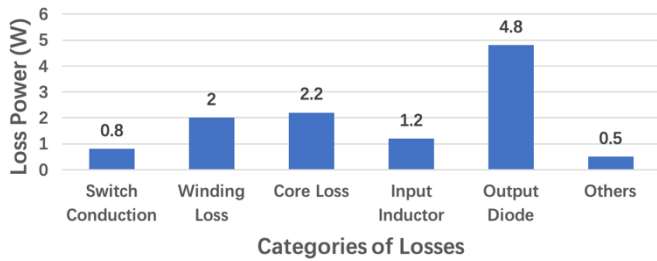


Fig. 15. Losses Breakdown under 24 V Input Voltage and Full Power

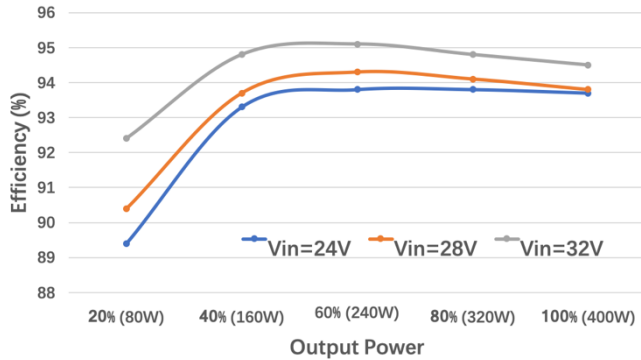


Fig. 16. System Efficiency Curve

## VI. CONCLUSION

This study proposed, analyzed and quantified a high efficiency and high step-up isolated DC-DC converter with a new topology configuration. A ZVS/ZCS current-fed push-pull converter and an active clamp flyback converter are connected in input-parallel-output-series structure which is suitable for unregulated dc-dc conversion from a low-voltage high-current source. From the experimental results, the main switch of push-pull converter can be operated under both ZVS and ZCS. The operating principles and theoretical analysis of this proposed converter were verified by using a 400 V/ 400 W prototype. The maximum efficiency reaches 95.1% and the overall efficiency of the system is above 93.5% at full output power within the whole range of input voltage.

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