Universitat Politècnica de Catalunya

Departament d'Enginyeria Elèctrica

Doctoral Thesis

DC current flow controllers for meshed HVDC grids

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"All we have to
decide is what to do
with the time that
is given us."

J. R. R. Tolkien

To Montserrat,
Pere, Núria
and Josep

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Abstract

Meshed High Voltage Direct Current (HVDC) grids are seen as a solution to transmit and exchange high amounts of power across long distances with high levels of flexibility and redundancy. Also, they can be especially suitable for integrating offshore energy resources such as offshore wind power.

This thesis focuses on the DC Current Flow Controllers (CFC) for meshed HVDC grids. CFCs are being thought as power electronics based devices that may be installed in future meshed HVDC grids to aid in the current flow regulation. The concept is similar to Flexible Alternating Current Transmission Systems (FACTS) but applied to HVDC grids.

Firstly, an overview of the different CFC concepts found in the literature is presented. Then, the modelling and control of a DC/DC CFC converter is developed and the benefits of installing it in a meshed HVDC grid are analysed. The functionality of the previous CFC is also integrated into a DC Circuit Breaker (DCCB), in order to have a single device with both capability to interrupt DC faults and provide DC current regulation. Afterwards, an interline DC/DC CFC topology is proposed, which has the advantage of a simplified converter structure. It is validated using dynamic simulations and a prototype is built and tested in a meshed DC grid experimental platform.

A single CFC may not be enough to regulate the current flows in complex meshed HVDC grids, thus, this work also considers the concept of Distributed CFCs (DCFC) in a meshed HVDC grid, which are being operated selectively, allowing more flexibility when regulating the current flows.

Also, multiple lines can be connected to a certain HVDC node, therefore, the presented CFC is extended to be connected to any number of HVDC lines and so, be able to control the current circulating through any of them. The obtained multi-port CFC is validated using simulations.

Other devices can help to the current regulation in meshed HVDC grids, for example already installed DC/DC converters that adapt the different voltages of the HVDC systems. A transformerless DC/DC topology is analysed in this work and the design of its AC filter addressed.

Finally, taking into account that some HVDC links based on Line Commutated Converters (LCC-HVDC) are installed near to potential offshore wind power resources, this work studies the operation and control of a Current Source Converter (CSC) based tapping station connected in series with the HVDC link to integrate offshore wind power.

Resum

Les xarxes d'alta tensió mallades en contínua, *meshed High Voltatge Direct Current* (HVDC) *grids*, es presenten com una solució per transportar grans quantitats d'energia a través de llargues distàncies o mitjançant cables submarins amb alts nivells de flexibilitat i redundància. També, són especialment adequades per la captació d'energia de parcs eòlics marins.

Aquesta tesi se centra en els controladors del flux de corrent, *Current Flow Controllers* (CFC), per a xarxes HVDC mallades. Els CFC es plantegen com dispositius d'electrònica de potència que es podrien instal·lar en les futures xarxes HVDC mallades per tal d'ajudar en la regulació dels fluxos de corrent de les línies. Aquest concepte és similar als dispositius FACTS (*Flexible AC Transmission Systems*), però aplicat a xarxes HVDC.

Primer, es realitza un recull de les diferents propostes de CFCs a la literatura. Després, es modelitza i es dissenya el control d'un convertidor DC/DC CFC i s'analitzen els beneficis d'instal·lar-lo en una xarxa HVDC mallada. La funcionalitat de l'anterior CFC s'inclou en els interruptors de contínua, *DC Circuit Breakers* (DCCB), per tal de tenir un dispositiu amb capacitat d'interropre faltes DC i també controlar corrents. A continuació, es proposa una topologia de CFC simplificada, que es valida per mitjà de simulacions i se'n construeix un prototip que es prova experimentalment al laboratori.

Un únic CFC pot no ser suficient per a controlar els fluxos de corrent en xarxes HVDC mallades d'una certa complexitat. És per això, que també s'introdueix el concepte de CFCs distribuïts en diferents nodes de la xarxa i que s'operen de forma selectiva.

Vàries línies HVDC poden estar connectades a un node, és per això, que la topologia de CFC anteriorment presentada s'actualitza per tal de poder ser connectada a un nombre qualsevol de línies. La topologia *multi-port* obtinguda es valida per mitjà de simulacions.

Altres dispositius que poden ajudar a controlar els fluxos de corrent són els propis convertidors DC/DC que s'encarreguen d'adaptar la tensió dels sistemes HVDC. S'analitza un convertidor DC/DC sense transformador AC i es realitza un disseny del seu filtre AC.

Finalment, algunes de les línies HVDC basades en tecnologia *Line Commutated Converter* (LCC) es troben a prop de zones amb energia eólica potencial. Per aquest motiu, s'estudia l'operació i control d'un convertidor *Current Source Converter* (CSC) que actua com una estació de *tapping* per tal d'injectar l'energia d'un parc eòlic marí a la línia LCC-HVDC.

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Nomenclature

2B-CFC	Dual H-Bridge CFC
ABB	ASEA Brown Boveri
AC	Alternating Current
CB	Circuit Breaker
CFC	Current Flow Controller
CIGRÉ	Conseil International des Grands Réseaux Électriques
CITCEA	Centre d'Innovació en Convertidors Estàtics i Accionaments
CL	Current Loop
CSC	Current Source Converter (self-commutating)
DAB	Dual Active Bridge
DC	Direct Current
DCCB	DC Circuit Breaker
DCFC	Distributed Current Flow Controller
DSP	Digital Signal Processor
dSPACE	Digital Signal Processing and Control Engineering
FACTS	Flexible Alternating Current Transmission Systems
FDCTS	Flexible Direct Current Transmission Systems
FPC	Full Power Converter
GE	General Electric
GSC	Grid Side Converter
HCB	Hybrid Circuit Breaker
HF	High Frequency
HV	High Voltage
HVDC	High Voltage Direct Current
HVAC	High Voltage Alternating Current
IGBT	Insulated-Gate Bipolar Transistor
IMC	Internal Model Control
LCC	Line-Commutated Converter
LV	Low Voltage
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor

NPO	Non-Possible Operation
OWPP	Offshore Wind Power Plant
PFC	Power Flow Controller
PHCB	Proactive Hybrid Circuit Breaker
PI	Proportional-Integral controller
PMSG	Permanent Magnet Synchronous Generator
PMSM	Permanent Magnet Synchronous Machine
PLL	Phase Locked Loop
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Mean Square
SCR	Short Circuit Ratio
TL	Transformerless
TSO	Transmission System Operator
UPC	Universitat Politècnica de Catalunya
VSC	Voltage Source Converter
WEC	World Energy Council
WFC	Wind Farm Converter
WPP	Wind Power Plant

Chapter 1

Introduction

1.1 Current context

The European Union (EU) has set a series of ambitious climate and energy targets to fight against climate change. The 2020 targets [1] established three key objectives for the year 2020, which are the 20% reduction in greenhouse gas emissions (from 1990 levels), the commitment that the 20% of the EU energy consumption must come from renewable resources and a 20% improvement in energy efficiency.

The targets beyond 2020 are even more ambitious, specifically for 2030 are the following ones: the cuts in greenhouse gas emissions are set at 40% with respect 1990 levels, the share in consumption coming from renewable resources is to be increased to 27% and also the efficiency must improve in a 27% [1].

The role of wind generation will be decisive in order to meet the current climate and energy commitments [2]. At the end of 2017, wind energy accounted for the 18% of EU's total installed power generation capacity [3] and during the same year covered 11.6% of the EU's electricity demand. Among Wind Power Plants (WPP), offshore installations present a number of benefits compared to the traditional onshore installations. These benefits lie on the availability of higher wind speeds, the possibility to transport larger structures (bigger wind turbines able to extract more wind power) and the fact that some onshore locations are already saturated with older wind turbines.

The cumulative wind power installations from 2005 to 2017 can be seen in Fig. 1.1.

The numbers show that the European installed capacity of wind power was at the end of 2017 168.7 GW and 15.8 GW of those belong to offshore installations [3]. By 2020, the installed wind capacity is expected to reach 204 GW, of which 25 GW will be from offshore.

The cumulative wind power installations by country at the end of 2017

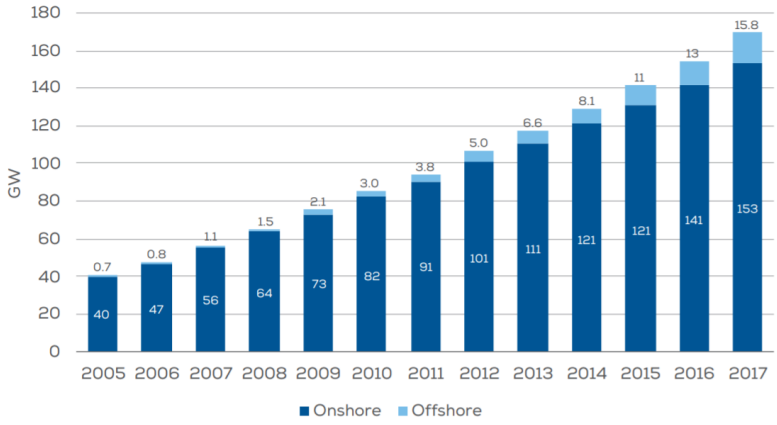

Fig. 1.1: Cumulative wind installations onshore and offshore in the EU. Total: 168.7 GW. Source: WindEurope [3].

are shown in Fig. 1.2. Germany is the leading country in installed capacity, followed by Spain and UK [3].

Offshore Wind Power Plants (OWPP) can be connected to the AC grid using High Votlage Alternating Current (HVAC) or High Voltage Direct Current (HVDC) technologies [4]. The choice between them depends on the economic aspects, which depend in turn on the transmission distance and power rating [4]. In HVAC, there is the need to compensate the impedance of the cables, and this grows with the distance of the transmission at a higher rate than for HVDC. On the other side, HVDC implies a fixed cost for the converter stations. Therefore, there is break-even distance where the HVDC option has a lower price than HVAC. This break-even distance for submarine cables is around 100 km [4].

Among HVDC technologies, there are two commercial options: Line-Commutated Converters (LCC) using thyristors and Voltage Source Converters (VSC) employing self-commutating devices [5]. LCC-HVDC transmission systems have been the traditional option and possess a high degree of reliability and maturity, with many stations interconnecting mainland and islands. The available power and voltage levels are also higher in LCC-HVDC compared to VSC-HVDC. However, VSC-HVDC seems more suitable to interconnect OWPPs due to the following reasons: active and reactive power can be controlled independently, they can feed passive loads without an AC grid to operate. They also have black-start capability and a reduced footprint compared to LCC-HVDC due to a reduction of the ouput

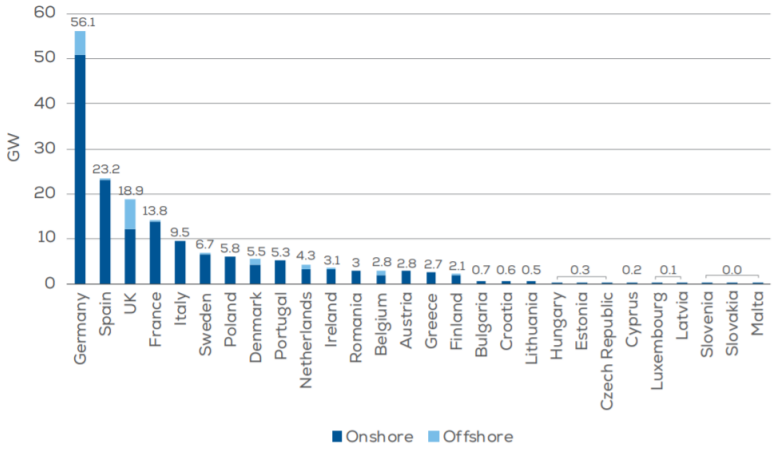

Fig. 1.2: Cumulative installations onshore and offshore by country. Total: 168.7 GW. Source: WindEurope [3]

filter requirements [6, 7]. This last feature is especially relevant for offshore applications, where the footprint and weight of the converter station play an important role [4].

The latests VSC-HVDC designs based on Modular Multilevel Converters (MMC) [8] employ the cascading of a large number of submodules per arm. This concept allows to handle higher DC voltages by simply adding more submodules and the switching frequency can be reduced while still fulfilling the requirements on harmonic distortion in the output voltage. This fact implies that the losses drop and the converter also has benefits at the manufacturing stage as it is composed of a number of identical units (submodules) [9].

The world's first VSC-HVDC for offshore power transmission (BorWin1) was constructed off the coast of Germany in 2009 by ABB. Since then, a number of VSC-HVDC links for the integration of offshore wind power have been constructed successfully offshore in the north of Germany. Three of them have been delivered by ABB (BorWin 1, DolWin 1 and DolWin 2) [10] and the others (BorWin2, SylWin1, HelWin1 and HelWin2) have been handed over to the same customer, TenneT (German-Dutch TSO), by Siemens [11]. An image of the offshore platform of Dolwin 1 is shown in Fig. 1.3.

Fig. 1.3: DolWin1 offshore wind platform. Source: ABB [12].

1.2 HVDC grids

The existing VSC-HVDC links in Europe are point-to-point connections, which means that each converter station is directly connected to another single converter by means of an HVDC line. More terminals can be added and interconnected with the existing links, evolving into a multi-terminal HVDC system, something that is being studied in Europe but that is a reality in China, where two multi-terminal HVDC systems are in operation: Nan'ao project (3 terminals) and Zhoushan project (5 terminals) [13].

The increased offshore wind penetration is one of the drivers of this multi-terminal initiative, since such a scheme could ease the power exchange and increase the flexibility of the network, while reducing the renewable energy intermittency [14]. Besides, there is the opportunity to create meshed HVDC grids offshore, both interconnecting different countries and transmitting the generated offshore wind power. The offshore grid concept can eventually evolve into the so called European Supergrid [15], which consists on the interconnection by means of an HVDC grid of the different European states and allows the integration of multiple renewable resources. Such a concept, provides a number of advantages in terms of efficiency, especially

compared to point-to-point HVDC and HVAC, but requires standardisation and coordination. The development of HVDC grids presents many technical challenges: definition of optimum grid topologies; reliable and cost effective power converters able to create AC grids and give support to the existing AC systems when required; development of technologies to control the power flows within the grid and grid operation and control strategies; HVDC circuit breakers with reasonable cost to isolate faults; voltage control during normal and fault conditions. Also, non-technical challenges as grid ownership and legal aspects are crucial. [4].

Currently, the first meshed HVDC grid is being designed in China, the so called Zang-Bei project, which is meant to secure power supply to Beijing from a variety of clean sources including wind, solar and hydro power [16]. In phase 1, four VSC stations will be built and interconnected through HVDC in a ring configuration. Three of the terminals will have a rating of 1500 MW/ $\pm$500 kV each and the rating of the other receiving terminal is expected to be of 3000 MW/$\pm$500 kV. Two more terminals have also been planned for phase 2, with commissioning expected in 2021 [13].

The present thesis focuses on the challenge of the development of technologies to control the power flows within the meshed HVDC grids. It is reasonable to assume that if complex HVDC grids are built, they will not be constructed all at once, but built from the interconnection of point-to-point HVDC links and multi-terminal HVDC systems. Each one of them will have different power ratings and limitations, and due to this, power flow control becomes a concern.

In a meshed HVDC grid, the power flows cannot be controlled independently for each line, but they are determined passively by the resistances between nodes and the DC voltages applied at each node by the VSCs [17]. A poor power flow management can lead to exceed the current rating of the cables or create bottle-necks that restrict the overall operation of the entire HVDC grid [18].

To tackle this challenge, additional devices, named Power Flow Controllers (PFCs) or Current Flow Controllers (CFCs), based on power electronics, may be installed in the grid [17, 18]. Those devices are the equivalent to Flexible Alternating Current Transmission Systems (FACTS) but applied to DC grids, the so called Flexible Direct Current Transmission Systems (FDCTS) [19,20]. They can provide additional degrees of freedom to control the current flows by slightly modifying the voltage at one end of the desired HVDC line. Due to the reduced value of cable resistances, a small DC voltage variation can be translated into a large change in the DC current (applying few kV, hundreds of A can be redirected) [17].

1.3 Objectives and scope

This Section presents the objectives and scope of the work conducted by the author during the realisation of this thesis. Fig. 1.4 depicts a conceptual overview of a number of HVDC systems used to interconnect different countries and to integrate offshore wind power. Submarine cables are assumed for the interconnections and two voltage levels for the HVDC systems are considered: Low Voltage (LV) HVDC and High Voltage (HV) HVDC. The wind turbines represent OWPPs that are interconnected by means of HVDC systems and the different converter topologies are depicted with coloured boxes. The AC grid is not illustrated but it is assumed to be present in the mainland. The previous figure serves as a roadmap to introduce the different topics that have been analysed throughout this thesis.

Firstly, the modelling and control of a 3-port interline DC/DC Current Flow Controller is analysed (1) and the increase in the operational range that it provides is also investigated. Then, this work continues by proposing an additional 3-port interline DC/DC CFC topology to regulate the current flows with a reduced number of switches (1). The previous CFC topology is used as a building block to develop the concept of distributed CFC devices with a simplified structure that are installed in different nodes of the grid and that are being operated selectively (2). Afterwards, the thesis proposes a multi-port CFC converter structure that can be connected to any number of lines, which is based on the previous CFC topology (3). Taking into account that DC Circuit Breakers (DCCB) are going to be required in HVDC grids, this thesis presents the idea of integrating the CFC capability into the DCCB design, obtaining a device able to provide both functionalities (4). Focusing on the interconnection of HVDC lines with different voltage level, this thesis also investigates a DC/DC converter for high power and high voltage applications which is based on the autotransformer concept, where the transformer has been substituted for an AC filter. This converter can also be used to control the power flow between the lines where it is connected (5). Finally, the operation and control of a tapping station based on a Current Source Converter of an LCC-HVDC link is investigated. The previous device shares some features with CFCs as it is also connected in series and applies a variable voltage source, though it is used to integrate offshore wind power (6).

After introducing the topics analysed in the thesis, the objectives and scope are described below:

- **Analyse the different CFC concepts presented so far in the**

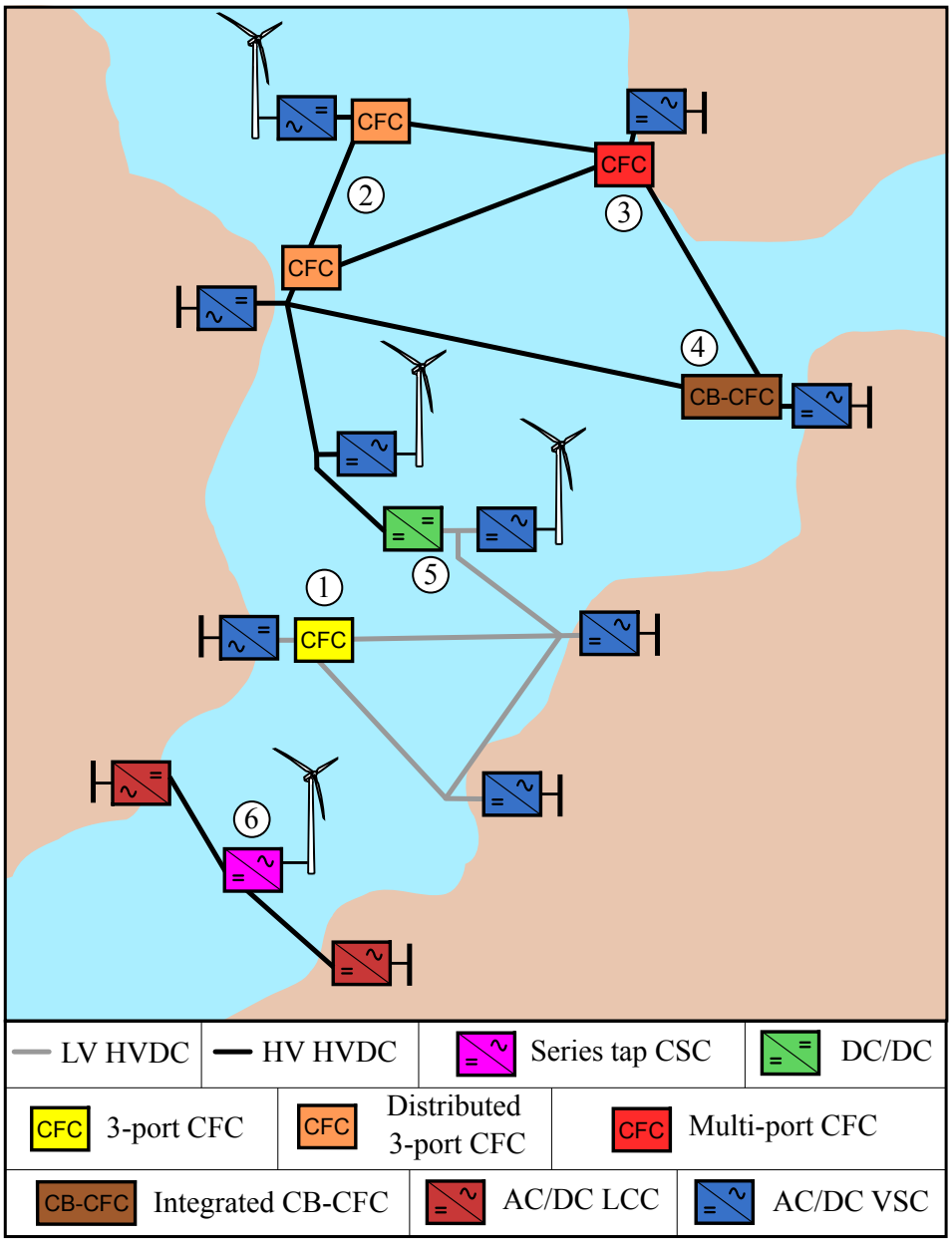

Fig. 1.4: Global overview of HVDC systems including point-to-point links and meshed HVDC grids used to integrate offshore wind power and interconnect different countries.

literature. The state of the art of the CFCs is described, gathering the CFC proposals in parallel-connected, series-connected and series-parallel-connected devices. The series-connected CFC are classified in three different groups: variable resistances, AC/DC converters and DC/DC converters.

- **Analyse the modelling and design the control of a 3-port interline DC/DC CFC**. The modelling of the CFC topology is provided and an average model of the device is obtained and used to analyse the steady-state operation of the CFC in a meshed HVDC grid to illustrate its benefits. Then, the model of the whole system is linearised and the control of the CFC is designed considering a single current loop and a cascaded approach with a voltage and a current loop to avoid high voltages in the device. After, the control is validated using dynamic simulations.

- **Investigate how the CFC functionality can be integrated into a DC hybrid circuit breaker**. First the two devices are presented separately and it is shown how the two functionalities are included in a single layout. A state-space modelling of the CB-CFC is provided, analysing the commutation process. Then, the CFC controller of the integrated device is designed and verified in a meshed HVDC grid using detailed models of the system. After, the protection performance of the integrated device and the separate devices is also compared by means of simulations.

- **Present a 3-port interline DC/DC CFC topology for unidirectional current flows with a reduced number of switches and validate the CFC experimentally**. The converter structure is detailed and its operating principle is presented. The CFC topology is compared to the one discussed in Chapter 3 identifying advantages and disadvantages. Then, an extended version of the converter is introduced to work with bidirectional current flows. Afterwards, the control of the bidirectional CFC is designed and validated through dynamic simulations. Finally, a unidirectional CFC prototype is built and tested in a 3-terminal meshed DC grid with different control approaches.

- **Analyse the selective operation of Distributed CFC devices**. The concept of Distributed CFC (DCFC) devices is presented, which consists on installing simplified CFCs in different nodes of the grid

and operating them selectively. The concept permits to use the most adequate CFC for a given overload and the CFC converter structure of each distributed CFC is derived from the previous unidirectional CFC topology. The analysis methodology to investigate the effect of introducing DCFCs and the corresponding operational area increase brought by the concept is presented. The distributed concept is also validated using dynamic simulations.

- **Extend the series interline DC/DC CFC topology to any number of lines**. The converter structure of the unidirectional series interline CFC is extended to be connected to any number of lines obtaining a multi-port CFC. The modelling, modulation and control strategy of the multi-port CFC are provided and a 5-port CFC is validated using dynamic simulations.

- **Analyse and design the AC filter Transformlerless DC/DC converter topology based on the autotransformer concept.** Among the topologies of DC/DC converters for high power and high voltage applications, the autotransformers can be rated for a fraction of total power of the interconnection since not all the power circulates through the AC transformer. In this work the AC transformer present in the topology is replaced and substituted for an AC filter with the aim of reducing its cost. The effect on the operational limits of the converter as a function of the filter parameters is investigated. The converter is, then, validated with the designed filter using dynamic simulations.

- **Design the operation and control of a series-connected CSC based tapping station of an LCC-HVDC link for integration of wind power**. The possibility of integrating wind power into an already built LCC-HVDC link is investigated. The tapping converter is a Current Source Converter with bidirectional capability, whose control is designed during normal operation and also under current reduction of the LCC-HVDC link, which can reduce the capability to extract wind power. A power reduction algorithm to face this issue is implemented to ensure the stability of the system and it is validated using dynamic simulations.

1.4 Work and activities during the thesis period

This section provides an overview of the chronological activities developed by the author during the thesis period, both the ones included and non-included in the thesis document.

The predoctoral activities started in March 2014 with a project with Alstom Grid (currently GE). The work consisted on the development of a current flow controller topology for the regulation of DC currents in meshed HVDC grids. The outcomes of that project were two patents filed [P1], [P2] and two journal papers were later published [J1], [J2]. Also, later on a conference paper [C3] related to [J1] was published.

During 2014 the project ENE2013-47296-C2-2-R ("Offshore wind power plants integration in the Spanish electrical system by multi-terminal HVDC links") started, which was funded by the Spanish Ministry of Economy and Competitiveness. The work developed in that project was focused on the integration of offshore wind power plants by means of a bidirectional tapping station of an HVDC link. From this work a conference paper [C1] and a journal paper [J4] were published, which are both part of this thesis. Another journal paper [J8] was published focused on the optimal operation of hybrid AC/DC grids, which is not included in the thesis.

The author participated in a project related to the state of the art of the superconductor cables during 2015. The project was funded by Red Eléctrica de España (Spanish TSO). The results of this project are not part of this thesis.

In 2016, the project ENE2015-67048-C4-1-R funded by the Spanish Ministry of Economy and Competitiveness started, whose name was "Breaking technical, economical and regulatory barriers for the development of DC Supergrids". From this work a conference paper was obtained [C2]. A number of collaborations were conducted with other universities during this period with the respective outcomes: Technical University of Denmark, journal paper [J6], conference paper [C5]; University of Porto, a journal paper [J7]; University of Manchester, a journal paper [J5]. Only, [J5] is part of the thesis.

The PhD European mobility was carried out from January 2017 to June 2017, at the ABB Corporate Research Center (CRC), Västerås, Sweden. The author participated in a project to study a transformerless DC/DC converter topology. Form this work, a conference paper [C4] and a submitted journal paper [S-J11] were obtained.

At the end of 2017, the author participated in a project funded by EIT InnoEnergy, which consisted on testing a three-phase active filter to com-

pensate unbalanced loads and harmonics. This work is not part of the thesis.

In 2017 a scholarship from Fundación Iberdrola in Spain was obtained to investigate the development of DC/DC converters to regulate the power flows in meshed HVDC grids. From this work, a journal paper was published [J3].

Finally, from the results of project ENE2015-67048-C4-1-R two journal papers were submitted [S-J9] and [S-J10], but only [S-J10] is included in the thesis.

The author is also a member of the EIT InnoEnergy PhD School.

1.5 Thesis outline

The contents of the thesis are organized as follows, where each chapter and the appendix A corresponds to one of the objectives of the work:

- **Chapter 2** presents the Current Flow Controller concepts that can be found in the literature. The different concepts are gathered and analysed qualitatively.
- **Chapter 3** deals with the Dual H-bridge CFC topology, which is a 3-port interline DC/DC converter. The modelling of the converter is provided and its control is designed. The operational area increase is also addressed and simulations are used to validate the designed controllers.
- **Chapter 4** integrates the CFC capability of the Dual H-bridge CFC into an Hybrid Circuit Breaker (HCB). The combined circuit is presented and both functionalities are validated. A comparison of the performance of the presented concept and the CFC and the CB in a separate design is also given.
- **Chapter 5** introduces a 3-port series interline DC/DC CFC for unidirectional current flows with a reduced number of switches. The modelling and control of the device is presented and then validated using dynamic simulations. The topology is qualitatively compared with the one in Chapter 3. Finally, a prototype of the unidirectional CFC is built and tested in the laboratory.
- **Chapter 6** presents the concept of Distributed CFC devices installed in different nodes of the HVDC grid that are operated selectively. The Distributed CFC topology is derived from the converter structure from Chapter 5.
- **Chapter 7** extends the CFC topology presented in Chapter 5 for a generic number of lines and describes the modelling and the control strategy. It also provides a validation of a 5-port CFC using simulations.
- **Chapter 8** describes the Transformerless DC/DC converter topology and analyses and designs the AC filter investigating its effect on the operational limits of the converter.

- **Chapter 9** summarises the conclusions of the work and introduces the future research lines for each one of the research topics addressed.
- **Appendix A** presents the operation and control of a series tapping station based on a Current Source Converter of an LCC-HVDC link for integrating Wind Power Plants.
- **Appendix B** enumerates the publications related and non-related to the thesis.

Chapter 2

Review of power flow controllers or current flow controllers

Chapter 1 has introduced the need of additional devices acting as regulated voltage sources when dealing with meshed HVDC grids in order to regulate the current flows. This Chapter provides a review of the different concepts of CFC or PFC that have been proposed so far in the literature. CFC devices can be gathered in the three following groups according to the way they are connected to the HVDC grid:

- Parallel-connected CFCs
- Series-connected CFCs
- Series-parallel-connected CFCs

The previous concepts are illustrated in Fig. 2.1.

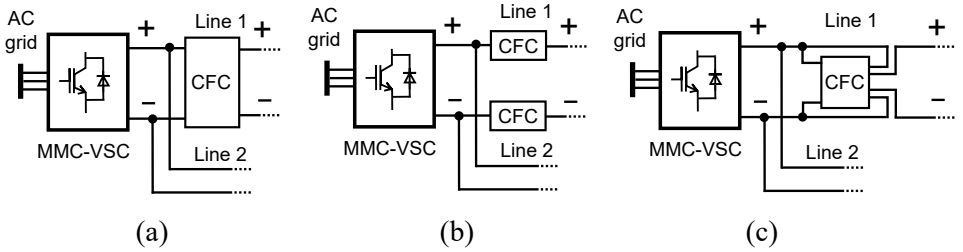

Fig. 2.1: CFC concepts. (a) Parallel-connected. (b) Series-connected. (c) Series-parallel-connected.

2.1 Parallel-connected CFCs

Parallel-connected devices are connected between the positive pole and the negative pole of the transmission system [17,21]. They are essentially DC/DC

transformers with a voltage transformer ratio between the input and the output that are used to interconnect HVDC systems with different voltage level and can provide other functionalities as power flow control [22]. According to [17], in power flow applications the needed voltage ratio between DC sides of the converter is in the order of 0.9 to 1.1. For instance, in [23, 24] a DC/DC transformer based on resonant converters for HVDC applications is suggested as a power flow controlling device. There are many proposals of DC/DC transformers that can be used to regulate the power flow between the lines [25]. Due to the high voltage and power requirement of the switches, topologies based on Modular Multilevel Converters are seen as a suitable technology to implement those structures [26].

The main drawback of parallel-connected devices is that they have to withstand the nominal voltage of the transmission system and need to be rated for the full power flowing through the device, which can mean hundreds of megawatts. Therefore, this leads to high costs not always justifiable for only power flow applications [26].

2.2 Series-connected CFCs

Series-connected can be smaller devices and are floating at the positive or negative pole of the HVDC system inserting a variable voltage in series with the line [17]. Therefore, they must not be rated for the nominal voltage of the transmission system but for the nominal current of the line. With few kV it is possible to regulate tens or hundreds of amperes since the cable resistances are very low [17]. This fact may diminish their cost, compared to parallel-connected CFCs and can make them more eligible to regulate current flows. The concept of a series CFC is analogous to the series tap on a traditional HVDC link [27]. The series tap is meant to absorb power from the link and unidirectional in terms of power flow, whereas the series CFCs may have bidirectional capability depending on the considered topology.

Another consideration regarding series devices is that they have to be placed in the positive pole and also in the negative pole, otherwise the symmetry of the current flow is lost in the HVDC grid [22]. For the reasons presented before, the series devices seem to be the preferred option to control and regulate current flows in a meshed HVDC grid.

They can be classified as: series variable resistors, AC/DC converters and DC/DC converters.

2.2.1 Series variable resistors

This proposal achieves the variable voltage source by means of a variable resistance in series with the line. A series variable resistor can be inserted in the DC grid to directly modify the impedance of the line. It allows to apply only positive voltage which reduces the current through that cable. Its main disadvantage is that the losses of the system get increased and may require additional cooling equipment [26], though, its simplicity is a key factor to take into account. Each unit is composed of a resistor and a pair of IGBTs to handle bidirectional current flows; a reactor to smooth the switching impact can also be added in series with the device [22]. As IGBTs have a reduced reverse blocking voltage, a diode can be inserted in series in each IGBT. Applying a duty cycle to the IGBT the mean value of the resistance can be changed from 0 to R, no current limitation to maximum current limitation, respectively. A scheme of the series variable resistor is shown in Fig. 2.2.

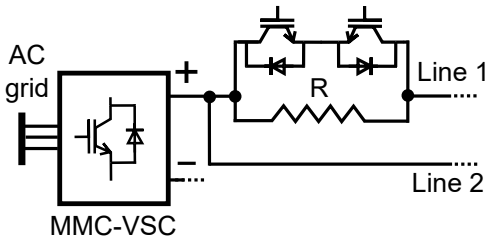

Fig. 2.2: Series variable resistor.

2.2.2 AC/DC converters

AC/DC converters exchange power between the AC system and the HVDC grid. Therefore, they apply positive or negative voltage in series with the line where they are connected and this allows to regulate the current flow. The voltage applied depends on the external AC source and the converter topology. An isolation transformer is required to be floating at the positive pole or the negative pole, so that the device does not need to withstand the nominal voltage of the DC system, only a small percentage of it [17]. The concept is very similar to traditional series tapping systems in HVDC links, with the difference the CFCs based on AC/DC converters need bidirectionality in terms of power. The AC/DC CFC concept is shown in Fig. 2.3.

Several topologies of AC/DC converters for power flow control have been proposed in the literature. An AC/DC controller made of two six-pulses thyristor converters connected in dual-configuration is presented in [28]. For

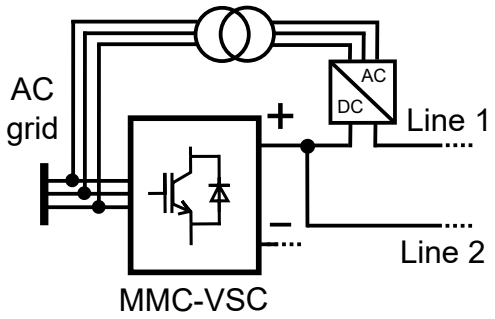

Fig. 2.3: AC/DC converters.

a given DC current direction, each converter has the ability to apply positive or negative voltage, acting as a rectifier or an inverter (four-quadrant operation). Although thyristor converters produce significant harmonics in the AC side, it is not severe as the CFC has a reduced power rating compared to the MMC-VSC terminal. It cannot control active and reactive power independently, however, it is not a major drawback for the same reason as before. Advantages lie in the simplicity and reliability of thyristor converters and their low losses. Fig. 2.4 depicts the scheme of the thyristor-based CFC.

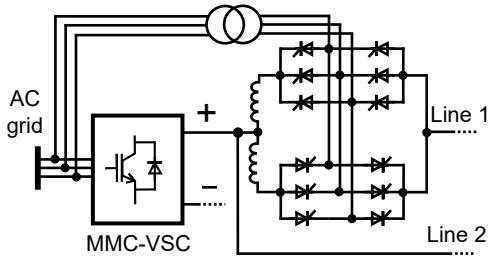

Fig. 2.4: Thyristor-based current flow controller.

Another proposal regarding AC/DC converters for power flow is the concept introduced in [29]. The converter is shown in Fig. 2.5 and it is made of a two-level, three phase VSC and a four-quadrant chopper. The switches are IGBT and are controlled with pulse-with-modulation (PWM) technique. The two-level VSC maintains the capacitor voltage constant, while the chopper regulates DC current by generating a variable mean DC voltage on the DC line. The chopper allows to operate with any direction of line current and charges or discharges the capacitor (four-quadrant operation). A transformer is used in the AC side in order to provide galvanic isolation an allow

the CFC to be floating at HVDC line voltage. This topology is more flexible since allows reactive power regulation in the AC side. Nevertheless, converter losses can be higher in comparison with the thyristor-based converter [28].

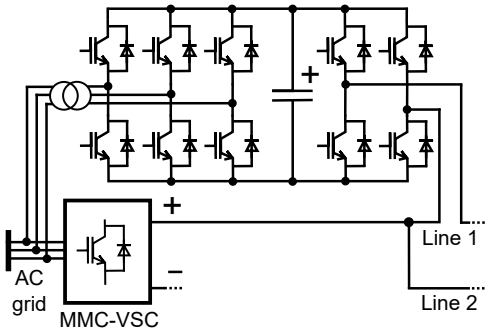

Fig. 2.5: IGBT-based current flow controller.

ABB has also filed two patents regarding AC/DC based CFCs [30,31]. In [30], the same concept as in Fig. 2.5 is introduced and in [31], an analogous AC/DC converter but based on modular multilevel current source technology [32] is presented.

2.2.3 DC/DC converters

DC/DC converters based CFCS exchange power between different lines of the HVDC system, thus they are also called *interline* CFCs [33]. Therefore, they do not require an AC grid to create the variable voltage source, thus, the AC isolation transformer is not needed. In comparison with the AC/DC converters, the variable voltage they can apply is limited by the HVDC line currents and the converter topology. They are also floating at the HVDC poles and the power extracted from one line is injected into the other line, applying positive voltage in one line and negative voltage in the other line if currents flows have the same direction. Fig 2.6 illustrates the general scheme of a DC/DC converter used for power flow regulation.

One of the first DC/DC converter for current flow control was proposed in [34] by Alstom Grid (currently GE) with the corresponding patent [35]. It consists on two H-bridges each one connected to one HVDC line. Fig. 2.7(a) shows the presented topology, which was chosen to take advantage of the standard Alstom VSC full-bridge [34]. Nonetheless, an alternative topology with the same functionality is depicted in Fig. 2.7(b), which consists on merging the two capacitors and removing the redundant switches. It allows

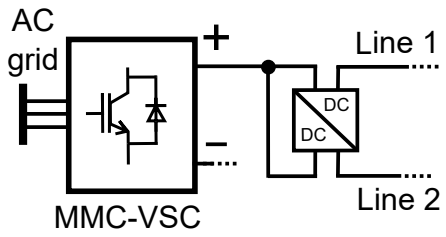

Fig. 2.6: DC/DC converter based CFC.

to apply positive or negative voltage in any line, and it is prepared to operate with any current flow through the lines. The capacitor is used to exchange power between the two HVDC lines. The previous topology is analysed in detail in the Chapter 3 of this thesis and other alternative control approaches are also presented in [36–38]. In [39], an experimental validation of this CFC topology is also provided along with the coordination and control of two of these converters in the same HVDC grid.

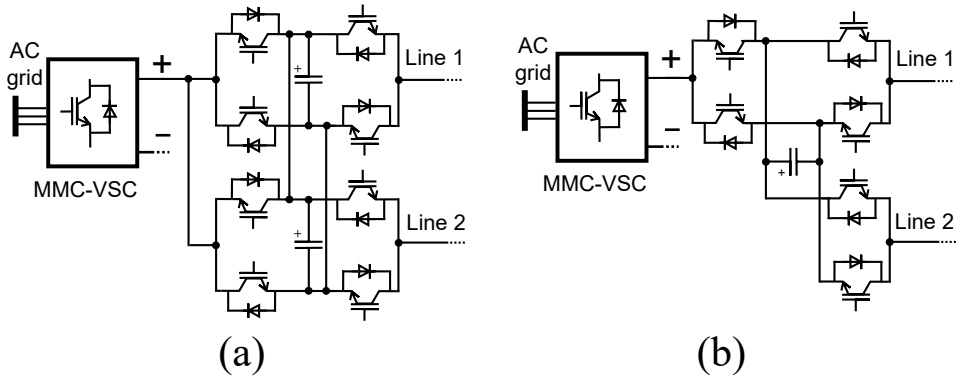

Fig. 2.7: Dual H-bridge. (a) General topology. (b) Simplified topology.

Another proposal of an interline DC/DC converter for power flow regulation is presented in [33]. Although this converter is made of two H-bridges as well, their switches require reverse-voltage blocking capability since capacitor voltages can be positive or negative. Introducing a diode in series with each IGBT is one option to achieve such capability. This device also allows to operate with any current flow. The element which exchanges power with the two H-bridges is an inductance (made of DC inductance plus an isolation transformer), instead of the capacitor used in [34]. The general topology scheme is depicted in Fig. 2.8(a).

When considering a three terminal meshed DC grid, the previous topology

can be simplified into Fig. 2.8(b). This converter topology is rather simple but it allows to operate only when line currents are entering the CFC, so that the MMC-VSC in Fig. 2.8(b) is acting as an inverter. The experimental validation of the structure in Fig. 2.8(b) is also presented in [33].

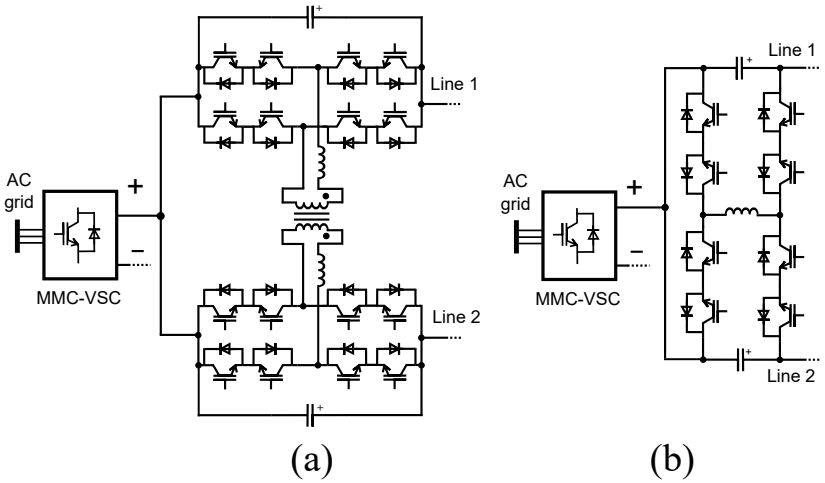

Fig. 2.8: Interline DC/DC topology. (a) General topology. (b) Simplified topology.

The same authors introduced and enhanced interline CFC topology that can operate with any current flow direction and that at the same time has a rather simple structure [40]. The CFC structure is depicted in Fig. 2.9. Another modification of this CFC topology can be found in [41], where the CFC is able not only to provide bidirectional power flow but also to be connected to HVDC lines with different voltage level.

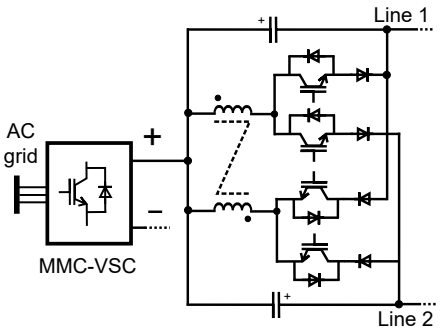

Fig. 2.9: Enhanced interline DC/DC topology.

In Chapter 5 of this thesis, a simplified interline DC/DC CFC structure for unidirectional current flow control is introduced and analysed, which was presented in the patent [42]. The two possible converter structures of the aforementioned topology are shown in Fig. 2.10.

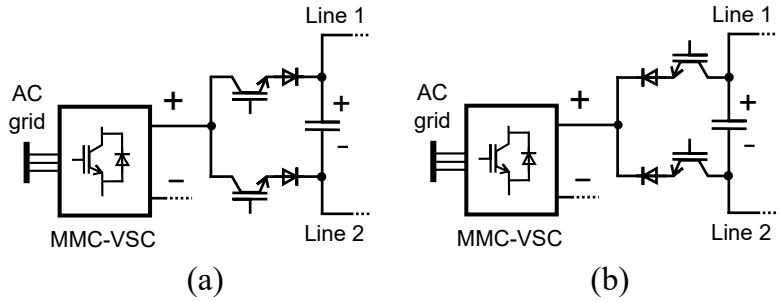

Fig. 2.10: Series interline DC/DC unidirectional CFC. (a) Structure when the currents of line 1 and 2 are going out the device. (b) Structure when the currents of line 1 and 2 are going in the device.

Finally, other approaches can also be found in the literature, for instance in [43] two varaible resistors are added in each HVDC line in series to the CFC structure in Fig. 2.8(b) in order to have additional degrees of freedom. This represents a combination of the series variable resitor CFC and an interline DC/DC CFC.

ABB filed also two patent applications regarding DC/DC CFCs [44, 45], which consist in a design similar to the one in Fig. 2.8(a). Nevertheless, [45] incorporates an additional H-bridge between the AC transformer and each HVDC line, obtaining an additional DC stage at each side.

MMC-based DC/DC CFC converters

Due to the fact that CFCs are going to be installed in HVDC grids, where the converters terminals are expected be MMCs, it is reasonable to think of CFCs made of MMCs submodules. Several authors suggested CFC converter structures based on submodules that provide easy scalability and modularity to be adapted to different voltage levels at the expense of having more complex structures.

For instance, in [46], two 3-phase MMCs based on full-bridge submodules are connected through the AC side via an AC transformer in a Front-to-Front (F2F) configuration and the DC sides of each MMC are connected to different HVDC lines. The MMCs exchange power through the AC side to

apply series voltages on the lines to regulate the current flows and a scheme of the converter structure can be found in Fig. 2.11(a).

Another proposal of a modular and scalable CFC based on full-bridge submodules is presented in [47] and depicted in Fig. 2.11(b). This converter does not require an isolation transformer and it is made of 5 MMC arms. MMC arms 1 and 2 inject the required DC voltage to perform the current control, while at the same time modulate AC circulating current between them and MMC arm 3 to maintain the balancing of the submodules. MMC arm 3 provides a short-circuit path for the AC current and MMC arms 4 and 5 apply the inverse AC voltage of MMC arms 1 and 2, respectively, in order to avoid the circulation of AC current through the HVDC lines. In [48], the same authors provide a design optimization of the previous CFC topology. The previous CFC device offers a suitable option for high CFC voltage ratings but with some disadvantages for lower voltage ratings due to the semiconductor effort [49].

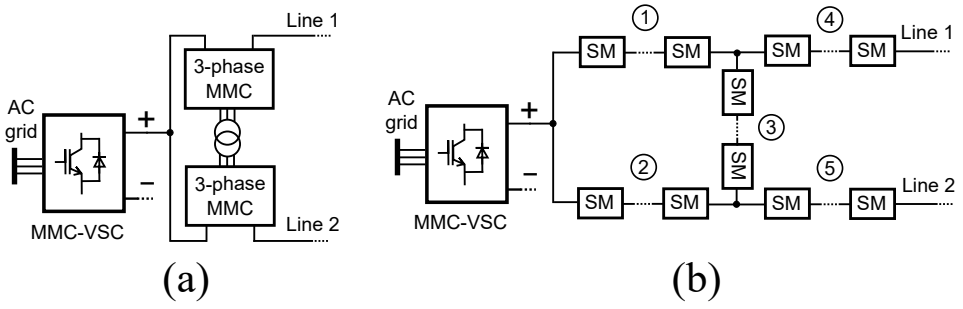

Fig. 2.11: CFCs based on MMC structures. (a) CFC with two 3-phase MMCs in F2F configuration with an isolation transformer. (b) CFC based on 5 MMC arms without AC transformer.

As a result, the authors of the previous modular and scalable CFC device, suggest another more suitable CFC structure for medium CFC voltage ratings [49, 50]. The circuit in [49, 50], is based in CFC cells, each one made of full-bridge units in each HVDC line connected between them through a capacitor and bidirectional switches.

Multi-port DC/DC CFC converters

The majority of the proposed DC/DC or interline CFCs in the literature consider that the device is connected between three different ports: one HVDC node and two HVDC lines, which means that the devices can be

called 3-port CFCs. However, in a highly meshed HVDC grid, the number of possible HVDC lines connected to the same node can be higher than three. As a result, researchers are also considering multi-port CFC structures that can be connected to a generic number n of lines. Some multi-port CFC devices can be found in [46, 51–53]

For example, in [51,52] an extended version of the Dual H-bridge presented in [34] is proposed. For each HVDC line, a H-bridge is added and a single capacitor is connected to each H-bridge (see Fig. 2.11(a)).

Also, an extension of the MMC-based DC/DC CFC topology presented in [46] for a number n of lines is introduced in [54].

A multi-port CFC concept based on MMC arms and called Multi-port polygon-shape is introduced in [53] and also illustrated in Fig. 2.12(b).

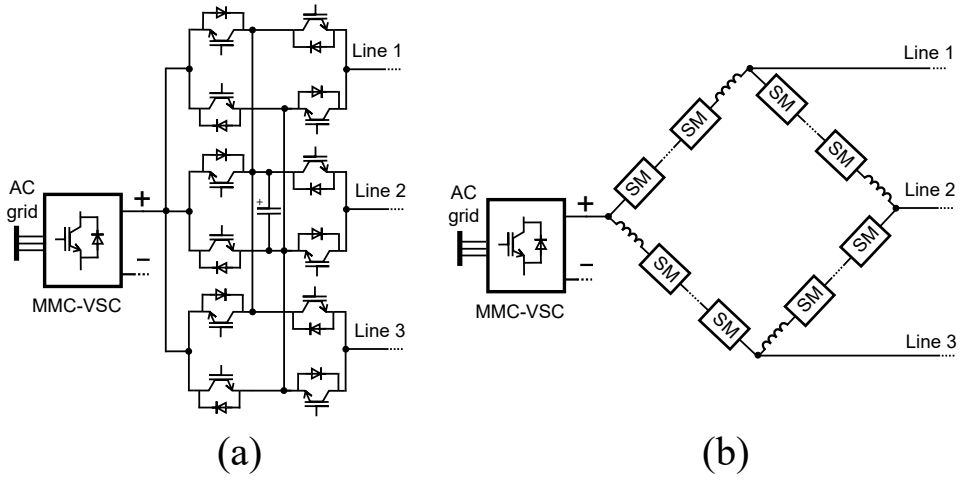

Fig. 2.12: Multi-port CFCs. (a) Multi-port topology of the Dual H-bridge. (b) Multi-port polygon-shape CFC based on MMC arms.

Finally, a multi-port version of the interline DC/DC CFC for unidirectional current flow introduced in [42] is presented and analysed in the Chapter 7 of this thesis.

2.2.4 DC circuit breakers and CFCs

Since series CFCs are installed in series with the lines of the HVDC grids, those devices can eventually be exposed to DC faults. In the literature, some research is being focused on this topic and two different investigation lines can be identified.

The first one consists on suggesting additional equipment or control approaches to ensure that the already installed CFCs in the HVDC grid are able to survive a DC fault. For instance, in [55] the necessary equipment to be added in the Dual H-bridge CFC device [34] and an enhanced control strategy for the CFC are outlined. The work in [39] also considers the Dual H-bridge CFC under DC fault conditions and provides an experimental validation.

The second one consists on proposing devices that are both able to interrupt DC faults and that have current flow control capability. Some research can be found following this approach, for instance, Chapter 4 deals with this topic and also [57, 58]. In Chapter 4 and in [57], the Dual H-bridge [34] is combined with the Hybrid Circuit Breaker (HCB) of ABB [59] obtaining two different outcomes, though both of them present an integrated device that can interrupt DC faults and has current flow control capability. In [58], the HCB is also combined with the interline DC/DC CFC topology introduced in [40], and a device with DC fault interruption and current flow control capability is obtained.

Fig. 2.13 shows the integrated DCCB-CFC design where two HCB in the same node but connected to diffrent lines are combined to achieve CFC capability. The Load Commutation Switch (LCS) of each HCB is rearranged to obtain a dual H-bridge CFC and at the same time maintaining the fault interruption capability. The aforementioned structure is presented in detail in Chapter 4.

2.3 Series-parallel-connected CFCs

The series-parallell-connected CFCs are a combination of both series and parallel-connected devices. One side of the CFC is installed in series with the HVDC lines and the other side is connected in parallel between the two poles of the HVDC system. The advantage of this type of CFCs is that they can control independently the currents of different lines, because the applied series voltage source on one line does not depend directly on the series voltage applied on the other line, as there is a third parallel connection [60]. One drawback is that a converter to withstand the full pole-to-pole HVDC voltage is required as in the parallel-connected CFCs. However, the rating of this converter can be lower, since not all the power of the HVDC system circulates through it.

The concept proposed in [60] uses a Dual Active Bridge (DAB) as a parallel-connected converter and then a extended version of the topology

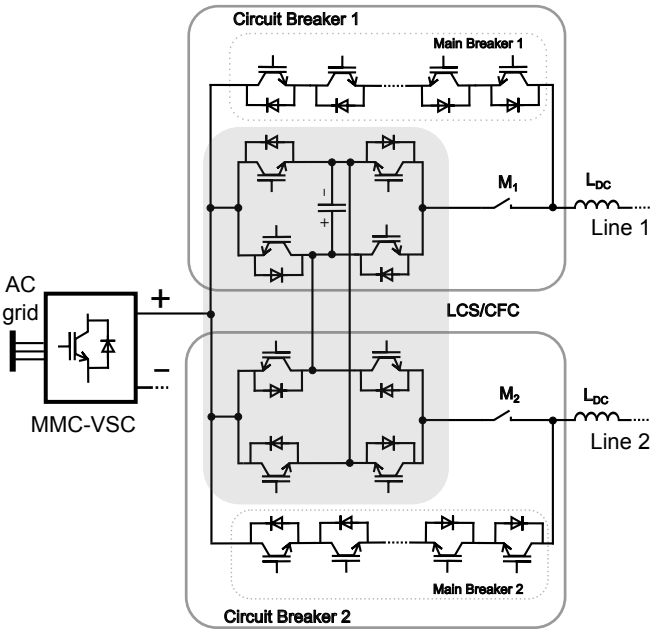

Fig. 2.13: Integrated DCCB with CFC capability.

introduced in [40] is connected in series with two HVDC lines.

In [61, 62], a series-parallel-connected CFC is also suggested and focuses the analysis on the influence of this kind of CFCs in power system studies. Specifically, in [62], a topology is proposed and then, its average model is also obtained and used to perform a small-signal and stability analysis.

Another series-parallel-connected CFC structure can be found in [63], where a DAB is also used as a parallel-connected DC/DC converter.

ABB filed a patent proposing a series-parallel CFCs similar to the thyristor concept in [28], where the AC voltage is obtained from a AC/DC converter connected in parallel with the transmission line [64].

Finally, a concept which can be included in the series-parallel group, though it does not share all of its drawbacks, is the one proposed by ABB in [65, 66]. The CFC is depicted in Fig. 2.14, where a submodule of the MMC at the node is used to generate an AC source via an AC/DC converter connected to the capacitor submodule. The AC source is connected through an AC transformer to another AC/DC converter, which has a series connection with the HVDC line and can apply a variable voltage. The previous CFC structure brings the advantages of a series-parallel CFC concept but it does not require to withstand the pole-to-pole voltage of the HVDC

system. Nonetheless, this type of CFC must guarantee the proper balancing and operation of the MMC when current flow control capability is used.

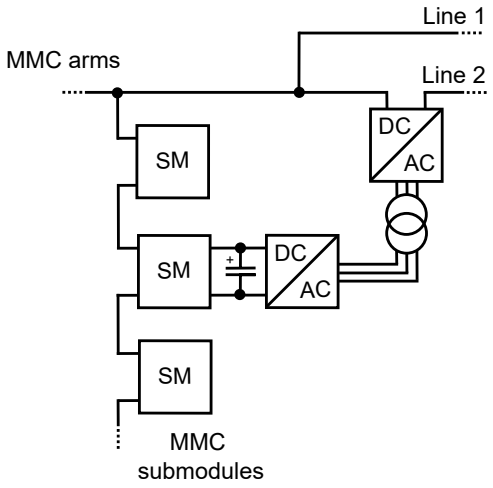

Fig. 2.14: Series-parallel CFC connected to the MMC submodules.

2.4 Conclusions

Parallel-connected CFCs are a reasonable option when they are already required to adapt the voltage between two different HVDC systems. If not, series and series-parallel concepts provide a more suitable CFC device, since the rating of the converter can be lower. Among them, the series-connected CFCs also withstand lower voltages and they are the group with a higher number of proposals in the literature. The last concepts incorporate structures with MMC submodules, which can bring more flexibility at the expense of a more complex structure. Also, multi-port concepts, to be connected to many lines are arising and the combination of DCCB with CFCs has been also suggested in order to have a single integrated device that can interrupt DC faults and that has current flow control capability.

Chapter 3

Modelling and control of an interline current flow controller for meshed HVDC grids

3.1 Introduction

This chapter provides the modelling and control of an interline DC/DC CFC for meshed HVDC grids presented in [34]. An average model is derived considering all possible operation states of the converter and it is used to analyse the steady-state operation and the benefits of introducing a CFC in a 3-terminal meshed HVDC grid. Employing a linearised model of the grid and the CFC, the control of the CFC is designed and the system performance is tested using dynamic simulations in Matlab Simulink.

3.2 Model derivation

3.2.1 DC grid under study

A 3-terminal meshed grid with 3 nodes is used for the following analysis, which can be seen in Fig. 3.1, however, the work can be applied to any meshed DC grid. Additionally, in Section 3.5 a 5-terminal meshed DC grid is also employed for the dynamic validation of the CFC.

The DC grid in Fig. 3.1 is a symmetrical monopole, but this work considers only one half in order to keep the symmetry using a single CFC device. The CFC is assumed to be located in node 1, though, it could also be placed in node 2 or 3, given its bidirectionality.

3.2.2 CFC under study

The CFC under study is a DC/DC converter connected between two lines. Its operation consists on exchanging power between these lines in order to

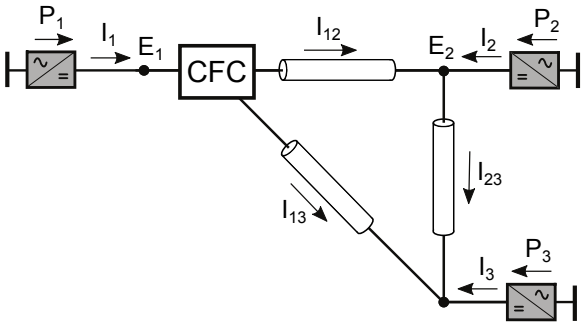

Fig. 3.1: 3-terminal DC grid with CFC located in node 1.

regulate DC currents. It extracts power from one line and it feeds the other, thus, it applies positive voltage on one line and negative voltage on the other one. The converter is made of two H-bridges with 4 IGBTs and their anti-parallel diodes (see Fig. 3.2(a)). For this specific study, a simplified topology, also presented in [34], is used. The two capacitors of the H-bridges are merged into a single one and two IGBTs are removed from the model leading to the converter depicted in Fig. 3.2(b). The CFC has bidirectional capability, it can deal with all possible current configurations: There are 6 possible combinations of currents I_1, I_{12} and I_{13}, each one of them either going in or going out of the converter.

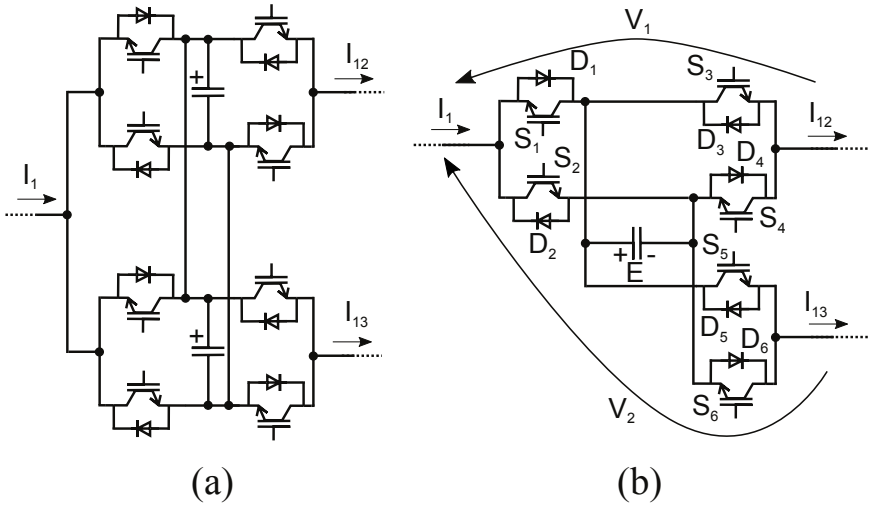

Fig. 3.2: CFC topologies. (a) Dual H-bridge CFC. (b) Simplified dual H-bridge CFC.

The current direction of each branch defines the available switches to operate. For example, if I_1, I_{12} and I_{13} are positive, the devices that are able to conduct given the current direction are: Diodes D_1, D_4 and D_6 and switches S_2, S_3 and S_5. When the switch of one branch is ON, the corresponding diode of the other branch of the H-bridge cannot be conducting as it is reverse-biased since the capacitor voltage is always positive. Therefore, if S_2 is conducting, D_1 is reverse-biased and consequently in open state. Considering this scenario of current flow, the possible states concerning the available switches are summarized in Table 3.1. Value 1 represents the switch in ON state and 0 is the notation when it is in OFF state. The capacitor voltage is represented as E.

Table 3.1: CFC states in positive and negative currents scenarios

Positive currents scenario						Negative currents scenario					
State	S_2	S_3	S_5	V_1	V_2	State	S_1	S_4	S_6	V_1	V_2
a	0	0	0	$-E$	$-E$	i	0	0	0	$+E$	$+E$
b	0	0	1	$-E$	0	j	0	0	1	$+E$	0
c	0	1	0	0	$-E$	k	0	1	0	0	$+E$
d	0	1	1	0	0	l	0	1	1	0	0
e	1	0	0	0	0	m	1	0	0	0	0
f	1	0	1	0	$+E$	n	1	0	1	0	$-E$
g	1	1	0	$+E$	0	o	1	1	0	$-E$	0
h	1	1	1	$+E$	$+E$	p	1	1	1	$-E$	$-E$

Table 3.1 also summarizes the operation states when the currents I_1, I_{12} and I_{13} are negative. In order to exchange power, the important states are those which are not imposing the same voltage to both lines (b, c, f, g) and (j, k, n, o).

The behaviour of the previous converter can be also described considering that it is made of three H-bridge legs, each one able to apply a positive or negative voltage source. This fact does not require taking into account the current directions. Nonetheless, for sake of comparison with other CFC approaches, such as in Chapter 5, the analysis as a function of the current directions is considered.

A possible operation of the considered CFC has been presented in [38] where a duty ratio is applied to several switches. However, the objective of this work is operating the CFC with the minimum required switches.

3.2.3 Operation principle

In this section, the operation principle of the CFC is presented. Two current flow scenarios are considered: The first one assumes that I_1 is entering the CFC and I_{12} and I_{13} are going out. The second one considers the currents in opposite direction compared with the first case. This analysis can be extended to the rest of possible current configurations.

In order to share power within the two lines, the converter capacitor should be charged and discharged continuously. Only 4 states (two pairs) from the group of 8 for each current configuration are used to control the device in such conditions: (b, c, f, g) for positive currents scenario and (j, k, n, o) for negative currents scenario. Those states enable the charge or discharge of the capacitor using only a line current and they are used in pairs of two states in a way that one state charges the capacitor with one line current and the other discharges it with the other line current. One pair limits the current through one line and the other pair increases current through the same line. Both pairs have a positive voltage in the capacitor, however, one pair applies a positive voltage in one line and the other applies a negative voltage in the same line (c with g, b with f). Both pairs can be seen in Fig. 3.3 for each scenario.

The following analysis is performed considering the first scenario with positive currents. It must be noticed that the difference between the two states of the same pair is only the switch S_2. Using the commutation of that switch is possible to increase one line current (I_{12}) and to decrease the other (I_{13}) (Pair A). If the reverse effect wants to be achieved, the procedure should be changing the states of switches S_3 and S_5 and keep operating with S_2, what is equivalent as working with Pair B. Below, the analytical analysis of the converter is performed for the two pairs of states presented before. Then, the conclusions and the average model can be extended to all the current configurations. The duty cycles of switch S_2 for pair A and B are defined as (3.1).

$$D_{s2A} = \frac{t_{s2A}}{T}, \qquad D_{s2B} = \frac{t_{s2B}}{T} \tag{3.1}$$

The average current through the capacitor can be calculated as a function of the line currents and the duty cycles for each pair: (3.2) and (3.3).

$$\begin{aligned} \overline{I}_{cA} &= \frac{1}{T}\int_0^T i_{cA}dt = \frac{1}{T}(-I_{12}t_{s2A} + I_{13}(T - t_{s2A})) \\ &= -I_{12}D_{s2A} + I_{13}(1 - D_{s2A}) \end{aligned} \tag{3.2}$$

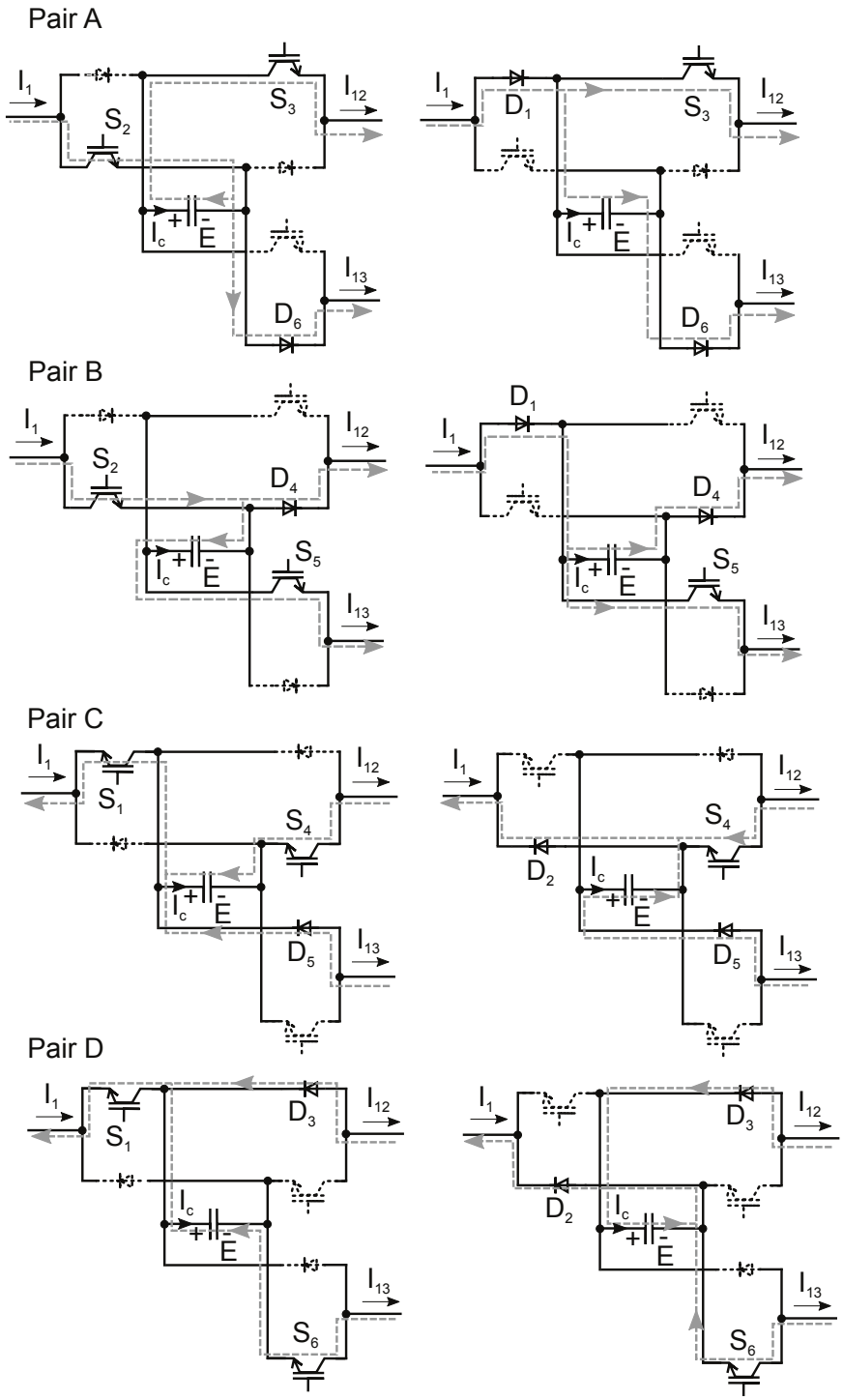

Fig. 3.3: Pairs A, B, C and D.

$$\begin{aligned}\overline{I}_{cB} &= \frac{1}{T}\int_0^T i_{cB}dt = \frac{1}{T}(-I_{13}t_{s2B} + I_{12}(T - t_{s2B})) \\ &= -I_{13}D_{s2B} + I_{12}(1 - D_{s2B})\end{aligned} \tag{3.3}$$

In order to ensure that the average capacitor voltage is constant in steady state, both capacitor currents from equations (3.2), (3.3) must be zero. This fact shows that the duty cycle for each pair is going to be related to the line currents relation. The relation derived from equations (3.2) and (3.3) it is shown in expression (3.4).

$$D_{s2A} = \frac{I_{13}}{I_{12} + I_{13}} = \frac{I_{13}}{I_1}, \quad D_{s2B} = \frac{I_{12}}{I_{12} + I_{13}} = \frac{I_{12}}{I_1} \tag{3.4}$$

In order to gather both duty cycles in the whole average model, a new one is defined as a relation between DC currents (3.5).

$$D = \frac{I_{12}}{I_1} = D_{s2B} = (1 - D_{s2A}) \tag{3.5}$$

The average voltages applied by the CFC with I_1, I_{12} and I_{13} positive are (3.6), and (3.7) working with pair A.

$$\overline{V}_{1A} = \frac{1}{T}\int_0^T v_{1A}dt = \frac{1}{T}(\overline{E}t_{s2A}) = D_{s2A}\overline{E} = (1 - D)\overline{E} \tag{3.6}$$

$$\begin{aligned}\overline{V}_{2A} &= \frac{1}{T}\int_0^T v_{2A}dt = \frac{1}{T}(-\overline{E}(T - t_{s2A})) \\ &= -(1 - D_{s2A})\overline{E} = -D\overline{E}\end{aligned} \tag{3.7}$$

And (3.8) and (3.9) working with B.

$$\begin{aligned}\overline{V}_{1B} &= \frac{1}{T}\int_0^T v_{1A}dt = \frac{1}{T}(-(T - t_{s2B})\overline{E} \\ &= -(1 - D_{s2B})\overline{E} = -(1 - D)\overline{E}\end{aligned} \tag{3.8}$$

$$\overline{V}_{2B} = \frac{1}{T}\int_0^T v_{2B}dt = \frac{1}{T}(t_{s2A}\overline{E}) = D_{s2B}\overline{E} = D\overline{E} \tag{3.9}$$

The same analysis can be done considering currents I_1, I_{12} and I_{13} negative. In that scenario, the available switches and diodes to conduct are: S_1, S_4, S_6, D_2, D_3 and D_5. The difference between the two states of the same pair is also the switch state that gathers all the current from two lines, S_1. The voltage applied on each line is positive or negative depending on the state

of switches S_4 and S_6.

In order to exemplify the operation of the CFC, Fig. 3.4 shows the operation principle working with pair A. The variables E, I_c, V_1 and V_2 are depicted considering constant line currents ($I_{12} = 1.5$ kA and $I_{13} = 0.7$ kA).

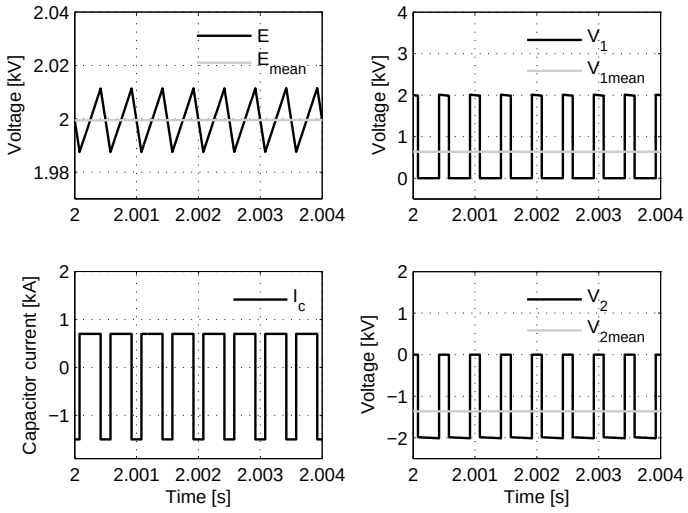

Fig. 3.4: E, I_c, V_1 and V_2 working with pair A.

From the previous analysis the voltage ripple can be deduced and it is given by equation (3.10).

$$\Delta E_{ripple} = \frac{I_{12} I_{13}}{fC(I_{12} + I_{13})} \tag{3.10}$$

where ΔE_{ripple} is the voltage ripple of the capacitor, f is the switching frequency of the CFC and C is the CFC capacitance.

3.2.4 CFC average model

In this section an average model for the CFC is derived. The voltages applied by the converter considering pairs A, B, C and D are shown in Table 3.2. Pairs A and B are applying opposite effects on the DC grid and the same happens with C and D, while one increases I_{12}, the other rises the value of I_{13}. It can be noticed that the voltages applied by the CFC have the same expression for both pairs (in both scenarios) with the difference of a sign. E

Table 3.2: CFC voltages applied for each pair of operation states

Pair	$\overline{V}_1$	$\overline{V}_2$
A	$(1-D)\overline{E}$	$-D\overline{E}$
B	$-(1-D)\overline{E}$	$D\overline{E}$
C	$-(1-D)\overline{E}$	$D\overline{E}$
D	$(1-D)\overline{E}$	$-D\overline{E}$

must be always positive because of the inherent functionality of the device, therefore, when deriving an average model for the 4 pairs considered before, a restriction of positive value should be placed on the variable E. However, instead of restricting its value, it is chosen to allow negative values and using the equivalent model of pair A and D. With this consideration, when solving the system equations, E will get a negative value when the opposite effect of pair A or D is expected. The negative value is not a real magnitude, it simply means that the CFC is working with pair B or C and the real average voltage of the capacitor is $|E|$.

Following this procedure, an equivalent model for the considered two current scenarios is obtained. It includes two voltage sources in series with lines, whose average values are $\overline{V}_1$ and $\overline{V}_2$:

$$\overline{V}_1 = (1-D)\overline{E} \qquad \overline{V}_2 = -D\overline{E} \tag{3.11}$$

This model is illustrated in Fig. 3.5, taking into account that the duty cycle is defined as $D = \frac{I_{12}}{I_1}$. This average model for two current flow configurations can be extended for all the possible current combinations (six possibilities) performing the same analysis as before. Then, a new duty cycle (line current relation) to represent each couple of voltage sources must be defined. The global average model for the CFC located in one node capable of operating with all current flow combinations can be made of three couples of voltage sources.

3.3 Steady-state analysis

In this section the influence of the CFC among grid currents is analysed by means of its average model. Therefore, two steady state analysis are conducted: current and voltage variation and operational area analysis. Both

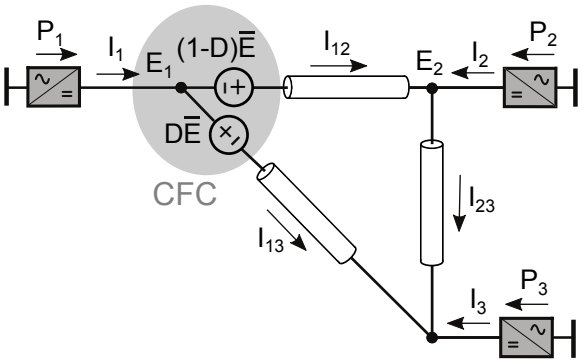

Fig. 3.5: 3-terminal DC grid with a CFC average model in node 1.

analysis consider that the converter in node 1 acts as a slack bus regulating the DC voltage while the other converters in nodes 2 and 3 are operating in constant power mode. The general parameters of the system are listed in Table 3.5. Cable parameters are extracted from [67] for a DC voltage of ±200 kV.

In order to address both analysis, some considerations on system and CFC limitations must be taken into account. Firstly, a maximum current limitation through cables must be considered, which is obtained from [67] and corresponds to 2 kA. The power limitation is derived considering that any converter station can absorb the maximum current from two cables, which leads to a node current limitation of 4 kA and power node limitation of 1600 MW. A DC voltage variation of ±5% is considered for any converter station. Finally, a limitation on the CFC voltage must also be taken into account. Higher voltage allows higher current changes, nonetheless, it also increases the device cost as more IGBT must be connected in series to withstand that voltage. For this work, a value of 4 kV is considered for CFC maximum voltage, in order to be able to build the mentioned CFC with one or two IGBTs in series for each switch.

3.3.1 Current and voltage variation analysis

This analysis performs a duty cycle sweep and the system equations are solved for all its range (0-1). Graphics are plotted about the variables in the system: node and line currents, node voltages, CFC capacitor voltage, node powers and CFC power; all of them as a function of the duty cycle.

The restrictions concerning system variables plotted as horizontal lines are: node current limitation, node voltage limitation and node power limi-

tation. Line current limitation and CFC capacitor voltage are depicted as vertical lines. Vertical and horizontal lines define the operation area of the CFC. Results are exhibited working with two pairs of CFC states (equivalent to the model of a couple of voltage sources).

The powers delivered for terminal 2 and 3 are 400 MW and 800 MW, respectively and the CFC is working with pair C and D. In all of the following graphics horizontal dashed lines set the maximum value of the magnitude which is being plotted. Vertical dotted line shows the current relation in neutral state, when no CFC is operating. Greater duty cycles correspond to states of pair C and lower ones represent states of pair D since different pairs have opposite effects among currents within the DC grid. Vertical dash-dot line illustrates the duty cycle where capacitor voltage is exceeded. When one of the line currents exceeds the maximum rating of the DC cable, a vertical dashed line is used to show that duty cycle. Finally, the possible region of operation is shown in shaded grey area. $D = 0$ means that all current flows through cable 13 and $D = 1$ all current flows through cable 12.

Line and node currents evolution while operating the CFC device are depicted in Fig. 3.6. On the one hand, it can be seen that the CFC has a large impact in the line currents, with few kV, current can be changed in terms of hundreds of amperes. Edge duty cycles are not allowed as line current limits are exceeded and so it is capacitor voltage. For this specific scenario, the most restrictive limitation is the rating of DC cables. On the other hand, node currents suffer small variations compared to line currents.

Node voltages are depicted in Fig. 3.7. E_1 is completely constant since it acts as slack bus, while E_2 and E_3 are slightly higher than the nominal value as they are delivering constant power into the DC grid. The effects of the CFC are small variations in node voltages of a few kV. In this graphic, CFC capacitor voltage is also shown, whose real voltage is being plotted, equivalent to the absolute value of the variable E in the average model implemented. The line current limit is exceeded before reaching the maximum voltage value.

Fig. 3.8 shows the total power extracted or injected in each node terminal and the CFC power. Powers from node 2 and node 3 are constant, 400 MW and 800 MW, respectively. Regarding power extracted by node 1, there is a small variation due to the DC grid losses (losses from the converters or CFC are not considered). The point where losses are the lowest is the duty cycle in neutral state (see dotted line), equivalent to have no CFC in the DC grid. For this duty cycle, the power extraction of node 1 has the maximum value. The power of the CFC starts to increase when rising the voltage, however, for edge duty cycles the current through one of the lines becomes very small

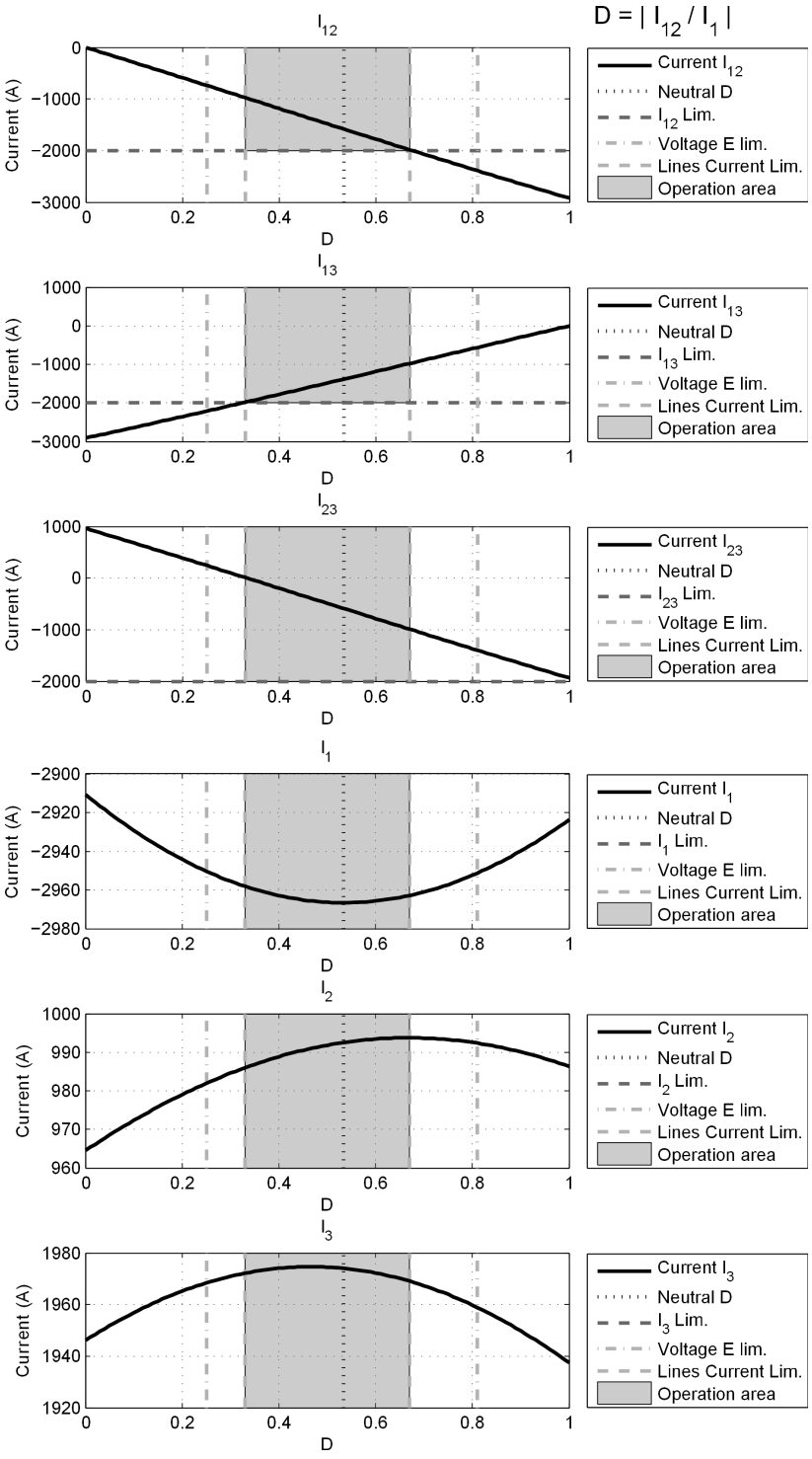

Fig. 3.6: Line and node currents.

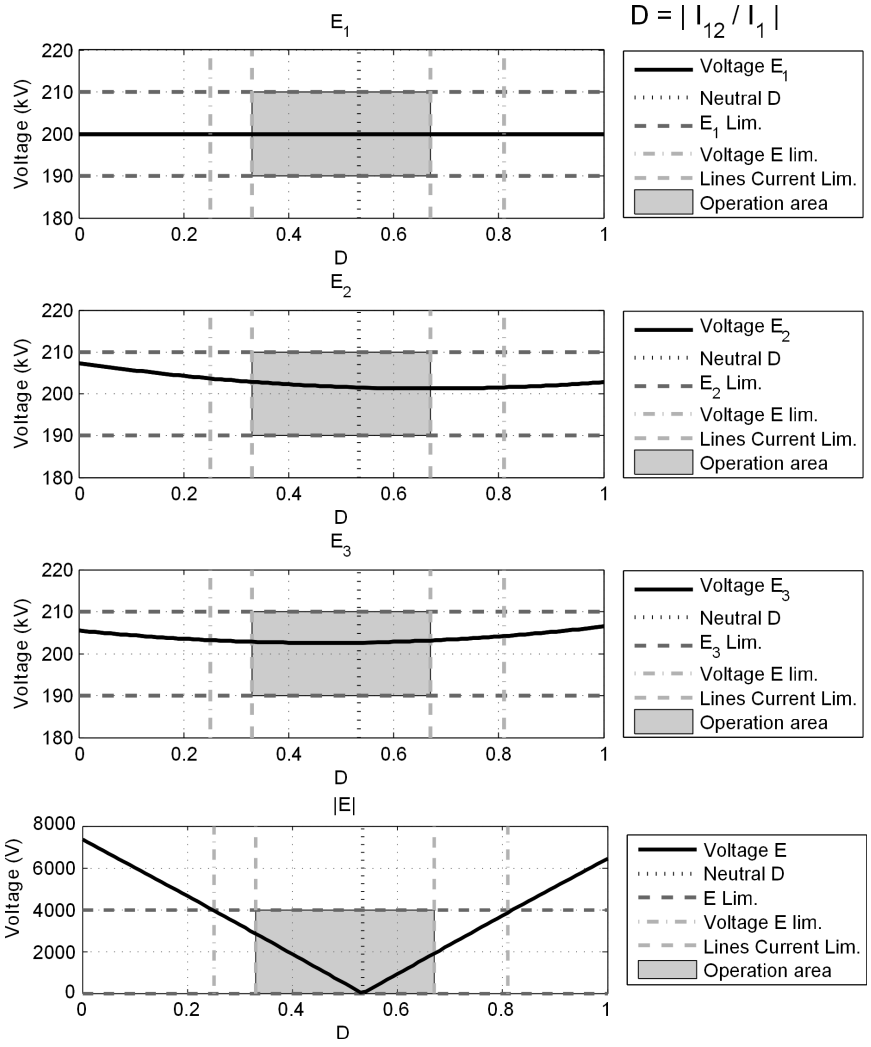

Fig. 3.7: Node voltages and CFC capacitor voltage.

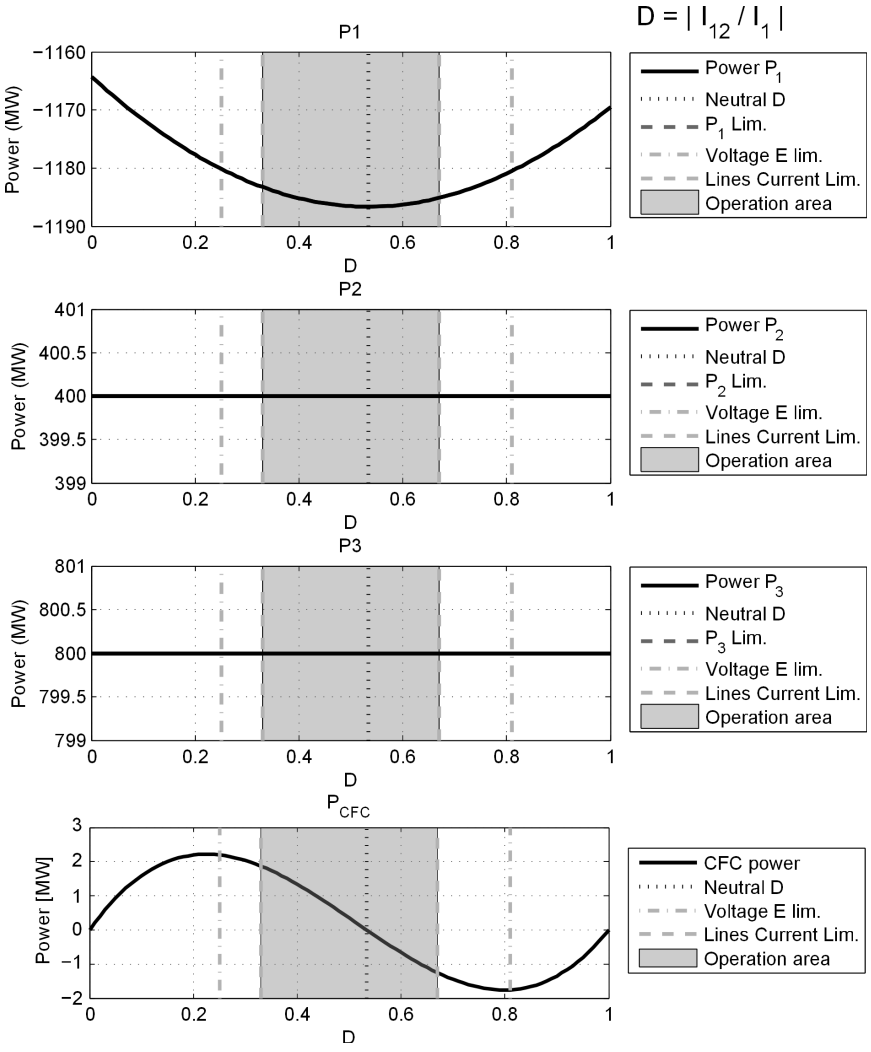

Fig. 3.8: Node powers and CFC power.

and the power is reduced.

3.3.2 Operational area analysis

In this section the system is analysed in terms of its operational area. A power sweep for both power of node 2 (P_2) and node 3 (P_3) is carried out. For each couple of power values, the equations of the system are solved and the solution is depicted in Fig. 3.9 with different colours depending on the limitations that are exceeded.

Horizontal axis of Fig. 3.9 shows the power of node 2 and vertical axis shows the power of node 3. If line currents are below the limitations, the CFC is not necessary to keep the system under the operation limits and this region where the CFC is not needed is depicted with light grey colour. The border of this region is given by black lines, which show the line current that is exceeded.

The main application of the CFC is to drive part of the current through other lines that are not overloaded. If one of the line currents is exceeded, the equation system is solved again introducing the equations of the CFC for any of the 6 possible current configurations. If the CFC is able to reduce the current through the overloaded line, the points are depicted in different tones of grey. The different tones indicate the average voltage of the CFC that is required to produce such effect in the DC grid. The darker the grey is, the higher the required voltage of the CFC. As mentioned before, the maximum voltage for the CFC is set at 4 kV, however, several maximum values of voltage are also depicted in order to show its effect. The higher the voltage limitation, the higher the enlargement of the operation area. Several CFC maximum voltages with its associated increase of the operation area are listed in table Table 3.3. It is interesting to note that for a certain maximum voltage, there is no improvement of the operation area because the limitation on node currents is exceeded. In this case of study, the node current limitation, which is equivalent to the power limitation of the converter stations, sets the maximum possible operation area of the system. This fact is according with the CFC specifications, as if the power of one station is exceeded, the CFC has no capability to solve the problem even if CFC maximum voltage is increased.

There are two regions in the upper-left side and lower-right side that deserve some consideration. They are named No-Possible-Operation (NPO). In those points, nearly all power flow goes through line I_{23}, but the CFC is located between line 12 and 13. In this case node 1, practically does not absorb or inject power, $I_1 \approx 0$. It means that a small amount of current

goes through the device, which implies that its capability to apply voltages and affect currents is drastically reduced. It is an important limitation to bear in mind when choosing the location of the CFC device in the DC grid.

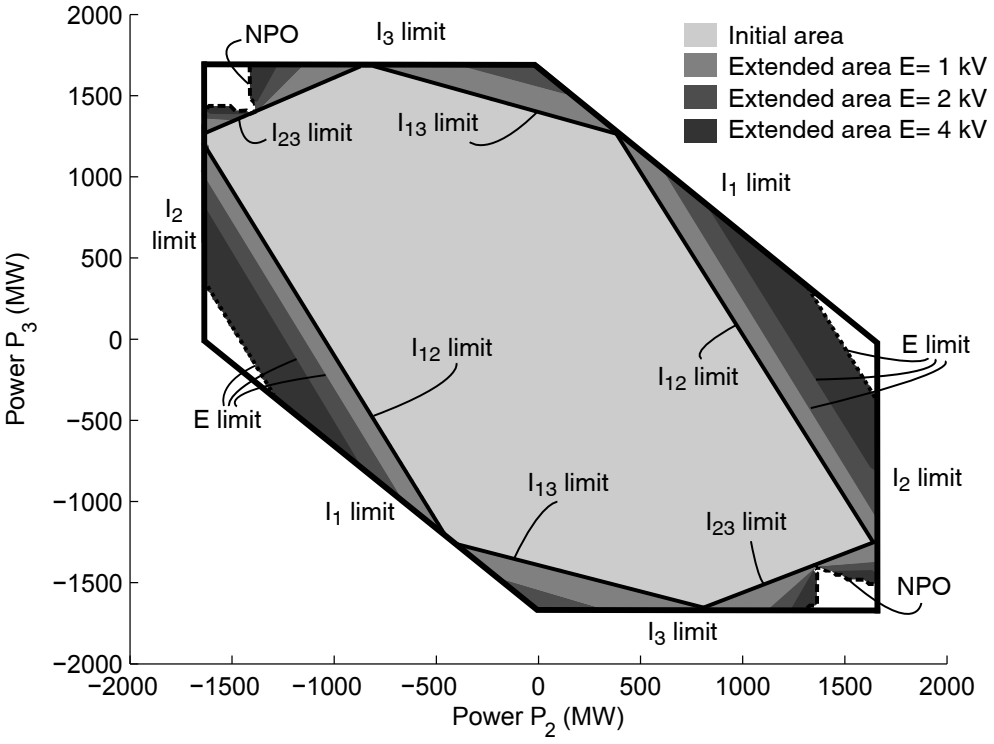

Fig. 3.9: Operation area.

3.4 Control design of the current controller

In this section the state-space representation of the meshed HVDC grid and the CFC is obtained, also the procedure to obtain a linear model of the HVDC grid and the CFC is detailed. After analysing its stability, the linearised model is used to design the current controller of the CFC.

The whole system is clearly non-linear due to the duty cycle relation imposed by the CFC. Only the DC part of the system is considered for control design and it is depicted in Fig. 3.10. Cables are modelled as T-

Table 3.3: Operational area increase for different maximum CFC voltages

Maximum voltage E [kV]	1	2	3	4	5	6
Operational area increase (%)	14	23	29	32	34	34

equivalent in simulations, nevertheless, the cable capacitance is neglected to derive the linearised model due to its reduced value. The DC parts of each VSC are modelled by means of its average model and the capacitor at each node is the power converter capacitance.

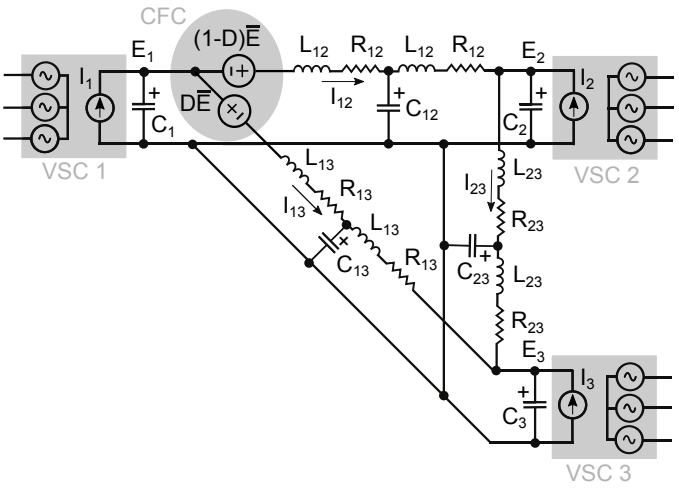

Fig. 3.10: 3-terminal HVDC grid system model.

The model is linearised as [68]:

$$X \approx X_0 + \Delta X \tag{3.12}$$

where X is a general variable, X_0 is its linearisation point and ΔX is the increment over the linearisation point.

Terminal 1 is considered to be operating as a constant power injection node (3.13).

$$I_1 = \frac{P_1}{E_1} \tag{3.13}$$

where P_1 is the power injected into the DC grid, E_1 is the measured DC voltage and I_1 is the DC current. Node 2 and 3 are performing *droop* voltage

control [69]. The equations describing its behaviour are:

$$I_2 = k_2(E_2^* - E_2), \quad I_3 = k_3(E_3^* - E_3) \tag{3.14}$$

where, I_2 and I_3 are the node currents, E_2 and E_3 are the measured DC voltages, E_2^* and E_3^* are the voltage references and k_2 and k_3 are the *droop* constants.

The equations describing model of the HVDC grid with the CFC that are used to derive the linearised model are (3.15)-(3.21):

$$\frac{dE_1}{dt} = \frac{1}{C_1}(\frac{P_1}{E_1} - I_{12} - I_{13}) \tag{3.15}$$

$$\frac{dE_2}{dt} = \frac{1}{C_2}(k_2(E_2^* - E_2) + I_{12} - I_{23}) \tag{3.16}$$

$$\frac{dE_3}{dt} = \frac{1}{C_3}(k_3(E_3^* - E_3) + I_{13} + I_{23}) \tag{3.17}$$

$$\frac{dI_{12}}{dt} = \frac{1}{2L_{12}}(E_1 - E_2 - 2R_{12}I_{12} + (1-D)E) \tag{3.18}$$

$$\frac{dI_{13}}{dt} = \frac{1}{2L_{13}}(E_1 - E_3 - 2R_{13}I_{13} - DE) \tag{3.19}$$

$$\frac{dI_{23}}{dt} = \frac{1}{2L_{23}}(E_2 - E_3 - 2R_{23}I_{23}) \tag{3.20}$$

$$\frac{dE}{dt} = \frac{1}{C}(-(1-D)I_{12} + DI_{13}) \tag{3.21}$$

where, E_i is the DC voltage of node i, I_i is the current of node i, I_{ij} is the current from node i to j, L_{ij} is half of the cable inductance from node i to j, R_{ij} is half of the cable resistance from node i to j, C_i is the power converter capacitance at node, C is the CFC capacitance, E is the CFC voltage and D is the duty cycle of the CFC.

The voltages in series applied by the CFC are included in (3.18) and (3.19). The dynamics during the charging and discharging of the CFC capacitor along with the relation between the duty cycle and the line currents relation is provided by (3.21).

Then, the differential equations describing the linearised HVDC grid with the CFC are (3.22)-(3.28):

$$\frac{d\Delta E_1}{dt} = \frac{1}{C_1}(\frac{\Delta P_1}{E_{10}} - \frac{\Delta E_1 P_{10}}{E_{10}^2} - \Delta I_{12} - \Delta I_{13}) \tag{3.22}$$

$$\frac{d\Delta E_2}{dt} = \frac{1}{C_2}(-k_2\Delta E_2 + \Delta I_{12} - \Delta I_{23}) \tag{3.23}$$

$$\frac{d\Delta E_3}{dt} = \frac{1}{C_3}(-k_3\Delta E_3 + \Delta I_{13} + \Delta I_{23}) \tag{3.24}$$

$$\frac{d\Delta I_{12}}{dt} = \frac{1}{2L_{12}}(\Delta E_1 - \Delta E_2 - 2R_{12}\Delta I_{12} - (D_0 - 1)\Delta E - E_0\Delta D) \tag{3.25}$$

$$\frac{d\Delta I_{13}}{dt} = \frac{1}{2L_{13}}(\Delta E_1 - \Delta E_3 - 2R_{13}\Delta I_{13} - D_0\Delta E - E_0\Delta D) \tag{3.26}$$

$$\frac{d\Delta I_{23}}{dt} = \frac{1}{2L_{23}}(\Delta E_2 - \Delta E_3 - 2R_{23}\Delta I_{23}) \tag{3.27}$$

$$\frac{d\Delta E}{dt} = \frac{1}{C}((D_0 - 1)\Delta I_{12} + D_0\Delta I_{13} + (I_{120} + I_{130})\Delta D) \tag{3.28}$$

where, P_{10}, E_{10} are the power and voltage of node 1 in the linearisation point; I_{120} and I_{130} are the currents circulating through lines 12 and 13 in the linearisation point; D_0, E_0 are the duty cycle and voltage of the CFC in the linearisation point.

Afterwards, the linearised state-space representation of the DC grid is described (3.29).

$$\frac{d\Delta x}{dt} = \mathbf{A}\Delta x + \mathbf{B}\Delta u \tag{3.29}$$

where, $\mathbf{A}$ and $\mathbf{B}$ are:

$$\mathbf{A} = \begin{pmatrix} -\frac{P_{10}}{C_1E_{10}^2} & 0 & 0 & -\frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & -\frac{k_2}{C_2} & 0 & \frac{1}{C_2} & 0 & -\frac{1}{C_2} & 0 \\ 0 & 0 & -\frac{k_3}{C_3} & 0 & \frac{1}{C_3} & \frac{1}{C_3} & 0 \\ \frac{1}{2L_{12}} & -\frac{1}{2L_{12}} & 0 & -\frac{R_{12}}{L_{12}} & 0 & 0 & \frac{1-D_0}{2L_{12}} \\ \frac{1}{2L_{13}} & 0 & -\frac{1}{2L_{13}} & 0 & -\frac{R_{13}}{L_{13}} & 0 & \frac{-D_0}{2L_{13}} \\ 0 & \frac{1}{2L_{23}} & -\frac{1}{2L_{23}} & 0 & 0 & -\frac{R_{23}}{L_{23}} & 0 \\ 0 & 0 & 0 & \frac{D_0-1}{C} & \frac{D_0}{C} & 0 & 0 \end{pmatrix} \tag{3.30}$$

$$\mathbf{B} = \begin{pmatrix} \frac{1}{C_1E_{10}} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -\frac{E}{2L_{12}} \\ 0 & -\frac{E}{2L_{13}} \\ 0 & 0 \\ 0 & \frac{I_{120}+I_{130}}{C} \end{pmatrix} \tag{3.31}$$

and Δx is the linearised state vector and Δu i the input vector, (3.32) and (3.33) respectively.

$$\Delta x = (\Delta E_1,\ \Delta E_2,\ \Delta E_3,\ \Delta I_{12},\ \Delta I_{13},\ \Delta I_{23},\ \Delta E) \tag{3.32}$$

$$\Delta u = (\Delta P_1,\ \Delta D) \tag{3.33}$$

A linearised model gives similar results to the detailed model when the system is working close the linearisation point. If the point where the system works is far from the linearisation point, the two models may diverge. The control strategy is presented for the linearisation point of pair B. Though, the same methodology is also applied for the linearisation point of pair A. Based on the linearised state space, a transfer function $G(s)$ relating the duty cycle of the converter D and the current I_{12} is obtained. The frequency response of this transfer function is depicted in Fig. 3.11 showing different gain peaks that must be taken into account in the controller design stage, which are the consequence of the resonances between the inductance of the cables and capacitance of nodes.

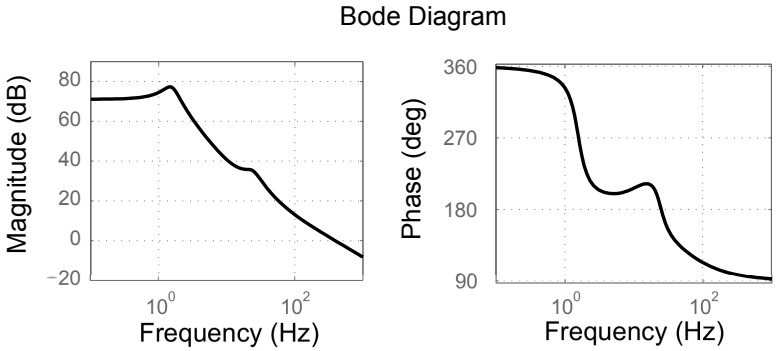

Fig. 3.11: Bode diagram representation of the open-loop transfer function $G(s)$

Initially, two control structures are considered: a single PI and a PI controller in series with a Second Order Compensator (SOC) to damp the system oscillations. Both controllers are:

$$K_{PI}(s) = \frac{k_p s + k_i}{s} \qquad K_C(s) = k_c \frac{(s+z_1)(s+z_2)}{(s+p_1)(s+p_2)} \tag{3.34}$$

where, $K_{PI}(s)$ and $K_C(s)$ are the transfer functions of the PI and the compensator, respectively.

Fig. 3.12 depicts the control scheme with the PI and second order compensator approach.

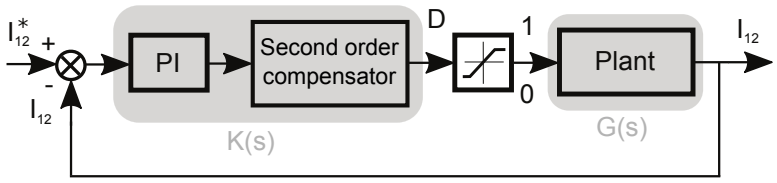

Fig. 3.12: Line current control scheme.

Regarding the closed-loop control, the system time response is set to 150 ms, assuming a first order time response. The desired time response must be at least 10 times slower than the switching frequency of the CFC (0.5 ms) and fast enough to provide a reasonable system response. Then, a combined design of the PI and the compensator is carried out based on a frequency domain analysis. Fig. 3.13 shows the bode diagram representation of both controllers. Having large gain peaks in open-loop (see Fig. 3.11) is not desirable as they can cause oscillatory behaviour in closed loop. The PI controller does not apply gain reduction at the resonance frequencies, thus, a second order compensator in series is used for control design [70].

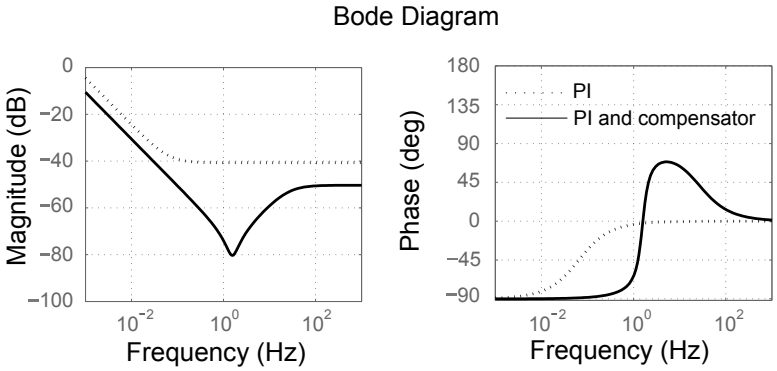

Fig. 3.13: Bode diagram representation of the controller transfer function $K(s)$

Besides, some additional considerations regarding device limits must be taken into account. Considering the previous control scheme, the physical system cannot apply duty cycles higher than 1 or lower than 0. For this reason, the control action must be limited in order to have the output of the controller between these values for any possible current reference, which

implies that the gain at any frequency must be equal or lower that the gain a 0 Hz. The transfer function that relates the control action with the input reference is $KS(s)$, where $S(s)$ is the sensibility transfer function and $K(s)$ is the transfer function of the controller (3.35).

$$KS(s) = S(s)K(s) = \frac{K(s)}{1 + G(s)K(s)} \tag{3.35}$$

Fig. 3.14 depicts the frequency response of $KS(s)$ for different controller options. Considering a PI or a PI and compensator it is not possible to achieve a gain at any frequency equal or lower than the gain at 0 Hz. Therefore, a Low Pass (LP) filter is included in series with the PI and the compensator in order to damp the gain at high frequencies, which has the structure of (3.36).

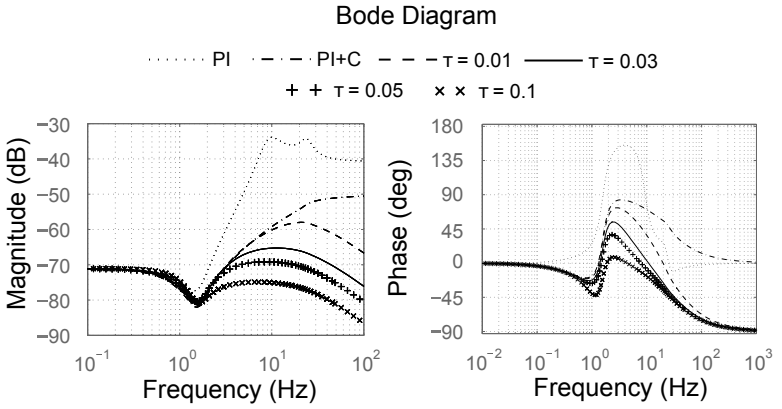

Fig. 3.14: Bode diagram representation of transfer function $KS(s)$

$$K_{LP}(s) = \frac{1}{\tau + 1} \tag{3.36}$$

Fig. 3.14 also shows the frequency response for different time constants τ of the LP filter. The LP filter must be chosen to provide a gain lower than the one at 0 Hz but also to be fast enough not to disturb the time response of the closed-loop system. The time constant of the LP filter is set to $\tau = 0.05$ s because it is the fastest time constant that provides a gain according to the previous requirements.

Fig. 3.15 shows the frequency and time response of the closed-loop transfer function of the system. Three approaches are considered: single PI, PI+compensator and PI+compensator+LP filter. Fig. 3.15(a) shows that the approaches with the compensator are able to damp the gains peaks. All

controllers show 0 dB gain at zero frequency, which means that the control is able to track DC current references. In order to validate the controller, the control system response for a step current reference input I_{12} is represented in Fig. 3.15(b) for all control approaches. The designed controllers are able to track the current reference without steady-state error in the specified time. The system without compensator has large oscillations due to the large peaks in closed-loop response. This fact reveals that the compensator is useful to operate the system with smooth transients. Finally, the designed LP filter allows to operate the system taking into account the device limits and achieving a smooth time response similar to a first order response without overshoot.

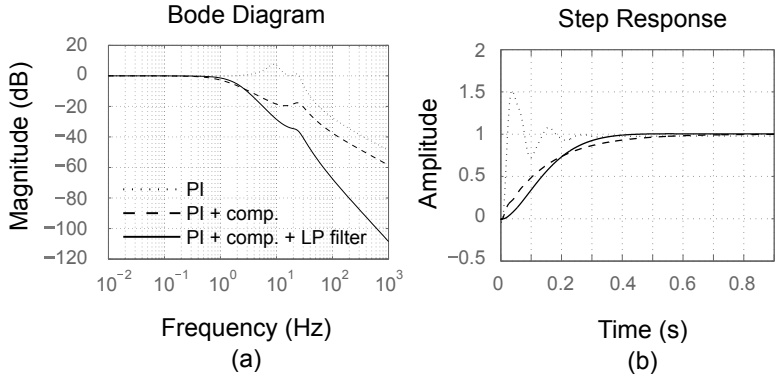

Fig. 3.15: Frequency and time response of the closed loop transfer function

Finally, the stability of the closed loop system is discussed considering the Gain margin and Phase margin with the controller $K(s)$ that includes: PI+compensator+LP filter. Fig. 3.16 shows the frequency response of the transfer function $GK(s)$ and their margins. Both margins are positive, ensuring stability of the system with the designed controller.

The parameters of the controllers are illustrated in Table 3.4 for both pairs (considering that the currents are measured in amperes).

Table 3.4: Controllers parameters

	k_p	k_i	k_c	$z_{1,2}$	p_1	p_2
Pair A	0.0003	0.0023	12.86	$-2.33 \pm j9.49$	-79.89	-8.70
Pair B	0.009	0.0037	0.33	$-2.48 \pm j9.50$	-157.52	-0.41

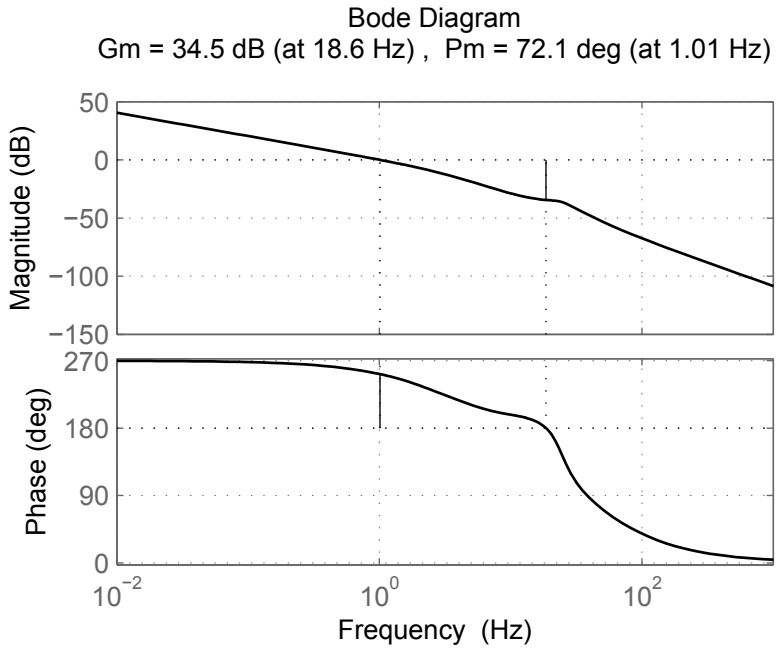

Fig. 3.16: Frequency response of the transfer function $GK(s)$

3.5 Case studies with a current controller

3.5.1 Case studies 1-2: simulation results with a 3-terminal grid

In this section, simulation results for the CFC and the 3-terminal grid are presented. The linearised average model of the CFC, which is represented by a couple of voltage sources is compared with the switching one (composed of 6 IGBTs as shown in Fig. 3.2(b)). Two case studies are addressed, whose parameters are depicted in Tables 3.5 and 3.6.

The black lines of the graphics are the variables of the switching model of the CFC, whereas the grey lines are the variables of the average model that has been linearised.

Case study 1

Case study 1 considers Node 1 delivering 0.875 pu of power into the HVDC grid. As a result, the current through line 12 is exceeding the maximum value. The CFC is used to drive part of this current through another cable allowing the operation of the whole system under such conditions. Fig 3.17 shows the system variables. At instant $t = 0.5$ s, I_{12} is reduced to keep the

Table 3.5: 3-terminal system parameters

DC line parameters			
DC lines	12	13	23
Distance [km]	100	200	200
Resistance [Ω/km]	0.0095		
Inductance [mH/km]	2.111		
Capacitance [µF/km]	2.104		
Conductance [µS/km]	0.062		
Nominal current [kA]	2		
Converter terminal parameters			
Nominal voltage [kV]	± 200		
Nominal power [MW]	1600		
Capacitance [µF]	450		
CFC parameters			
Nominal voltage [kV]	4		
Switching frequency [kHz]	2		
Capacitor [mF]	10		

Table 3.6: Node parameters for Case study 1 and 2

	k_2 [A/V]	k_3 [A/V]	P_1 [MW]	E_2^* [kV]	E_3^* [kV]
Case study 1	0.075	0.05	1400	165	165
Case study 2	0.05	0.05	600	170	170

system operating inside the maximum rating of the cables and the rest of the current goes through cable 13. At instant $t = 2$ s, I_{12} is again reduced to show the capabilities of the device. Node voltages suffer small variations due to the CFC device operation. Simulation results show that the duty cycle is reduced since a portion of current through cable 12 is driven through cable 13. Capacitor voltage is positive, however the voltage applied by the device is negative. Pair B is used for this case study.

Case study 2

Case study 2 considers Node delivering 0.375 pu power. In this case the CFC is used to null the current through one of the line cables. Fig 3.18 depicts the system variables. At instant $t = 0.5$ s, CFC is used to reduce I_{13} to 0 A, which it is equivalent to redirect all the current coming from node 1 through cable 12. At instant $t = 2$ s, the device allows again the current flow through line 13. In this case sutdy, duty cycle increases when I_{13} is reduced. Capacitor voltage and the voltage applied by the CFC are both positive as the device is working with pair A. The voltage of node 1 shows small divergence between the linearised model and the detailed one, the reason is that equation (3.13) is highly non-linear compared to the equations of other nodes, which are performing *droop* voltage control.

3.5.2 Case studies 3-4: simulation results with a 5-terminal grid

In this section, a more complex HVDC grid is considered and the same control methodology of Section 3.4 is applied to a meshed 5-terminal HVDC grid. The state-space model is linearised and the CFC controller is tuned following the same strategy than in Section 3.4. The 5-terminal grid scheme with the CFC in node 1 is depicted in Fig. 3.19 and the grid parameters are illustrated in Table 3.7. The following simulations are performed considering average models for converter terminals and the switching model for the CFC.

Case study 3: power step change

In this Case study, the controlled current is I_{41}. At instant 1 s, a reference change of -200 A is introduced into the controller (see Fig. 3.20) and the system achieves a first order transient response. A power step change of -200 MW is applied in terminal 5, at instant 3 s, while the current reference for I_{41} is kept the same. The system suffers some oscillations after the power change, however, the CFC is able to maintain the current I_{41} to the same

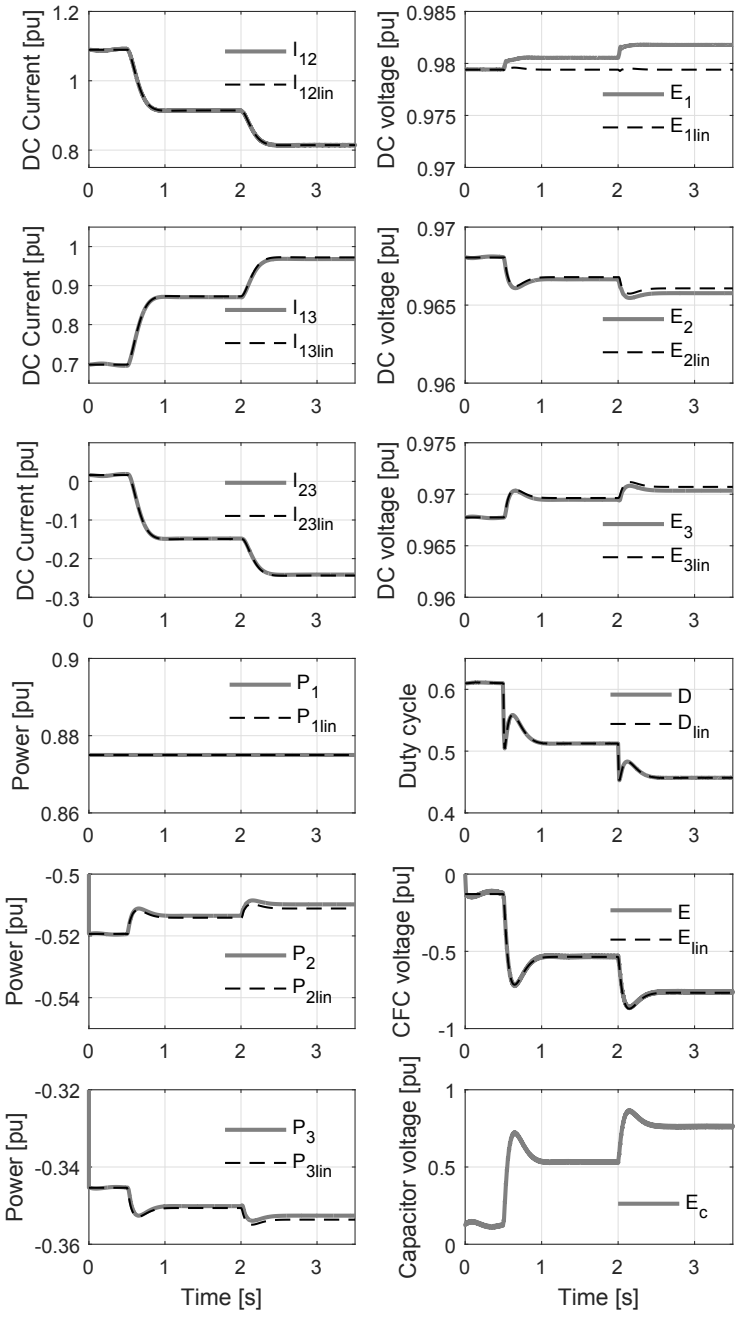

Fig. 3.17: Simulation resuls of Case study 1: Line currents, node voltages, node powers, duty cycle, CFC voltage and capacitor voltage.

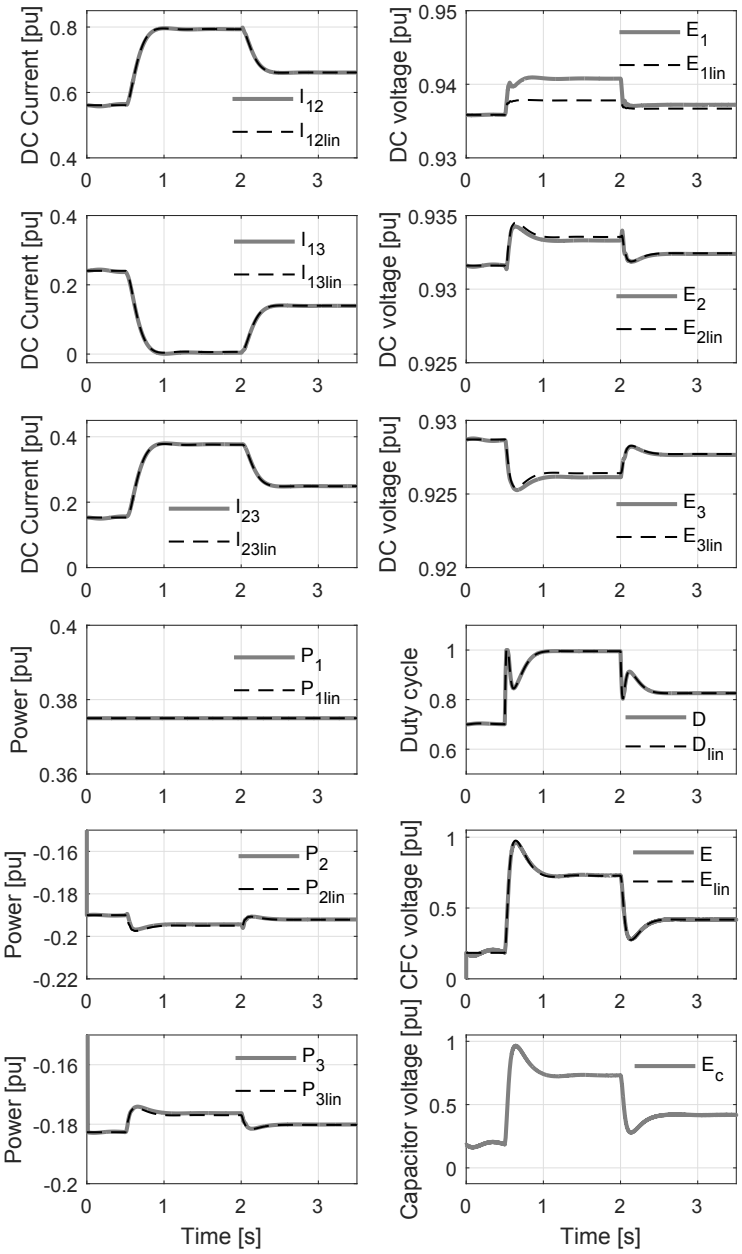

Fig. 3.18: Simulation results of Case study 2: Line currents, node voltages, node powers, duty cycle, CFC voltage and capacitor voltage.

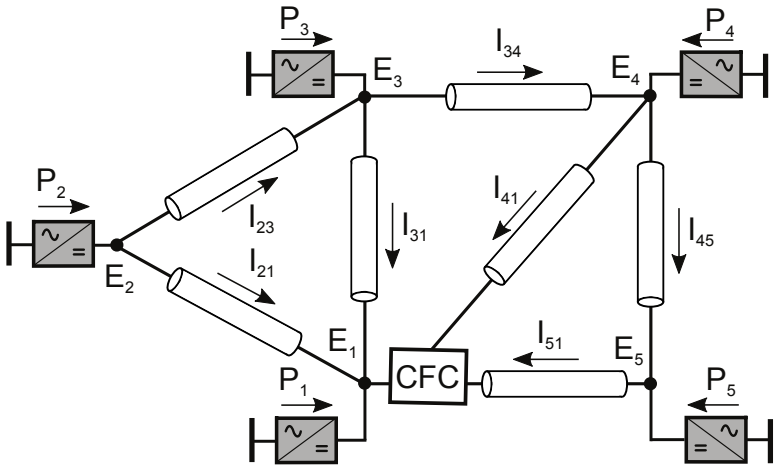

Fig. 3.19: 5-terminal DC grid with the CFC in node 1.

Table 3.7: 5-terminal system parameters

DC cable parameters							
Lines	23	21	31	34	41	45	51
Distance [km]	100	80	120	100	100	120	80
Converter terminal parameters							
Nodes			1	2	3	4	5
Capacitance [µF]			300	300	150	150	450
Power [MW]			-	800	-	-200	-1200
E_i^* [kV]			200	-	200	-	-
Droop constant k_i [A/V]			0.05	-	0.05	-	-

value after a transient of some seconds. The CFC voltage in the capacitor has also some oscillations while trying to maintain the same current through line 41.

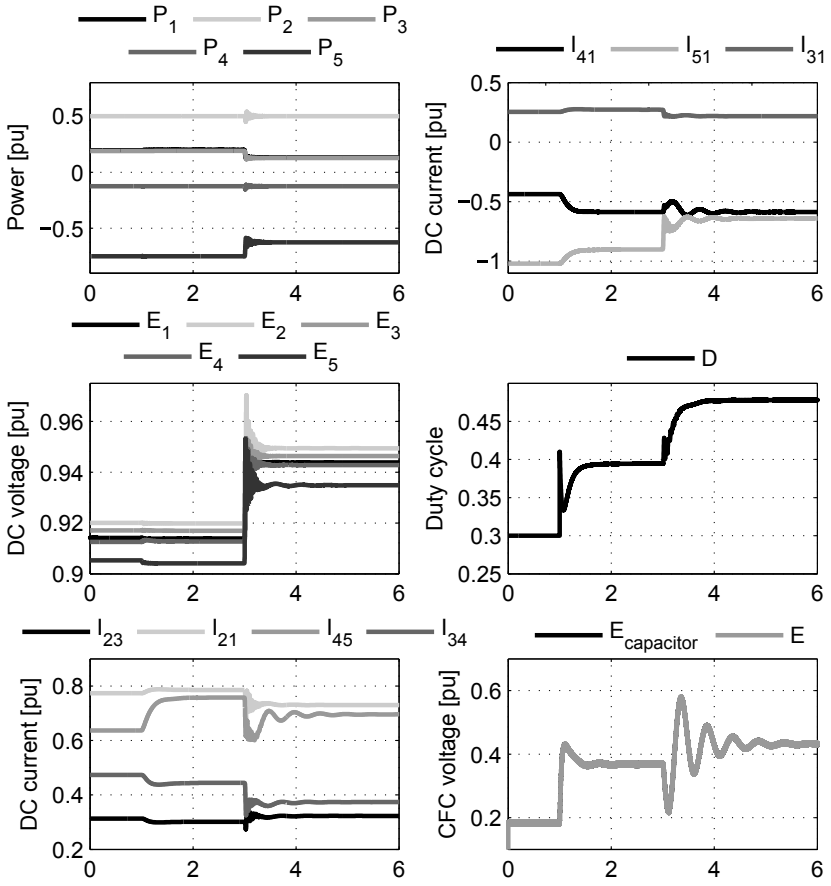

Fig. 3.20: Simulation results of Case study 3: System variables under a power step change.

Case study 4: terminal outage

In Case study 4, the controlled current is also I_{41}. At instant 1 s, a reference change of -700 A is introduced into the controller (see Fig. 3.21). The CFC is able to achieve the desired current with a smooth response. A terminal outage happens in node 2 while the current reference for I_{41} is kept the same. Power of node 2 goes to 0 and the whole system suffers important

oscillations. A few seconds later, the CFC is able to regulate I_{41} to the same level as before. The CFC voltage and duty cycle experiment also transient oscillations due to the converter outage.

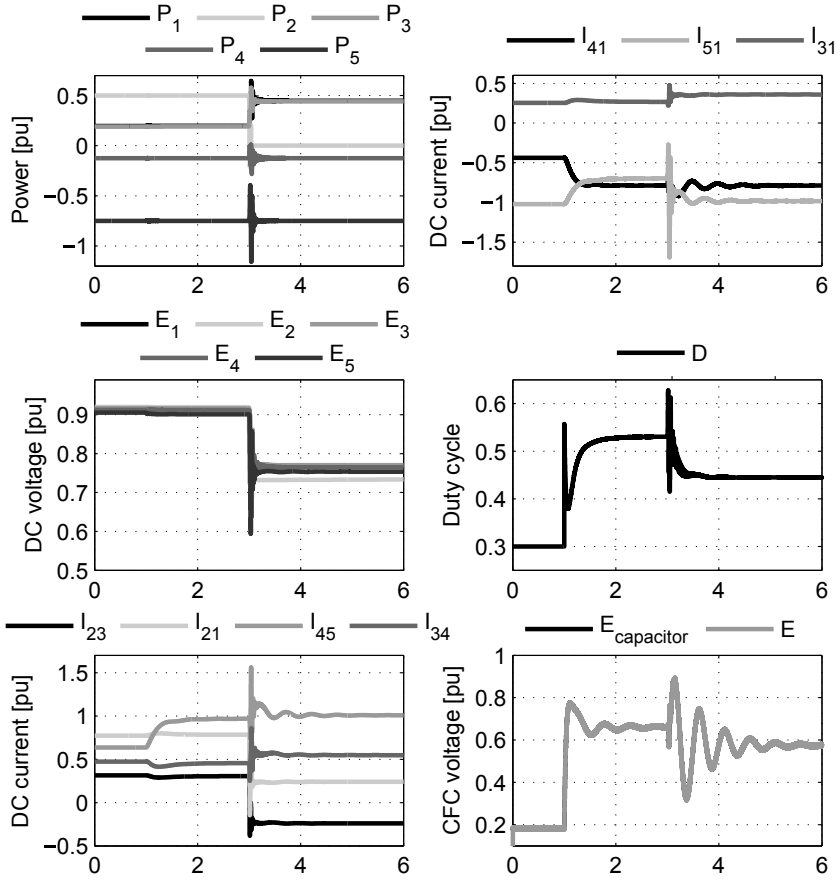

Fig. 3.21: Simulation results of Case study 4: System variables under a converter terminal outage.

3.6 Coordinated control design of the voltage and current controller

An enhanced control design methodology is presented in this section, compared to the one introduced in Section 3.4. In Section 3.4 a current loop is considered to regulate line currents, but the CFC voltage is not controlled.

This issue can lead the voltage of the capacitor to achieve values over its rating and the rating of the switches both during transients and in steady-state. Therefore, a coordinated control design of the CFC voltage loop and the current loop is presented. The voltage controller is designed to be operated independently or as an inner controller. The control scheme is depicted in Fig. 3.22 and the methodology used in this section is applied to the linearised model of the meshed 5-terminal HVDC grid and the CFC as in the previous section.

In Fig. 3.22, the two designed controllers are illustrated, the inner voltage controller $K_v(s)$ and the outer current controller $K_c(s)$. The previous scheme permits to use two independent control methodologies: a direct control of the CFC voltage, when the switch is in the upper position and the reference for the voltage, E^*, is freely chosen but there is no current regulation; or a cascaded control of the line current where the reference for the CFC voltage, E^*, is given by the output of the current controller, so that the switch is in the lower position. This last cascaded methodology permits to have a limitation on the voltage that is being applied.

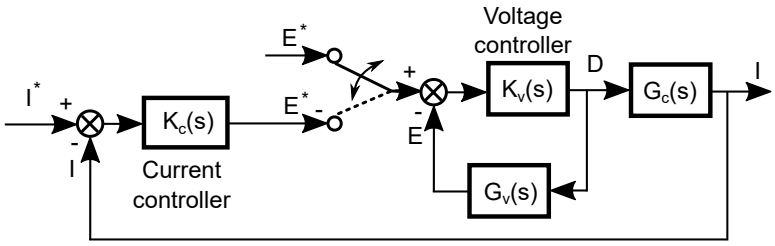

Fig. 3.22: Control scheme with an inner voltage controller and an outer current controller.

The current to be controlled is defined to be I_{41}. The first step consists on designing the inner loop, which it is the voltage loop. Consequently, the transfer function $G_v(s)$ relating the CFC voltage E and the duty cycle D is obtained using the linearised model of the system. The transfer function of the voltage controller $K_v(s)$ is composed of a PI controller and a SOC to damp the system oscillations in closed-loop, as presented in Section 3.4. The transfer function of the voltage controller has the following expression:

$$K_v(s) = \left(\frac{k_{pv}s + k_{iv}}{s}\right)\left(\frac{a_2s^2 + a_1s + a_0}{b_2s^2 + b_1s + b_0}\right) \tag{3.37}$$

$K_v(s)$ is designed to be able to control the voltage independently from the

current loop and to achieve a closed-loop first order response of time constant τ_v without overshoot. Then, an outer controller is added in cascade to regulate the line current I_{41}, whose output or control action is the reference voltage of the CFC, E^*. This outer controller must be slower than the inner voltage controller to avoid interactions between them. A single PI controller for the outer loop is considered for simplicity. It is designed considering the addition of the previous inner controller into the system and (3.38) shows the $K_c(s)$ controller of the current loop.

$$K_c(s) = \left(\frac{k_{pc}s + k_{ic}}{s} \right) \tag{3.38}$$

The tuning goal is obtaining a first order time response, τ_r, as well, without overshoot. The relation between time constants is given by:

$$\tau_c = F\tau_v \tag{3.39}$$

where F is a factor > 1

Before obtaining the final controllers design, there are several considerations regarding system limitations that must be taken into account. Firstly, the inner loop time response must be slower than the switching frequency of the CFC (2 kHz) due to the modulation effect. Secondly, the control action that the CFC is able to apply (duty cycle D) ranges from 0 to 1. Therefore, although the linearised model can impose duty cycles higher than 1, they are not feasible in the real system. For this reason, the control action (D) must be limited between 0 and 1 during transients. In steady-state the D will always be between 0 and 1 as they mean nulling one DC current or the other. Moreover, when considering the two cascaded controllers, the designed first order time response of the inner controller cannot be ensured, as it will be affected by the output of the outer loop, the voltage reference (E^*). In order to tackle these issues, the following transfer functions are obtained from the linearised model. $T_v(s)$ is the closed-loop transfer function of the CFC voltage relating the reference, E^*, with the measured voltage, E. $KS_v(s)$ is the transfer function relating the reference, E^*, with the duty cycle, D. Both expressions are shown below:

$$T_v(s) = \frac{G_v K_v}{1 + G_v K_v} \qquad KS_v(s) = \frac{K_v}{1 + G_v K_v} \tag{3.40}$$

The open loop transfer function that relates the duty cycle, D, with the current reference, I^*, is $G_c(s)$. Then, the closed loop transfer function relating

I^* with the measured current, I, is $T_c(s)$, whose expression is:

$$T_c(s) = K_c T_v G_v^{-1} G_c = \frac{K_c K_v G_c}{1 + G_v K_v} \tag{3.41}$$

The input of the final control system is the current reference, I^*, as the voltage controller is part of the inner loop. In order to perform a proper design, the transfer functions relating I^* with the measured voltage of the CFC ($G_{overshoot}(s)$) and the duty cycle ($G_{action}(s)$) must be obtained. Fig. 3.23 depicts the scheme to obtain these transfer functions.

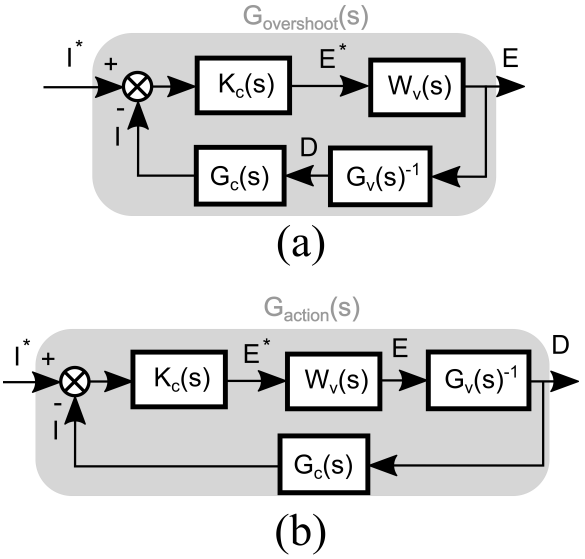

Fig. 3.23: Block diagrams of the transfer functions $G_{overshoot}(s)$ and G_{action}.

$G_{overshoot}(s)$ can be seen in (3.42) and $G_{action}(s)$ is presented in (3.43).

$$G_{overshoot}(s) = \frac{K_c T_v}{1 + \frac{G_c K_c T_v}{G_v}} = \frac{K_c K_v G_v}{1 + K_c K_v G_c + K_v G_v} \tag{3.42}$$

$$G_{action}(s) = \frac{K_c T_v G_v^{-1}}{1 + K_c T_v G_v^{-1} G_c} = \frac{K_c K_v}{1 + K_c K_v G_c + K_v G_v} \tag{3.43}$$

After deriving the previous transfer functions, the effect of using different time constants τ_v and τ_c is analysed. The first value chosen for τ_c is 0.15 ms, the same as the current loop designed in Section 3.4. Then, 0.20 and 0.25 ms are also considered to see the effect of increasing τ_c. For each τ_c, four different τ_v are considered with factors F of: 5, 7, 10 and 15.

Fig. 3.24 and Fig. 3.25 depict the results of this analysis. Figs. 3.24(a), 3.24(c) and 3.24(e) illustrate the frequency response of the closed-loop transfer function $T_c(s)$ and Fig. 3.24(b), 3.24(d) and 3.24(f) depict the frequency response of $G_{action}(s)$ for the τ_v and τ_c presented before. In dashed grey line, the system response of the design considered in Section 3.4 without voltage loop is shown. The rest of the lines depict the behaviour considering different time constants, τ_v, for the voltage loop. It can be seen that the gain of $T_c(s)$ at 0 Hz is 0 dB, which means that is capable of following DC references. The bandwidth of $T_c(s)$ is decreasing if τ_c increases. Regarding the frequency response of $G_{action}(s)$, increasing τ_c, reduces the gain at higher frequencies and the same happens for τ_v. The duty cycle cannot get values higher than in steady-state in order to avoid values lower than 0 and higher than 1, which is only possible in the average model, but not feasible in the detailed model with switches. For this reason, the maximum allowed gain of $G_{action}(s)$ is the steady-state value, which is always around -70 dB. This discards the values considered in Figs. 3.24(a) and 3.24(b) and sets a lower limit for τ_v (0.029 s) considering $\tau_c = 0.2$ ms.

Figs. 3.25(a), 3.25(c) and 3.25(e) show the frequency response of $G_{overshoot}(s)$ and Figs. 3.25(b), 3.25(d) and 3.25(f) depict the unitary time step response of $G_{overshoot}(s)$. For this case, a maximum overshoot of 25% is allowed. According to Figs. 3.25(a), 3.25(c) and 3.25(e), the gain of $G_{overshoot}(s)$ at 0 Hz is 7.32 dB (2.323 V/A) for any time constant. Then, the maximum gain is extended to all frequencies to be more restrictive and can be calculated as:

$$G_{max} = 20log(2.323 + 2.323 \cdot 0.25) = 9.26 \text{ dB} \tag{3.44}$$

The region above this limit is illustrated with a shaded area. It can be seen that all the values considering $\tau_c = 0.15$ ms have a large overshoot in the range of the design addressed in Section 3.4 for any τ_v. With $\tau_c = 0.20$ ms the overshoot is considerably reduced and it is below the limit for values of τ_v lower than 0.029 s. This defines an upper limit for τ_v. Any value of τ_v could be chosen with $\tau_c = 0.25$ s since the overshoot is much lower, however, the time constant of the closed loop function is higher, making current response slower. Therefore, for this analysis the time constants are set to:

$$\tau_c = 0.2 \text{ s} \quad \tau_v = 0.029 \text{ s} \quad F = 7 \tag{3.45}$$

Besides, saturation after the current controller between 0 pu and 1 pu is included in order to limit the voltage references, E^*, that are introduced into the voltage loop. A similar saturation is added after the voltage controller

Table 3.8: Controllers' parameters

Parameter	Symbol	Value
Current controller proportional constant	k_{pc}	2.7807
Current controller integral constant	k_{pc}	11.0301
Voltage controller proportional constant	k_{pv}	0.0127
Voltage controller integral constant	k_{iv}	0.1625
Anti-windup constant	k_{aw}	1.1030
Numerator SOC constant	a_2	0.0094
Numerator SOC constant	a_1	0.0420
Numerator SOC constant	a_0	1.7234
Denominator SOC constant	b_2	1
Denominator SOC constant	b_1	17.5232
Denominator SOC constant	b_0	60.1029

to limit the duty cycle value between 0 and 1.

Finally, an Anti-Windup (AW) scheme is included in the model to avoid windup effects when the voltage reference, E^*, is saturated. The final controllers' parameters are shown in Table 3.8 (considering voltages measured in volts and currents in amperes).

3.7 Case studies with a current controller and voltage controller

3.7.1 Case studies 5-7: simulation results with a 5-terminal grid

In this section, three case studies are considered to validate the proposed control design methodology. Simulations are carried out using the 5-terminal meshed HVDC grid and the switching model of the CFC.

Case study 5: comparison of the linearised and the detailed model

The linearised and the detailed model are compared in this section considering the controllers designed in Section 3.6. Fig. 3.26(a) shows how both systems are following the I_{41} references with a first order time response. The difference between them is negligible, still, it is increasing the further the system goes away from the linearisation point. Fig. 3.26(b) depicts the CFC voltage E required to change the current. It can be seen that both models

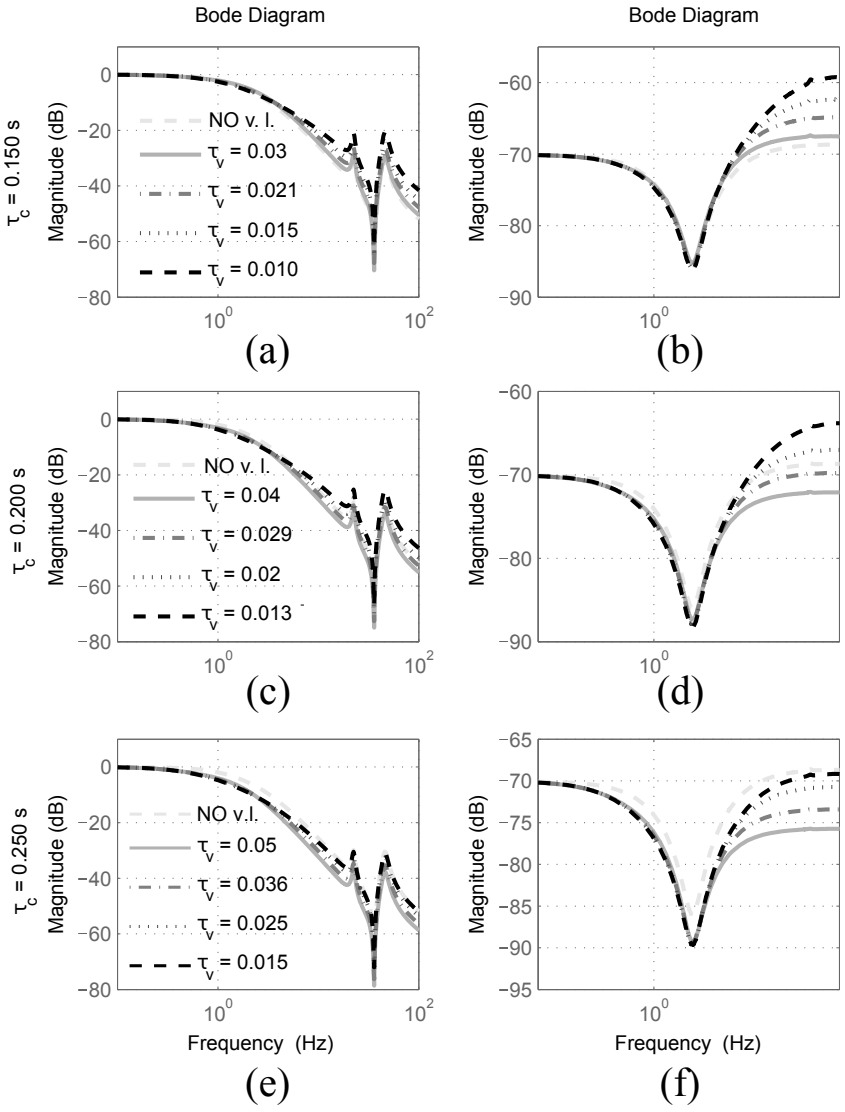

Fig. 3.24: Frequency response of $T_c(s)$ (left column) and $G_{action}(s)$ (right columns) for different τ_c and τ_v.

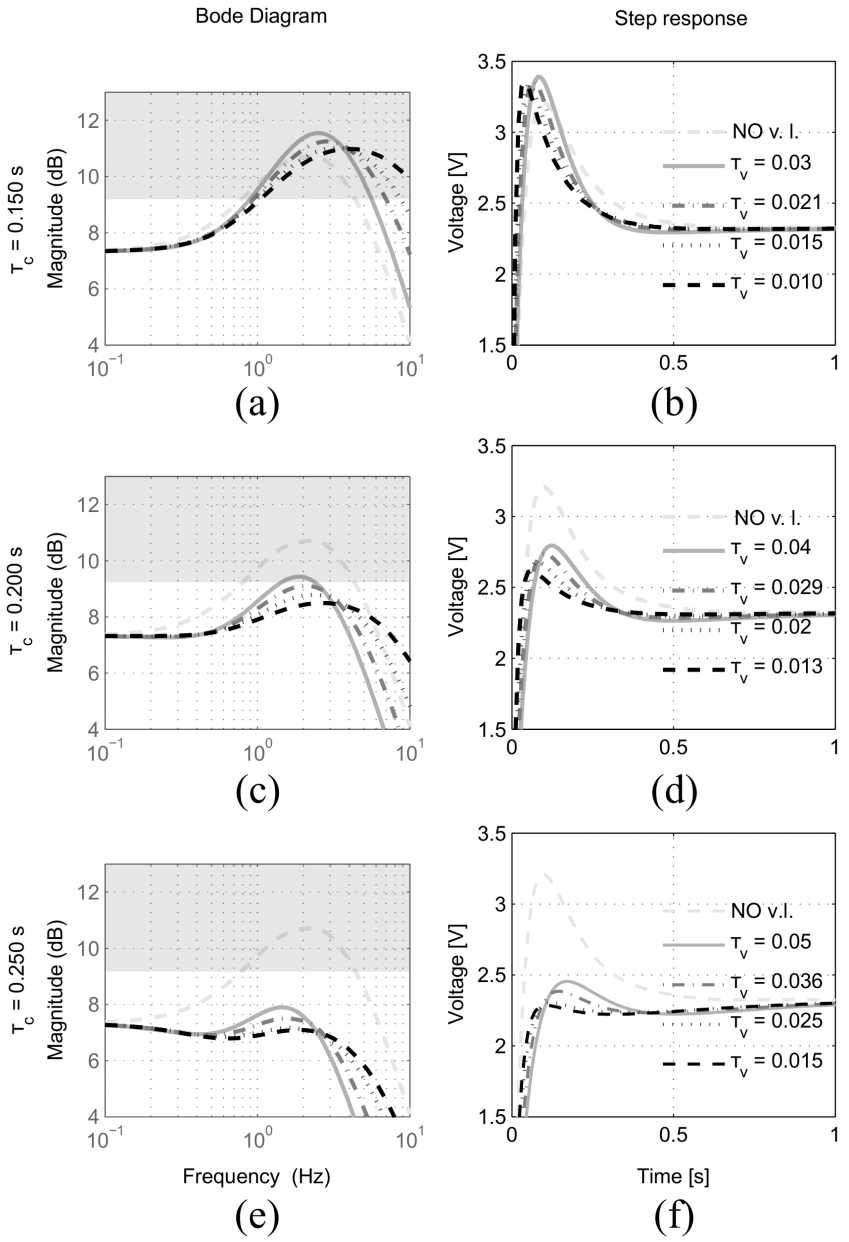

Fig. 3.25: Frequency and time step response of $G_{overshoot}(s)$ for different τ_c and τ_v.

have a reduced overshoot. It is important to notice that when the system is far from the linearisation point, the voltage overshoot is slightly reduced but the steady-state value differs from one model to the other.

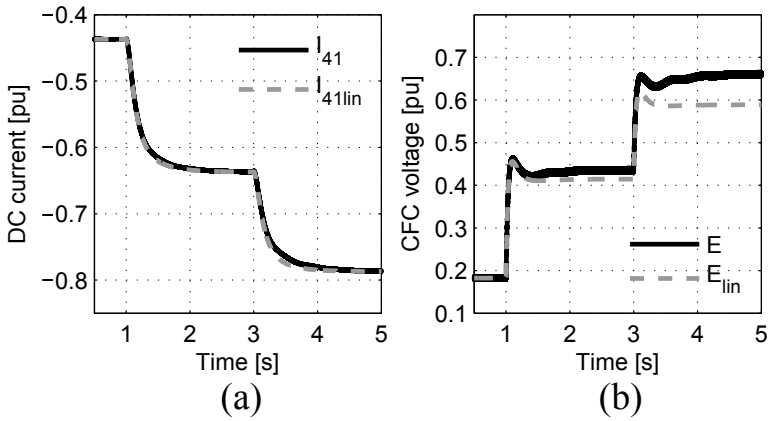

Fig. 3.26: Comparison between the linearised and detailed model. (a) DC current of line 41. (b) CFC voltage.

Case study 6: comparison of different CFC control schemes

In this Section, the control scheme with a single current loop of Section 3.4 and the voltage and current loop approach presented in Section 3.6 are compared. In this case, the detailed model is used and the current reference sent to the CFC implies a CFC voltage higher than the ratings (1 pu).

Fig. 3.27(a) and Fig. 3.27(b) show the current of line 41 and the CFC voltage, respectively, for the different control approaches. The reference for the current control is depicted in dashed grey line ($I_{41}\ ref$). The solid grey line shows the control approach considering only one current loop as in Section 3.4. Finally, the dotted grey line and the solid black line depict the controllers designed in Section 3.6 without and with AW, respectively. The controller presented in Section 3.4 shows a faster time response when following current references. However, the second step implies exceeding the CFC nominal voltage which could damage the CFC device. The CFC voltage gets a value higher than 1.2 pu as it can be seen in Fig. 3.27(b) in grey solid line. The addition of the voltage loop allows to saturate the maximum voltage reference, E^*, that is sent to the voltage controller. Thus, the current reference cannot be followed in this case (see Fig. 3.27(a)) but the voltage is kept at 1 pu (see Fig. 3.27(b)). At instant $t = 6$ s, a new current

reference is received that implies reducing the CFC voltage. Without using the AW scheme, the system has too much error in the integrator, leading to a slower response. The addition of the anti-windup allows having a faster response as it can be seen in Fig. 3.27(b) with the black solid line.

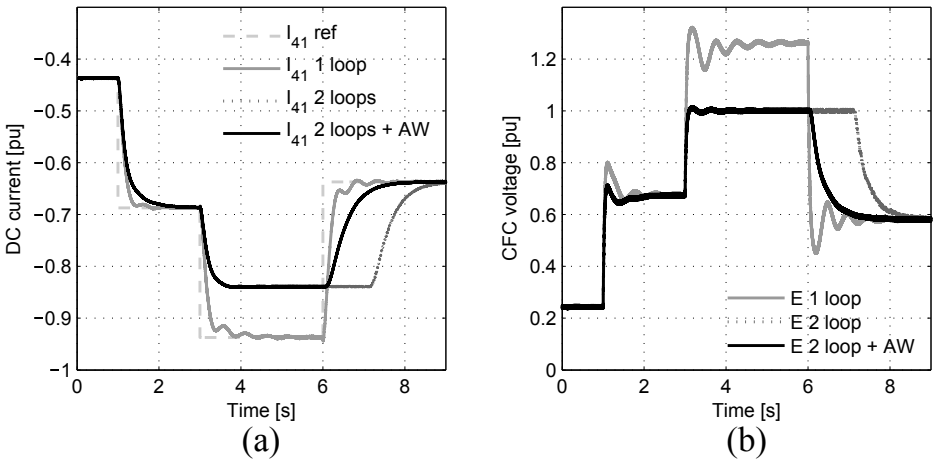

Fig. 3.27: Comparison between different CFC control schemes. (a) DC current of line 41. (b) CFC voltage.

Case study 7: VSC terminal outage

In this Section, the behaviour of the designed controllers for the CFC is tested when there is an outage in a VSC terminal. The detailed model is considered and the VSC 2 suffers the terminal outage and it is disconnected from the HVDC grid.

Fig. 3.28 shows the variables of the system during the VSC outage. The node powers and node voltages are illustrated in Figs. 3.28(a) and 3.28(c), respectively. DC line currents are depicted in Fig. 3.28(b) and 3.28(e). The duty cycle and voltage of the CFC are illustrated in Figs. 3.28(d) and 3.28(f), respectively.

At instant $t = 1$ s, in Fig. 3.28(b), the CFC increases the current through I_{41} and reduces current I_{51} that is near the maximum rating (1 pu). In Fig. 3.28(d), it is shown that the duty cycle suffers a transient peak with the same gain than the steady-state value, as designed in Section 3.6. Fig. 3.28(f) depicts a small overshoot in the CFC voltage. At instant $t = 3$ s, VSC 2 suffers an outage and it is disconnected from the DC grid. Power and voltage of node 2 go to 0 (see Figs. 3.28(a) and 3.28(c)). The DC currents also suffer

some oscillations; however, the CFC is able to maintain I_{41} to the same level (see Fig. 3.28(b)). Finally, the duty cycle and the CFC voltage experiment important oscillations but after 1 second approximately, they return to stable operation.

3.8 Conclusion

In this chapter, an interline DC/DC CFC has been analysed. The different operation states of the converter have been gathered in pairs in order to apply voltages on the lines with the minimum number of active switches. Then, an average model of the CFC is derived and it is used to perform steady-state analysis in a 3-terminal HVDC grid. Changing the duty cycle of the active switch of the CFC allows varying the line currents significantly. It also shows that with few kV in the CFC capacitor, several hundreds of amperes can be redirected. The operation area of the system with and without CFC has been illustrated. This operation area shows an important increase and this analysis also provides a criterion to choose the voltage rating of the CFC. Two CFC control strategies have been proposed based on the linearised model of the meshed HVDC grid and the CFC; a single current controller and a cascaded approach with an outer current controller and an inner voltage controller. Dynamic simulations with 3-terminal and 5-terminal HVDC grids are used to validate both control approaches. The CFC shows good performance during step changes and the detailed model of the grid and the CFC show close similarity with the linearised one near the operational point. The cascaded approach with a current and voltage controller is able to limit the maximum voltage of the CFC when regulating the current to avoid voltages above the ratings of the device. The system performance is also tested considering node power changes and a terminal outages, showing an acceptable CFC performance under such conditions and validating the control procedure.

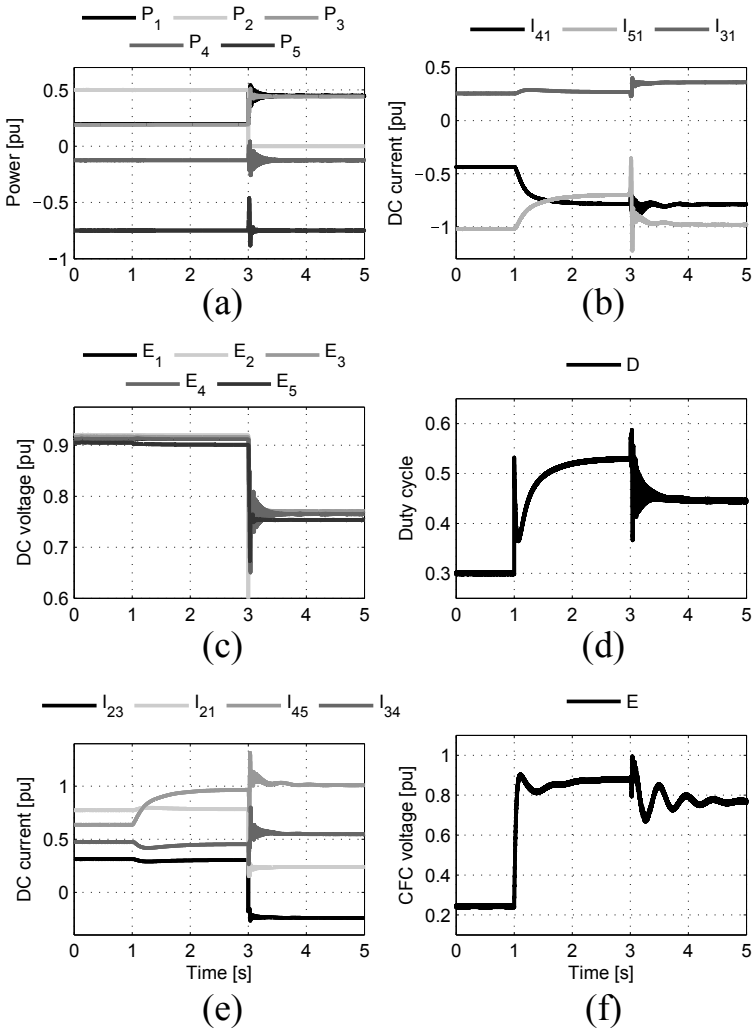

Fig. 3.28: Comparison between different CFC control schemes. (a) DC current of line 41. (b) CFC voltage.

Chapter 4

Integrated HVDC circuit breakers with current flow control capability

4.1 Introduction

On one hand, CFCs will be required in meshed DC grids in order to prevent cables from being over loaded [17]. Using power electronics they insert variable voltage sources in series with the selected lines, thus modifying its current flow. Several topologies have been presented so far [22, 28, 34], ranging from variable resistors, DC/AC converters and DC/DC converters [34]. CFCs based on DC/DC converters provide reasonable possibilities and isolation transformers are not required [34].

On the other hand, DC Circuit Breakers (DCCB) are likely to be required for grid power ratings that exceed the AC systems' maximum infeed loss limits. Advanced circuit breakers designs are so-called hybrid DC breakers incorporate power electronics into their designs [59].

The development of both CFC and DCCB is an important step on the road to meshed HVDC grids. While the two functional aspects of CFCs and fault protection exist separately, there is opportunity to integrate the functionality into the same equipment. This chapter investigates how CFC functionality can be integrated into a hybrid circuit breaker's design if it contains a Line Commutation Switch (LCS), or equivalent, in its primary branch.

First, an overview of the two systems under investigation is given showing a high level view of integrating CFCs into DCCBs. Then, this chapter discusses hybrid circuit breakers, with specific attention given to the Proactive Hybrid Circuit Breaker (PHCB) developed by ABB [59]. After that, the CFC under study is introduced, based on the topology of a DC/DC converter presented in [34], which consists of two H-bridge converters joined through a capacitor, where each H-bridge is connected in series with a DC line, also analysed in detail in Chapter 3. It is then shown how the CFC can

be integrated into the PHCB by changing the orientation of the switches within the LCS. This new layout is then discussed and a state-space analysis is performed on the circuit breaker's commutation process. Then, the controller of the LCS/CFC is designed based on the state-space model of the meshed HVDC grid, and is tested in both MATLAB Simulink and PSCAD normal operation simulations. After, case studies are performed to verify the protection operation of the LCS/CFC and the descriptive equations. The performance of the combined LCS/CFC and separate the CB and CFC in a separate design are also compared. The major contribution of this chapter is the concept of integrating CFCs into the PHCB, the control, and the associated analysis of this idea.

4.2 DC circuit breakers with current flow control capability

CFCs are used to overcome the limitations imposed on the power transmitting capability of a meshed DC system due to differences in line impedance, whereas the CBs are required in meshed HVDC grids to protect the system from DC faults. Both the CFC and HCB require power electronic elements which are permanently exposed to the DC line current. The structure of the technology that is in series with the line is similar in each case. Due to the similarities in these two pieces of equipment, it is possible to integrate the CFC capability into the circuit breaker's design. Therefore, space, power loss and material costs can be saved. The initial meshed HVDC grid under study with the CFC located at station 1 is shown in Fig. 4.1(a). The meshed HVDC grid is composed of 4 stations based on VSCs interconnected with four cables where a HCB is included at each end of the cables. Fig. 4.1(b) illustrates the same HVDC system with the proposed concept which integrates the CFC functionality into the two DCCBs in station 1.

4.3 Proactive hybrid circuit breaker

The PHCB was developed by ABB and is shown in Fig. 4.2. This circuit breaker design has been proposed as one potential design for future HVDC circuit breakers. This type of circuit breaker uses a LCS to divert current out of a mechanical switch into a semiconductor breaker. The operation of this circuit breaker is discussed in [59], with a more detailed analysis given in [71–73]. Other circuit breaker designs also contain LCSs or equivalent switches [74, 75].

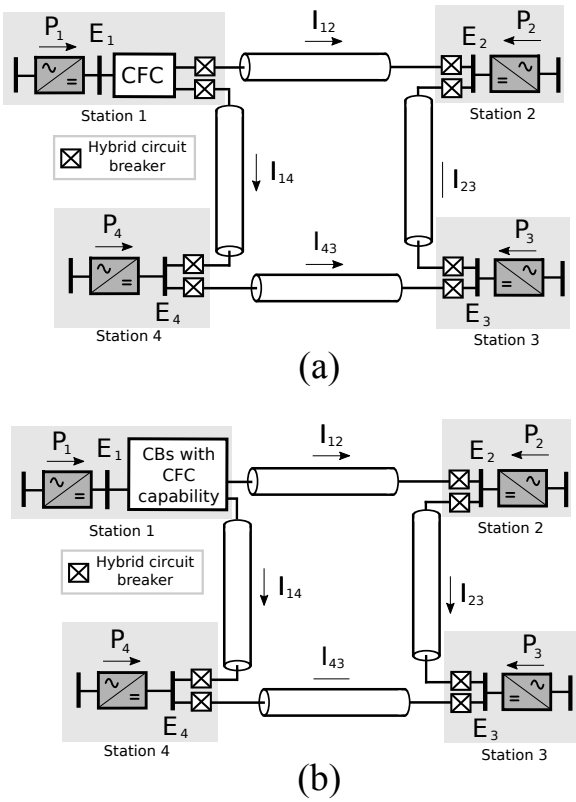

Fig. 4.1: Meshed HVDC grid under study. (a) CFC and CBs in a separate design. (b) Proposed integrated CBs with CFC functionality.

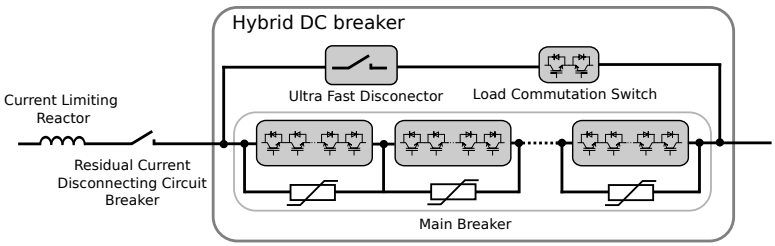

Fig. 4.2: The proactive hybrid circuit breaker [59].

The circuit breaker's LCS is a small matrix of semiconductors which are placed permanently in series with the DC line. The LCS normally remains in the conducting state and passes the line current, incurring several kilowatts of losses. Once a fault is detected, the current is diverted into a main breaker by turning off the LCS.

The LCS could be a single device, but due to the voltage, current, redundancy, and power loss requirements, the LCS will likely be made up from several devices [72].

The circuit breaker is modelled representing each power electronic switch as a single switch model, parametrised for the desired voltage rating. The mechanical switches have been modelled as ideal switches with a fixed delay to replicate the opening of the mechanical switch. The circuit breaker has been parametrised for a 300 kV application using the information given in Table 4.1, [59], [72], and analysis in [71].

Table 4.1: Circuit Breaker parameters. MB=Main Breaker

Parameters	Values	Units
L_1/L_s	100/30	µH
V_{on}	904	V
R_{on}	0.1	Ω
Series devices per direction	149	-
Snubber capacitance	0.234	µF
Mech. opening time	2	ms
Detection time	1	ms
Knee Voltage	320	kV
K_v	2	-

4.4 Current flow controller

A diagram of the CFC is presented in Fig. 4.3. The CFC topology used in this paper is presented in [34] and its operation and control methodology are described in Chapter 3. The CFC is based on two H-bridge converters joined through a capacitor and each bridge connected to a different DC line in the meshed HVDC grid. The CFC extracts power from one cable and feeds the other, thus, applying variable voltage sources in series with the lines. By doing so, it is able to reduce or increase the DC currents circulating through

the lines of the HVDC grid. The proposed DC/DC converter can be used for any current direction, though for this analysis, I_1, I_{12} and I_{14} are considered to be positive during normal operation. Considering the aforementioned current configuration, the active switches that are able to operate are: S_{A1}, S_{B1}, S_{A2} and S_{B2} and according to the analysis in Chapter 3. The rest of the switches are always in OFF state. The operation states of the CFC are summarized in Table 4.2, considering I_1, I_{12} and $I_{14} > 0$. "1" means the switch is on and "0" means the switch is OFF.

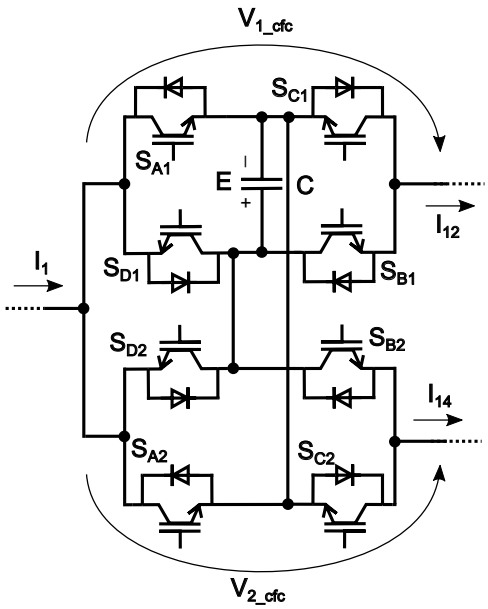

Fig. 4.3: Dual H-bridge CFC topology.

Table 4.2: Switching states of the CFC

	I_1, I_{12}, $I_{14} >$ 0							
$S_{A1,2}$	0	0	0	0	1	1	1	1
S_{B1}	0	0	1	1	0	0	1	1
S_{B2}	0	1	0	1	0	1	0	1
V_{1_cfc}	+E	+E	0	0	0	0	-E	-E
V_{2_cfc}	+E	0	+E	0	0	-E	0	-E

4.4.1 CFC modelling

Table 4.2 illustrates the switching states of the CFC and the voltage that they are applying in both lines 12 and 14. Combining some of the states depicted in Table 4.2, the CFC is able to apply a positive voltage in one line and a negative voltage in the other so that the line current of one line can be diverted to the other. The converter average model can be derived as two voltage sources in series by combining adequately some states in Table 4.2 as explained in Chapter 3. The average voltages applied by the CFC are:

$$\overline{V}_{1_cfc} = (1 - D)\overline{E} \qquad \overline{V}_{2_cfc} = -D\overline{E} \tag{4.1}$$

D is the current relation between I_{12}/I_1, which is equivalent to the duty cycle of the switch S_{A1} and S_{A2} when the CFC is reducing the current I_{12} compared to the initial conditions. When the CFC is reducing current I_{14}, D corresponds to the duty cycle of the diodes in S_{D1} and S_{D2}. E is the voltage of the CFC capacitor when the CFC is reducing I_{12}. When the CFC is decreasing I_{14}, E corresponds to the negative value of the capacitor voltage. The previous average model derivation is explained in detail in Chapter 3. For the MATLAB and PSCAD simulations the CFC is modelled in detail using a switch model composed of 8 IGBTs. The switching frequency of the CFC is 2 kHz and its capacitance, C, is set to 10 mF. The average model of two voltage sources is used only for the controller design.

4.5 Integrated LCS with CFC capability

The LCS structure of the PHCB shares many similarities with the CFC topology presented in Section 4.4, therefore, the CFC capability is integrated in the PHCB using the LCS of the two CBs in the same Station 1. An example of LCS structure is shown in Fig. 4.4(a). This topology allows bidirectional current breaking in the primary branch. Taking the same switches and rearranging their orientation allows the LCS to act as a CFC during normal operation, as shown in Fig. 4.4(b).

The LCS now resembles one half of the traditional CFC structure given in Fig. 4.3. Neighbouring circuit breakers can then have their LCSs connected together as shown in Fig. 4.5.

During normal operation the main breakers within each circuit breaker will be turned OFF and the mechanical switch M_1 must be in ON state. The required DC side inductor L_{DC} must be placed on the cable side rather than the converter side of the circuit breaker. This allows the LCS/CFC

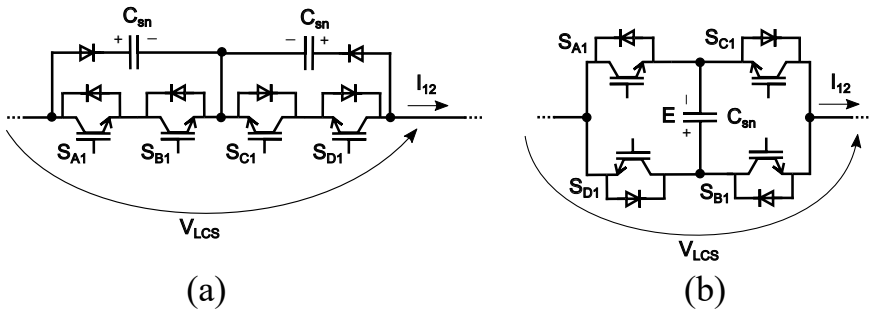

Fig. 4.4: (a) LCS structure. (b) LCS structure with CFC capability.

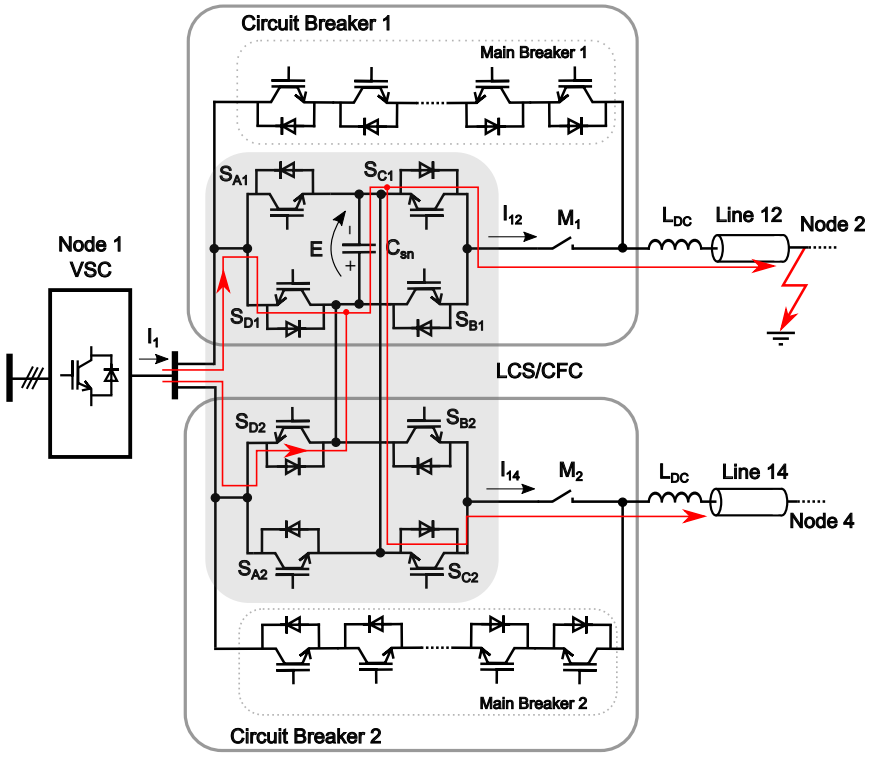

Fig. 4.5: LCS interconnected with CFC capability. Current flow considering a fault on line 12 with the LCS/CFC switches in OFF state and the main breakers turned OFF.

to have the common node required for CFC operation. The LCS/CFC is operated following the same procedure of the single CFC [76]. When a fault occurs, current starts to flow from the converter and other lines towards the fault location. When the circuit breaker is required to open, the switches in both LCS/CFCs are turned OFF (see Fig. 4.5) and the main breaker of the faulted line is turned ON. The current flowing through the LCS/CFC diodes charges the LCS/CFC capacitor.

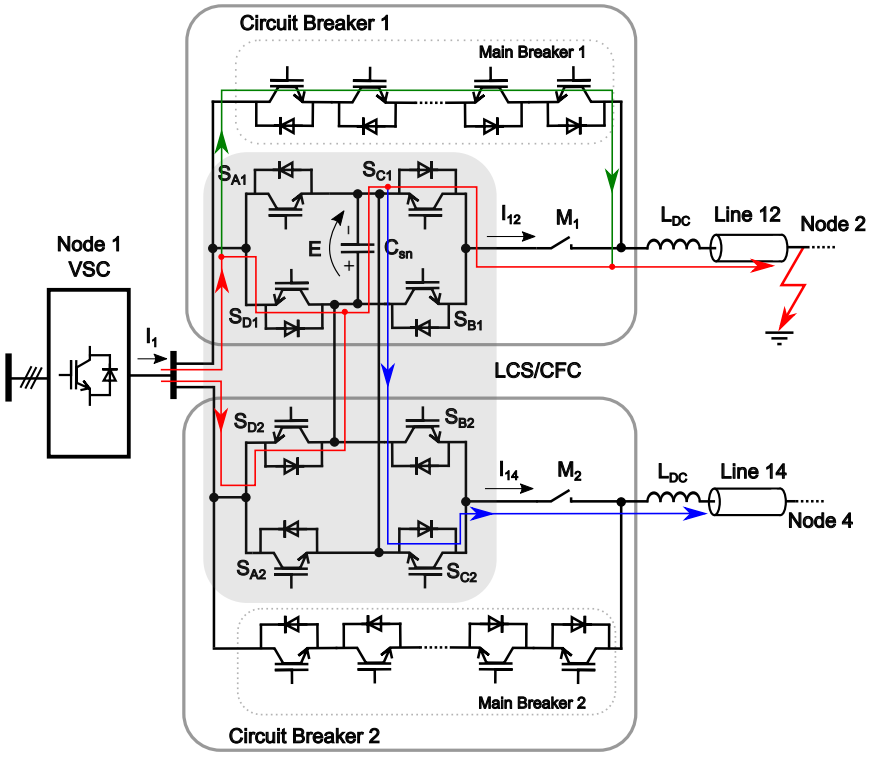

Fig. 4.6: Shows the current flowpath within the LCS/CFC once the Main Breaker 1 is turned ON.

Current starts to flow through the Main Breaker 1 as it now provides a low impedance path allowing current to be diverted away from the mechanical switch M_1 by the voltage across the LCS, V_{LCS}, as shown in Fig. 4.6. This allows the mechanical switch to be opened without an arc, and once the switch is fully open the Main Breaker 1 can be turned OFF to break the flow of current. Also, when the fault is isolated, the required switches in the LCS/CFC of Circuit Breaker 2 can be closed to permit the flow of the current without charging the capacitor.

The switches S in the CFC/LCS can be driven by using the CFC capacitance as a floating voltage supply. The CFC capacitance will naturally charge once a DC line current starts to flow in either direction. The current will flow through the CFC/LCS diodes and pass through the CFC capacitance. Once charged this can be used to provide the gate drives voltages to allow switching to start.

The LCS/CFC design also requires the circuit breaker's inductance to be on the cable side of the circuit breaker, rather than the converter side. The CB is able to operate in this fashion for pole-to-pole and pole-to-ground faults. The circuit breaker can still operate without a fault as the CFC/LCS voltage can be used to push the load current into the secondary branch. Providing that there is a DC current flowing or if the CFC is sufficiently charged, the circuit breaker will be able to operate as described.

4.5.1 State-space analysis of LCS/CFC commutation

A state-space analysis of the circuit breaker with CFC capability has been performed using the equivalent circuit during commutation given in Fig. 4.7. This analysis works for circuit breakers on the positive or negative poles of the DC link, as well as for pole-to-ground faults.

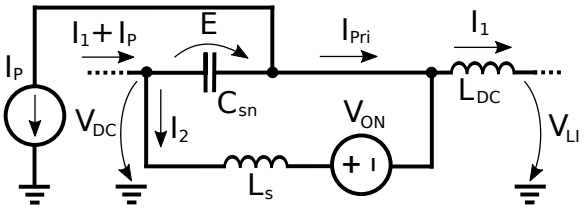

Fig. 4.7: Equivalent circuit during commutation.

This equivalent circuit was developed based on a reduction of the physical circuit layout, where: C_{sn} is the capacitance of the LCS/CFC; L_{DC} is the circuit breaker's series DC side inductor; L_s is the parasitic inductance of the secondary branch; I_p is the partner line current, V_{ON} is the total on-state voltage of the semiconductors in the secondary branch. V_{DC} is the voltage across the converter's terminals and V_{LI} is the line voltage.

The partner line current I_p, refers to the amount of current from node 1 that does not flow towards the fault but through the not faulty line. In Fig. 4.6, the partner line current corresponds to I_{14} (blue one).

Starting with:

$$\begin{bmatrix} L_{DC} & 0 & 0 \\ 0 & L_s & 0 \\ 0 & 0 & C_{sn} \end{bmatrix} \dot{\mathbf{X}} = \begin{bmatrix} 0 & 0 & -1 \\ 0 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \mathbf{X} + \begin{bmatrix} 1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \mathbf{U} \tag{4.2}$$

and the matrix layout given as:

$$\mathbf{X} = \begin{bmatrix} I_1 \\ I_2 \\ E \end{bmatrix}, \ \mathbf{X_0} = \begin{bmatrix} I_0 \\ 0 \\ V_0 \end{bmatrix}, \ \mathbf{U} = \begin{bmatrix} V_{DC} - V_{LI} \\ V_{ON} \\ I_P \end{bmatrix} \tag{4.3}$$

The primary branch current can be solved for as the difference between the two current state variables in the s-domain, yielding:

$$I_{pri}(s) = I_1(s) - I_2(s) = \frac{[I_0 + I_P]s + G}{s^2 + \frac{L_{DC+L_s}}{C_{sn}L_{DC}L_s}} - \frac{I_P}{s} \tag{4.4}$$

Converting this to the time domain:

$$I_{pri}(t) = \left[\sqrt{[I_0 + I_P]^2 + G^2}\right] \cos(\omega_{com}t - \varnothing) - I_P \tag{4.5}$$

where:

$$G = \left[\frac{[L_s V_{DC} + L_{DC} V_{ON}] - V_0[L_{DC} + L_s]}{L_{DC}L_s\omega_{com}}\right] \tag{4.6}$$

$$\omega_{com} = \sqrt{\frac{L_{DC} + L_s}{C_{sn}L_{DC}L_s}} \tag{4.7}$$

$$\varnothing = \tan^{-1}\left[\frac{G}{I_0 + I_P}\right] \tag{4.8}$$

Then, solving for the state variable that describes the LCS voltage:

$$E(t) = A + [V_0 - A]\cos(\omega_{com}t) + \left[\frac{I_0 + I_P}{C_{sn}\omega_{com}t}\right]\sin(\omega_{com}t) \tag{4.9}$$

where:

$$A = \frac{L_s V_{DC} + L_{DC} V_{ON}}{L_{DC} + L_s} \tag{4.10}$$

Manipulating (4.5), the commutation time (the time when $I_{pri} = 0$) is given

by:

$$t_{com} = \frac{1}{\omega_{com}} \left[\cos^{-1} \left[\frac{I_P}{\sqrt{[I_0 + I_P]^2 + G^2}} \right] + \varnothing \right] \tag{4.11}$$

Based on the analysis presented in [71] the commutation time of the PHCB is normally bounded between $\frac{\pi}{2\omega_{com}}$ and $\frac{\pi}{\omega_{com}}$ for a fixed capacitance value. The combined LCS/CFC does not have this limitation as the commutation time can be reduced below $\frac{\pi}{\omega_{com}}$.

Fig. 4.8 shows comparison of simulations of the traditional LCS (Case 3), a CFC/LCS (Case 1), and the analysis presented in this section. Details of the simulations can be found in Section 4.9; where a case study has been performed. The analysis is compared to the simulations which show a strong agreement.

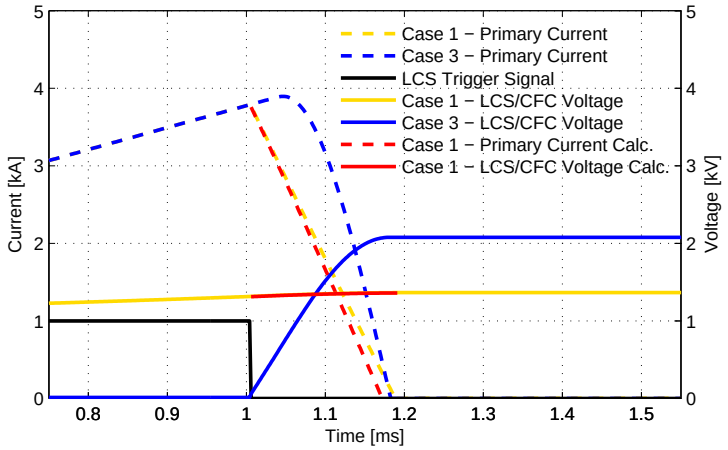

Fig. 4.8: Verification of commutation analysis for combined and separate cases. PSCAD results and calculations.

This shows the difference in the circuit breaker currents and voltages during commutation for the LCS and CFC/LCS. When the LCS is turned OFF the LCS voltages increase in both cases, and start to force the primary branch current into the Main Breaker. The CFC/LCSs able to commutate the current quicker and with a lower peak voltage; for the examples given. This fundamental difference comes from the pre-charged nature of the CFC/LCS and the coupling from the partner line current; the latter is shown in Fig. 4.9. The CFC/LCS current is the current that flows through the CFC/LCS capacitor. As the partner line current can be quickly diverted

into this capacitor, this is able to contribute to the commutation voltage; resulting in a shorter commutation time.

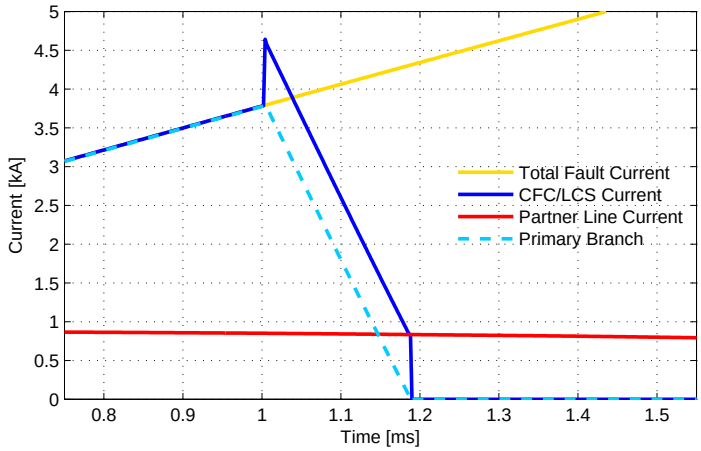

Fig. 4.9: Commutation process with LCS/CFC. Partner line current = I_p. PSCAD Results.

4.6 PSCAD modelling

In the PSCAD simulations, the HVDC system in Fig. 4.1(b) is modelled using the full 4-terminal model shown in Fig. 4.10. During normal operation, the offshore wind farm, Station 4, is delivering 0.2 GW into HVDC system and Station 1 delivers 1 GW. Converter stations 2 and 3 receive 0.7 GW and 0.5 GW, respectively. The onshore two-level converters are modelled with switched IGBTs, phase reactors, transformers and DC link capacitors and are controlled using voltage droop control [77]. Based on [78], Station 4 is configured to provide the offshore AC grid voltage and frequency. The wind farm is modelled aggregately, with the back-to-back converter in each wind turbine modelled using an average model. The offshore side transformer configuration is based on [79] and DC choppers have been used in each onshore converter's terminal to regulate the DC voltage within the normal voltage range, with the parameters from [80].

The MMC model here uses the Detailed Equivalent Model (DEM) [81]. In the DEM used in this paper, each phase arm consists of 30 sub-modules which can provide 31 voltage levels. The MMC station is set to control active and reactive power and its control diagram is illustrated in Fig. 4.11.

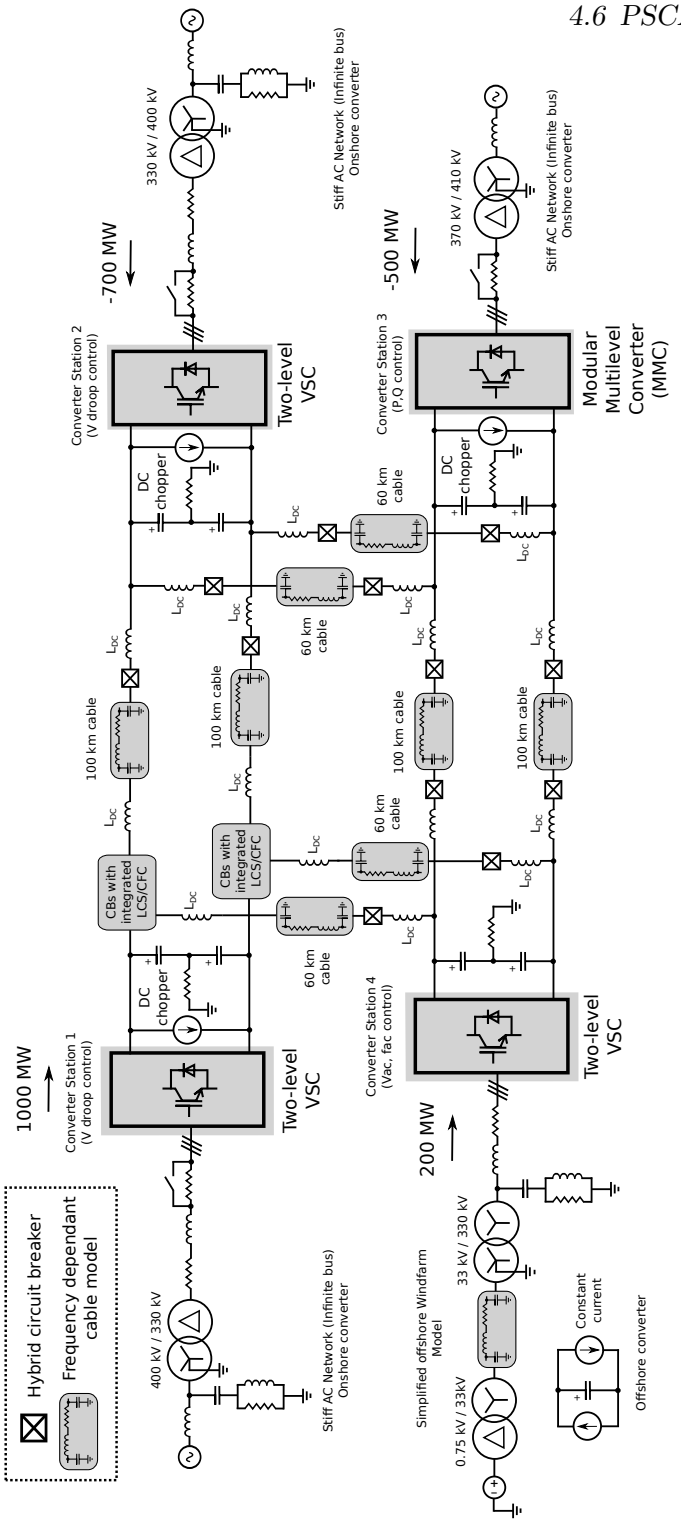

Fig. 4.10: Full PSCAD simulation model.

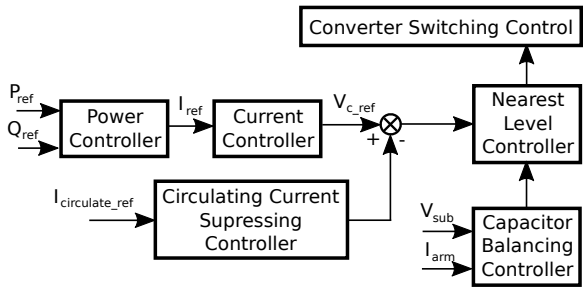

Fig. 4.11: Control structure of the MMC system.

4.7 Simulink modelling

The system presented in Fig. 4.1(a) is modelled also in Simulink. Two models are employed: First, a linearised state-space model of the HVDC grid with the average model of the CFC for controller design purposes. A second one, with the switching model of the CFC is utilised to validate the control design methodology and it is compared with the full model in PSCAD from Section 4.6. The Simulink models are used to verify the controller design and only consider half of the symmetrical monopole. These are then compared to the PSCAD simulations to provide a cross simulation verification of the design.

4.7.1 Linearised state-space

The linearised model of the meshed HVDC grid is derived following the same strategy as in Chapter 3. The model is shown in Fig. 4.12, where only the upper half of the symmetrical monopole of the system is considered due to its symmetry.

Following this approach, only one CFC needs to be included in the HVDC grid due to the symmetry. It is modelled according to the average model with two voltage sources and the corresponding equation representing the charging and discharging of the CFC capacitor (see Chapter 3). Cable capacitance is neglected due to its reduced value compared with node capacitance; only the inductance and resistance of the cable are considered. L_{ij} gathers the inductance of the cable between node i and node j and the two DC limiting reactors of each line L_{DC}. R_{ij} comprises the resistance of the cable and C_i is the power converter capacitance of node i. The system is linearised as:

$$X_i \approx X_{i0} + \Delta X_i \tag{4.12}$$

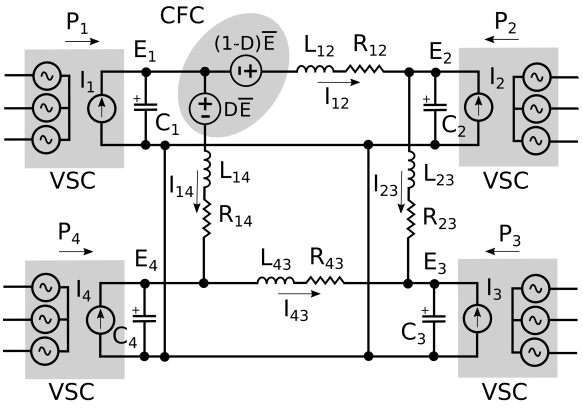

Fig. 4.12: Equivalent model of the 4-terminal HVDC system with CFC used for linearisation.

where, X_i is a general variable, X_{i0} is its linearisation point and ΔX_i is the increment over the linearisation point. Terminal 1 and 2 are operating in DC voltage droop control and terminal 3 and 4 in constant power injection mode:

$$I_1 = \frac{P_1}{E_{base}} + \frac{k_d P_{base}}{E_{base}^2}(E_1^* - E_1) \tag{4.13}$$

$$I_2 = \frac{P_2}{E_{base}} + \frac{k_d P_{base}}{E_{base}^2}(E_2^* - E_2) \tag{4.14}$$

$$I_3 = \frac{P_3}{E_3}, \qquad I_4 = \frac{P_4}{E_4} \tag{4.15}$$

where, P_i is the power of node i; I_i is the current of node i; E_i is the voltage of node i; E_i^* is the voltage droop reference of node i; k_d is the droop constant and P_{base} and E_{base} are the base power and voltage. The meshed HVDC grid and the previous equations are linearised following the same approach as in Chapter 3 and the following state-space model is obtained:

$$\frac{d\Delta x}{dt} = \mathbf{A}\Delta x + \mathbf{B}\Delta u \tag{4.16}$$

where:

$$\Delta x = (\Delta E_1, \Delta E_2, \Delta E_3, \Delta E_4, \Delta I_{12}, \Delta I_{14}, \Delta I_{23}, \Delta I_{43}, \Delta E) \tag{4.17}$$

$$\Delta u = (\Delta P_1, \Delta P_2, \Delta P_3, \Delta P_4, \Delta D) \tag{4.18}$$

$$\mathbf{A} = \begin{bmatrix} \frac{-k_d P_{base}}{C_1 E_1^2} & 0 & 0 & 0 & -\frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{-k_d P_{base}}{C_2 E_2^2} & 0 & 0 & \frac{1}{C_2} & 0 & -\frac{1}{C_2} & 0 & 0 \\ 0 & 0 & \frac{-P_{30}}{C_3 E_3^2} & 0 & 0 & 0 & \frac{1}{C_3} & \frac{1}{C_3} & 0 \\ 0 & 0 & \frac{-P_{40}}{C_4 E_4^2} & 0 & 0 & \frac{1}{C_4} & 0 & -\frac{1}{C_4} & 0 \\ \frac{1}{L_{12}} & -\frac{1}{L_{12}} & 0 & 0 & \frac{-R_{12}}{L_{12}} & 0 & 0 & 0 & \frac{1-D}{L_{12}} \\ \frac{1}{L_{14}} & 0 & 0 & -\frac{1}{L_{14}} & 0 & \frac{-R_{14}}{L_{14}} & 0 & 0 & \frac{-D}{L_{14}} \\ 0 & \frac{1}{L_{23}} & -\frac{1}{L_{23}} & 0 & 0 & 0 & \frac{-R_{23}}{L_{23}} & 0 & 0 \\ 0 & 0 & -\frac{1}{L_{43}} & \frac{1}{L_{43}} & 0 & 0 & 0 & \frac{-R_{43}}{L_{43}} & 0 \\ 0 & 0 & 0 & 0 & \frac{D_0-1}{C} & \frac{D_0}{C} & 0 & 0 & 0 \end{bmatrix} \tag{4.19}$$

$$\mathbf{B} = \begin{bmatrix} \frac{1}{C_1 E_{base}} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2 E_{base}} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_3 E_{30}} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_4 E_{40}} & 0 \\ 0 & 0 & 0 & 0 & \frac{-E_0}{L_{12}} \\ 0 & 0 & 0 & 0 & \frac{-E_0}{L_{14}} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{I_{12}+I_{14}}{C} \end{bmatrix} \tag{4.20}$$

The parameters of the Simulink models are illustrated in Table 4.3.

4.7.2 CFC switching model

The second model of the HVDC grid and the CFC also only considers the upper half of the symmetrical monopole, but in this case the cables are modelled as PI sections and two DC limiting inductors with L_{DC} each, are placed in each line. The modelling of the converter terminals are the same as in Section 4.7.1. The CFC is modelled as two H-bridges as shown in Fig. 4.3 and the overall system model is depicted in Fig. 4.13.

4.8 LCS/CFC control design methodology

The control design methodology is based on the state-space representation of the 4-terminal HVDC system, presented in Section 4.7.1 and the same procedure as in Chapter 3 is applied. The variable to be controlled is set to

Table 4.3: Simulink model parameters

Cable parameters				
Resistance [Ω/km]			0.0113	
Inductance [mH/km]			2.777	
Capacitance [µF/km]			0.2635	
Lines	12	14	23	43
Distance [km]	100	60	100	60
VSC parameters				
Node i	12	14	23	43
Power P_i [MW]	1000	−700	200	−500
Capacitance C_i [µF]	200	200	200	200
Voltage E_i^* [kV]	298	298	–	–
Droop k_d [pu/pu]	2	2	–	–
Base values				
Node voltage [kV]			300	
Node power [MW]			1200	
Line current [kA]			300	
CFC voltage [kV]			4	

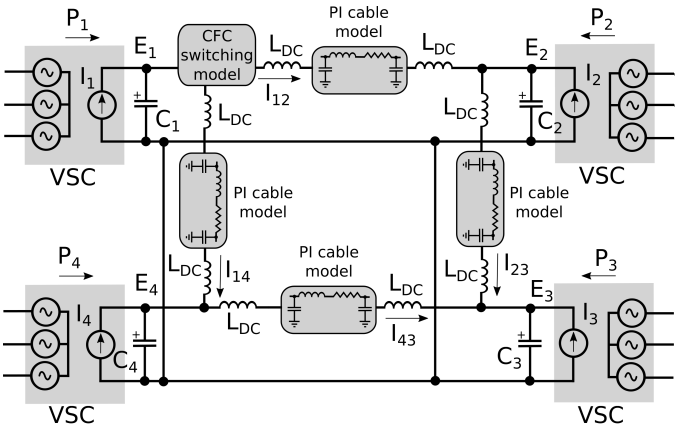

Fig. 4.13: Equivalent model of the 4-terminal HVDC system with the CFC switching and PI cable models.

be DC current I_{12} and the control action is the duty cycle D of the operating switch $S_{A1,2}$. Based on the state-space model, a transfer function relating the current I_{12} and duty cycle D is obtained, $G_{I_{12}-D}$. For this work, a PI controller, a second order compensator and a low pass filter are used for the controller. It is tuned to achieve a closed-loop time response of 0.6 s and no overshoot in the capacitor voltage. The controller parameters are presented in Table 4.4, considering that current I_{12} is measured in Amps. Fig. 4.14 illustrates the control scheme.

Table 4.4: Controller parameters

PI controller	2^{nd} order compensator			L. P. Filter
K_p	a_2	a_1	a_0	τ
$2.48\dot{1}0^{-5}$	522	1094	29889	0.03
K_i	b_2	b_1	b_0	
$6.29\dot{1}0^{-4}$	1	746	18616	

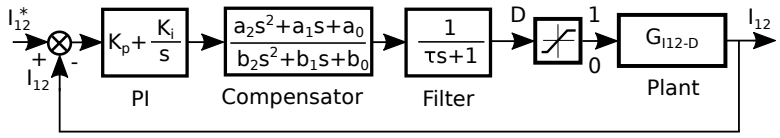

Fig. 4.14: Control scheme of the CFC.

4.9 Simulation results

4.9.1 Normal operation of the LCS/CFC

The first study performed is a normal operation analysis of the LCS/CFC, to ensure that its CFC operation is conserved. The results of the CFC in the Simulink and PSCAD models are shown in Fig. 4.15.

Figs. 4.15(a) and 4.15(b) illustrate the LCS/CFC voltage and current I_{12} response, respectively, after a change of 0.1 pu in the I_{12} setpoint. The voltage dip seen in the PSCAD simulations is due to the different cable models used. However, the dominant dynamics of the response are very similar, showing that the controller designed using the linearised model in Simulink can be used to control the LCS/CFC in the detailed PSCAD model. It

can be seen than at instant $t = 2.6$ s (a time constant after the reference change), the value of the line current I_{12} is approximately 0.657 pu, which correspond to the 63% of the final value and matches the design criteria applied in the linearised model to obtain the controller parameters. Although a complete validation between the two models in Simulink is not provided in this chapter, it can be found in Chapter 3 for a 3-terminal HVDC grid.

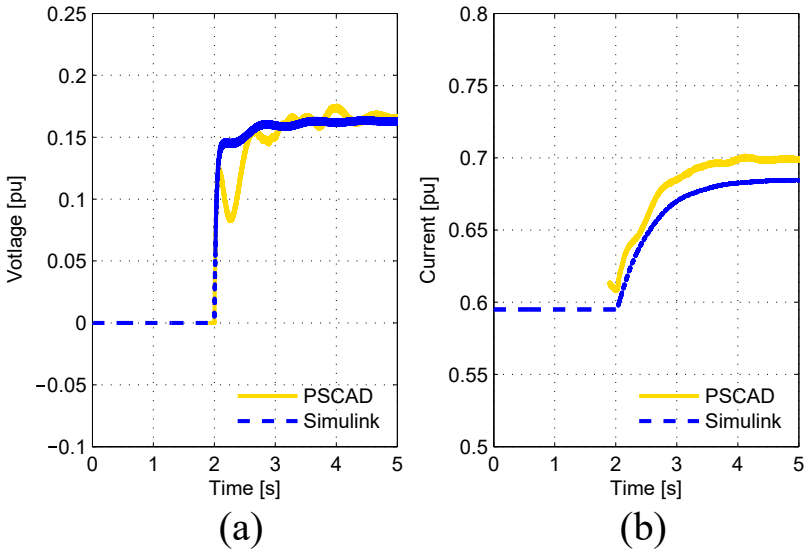

Fig. 4.15: Comparison of normal operation case study results from MATLAB and PSCAD simulations. (a) LCS/CFC voltage V_{LCS}. (b) Current I_{12}.

4.9.2 Protection simulations

A second study was undertaken to assess the differences in protection performance of combined and separate designs. The study aimed to show that the circuit breaker is still capable of operating when the CFC is integrated into the LCS and verify the analysis performed in Section 4.5.

The major design choices for an LCS are the peak voltage, and commutation time. These two attributes are heavily dictated by the snubber circuit capacitance used. For the combined LCS/CFC, the capacitance is fixed based on the acceptable ripple voltage in the CFC. This capacitance is several orders of magnitude larger than what is thought to be used in the LCS. In order to compare the separated and integrated approach properly,

several different LCS capacitance values were chosen (10 mF, 160 µF and 30 µF).

A protection study was undertaken for a fault located between converter station 1 and 2, 50 km along the line and four different design cases were assessed. Case 1 is the case where the CFC and LCS are combined. The commutation circuit capacitance is defined by the design of the CFC, which was 10 mF. In Case 2 the CFC and LCS exist separately and the LCS capacitance is chosen to be the same as Case 1. Case 2 was chosen to show that the commutation time is drastically impacted if the LCS capacitance is increased to reduce the peak LCS voltage. In Case 3 the capacitance is designed to have a similar commutation time in Case 1. Case 4 uses a low value of capacitance to show a fast commutation time. For the separated designs the CFC capacitance is 10 mF.

Fig. 4.16 compares the performance of the four case studies during a protective action and it shows the current through the primary branch and the total current of the line for each case. Cases 1,3 and 4 all maintain a reasonable circuit breaker operation time, due to the commutation times being kept in the order of microseconds. Case 2 has a commutation time of 2.2 ms, which extends the operation time of the protection beyond a reasonable time frame. This shows that reduction in peak voltage obtained from this design, cannot be achieved by simply increasing the LCS capacitance without compromising protection performance.

Fig. 4.17 shows a plot of the governing equations for commutation time and peak voltages across the inline power electronics (LCS and CFC) [71]. This shows that there is a fundamental difference in the governing equations due to the LCS/CFC capacitor being pre-charged and the coupling between the DC lines I_P. As there is less variation in commutation time when the LCS/CFC capacitance is increased, a higher capacitance can be used, which results in a significantly lower peak voltage across the LCS. A summary of the commutation times, voltages across the power electronic elements and the case parameters is given in Table 4.5. The results show that even though the LCS/CFC has a significantly larger capacitance, the commutation time is not detrimentally extended and is within the experimental times stated in [59]. The peak voltages across the CFC and LCS are also significantly reduced compared to the other cases. The CFC voltage will start to increase naturally in the separated design as the diodes become forward biased and result in the CFC capacitor charging, for which it must be designed.

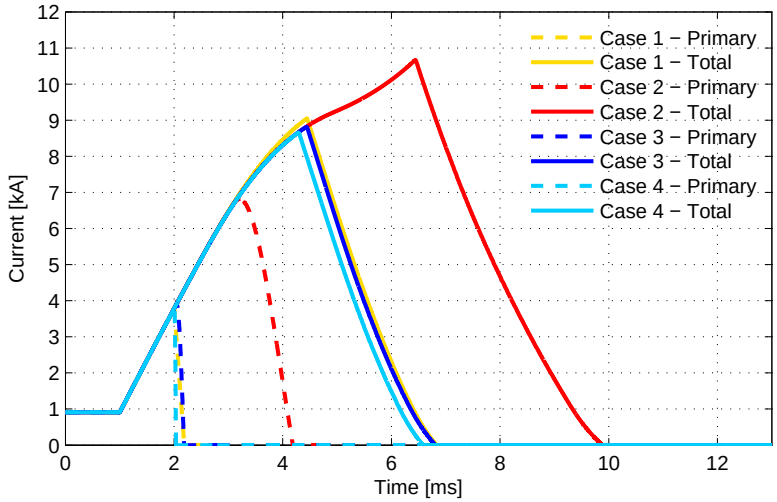

Fig. 4.16: Fault Current Comparison for each case. Total fault current (solid lines). Primary branch current (dashed lines) - PSCAD Results.

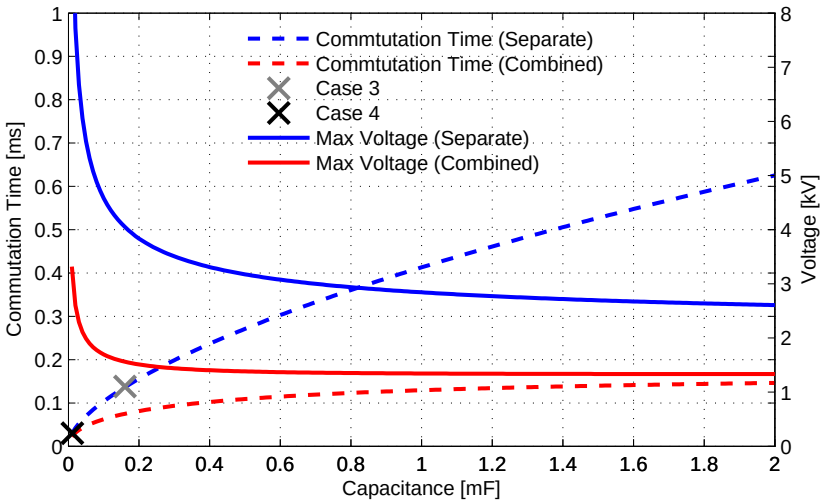

Fig. 4.17: Comparison of combined and separate cases.

Table 4.5: Comparison of Combined and Separate LCS and CFC desgins

	Case	C_{sn} [µF]	LCS voltage V_{LCS} [kV]	CFC voltage E [kV]	Com. time [µs]
Combined	1	10000	1.32		184
Separate	2	10000	1.02	5.89	2286
Separate	3	160	3.84	3.32	104
Separate	4	11	6.81	3.28	30

4.10 Conclusions

The integration of CFC functionality into hybrid circuit breaker designs can provide significant advantages. This concept has been verified using two independently developed simulations of a mixed converter topology 4-terminal VSC-HVDC grid. The normal operation case study has shown that the CFC operation can be conserved when integrated in to the circuit breaker's design, and details of the control used in this work have been given. The protection case study has shown that the circuit breaker's operation is not significantly affected by the LCS/CFC, as a reasonable commutation time is maintained, even with the increased primary branch capacitance. This has the added benefit of reducing the peak voltage across the LCS significantly. The breaker also provides over voltage protection for the CFC, as current is diverted away from the CFC during a DC fault transient.

The pre-charged nature of LCS/CFC capacitance and the coupling between the two branches allows the limitations of the original LCS design to be overcome, potentially resulting in faster breaking times. The CFC/LCS may also provide a useful power source for other power electronics that require a power source. The limitations of the design are the re-start capability in the event the CFC is discharged. In such an event, there is a need to recharge the CFC capacitance, which will cause a delay or a short disturbance in the DC line power flow. Backup protection cannot immediately start to act once the fault is detected. This results in a delay equal to the commutation time. There will also need to be a more complex controller that sits around the CFC controller to ensure that protection functionality is maintained under all scenarios.

Chapter 5

Series interline DC/DC current flow controller for meshed HVDC grids

5.1 Introduction

This chapter presents a series interline CFC topology for current flow control in meshed HVDC grids [82]. The aforementioned device is based on a DC/DC converter connected between three lines and has the ability to increase, reduce or null the current through one of those lines. The main advantage of the presented topology for unidirectional current flow is its simple structure that allows to regulate DC currents with a reduced number of switches compared to the dual H-bridge presented in [34]. The initial CFC topology can be extended in order to operate with all the current flows by merging CFC structures, providing then the capacity to invert the desired currents. Firstly, the CFC topology and its extended version are presented. Secondly, the work illustrates the operating principle of the CFC and an average model for the circuit is derived. Then, a comparison between the proposed CFC and the dual H-bridge [34] is provided, analysing advantages and disadvantages. After that, the operation procedure for the extended CFC topology, which permits to invert line currents, is presented and its modulation strategy is also addressed. This work also outlines the protection equipment required to protect the CFC when a DC fault occurs in the HVDC grid. The control of the CFC is designed and a 5-terminal meshed HVDC grid is modelled and used to validate the device. The CFC is tested by means of dynamic simulations using Matlab Simulink in a 5-terminal meshed HVDC grid. Finally, a prototype of the CFC is built and tested in an experimental platform in the laboratory, which represents a scaled down symmetrical monopole HVDC grid with three terminals. For the experimental validation, different control modes of the CFC are also tested.

5.2 Series interline current flow controller

In this section, the CFC topology is presented and its extended version which is able to operate with all current flows is detailed. The CFC under study is a DC/DC converter connected between three DC lines. It inserts two variable voltage sources of opposite polarity on two transmission lines, by exchanging power between them. By applying these voltages, the CFC is able to regulate DC currents flowing through the transmission lines.

5.2.1 CFC topology

The structure of the proposed CFC topology is composed of two switches and one capacitor as it can be seen in Fig. 5.1. This figure depicts each switch as an IGBT with a diode in series. Nonetheless, other types of fully controllable switches with reverse blocking voltage capability can be used for real implementation, such as symmetrical Integrated Gate-Commutated Thyristors (IGCTs). The presented structure has three ports to be connected to three different DC transmission lines. According to the orientation of the switches, the DC currents of lines A, B and C cannot be reversed due to the presence of a diode in series with each transistor. This structure can only be used when no power reversal is expected in DC transmission lines. The previous structure in Fig. 5.1(a) is operational when two of the three DC currents are entering the device and one is going out. However, when one current is entering and two of them are going out, the required structure is illustrated in Fig. 5.1(b).

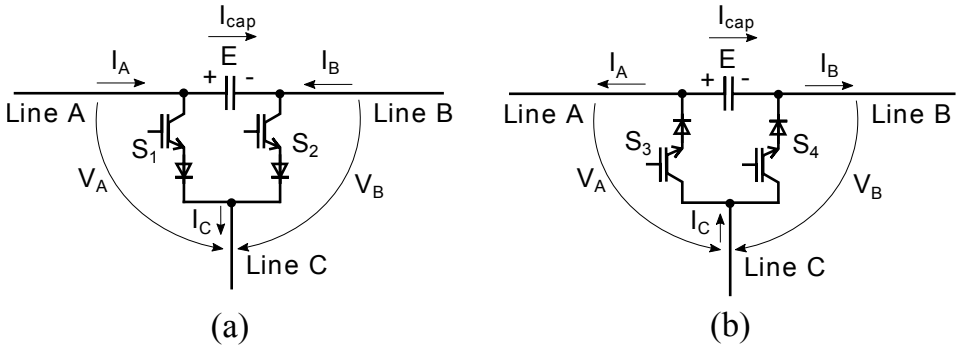

Fig. 5.1: Proposed CFC topology. (a) Two currents entering and one going out. (b) Two currents going out and one entering.

5.2.2 Extended CFC topology for all current flows

Considering a three port CFC, with three different connections to DC transmission lines, Table 5.1 depicts the six possible current configurations. + means the current is entering the device and − that is going out. Each one of this six configurations can be associated to a different CFC structure (as the presented in Section 5.2.1) and they also give name to the operation modes of the extended CFC topology. For example, if the required CFC needs to be able to regulate currents considering configurations 2 and 6, the structure presented in Fig. 5.2 can be employed. Fig. 5.2 shows a CFC layout composed of two CFC structures that can be used when I_A is entering and I_C is going out, whereas I_B can be entering or going out the device.

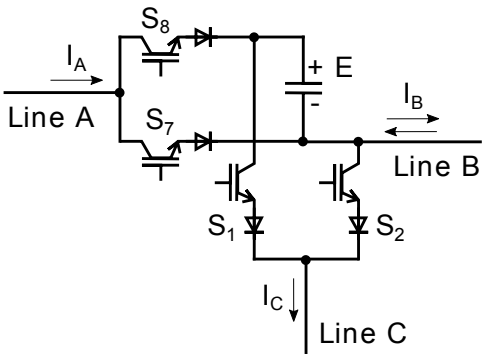

Fig. 5.2: Extended CFC topology able to operate with current configurations 2 and 6.

Table 5.1: Possible current configurations in a 3-port CFC

Configuration	1	2	3	4	5	6
I_A	-	+	-	+	-	+
I_B	-	+	+	-	+	-
I_C	+	-	-	+	+	-

In order to have a device with CFC capability for all configurations, six CFC structures are merged in a single CFC device which is illustrated in Fig. 5.3. Each structure adds two switches, nevertheless, only one capacitor is required since it is shared between the six structures. This configuration provides CFC capabilities for all possible current configurations, though, not

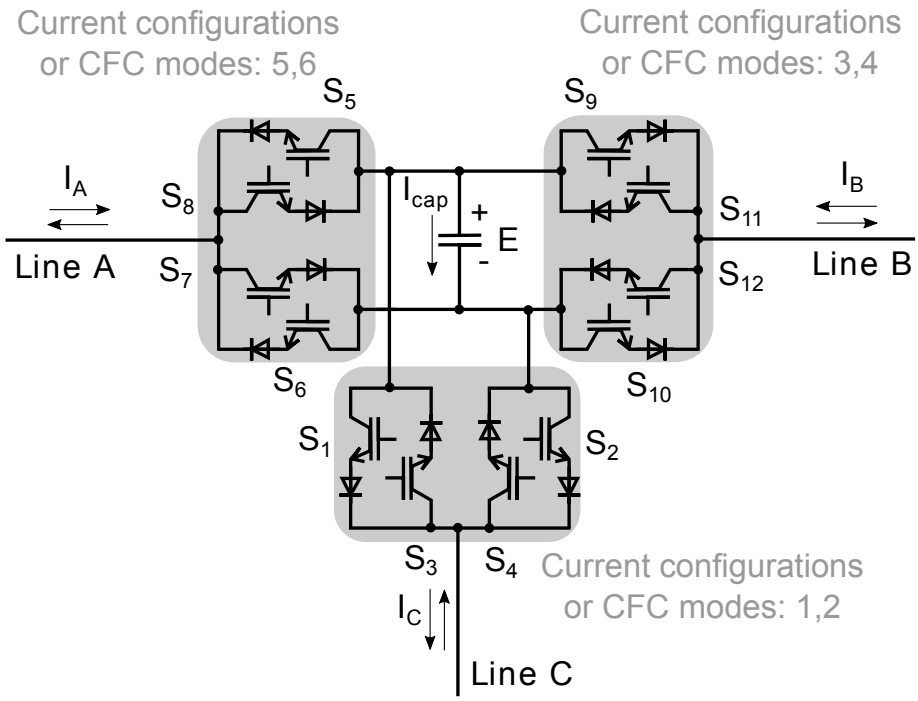

Fig. 5.3: Extended CFC topology for all current configurations.

all of them may be required as some current flow configurations may not be intrinsically possible in the corresponding HVDC grid. The extended CFC topology has the possibility to incorporate only the required CFC structures according to the expected current flow, thus, reducing the number of needed switches depending on the application.

5.2.3 Implementation methodology for the extended CFC topology for all current configurations

Initially, the reverse blocking voltage capability required for the switches is ensured placing an additional diode in series with the IGBT. Nevertheless, considering the extended CFC topology, the same behaviour can be achieved taking advantage of commercial IGBT packages that incorporate an anti-parallel diode. In this scheme, each pair of IGBTs are placed in series and the CFC layout is depicted in Fig. 5.4.

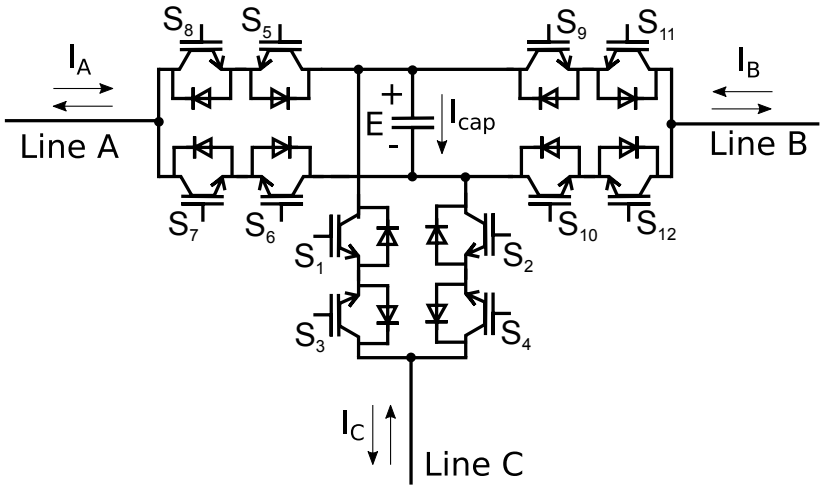

Fig. 5.4: CFC layout of the extended topology taking advantages of the anti-parallel diodes.

5.3 CFC modelling

5.3.1 Operating principle

Considering the CFC structure for current configuration 2 (CFC mode 2, see Table 5.1, Fig. 5.1(a)), the operating principle of the CFC is described

below. It is based on the complementary operation of the two switches S_1 and S_2. When S_2 is in ON state, S_1 must be in OFF state and viceversa. The capacitor is being charged when S_2 is ON with current I_A and V_A is the capacitor voltage, E, (which can be either positive or negative). In this situation, the applied voltage V_B is 0. When S_1 is ON, S_2 is OFF, so that the capacitor is discharged with current I_B and V_B corresponds to the voltage of the capacitor in inverse polarity. At this moment, in line A the applied voltage, V_A, is 0. As a result, considering constant I_A and I_B currents, the voltage across the capacitor is a triangular waveform with an average value of E and the current through it is a square waveform, I_{cap}. Note that, for the real implementation of the CFC, the switches S_1 and S_2 must have a negative dead-time, which means that both of them should be closed during a reduced period of time between switching states to allow the flow of DC current through the device at any time.

Taking into account that switches S_1 and S_2 operate complementary, the duty cycle of S_1 is defined as D, and the duty cycle for S_2 is $1 - D$. Then, the average current through the capacitor is:

$$I_{cap} = \frac{1}{T}\int_0^T i_{cap}\,\mathrm{d}t = -\frac{t_{S_1}}{T}I_B + \frac{t_{S_1}}{T}I_A = -DI_B + (1-D)I_A \tag{5.1}$$

where t_{S_1} and t_{S_1} are the time that S_1 and S_2 are closed, respectively, and T is the switching period of the converter. In order to ensure a constant steady-state voltage in the capacitor, the average current through the capacitor must be 0. Therefore, assuming no power losses in the CFC, the following equation must be met:

$$-DI_B + (1-D)I_A = 0 \tag{5.2}$$

Then, the relation between I_A and I_B can be expressed as a function of the duty cycle:

$$I_A = \frac{D}{1-D}I_B \qquad D = \frac{I_A}{I_A + I_B} \tag{5.3}$$

It means that if the total current entering in the CFC is constant $(I_A + I_B)$, increasing D leads to an increase of I_A. The average voltages applied in both lines are:

$$V_A = \frac{1}{T}\int_0^T \mathrm{v}_A\,\mathrm{d}t = \frac{t_{S_2}}{T}E = (1-D)E \tag{5.4}$$

$$V_B = \frac{1}{T}\int_0^T \mathrm{v}_B \,\mathrm{d}t = \frac{t_{S_1}}{T}E = -DE \tag{5.5}$$

Besides, the voltage ripple of the capacitor voltage can be expressed as:

$$\Delta E = \frac{I_A I_B}{fC(I_A + I_B)} \tag{5.6}$$

Finally, it can be concluded that the CFC structure can be modelled as a couple of voltage sources:

$$\overline{V}_A = (1-D)E \qquad \overline{V}_B = -DE \tag{5.7}$$

The operation of the CFC is exemplified considering constant DC currents through lines A and B (I_A = 1.5 kA and I_B = 0.7 kA) in Fig. 5.5. The capacitor voltage is controlled to 1 kV and the duty cycle corresponds to the current relation of (5.3), $D = 0.682$. The capacitance of the CFC, C, is 10 mF and the switching frequency is set at f_s = 2 kHz. The CFC voltage and capacitor current, E and I_{cap}, and the voltages applied to both lines, V_A and V_B, are illustrated in Fig. 5.5.

The capacitor of the CFC must be rated for the total nominal current of the lines since it is connected in series. Its capacitance value, C, can be chosen to minimize the ripple of the capacitor voltage according to (5.6). However, its voltage rating will depend on the desired DC current adjustment range that is expected from the CFC. The higher the CFC capacitor voltage, the larger the DC current adjustment that the CFC can bring to the HVDC grid (as it was reported in Chapter 3) and a larger current adjustment range leads to a greater increase of the operation area of the system as illustrated in Chapter 3. Both the CFC presented in this chapter and the one in Chapter 3 can be represented by the same average model, which leads to an analogous operational area increase. Finally, note that the voltage rating of the switches will depend on the chosen maximum capacitor voltage plus its voltage ripple.

Considering the structure of Fig. 5.1(b), which corresponds to current configuration 1 of Table 5.1, the same procedure to obtain the average model can be applied. The obtained voltage sources have the same expression than (5.7), which allows to represent both current configuration 1 and 2 with the same two voltage sources (see Fig. 5.6). Fig. 5.7 depicts the average model of the extended CFC topology (see Fig. 5.3) for the 6 different current configurations or CFC modes. It illustrates that in order to represent the 6 different converter operation modes, with its corresponding operating struc-

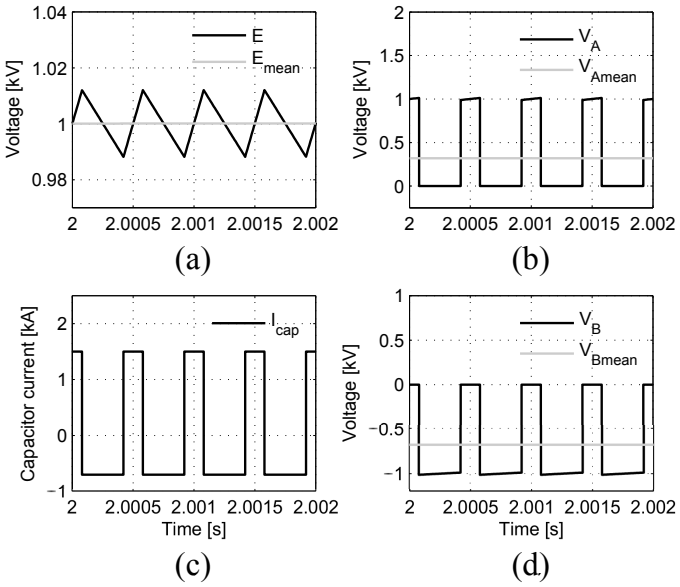

Fig. 5.5: CFC operation in mode 2 considering constant DC currents through lines A and B. (a) CFC voltage. (b) Voltage across switch S_1. (c) Current through the capacitor. (d) Voltage across switch S_2.

ture, 3 average models are required (each one with two voltage sources). These 3 models can be merged to represent the extended CFC topology. It must be noticed that only two voltage sources are acting simultaneously, as only one CFC structure is operating for a defined current configuration. In Fig. 5.7, D_{XY} and E_{XY} represent the duty cycle and the capacitor voltage of CFC modes X and Y, respectively. D_{12} is associated to the conduction time of switch S_1 (mode 2) and S_3 (mode 1). D_{34} is associated to the conduction time of switch S_9 (mode 4) and S_{11} (mode 3). D_{56} is associated to the conduction time of switch S_5 (mode 5) and S_7 (mode 6).

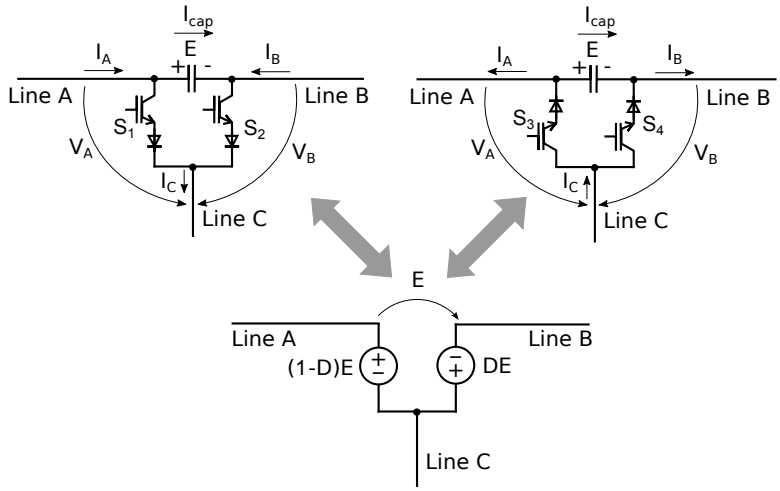

Fig. 5.6: Average model of the CFC considering current configurations 1 and 2.

5.4 Comparison between the proposed CFC topology and the dual H-bridge

5.4.1 Switch requirement for different current configurations

In this subsection, the layout of the presented topology is compared with the dual H-bridge introduced in [34] and further analysed in Chapter 3 and [36] and an analysis of the required switches for both topologies is provided. Fig. 5.8 shows four different layouts of both CFCs considering four different groups of current configurations of Table 5.1. Figs. 5.8(a), 5.8(c), 5.8(e) and 5.8(g) depict the dual H-bridge considering the required switches to be able to operate with the following four groups of current configurations: 2; 2 and

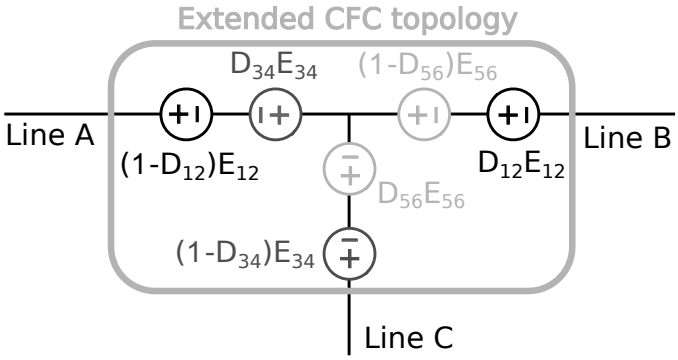

Fig. 5.7: Average model of the extended CFC topology for all the current configurations.

6; 2, 4 and 6; and 1 to 6, respectively. Figs. 5.8(b), 5.8(d), 5.8(f) and 5.8(h) illustrate the required switches considering the proposed CFC topology and the extended topologies according to the same current configurations.

Table 5.2 illustrates the number of diodes and IGBTs required for both topologies. It must be noticed that the number of IGBTs in each circuit is equal to the number of diodes in the same circuit.

Table 5.2: Comparison of the required diodes and IGBTs between the presented topology and the dual H-brigde CFC for different current configurations

Current config.	Presented topology	Dual H-bridge	Reduction
2	2	3	+1
2, 6	4	4	0
2, 4, 6	8	5	-3
All	12	6	-6

It can be seen that the presented topology can bring a reduction of the 33% of the switches compared to the dual-H bridge when a single current configuration in the CFC is expected. It has the same number of switches than the dual H-bridge when two current configurations are required. Although, when more than two current configurations are needed, the dual H-bridge may be a preferable solution due to the lower switch requirement. Consequently, the proposed CFC topology is more attractive when unidirec-

tional current flow is expected. It must be noticed that the previous analysis has been performed assuming that the reverse blocking voltage requirement of the IGBTs is ensured placing a diode in series in the presented CFC topology for sake of comparison. Nevertheless, considering switches with reverse blocking voltage capability, such as symmetrical IGCT, it would be possible to eliminate the need of diodes; while in the dual H-bridge, the diodes would still be required. However, it should be analysed if the reduction in diodes compensates some drawbacks of the symmetrical IGCTs such as the poorer thermal performance among others [83].

5.4.2 Unidirectional current flow topologies

In the previous subsection, it has been demonstrated that the proposed topology can bring a switch reduction for the unidirectional current flow structure comparing the proposed topology (see Fig. 5.8(b)) with the equivalent dual H-bridge for unidirectional current flow (see Fig. 5.8(a)). However, a deeper analysis is needed in order to identify advantages and disadvantages of the proposed unidirectional CFC concept.

On the one hand, the dual H-brigde has S_3' switching while S_1' and S_2' are used to select the voltage polarity to be applied on the lines (according to the methodology of Chapter 3) since the capacitor of the CFC is always charged with positive polarity, which allows using electrolytic capacitors. On the other hand, in the proposed CFC topology, S_1 and S_2 are switching in a complementary manner and it does not require additional switches because the voltage polarity to be applied on the lines is selected by charging the capacitor with positive or negative polarity. This implies that other sort of capacitors, able to handle both positive and negative voltage, must be considered.

Regarding the states of the switches, the dual H-bridge permits 8 states due to the higher number of switches, which can increase the controllability of the capacitor voltage. Nevertheless, the interesting states for current flow control are those that charge the capacitor with the current of one line and discharge it with the current of the other line (so that the CFC applies opposite effects on the lines as analysed in Chapter 3). Therefore, states that use both currents to charge or discharge the capacitor produce the same effect in both lines and do not contribute to the current flow control. The proposed CFC has only 4 states: two of them apply opposite effects on the lines (S_1 ON, S_2 OFF and S_1 OFF, S_2 ON) and are used for current flow control; S_1 and S_2 ON can be used to bring the capacitor voltage to 0 and the state with S_1 and S_2 OFF is not considered as it disconnects Line

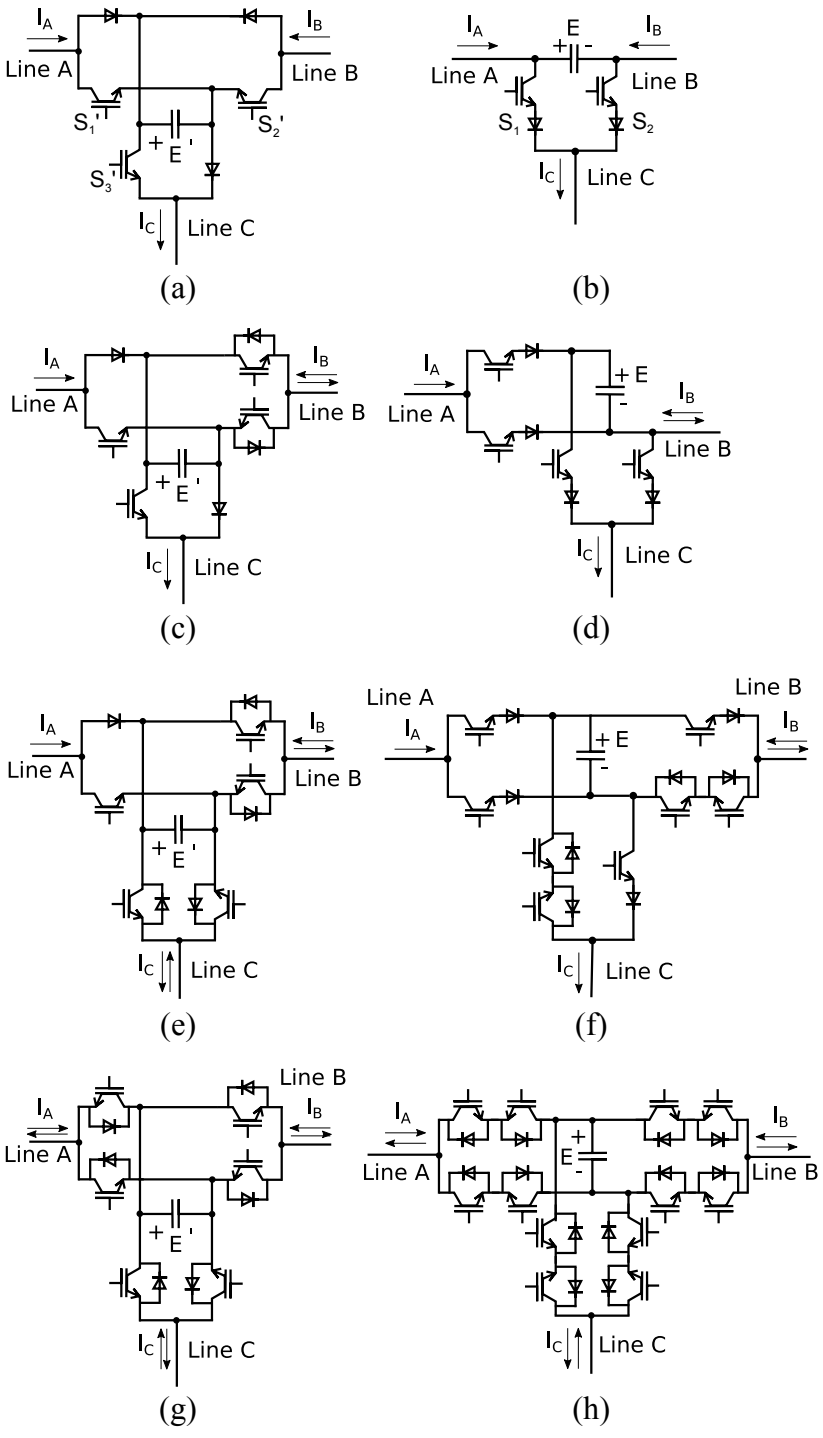

Fig. 5.8: Comparison between the presented topology and the dual H-brigde CFC for different groups of current configurations.

C from Line A and B.

One disadvantage of the proposed topology is that it does not incorporate a free wheel path for the current, while, in the dual H-bridge, the current can circulate through the diodes charging the capacitor when the IGBTs are open.

Table 5.3 summarizes the advantages and disadvantages of both topologies.

Table 5.3: Advantages and disadvantages of the proposed CFC and the dual-H bridge for unidirectional current flow

	Proposed CFC	Dual H-bridge CFC
Advantages	- Less switches (2 diodes 2 IGBTs) - Less states, simpler control - Simpler structure	- More states and control of the capacitor voltage - Capacitor with + polarity (electrolytic) - Free wheel path - 1 IGBT switching
Disadvantages	- Less control of the capacitor voltage - Capacitor with + and - polarity - No free wheel path - 2 IGBTs switching	- More complex control (voltage polarity selection) - More switches (3 diodes 3 IGBTs)

5.5 Operation of the extended CFC topology

5.5.1 Transitions between CFC modes

In this section, the transitions between CFC structures in the extended CFC topology are explained for sake of completeness. The extended CFC topology for all current configurations introduced in Section 5.2.2 is capable of switching from one current configuration to another, or what is equivalent, to invert one of the controlled currents. In order to do so, the converter must first null the current to be inverted. Besides, only transitions to invert one current each time are considered. For the following analysis, current I_A is considered to be the current coming directly from a VSC terminal in the HVDC grid. Therefore, the CFC has no capability to change the direction

of this current as it is related to the power injected into the HVDC grid. Based on this, the transition scheme is divided into two groups considering either the current I_A positive or negative, which are analogous. Fig. 5.9 depicts the transition scheme between CFCs modes considering I_A positive.

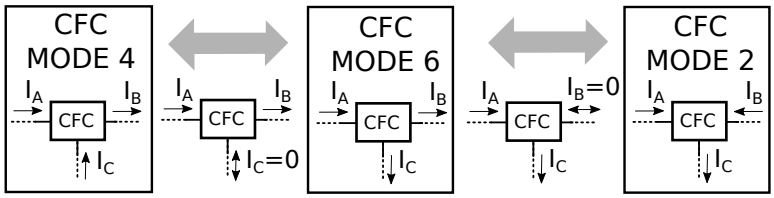

Fig. 5.9: Transition scheme between CFC modes 4, 6 and 2 considering $I_A > 0$.

Fig. 5.10 illustrates the layout and the operating switches of each mode and their transitions.

Assuming $I_A > 0$ and the converter operating in mode 4, S_9 and S_{10} are switching and S_3 and S_7 are closed. In order to go to CFC mode 6, the current to be inverted must be reduced to 0 (in this case I_C) by opening S_9. When S_9 is OFF, current flows transiently through the capacitor, charging it until its voltage level compensates the voltage difference between the DC grid nodes. As a result, the current from line C goes to 0. Then, the anti-parallel switch of S_3 (S_1) must be closed in order to allow current reversal and S_3 can be opened. After that, operation mode 6 can start by switching complementary S_7 and S_8. At this point, the capacitor voltage is different from 0 since it maintains the actual current flow. Once the CFC is in mode 6, it is able to reduce I_B. To null completely I_B, S_7 must open and then, once it is 0, S_{12} closes and S_{10} can be opened. After this procedure the converter can start operating with mode 2 by switching complementary S_1 and S_2. An analogous strategy can be used when the current I_A has a negative value.

5.5.2 Modulation strategy

The modulation is designed in order to allow the transitions between the different CFC modes depicted in Fig. 5.9 and Fig. 5.10 and it is presented considering the scenario where I_A is positive for simplicity. Nevertheless, the procedure is analogous for $I_A < 0$.

The modulation is based on a Pulse Width Modulation (PWM) that compares a global duty cycle D_g with three triangular waveforms placed one

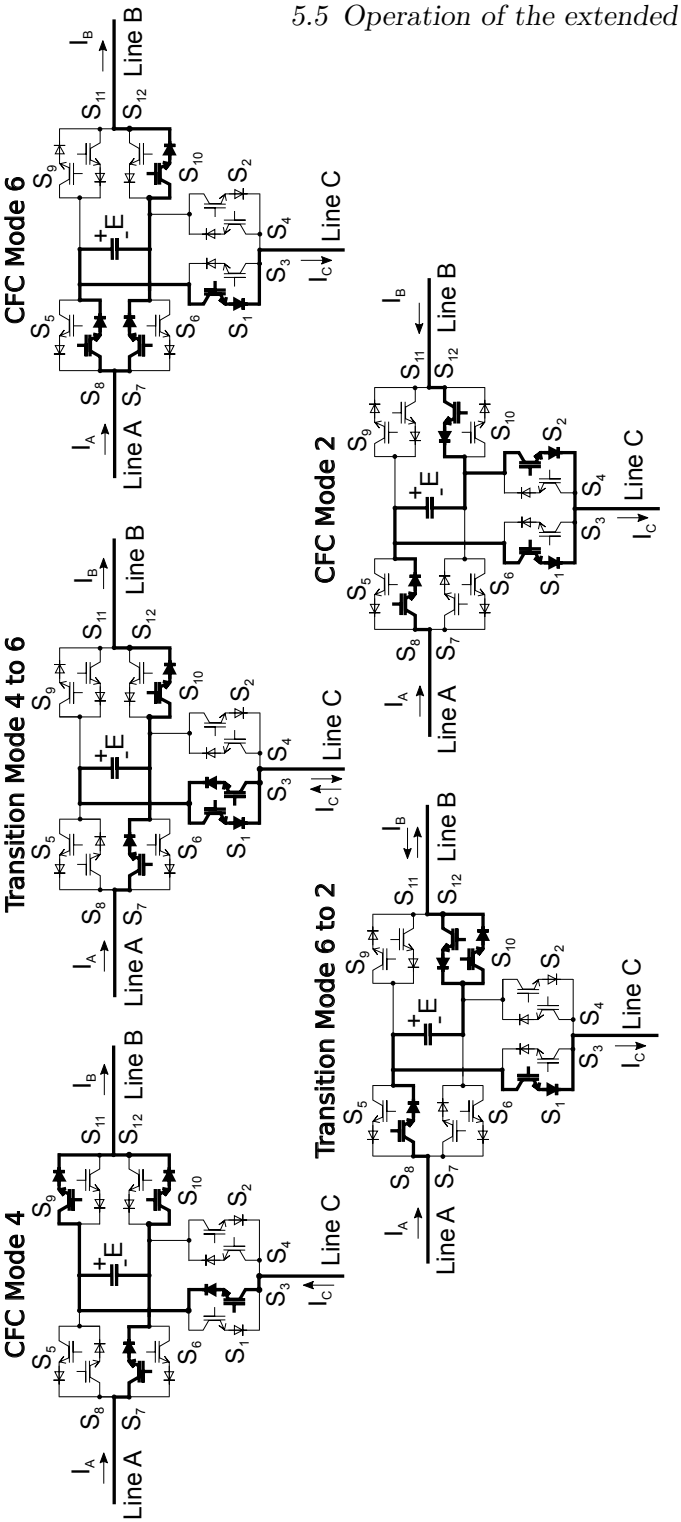

Fig. 5.10: Layout of the extended CFC topology for all current configurations considering transitions between modes 2, 4 and 6 with $I_A > 0$.

above the other. Each triangular waveform is associated to a CFC mode and generates a square waveform pulse that is sent complementary to the corresponding switches. By increasing or decreasing D_g is possible to control the DC current and perform the transitions between CFC modes. Fig. 5.11 depicts the modulation described before.

Besides, it is necessary to keep switch S_3 ON during CFC mode 4 ($1 < D < 2$) and S_{12} must be ON during mode 2 ($-1 < D < 0$) to ensure the right path for the current. The following expression relates the global duty cycle D_g with the specific duty cycles of each CFC mode depicted in Fig. 5.7.

$$D_{34} = D_g - 1 \quad D_{56} = D_g \quad D_{12} = D_g + 1 \tag{5.8}$$

The logic implementation described above is illustrated in Fig. 5.12. Additionally, the extended CFC must be able to get bypassed in case of need. Table 5.4 shows the switch states to bypass the device.

Table 5.4: Switch states during CFC bypass

	S_1, S_3, S_5, S_8, S_9, S_{11}	S_2, S_4, S_6, S_7, S_{10}, S_{12}
Option 1	ON	OFF
Option 2	OFF	ON

5.6 CFC protection under DC fault conditions

The CFC is a reduced converter that must be protected during abnormal conditions, such as DC faults. Fig. 5.13 shows a schematical diagram of the CFC in presence of a DC fault in Cable 1. Besides, it also illustrates the required additional equipment in order to ensure the safety of the CFC. Considering a DC fault in Cable 1, according to Fig. 5.13, the DC current flowing through that line will increase in a rate of change that will depend on the inductance of the Cable 1 and the reactor L_{lim}. This current can easily reach few kA before the protective action of the DC breaker opens the circuit [59] and it will charge the CFC capacitor so that the CFC switches will suffer the corresponding overvoltage. Neither the CFC switches nor the capacitor are rated to withstand this amount of current or for the overvoltage due to the capacitor charge. Therefore, Fig. 5.13 shows a possible protection scheme in order to bypass the CFC and divert the fault current. The protective

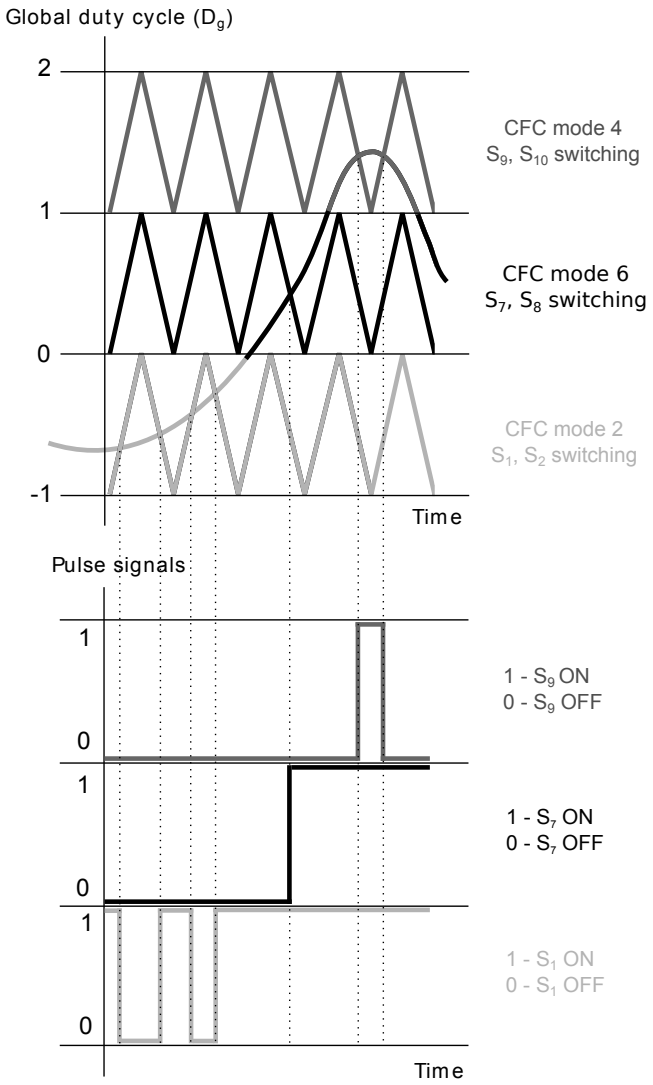

Fig. 5.11: Modulation strategy for the extended CFC topology for CFC modes 2, 4, 6.

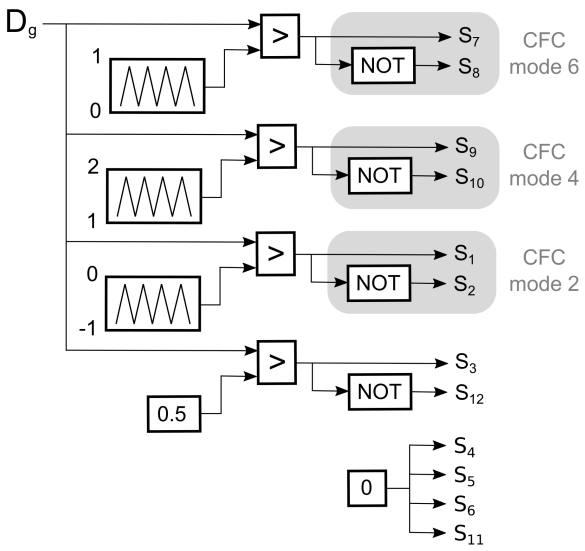

Fig. 5.12: Modulation and switch selection logic for the extended CFC topology considering modes 2, 4 and 6.

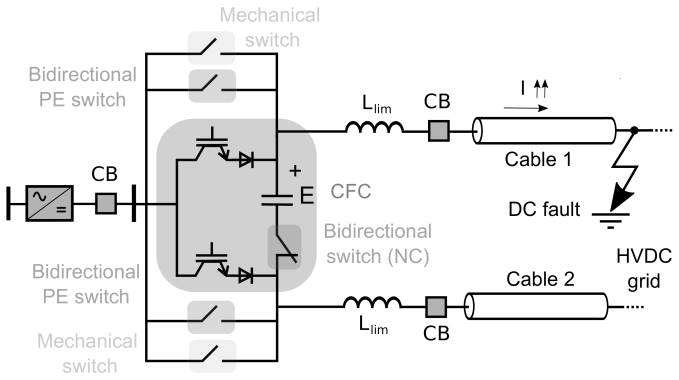

Fig. 5.13: Scheme of the CFC and the protection equipment considering a DC fault in Cable 1.

equipment is composed of two sets of bidirectional switches connected in parallel in order to bypass the CFC and a bidirectional switch normally closed (NC) in series with the capacitor. This NC switch should be opened whenever the DC fault happens in order to isolate the capacitor and must be coordinated with the CFC switches to allow always a path for the current. Then, the first set of bypass switches based on power electronics (with high current capability and with fast turn ON time) can be activated without short-circuiting the capacitor. A second set of mechanical switches (with slower turn ON time and lower losses) can be introduced in order to bypass the CFC after the activation of the first set or even to bypass the CFC when its operation is not required. In case of considering the CFC switches rated for the fault current, the bidirectional switches based on power electronics could be omitted.

The control references for the CFC to regulate the DC currents should come from a centralised control in charge of regulating the whole HVDC grid. Therefore, in case of DC faults in other locations or AC faults at converter stations, the local current CFC references must be updated by the centralised control in order to prevent the CFC of applying an effect that could overload one of the lines.

5.7 5-terminal meshed HVDC grid for CFC validation

In this section, a 5-terminal HVDC grid is presented to validate the CFC operation. It is composed of 5 two-level VSC nodes connected through DC cables and it is depicted in Fig. 5.14. Three DC circuit breakers (CB) are placed in the HVDC grid to isolate two different areas in case of a fault. The CFC is located in node 1, before the CBs and connected to cables 41 and 51. According to Fig. 5.1, line A corresponds to node 1 and line B and C, correspond to cables 41 and 51, respectively. The VSC terminals are operating with the control scheme presented in [67] with a voltage droop control and an inner power loop with a time constant τ_i [67]. E_i^* is the voltage reference for the droop control, k_{di} is the droop constant and P_i^* is the power setpoint of node i.

5.7.1 5-terminal meshed HVDC grid modelling

The meshed HVDC grid is modelled considering only the upper half of the symmetrical monopole. For this reason, only the CFC of the positive pole is modeled and included in the system. The DC cables are modelled based on the equivalent PI model with parallel series branches presented in [84].

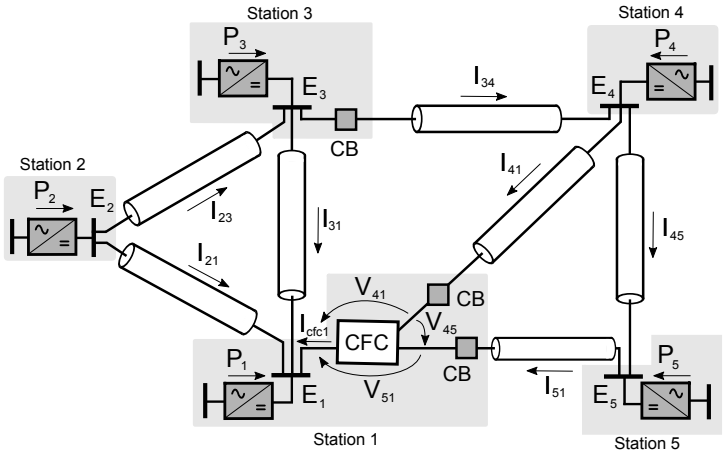

Fig. 5.14: 5-terminal meshed HVDC grid used for CFC validation.

Its parameters are extracted from [85] and the model is shown in Fig. 5.15. The DCCBs are represented as a series inductance (L_{lim} = 0.1 H) and a parasitic resistance (R_{lim} = 0.0446 Ω) according to the values of [59] and [5]. The parameters of the cable and the system are illustrated in Table 5.5

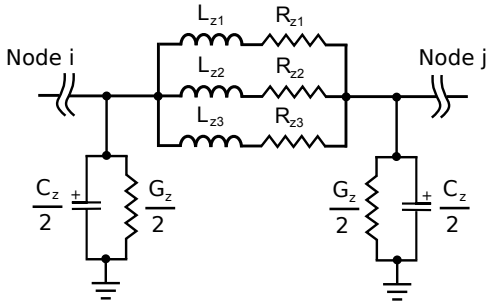

Fig. 5.15: DC cable model with parallel series branches.

and Table 5.6, respectively.

5.8 CFC control design

In this section, the control of the complete CFC structure is addressed, which is based on the approach presented in Chapter 3. The controller scheme is based on an inner voltage loop and an outer current loop, which is depicted in Fig. 5.16. The inner voltage loop allows to regulate the capacitor voltage of

Table 5.5: Cable model parameters

Parameter	Value	Unit	Parameter	Value	Unit
R_{z1}	$1.1724 \cdot 10^{-1}$	Ω/km	L_{z1}	0.22851	mH/km
R_{z2}	$8.2072 \cdot 10^{-2}$	Ω/km	L_{z2}	1.5522	mH/km
R_{z3}	$1.1946 \cdot 10^{-2}$	Ω/km	L_{z3}	3.2942	mH/km
G_z	$7.633 \cdot 10^{-11}$	S/km	C_z	0.1983	µF/km

Table 5.6: HVDC grid parameters

Cable ij	23	21	31	34	41	45	51
Distance d_{ij} [km]	100	80	120	100	100	120	120
Node i			1	2	3	4	5
Power reference P_i^* [MW]			1000	800	−400	−200	−1200
Voltage reference E_i^* [kV]					310		
Power loop time constant τ_i [ms]					25		
Droop constant k_i^* [MW/kV]					40		

the CFC and keep it below the maximum value according to the rating of the switches. The outer current loop allows the control of the line currents I_{41} or I_{51}. $K_c(s)$ is based on a Proportional-Integral (PI) controller and $K_e(s)$ is composed of a PI and a second order compensator, whose structures are shown in (5.9-5.10) and their parameters in Table 5.7, considering voltages and currents measured in volts and amperes, respectively.

To provide a smooth start-up, both voltage and current controllers must be correctly initialized. Firstly, the CFC will be bypassed and the output of the voltage controller must be initialized at the duty cycle corresponding to the current relation of (5.3), also called Neutral Duty Cycle (NDC). Besides, the voltage reference E^* must be 0 V. When the CFC starts to operate with the NDC it will maintain a mean voltage in the capacitor of 0 V, while it is not applying any change in line currents. Secondly, the voltage reference can be switched to the ouput of the current controller with the output initialized at 0 V in order to start the current regulation.

$$K_c(s) = \frac{k_{pc}s + k_{ic}}{s} \tag{5.9}$$

$$K_e(s) = \left(\frac{k_{pe}s + k_{ie}}{s}\right)\left(\frac{a_2s^2 + a_1s + a_0}{b_2s^2 + b_1s + b_0}\right) \tag{5.10}$$

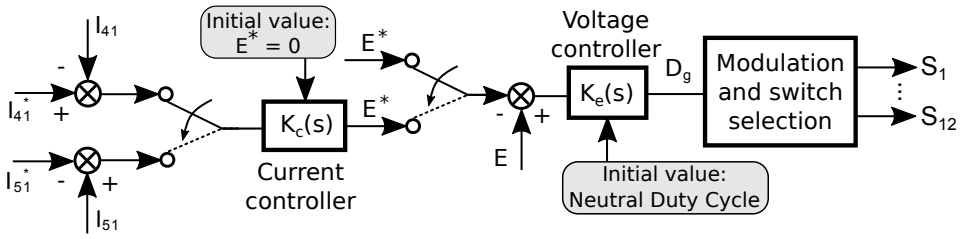

Fig. 5.16: CFC control scheme with a inner voltage loop and an outer current loop.

Table 5.7: Control parameters

k_{pc}	k_{ic}	k_{pe}	k_{ie}	a_2	a_1	a_0	b_2	b_1	b_0
5.08	21.93	0.03	1.03	0.01	0.08	0.85	1	48.35	151.81

5.9 Simulations results

In this section, the following case studies are presented to validate the operation of the CFC considering the meshed HVDC grid described in Section 5.7. The switching model of the extended CFC topology for all current configurations of Section 5.2.2 is considered for simulations. The base values for grid power, voltage and current are: 1200 MW, 320 kV and 1875 A, respectively. The base voltage value for the CFC is 4 kV.

5.9.1 CFC start-up

In this case, the CFC start-up is presented considering the CFC operating with mode 6 and the results are depicted in Fig. 5.17. The CFC is initially bypassed considering option 1 in Table 5.4 until $t = 1.5$ s. Then, the CFC starts to control the voltage of the capacitor to 0 V, applying the NDC. Fig. 5.17(b) shows how the capacitor is being charged and discharged with I_{41} and I_{51}, respectively, after $t = 1.5$ s. During this time, the CFC is operating but without changing the grid currents (see Fig. 5.17(a)) since the applied voltage on the grid is 0 V as it can be seen in Fig. 5.17(d). After $t = 3$ s, the current controller is enabled and the CFC starts to regulate I_{51} to -0.4 pu. It can be seen that the capacitor voltage E reaches a value close to -0.3 pu and the mean voltages V_{41} and V_{51} correspond to the values of the average model in (5.7). Fig. 5.17(c) illustrates the general duty cycle of the CFC, D_g, which changes in order to achieve the reference value of I_{51}.

5.9.2 CFC increasing, nulling and inverting I_{51}

In this case study, the CFC is used to increase I_{51} following its reference I_{51}^* and the transition from mode 6 to 4 is illustrated. In Fig. 5.18, the variables concerning both the CFC and the meshed HVDC grid are depicted. Initially, the CFC is operating with mode 6 and it starts to increase I_{51} (see Fig. 5.18(a)). Fig. 5.18(b), 5.18(d) and 5.18(f) show how the grid currents, node voltages and node powers are affected by the CFC operation, respectively. The effect among grid currents is considerable, but powers and voltages are rather constant. The global duty cycle D_g increases according to (5.8) and $D_{56} = \frac{I_{41}}{I_{51}+I_{41}}$ as it can be seen in Fig. 5.18(e) since I_{41} is also increasing in absolute value. The capacitor is charged negatively (Fig. 5.18(c)) and the mean voltages applied to the grid are depicted in Fig. 5.18(g), where V_{45} corresponds to the capacitor voltage. The shaded area in grey illustrates the zone where the CFC is passing from mode 6 to mode 4 by nulling I_{51}.

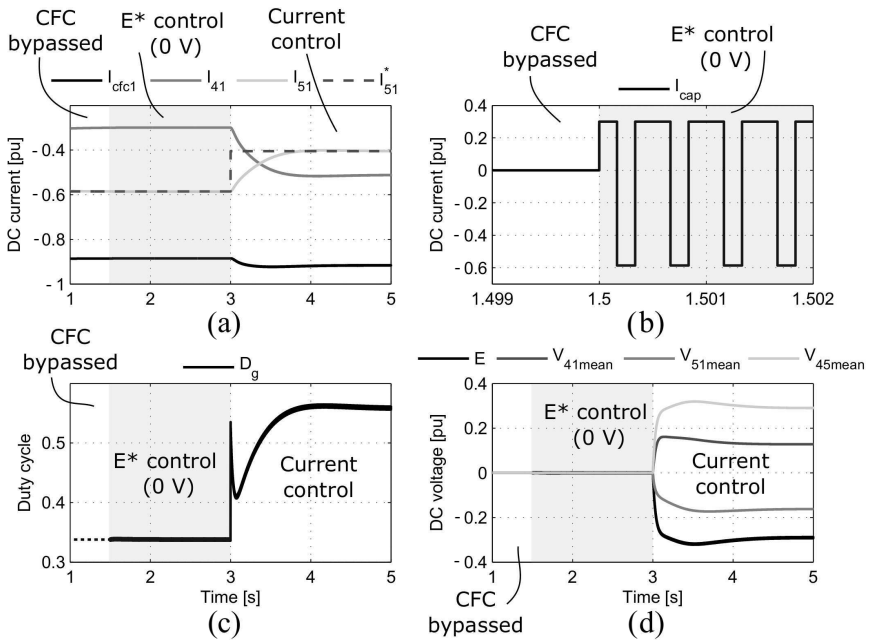

Fig. 5.17: CFC start-up procedure. (a) CFC currents. (b) Current through the CFC capacitor. (c) CFC duty cycle. (d) Applied mean voltages by the CFC.

The global duty cycle achieves a value of 1, and all the current I_{cfc1} goes through cable 41. After this zone, the CFC works with mode 4, so that I_{51} changes its direction and the CFC voltage gets more negative. In this case, the mean voltage applied by the CFC V_{51} corresponds to the capacitor voltage E. It can be noticed that after changing the CFC mode, I_{41} is no longer decreasing when I_{51} is increasing, which is due to the fact that the CFC equivalent model is different from the one of mode 6.

5.9.3 CFC increasing, nulling and inverting I_{41}

This case study presents the CFC operation from mode 6 to mode 2. In this situation, current I_{41} is increased until it gets a value of 0 A, and then it is inverted. Fig. 5.19 illustrates the variables concerning the CFC and the meshed HVDC grid. In this case, the CFC is applying the opposite effect to the grid, so that, D_g decreases according to the relation $D_{56} = \frac{I_{41}}{I_{51}+I_{41}}$, and the capacitor voltage increases. The shaded area also depicts the transition zone between CFC mode 6 and mode 2, where I_{41} has been nulled. In this situation, D_g is 0, which means that D_{12} is 1, thus, switch S_1 is in ON state. After the transition, the CFC operates with mode 2, and I_{41} changes its direction and continues rising following the reference. D_g achieves negative values according to the presented modulation strategy and the CFC voltage keeps rising. Fig. 5.19(g) shows the applied mean voltages for the CFC, and in mode 2, V_{41} corresponds to the capacitor voltage. The CFC is operating with S_1 and S_2 during mode 2 (see Fig. 5.19(h)).

5.9.4 CFC operation during power flow change

This case study shows the behaviour of the CFC when it is regulating current I_{51} and the current flow within the HVDC grid is modified due to power changes in the nodes. The results are depicted in Fig. 5.20. The CFC is operating with mode 6 and after $t = 1.5$ s it starts to control I_{51} to -0.35 pu (see Fig. 5.20(a)). At $t = 3$ s, the power setpoint of node 5 is modified from -0.42 pu to -0.19, which leads to a different power flow within the DC grid (Fig. 5.20(a) and 5.20(b). The CFC continues regulating I_{51} and keeps it to the reference value after a transient of approximately one second. It can be seen in Fig. 5.20(e) that duty cycle suffers a transient as well, and achieves a new value according to the relation of grid currents. Fig. 5.20(c), shows that the CFC voltage goes from a negative value to a positive one as the effect that the CFC has to apply is the opposite compared to the previous current flow. The droop control in converter nodes slightly modifies the

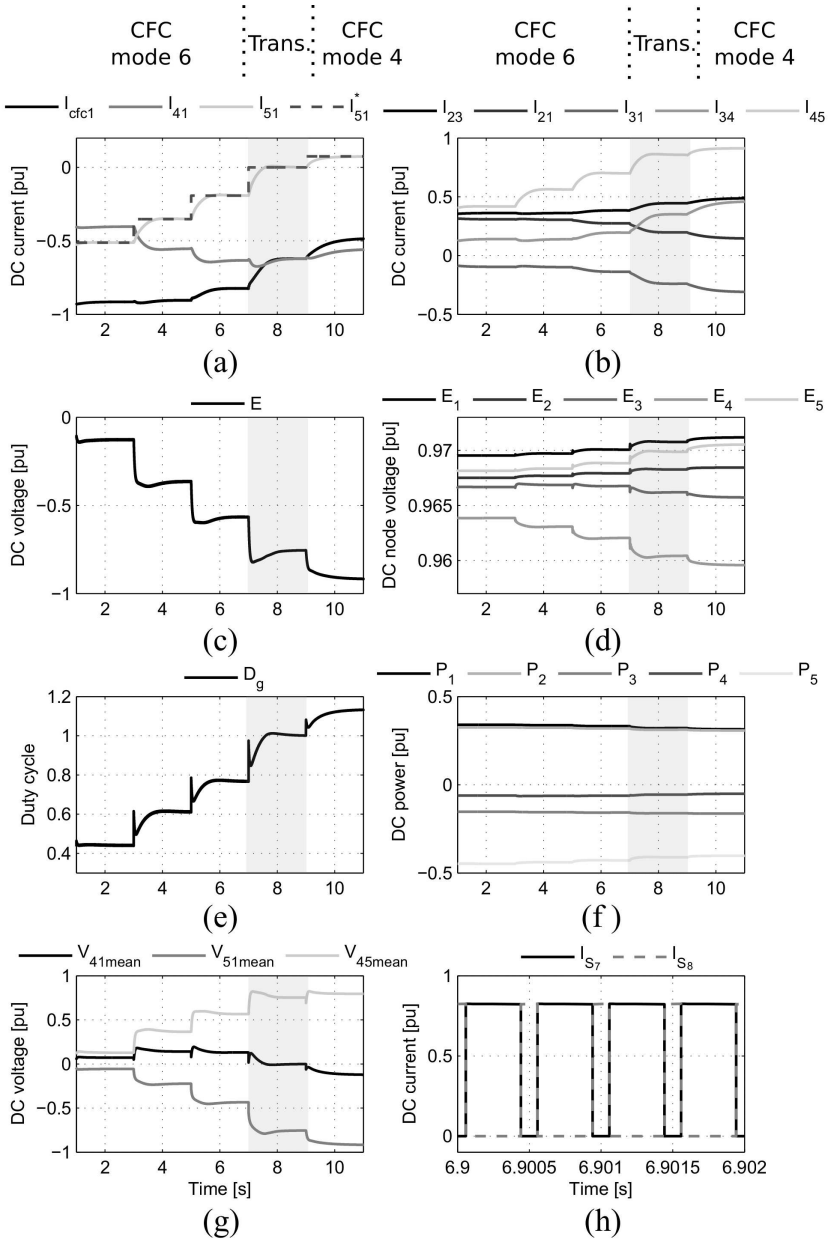

Fig. 5.18: CFC increasing, nulling and inverting I_{51}. (a) CFC currents. (b) DC grid currents. (c) CFC voltage. (d) Node voltages. (e) CFC duty cycle. (f) Node powers. (g) Applied mean voltages by the CFC. (h) Currents through switches S_7 and S_8.

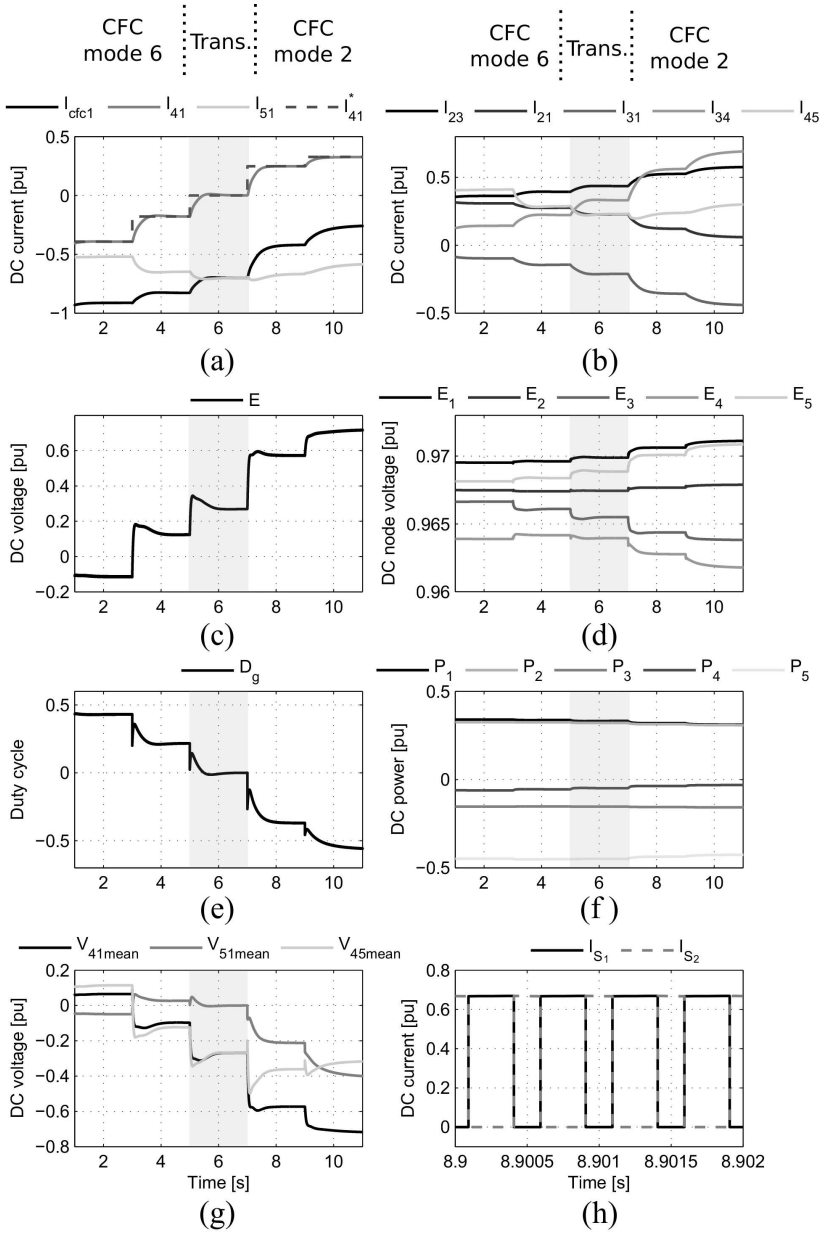

Fig. 5.19: CFC increasing, nulling and inverting I_{41}. (a) CFC currents. (b) DC grid currents. (c) CFC voltage. (d) Node voltages. (e) CFC duty cycle. (f) Node powers. (g) Applied mean voltages by the CFC. (h) Currents through switches S_1 and S_2.

node voltages to balance the new power flow (see Fig. 5.20(d)). Finally, at $t = 5$ s, the power setpoint of node 4 is changed from -0.08 pu to -0.25 pu, leading to a new power flow while the CFC is able to keep I_{51} constant after a minor transient.

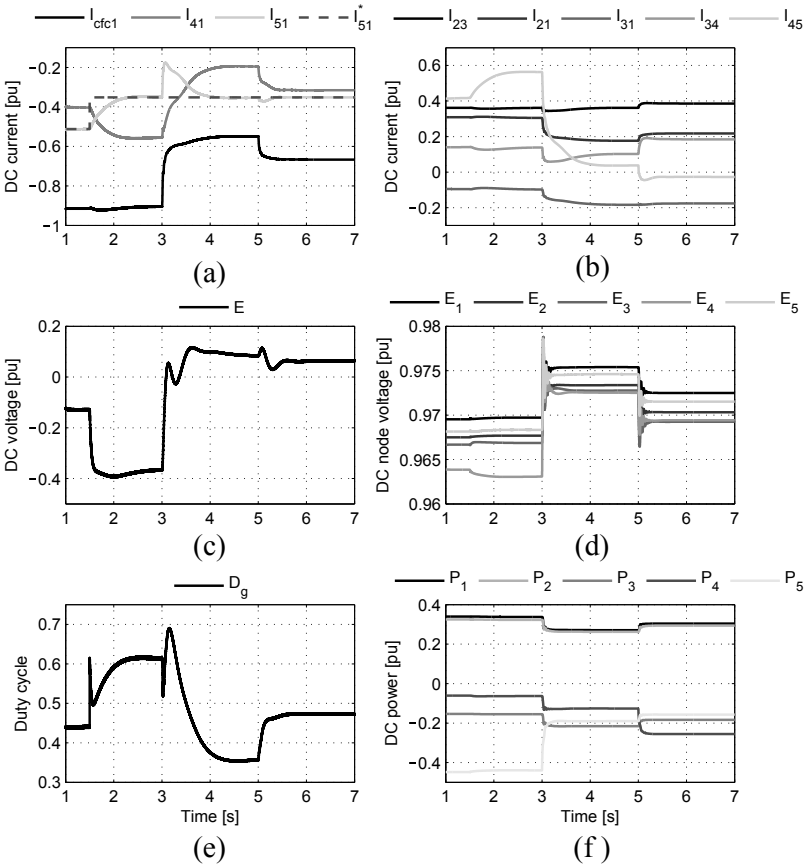

Fig. 5.20: CFC operation during a power change in node 5. (a) CFC currents. (b) DC grid currents. (c) CFC voltage. (d) Node voltages. (e) CFC duty cycle. (f) Node powers.

5.10 Experimental validation

5.10.1 System description

An unidirectional CFC prototype for low voltage is built and tested in an experimental platform illustrated in Fig. 5.21. The platform represents a DC grid composed of three terminals connected via the DC side forming a meshed DC grid. Each terminal consists of a cabinet as shown in Fig. 5.22, which contains an AC transformer, a two-level three-phase VSC with its control board and several measuring boards and data acquisition systems. The cables of the DC grid are physically emulated using a resistance and an inductance. The 3-port CFC is installed at the positive pole in Node 1, at the DC output of the cabinet and is depicted in Fig. 5.23. The device is made of two SiC MOSFETS included in two evaluation boards CRD-5FF0912P from CREE. The two SiC MOSFETs are then connected to the the PCB that contains the diodes and the capacitors of the CFC.

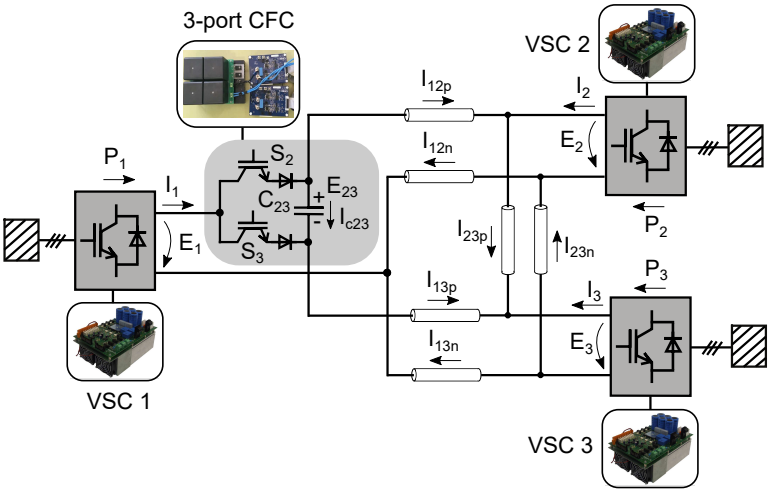

Fig. 5.21: Scheme of the experimental 3-terminal meshed DC grid with a 3-port CFC in the laboratory.

Tables 5.8, 5.9 and 5.10 show the parameters of the VSC, the DC lines and the CFC, respectively.

A monitoring system based in National Instruments (NI) Labview is also implemented in the experimental platform that acquires data regarding the DC voltages and currents of the DC grid. A NI cRIO 9024 controller is used to collect the data and send it to the monitoring PC.

Fig. 5.22: Image of the experimental platform, including the CFC and the three VSCs.

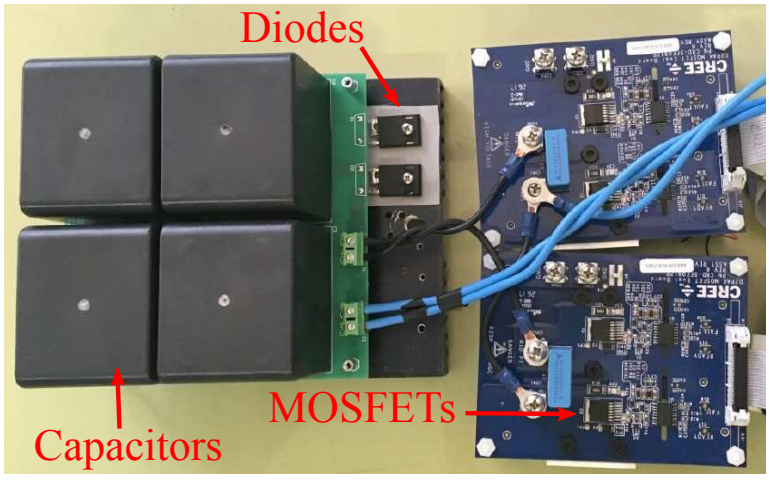

Fig. 5.23: Detail of the CFC converter.

Table 5.8: VSC parameters

Parameter	Value	Unit
DC voltage	±250	V
Nominal power	5.7	kW
AC voltage (l-l)	230	Vrms
AC inductors	1.6	mH
DC capacitance	1020	µF
Switching frequency	20	kHz

Table 5.9: DC line parameters

Parameter	Value	Unit
Resistance lines 12: R_{12p}, R_{12n}	3.2	Ω
Resistance lines 13: R_{13p}, R_{13n}	0.4	Ω
Resistance lines 23: R_{23p}, R_{23n}	0.7	Ω
Inductance lines 12: L_{12p}, L_{12n}	2.5	mH
Inductance lines 13: L_{13p}, L_{13n}	1.22	mH
Inductance lines 23: L_{23p}, L_{23n}	1.5	mH

Table 5.10: CFC parameters

Parameter	Value	Unit
Rated CFC voltage	±20	V
Rated DC current	11.4	A
CFC capacitance: C_{23}	1000	µF
Switching frequency	2	kHz

5.10.2 Control of the converters

Each of the VSCs of the scaled laboratory set up is controlled using a Digital Signal Processor (DSP) F28M35 of Texas Instruments (TI). Each VSC operates in voltage *droop* control [67], and uses the classic vector control in the *dq* reference frame for the current loop [67].

The control of the CFC is implemented in the same control board as VSC 1 and its scheme is illustrated in Fig. 5.24, which is based on the one proposed in Section 5.8 for the unidirectional CFC structure. As it can be seen in Fig. 5.24, the CFC has four control modes implemented: It can be bypassed, with both S_2 and S_3 in ON state; the duty cycle of both switches can be controlled directly using a ramp limiter; the CFC can also perform voltage control, by regulating the voltage of its capacitor; and finally, a current control of the DC lines is also implemented with an outer current controller and an inner voltage controller to limit the voltage that the CFC is applying.

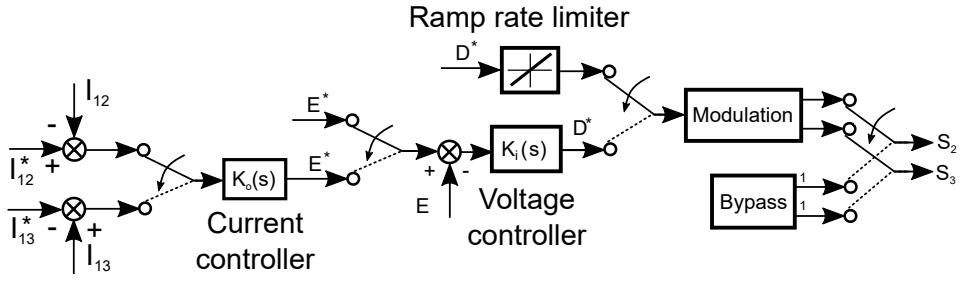

Fig. 5.24: Control scheme of the experimental 3-port CFC.

5.10.3 Experimental results

For all the tests performed in this section, the power that is being injected into the DC grid by VSC 1 is 4.7 kW and the powers extracted from the DC grid by VSC 2 and 3 are 2.1 kW and 2.3 kW, respectively.

Open-loop control

Fig. 5.25 and 5.26 depict the results considering the open-loop control of the CFC, where the duty cycle reference is given to the switches through a ramp rate limiter to avoid voltage and current transients.

At the beginning of the test, the duty cycle D_2 is zero, which implies that S_2 is OFF and S_3 is ON. All the current I_1 circulates through S_3 and line

13, and the capacitor is charged negatively. Then, the duty cycle reference changes from 0 to 1. This variation is applied through a ramp, and at the end the capacitor gets charged at 18 V and the current of line 13 is totally diverted into line 12.

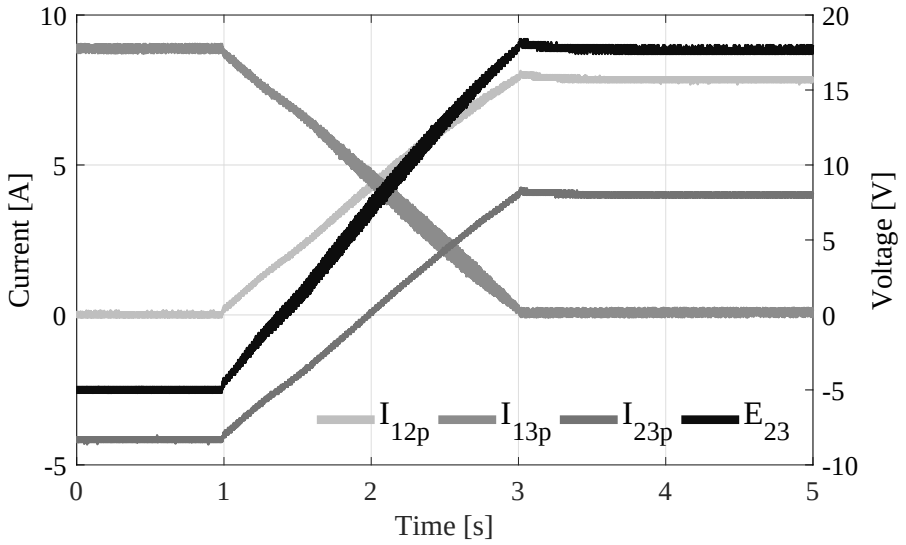

Fig. 5.25: Experimental results considering a ramped change of the duty cycle of the CFC in open-loop: Line currents and CFC voltage.

Fig. 5.26 depicts current I_{12p} and the voltages that the CFC is applying on the grid for a constant duty cycle of $D_2 = 0.5$. It can be seen that the voltage across the CFC capacitor, E_{23}, is a triangular waveform, showing the charge and discharge of the capacitor when the CFC is switching. The voltages applied on the lines are illustrated also in Fig. 5.26, showing that whenever the corresponding switch of the line is in ON state, the voltage is almost zero and when it is OFF, the voltage applied is the the voltage of the CFC capacitor (in positive or negative polarity depending on the switch). For such a low scale platform, the voltage drops across the switches play an important role as their value is considerable, around 1.5 V, as it was also reported in [39]. The average values of V_{12} and V_{13} correspond to the expressions $(1 - D_2)E_{23}$ and $-D_2E_{23}$, respectively, where its value is highly affected by the voltage drop. The mean values of the variables on the graphic are depicted below the legend.

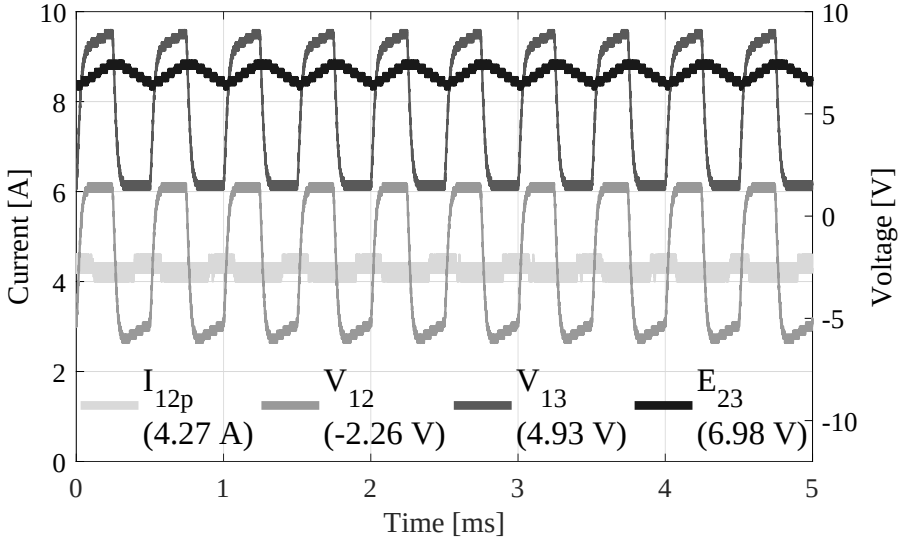

Fig. 5.26: Experimental results considering a constant duty cycle of $D_2 = 0.5$ in open-loop: Current I_{12p} and voltages applied by the CFC on the lines.

Closed-loop with voltage control

Fig. 5.27 illustrates the results using the voltage controller to regulate directly the voltage across the capacitor of the CFC.

Fig. 5.27 shows the results considering a closed-loop control for the CFC, where the voltage reference, E_{23}^{*} is given to the voltage controller whose output is the duty cycle of the switches. Initially, the voltage reference is zero, which means that the CFC is operating with the NDC, so that, it does not apply any change in the currents. Then, the voltage reference is changed to 10 V and the CFC achieves this value after 40 ms following a first order system response. Due to the charging of the capacitor, voltages are applied in series with the lines, which provokes a certain change in the line currents.

Closed-loop with current control

Finally, the closed-loop current control of the CFC is tested and the results can be seen in Figs. 5.28, 5.29 and 5.30. This control scheme includes an outer current controller and an inner voltage controller as it is shown in Fig. 5.24.

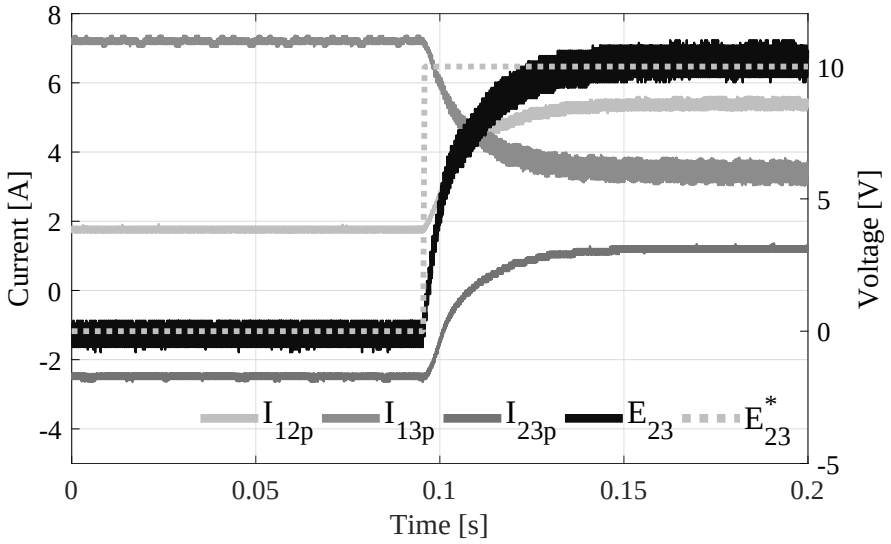

Fig. 5.27: Experimental results considering a voltage step change in closed-loop using the voltage controller: Line currents and CFC voltage.

Fig. 5.28 shows a current step change in current I_{12}, where initially, the current through line 12 is zero, and then achieves a value of 5 A. The CFC voltage also changes its value and is charged up to 10 V.

In Fig. 5.29, the current of line 12 is being controlled to 3 A, when, the power reference of VSC 2 goes from 2.5 kW to zero. The *droop* control implemented in each VSC compensates the unbalance in power, so that the powers from VSC 1, VSC 2 and VSC 3, end up being -3.9 kW, 0.5 kW and 3.1 kW, respectively. The line currents change their values according the new power flow, yet the CFC is able to maintain the current regulation of line 12 to 3 A, after the transient. It is possible to see in Fig. 5.29, that the voltage of the capacitor achieves a higher value to keep the current to the same level.

Fig. 5.30 is meant to illustrate the effect that the CFC located on the positive pole exerts on the negative pole of the grid.

The current I_{12p} is regulated at 4 A, and the capacitor charges up to 7.5 V to provide such change. The currents through the negative pole, I_{12n} and I_{13n} are not affected while the CFC is changing the currents in the positive pole. Only a small increase in the ripple of current I_{13n} can be observed due to the CFC operation.

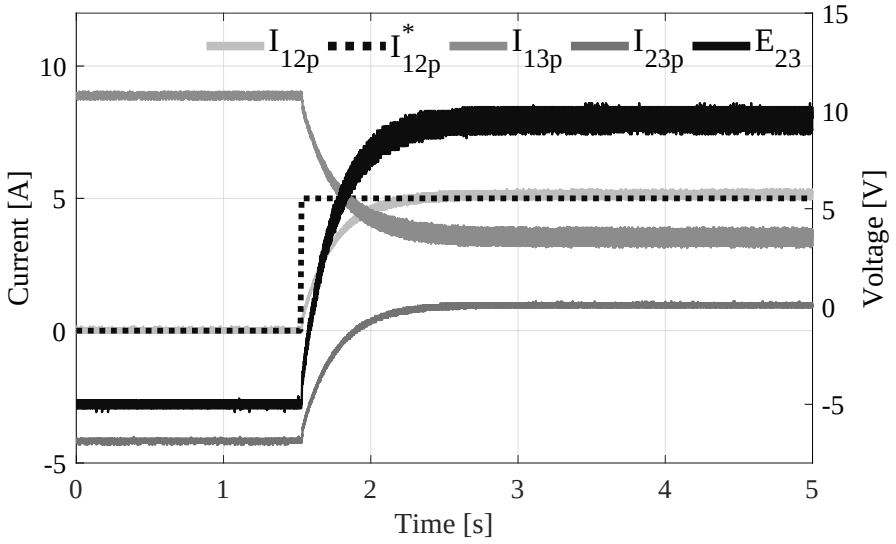

Fig. 5.28: Experimental results considering a current step change in closed-loop using the voltage and current controllers: Line currents and CFC voltage.

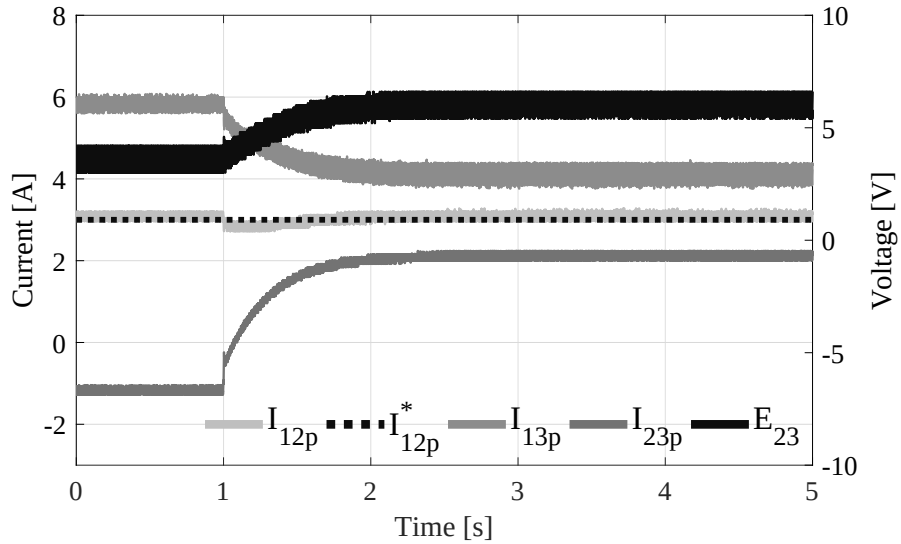

Fig. 5.29: Experimental results with current control and changes in the power of the nodes: Line currents and CFC voltage.

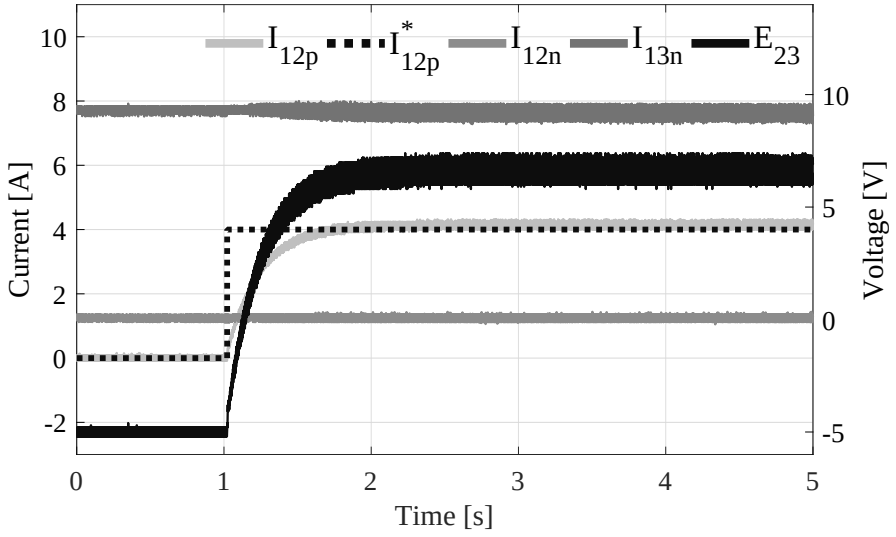

Fig. 5.30: Experimental results considering a current step change in closed-loop using the voltage and current controllers: Line currents of the positive and negative pole and CFC voltage.

5.11 Conclusion

A series interline DC/DC based CFC has been presented in this work, which requires less switches than the dual H-bridge CFC, when unidirectional current flows through the DC lines are expected. The average model of the CFC is derived and its operating principle explained. The advantages and disadvantages of the proposed topology are analysed showing that it has a simpler structure at the expense of not having a free wheel path and having two IGBTs switching, compared to the dual H-bridge, which incorporates a free wheel path and has an IGBT switching, with a more complex control, though. Additional CFC structures can be merged in the proposed circuit to deal with all the current configurations in the DC grid. This work also describes the operation and the modulation strategy for the extended CFC topology able to operate with all current configurations and outlines a protection equipment to ensure its safety when a DC fault occurs. A 5-terminal meshed HVDC grid is also modelled in order to test the CFC performance and the control scheme of the CFC is presented. Simulation results with the extended CFC topology show that the device is able to do a smooth start-up and also illustrate that it can control the currents through the DC lines to

the reference value. It can also null and invert DC currents and maintain current regulation during changes in the power flow. A scaled down unidirectional CFC has also been built and tested in a experimental platform in the laboratory. The tests shown that the CFC can be bypassed, operated in open-loop, performing voltage control and current control. It can also keep the current control during power changes in the nodes of the DC grid and if installed in the positive pole can only affect the currents of the positive pole.

Chapter 6

Selective operation of distributed current flow controller devices for meshed HVDC grids

6.1 Introduction

This chapter proposes a new Distributed CFC (DCFC) concept, which is based on using simplified CFC devices located in different nodes and operating them selectively. This concept was firstly introduced by the authors in the patent [82] and it is further extended, analysed and discussed in the present chapter. The DCFCs are operated selectively, one at a time, and the concept permits to use the most adequate DCFC for a given overload, which lets to control the currents with a lower CFC voltage. These DCFCs are based on the topology presented in Chapter 5 and [42] and its converter structure is derived after performing a steady-state and a sensitivity analysis. This work also presents an analysis methodology to investigate the effect of introducing DCFCs in different locations of an HVDC grid. Two case studies are considered: a thorough analysis in a 3-terminal grid with all the possible CFCs and another case study regarding a 7-terminal meshed HVDC grid. The increase in the operational area considering a 2B-CFC in one node and DCFCs in several nodes of a 3-terminal meshed grid are compared. Besides, the losses of DCFCs are calculated and compared depending on the location of the device inside the grid. The operation and control of the DCFCs is explained and tested using dynamic simulations in Matlab Simulink.

6.2 Distributed CFC concept

This chapter introduces the DCFC concept, where simplified CFCs located in different nodes in a meshed HVDC grid are operated selectively. Fig. 6.1(a)

depicts a 2B-CFC located in one node, while Fig. 6.1(b) illustrates the distributed approach, where several DCFCs are placed in different nodes of a generic meshed HVDC grid.

The DCFCs are used selectively depending on the location of the overloaded cable, allowing to avoid overloads where a single CFC in the grid is not able to, and reducing the CFC voltage requirement to modify the line currents.

This work considers the selective operation of the DCFCs in order to avoid certain interactions between CFCs that are connected to the same line as reported in [39]. In [39], a hierarchical control scheme is introduced to coordinate the operation of multiple 2B-CFC and avoid interactions. The DCFC concept considers the operation of only one DCFC at a time, but its structure is simplified compared to the 2B-CFC, in order to have a converter thought for specific current flow directions and less switches.

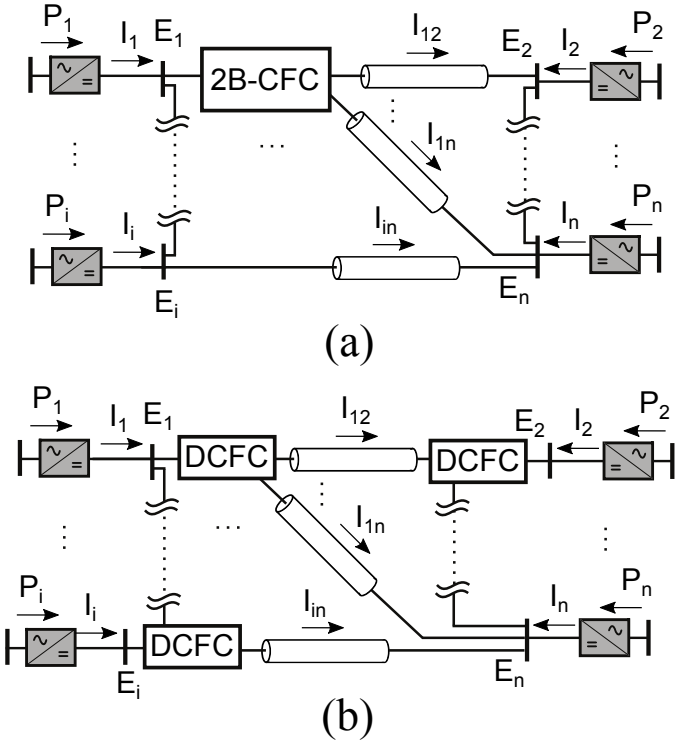

Fig. 6.1: n-terminal meshed HVDC grid. (a) 2B-bridge CFC located in node 1. (b) DCFCs in several nodes.

The base topology of CFC considered in this work to study the effect

among the meshed HVDC grid and develop the DCFC devices is the series interline DC/DC CFC presented in Chapter 5 and [42], which is illustrated in Fig. 6.2. As it can be seen in Fig. 6.2, it is a 3-port CFC connected to three different lines. The aforementioned topology brings some advantages compared to the 2B-CFC, introduced in [34] and further analysed in Chapter 3 and [36, 37, 39], when unidirectional current flow is considered.

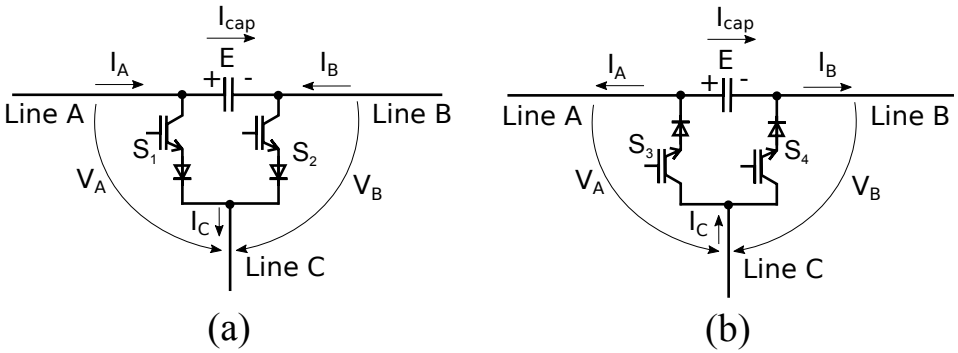

Fig. 6.2: Series interline DC/DC CFC for unidirectional current flow. (a) Two currents entering the device. (b) Two currents going out of the device.

6.3 Modelling of the CFCs and the meshed HVDC grid

6.3.1 CFC modelling

The unidirectional CFC under study is modelled using its average model obtained and described in Chapter 5. It consists on two voltage sources, which depend on the duty cycle applied to the switches of the CFC, D, and the average voltage of its capacitor, E. According to Fig. 6.2(a), D, is calculated as the time that S_1 is ON divided by the switching period. In Fig. 6.2(b), D expresses the time that S_3 is ON divided by the switching period. Notice that D can achieve values between 0 and 1. The average voltages applied on the DC grid by the CFC are:

$$V_A = (1 - D)E \qquad V_B = -DE \tag{6.1}$$

Fig. 6.3 shows the two unidirectional CFC structures presented before and the average model that represents both of them.

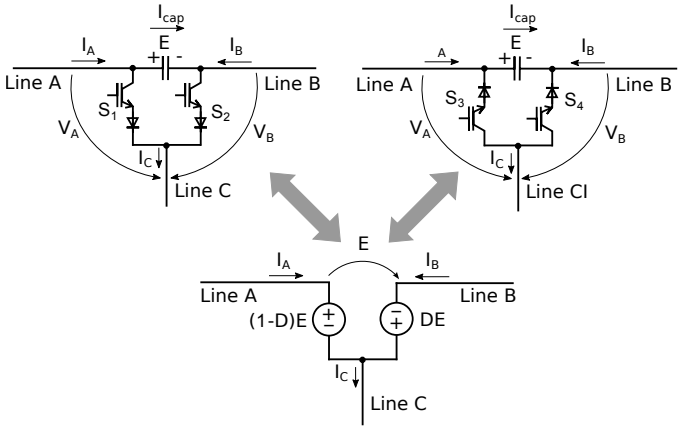

Fig. 6.3: Average model of the unidirectional CFC.

6.3.2 Meshed HVDC grid modelling

An n-terminal meshed HVDC grid as the one in Fig. 6.1(b) is used to present the methodology of the analysis. Fig. 6.4 depicts the model of the n-terminal meshed HVDC grid with three CFC average models located in nodes 1, 2 and i. For the steady-state study, cables are represented considering only their resistances and the half of the symmetric monopole is modelled due to its symmetry.

The average models included in the model neither represent all the CFCs to be installed in the grid nor are the most optimum configuration, they are included as an example to present the general methodology of the analysis. The average models are represented as a function of E_{iX} and D_{iX}, which are the average voltage of the CFC capacitor and the duty cycle of the CFC, respectively. The subscript i informs about in which node the CFC is located and X uses a letter to name the CFC according to how it is connected to the HVDC grid. Note, for instance, that the CFCs with *Line C* (see Fig. 6.3) connected directly to a VSC station are named A.

Assuming a general meshed HVDC grid as the one in Fig. 6.4, with n nodes, the equations describing its behaviour are illustrated below. Considering the node in the grid that operates as a DC slack bus, then:

$$E_{slack} - E^{*}_{slack} = 0 \tag{6.2}$$

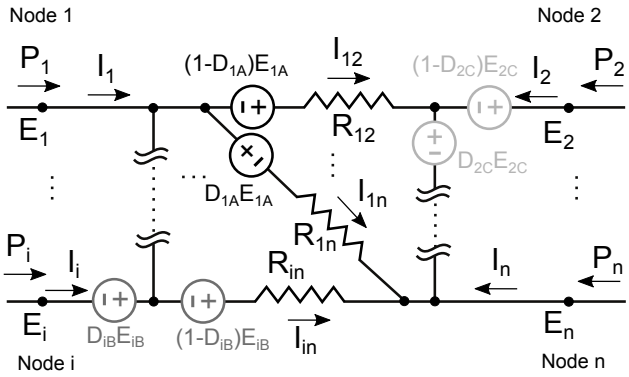

Fig. 6.4: Model of the n-terminal meshed HVDC grid with three CFC average models.

where, E_{slack} and E^*_{slack} are the real DC voltage and the reference DC voltage of the node in the HVDC grid that operates as a slack bus. If node i is injecting or extracting constant power from the DC grid is modelled as:

$$I_i - \frac{P_i^*}{E_i} = 0 \qquad \forall i \leq n \tag{6.3}$$

where, I_i and P_i^* are the real DC current and the power reference of node i. Note that, P_i^* correspond to the half of the total power that the real system would exchange, since only the half of the symmetric monopole is modelled.

Then, according to the cables depicted in Fig. 6.4 and Kirchhoff law:

$$I_i = \sum_{j=1}^{n} I_{ji} \qquad \forall i \leq n \tag{6.4}$$

where, I_{ji} is the current between node j and i. Each node j connected to node i adds a term in the equation with the corresponding sign. The node voltages and the voltage drop of the CFCs are related as:

$$\frac{1}{R_{12}}(E_1 + (1 - D_{1A})E_{1A} + (1 - D_{2C})E_{2C} - E_2) - I_{12} = 0 \tag{6.5}$$

$$\frac{1}{R_{1n}}(E_1 - D_{1A}E_{1A} - E_n) - I_{1n} = 0 \tag{6.6}$$

$$\frac{1}{R_{in}}(E_i + E_{iB} - E_n) - I_{in} = 0 \tag{6.7}$$

where, R_{ij} is the resistance of the cable connecting node i and j.

For each CFC included in the meshed HVDC grid, also an equation relating its duty cycle and the DC currents is required (see Chapter 5):

$$D_{1A}(I_{12} + I_{1n}) - I_{12} = 0 \tag{6.8}$$

$$D_{2C}(-I_{12}) - I_2 = 0 \tag{6.9}$$

$$D_{iB}(I_i - I_{in}) - I_i = 0 \tag{6.10}$$

6.4 Steady-state analysis

6.4.1 Analysis methodology

In order to analyse the effect of different CFCs in a meshed HVDC grid, the following methodology is proposed, which it is explained in detail using an example in Section 6.4.2:

(1) Define a meshed HVDC grid to study and include the CFCs in the desired locations to analyse its effect.

(2) Obtain the equations describing the system, as presented in Section 6.3.2, with all the CFCs that will be analysed.

(3) According to the DCFC concept, only one CFC is expected to be operating at any time. A new equation must be added into the model for the CFCs that are not analysed ($E_{kZ} = 0$), which cancels the effect of the CFC kZ in the analysis.

(4) Derive the equations of the meshed HVDC grid and the selected CFC (named with the subscript jY) as a function of the CFC voltage $\frac{\partial}{\partial E_{jY}}$.

(5) Solve the system of equations for a given duty cyle $0 \leq D_{jY} \leq 1$ of the selected CFC jY.

(6) Use the previous solutions to solve the system of equations of the derivatives for the same duty cycle D_{jY} in order to obtain the current sensitivity for the desired CFC.

6.4.2 Methodology example

(1) A 3-terminal meshed HVDC grid as depicted in Fig. 6.5(a) is used to present an example of the analysis methodology with a CFC in node 1. The average model of the CFC 1A is illustrated in Fig. 6.5(b).

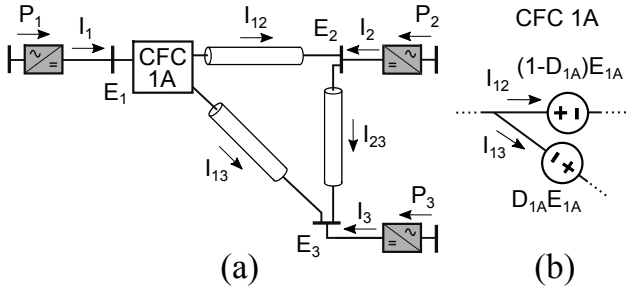

Fig. 6.5: 3-terminal meshed HVDC grid with a CFC. (a) Scheme of the meshed grid. (b) Average model of the unidirectional CFC in node 1.

(2) The model of the grid and the CFC is described by the following equations:

$$E_1 - E_1^* = 0 \tag{6.11}$$

$$I_2 - \frac{P_2^*}{E_2} = 0 \tag{6.12}$$

$$I_3 - \frac{P_3^*}{E_3} = 0 \tag{6.13}$$

$$I_1 - I_{12} - I_{13} = 0 \tag{6.14}$$

$$I_2 + I_{12} - I_{23} = 0 \tag{6.15}$$

$$I_3 + I_{13} + I_{23} = 0 \tag{6.16}$$

$$\frac{1}{R_{12}}(E_1 + (1 - D_{1A})E_{1A} - E_2) - I_{12} = 0 \tag{6.17}$$

$$\frac{1}{R_{13}}(E_1 - D_{1A}E_{1A} - E_3) - I_{13} = 0 \tag{6.18}$$

$$\frac{1}{R_{23}}(E_2 - E_3) - I_{23} = 0 \tag{6.19}$$

$$I_1 D_{1A} - I_{12} = 0 \tag{6.20}$$

By combining (6.15), (6.17) and (6.19) with (6.12) and combining (6.16), (6.18) and (6.19) with (6.13) leads to:

$$P_2^* = -\frac{E_1^* E_2}{R_{12}} + \frac{E_2 D_{1A} E_{1A}}{R_{12}} - \frac{E_2 E_{1A}}{R_{12}} + \frac{E_2^2}{R_{23}} - \frac{E_2 E_3}{R_{23}} \tag{6.21}$$

$$P_3^* = -\frac{E_1^* E_3}{R_{13}} + \frac{E_3 D_{1A} E_{1A}}{R_{13}} + \frac{E_3^2}{R_{13}} - \frac{E_2 E_3}{R_{23}} + \frac{E_3^2}{R_{23}} \tag{6.22}$$

(3) (4) The current sensitivity of the line currents is investigated by doing the partial derivative with respect to the capacitor voltage of the CFC, E_{1A}. The partial derivatives of (6.17)-(6.22) are:

$$\frac{1}{R_{12}}\left(1 - D_{1A} - \frac{\partial D_{1A}}{\partial E_{1A}} E_{1A} - \frac{\partial E_2}{\partial E_{1A}}\right) = \frac{\partial I_{12}}{\partial E_{1A}} \tag{6.23}$$

$$\frac{1}{R_{13}}\left(-D_{1A} - \frac{\partial D_{1A}}{\partial E_{1A}} E_{1A} - \frac{\partial E_3}{\partial E_{1A}}\right) = \frac{\partial I_{13}}{\partial E_{1A}} \tag{6.24}$$

$$\frac{1}{R_{23}}\left(\frac{\partial E_2}{\partial E_{1A}} - \frac{\partial E_2}{\partial E_{1A}}\right) = \frac{\partial I_{23}}{\partial E_{1A}} \tag{6.25}$$

$$\frac{\partial I_{12}}{\partial E_{1A}}(D_{1A} - 1) + \frac{\partial I_{13}}{\partial E_{1A}} D_{1A} + \frac{\partial D_{1A}}{\partial E_{1A}}(I_{12} + I_{13}) = 0 \tag{6.26}$$

$$\begin{aligned}\frac{\partial P_2^*}{\partial E_{1A}} &= \frac{E_2}{R_{12}}\left(\frac{\partial E_2}{\partial E_{1A}} + D_{1A} + \frac{\partial D_{1A}}{\partial E_{1A}} E_{1A} - 1\right) \\ &+ \frac{E_2}{R_{23}}\left(\frac{\partial E_2}{\partial E_{1A}} - \frac{\partial E_3}{\partial E_{1A}}\right) + \frac{1}{R_{23}}\left(\frac{\partial E_2}{\partial E_{1A}}(E_2 - E_3)\right) \\ &- \frac{1}{R_{12}}\frac{\partial E_2}{\partial E_{1A}}(E_{1A} + E_1^* - E_2 - D_{1A} E_{1A})\end{aligned} \tag{6.27}$$

$$\begin{aligned}\frac{\partial P_3^*}{\partial E_{1A}} &= \frac{1}{R_{13}}\frac{\partial E_3}{\partial E_{1A}}(E_3 - E_1 + D_{1A} E_{1A}) \\ &+ \frac{E_3}{R_{13}}\left(\frac{\partial E_3}{\partial E_{1A}} + \frac{\partial D_{1A}}{\partial E_{1A}} E_{1A}\right) - \frac{E_3}{R_{23}}\left(\frac{\partial E_2}{\partial E_{1A}} - \frac{\partial E_3}{\partial E_{1A}}\right) \\ &- \frac{1}{R_{23}}\frac{\partial E_3}{\partial E_{1A}}(E_2 - E_3)\end{aligned} \tag{6.28}$$

Assuming that the power of the nodes 2 and 3 is constant with respect to the voltage of the CFC yields to:

$$\frac{\partial P_2^*}{\partial E_{1A}} = 0 \qquad \frac{\partial P_3^*}{\partial E_{1A}} = 0 \tag{6.29}$$

(5) (6) Then, the current sensitivity with respect to the CFC voltage,

$\frac{\partial I_{12}}{\partial E_{1A}}, \frac{\partial I_{13}}{\partial E_{1A}}$ and $\frac{\partial I_{23}}{\partial E_{1A}}$, can be found solving numerically the system of equations from (6.23) to (6.28).

6.4.3 Case study 1: 3-terminal meshed grid with all possible CFCs

The methodology explained in Section 6.4.1 is applied to this case study, where the results of the steady-state analysis considering a 3-terminal meshed grid and CFCs in all the possible locations are presented (see Fig. 6.6). Note that for a given power flow, only a CFC average model is able to operate in each node due to the directions of the currents and the topology used (see Chapter 5). The following analysis is performed considering the parameters in Table 6.1.

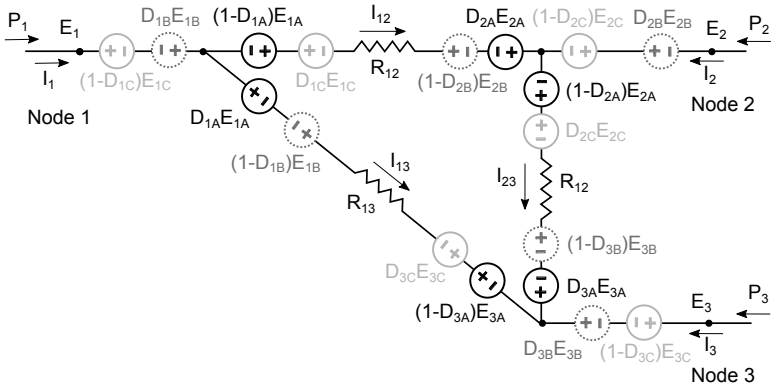

Fig. 6.6: Model of a 3-terminal meshed HVDC grid with all the possible CFC average models.

Fig. 6.7 shows the effect that the available CFCs bring among line currents, I_{12}, I_{13} and I_{23}, and the required CFC voltage, E_{jY}, to produce such an effect. The variables are illustrated as a function of the duty cycle applied to the CFC switches, D_{jY}. Considering the power flow in Table 6.1, the available CFCs to operate are 1A, 2C and 3A. The limits of each CFC operation are established considering that the duty cycle can go from 0 to 1, except if the maximum CFC voltage is exceeded, which is set at 4 kV. The vertical dashed line in each graphic depicts the Neutral Duty Cycle (NDC) which corresponds to the initial current relation when either there is no CFC or it is applying no effect in the DC grid. In such a situation the voltage of the CFC is 0 V (as seen in Chapter 5).

From Fig. 6.7, it can be seen that the CFCs with *Line C* connected to

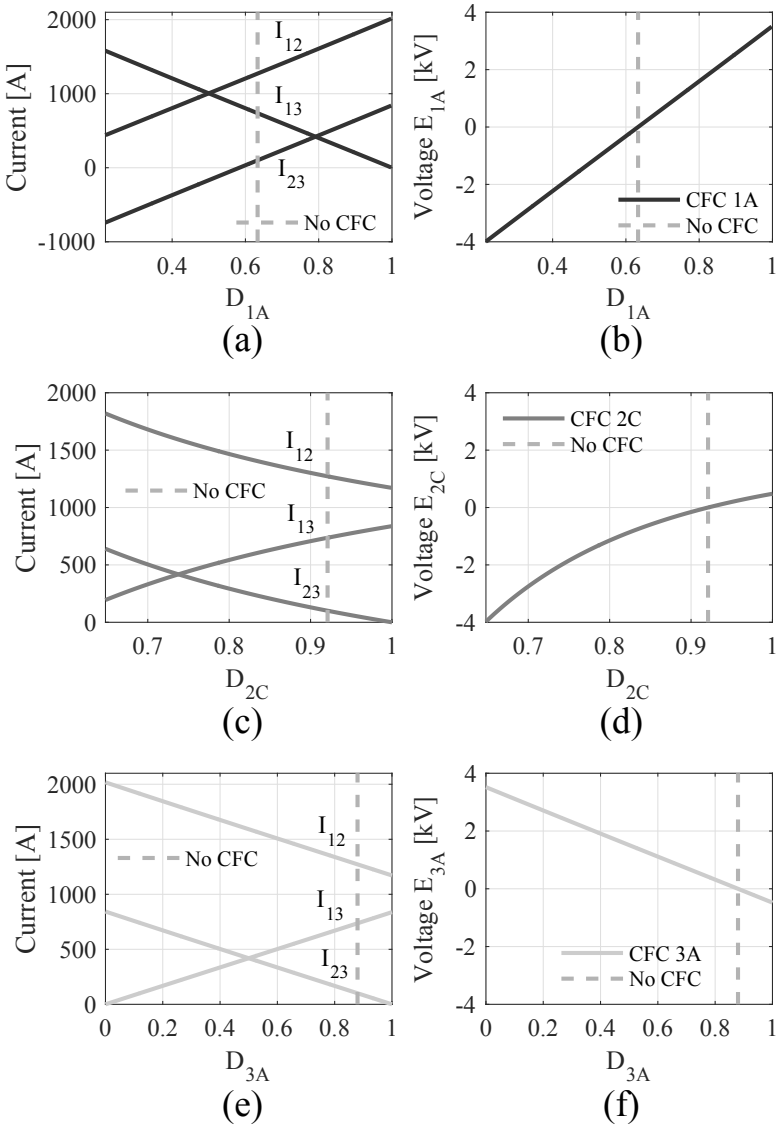

Fig. 6.7: Current variation and voltage requirement using different CFCs. (a) Current variation with CFC 1A. (b) Voltage requirement with CFC 1A. (c) Current variation with CFC 2C. (d) Voltage requirement with CFC 2C. (e) Current variation with CFC 3A. (f) Voltage requirement with CFC 3A

.

Table 6.1: Case Study 1: System Parameters

Node parameters	
E_1^* [kV]	300
P_2^* [MW]	-350
P_3^* [MW]	-250
Cable parameters	
Resistance [Ω/km]	0.0095
Cable length 12 [km]	100
Cable length 13 [km]	200
Cable length 23 [km]	200
CFC parameters	
Nominal voltage E [kV]	4

one VSC node (1A and 3A), show almost a linear relation between the line currents and the CFC voltage with respect to the duty cycle. However, CFC 2C depicts a non-linear dependence of the duty cycle. Analysing Fig. 6.6, it can be seen that the voltage sources of CFC 2C are placed in cable 23 and in the point where node 2 is connected to the DC grid. In such a situation, the CFC 2C could be used to modify currents I_{23} and I_2. Nonetheless, I_2 cannot be excessively changed as it is related to the power that node 2 absorbs or injects and it is beyond the capability of the CFC to regulate it. This applies for all the CFCs jB and jC which have a voltage source between the node connection and the DC grid. The previous analysis has been done considering different power flows to validate that the aforementioned behaviour applies for all the CFCs.

Fig. 6.8 shows the same information than Fig. 6.7 but comparing the effect of the different available CFCs among the line currents. A dashed line shows the initial values of line currents that also correspond when the CFCs are applying the NDC. The color bars illustrate the range of current in which the CFC can regulate the line currents. The limits are established considering the duty cycle range between 0 to 1 except when the CFC nominal voltage is exceeded. The voltages below and at the top of each bar show the associated CFC voltage of that current limit. Fig. 6.8 illustrates that the highest current variation is the one of CFC 1A, CFC 3A is the second and CFC 2C can bring the lowest current variation for all the line currents.

Fig. 6.9 shows the line currents and the line current sensitivities as a function of the CFC voltage for each available CFC. Fig. 6.9(a), 6.9(c) and 6.9(e)

show that CFC 1A or 3A can bring the same effect among line currents, besides of utilising the equal value of CFC voltage. The current variation range of CFC 1A is limited because I_{13} goes to 0 (see Fig. 6.9(c)) and due to the lower voltage limit (-4 kV). In the case of CFC 3A (grey dotted line), the variation range is lower compared to CFC 1A since I_{23} is reduced to 0 (see Fig. 6.9(e) around $E = -0.5$ kV). CFC 2C shows a less linear dependence of the CFC voltage compared to CFC 1A and 3A and its operation is also restricted before reaching the voltage limit because of the current reversal of I_{23}. On the one hand, regarding the current sensitivity of line currents (see Fig. 6.9(b), 6.9(d) and 6.9(f)), it can be seen that the current sensitivity for CFC 1A and 3A is almost constant when varying the CFC voltage. Its value is around 0.21 A/V for the three line currents. On the other hand, the current sensitivity of CFC 2C depicts a non-linear behaviour compared to CFCs 1A and 3A and a lower value than 0.21 A/V, except for a small range. These results show that the capability of CFC 1A and 3A to modify the current using the voltage is almost constant in all the operation points of the system, however, in the case of CFC 2C, this capability highly depends on the operation point and tends to be lower compared with 1A and 3A. This fact means that more CFC voltage is needed to produce the same current variation in the case of CFC 2C compared to 1A and 3A.

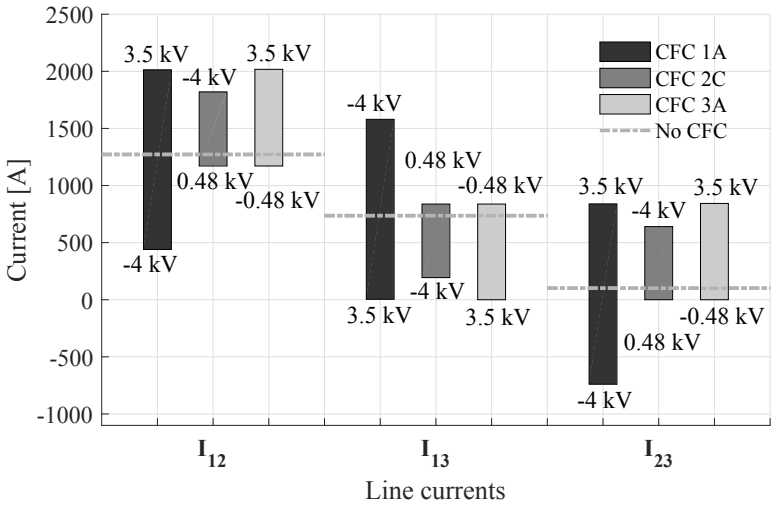

Fig. 6.8: Current variation range for different CFCs.

In order to evaluate the current variation with a single parameter, the

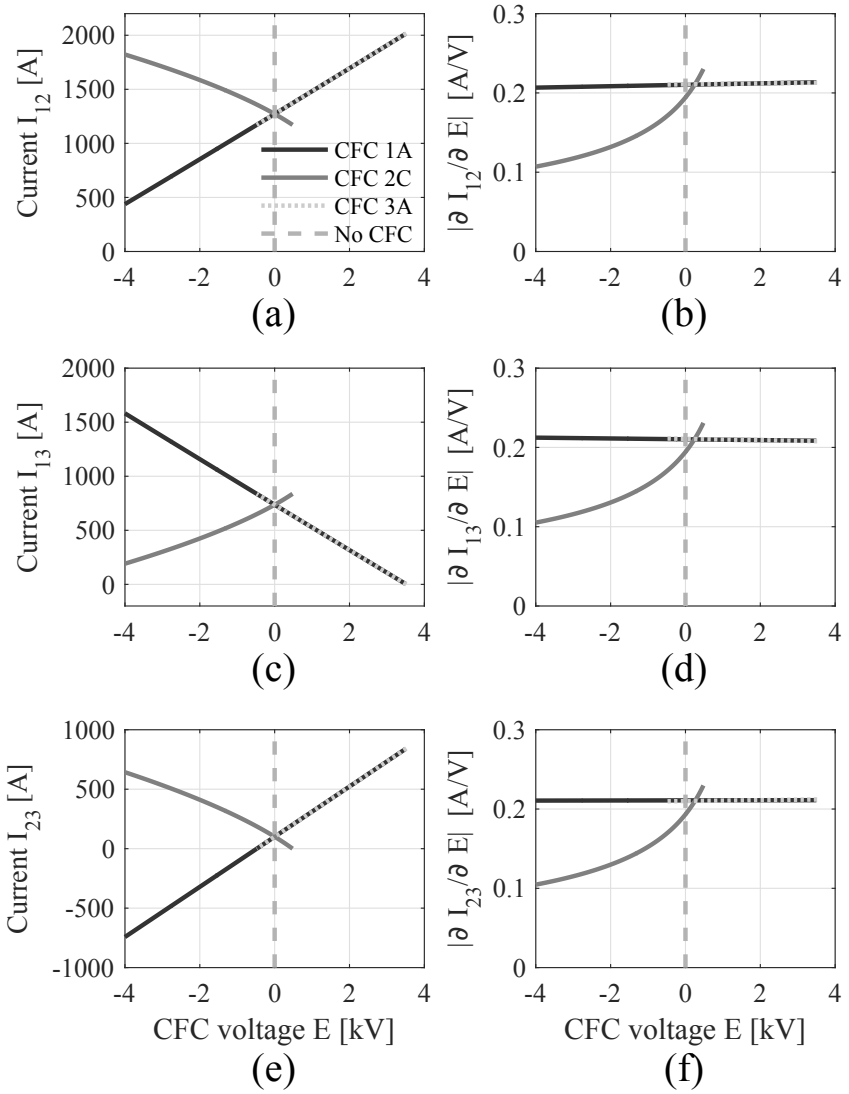

Fig. 6.9: Current variation and sensitivity analysis for different CFCs. (a) I_{12} variation with respect to CFC voltage. (b) I_{12} sensitivity with respect to CFC voltage. (c) I_{13} variation with respect to CFC voltage. (d) I_{13} sensitivity with respect to CFC voltage. (e) I_{23} variation with respect to CFC voltage. (f) I_{23} sensitivity with respect to CFC voltage.

following concept of the Current Variation Capability (CVC) is proposed:

$$CVC_i = \frac{|\Delta I_i|}{|\Delta E_i|} = \frac{|I_i^{max} - I_i^{min}|}{|E_i^{max} - E_i^{min}|} \tag{6.30}$$

where, I_i^{max} and I_i^{min} are the upper current limit and the lower current limit, respectively, where the CFC can drive the current of cable i. E_i^{max} and E_i^{min} are the CFC voltages which are required to bring the current to I_i^{max} and I_i^{min}, respectively. The CVC_i provides an approximation to compare the effect of different CFCs, in a way that CVC_i increases if the current variation range of cable i also increases. Nonetheless, its value drops if the required range of CFC voltage to produce such an effect rises, so that it gives an idea of how the voltage is used for each CFC.

Table 6.2 considers different powers, P_2^* and P_3^*, and the effects of the available CFCs are analysed. The second column of Table 6.2 shows the available CFC in each power flow and the next columns illustrate the current variation range, ΔI_i, and the CVC_i in each line. The rows in bold letter indicate the CFC that can provide the highest current variation range with the highest CVC as well, for a given power flow.

From Table 6.2 it can be noticed that the CFCs named jA have always the highest CVC, around 0.21 A/V, while the CFCs jB and jC have a CVC considerably lower, between 0.1 and 0.15 A/V in the cases considered. Another conclusion that can be extracted from Table 6.2 is that the CFC which can bring a greater current variation range, having a high CVC at the same time, is located in the node which exchanges the maximum power.

6.4.4 Case study 2: 7-terminal meshed grid with three different CFCs

In this section the methodology explained in Section 6.4.1 is applied to the 7-terminal meshed HVDC grid depicted in Fig. 6.10(a). The CFCs considered for the analysis are 5A, 3A and 5B, whose average models are shown in Fig. 6.10(b), 6.10(c) and 6.10(d), respectively. Tables 6.3 and 6.4 present the parameters of the system.

The variation of the line currents using the aforementioned CFCs is illustrated in Fig. 6.11 along with the required CFC voltage to provide such variation. Comparing its results with the ones in Case Study 1, it can be seen that in a DC grid with more terminals, the relations between the line currents and the CFC voltage with respect to the duty cycle, become less linear. It also points out that the location of the CFC plays an important

Table 6.2: CFC current range and current variation capability

P_2^*, P_3^* [MW]	CFC	ΔI_{12} [kA]	ΔI_{13} [kA]	ΔI_{23} [kA]	CVC_{12} [A/V]	CVC_{13} [A/V]	CVC_{23} [A/V]
-350, -250	**1A**	**1.573**	**1.576**	**1.580**	**0.210**	**0.210**	**0.211**
	2C	0.649	0.644	0.640	0.146	0.145	0.144
	3A	0.846	0.838	0.843	0.212	0.210	0.211
400, -200	1B	0.570	0.573	0.581	0.125	0.125	0.127
	2A	**1.323**	**1.317**	**1.312**	**0.212**	**0.211**	**0.210**
	3A	0.665	0.670	0.668	0.210	0.211	0.211
-200, 500	1A	0.967	0.977	0.966	0.210	0.212	0.210
	2B	0.574	0.577	0.584	0.126	0.126	0.128
	3A	**1.635**	**1.636**	**1.632**	**0.211**	**0.211**	**0.210**
400, 100	**1A**	**1.304**	**1.297**	**1.296**	**0.212**	**0.210**	**0.210**
	2A	0.982	0.971	0.973	0.212	0.210	0.210
	3B	0.475	0.473	0.477	0.103	0.102	0.103
400, -500	1C	0.680	0.679	0.657	0.117	0.117	0.113
	2A	1.221	1.229	1.216	0.210	0.212	0.210
	3A	**1.579**	**1.581**	**1.586**	**0.210**	**0.210**	**0.211**

Table 6.3: Case Study 2: Node Parameters

Parameter	Value	Units
E_4^*	300	kV
P_1^*	-600	MW
P_2^*	150	MW
P_3^*	-250	MW
P_5^*	300	MW
P_6^*	250	MW
P_7^*	600	MW

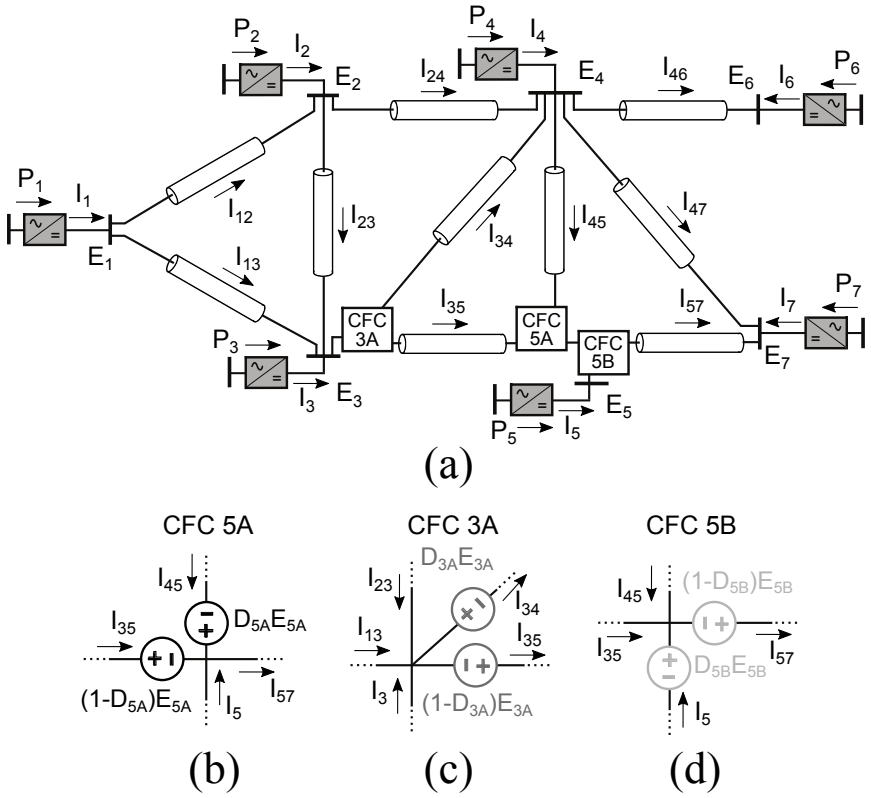

Fig. 6.10: Distributed CFCs in a 7-terminal meshed HVDC grid. (a) 7-terminal meshed HVDC grid scheme. (b) Model of CFC 5A. (c) Model of CFC 3A. (d) Model of CFC 5B.

Table 6.4: Case Study 2: Cable Parameters

Parameter	Value	Units
Cable length 12	100	km
Cable length 13	150	km
Cable length 23	200	km
Cable length 24	100	km
Cable length 34	250	km
Cable length 35	100	km
Cable length 45	200	km
Cable length 46	200	km
Cable length 47	250	km
Cable length 57	100	km
Resistance	0.0095	Ω/km

role. For instance, trying to regulate I_{57}, with CFC 5A is not a reasonable option, as from a $D_{5A} = 0.6$, increasing or reducing the duty cycle leads in both cases to a reduction in the current through that line (see Fig. 6.11(a)).

Fig. 6.12 shows the variation of line currents with respect to the CFC voltage and the line current sensitivity regarding each CFC considered. The results show that for the same CFC voltage range, CFCs 5A and 3A depict a higher variation range of current compared to 5B, except for current I_{57}, as no CFC is directly connected to cable 57. The right side graphics (see Fig. 6.12(b), 6.12(d), 6.12(f) and 6.12(h)), show the current sensitivity of each CFC for different line currents. It can be noted that in this Case Study 2, the derivatives of the line currents with respect to the CFC voltage are more dependant on the operation point if compared with the results of Case Study 1 where they are rather constant. Nonetheless, CFCs 5A and 3A show a higher value (absolute magnitude) of the current sensitivity compared to CFC 5B, except in the case of current I_{57}. The effect depicted before in Fig. 6.11(a), where I_{57} reduces its absolute value by increasing or reducing the duty cycle (and the CFC voltage) is explained by the change in the sign of the I_{57} sensitivity (see Fig. 6.12(h)).

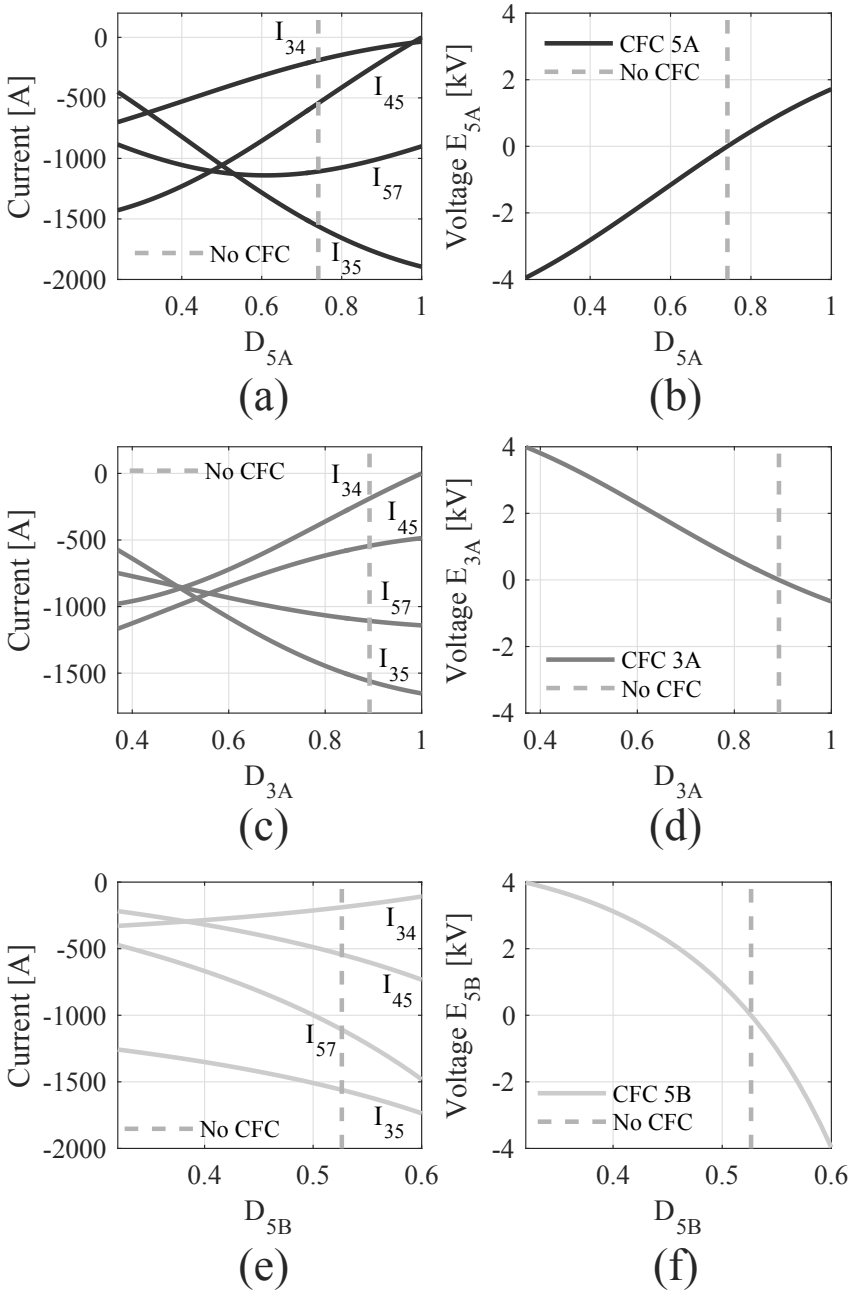

Fig. 6.11: Current variation and voltage requirement for different CFCs. (a) Current variation with CFC 5A. (b) Voltage requirement of CFC 5A. (c) Current variation with CFC 3A. (d) Voltage requirement with CFC 3A. (e) Current variation with CFC 5B. (f) Voltage requirement with CFC 5B.

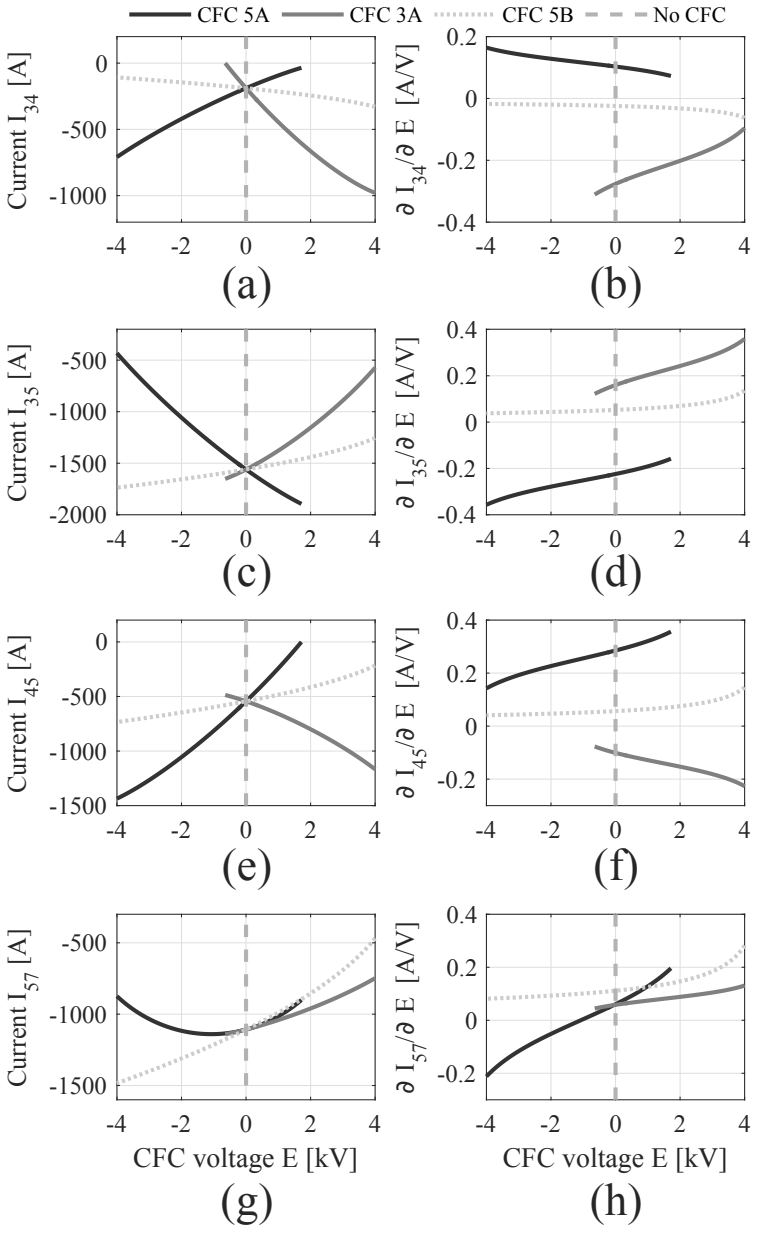

Fig. 6.12: Current variation and sensitivity analysis for different CFCs. (a) I_{34} with respect to CFC voltage. (b) I_{34} sensitivity with respect to CFC voltage. (c) I_{35} with respect to CFC voltage. (d) I_{35} sensitivity with respect to CFC voltage. (e) I_{45} with respect to CFC voltage. (f) I_{45} sensitivity with respect to CFC voltage. (g) I_{57} with respect to CFC voltage. (h) I_{57} sensitivity with respect to CFC voltage.

6.5 Design aspects of the DCFC devices and effect on the operational area

The results in Section 6.4 show that the CFCs named jA, which have *Line C* (see Fig. 6.2) connected directly to a VSC node, show some benefits as higher current variation range and better use of the CFC voltage than CFCs jB and jC. Besides, among them, the CFC jA connected to the node j that exchanges the maximum power has the maximum current variation range. Based on this outcome, the proposed DCFCs are built of the structures CFC jA that have *Line C* connected directly to a VSC node. As it is shown in Fig. 6.3, there are two CFC structures that can have *Line C* connected to the VSC node depending on the direction of the lines currents, which are represented by the same average model. Those two structures are merged and conform a DCFC, which is shown in Fig. 6.13(a). A common capacitor is used in each DCFC and the anti-parallel diodes of the IGBTs are used to obtain reverse blocking switches. Fig. 6.13(b) depicts the 3-terminal meshed HVDC grid with a DCFC in each node. A DCFC in each node is placed to illustrate the concept, though it does not imply the 3-terminal meshed grid would need one DCFC in each node.

The DCFC in node j is named DCFC jA as it produces the effect described by the average model CFC jA.

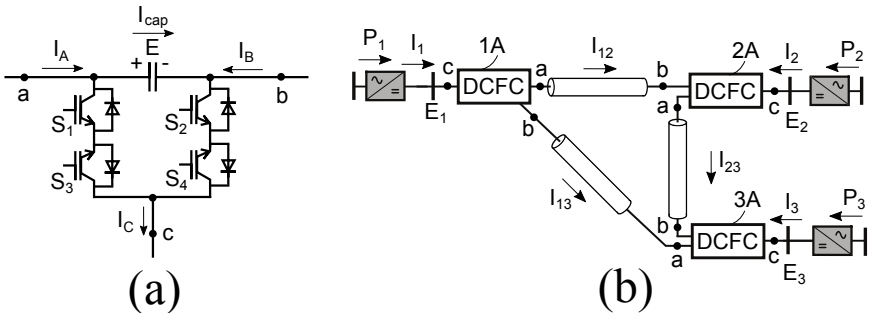

Fig. 6.13: Distributed CFCs in the 3-terminal meshed HVDC grid. (a) Converter structure of each DCFC. (b) Scheme showing the connection of each DCFC to the meshed HVDC grid.

6.5.1 Comparison of the operational area of the system using DCFCs or a 2B-CFC located in one node

This section compares the performance of the DCFCs installed in the HVDC grid with the 2B-CFC topology presented in [34] located only in node 1. Fig. 6.14(a) shows the 2B-CFC which is able to operate with all the current flows and can be represented with the average models CFC 1A, 1B and 1C (see Fig. 6.6) according to Chapter 3. Fig. 6.14(b) illustrates the 2B-CFC located in node 1 in the HVDC grid.

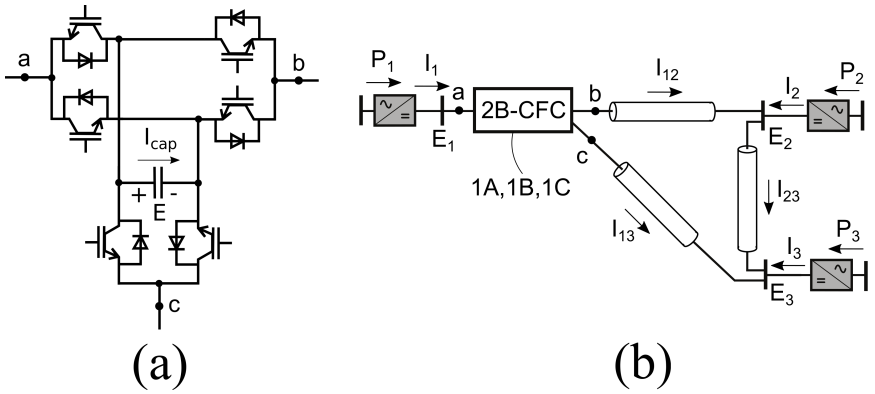

Fig. 6.14: 2B-CFC located in node 1 in the 3-terminal meshed HVDC grid. (a) Converter structure of the 2B-CFC topology able to operate with all current flows. (b) Scheme showing the connection of the 2B-CFC in node 1 to the meshed HVDC grid.

The parameters of the DC grid are the ones in Table 6.1 and the specific limits for this analysis are listed in Table 6.5. The CFCs are used to reduce the current through the overloaded line when it reaches the limit with the aim of extending the operational area of the system. Note that for this analysis it is assumed that all the lines have the same DC current limit.

Table 6.5: Limits of the CFC and the meshed HVDC grid

System limits		
Line DC current limit	I_{limit}	1.5 kA
Line DC current reference	I_{ref}	1.5 kA
Node DC current limit	I_{nlimit}	3 kA
CFC capacitor voltage limit	E_{limit}	2 kV

Fig. 6.15 and Fig. 6.16 show the operational area of the system considering the two CFC approaches of Fig. 6.14 and Fig. 6.13, respectively. In both

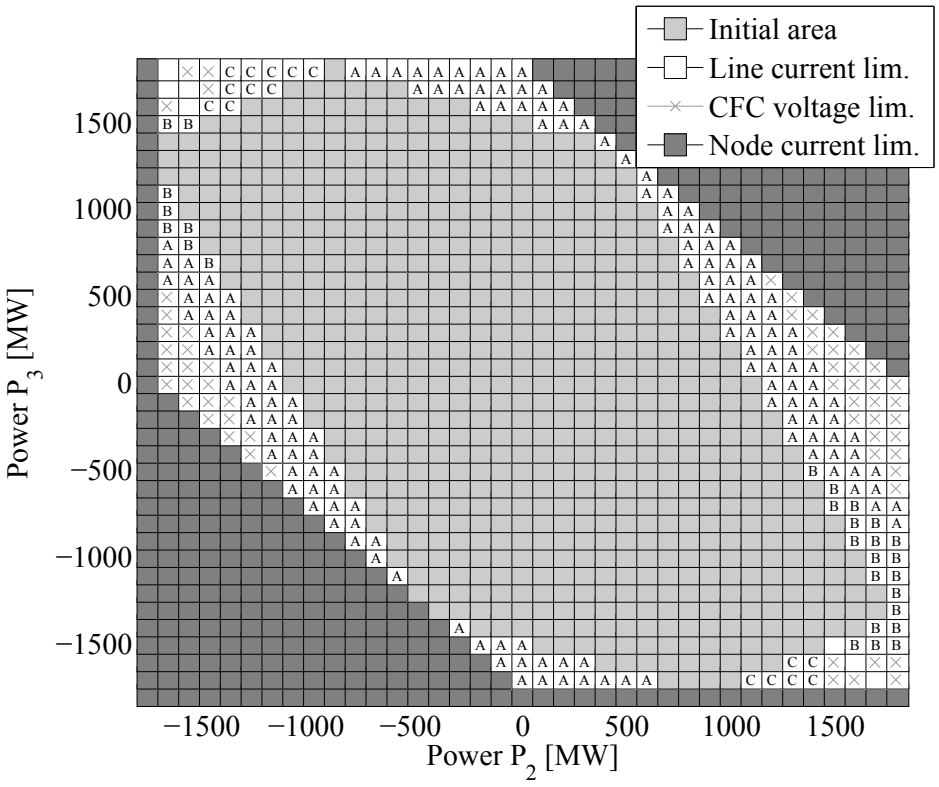

Fig. 6.15: Increase in the operational area of the system due to the 2B-CFC located in node 1 of Fig. 6.14.

Fig. 6.15 and 6.16, the light grey-filled squares depict the points where a CFC is not required since the cables of the DC grid are not overloaded. The white-filled squares show the points where some cable is overloaded and the dark grey-filled squares illustrate the points where the node current is higher than the VSCs limits.

In the case of Fig. 6.15, the squares with the letters A, B and C show the points where the CFC average models 1A, 1B or 1C are able to reduce the overload of the line, respectively, which means that the 2B-CFC in node 1 can be used to operate the system in those points. The points with a grey cross indicate that the 2B-CFC is not able to reduce the current through the overloaded cable due to the CFC voltage restriction. Finally, the white-

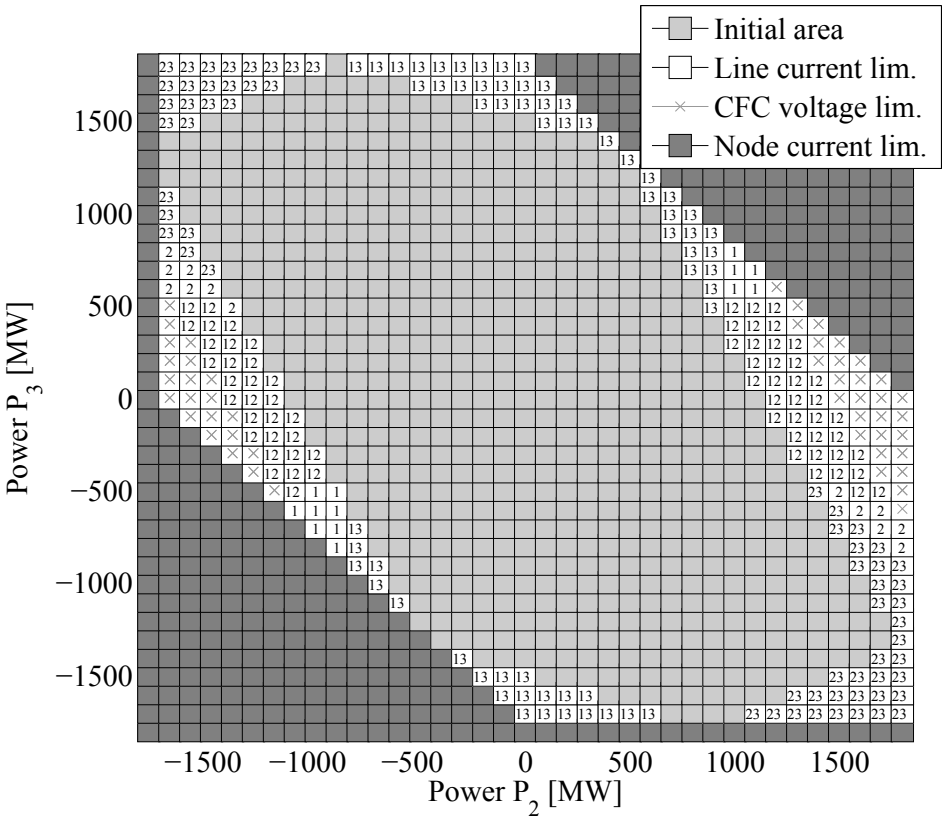

Fig. 6.16: Increase in the operational area of the system due to the Distributed CFCs of Fig. 6.13.

filled squares with no letter depict the points where almost all the current circulates through cable 23. In those cases, the current of node 1 is very small, and due to the fact that the power of node 1 is constant (without considering losses), it cannot be changed excessively. This fact limits the operation of the CFC and reduces its capability to limit the current through cable 23.

Regarding Fig. 6.16, the squares with the grey cross indicate that the DCFCs are not able to reduce the current due to the CFC voltage restriction as well. The numbers inside the white-filled squares illustrate the node or nodes where are located the DCFCs that can prevent the overload.

If comparing both Fig. 6.15 and Fig. 6.16, it can be seen that considering the 2B-CFC located in node 1, the current can be reduced using the converter in node 1, while considering the DCFCs, in some points two DCFCs located in different nodes can be used. This shows that only considering DCFCs in node 1 an 2 (DCFC 1A and 2A) would be sufficient to prevent the current overloads. Nonetheless, considering the three DCFCs in the grid introduces also a redundancy that could be advantageous for the controllability of the system. Another outcome is that when the majority of the current circulates through cable 23 (top left and bottom right regions of both figures), the 2B-CFC located in node 1 depicts a poor capacity to reduce the overload, while in the distributed approach, DCFCs 2A and 3A have the capability to reduce the current in those regions.

6.5.2 Losses consideration

This Section compares the performance of DCFCs (see Fig. 6.13(a)) in the DC grid of Section 6.5.1 in terms of required CFC voltage and losses. Considering three case studies with and overload in cable 23, three different DCFCs located in different nodes are used to regulate the current through the overloaded cable to I_{ref} for each case study. Table 6.6 illustrates the comparison between the different DCFCs for the case studies defined. Note that only for this section, the DCFCs can also be connected as CFC 1B or 1C in node 1 to analyse its effect. The IGBTs used for the losses calculation are the ABB StakPack [86] and the switching frequency is $f_{sw} = 1$ kHz.

It can be noted that whenever the DCFC that prevents the overload in cable 23 is the one in node 1 (1B or 1C), a higher value of the CFC voltage (in absolute value) is required, compared to the DCFCs 2A and 3A, located in node 2 and 3, respectively, which are much closer to the overloaded cable. The losses of the CFC, P_{cfc}, are much lower than the losses due to the resistances in the DC lines, P_{lines}. The losses in the DCFCs located away

Table 6.6: Losses comparison for three different case studies

P_2^*, P_3^*	Case Study 1 -800, 750			Case Study 2 -700, 900			Case Study 3 900, -750		
E_1^* [kV]	300			300			300		
DCFC	1B	2A	3A	1C	2A	3A	1B	2A	3A
E_2 [kV]	298.1	299	298.9	300.9	299.7	299.2	302.4	301.2	301.4
E_3 [kV]	301.8	301.9	301.8	303.7	302.8	302.4	299.5	298.1	298.4
I_{12} [kA]	1184	1175	1176	828	836	840	-1475	-1488	-1486
I_{13} [kA]	-993	-984	-985	-1465	-1472	-1476	1004	1016	1014
I_{23} [kA]	-1500	-1500	-1500	-1500	-1500	-1500	1500	1500	1500
D	0.838	0.561	0.396	0.440	0.642	0.496	0.68	0.502	0.403
E [V]	990	137	140	-1637	741	752	1438	-495	-488
P_{cfc} [kW]	8.18	14.82	13.35	14.49	16.41	22.97	13.17	20.38	15.89
P_{lines} [MW]	7.48	7.43	7.43	9.00	9.06	9.08	8.26	8.34	8.33
P_{total} [MW]	7.49	7.44	7.45	9.02	9.07	9.11	8.27	8.36	8.34

from the overloaded line (DCFC 1B and 1C) tend to have a lower value compared to the ones of DCFC 2A and 3A, due to the lower currents that circulate through the device, despite having a higher CFC voltage value. Nevertheless, this losses value is quite small compared to the losses in the DC lines and slightly affect the total losses, P_{total}, which are the sum of both.

6.6 Operation and control of the DCFCs

The control scheme in each DCFCs is sketched in Fig. 6.17, which consists of an inner voltage loop and an outer current loop. The voltage controller is in charge of regulating the voltage of the CFC capacitor and the current controller regulates the DC current through the cables of the DC grid. This control scheme is designed and its control parameters are obtained following the methodology explained in Chapter 3 and Chapter 5.

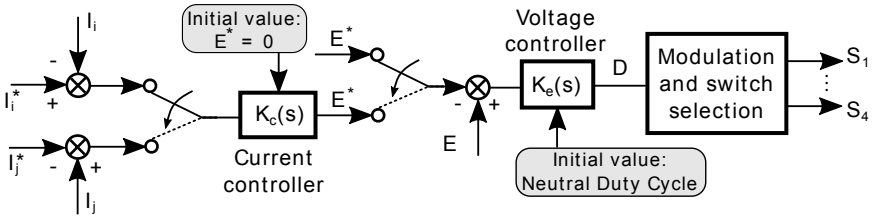

Fig. 6.17: Control scheme of each DCFC with a voltage loop and a current loop.

The overall DCFC concept is based on the idea that only one DCFC is selected to be operating whenever there is an overload in a line. The DCFC chosen to be in operation is one connected to the overloaded cable. In case of no overloads in the cables, all the DCFCs remain bypassed using mechanical switches. The bypass is based on the scheme presented in Chapter 5 and the start-up of each DCFC is performed initializing it with the NDC (see also Chapter 5).

Fig. 6.18 shows the flowchart of the algorithm used to keep the HVDC without overloads that governs the operation of the DCFCs in the 3-terminal meshed HVDC grid. The described algorithm is executed every 0.1 s while the HVDC grid is in operation.

Regarding the operation of the DCFCs during DC faults, there are two approaches to follow. The first one is being investigated in [55] and consists on bypassing the CFC with additional equipment and using additional control schemes in order to protect it from overcurrents and overvotlages. The second approach is to integrate the CFC functionalities into the DCCBs which it is proposed in Chapter 4, thus the circuit breaker equipment is able to both protect the system from DC faults and also perform current control when is needed.

6.7 Dynamic simulations

The operation of the proposed DCFCs (see Fig. 6.13) is validated using dynamic simulations in the 3-terminal meshed HVDC grid of Fig. 6.13(b). The length of the cables are illustrated in Table 6.1 and they are modelled considering PI models with parallel series branches [84], whose parameters are the same ones as in Chapter 5. Each cable is supposed to have one DCCB at each end, which is modelled as an inductance and a resistance with the values of Chapter 5. Node 1 is operating as a voltage slack bus and node 2 and 3 are extracting or injecting power according to the references. For the simulations, the half of the symmetric monopole is modelled due to its symmetry.

Fig. 6.19 and Fig. 6.20 illustrate the results of the simulation of the DCFCs in the 3-terminal meshed HVDC grid. The subscript 'o' correspond to the variables considering that there are no DCFCs in the grid (dashed lines), so that the cables may be overloaded (see Fig. 6.19).

Fig. 6.19(b) shows the power of node 2 is constant, -1.4 GW, and the ramped decrease of the power of node 3, P_3, from 1.2 GW to 0.3 GW. Then, it increases until 1.2 GW and after that until 1.7 GW. From Fig. 6.16 it

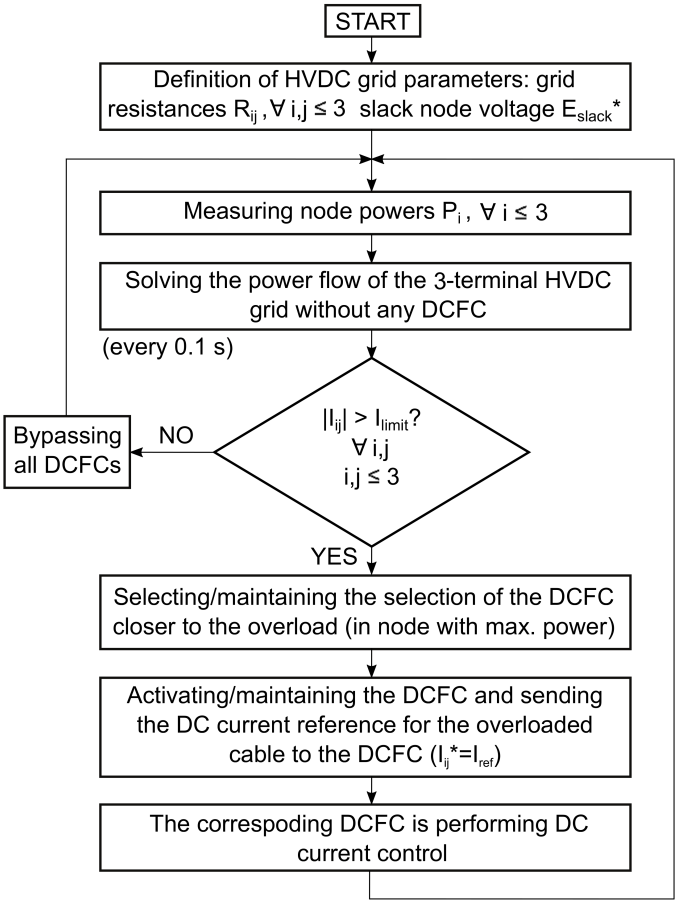

Fig. 6.18: Flowchart of the algorithm that governs the DCFCs.

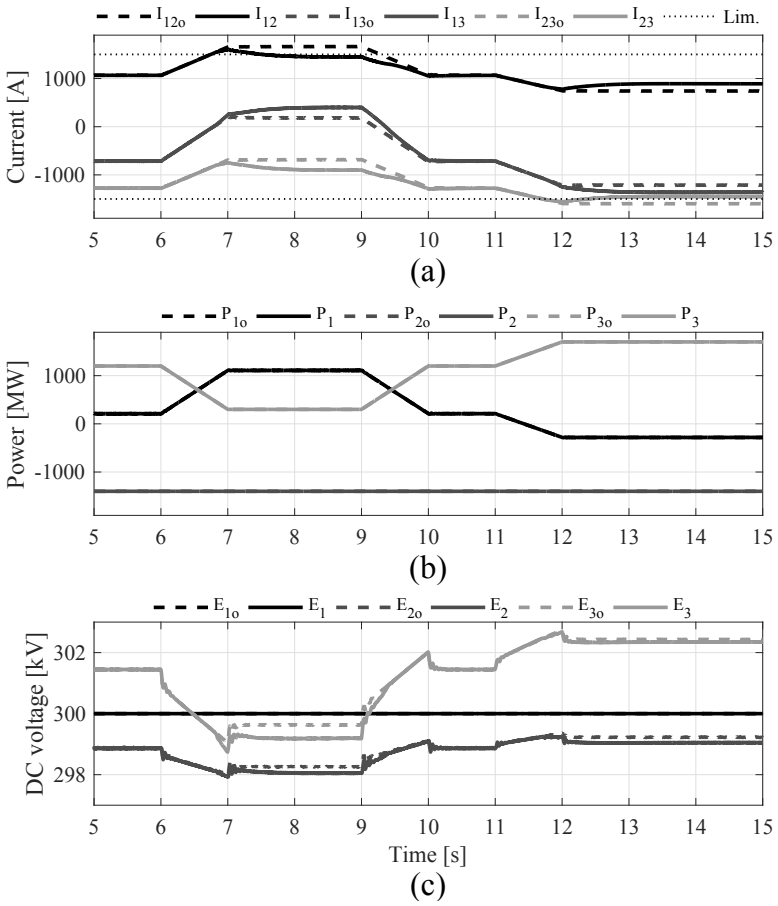

Fig. 6.19: Simulation results of the 3-terminal HVDC grid without CFC (dashed lines) and with the three DCFCs (solid lines). (a) Line currents. (b) Node powers. (c) Node voltages.

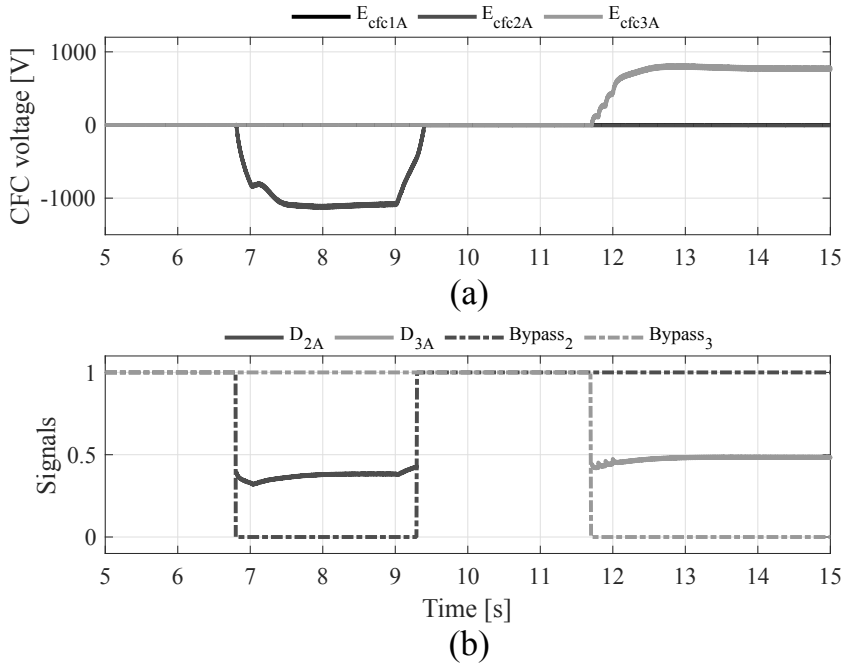

Fig. 6.20: Simulation results of the 3-terminal HVDC grid with three DCFCs. (a) CFC voltages of the DCFCs. (b) Bypass and duty cycle signals of the DCFC 2A and 3A.

is possible to see that the powers $P_3 = 0.3$ GW and $P_3 = 1.7$ GW, along with $P_2 = -1.4$ GW, require the activation of some DCFC as a cable exceeds the limit of 1.5 kA (see Section 6.5.1). This matches with the results of Fig. 6.19(a), where I_{12} and I_{23} reach the current limit and they are reduced using the DCFCs in node 2 and 3, respectively (DCFC 2A and 3A). Fig. 6.19(c) depicts the evolution of the DC voltages of the nodes, which are not really affected by the DCFCs operation.

Fig. 6.20 illustrates the capacitor voltage of the DCFC in node 2 and 3, the bypass and duty signals of both DCFCs. Whenever the algorithm in Fig. 6.18 detects that the line current is exceeding the cable limit, the bypass signal of the corresponding DCFC (first DCFC 2A and then DCFC 3A) goes to 0 and activates the start-up procedure of the DCFC (see Fig. 6.20(b)). Then, the duty cycle is applied to the switches of the DCFC and the their capacitor is charged (see Fig. 6.20(b)) what leads to the reduction of the corresponding line current.

6.8 Conclusions

This chapter has presented the concept of DCFCs in different nodes of a meshed HVDC grid that are operated selectively to avoid overloads in the cables. The DCFCs are simplified CFC converters derived for specific current flow directions that are chosen to operate depending on the location of the overload. The topology of the DCFCs is based on the series interline DC/DC CFC and has been obtained after a steady-state and a sensitivity analysis. A methodology to investigate the effect of introducing DCFCs in a generic meshed HVDC grid has been also presented. The cases considered point out the importance of choosing properly the location of the DCFCs in order to have a high current variation capability and adequate use of the CFC voltage. The increase in the operational area considering DCFCs in several nodes or a 2B-CFC in one node is compared showing that the 2B-CFC depicts a worse performance when it is not directly connected to the overloaded cable. The distributed approach allows to reduce the overload with a lower CFC voltage and brings also the possibility to have extra redundancy, at the expense of having more switches in total. The losses of DCFCs depending on the location are also analysed, showing that its value is quite low compared to the losses in the cables. The operation and control of the DCFCs is presented and its performance is validated using dynamic simulations.

Chapter 7

Multi-port interline current flow controller for meshed HVDC grids

7.1 Introduction

This chapter presents a n-port DC/DC based CFC topology for unidirectional current flows, which represents the generalisation of the converter introduced in Chapter 5 and [42] for n lines. The concept brings the advantage of a simplified circuit compared to other topologies, especially attractive for distributed approaches (see Chapter 6), at the expense of being able to operate only with unidirectional current flows. The modelling of the converter is provided and its average model derived for a generic number n of lines. Then, the modulation and control strategy of the converter are also described. Afterwards, the case study presents the dynamic simulation results of two 5-port CFCs based on the presented topology, one located on the positive pole and the other on the negative pole of a symmetric monopole 5-terminal meshed HVDC grid.

7.2 Multi-port current flow controller

This work presents a multi-port CFC topology, which is able to control the DC current through the lines where it is connected. The topology is meant for unidirectional current flows and it is based on the 3-port concept introduced in Chapter 5 and [42] but extended to n lines. The two CFC structures are presented in Fig. 7.1, depending on the direction of the currents. On the one hand, in Fig. 7.1(a), it is assumed that the total current goes into the CFC from Node 1 and then it is distributed between the other lines. On the other hand, Fig. 7.1(b) considers that the currents through the lines enter into the the CFC and the total amount goes out to Node 1.

As shown in Fig. 7.1, taking n as the number of lines where the converter is connected to, its structure is made of $n-1$ switches and $n-2$ capacitors.

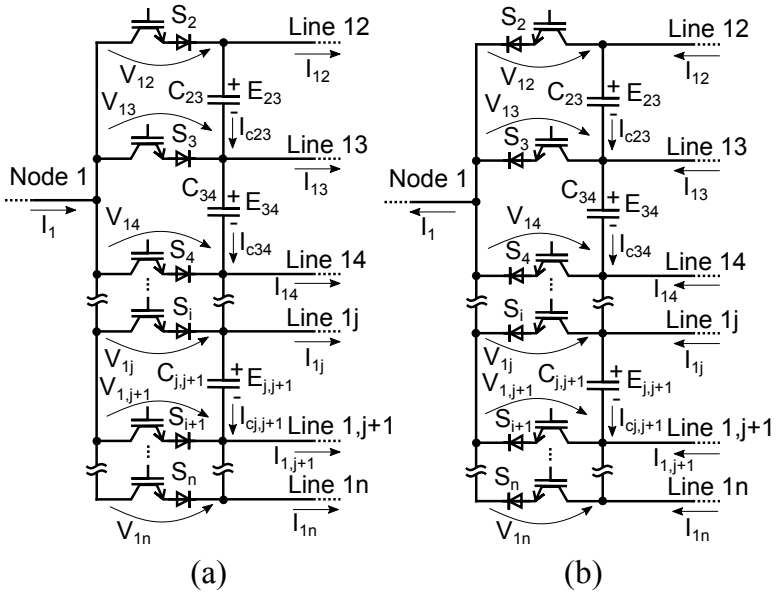

Fig. 7.1: Scheme of the multi-port CFC topology located in Node 1 and connected to $n-1$ lines. (a) DC currents circulating from Node 1 to the other lines. (b) DC currents circulating to Node 1 coming from the other lines.

The switches require reverse blocking voltage capability and the capacitors must allow positive and negative voltage polarity for the adequate operation of the converter. For this work, IGBTs with a diode connected in series are assumed to obtain the reverse blocking voltage capability, though other options can be applicable.

The previous converter structure provides a unidirectional multi-port solution for current flow control. Nevertheless, it must be acknowledged that if the number of lines where it is connected is high, it is less likely that all of them will have unidirectional current flow. For this reason, although it provides a multi-port solution, it becomes rarer to find a system where it can be applied when the number of ports increases. However, for HVDC applications it can be feasible to find nodes where the power is unidirectional, such as wind power plants.

7.3 Converter modelling

For simplicity, the following work derives the model of the converter based on the structure of Fig. 7.1(a). However, the derivation is analogous for the structure in Fig. 7.1(b). The procedure is the same as the one applied in Chapter 3 and Chapter 5 but for a generic n-port CFC.

7.3.1 Operating principle

In order to allow a path for the current, there must always be a switch in ON state and it is assumed that only one of them is in ON state at a time. Based on this, the following equation is obtained:

$$\sum_{i=2}^{n} t_{Si} = T \tag{7.1}$$

where t_{Si} is the time that switch i is in ON state and T is the period of the switching frequency of the converter. Transforming the previous expression to duty cycles, yields to:

$$\sum_{i=2}^{n} D_i = 1 \tag{7.2}$$

where D_i is the duty cycle of switch i.

For instance, $D_i = 1$ implies that switch i remains in ON state all the period. Analysing Fig. 7.1(a) under this situation, initially the current from Node 1 flows through the switch i and then is distributed through all the lines. The current finds no obstacle through the line connected to switch

S_i, but regarding the other lines, the current charges the capacitors and increases their voltage. Whenever the voltages of the capacitors are high enough to block the currents through the other lines, the steady-state is reached and I_1 flows entirely through the line connected to switch S_i.

In order to bypass the device without using external switches, which are required for bypassing permanently the converter (see Chapter 5), the procedure consists on turning ON all the switches. By doing this, the voltage of the capacitors goes to zero and the converter is not applying any effect on the DC grid currents.

Assuming that the line currents remain constant for the following analysis, when one of the switches is in ON state, a voltage between Node 1 and the other lines is applied and it is dependent on the voltage of the capacitors at that time. The subscript i is used to identify the switch that is in ON state and the subscript j refers to the Node j that is connected to the CFC through line $1j$. The following equations describe the voltage between Node 1 and line $1j$, assuming no voltage drops on the switches:

$$V_{1j} = 0 \ , \qquad i = j \tag{7.3}$$

$$V_{1j} = \sum_{k=i}^{j-1} E_{k,k+1} \ , \qquad i < j \tag{7.4}$$

$$V_{1j} = \sum_{k=j}^{i-1} -E_{k,k+1} \ , \qquad i > j \tag{7.5}$$

The current that circulates though each capacitor is given by (7.6) and (7.7).

$$I_{c_{j,j+1}} = \sum_{k=j+1}^{n} I_{1k} \ , \qquad i \leq j \tag{7.6}$$

$$I_{c_{j,j+1}} = \sum_{k=2}^{j} -I_{1k} \ , \qquad i > j \tag{7.7}$$

where, i defines the switch that is ON and $1j$ and $1, j+1$ correspond to the lines where the capacitor is connected. In order to have each capacitor balanced, the equation that must be met for each capacitor between lines $1j$ and $1, j+1$ is:

$$\sum_{i=2}^{n} \frac{t_{Si}}{T} I_{c_{j,j+1}} = 0 \ , \qquad \forall j \leq n-1 \tag{7.8}$$

and considering the duty cycles of the switches:

$$\sum_{i=2}^{n} D_i I_{c_{j,j+1}} = 0 \ , \qquad \forall j \leq n-1 \tag{7.9}$$

Then, combining (7.6), (7.7) and (7.8) is it possible to obtain:

$$D_i = \frac{I_{1i}}{\sum_{i=2}^{n} I_{1i}} \ , \qquad \forall i \leq n \tag{7.10}$$

Based on (7.10), imposing a duty cycle drives the system to achieve a certain current relation in order to have the CFC capacitors balanced, as it was also reported for the 3-port CFC topology presented in Chapter 5. Then, when a certain duty cycle is applied, the capacitors will achieve the CFC voltage that provides the corresponding current relation. The present work seeks to introduce the multi-port concept but does not design a complete closed-loop control scheme as in Chapter 5.

7.3.2 Modulation and control strategy

According to (7.10), imposing a duty cycle defines the current relation between the corresponding line and the total current from Node 1. Based on this, it is possible to control DC currents by assigning a duty cycle to each switch according to the desired current of that line. Fig. 7.2 presents the generalised modulation strategy for a n-port CFC. As shown in Fig. 7.2, the signals sent to each switch are time-consecutive in a way that always one of the switches is in ON state. The time that the signal has a value of 1 is proportional to the duty cycle of that switch. For the real implementation of the converter, negative dead-times are required so that there is always a path for the current through the converter. The logic implemented to obtain the desired signals according to Fig. 7.2 is illustrated in Fig. 7.3. Using this approach and according to (7.2), it is possible to see that the n-port CFC has $n-2$ degrees of freedom since when D_2 to D_{n-1} have been set, D_n achieves a certain value to guarantee a path for the current at any time. Other modulation and control strategies can be studied where more than one switch can be ON at the same time. Nevertheless, this work presents the previous modulation in order to provide an intuitive control of the converter, where each duty cycle is directly related to the current value of a certain line.

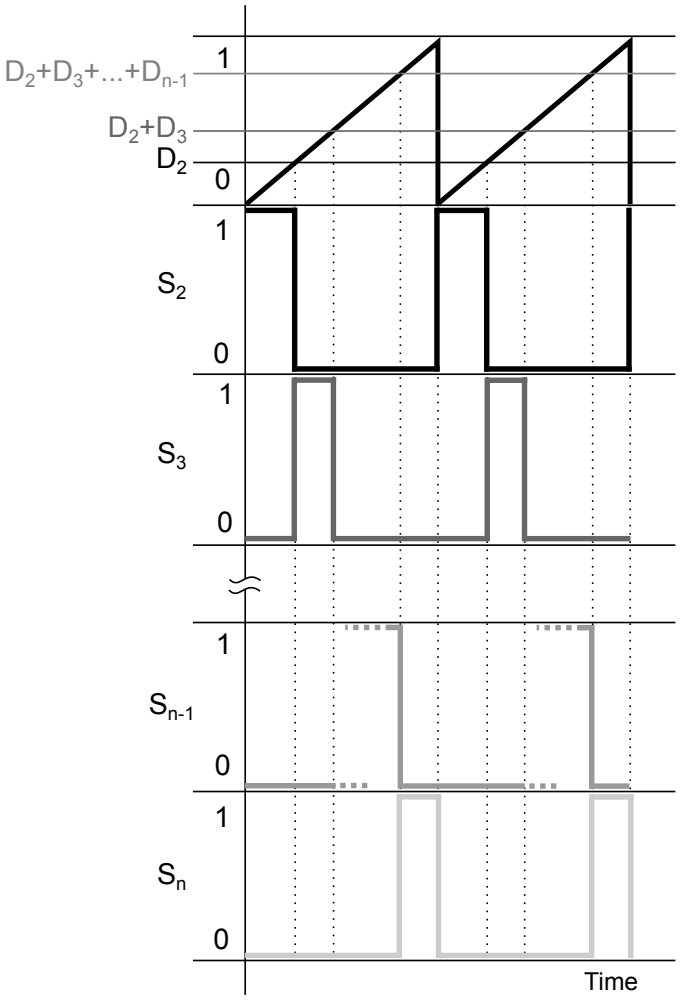

Fig. 7.2: Modulation strategy applied to the n-port CFC.

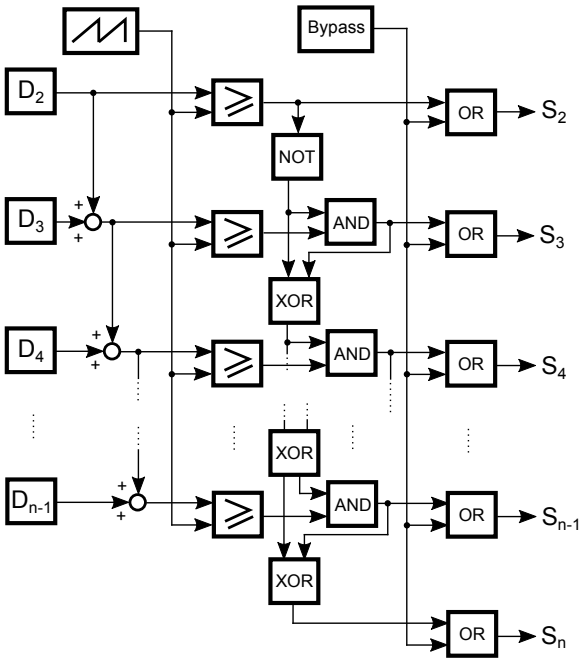

Fig. 7.3: Modulation implemented with logic blocks for a n-port CFC.

7.3.3 Average model

As illustrated in Section 7.3.1, when one of the switches is in ON state, a certain voltage, which is dependent on the actual voltage values of the CFC capacitors, is applied on the lines. Then, knowing the time that each switch is conducting, given by the duty cycle, it is possible to obtain the average voltage applied to each line as a function of the CFC capacitor voltages and the duty cycles of the switches:

$$\overline{V}_{1j} = \sum_{i=2}^{n} D_i V_{1j} \ , \qquad 2 \leq j \leq n \tag{7.11}$$

And using (7.3)-(7.5) yields to:

$$\overline{V}_{1j} = \sum_{i=2}^{j-1} D_i \sum_{k=i}^{j-1} E_{k,k+1} - \sum_{i=j+1}^{n} D_i \sum_{k=j}^{i-1} E_{k,k+1} \ , \quad 2 \leq j \leq n \tag{7.12}$$

Fig. 7.4 illustrates the average model of the n-port CFC where a variable voltage source is placed between Node 1 and each line. An additional circuit

is introduced for each capacitor in the CFC, which is composed of a capacitor and several current sources in parallel that represent the charging and discharging of the capacitors of the CFC due to the DC line currents. The analytical expression of $\overline{V}_{1j}$ and $I_{cj,j+1}$ can be obtained from (7.6), (7.7) or (7.12).

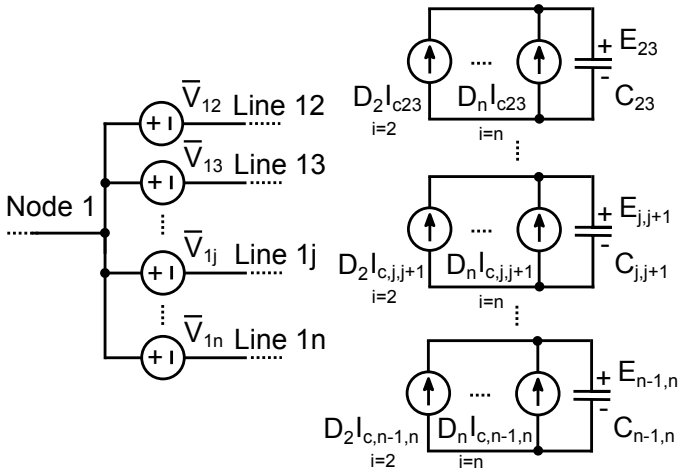

Fig. 7.4: Average model of the n-port CFC made of $n-1$ voltage sources and $n-2$ circuits with a capacitor and $n-1$ current sources in parallel.

7.4 Case study: simulations of a 5-port CFC

7.4.1 System description

This case study considers a 5-terminal meshed HVDC grid as the one illustrated in Fig. 7.5(a). Two 5-port CFCs are installed in Node 1, one in the positive pole and the other in the negative pole. Both converters are shown, respectively, in Fig. 7.5(b) and 7.5(c). Node 1 operates as a slack bus keeping constant the DC voltage and the remaining nodes perform power control. The cables of the DC grid are modelled using a section of parallel series branches model proposed in [84], whose parameters are shown in [85]. Tables 7.1 and 7.2 depicts the parameters of the HVDC grid and the 5-port CFC.

For instance, in order to provide an example for (7.12), the average volt-

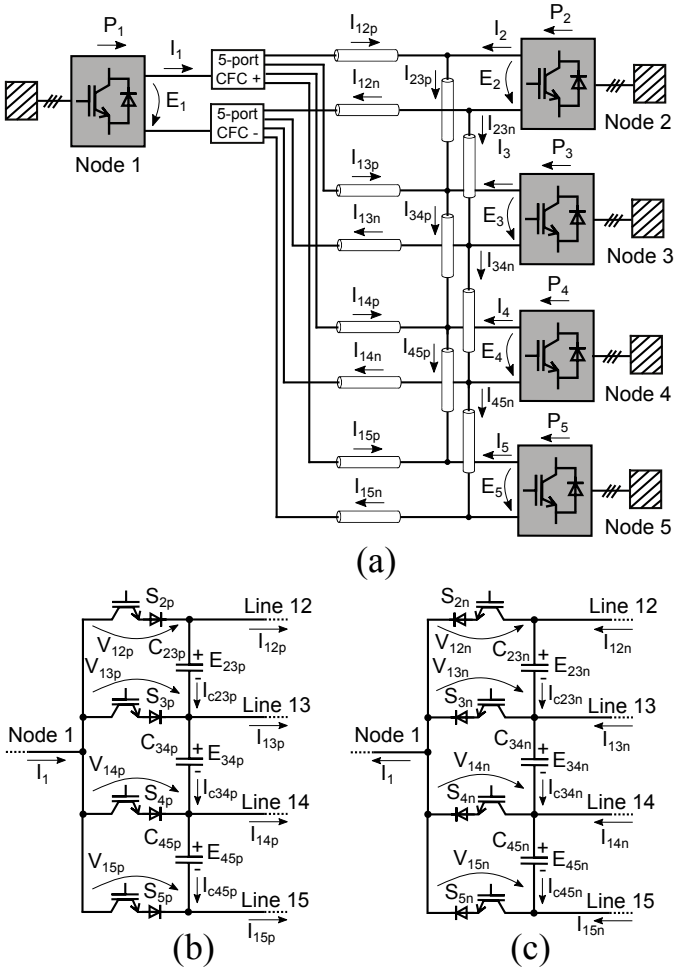

Fig. 7.5: Scheme of a 5-terminal meshed HVDC grid with two 5-port CFCs considered for the dynamic simulation. (a) 5-terminal HVDC grid (b) Scheme of the 5-port CFC of the positive pole. (c) Scheme of the 5-port CFC of the negative pole.

Table 7.1: HVDC grid parameters

Parameters of the meshed HVDC grid							
Cable ij	12	13	14	15	23	34	45
Distance d_{ij} [km]	100	150	150	150	100	200	150
Node i			1	2	3	4	5
Power reference P_i^* [MW]			-	-500	-300	-500	-100
Voltage reference E_1^* [kV]			320	-	-	-	-
Power loop time constant τ_i [ms]			-		100		

Table 7.2: CFC parameters

Parameters of the CFCs			
CFC between lines ij (+ & − pole)	23	34	45
Rated voltage E_{cfc} [kV]		± 4	
CFC capacitance C_{ij} [mF]		10	
Switching frequency f_{sw} [Hz]		2000	

ages applied on the lines by the 5-port CFC in the positive pole are:

$$\overline{V}_{12} = -D_3E_{23} - D_4(E_{23} + E_{34}) - D_5(E_{23} + E_{34} + E_{45}) \tag{7.13}$$

$$\overline{V}_{13} = D_2E_{23} - D_4E_{34} - D_5(E_{34} + E_{45}) \tag{7.14}$$

$$\overline{V}_{14} = D_2(E_{23} + E_{34}) + D_3E_{34} - D_5E_{45} \tag{7.15}$$

$$\overline{V}_{15} = D_2(E_{23} + E_{34} + E_{45}) + D_3(E_{34} + E_{45}) + D_4E_{45} \tag{7.16}$$

7.4.2 Simulation results

Figs. 7.6 and 7.7 show the simulation results of the 5-port CFCs in the meshed HVDC grid. Fig. 7.6(a) depicts the voltages at the nodes, which remain fairly constant and in Fig. 7.6(b), the node powers are illustrated, showing that VSC 1 injects 1 pu into the HVDC grid and the rest of the converters extract a constant amount of power. It can be seen that the line currents that circulate through the CFCs, in the postive pole go from VSC 1 to the other VSCs (see Fig. 7.6(c)) and viceversa, in the negative pole (see Fig. 7.6(d)). Initially, the currents in the grid are not affected by the CFCs because both of them are applying the Neutral Duty Cycle (NDC) (see Chapter 5), which means that the duty cycle sent to the switches also corresponds to the current relation that would circulate through each line if the CFCs were not installed (see Fig. 7.7(c) and 7.7(d)). At that time, Fig. 7.7(a) and 7.7(b) illustrate that the voltages of the capacitors of the CFCs in both poles are zero since the devices are not affecting the grid.

Then, at instant $t = 3$ s new duty cycles (that correspond to the desired percentage of current through each line) are sent to the CFCs (see Fig. 7.7(c) and 7.7(d)). It can be observed that the duty cycles are different for the CFC on the positive pole and the one on the negative pole, because they can be controlled independently. The references for the CFC on the positive pole are to null the current through line 13 and increase 10% the current through line 12. Also, D_{5p} (related to line 15) is automatically modified to absorb the remaining current (see Fig. 7.7(c)) as the current reference for line 14 is kept constant. It can be seen in Fig. 7.6(c), that the line currents achieve the same value than the duty cycles after a dynamic transient. Meanwhile, the voltages of the capacitors in the CFC adapt their values in order to provide such change in the currents in Fig. 7.7(a). Regarding the line currents of the negative pole, different references are sent to the corresponding CFC. The desired current through line 13 must be reduced a 20% and current through line 14 is to be diminished until zero. The reference for 12 is kept

constant so that the duty cycle D_{5n} changes its value to absorb the remaining current (see Fig. 7.7(d)). Also, for the negative pole, the currents showed in Fig 7.6(d) achieve the reference value (see Fig. 7.7(d)) and the capacitors are also charged accordingly (see Fig. 7.7(b)) to a value that allows the desired current distribution. The results illustrate that the line currents from the positive pole and the negative pole can be regulated to different values independently.

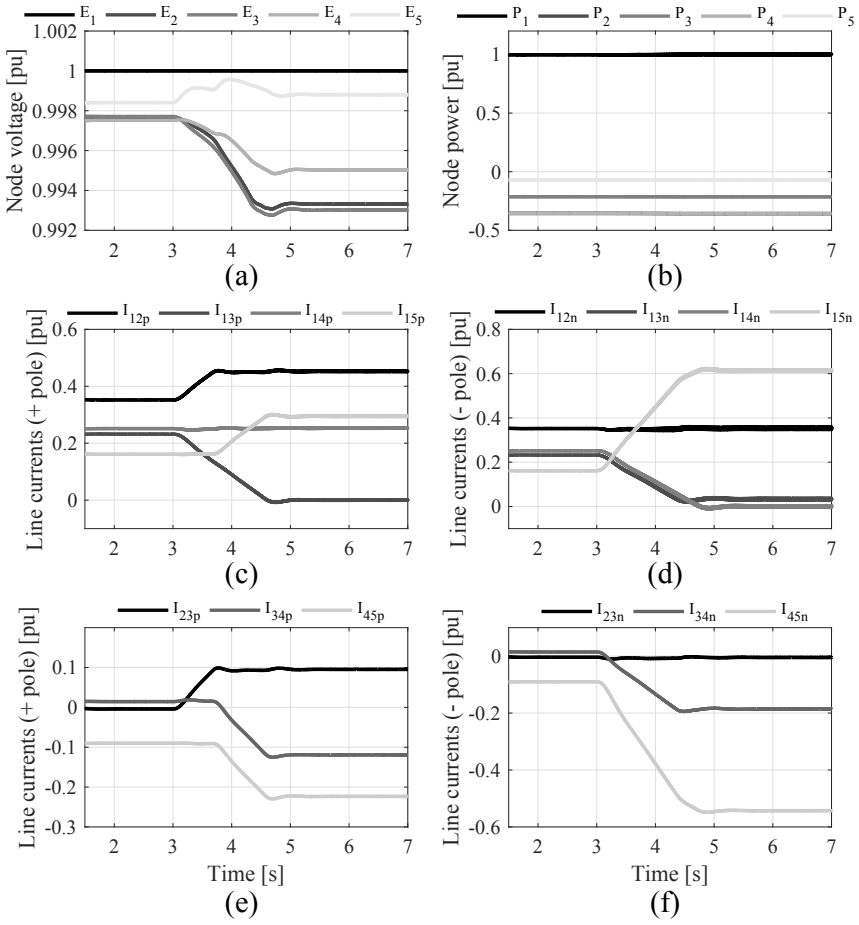

Fig. 7.6: Simulation results. (a) Node voltages. (b) Node powers. (c) First set of line currents in the positive pole. (d) First set of line currents in the negative pole. (e) Second set of line currents in the positive pole. (f) Second set of the line currents in the negative pole.

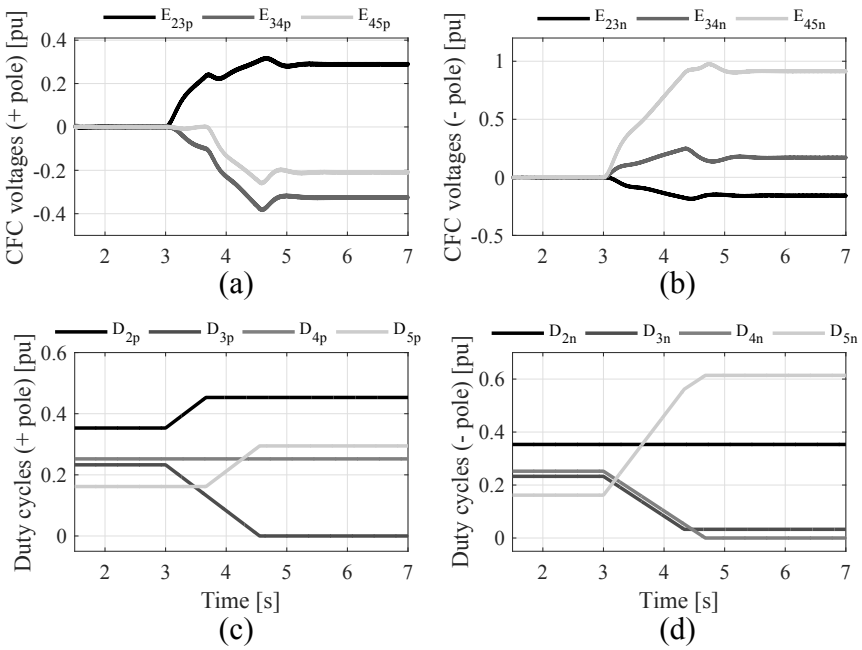

Fig. 7.7: Simulation results. (a) Voltages of the capacitors in the CFC on the positive pole. (b) Voltages of the capacitors in the CFC on the negative pole. (c) Duty cycles of the CFC in the positive pole. (d) Duty cycles of the CFC in the negative pole.

7.5 Conclusion

This chapter has presented a multi-port CFC for unidirectional current flows that can be connected to n lines. It can regulate the current through those lines in order to prevent overloads by charging and discharging the CFC capacitors. The modulation and control strategy for a n-port CFC have been presented and a 5-port CFC is validated using dynamic simulations. The simulations show how the CFCs located on the positive and negative poles can regulate the currents, independently, by setting the corresponding duty cycle of the switches.

Chapter 8

Filter design of a transformerless DC/DC converter based on the autotransformer concept for the interconnection of HVDC grids

8.1 Introduction

The idea of interconnecting point-to-point HVDC links to build an HVDC grid appears to be an attractive concept as a way to enable the integration of the renewable sources and providing additional flexibility and redundancy in the power transmission [14]. Nonetheless, there are many challenges related to the interconnection of these already build HVDC links: different voltage levels, HVDC technologies, converter manufacturers, etc.

The aforementioned challenges have encouraged the research in high power, high voltage DC/DC converters [25]. The number of suggested DC/DC topologies is increasing and some works are starting to classify the different topologies by grouping them in families of common characteristics [25, 87]. The family of the DC/DC autotransformer brings some advantages, compared to other designs, because only a fraction of the total power of the interconnection is passing through the AC interface, so that, the rating of the switches and the AC transformer can be lower compared to other Front to Front topologies (F2F) [88]. Several proposals of DC/DC autotransformers can be found in [88–91] implemented with Modular Multilevel Converters (MMC)[8], due to its high modularity and scalability. One of the drawbacks of the DC/DC autotransformer topology is that it requires an AC transformer with high insulation requirements and the DC/DC autotransformer itself does not provide galvanic insulation between DC sides. Some works consider a Transformerless (TL) topology where the AC transformer has been replaced by an AC filter [92] or equivalent converter schemes with a

capacitor instead of an AC transformer [93].

The present chapter deals with the TL DC/DC autotransformer topology, which was introduced in the patent [92], and it is further analysed and extended in this work. The aim of the chapter is to design the most simple AC filter that can guarantee the proper operation of the TL converter. Three different models of the TL topology with different levels of accuracy are developed and compared in order to study the AC filter. The control of the converter is also proposed, based on regulating the power that circulates through the AC filter. Then, this work investigates how the operational limits of the TL topology are affected by the filter parameters and the design of the filter is presented. Finally, the three models of the TL topology are compared and the validation of the AC filter design is done by means of dynamic simulations using Matlab Simulink.

8.2 DC/DC autotransformer concept

The concept of the DC/DC transformer and the autotransformer is introduced in Fig. 8.1. Fig. 8.1(a) depicts the scheme of a DC/DC transformer that allows the interconnection of two DC sides with different voltage levels. The part in between connects the Converter 1 and Converter 2 using a general interface, that could be a transformer, filter, another converter, etc. Fig. 8.1(b) shows how the DC/DC autotransformer is obtained by adding external connections into the DC/DC transformer (red lines). The DC/DC autotransformer can also be used to interconnect two DC sides with different voltage level. Nevertheless, only a fraction of the total power circulates through the interface. For the following analysis, it is assumed that $V_{HV}^{DC} > V_{LV}^{DC}$, where V_{HV}^{DC} and V_{LV}^{DC} are the voltages of the High Voltage (HV) and Low Voltage (LV) sides.

The power distribution inside the DC/DC autotransformer mentioned before is independent of the interface used and of the topology considered for Converter 1 and Converter 2. Fig. 8.1 illustrates that a fraction of the total input power, P_{HV}^{DC}, is transformed by Converter 2 and circulates through the interface to Converter 1. This power is named transformed power, P_T, and it is transformed again by Converter 1. However, there is a fraction of P_{HV}^{DC}, the transferred power P_C, that is not transformed by the converters, and it is transferred through the external connections to the output.

This leads to a reduction in the rating of the converters if the same DC power of the interconnection is kept, or an increase of the total available DC power transfer if the rating of the converters is maintained, compared

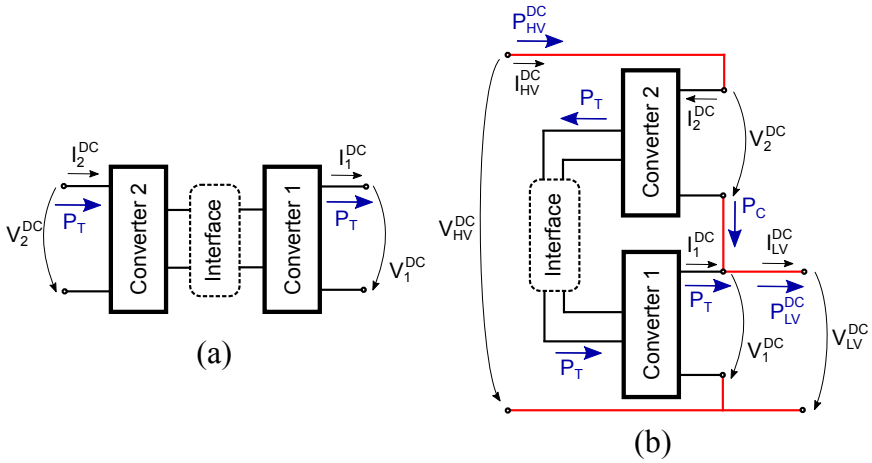

Fig. 8.1: DC/DC interconnectors. (a) DC/DC transformer. (b) DC/DC autotransformer.

with the DC/DC transformer concept of Fig. 8.1(a). The following analysis assumes no losses in the converters. The voltage ratio of the DC/DC transformer of Fig. 8.1(a) is:

$$n_T = \frac{V_2^{DC}}{V_1^{DC}} = \frac{I_1^{DC}}{I_2^{DC}} \tag{8.1}$$

The voltage ratio of the DC/DC autotransformer corresponds to:

$$n_{AT} = \frac{V_{HV}^{DC}}{V_{LV}^{DC}} = \frac{V_2^{DC} + V_1^{DC}}{V_1^{DC}} = \frac{I_{LV}^{DC}}{I_{HV}^{DC}} = n_T + 1 \tag{8.2}$$

The total power of the DC/DC autotransformer is:

$$P_{HV}^{DC} = P_{LV}^{DC} = P_T + P_C \tag{8.3}$$

Then, P_T can be expressed as:

$$P_T = P_{LV}^{DC} - P_C = P_{LV}^{DC} - V_1^{DC} I_2^{DC} = P_{LV}^{DC} - \frac{P_T}{n_T} \tag{8.4}$$

Rearranging (8.4), it is possible to obtain:

$$P_T = \frac{n_T}{n_T + 1} P_{LV}^{DC} = \frac{n_{AT} - 1}{n_{AT}} P_{LV}^{DC} \tag{8.5}$$

From (8.5), P_C corresponds to:

$$P_C = P_{LV}^{DC} - \frac{n_T}{n_T+1} P_{LV}^{DC} = \frac{P_{LV}^{DC}}{n_T+1} = \frac{P_{LV}^{DC}}{n_{AT}} \tag{8.6}$$

Fig. 8.2 illustrates the power distribution in the DC/DC autotransformer as a function of the voltage ratio between DC sides, n_{AT}. Consequently, the fraction of P_T that will be transformed by the converters, which determines their rating, depends on the voltage relation between DC sides. The higher the n_{AT}, the lower the P_C and the higher will be P_T for the same output DC power P_{LV}^{DC}. Therefore, the DC/DC autotransformer concept is specially attractive when low ratios n_{AT} are considered since the transformed power, P_T, will be lower, and so will be the rating of the Converters 1 and 2 for the same total DC power.

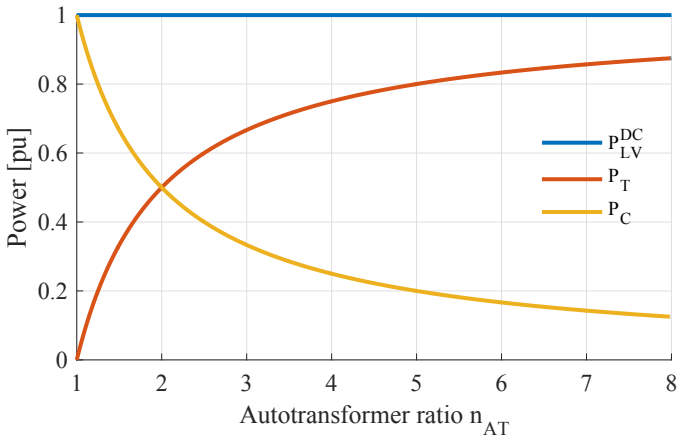

Fig. 8.2: Power distribution inside the DC/DC autotransformer as a function of the voltage ratio between DC sides, n_{AT}.

8.3 Transformerless DC/DC converter

The DC/DC converters presented in [88–91] are based on the DC/DC autotransformer concept introduced in Section 8.2. The previous works consider three-phase Modular Multilevel Converters (MMC) for Converter 1 and 2, both composed of half-bridge submodules and the interface that connects them is a three-phase AC transformer. Due to the converter structure of the DC/DC autotransformer, the AC transformer is expected to have a rel-

evant cost as it is floating at a certain DC voltage level and more insulation is required. This work analyses the replacement of the AC transformer in the interface for an AC filter with the aim of reducing the total cost of the DC/DC converter. Fig. 8.3(a) shows the DC/DC autotransformer composed of MMCs with an AC transformer as the interface, while Fig. 8.3(b) depicts the Transformerless (TL) also with MMCs and with an AC filter as the interface.

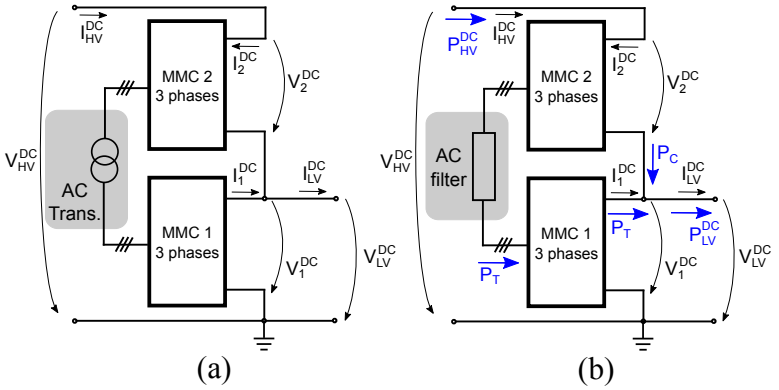

Fig. 8.3: Scheme of the DC/DC autotransformers based on three-phase MMCs. (a) Topology with an AC transformer as the interface. (b) Transformerless (TL) topology using an AC filter (LC) as the interface.

This work considers an asymmetrical monopole scheme, though other configurations can be possible. Besides other topologies of Converter 1 and 2 can be used, however, considering high voltage applications, this work assumes MMCs.

8.3.1 AC filter purposes

The purposes of the filter in the TL topology are similar to the AC transformer ones:

- The filter should enable the power transfer path between the AC side of MMC 1 and 2.
- It needs to allow the energy balancing of the capacitors in the submodules between arms in both converters through the AC side.
- It must block the DC voltage component in order to avoid the DC current, so that a capacitor is needed in series between the two MMCs.

One of the filter's drawbacks is that it does not have the ability to adapt the AC voltages in such a way as the AC transformer does. Therefore, the maximum AC voltage amplitude that can be modulated in the AC side of the MMCs is limited by the lowest DC voltage of both converters. The objective is to have the highest possible value of AC voltage in order to reduce the losses for the same power, or what is the same, maximise the modulation factor of both MMCs. For this reason, the attractiveness of the topology decreases when the difference between the DC voltage value of the MMCs increases.

Considering the previous points, it can be concluded that a capacitor in series must be present in the filter to block the DC component. Thus, the following work is based on this assumption. Initially, in order to design the filter in a generic manner, it is assumed to be made of a capacitor, an inductor and a resistance in series with two MMCs. For the following analysis it is assumed that $n_{AT} = 2$ and $n_T = 1$, which is the optimum configuration to maximise the modulation factor. Nevertheless, other voltage relations can be used according to the required application.

8.4 Modelling of the TL converter

8.4.1 Description of the converter

The TL topology under study consist of two three-phase MMCs based on n half-bridge submodules per arm. The IGBTs considered for this study are the StakPak IGBT Module 5SNA 1300K450300 [94] and it is assumed that each submodule is composed of two valves (half-bridge), and each one of them contains n_{series} IGBTs in series. However, other MMC approaches can be used to implement the converters. Three models of the TL topology (detailed, average and simplified), which are described in the following subsections, are developed in order to address the design of the AC filter. The TL topology interconnects two DC grids by means of a short cable at each side. The parameters of the system are illustrated in Table 8.1.

8.4.2 Detailed model

The TL DC/DC converter is modelled using a detailed model of the MMC with n submodules per arm. Each submodule contains two valves, represented as two IGBTs, and a capacitor. The IGBTs in the model are the equivalent of n_{series} IGBTs in series. Each arm includes the arm reactor,

L_{arm}, with the corresponding parasitic resistance, R_{arm}. The model of each MMC is depicted in Fig. 8.4.

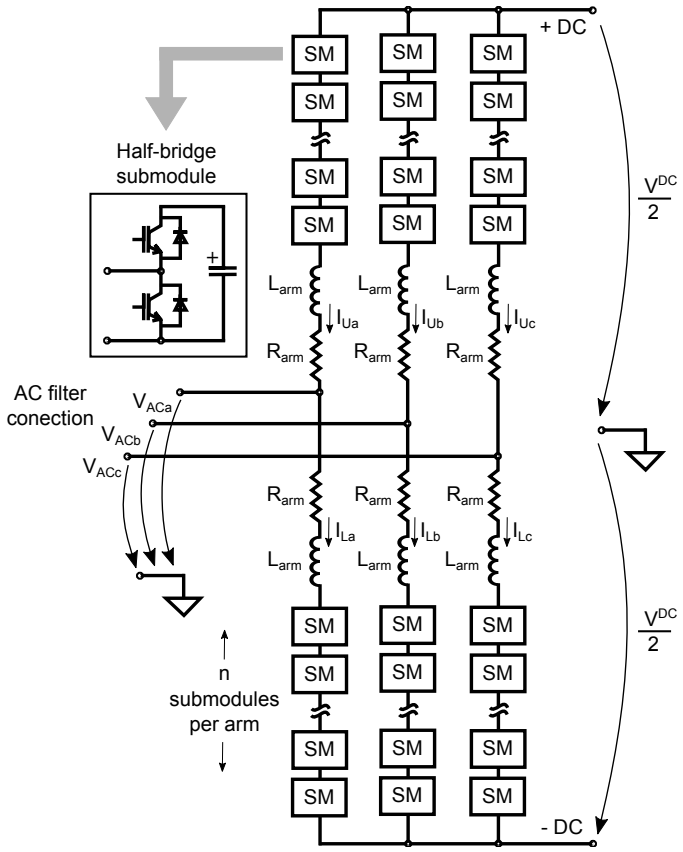

Fig. 8.4: Model of the MMC used in the detailed model of the TL topology.

The three-phase AC filter is modelled as a capacitor, C_m, an inductor, L_m, and a parasitic resistance, R_m, in series with the two MMCs. The DC grids at each DC side of the TL converter are modelled as constant DC voltage sources connected to the TL converter by means of short cable interconnections. The cables are assumed to be 10 km DC cables, which are modelled as π sections.

8.4.3 Average model

This model considers the whole TL converter, as the detailed model, but with a less complex model for the MMCs in order to simulate faster. It pro-

vides a trade-off between accurate results and reduced simulation time. In this case, MMC 1 and MMC 2 are modelled using an average model [95,96], where all the submodules in each arm are replaced by a voltage source. The dynamics of the submodule capacitors is represented in a separate circuit which consists on a current source and an equivalent capacitor for the whole arm. The current source injects in this circuit the same power that is exchanged by the voltage source in the arm, in order to represent the behaviour of charging and discharging the submodule capacitance.

8.4.4 Simplified model

This model of the TL converter considers only one phase of the AC side of MMC 1 and MMC 2. It is used to study specifically the effects on the filter, considering that the whole system is operating at nominal DC power. The starting point to derive the model is the average model used in Section 8.4.3. Then, considering only one phase and applying superposition and the Thévenin theorem at the filter terminals it is possible to obtain a simplified model of the system. Fig. 8.5 shows the average model of one AC phase of the DC interconnector, where the DC cables have been neglected and without including the equivalent capacitor of each arm. The Thévenin theorem is applied between point A and point B and the resulting circuit is shown in Fig. 8.5. The following equations illustrate the Thévenin AC and DC voltage and impedance.

$$V_{th} = \frac{1}{2}(V_{L2} - V_{U2} + V_{U1} - V_{L1}) \tag{8.7}$$

$$R_{th} = \frac{1}{2}(R_{arm2} + R_{arm1}) \tag{8.8}$$

$$L_{th} = \frac{1}{2}(L_{arm2} + L_{arm1}) \tag{8.9}$$

$$V_{th}^{DC} = \frac{V_{HV}^{DC} - V_{LV}^{DC}}{2} + \frac{V_{LV}^{DC}}{2} = \frac{V_{2}^{DC} + V_{1}^{DC}}{2} \tag{8.10}$$

where, V_{U1}, V_{L1}, V_{U2}, V_{L2}, are the upper and lower arm voltages of MMC 1 and 2, respectively, R_{arm1}, R_{arm2}, L_{arm1}, L_{arm2}, are the parasitic resistance and inductance of the arm inductors of MMC 1 and 2, respectively. The resonance frequency of the simplified model is given by:

$$f_{res} = \frac{1}{2\pi\sqrt{(L_{th} + L_m)C_m}} \tag{8.11}$$

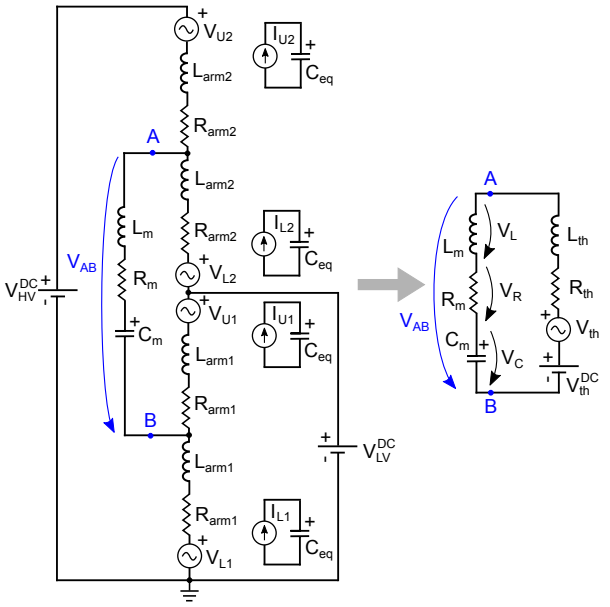

Fig. 8.5: Simplified model of one phase of the AC side of the TL converter obtained from the average model of the MMCs and the filter.

8.5 Control of the converter

The TL converter is used to control the DC power, which is being exchanged between the two DC sides. This power can be controlled by regulating the AC power that circulates through the AC filter, P_T. Then, the power injected into the LV side is $P_{LV}^{DC} = \frac{n_{AT}}{n_{AT}-1} P_T$.

The control implemented in the simulation models consists on regulating the AC voltages of both MMC 1 and 2. MMC 1 regulates the AC voltage with the desired frequency and amplitude. Then, MMC 2 imposes the same AC voltage amplitude but shifts its phase in order to control the active power transmitted between converters, while keeping the reactive power transmission to zero, since both voltages have the same amplitude. The control approach used to regulate the DC voltage of the submodules is described in detail in [97]. It regulates the AC internal voltage of the MMC to the desired value while performing the energy balance of the capacitors in each arm, which is based on an estimation of the capacitor energies.

According to [97], the AC voltage reference given to the control is not the AC voltage at AC converter terminals, but the internal AC voltage generated by the submodules. Considering the equivalent circuit of the MMC

illustrated in [97], which is depicted in Fig. 8.6, the MMC can be represented as a simplified circuit where the voltage generated by the converter between the AC terminal (ac) and the neutral point (n) of the DC side is V_V. This V_V is the result of the AC voltage reference, E_V, given to the control, after the voltage drop due to the half of the resistance and impedance of the arm (see Fig. 8.6). Extending the circuit of Fig. 8.6 to the TL topology, the sim-

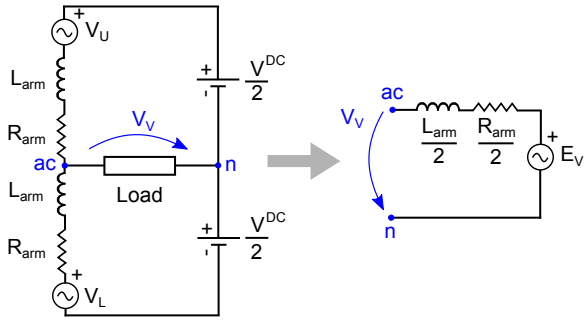

Fig. 8.6: Equivalent model of one phase leg of the MMC according to [97].

plified model of Fig. 8.7 is obtained, which includes the filter and one phase leg of the two MMCs in the TL topology. The circuit of Fig. 8.7 matches with the simplified model of Section 8.4.4 (see Fig. 8.5), but in this case it is seen from the control perspective. E_{V1} and E_{V2} are the desired AC voltages of MMC 1 and MMC 2, which have the same amplitude but different phase, and are the control references given to the controllers of MMC 1 and 2, respectively.

According to the model of Fig. 8.7 and considering phasor notation and neglecting the resistances and the losses of the MMCs, the power transmitted through the filter and the equivalent arm inductances is:

$$P_{ac} = 3\frac{|\underline{E}_{V2}||\underline{E}_{V1}|}{X_{total}}\sin(\delta) = \frac{V_{ac}^2}{X_{total}}\sin(\delta) \approx P_T \tag{8.12}$$

where, $\underline{E}_{V1}$ and $\underline{E}_{V2}$ are the phasor AC voltage references for MMC 1 and 2, respectively. δ is the phase difference between $\underline{E}_{V2}$ and $\underline{E}_{V1}$, X_{total} is the total reactance of the filter plus the arm inductance of the MMC:

$$X_{total} = \omega(L_{th} + L_m) - \frac{1}{\omega C_m} \tag{8.13}$$

$$\omega = 2\pi f_{ac} \tag{8.14}$$

where, f_{ac} is the AC frequency of the AC voltages generated by the MMCs. Then, assuming that the angle reference is the one of MMC 1 ($\theta_1 = 0$) and P_T is related to P_{LV}^{DC} according to (8.5), the phase of the AC voltage that the MMC has to apply is:

$$\theta_2 = \theta_1 + \delta = \delta = \arcsin\left(\frac{X_{total}\frac{n_{AT}-1}{n_{AT}}P_{LV}^{DC}}{V_{ac}^2}\right) \tag{8.15}$$

So that, the MMCs modulate an AC voltage waveform with equal amplitude but MMC 2 shifts its phase in order to transmit power through the AC filter, and consequently, from one DC side to the other.

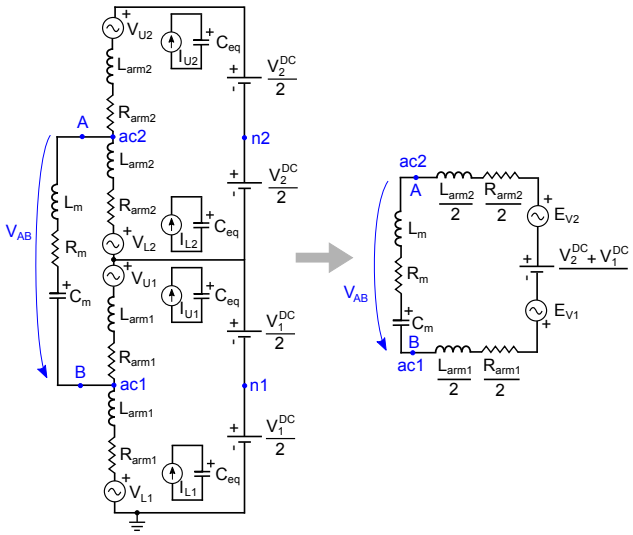

Fig. 8.7: Simplified model of one phase of the AC side of the TL converter from the control perspective explained in [97].

8.6 Filter design

Firstly, this work considers a filter composed only of a capacitor in order to have the simplest possible AC filter ($L_m = 0$ and $R_m = 0$), then, the effects of including an inductor are addressed. The capacitor withstands the DC voltage difference between the two middle points of the MMCs and at the same time has an AC voltage component due to the transmission of AC power through the filter. The DC that the capacitor must withstand is equal to $\frac{V_1^{DC}+V_2^{DC}}{2}$ and it is independent of the C_m used in the filter. However, the

AC component depends on the reactance of the capacitor, and consequently on C_m. The objective of this Section is to determine which is the minimum size of the capacitor in the filter that allows the adequate power transfer. To do so, the limits of the converter linked with the capacitance of the filter are investigated.

8.6.1 Limit 1: active power transfer between voltage sources

This limit comes from the maximum power that can be transmitted between two voltage sources. From (8.13) it is possible to see that varying C_m, X_{total} $\in$ [-∞, ωL_{th}]. The minimum C_m correspond to the minimum X_{total}:

$$X_{total} = \frac{V_{ac}^2}{P_{ac}} \sin(\delta) \tag{8.16}$$

This minimum is achieved when when $\sin(\delta) = -1$ which means that $\delta = -90$. Therefore, the minimum value of C_m is:

$$C_{Lim1} = \frac{1}{\omega \left(\frac{V_{ac}^2}{P_{ac}} + \omega L_{th} \right)} \tag{8.17}$$

8.6.2 Limit 2: apparent power of the MMCs

The reactive power that MMC 1 and 2 can deliver also sets a limit for the capacitance of the filter. The apparent power of MMC 1 and 2 is:

$$S_{ac} = \sqrt{P_{ac}^2 + Q_{ac}^2} \tag{8.18}$$

where, the maximum reactive power, Q_{ac}, can be expressed as:

$$Q_{ac} = \sqrt{S_{ac}^2 - P_{ac}^2} \tag{8.19}$$

The reactive power of the capacitor considering that both MMCs are operating at nominal power is:

$$Q_{cap} = 3X_{cap}I_{ac}^2 = 3\frac{I_{ac}^2}{\omega C_m} = \frac{S_{ac}^2}{\omega C_m V_{ac}^2} \tag{8.20}$$

Taking into account that the sum of reactive powers must be zero and assuming that both MMC 1 and 2 are providing the maximum reactive power,

Q_{ac}:

$$Q_{cap} = 2Q_{ac} \tag{8.21}$$

Then, combining (8.18)-(8.21) yields to the minimum C_m:

$$C_{Lim2} = \frac{S_{ac}^2}{2\omega V_{ac}^2 \sqrt{S_{ac}^2 - P_{ac}^2}} \tag{8.22}$$

8.6.3 Limit 3: modulation limit of the MMCs considering the voltage ripple in the submodules

Considering the previous C_{Lim1} and C_{Lim2} is still not enough to operate properly the TL topology. When considering an AC filter with a capacitor of C_{Lim2}, the voltage ripple in the cell capacitors does not permit to modulate the desired AC waveform in the arm, according to the given parameters. This happens because in some points of the AC waveform, the equivalent voltage of the capacitors in the arm is lower than the AC arm voltage reference. In order to study this issue, the average model of the MMC described in Section 8.4.3 is used. An expression of the equivalent voltage of the arm (gathering all the submodules) is derived following the same procedure than in [98] and it is compared with the AC arm voltage reference, V_{L1} and V_{U1}, for different C_m values. During a transmission of nominal power P_{ac} the MMC that restricts the operation of the TL topology is MMC 1, while if the power transmitted is $-P_{ac}$, the MMC 2 cannot modulate properly the voltage waveforms. The following analysis is performed considering positive power flow and the phase a of MMC 1 is studied, though the results are analogous for the other phases and for the MMC 2.

The internal voltage reference of the MMC 1 is:

$$E_{V1}(t) = m\frac{V_1^{DC}}{2}\cos(\omega t) \tag{8.23}$$

And the AC current at the output of the MMC 1 is defined as:

$$I_{ac1}(t) = \frac{2|S_{ac}|}{3m\frac{V_1^{DC}}{2}}\cos(\omega t + \phi) \tag{8.24}$$

where, m is the modulation factor relating the DC voltage with the AC voltage and ϕ is the angle difference between the internal AC voltage of the MMC 1 and the AC current. Then, according to [98], the powers that are being exchanged in the submodules of the upper and lower arms of phase a

of MMC 1 are, respectively:

$$P_{U1}^{stack}(t) = \frac{P_{ac}}{6m|\cos\phi|}(-1 + m\cos(\omega t))(2\cos(\omega t + \phi) + m\cos\phi) \quad (8.25)$$

$$P_{L1}^{stack}(t) = \frac{P_{ac}}{6m|\cos\phi|}(1 + m\cos(\omega t))(2\cos(\omega t + \phi) - m\cos\phi) \quad (8.26)$$

Then, by integrating (8.25) and (8.26) it is possible to obtain the energy variation of each arm and consequently the voltage equivalent ripple of both arms [98]. The voltage ripple of the upper and lower arm is depicted in Fig. 8.8 and Fig. 8.9, respectively for different capacitance values, C_m, of the filter.

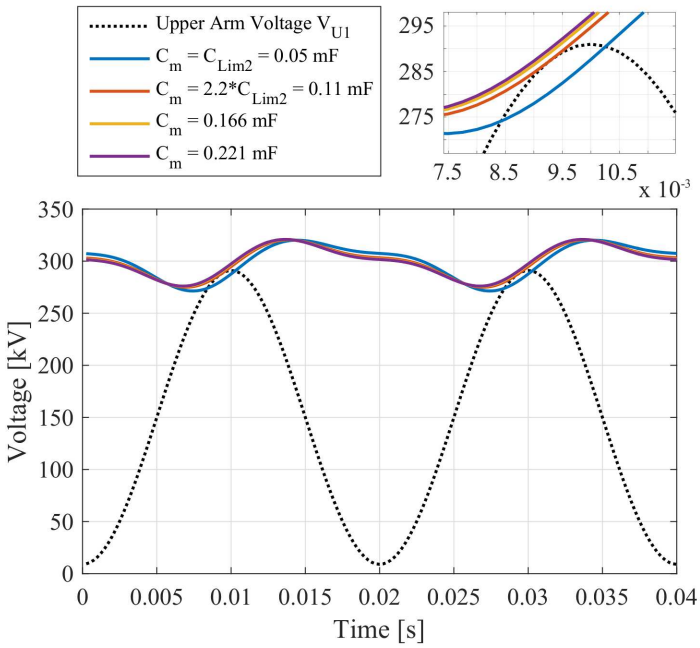

Fig. 8.8: Equivalent voltage ripple of the upper arm for different C_m compared with the voltage reference of the same arm V_{U1}.

This voltage ripple is compared with V_{L1} and V_{U1} which are the voltage that are going to be modulated using the equivalent voltage of each arm. V_{L1} and V_{U1} have both a DC component and an AC component which are

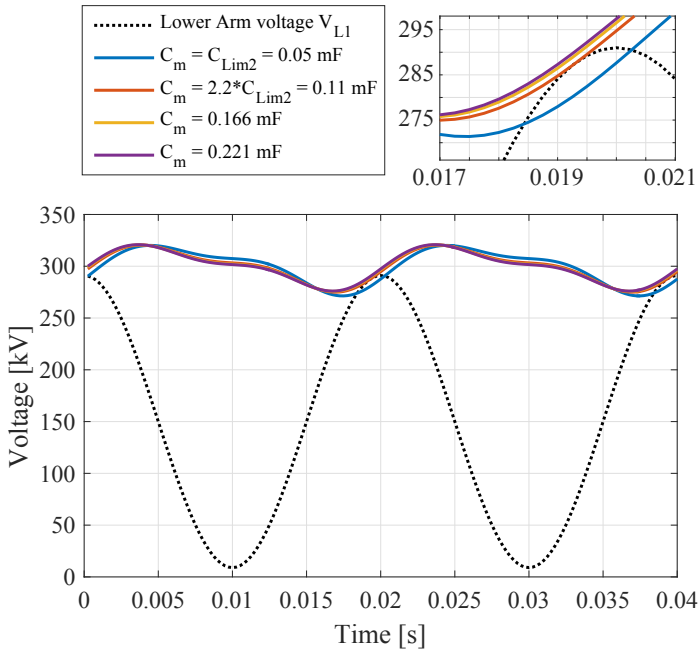

Fig. 8.9: Equivalent voltage ripple of the lower arm for different C_m compared with the voltage reference of the same arm V_{L1}.

related to the internal AC voltage reference in the following manner:

$$V_{U1}(t) = \frac{V_1^{DC}}{2} + V_1^{AC}(t) = \frac{V_1^{DC}}{2} - E_{V1}(t) \tag{8.27}$$

$$V_{L1}(t) = \frac{V_1^{DC}}{2} + V_1^{AC}(t) = \frac{V_1^{DC}}{2} + E_{V1}(t) \tag{8.28}$$

Fig. 8.8 and Fig. 8.9 illustrate that considering the value C_{Lim2} the TL topology cannot operate properly as in some parts of the AC waveforms, $V_{L1}(t)$ and $V_{U1}(t)$, there is not enough voltage in the corresponding arm capacitors due to the ripple. It can be seen that if the C_m increases, the voltage ripple of the arms diminishes, allowing to modulate the voltage waveforms for a value of approximately 2.2 times C_{Lim2} for the parameters considered, which is named C_{Lim3}. The previous relation between C_{Lim2} and C_{Lim3} is shown only to illustrate that C_{Lim3} must be higher than C_{Lim2}, but its relation may change depending on the considered parameters.

Other strategies can be applied to solve this issue, such as increasing the capacitance of the submodules (to reduce the voltage ripple) or decreasing the modulation factor, m. Nonetheless, the first also increases the cost and size of the MMCs and the second increases the AC current, thus increasing the losses for the same power.

Table 8.2 shows the C_{Lim1}, C_{Lim2} and C_{Lim3} for different AC frequencies (25, 50, 75 and 100 Hz) in order to compare the limits of the filter if the TL topology is not operated at 50 Hz. When considering different AC frequencies, some hypothesis are made, such as that the capacitance value of the submodules is chosen to keep the same ripple in the submodule capacitors as in the case of 50 Hz. Additionally, the values of the arm inductance L_{arm} for each MMC are reduced when increasing the frequency. It can be seen that the most restrictive limit is C_{Lim3}, and therefore, the minimum capacitance value C_m of the filter that allows the proper operation of the TL topology.

8.6.4 Steady-state analysis

In this section, an steady-state analysis of the filter variables using the simplified model of Section 8.4.4 is performed for different values of C_m and for the AC frequencies considered before: 25, 50, 75 and 100 Hz. The minimum C_m for each AC frequency are obtained from C_{Lim3} of Section 8.6.3. Fig. 8.10 depicts the resonance frequency, f_{res}, the AC current and the AC voltage of the filter as a function of C_m for the nominal power of the TL topology and for different AC frequencies. The dashed lines depict the limit

C_{Lim3} for each AC frequency. It can be seen in Fig. 8.10(a) that when increasing C_m, the resonance frequency of the filter is reduced and it augments when increasing the AC frequency of the converters. Fig. 8.10(b) shows the RMS value of the AC current that flows through the filter. Firstly, the increase of C_m brings a reduction in the current but when the minimum point is reached it starts to increase again. The minimum AC current point for all the AC frequencies correspond to a capacitance value, C_m, that sets the resonance Frequency to the actual AC frequency. Nevertheless, the reduction of current is not extremely significant as it goes from 905 A to 902.7 A, a drop of 0.25%. Fig. 8.10(c) shows the variation of the AC component in the filter capacitor voltage when increasing its capacitance. It can be seen that it leads to a reduction of the AC voltage, though the DC component is always the same. Increasing the AC frequency also allows to reduce the AC component for the same capacitance C_m.

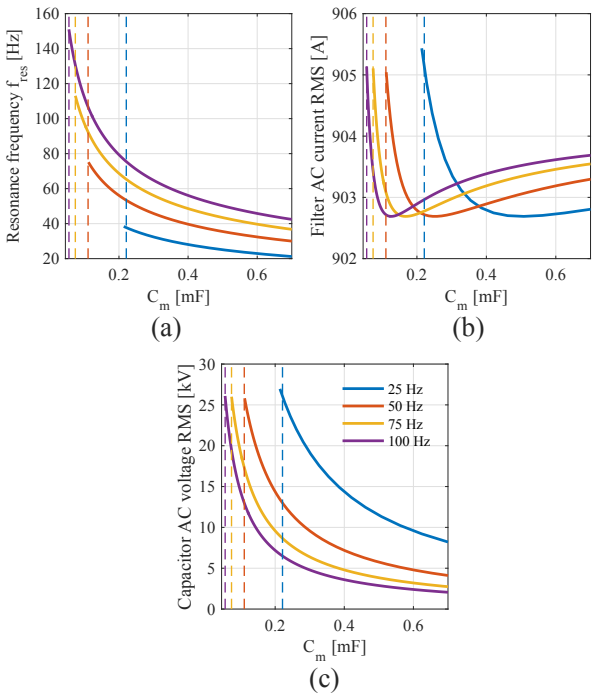

Fig. 8.10: Steady-state analysis of the filter variables considering nominal power. (a) Resonance frequency of the filter f_{res}. (b) RMS value of the AC current through the filter. (c) RMS value of the AC component of the voltage across the capacitor.

Based on the C_{Lim3} of Section 8.6.3, it possible to calculate the limit capacitive reactance of the filter plus the equivalent reactance of the arm reactors of the MMCs that permits the operation of the converter. It can be demonstrated that has the same value for all the AC frequencies:

$$X_{Lim} = \omega L_{th} - \frac{1}{\omega C_{Lim3}} \approx -16.1\ \Omega = -0.153\ \text{pu} \tag{8.29}$$

Besides, knowing that this limit reactance to operate the converter corresponds to (8.29), Fig. 8.11 illustrates how keeping $X_{total} = X_{Lim}$, the capacitance can be diminished if an additional inductor L_m is included in the filter.

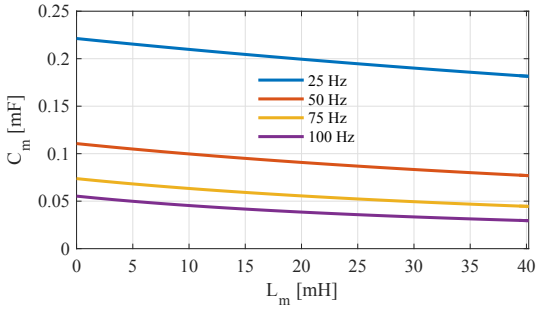

Fig. 8.11: Variation of C_m for a constant value of the $X_{total} = X_{Lim}$ as a function of L_m.

8.7 Dynamic simulations

Finally, the TL topology is tested considering two different approaches for the filter: a filter composed of a capacitor and an inductor, and then a filter made of a capacitor with a value C_{Lim3}. The parameters used for the simulations are illustrated in Table 8.1 (see Section 8.4).

8.7.1 Model comparison: filter made of a capacitor C_m and an inductor L_m

The detailed, average and simplified models of the TL topology are compared considering an AC filter composed of a capacitor $C_m = 1$ mF and an inductor $L_m = 4$ mH. Fig. 8.12 illustrates the results considering the nominal power transfer, showing a good match between models. Fig. 8.12(a) depicts the

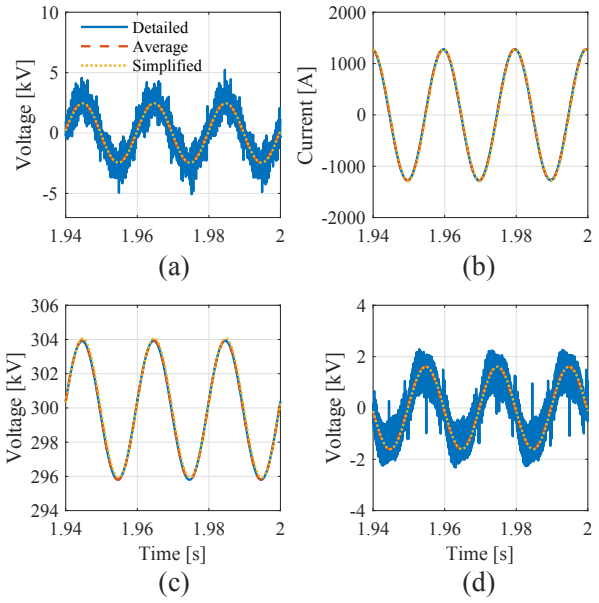

Fig. 8.12: Simulation results showing the comparison between the TL topology models: detailed, average and simplified. (a) Thevenin voltage of phase a V_{tha}. (b) AC current through phase a of the filter I_a. (c) Voltage of phase a across the capacitor of the filter V_{Ca}. (d) Voltage of phase a across the inductor of the filter V_{La}.

applied AC voltage by the two MMC on the filter, showing a good match between the fundamental frequency of the different models. The current that circulates through the filter is shown in Fig. 8.12(b). Fig. 8.12(c) illustrates the voltage of the capacitor in the filter. It can be seen that there are a DC component equal to $\frac{V_1^{DC}+V_2^{DC}}{2}$ and an AC component with a reduced value of 8 kV peak-to-peak. Finally, the voltage across the inductor is shown in Fig. 8.12(d), where the detailed model also presents voltage ripple due to the switching of the submodules.

8.7.2 Detailed model results: filter made of a capacitor C_m

The operation of the TL topology is tested considering a filter made of a capacitor $C_m = 0.11$ mF, the minimum capacitance considering the AC frequency at 50 Hz and according to the analysis of Section 8.6. The results are illustrated in Fig. 8.13 and Fig. 8.14. Fig. 8.13(a) depicts the input and output powers of the TL topology and the power that is being transmitted through the MMCs, P_T. It can be seen, that according to the autotransformer ratio, $n_{AT} = 2$, the power P_T corresponds to the half of the total power transmitted through the TL topology. Fig. 8.13(b) illustrates the DC voltages and Fig. 8.13(c), the active and reactive power of MMC 2. The voltage ripple of the submodules in the upper arm of phase a of MMC are shown in Fig. 8.13(d).

Fig. 8.14(a) shows the voltage at the output of MMC 2 and Fig. 8.14(b) depicts the AC current circulating through the filter. The voltage across the capacitor is shown in Fig. 8.14(c), with a DC component of 300 kV and an AC component of 80 kV peak-to-peak. It can be noted that the DC component is the same as the one in Fig. 8.12(c), however, the AC component, which depends on the capacitance of the filter is different, and it increases when reducing the capacitance, C_m. Finally, Fig. 8.14(d) shows the arm currents of the MMC 2.

8.8 Losses estimation

This section conducts an estimation of the losses of the TL topology, considering the approach with a capacitor in the AC filter ($C_m = 0.8$ mF) and the parameters of Table 8.1. The losses are calculated using analytical expressions as in [99,100] taking into account partial and full load of the converter. The conduction losses and the switching losses of each MMC are calculated (see Fig. 8.15(a) and Fig. 8.15(b)). Then, the total losses of the TL topology

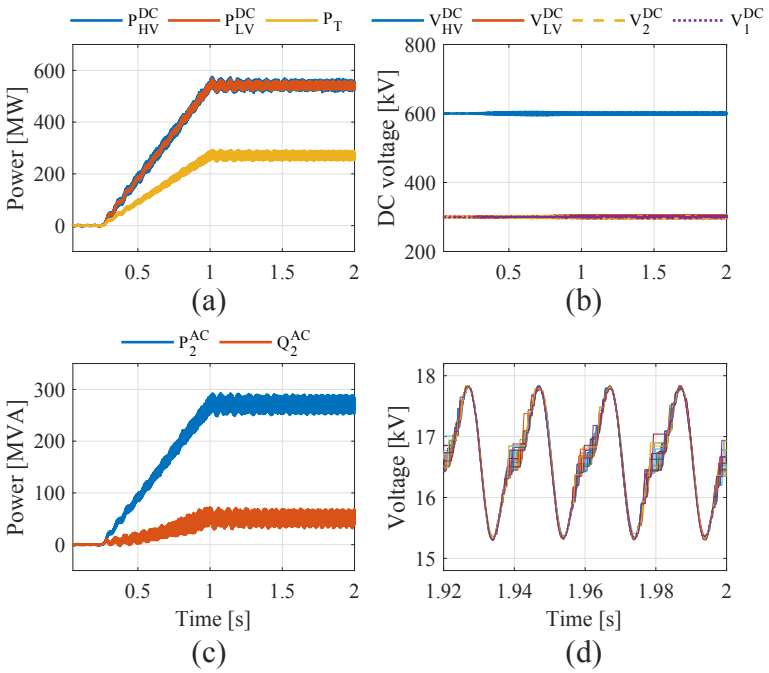

Fig. 8.13: Simulations results of the TL topology using the detailed model. (a) HV side power, LV side power and Transformed power. (b) HV side voltage, LV side voltage, DC voltage of MMC 2 and DC voltage of MMC 1. (c) Active power and reactive power of MMC 2. (d) DC voltage ripple of the submodules of the upper arm a of MMC 2.

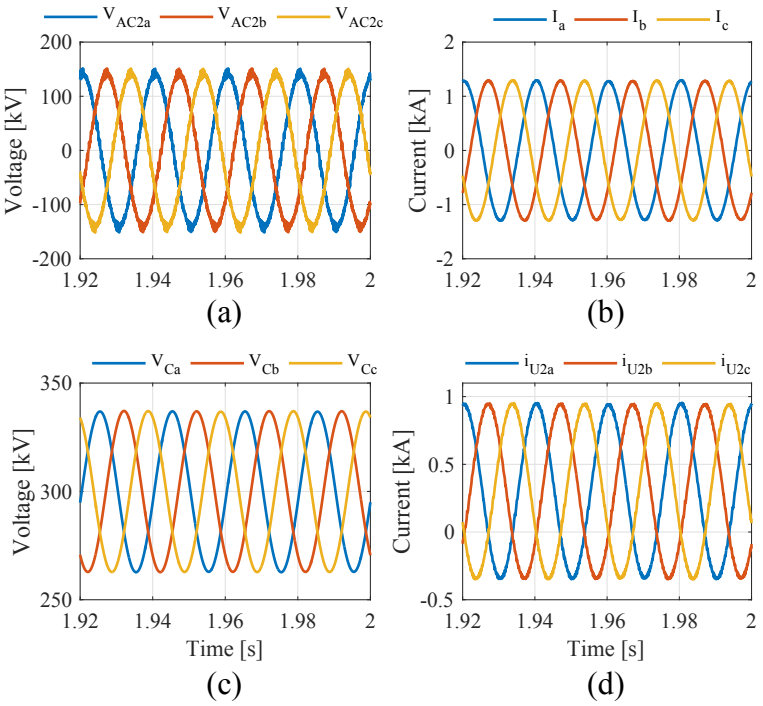

Fig. 8.14: Simulations results of the TL topology considering the detailed model. (a) AC voltages of MMC 2 at the point of the filter connection. (b) AC currents circulating through the filter. (c) Voltages across the capacitor in the filter. (d) Arm currents of the upper arms of MMC 2.

are obtained including the losses in the arm inductors of the MMCs as well (see Fig. 8.15(c)). The losses in the capacitors of the AC filter are neglected in this estimation.

It can be seen from Fig. 8.15(a) and Fig. 8.15(b), that at nominal power, the conduction losses represent 0.39% of the power through the MMCs (270 MW) and the switching losses are lower and correspond to 0.22%. Then, the total power loss in the MMCs is in the order of 0.61% at nominal power.

In Fig. 8.15(c), the losses of the arm inductors are added to the total losses of both MMCs. The total loss of the TL topology at nominal power is in the order of 4 MW, which represents 0.75% of the DC nominal power transfer of the TL topology (540 MW). The calculated efficiency is around 99.25% at full load.

8.9 DC fault considerations

The behaviour of the DC/DC converter in presence of DC faults is a topic that should be correctly address and also its implications in the circuit design. For instance, the work has assumed half-bridge submodules for the MMCs inside the DC/DC converter. However, such submodules do not have the capability to interrupt a DC fault since the antiparallel diodes will uncontrollably start to conduct.

A possibility to face this problem is the insertion of full-bridge submodules in each of the MMCs to permit the current interruption. In spite of solving the DC fault issue, this increases the cost and the losses of the converter.

One of the drawbacks regarding fault behaviour is the presence of a large capacitor (the filter) which stores energy and can be released in the event of a fault.

8.10 Conclusion

This chapter has investigated the design of the AC filter of the TL DC/DC autotransformer topology. Three models of the TL topology have been developed and compared and the control of the converter has been suggested. The first outcome is that a capacitor is required for the filter in order to block the DC voltage component generated by the two MMCs of the TL topology. Then, this work has analysed the converter limits of the TL topology considering only a capacitor for different AC frequencies, concluding that the there is a minimum capacitance (minimum impedance) related to the AC

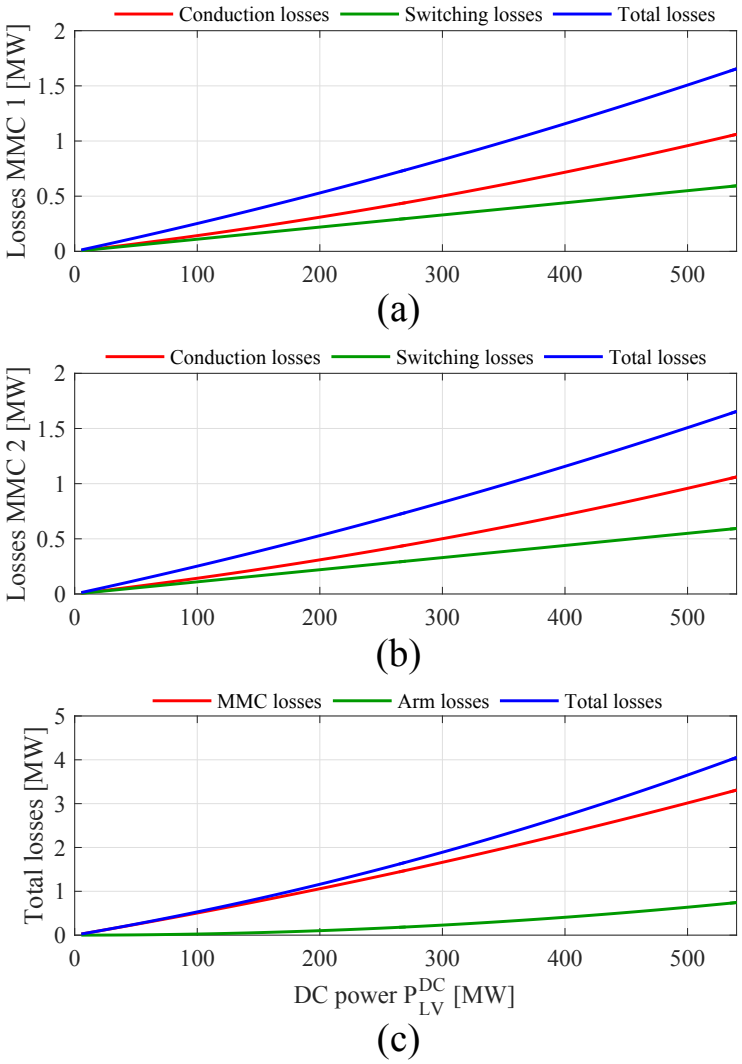

Fig. 8.15: Losses estimation of the TL topology considering the approach with a capacitor as the AC filter. (a) Losses in the semiconductors of MMC 1. (b) Losses in the semiconductors of MMC 2. (c) Total losses of the TL topology.

modulation that can be used in the filter. This minimum capacitance depends also on the AC frequency at which the MMCs operates. By including an inductor in the filter (not necessarily required if MMCs are considered) in addition to the arm inductors, it is possible to slightly reduce the minimum capacitance of the filter. Finally, the TL topology with the minimum capacitance in the filter is validated by means of dynamic simulations.

Table 8.1: System parameters

DC Parameters	Symbol	Value	Units
Interconnector power	P_{DC}	540	MW
HV side voltage	V_{HV}^{DC}	600	kV
Transformer ratio	n_T	1	-
Autotransformer ratio	n_{AT}	2	-
MMC power	P_{ac}	270	MW
LV side voltage	V_{LV}^{DC}	300	kV
AC parameters	Symbol	Value	Units
Base power	S_{ac}	283.08	MVA
Base voltage	V_{ac}	172.69	kV RMS
Base current	I_{ac}	946.41	A RMS
AC frequency	f_{ac}	50	Hz
Base impedance	Z_{ac}	105.35	Ω
Inductive arm impedance	X_{arm}^{pu}	0.12	pu
Arm inductor Q factor	Q_{arm}	30	-
Converter parameters	Symbol	Value	Units
Number of submodules/arm	n	18	-
Number of arms/mmc	n_{arms}	6	-
Number of series IGBTs/valve	n_{series}	8	-
Submodule capacitance	C_{sub}	0.566	mF
Switching frequency	f_{sw}	168	Hz
DC voltage	V_1^{DC}, V_2^{DC}	300	kV
Cable parameters	Symbol	Value	Units
Resistance	R_π	0.146	Ω
Inductance	L_π	1.02	mH
Capacitance	$C_\pi/2$	1.375	µF

Table 8.2: Capacitance limits as a function of the AC frequency of the TL converter

AC frequency f_{AC} [Hz]	25	50	75	100
C_{Lim1} [mF]	0.052	0.026	0.017	0.019
C_{Lim2} [mF]	0.101	0.050	0.034	0.025
C_{Lim3} [mF]	0.221	0.110	0.074	0.055

Chapter 9

Conclusions

This thesis gathers several studies related to the current flow controller devices. In this chapter, the general conclusions of the work done, the specific contributions and future work are detailed.

9.1 General conclusions

Interline DC/DC CFCs present a number of advantages since an AC transformer is not required and the power exchange is done between HVDC lines. It seems research is going in this direction with more concepts being proposed following this approach in the last years. Despite their benefits, the fact of not having an independent power source that allows the insertion of variable voltages in series can restrict its capability to apply variable voltages in series depending on the current flows circulating through the HVDC grid.

The dual H-bridge CFC topology has attracted rather attention from the research community and shows interesting features such as, simple structure, capability to operate with any current direction and easily adaptable to any number of HVDC lines.

Other topologies as the unidirectional interline DC/DC introduced in this thesis, can provide a suitable CFC solution in nodes where the current flow is expected to circulate always in the same direction. The main strength of such CFC is its simplicity in terms of converter structure and control strategy.

The research on the CFCs is not only focused on the converter structures, but also on the use of these CFCs. The idea of having several CFCs in the same grid is being investigated, either with the CFCs operating at the same time or selectively, depending on their location. In this area, selective operation and simpler CFC structures as the one introduced in the thesis can have an added value, since they do not need to operate in any situation, but only in specific cases. The distributed CFC approach can provide a

better control of the current flows in complex meshed HVDC grids as the CFCs can be strategically located in the most suitable nodes.

Also, concerning the operation of CFCs in complex meshed HVDC grids, the CFCs approaches may require current regulation in many HVDC lines. For this reason, multi-port topologies can provide further flexibility in the current regulation. Besides, CFC structures based on MMC are receiving interest as they represent an CFC alternative easily scalable to different voltage levels. The option of integrating the current flow control capability into the DC circuit breakers is being considered in order to have a single device with both functionalities.

Finally, for simple meshed HVDC grids, such as 3-terminal grids, the use of CFCs may not be required. It is in more meshed and complex HVDC grids where the need of these CFC devices lie. Specially, if those complex grids are built from existing point-to-point or multiterminal HVDC systems that have been interconnected. It may be more interesting in those situations, if there is risk of overloading a line, to install CFC devices rather than increasing the power rating of already constructed lines.

9.2 Contributions

The main contributions are listed below:

- Analysis, modelling and control design of the dual H-bridge CFC topology. Analysis of the effect of the device in the operational area of the system. The control strategy has been validated through simulations results.
- Integration of the current flow control capability into an hybrid circuit breaker. Modelling and analysis of the integrated device. Both the normal operation during current regulation and the current interruption functionality of the DCCB with CFC capability have been validated using dynamic simulations.
- Development of an interline DC/DC CFC topology for unidirectional current flows. Development of a extended topology for bidirectional current flows and control design of both converter structures validated through simulations. Building and testing a CFC prototype of the unidirectional topology in an experimental platform.
- Development of the selective operation of DCFC devices and a methodology to assess the effect of a DCFC installed in a certain location.

Analysis on the increase of the operational area of the system using the previous approach. The selective operation of DCFCs is also validated through dynamic simulations.

- Development of a multi-port CFC topology for unidirectional current flows based on the converter structure of Chapter 5.
- Analysis of a transformerless DC/DC converter topology based on the autotransformer concept and design of the AC filter. The system is validated through dynamic simulations.

9.3 Future work

The current flow controllers for meshed HVDC grids are still a relatively new topic, with much research to be done. Besides, the need of such devices is still a future event, since no meshed HVDC grids are built, yet some of them are being planned. CFC devices can also be applied to Medium Voltage (MV) and Low Voltage (LV) DC grids, thus, providing an alternative research line to be considered.

The future work regarding the different chapters of this thesis is listed below:

- Chapter 3:
  - Design the CFC controllers considering improved cable models and compare the impact on the design.
  - Investigate alternative modulation strategies for the CFC.
- Chapter 4:
  - Investigate if the current flow control capability can be added into the DCCB considering other CFC or CB topologies.
- Chapter 5:
  - Perform a quantitative comparison of the proposed CFC and other interline topologies.
  - Analyse the behaviour of the proposed CFC under DC faults or other abnormal conditions.
- Chapter 6:
  - Test the selective operation of DCFCs in an experimental platform.

  - Study the optimum location and number of DCFCs in a certain meshed HVDC grid.

- Chapter 7:
  - Develop a complete control strategy of the multi-port CFC device, including voltage and current loops.
  - Test a multi-port CFC prototype with a higher number of ports in an experimental platform.

- Chapter 8:
  - Perform a design of the AC filter considering the system stability perspective.
  - Build a small scale prototype of the transformerless topology and test it in a experimental platform.

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Appendix A

Operation and control of a current source converter series tapping of an LCC-HVDC link for integration of offshore wind power plants

A.1 Introduction

Traditionally, HVDC employs Line Commutated Converters (LCCs) based on thyristors [101]. LCC-HVDC is a mature and reliable technology with many stations interconnecting mainland and islands, using point-to-point connections. Fig. A.1 shows the existing LCC-HVDC transmission links using undersea cables in the Northern Europe [102]. These links can be located near to potential OWPP, however, one important drawback of HVDC is the difficulty of supplying or injecting reduced amount of power in the vicinity of the HVDC corridor. The HVDC tapping station is a possible solution to overcome this issue, which has been reported in the literature [27, 103, 104]. These HVDC taps can be designed to be bidirectional, thus they are able to inject or consume power and can allow to integrate offshore wind energy without building a whole HVDC link, a key factor in terms of reduction investment. An LCC-HVDC parallel tap based on Voltage Source Converters (VSC) is proposed in [105] for integration of wind power. Nonetheless, it does not allow power reversal in the LCC link while the tapping station is operational. Self-commutating Current Source Converters (CSC) have been considered for high voltage purposes in several papers: [106] presents a CSC based Static Synchronous Compensator (STATCOM), an HVDC link based on two CSCs is introduced in [107], an hybrid system with one CSC and a LCC is proposed in [108] and several cascaded CSCs in both OWPP side and grid side of the HVDC link are suggested in [109], [110]. Several more applications can be found in [111] and it is also considered as a full-power

converter for wind turbines [112–114]. CSC is suitable to be in series with LCC-HVDC as they share some features, for instance, DC current flows always in the same direction and voltage can be bidirectional. CSC technology allows the regulation of active and reactive power independently, it has black-start capability and the required filters are smaller than LCC-HVDC. CSCs require switches with reverse-blocking voltage capability: A diode can be placed in series with the IGBT to achieve this behaviour [115]. Other options are: Reverse-Blocking IGBT (RB-IGBT) with intrinsic diode, Gate Turn-Off thyristor (GTO) and Integrated Gate Commutated Thyristor (IGCT) [116],[117].

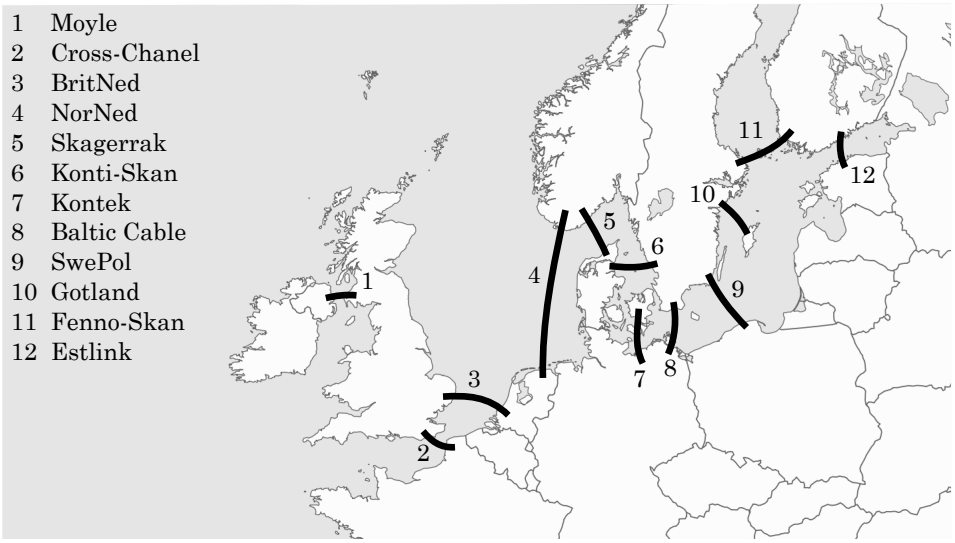

Fig. A.1: Undersea LCC-HVDC transmission links in Northern Europe

This chapter presents a series tapping CSC for integrating offshore wind energy into an LCC-HVDC link and a coordinated control of the CSC and the OWPP is designed. A steady-state analysis considering the modulation limit of the CSC is performed for different voltage levels and powers and after a Power Reduction Algorithm (PRA) is proposed in order to address system control when the CSC is not able to extract all the power from the OWPP. Three scenarios are simulated to test the behaviour of the system: a DC current reduction in the HVDC link with and without the proposed PRA and a loss of communications between the CSC and the OWPP.

A.2 System description

Fig. A.2 shows the LCC-HVDC transmission system and the interconnection of an OWPP by means of a bidirectional CSC connected in series with the HVDC link. The LCCs are twelve-pulse bridges with their two correspond-

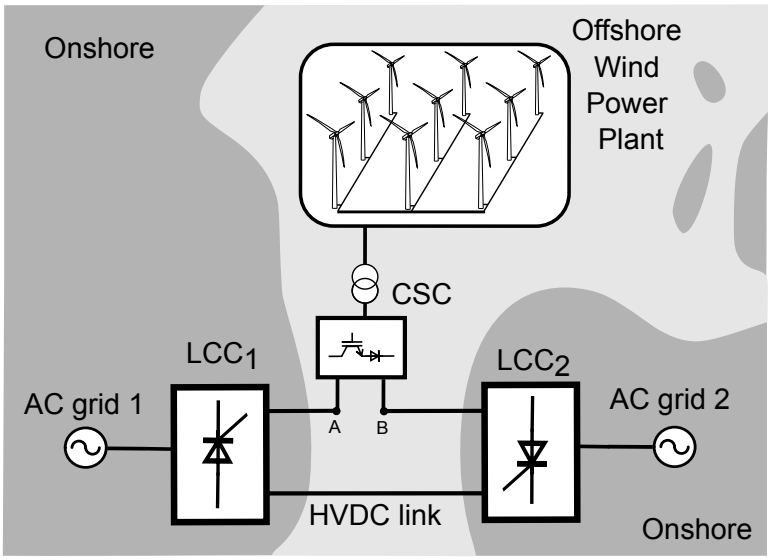

Fig. A.2: System scheme

ing transformers (star-star and star-delta). The converter stations include adequate tuned AC filters and they are connected to two different AC grids. CSC is a two-level converter made of six switches with reverse blocking voltage capability (IGBT with a diode in series) [115]. Finally, the OWPP is composed of m clusters of n turbines each. The wind turbines are based on full-power converter Permanent Magnet Synchronous Generator (PMSG). The system parameters can be found in Tables A.1, A.2 and A.3.

A.3 System modelling

A.3.1 LCC-HVDC transmission system

The modelling of LCC stations is based on the CIGRE benchmark [118]. LCC_1 is acting as a rectifier and LCC_2 is operating in inverter mode.

Table A.1: LCC-HVDC parameters

Parameter	Symbol	Value	Unit
Nominal power	P_{HVDC}	1000	MW
Nominal voltage	V_{HVDC}	500	kV
Nominal current	I_{HVDC}	2	kA
Cable length	l	200	km
Cable resistance	r_{cable}	0.25	Ω/km
Cable inductance	l_{cable}	5.9	mH/km
Cable capacitance	c_{cable}	0.13	µF/km
AC grid 1 voltage	V_{ac1}	345	kV
AC grid 2 voltage	V_{ac2}	230	kV
AC grid 1 inductance	L_{ac1}	0	mH
AC grid 2 inductance	L_{ac2}	16.5	mH
AC grid 1 frequency	f_{ac1}	50	Hz
AC grid 2 frequency	f_{ac2}	50	Hz

Table A.2: CSC parameters

Parameter	Symbol	Value	Unit
Nominal power	P_n	100	MW
Nominal AC voltage	V_c	61.2	kV
AC capacitor	C_{wf}	20.6	µF
HVDC transformer leakage inductance	L_{tr2}	8.14	mH
HVDC transformer resistance	R_{tr2}	0.256	Ω
HVDC transformer relation	r	0.8	-
Switching frequency	f_s	1000	Hz
Equivalent inductance of the OWPP AC grid	L_{eq}	12.8	mH

Table A.3: OWPP parameters

Parameter	Symbol	Value	Unit
Number of wind turbines per cluster	n	4	-
Number of wind turbine clusters	m	5	-
Full-rated VSC voltage	E_{btb}	7	kV
VSC transformer leakage inductance	L_{tr1}	41.59	mH
VSC transformer leakage inductance resistance	R_{tr1}	1.31	Ω
VSC capacitance	C_{btb}	1	µF
VSC coupling inductance	L_{btb}	103	mH
VSC coupling inductance resistance	R_{btb}	1.63	Ω
DBR high voltage level	E_2	1.1	pu
DBR low voltage level	E_1	1.05	pu
DBR value	R_{dbr}	11.86	Ω
Wind turbine power	P_{nom}	5	MW
Wind turbine rotational speed	ω_{nom}	15.7	rpm
Wind turbine inertia	J_t	43.8	Mgm^2
Wind turbine swept area	A	10,568	m^2
Cut-in speed	v_{in}	4.5	m/s
Cut-off speed	v_{off}	25	m/s
Pitch actuator speed	v_{pitch}	±8	°/s
Pairs of poles	p	100	-
Stator inductance	L_s	8.4	mH
Stator resistance	r_s	0.08	Ω

A.3.2 Current source converter

The CSC is modelled as a two-level converter shown in Fig. A.3. A multilevel

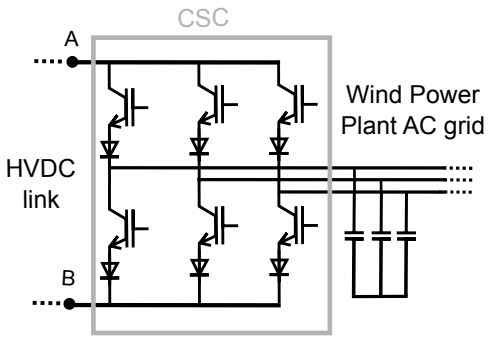

Fig. A.3: Two-level CSC with the AC capacitors

topology can also be considered for the real implementation [32] and the modulation strategy is based on [119]. It is directly connected to the AC capacitors of the OWPP grid as depicted in Fig. A.4.

The plant of the system are the AC capacitors, which can be described in the qd reference as (A.1).

$$\begin{bmatrix} i_{xq} \\ i_{xd} \end{bmatrix} - \begin{bmatrix} i_{mq} \\ i_{md} \end{bmatrix} = \begin{bmatrix} 0 & \omega_e C_{wf} \\ -\omega_e C_{wf} & 0 \end{bmatrix} \begin{bmatrix} v_{cq} \\ v_{cd} \end{bmatrix} + \begin{bmatrix} C_{wf} & 0 \\ 0 & C_{wf} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} v_{cq} \\ v_{cd} \end{bmatrix} \quad \text{(A.1)}$$

where, i_{xqd} is the current modulated by the converter, i_{mqd} is the current coming from the OWPP and v_{cqd} are the components of the capacitor voltage. ω_e is the grid frequency and C_{wf} is the capacitance of the AC capacitors.

The Park's transformation used is:

$$\mathbf{T}(\theta) = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad \text{(A.2)}$$

A.3.3 Offshore wind power plant

Only one single wind turbine is modelled and it is assumed that all wind turbines have the same wind speed in order to simplify the analysis. The wind turbine is modelled using the three blade horizontal axis characteristic and is coupled with a gearless Permanent Magnet Synchronous Generator (PMSG). The machine is connected to a full-rated VSC in *back-to-back* configuration.

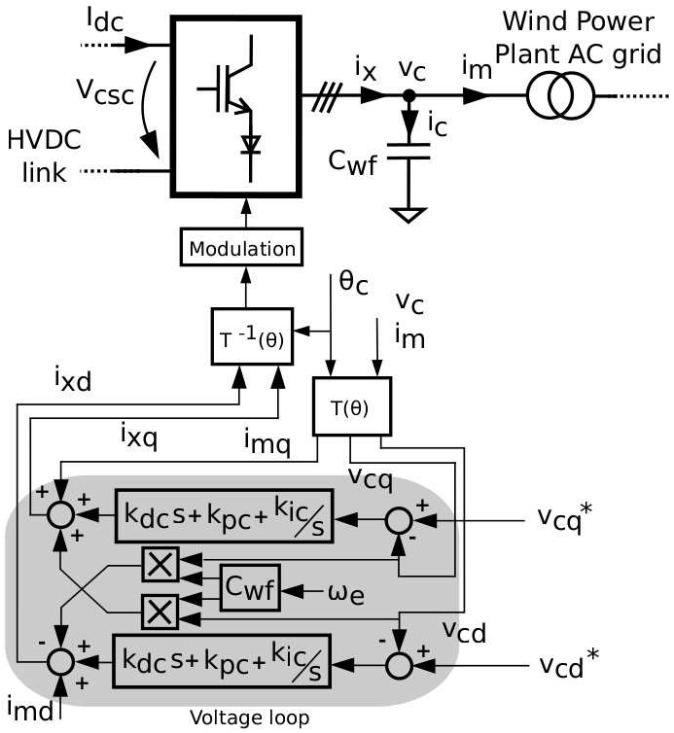

Fig. A.4: Single line and control scheme of the CSC

The behaviour of a whole OWPP is obtained through an aggregate model [120]. Fig. A.5 illustrates the scheme of one wind turbine.

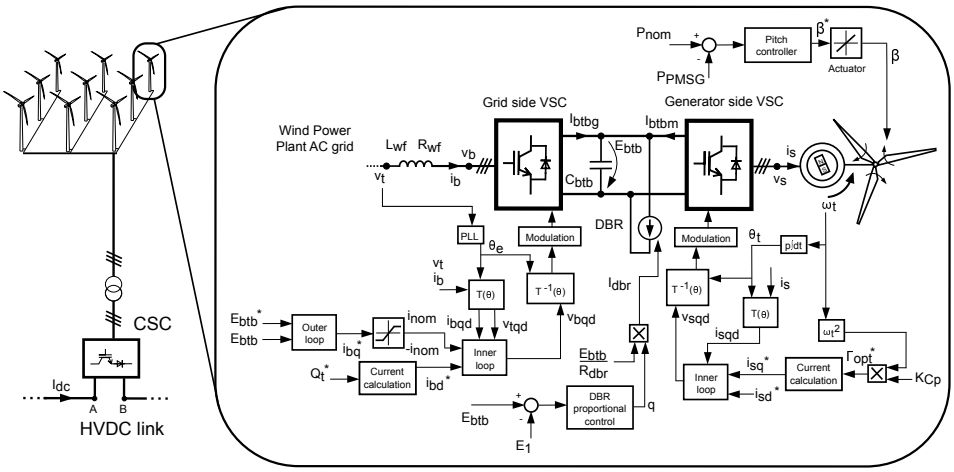

Fig. A.5: Wind turbine control scheme

Wind turbine

The wind turbine is modelled according to the power equation [121]:

$$P_t = \frac{1}{2} C_p p A v_{wind}^3 \tag{A.3}$$

where, C_p is the power coefficient, p is the density of air, A is the swept area of the turbine blades and v_{wind} is the wind speed. The turbine is coupled to a PMSG without gearbox, thus, the transmission equation is [121]:

$$\Gamma_m - \Gamma_e = J_t \frac{d}{dt} \omega_t \tag{A.4}$$

where, Γ_m and Γ_e is the mechanical and electrical torque, respectively. J_t is the inertia of the wind turbine and the PMSG and ω_t is the rotational speed of the turbine.

Generator side VSC

Both VSCs are modelled using the average model described in [122]. The generator side VSC is connected to the PMSG and the system is modelled

using (A.5) [123].

$$\begin{bmatrix} v_{sq} \\ v_{sd} \end{bmatrix} = \begin{bmatrix} r_s & \omega_t p L_s \\ -\omega_t p L_s & r_s \end{bmatrix} \begin{bmatrix} i_{sq} \\ i_{sd} \end{bmatrix} + \begin{bmatrix} L_s & 0 \\ 0 & L_s \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{sq} \\ i_{sd} \end{bmatrix} + \lambda_m p \omega_t \begin{bmatrix} 1 \\ 0 \end{bmatrix} \quad \text{(A.5)}$$

where, v_{sq} and v_{sq} are the stator voltages, r_s and L_s are the stator resistance and inductance, respectively. p is the pole pairs of the generator and λ_m is the flux linkage. The PMSG is based on a round-rotor, therefore, the electrical torque is proportional to q component of stator current (A.6).

$$\Gamma_e = \frac{3}{2} p \lambda_m i_{sq} \quad \text{(A.6)}$$

Grid side VSC

The grid side VSC is connected to the AC grid of the OWPP. The equation describing the system is [124]:

$$\begin{bmatrix} v_{tq} \\ 0 \end{bmatrix} - \begin{bmatrix} v_{bq} \\ v_{bd} \end{bmatrix} = \begin{bmatrix} r_{wf} & \omega_e L_{wf} \\ -\omega_e L_{wf} & r_{wf} \end{bmatrix} \begin{bmatrix} i_{bq} \\ i_{bd} \end{bmatrix} + \begin{bmatrix} L_{wf} & 0 \\ 0 & L_{wf} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{bq} \\ i_{bd} \end{bmatrix} \quad \text{(A.7)}$$

where, v_t is the voltage before the coupling inductances, v_b is the voltage modulated by the converter. i_b is the current through the converter, L_{wf} is the inductance value and r_{wf} is the parasitic resistance of the coupling inductances. The full-rated converter also includes a Dynamic Breaking Resistor (DBR), modelled as a current source, described by equation (A.8).

$$I_{dbr} = \frac{E_{btb}}{R_{dbr}} q \quad \text{(A.8)}$$

where, E_{btb} is the DC voltage of the full-rated converter, R_{dbr} is the resistance value of the DBR and q is de modulation factor of the DBR switch.

A.4 System control design

A.4.1 LCC-HVDC transmission system

The LCC-HVDC link is operated according to the following strategy: LCC rectifier regulates DC current to the nominal value in normal operation while LCC inverter controls the DC voltage. The V_{dc} reference in the inverter is compared with the measured DC voltage of the link, V_2, and introduced in a PI obtaining the firing angle. The I^*_{dc} reference comes from the Voltage

Dependent Current Order Limiter (VDCOL) and it is compared with the measured value and introduced in a PI obtaining the firing angle of the rectifier. The input for the VDCOL is the measured DC voltage of the link, V_1. VDCOL allows to operate the system with low currents when the voltage reference of the LCC inverter is also reduced. It also diminishes DC current reference if a fault appears on the inverter side. Controllers are tuned to achieve a first order response using the average model presented in [125]. A scheme of the control methodology is depicted in Fig. A.6 and the VDCOL is depicted in Fig. A.7.

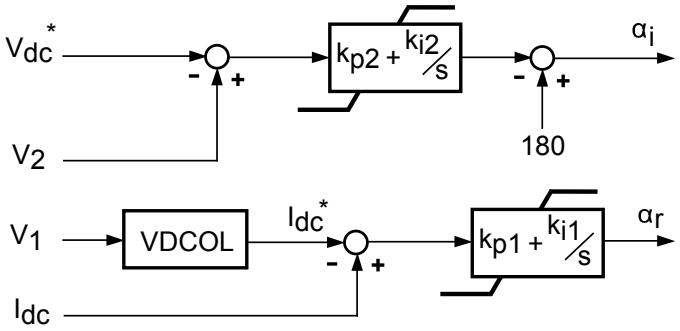

Fig. A.6: LCC transmission system control scheme

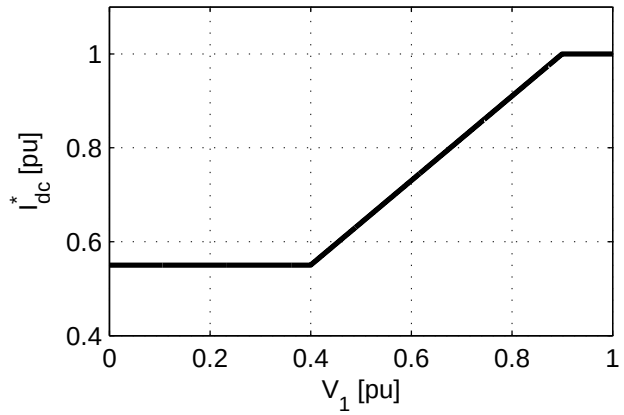

Fig. A.7: VDCOL law

A.4.2 Current source converter

The CSC maintains a constant AC voltage in the OWPP AC grid and it absorbs the incoming power of the OWPP. For this work, it is assumed that all available wind power will be injected into the LCC link independently of the power demand in the LCC transmission system. The control strategy of the CSC is based on the classical vector control and its scheme is based on a voltage loop, which is depicted in Fig. A.4. The system (A.1) is decoupled using (A.9), what leads to (A.10):

$$\begin{bmatrix} i_{xq} \\ i_{xd} \end{bmatrix} = \begin{bmatrix} \hat{i}_{xq} + i_{mq} + \omega_e C_{wf} v_{cd} \\ \hat{i}_{xd} + i_{md} - \omega_e C_{wf} v_{cq} \end{bmatrix} \tag{A.9}$$

$$\begin{bmatrix} \hat{i}_{xq} \\ \hat{i}_{xd} \end{bmatrix} = \begin{bmatrix} C_{wf} & 0 \\ 0 & C_{wf} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} v_{cq} \\ v_{cd} \end{bmatrix} \tag{A.10}$$

where $\hat{i}_{xq}$ and $\hat{i}_{xd}$ are the new decoupled current variables. From equation (A.10), transfer function for the capacitors can be deduced for both qd components:

$$\frac{V_{cq}(s)}{\hat{I}_{xq}(s)} = \frac{1}{C_{wf}s} \qquad \frac{V_{cd}(s)}{\hat{I}_{xd}(s)} = \frac{1}{C_{wf}s} \tag{A.11}$$

The transfer functions of the system are two integrators. Applying Internal Model Control (IMC) technique to tune the controllers to achieve a first order response, a proportional controller is obtained. However, any disturbance introduces steady-state error. For this reason, a IMC methodology improved for disturbance rejection is applied [126], obtaining a proportional-integral-derivative (PID) controller.

A.4.3 Wind turbine

Wind turbine operates following the optimum power curve [121] for low winds. A pitch control and an pitch actuator are included in the system in order to limit power extraction. When the measured electrical power, P_{PMSG}, is exceeding the reference, the pitch control increases the pitch angle to reduce the power extraction and maintain the turbine operating at nominal power, P_{nom}. The Pitch control is designed according *gain scheduling* technique [127]. Fig. A.8 shows the operation characteristic $P_t - v_{wind}$ of the wind turbine [127] and the control scheme of the whole wind turbine is depicted in Fig. A.9.

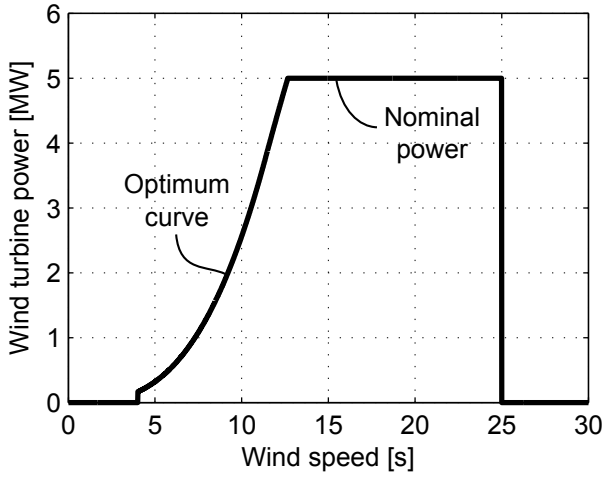

Fig. A.8: Wind turbine characteristic

Generator side VSC

The control design of the VSC is based on the average model of the VSC [122]. The generator side uses the classical vector control and it is operating with *maximum torque control* [123]. The electrical torque is proportional to the q component of the stator current (A.6) and d component of the current is set to 0. It extracts the maximum power of the wind turbine by driving it to the optimal rotational speed, ω_{opt}. The control scheme includes one current loop to regulate q and d components of the stator current. The obtained controllers are two PI designed using IMC methodology [124] in order to achieve a first order response. The control scheme is depicted in Fig. A.9.

Grid side VSC

The control design of the VSC is based on the average model of the VSC [122] and its scheme can be seen in Fig. A.10.

The grid side converter uses the classical vector control with two cascaded control loops [124]: The inner loop controls current qd components independently while the outer loop regulates the DC voltage. Reactive power is kept to 0, controlling i_{bd} to 0.

The PI controllers are also tuned with IMC technique [124]. The Dynamic Breaking Resistor (DBR) is in charge of keeping the DC voltage below its

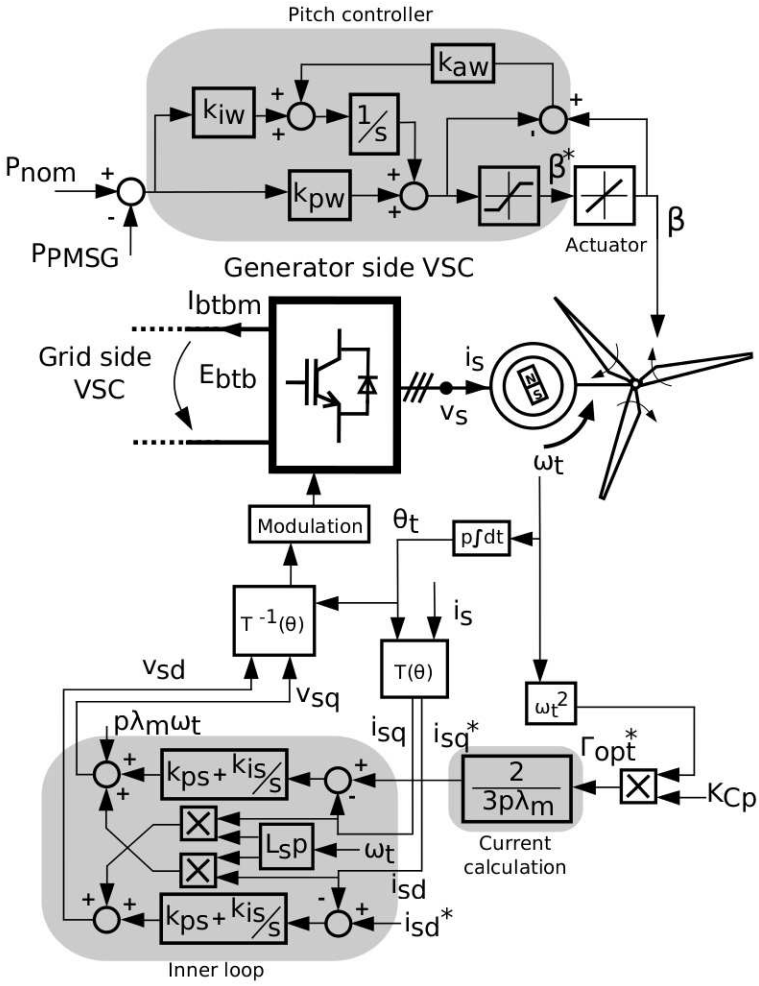

Fig. A.9: Wind turbine and generator side VSC control scheme

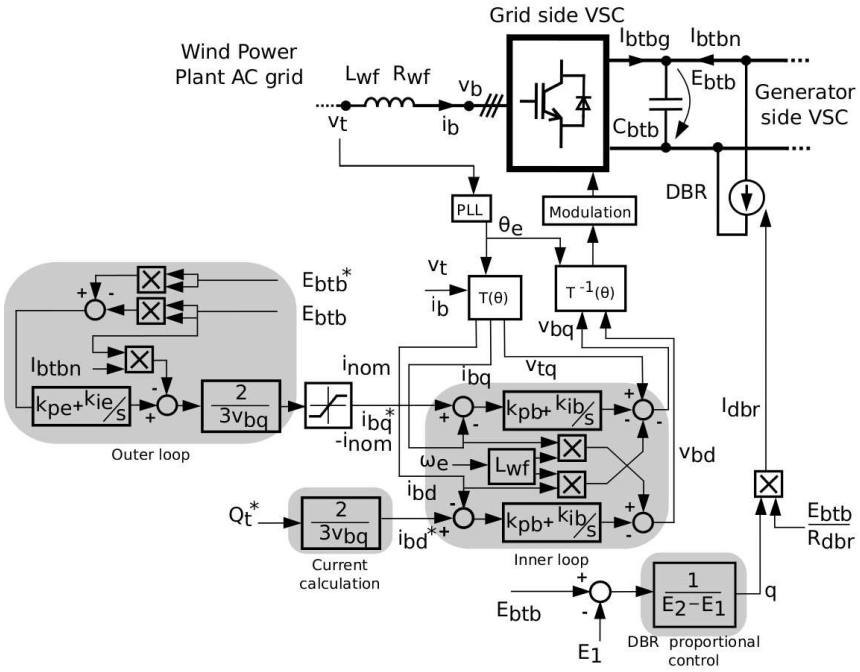

Fig. A.10: Grid side VSC control scheme

maximum value and is activated according a proportional control law when the DC voltage of the VSC, E_{btb}, is within two voltage levels: (E_1 and E_2) [128]. The modulation factor of the DBR switch is described as:

$$q = \frac{E_{btb} - E_1}{E_2 - E_1} \tag{A.12}$$

where, E_{btb} is the measured DC voltage.

A.5 Power reduction algorithm

A.5.1 Steady-state analysis during DC current reduction

CSCs based on self-commutating devices modulate current waveforms, instead of voltage waveforms. For a given DC current, there is a maximum waveform amplitude that the converter is able to synthesise. Equation (A.13) expresses the maximum amplitude of one of the phases [115].

$$i_{x-peak} = \sqrt{i_{xq}^2 + i_{xd}^2} = \frac{\sqrt{3}}{2} M I_{dc} \tag{A.13}$$

where, M is the modulation factor with a maximum value of 1 to work before entering in over modulation [115] and i_{x-peak} is the amplitude of the current waveform. The DC current of the HVDC link varies within a range established by the VDCOL and the power transfer between LCC stations. This fact may limit the injection of wind power in the HVDC transmission system when current is reduced. In order to address DC current reduction and its effects, the following equation system (A.14) is solved:

$$i_{mq}^2 + i_{md}^2 = \frac{3}{4} I_{dc}^2 - 2 i_{md} \omega_e v_{cq} - \omega_e^2 C_{wf}^2 v_{cq}^2 \tag{A.14a}$$

$$P = \frac{3}{2} v_{cq} i_{mq} \tag{A.14b}$$

$$Q = \frac{3}{2} v_{cq} i_{md} \tag{A.14c}$$

$$Q = -\frac{\omega_e L_{eq} (i_{mq}^2 + i_{md}^2)}{2 r^2} \tag{A.14d}$$

where, P and Q are the active power and reactive power at the AC capacitors. L_{eq} is the equivalent inductance of the OWPP AC grid and r is the relation of the transformer between the CSC and the AC grid. Combining equation (A.1) with (A.13) and assuming $M = 1$, (A.14a) is obtained.

(A.14b) and (A.14c) are the active and reactive power, respectively, at the AC capacitors. No losses are considered between the VSCs of each wind turbine and the CSC in order to simplify the steady-state analysis. (A.14d) calculates reactive power considering the equivalent inductance of the OWPP AC grid and the current module after the transformer because it is assumed that each VSC injects no reactive power in the OWPP AC grid. Solving the previous system permits to find the points where the system is operating with the maximum AC current which the converter is able to synthesize.

Relations between P, v_{cq} and I_{dc} are depicted in Fig. A.11 and Fig. A.12 using the results of the previous equations system (A.14a)-(A.14d). Fig. A.11 shows that the higher the DC current, the higher the maximum power that can be extracted from the OWPP. Fig. A.12 shows that AC voltage needs to be higher when there is a DC current reduction in order to inject the same power.

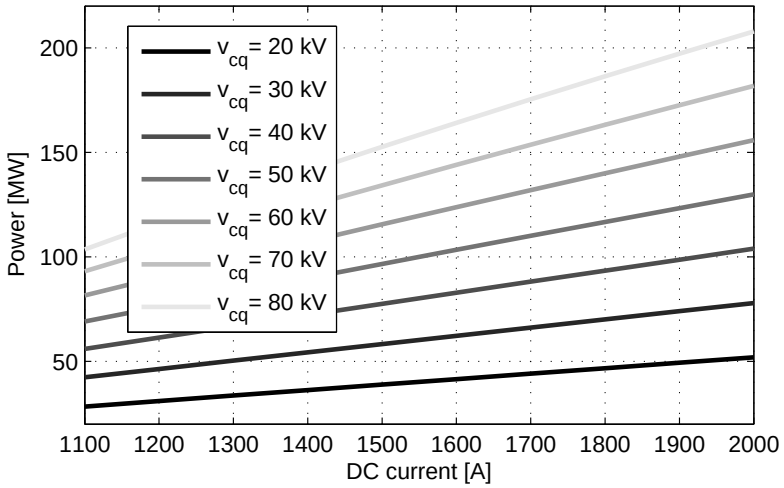

Fig. A.11: Relation $P - I_{dc}$ for different voltages v_{cq}

For this study a V_{cq} voltage of 50 kV has been considered. The chosen voltage allows a power transfer of 69% of nominal power at a DC current of 1.1 kA (minimum value of the VDCOL). When the current rises to 1.6 kA, nominal power of OWPP is guaranteed. In case of need of a power reduction, during a drop of DC current, an algorithm to address this problem is presented in section A.5.3.

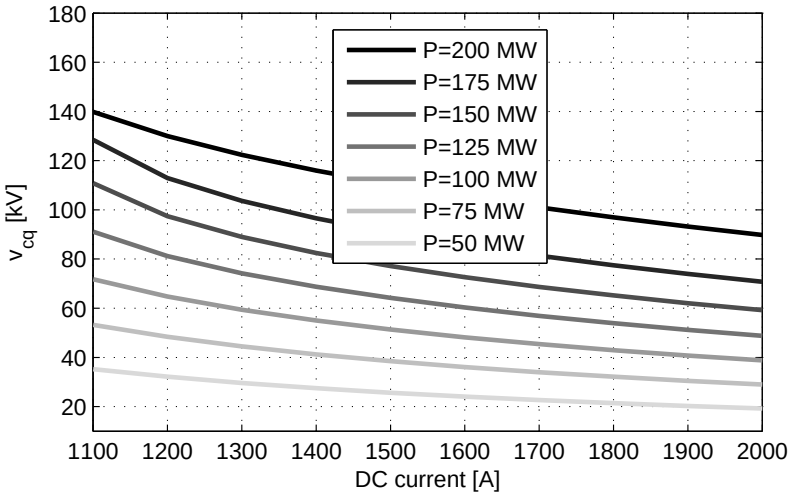

Fig. A.12: Relation $v_{cq} - I_{dc}$ for different active powers P

A.5.2 Considerations on system reliability

The addition of the CSC based series tapping station can decrease the reliability of the system if some measures are not taken into account. A solution more independent in terms of operation can be an HVDC point-to-point connection for the OWPP. Nonetheless, it would require an additional main converter and DC cables of several kilometres, a considerable increase in cost. The main considerations are presented below:

Firstly, the CSC must have bypass switches in order to bypass the converter and allow the operation of the system as a conventional LCC-HVDC link when it is desired.

Secondly, communications between the LCC stations and the CSC are required. For instance, it may be necessary due to market regulation or technical causes that the OWPP modify its power injection. In such situations, both LCC stations should be able to command to the CSC station to initiate or finalise its operation, as well as, changing its power reference.

Finally, the issue raised in Section A.5.1 about DC current reduction is addressed using a power reduction algorithm in Section A.5.3.

A.5.3 Proposed Power Reduction Algorithm (PRA)

Three different approaches can be considered to address the DC current reduction in the LCC-HVDC link: The first approach is to guarantee that

in the worst case (minimum DC current in the HVDC link), the CSC must be able to extract the nominal power of the OWPP. The second approach is introducing a power reduction algorithm in the OWPP to diminish wind power when DC current is low. The third approach is to adapt the VDCOL algorithm to the CSC and OWPP requirements.

The third option is not desirable as the OWPP represents a 10% of the nominal power of the link and the idea is not to modify the control and operation algorithms of the transmission system. The first approach simplifies the control design as it ensures that for any wind power, the CSC is capable of injecting all power into the HVDC link. Nonetheless, it requires high AC voltages in the OWPP that can lead to a cost increase not affordable by the increment in wind power extraction. The second approach permits lower AC voltage but needs an additional power reduction algorithm and communications between the CSC and the wind turbines. For this work, the second approach has been considered and the procedure implemented is as follows.

The first step is saturating the q component of the current of the grid side VSC of each turbine according with maximum value of i_m that the CSC is able to absorb. From (A.14a) and considering the transformer ratio and the total number of wind turbines in the OWPP, the maximum peak value of current injected by each grid side VSC is:

$$i_{cr} = \sqrt{\frac{1}{r^2 m^2 n^2}\left(\frac{3}{4}I_{dc}^2 - 2\omega_e i_{md} v_{cq} - \omega_e^2 C_{wf}^2 v_{cq}^2\right)} \tag{A.15}$$

where, i_{cr} is the maximum value of the q component of the current through grid side VSC of each turbine, i_b. r is the transformer ratio, m is the number of wind turbine clusters and n is the number of wind turbines in each cluster. This current limitation is transformed in a power limitation by means of the expression (A.16).

$$P_{cr} = \frac{3}{2} v_{tq} i_{cr} \tag{A.16}$$

This power limitation is assumed to be shared equally by all wind turbines. Pitch control also receives the new power reference, P_{cr}, and chooses the minimum value between this one and the nominal power of the turbine P_{nom}. The power reference sent to the pitch controller is set to be lower than P_{cr} in order to have a better control of the VSC voltage by the grid side VSC. A value of a 95% of P_{cr} has been set after performing an heuristic analysis. Then, it increases pitch angle to limit power extraction. Pitch control is much slower than current control in the VSC, therefore, the generator side

VSC is absorbing wind power but it cannot be injected into the AC grid. This leads to a transient increase of the DC voltage of the back-to-back converter. A DBR is used to eliminate the exceeding power during these few seconds. During loss of communications between the CSC and the wind turbines, the wind turbines set the power reference to the worst possible scenario (the power that the CSC is able to inject for a DC current of 1.1 kA). Fig. A.13 shows the control scheme of one wind turbine with the power algorithm implemented.

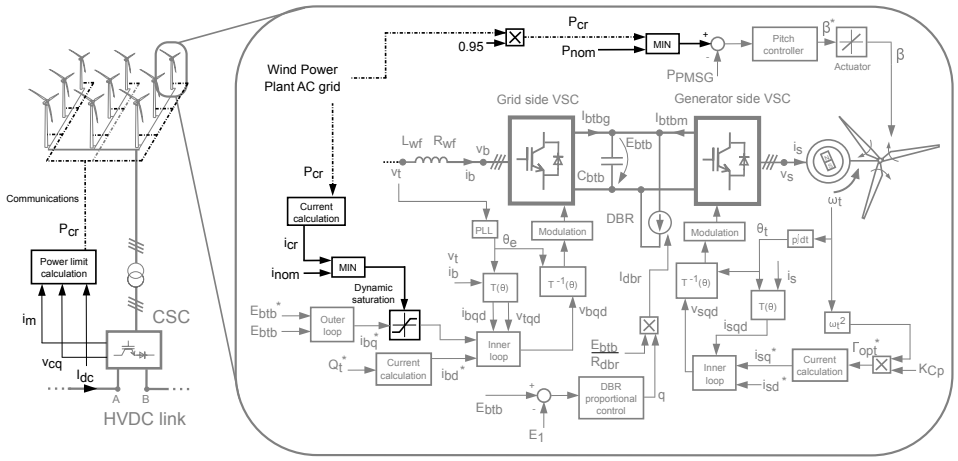

Fig. A.13: Wind turbine control scheme with the proposed power reduction algorithm

Several other approaches could also be considered: For instance, current could be saturated in the generator side VSC, which is equivalent to limit the electric torque. Then, the rotor of the PMSG would be accelerated and the pitch control also would increase pitch angle to keep the turbine below nominal power. This strategy avoids the DBR to be activated and the exceeding energy is used to accelerate the turbine increasing its mechanical stress. A combination of both ideas can also be an option. Nevertheless, they are not considered in this study since mechanical analysis is not performed.

A.6 Dynamic simulations

The simulations are performed considering switching models for LCCs and CSC, and average models for VSCs. The system parameters used for the simulations are listed in Tables A.1, A.2 and A.3 and Table A.4 shows the

Table A.4: Control parameters

Parameter	Symbol	Value
LCC rectifier proportional constant	k_{p1}	0.0315
LCC rectifier integral constant	k_{i1}	0.9053
LCC inverter proportional constant	k_{p2}	1.7e-7
LCC inverter integral constant	k_{i2}	0.0010
CSC proportional constant	k_{pc}	0.0091
CSC integral constant	k_{ic}	1.0965
CSC derivative constant	k_{dc}	7.5e-7
Grid VSC inner loop proportional constant	k_{pb}	5.1995
Grid VSC inner loop integral constant	k_{ib}	81.5
Grid VSC outer loop proportional constant	k_{pe}	0.0439
Grid VSC outer loop integral constant	k_{ie}	1.0622
Generator VSC proportional constant	k_{ps}	1.676
Generator VSC integral constant	k_{is}	16
Pitch proportional constant	k_{pw}	8.39e-05
Pitch integral constant	k_{iw}	1.08e-04
Pitch anti-windup constant	k_{aw}	43.6186

control parameters. Section A.6.1 and section A.6.2 present the simulation results of a DC current reduction in the HVDC link with and without PRA, respectively. Section A.6.3 presents the results during a communication loss between the CSC and the OWPP.

A.6.1 Start-up and DC current reduction without PRA

Fig. A.14 depicts the variables of the HVDC link and the CSC station and Fig. A.15 shows the variables of one wind turbine. At the initial instant, the CSC is bypassed and LCC_1 is acting as a rectifier and LCC_2 as an inverter. The voltage of the HVDC link is ramped until its nominal value (see Fig. A.14(a)) while the current is regulated by LCC_1 according to the VDCOL (see Fig. A.14(b)). The system is operating without absorbing power from the OWPP. At instant $t = 3.5$ s the wind farm is energized. Fig. A.14(e) shows how the AC voltage of the AC grid, v_{cq}, is regulated at 50 kV and the DC bus of the full-rated of each wind turbine is raised until the nominal value (see Fig. A.15(e)). During this instant the CSC is consuming power,

thus, component i_{mq} has a positive value as it can be seen in Fig. A.14(f). The generator side VSC starts to apply the maximum power extraction algorithm at $t = 4$ s (see Fig. A.15(b)), and the OWPP starts to inject power into the LCC-HVDC link (see Fig. A.14(c)). Fig. A.14(a) shows a negative voltage for the CSC since it is injecting power to the HVDC link. It can be seen that V_1 is lower than V_2, as part of the power is provided by the CSC (see Fig. A.14(c)). Fig. A.15(a) depicts the wind profile and Fig. A.15(c) the pitch angle of the wind turbine. The power from the generator is shown in Fig. A.15(d) as P_{PMSG} and P_{btb} is the power injected by each full-power converter to the OWPP grid. DC currents inside the full-power converter are illustrated in Fig. A.15(f). The AC voltage and the AC current in the CSC can be seen in Fig. A.14(d) and Fig. A.14(g), respectively. Fig. A.14(g) compares the modulated current of phase a, i_{xa}, with the reference signal for modulation, ${i_{xa}}^*$. It can be noticed that ${i_{xa}}^*$ is lower than the modulation limit, M_{lim}. After instant 7 s, the voltage reference of station LCC_2 is reduced (see Fig. A.14(a)). Fig. A.14(b) depicts how the VDCOL is also diminishing the DC current to 0.55 pu. This current reduction leads to a decrease of the wind power that the CSC is able to inject due to the current modulation. Fig. A.14(h) shows that the reference current, ${i_{xa}}^*$, to extract the power is higher than the modulation limit, M_{lim}. After instant, $t = 10s$, the CSC is not able to control the AC voltage (see Fig. A.14(e)).

A.6.2 Start-up and DC current reduction with PRA

Fig. A.16 and Fig. A.17 show the simulation results considering the same conditions that in Section A.6.1 but with the PRA implemented. Fig. A.16 depicts the variables of the HVDC link and the CSC station and Fig. A.17 shows the variables of one wind turbine. Before instant $t = 7s$ the system is evolving with no difference compared with Section A.6.1. After this instant, Fig. A.16(b) depicts how the VDCOL is diminishing the DC current to approximately 0.55 pu. This current reduction leads to a decrease of the wind power that the CSC is able to inject due to the modulation limit. The power limitation is calculated in the CSC station and sent considering no delays to all the turbines as P_{cr}. Pitch controller increases pitch angle to decrease the extraction of wind power as it can be seen in Fig. A.17(c). Fig. A.17(d) depicts how P_{cr} decreases and achieves a lower value than the power extracted by the generator P_{PMSG}. In this case, the power injected by each VSC *back-to-back* to the OWPP grid, P_{btb}, is saturated also according to the DC current reduction (see Fig. A.17(d)). This leads to a transient increase of the VSC voltage (see Fig. A.17(e)) that activates the DBR during a reduced

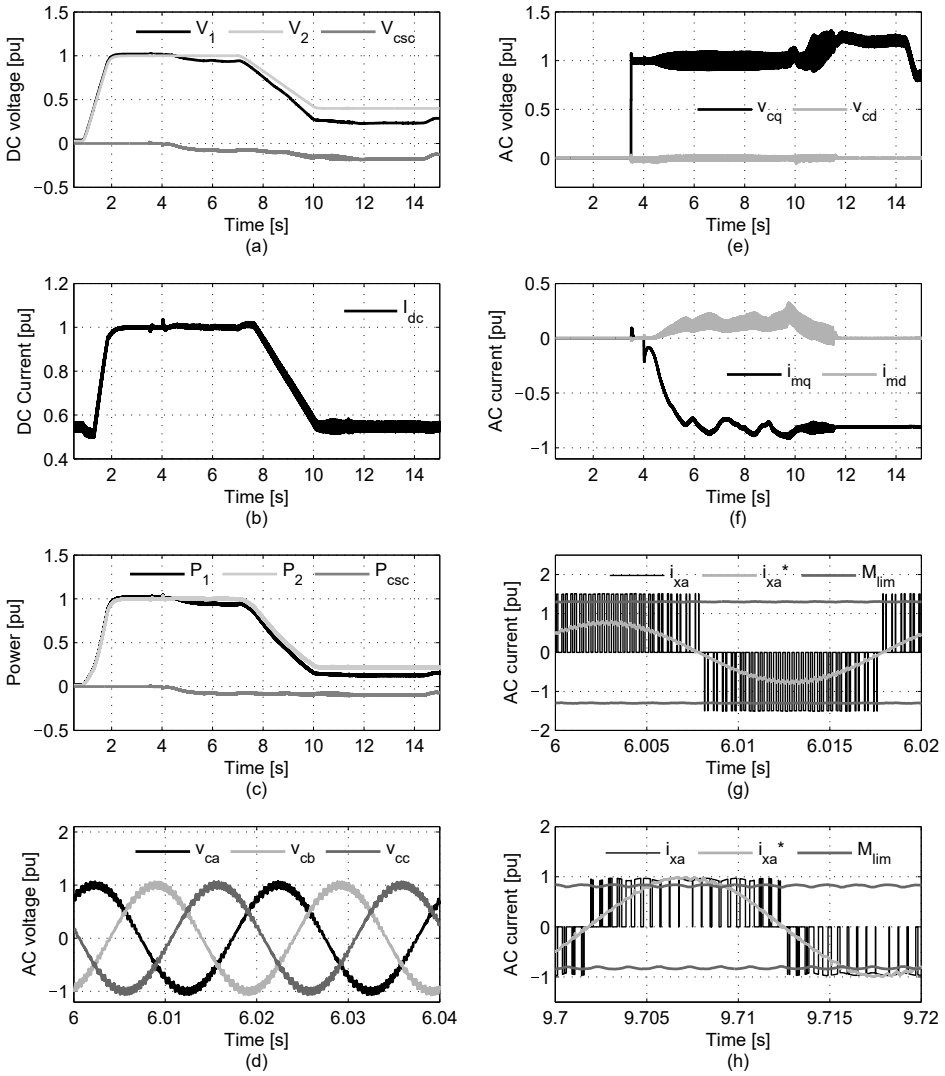

Fig. A.14: Simulation results for CSC start-up and DC current reduction without PRA: LCC-HVDC and CSC variables

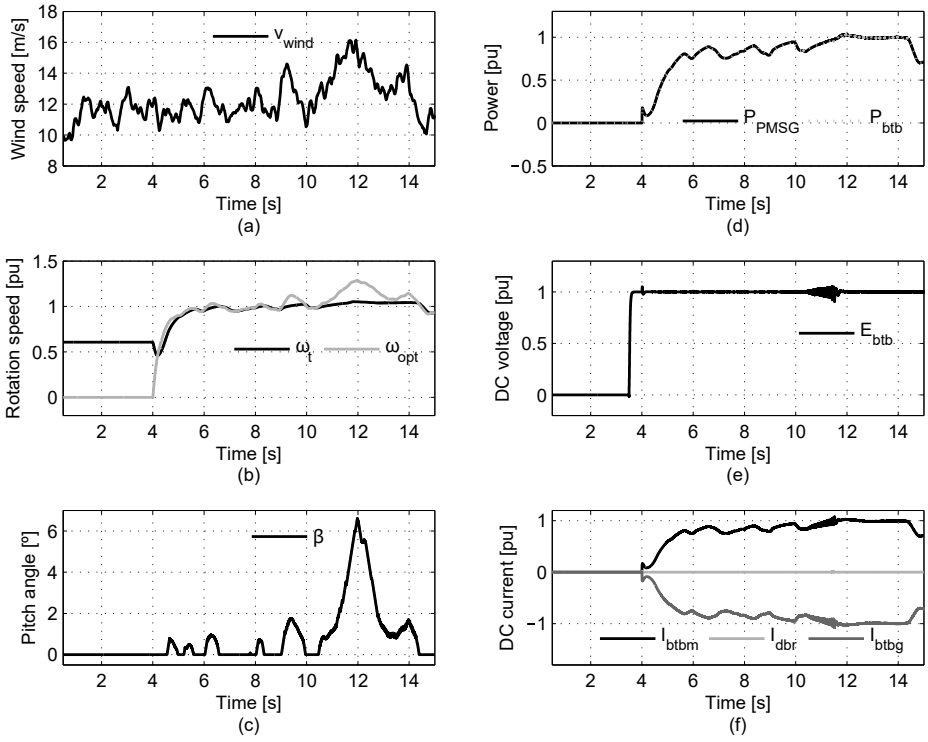

Fig. A.15: Simulation results for CSC start-up and DC current reduction without PRA: Wind turbine and VSCs variables

period of time in order to eliminate the exceeding power. Fig. A.17(f) shows the DC currents in the VSC. I_{btbm} is the current coming from the generator side VSC that has the same value that the current injected into the OWPP AC grid, I_{btbg}, unless during the activation of the DBR. The current through the DBR is depicted as I_{dbr}. In this case, Fig. A.16(h) shows that the reference signal, ${i_{xa}}^*$, reaches the modulation limit, M_{lim}, but it does not increase beyond this limit. As a result, the CSC is able to regulate the AC voltage of the OWPP to the reference level (see Fig. A.16(e)).

A.6.3 Communication loss

Fig. A.18 and Fig. A.19 show the simulation results for a loss of communication between the CSC station and the wind turbines. Fig. A.18 depicts the variables of the HVDC link and the CSC station and Fig. A.19 shows the variables of one wind turbine. At instant $t = 2$ s, there is a loss of communications and they are restored at $t = 10$ s. During this scenario the CSC is applying a negative voltage in the HVDC link (see Fig. A.18(a)) in order to inject power. Fig. A.18(b) shows how the LCC_1 is regulating the DC current to the nominal value. A fraction of the power demanded by terminal LCC_2 is provided by the CSC as it can be seen in Fig. A.18(c) while it is controlling the AC voltage of the OWPP to a constant value (see Fig. A.18(d)). Fig. A.18(e) shows the component q and component d of the current coming from the OWPP and illustrates a decrease of current due to the loss of communications. Fig. A.18(f) also shows the sinusoidal waveform of the AC voltage at the OWPP. Fig. A.19(a) shows the wind speed in each wind turbine. Graphic A.19(b) depicts the rotational speed of the wind turbine and the optimal speed to extract the maximum power. It can be seen that during the loss of communications the VSC drives the turbine to work below the optimal speed in order to reduce the power. Pitch angle in Fig. A.19(c) is also increased to reduce power extraction. In Fig. A.19(d), P_{cr} is presented and is diminished during the communication loss to the minimum value (equivalent to have a DC current of 1100 A). P_{cr} becomes lower than the power of the generator, P_{PMSG}; therefore, the power reduction algorithm is started and increases pitch angle to reduce the power extracted from the wind. The power injected into the AC grid by the VSCs, P_{btb}, is also saturated according to P_{cr}, though, it is set to be a 5% higher in order to have a better control of the DC bus. In Fig. A.19(e) the voltage of the DC bus of each VSC is increasing when P_{PMSG} is higher than P_{cr}. The DC currents of the back-to-back of each wind turbine are presented in Fig. A.19(f). It can be seen that during the first instants after second $t = 2$

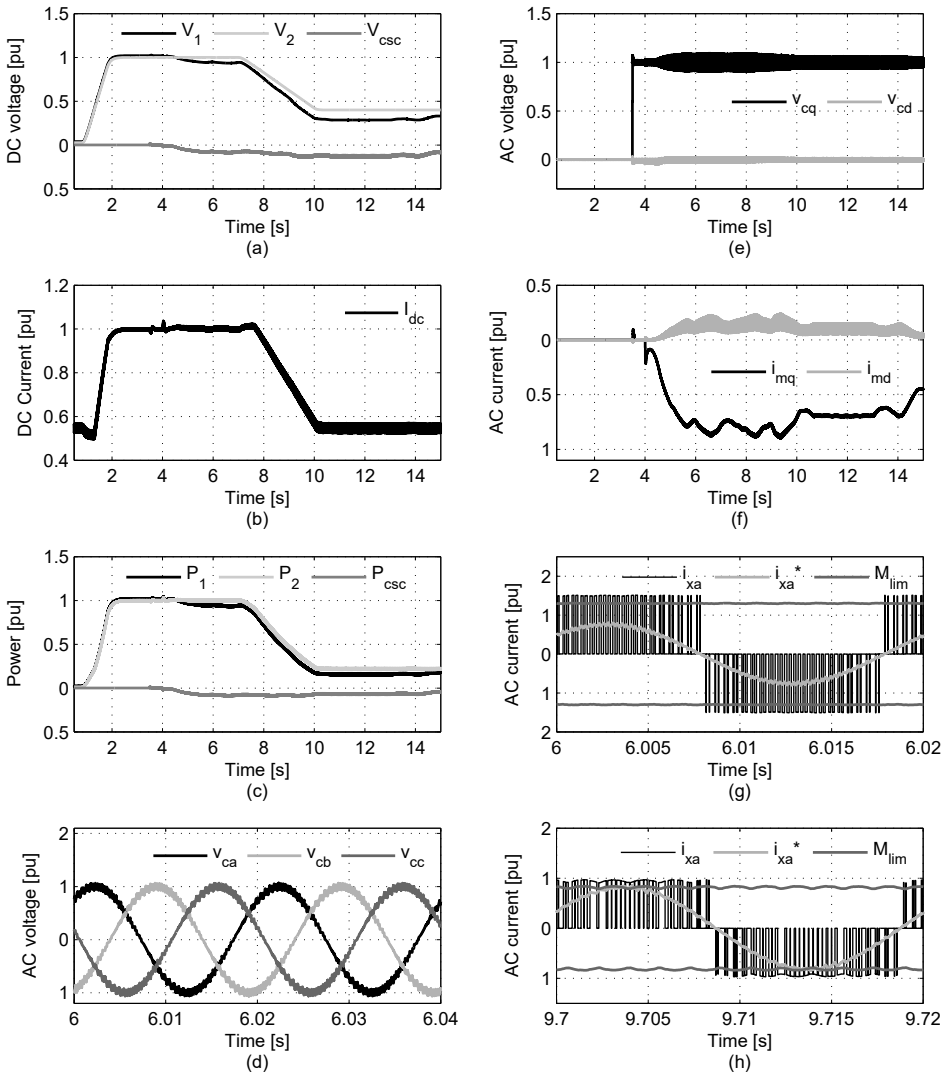

Fig. A.16: Simulation results for CSC start-up and DC current reduction with PRA: LCC-HVDC and CSC variables

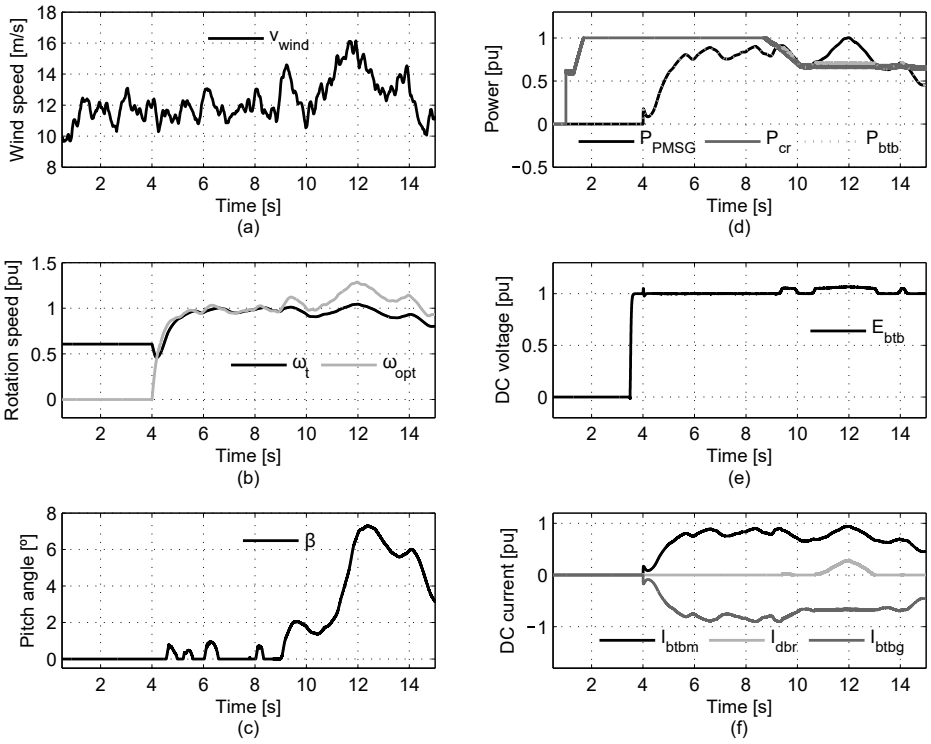

Fig. A.17: Simulation results for CSC start-up and DC current reduction with PRA: Wind turbine and VSCs variables

and before $t = 10$ s, P_{PMSG} is much higher than P_{cr}, thus, the DBR is activated to eliminate part of the power due to the raise of VSC DC voltage. The current extracted by the grid side VSC, I_{btbg}, follows the same shape than the one from the generator side VSC, I_{btbm}, however the first one is lower when the DBR is eliminating power.

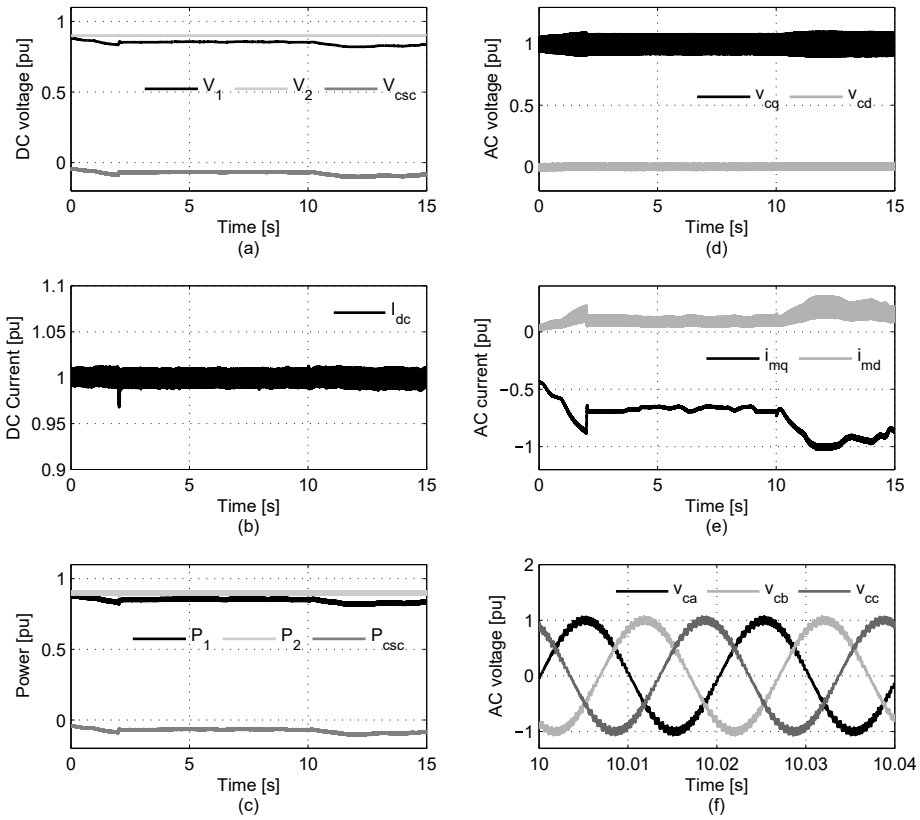

Fig. A.18: Simulation results during loss of communication: LCC-HVDC and CSC variables

A.7 Conclusions

This chapter has analysed the operation and control of a CSC series tapping station in order to integrate offshore wind energy into an LCC-HVDC transmission system. The operation and control is addressed during normal operation, DC current reduction and communication loss. An steady-state

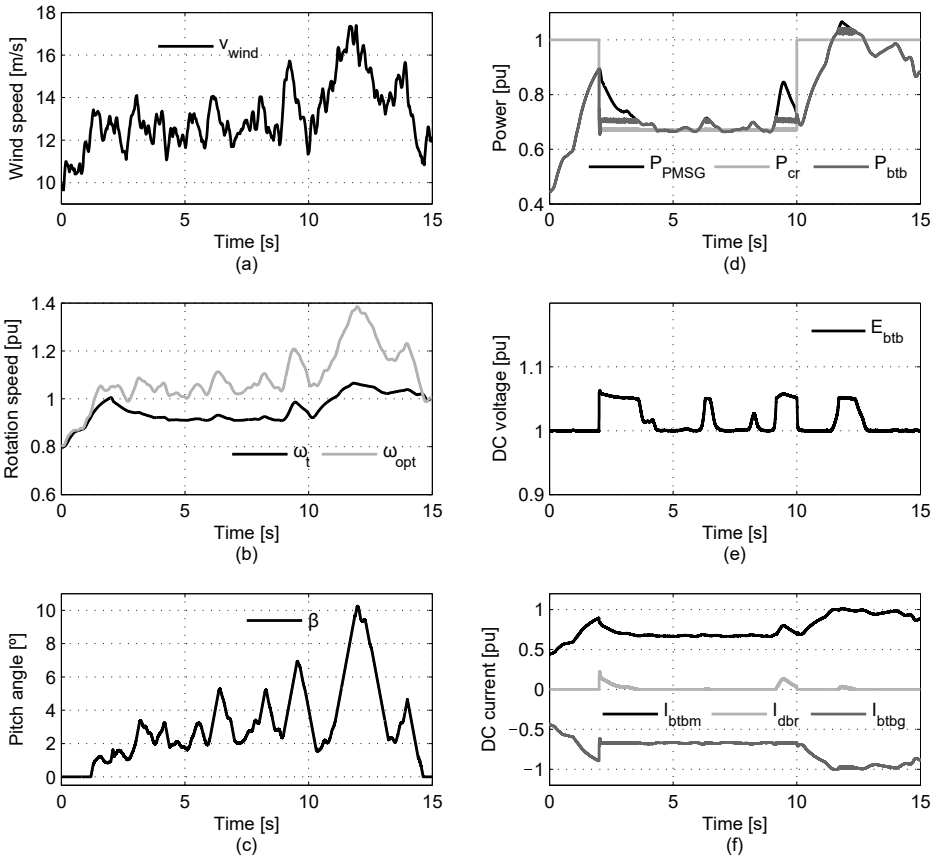

Fig. A.19: Simulation results during loss of communication: Wind turbine and VSCs variables

analysis shows that during DC current reduction in the HVDC link, the capability to inject power into the link is also reduced for a constant voltage in the OWPP AC grid. A power reduction algorithm is proposed to address this scenario. Simulation results during DC current reduction illustrates that the power algorithm reduces the power extraction using pitch control and the grid side VSC injects power according to the maximum current value that the CSC is able to modulate. The DBR is activated to reduce the transient increases in the VSC voltage. Simulation results during communications loss show that the power limitation is set to the minimum value considering the minimum possible DC current in the HVDC link. The system reduces the power injection using the same power algorithm and increases power extraction again when communications are restored. The simulation results validate the operation and control of the CSC and the proposed power reduction algorithm.

Appendix B

Publications

This section presents the publications related to the specific topics of this thesis the author has contributed to.

Journal papers

Published - Included in the thesis

J1 J. Sau-Bassols, E. Prieto-Araujo, O. Gomis-Bellmunt and Fainan Hassan, "Modelling and control of an interline current flow controller for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 32, no. 1, pp. 11-22, Feb. 2017.

J2 J. Sau-Bassols, E. Prieto-Araujo, O. Gomis-Bellmunt and Fainan Hassan, "Series interline DC/DC current flow controller for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 33, no. 2, pp. 881-891, Apr. 2018.

J3 J. Sau-Bassols, E. Prieto-Araujo and O. Gomis-Bellmunt, "Selective Operation of Distributed Current Flow Controller Devices for Meshed HVDC Grids," *IEEE Trans. Power Del.*, vol. 34, no. 1, pp. 107-118, Feb. 2019.

J4 J. Sau-Bassols, E. Prieto-Araujo, S. Galceran-Arellano and O. Gomis-Bellmunt, "Operation and control of a Current Source Converter series tapping of an LCC-HVDC link for integration of Offshore Wind Power Plants," *Electric Power Systems Research*, vol. 141, pp. 510-521, Dec. 2016.

J5 O. Cwikowski, J. Sau-Bassols, B. Chang, E. Prieto-Araujo, M. Barnes, O. Gomis-Bellmunt and R. Shuttleworth, "Integrated HVDC Circuit Breakers With Current Flow Control Capability," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 371-380, Feb. 2018.

Published - Not included in the thesis

J6 J. N. Sakamuri, J. Sau-Bassols, E. Prieto-Araujo, O. Gomis-Bellmunt, M. Altin, A. D. Hansen, N. A. Cutululis, "Experimental validation of frequency control from offshore wind power plants in multi-terminal DC grids", *CIGRE Science & Engineering*, vol. 10, pp. 95-112, 2018.

J7 A. Mokhberdoran, J. Sau-Bassols, E. Prieto-Araujo, O. Gomis-Bellmunt, N. Silva and A. Carvalho, "Fault mode operation strategies for dual H-bridge current flow controller in meshed HVDC grid," *Electric Power Systems Research*, vol. 160, pp. 163-172, Jul. 2018.

J8 M. Aragüés-Peñalba, J. Sau-Bassols, S. Galceran-Arellano, A. Sumper and O. Gomis-Bellmunt, "Optimal operation of hybrid high voltage direct current and alternating current networks based on OPF combined with droop voltage control," *Int. Journal of Electrical Power & Energy Systems*, vol. 101, pp. 176-188, Oct. 2018.

Submitted

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Patents

P1 Inventors: F. Hassan, J. Sau-Bassols, E. Prieto-Araujo, O. Gomis-Bellmunt. "Current Flow Controller", PCT WO 2016/055580, 2016.

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P-C1 Presentation of "Current Source Converter series tapping of a LCC-HVDC transmission system for integration of offshore wind power plants" in *5th HVDC Doctoral Colloquium*, London, UK, Jul. 2014.

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P-C4 Presentation of "Selective operation of current flow controller devices for meshed HVDC grids" in *9th HVDC Doctoral Colloquium*, Barcelona, Spain, Sept. 2018.