A VGA Linearity improvement technique for ECG analog front-end in 65nm CMOS

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***Abstract*— This paper presents a 65nm CMOS low-power, highly linear variable gain amplifier (VGA) suitable for biomedical applications. Typical biological signal amplitudes are in the 0.5-100mV range, and therefore require circuits with a wide dynamic range. Existing VGA architectures mostly exhibit a poor linearity, due to very low local feedback loop-gain. A technique to increase the loop-gain has been explored by adding additional feedback to the tail current source of the input differential pair. Stability analysis of the proposed technique was undertaken with pole-zero analysis. A prototype of Analog Front End (AFE) has been designed to provide 25-50dB gain, and post-layout simulations showed a 15dB reduction in the harmonic distortion for 20mV pk-pk input signal compared to the conventional architecture. The circuit occupies 3,108µm^2 silicon area and consumes 0.43µA from a 1.2V power supply.**

Keywords— offset, bias, stability, noise, electrode, body bias, linearity.

I. Introduction

In the medical world, Electrocardiogram (ECG) machines are very widely used to capture the electrical activity within the heart. These systems can be used short-term for diagnosis, as well as long-term for patient condition monitoring, for instance, following a heart attack. Long-term monitoring is also essential to detect, characterize and diagnose conditions such as cardiac arrhythmias [1]. As is self-evident, it is vital that these systems capture the electrical signals from the heart extremely accurately. When designing such systems, it is important to consider any trade-offs between such things as power-consumption (in the case of portable systems), accuracy and noise immunity etc. In addition to these considerations, intelligent ECG design is receiving more attention these days because an on-chip processor can perform signal filtering and data analysis. An intelligent ECG processor consists of an analogue front end (AFE), followed by the digital processing unit. If we consider the body to be an electrical generator of signals, the ECG electrodes can be considered the interface to the ECG system [2], the fundamental role of the electrode being to change the voltage from its ionic form in the body to its electrical form in the wires. There are two types of electrodes used, dry or wet, sometimes called polarizable or non-polarizable.

A typical ECG system consists of several AFE's, a multiplexer to allow multichannel processing, and a comparatively low-speed, but reasonably high-resolution (~10bit) analogue to digital converter (ADC) to convert the ECG signals from the analogue and into the digital domain for later digital signal processing (DSP) and data compression (if necessary). A variable gain amplifier is must to improve the dynamic range of the AFE.The rest of the paper is organized as follows: Section II introduces the AFE design challenges; Section-III explains the problems with existing VGA architectures; Section IV explains the proposed architecture; Section V summarizes the prototype silicon results.

II. Analog Front End challenges.

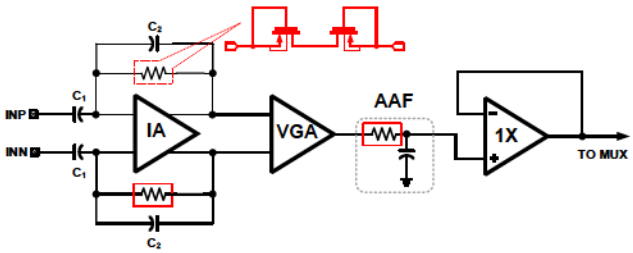

Fig. 1. Analog Front End schematic (AFE)

ECG signals are very weak, ranging in magnitude from 1µV to 10mV, and a bandwidth of the signals ranging from 0.1Hz to 1KHz. There is also interference on the signals, such as power supply noise and crosstalk amongst the differing channels. There could be several channels to simultaneously capture signals from different parts of the heart. The purpose of the AFE, therefore is to detect the incoming signals without adding significant noise, and whilst rejecting any common-mode/unwanted signals. Fig:1 shows a typical AFE architecture. The AFE receives the signal from electrodes, which, as mentioned earlier, can be as small as a microvolt. Additionally there could be a DC offset of up to 200mV, which could easily saturate the AFE. AC coupling is often used to nullify this offset problem, as shown in fig.1. Also, of consideration is the electrode impedance, which is very high, meaning that any leakage from AFE inputs could also generate noise or offset the voltage. The first block in the AFE is an instrumentation amplifier (IA), whose noise must be low enough for accurate signal acquisition. The IA small signal voltage gain must be very high, so that the noise from subsequent circuitry will have less impact on the input referred noise. Hence, we have used an operational transconductance amplifier (OTA) based design, with rail to rail output capability. The IA should also act like a high pass filter with very low cutoff frequency (~0.1Hz), which calls for

very high-value resistors and/or capacitors which would occupy a very large silicon area. For instance, if we could afford the area for a 5pF capacitor, then a resistor value of 610GΩ is required to get the 0.5Hz cut-off frequency. Fortunately, recent advances in the design 'pseudo resistors', based on sub-threshold operated transistors, offer an efficient solution to this problem [3]. In order to achieve the high gain necessary, the Opamp used for the IA is a gain-enhanced cascode amplifier [4]. The IA closed loop gain is defined by the ratio of C_1:C_2. In this design a ratio of 1:0 is needed to achieve a 102.8dB closed loop-gain. Following the IA is a VGA, which varies the gain according to input signal amplitude in order to maintain a fairly constant output voltage range in order to take advantage of the full dynamic range of the following ADC.

III. REVIEW OF EXISTING VGA ARCHITECTURES.

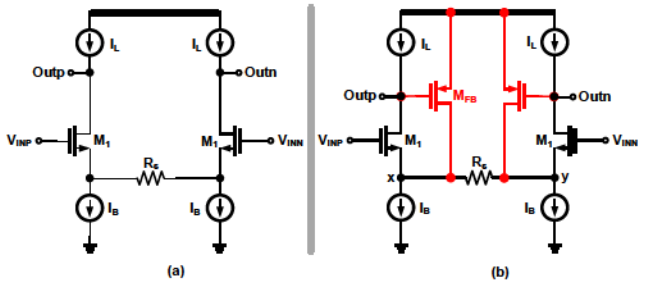

Fig. 2. Conventional VGA circuits

Fig. 2(a) depicts a widely used VGA, where its local series feedback through degeneration resistor R_s will improve the linearity by the extent of the loop-gain ($g_{m1}R_S$). The 3rd harmonic distortion (HD3) is given by (1).

$$HD_3 = \frac{1}{(1+g_m R s_S)^3} \qquad (1)$$

The tail current source is divided into two parts in order to minimize the DC voltage drop across the resistor R_s. This architecture has a few problems [6], one being that the noise of the circuit is much higher than without R_s. This is because without R_s the current source (I_B) noise appears as common mode noise at the output, whereas with the degeneration resistance R_s, each current source will contribute noise. This is because in fig. 2(a) I_B will experience $\frac{1}{g_{m1}}$ and $R_{deg} + \frac{1}{g_{m1}}$ impedances when looking into the transistors M_1 and M_2. The output referred current noise is given by (2).

$$O/p\ noise = 4KT\gamma g_{mt}\left[\frac{R_{deg}+\frac{1}{g_{m_1}}}{R_{deg}+\frac{2}{g_{m1}}} - \frac{\frac{1}{gm_1}}{R_{deg}+\frac{2}{g_{m1}}}\right]$$

$$= 4KT\gamma g_{mt}\frac{g_{m1}R_{deg}}{2+g_{m1}R_{deg}} \sim 2KT\gamma g_{mt} \qquad (2)$$

The second problem is that feedback is only provided by R_s, since it is very difficult to achieve very-high value of loop-gain due to limitations of the maximum R_s and bias current. The third problem is that common mode feedback is needed because of the high common mode output impedance, hence it requires an additional CMFB loop, which adds additional power requirements and area overhead [5][16]. Fig. 3(b) shows another promising architecture with the extra loop-gain [6]. The basic idea is to provide another feedback path in addition to the feedback through R_s. Additional transistors M_{FB} sense the output voltage and feeds back the amplified small signal current into the source of the differential pair input transistors. Hence, this will add extra negative feedback current to the existing feedback current through R_s. The loop gain of the VGA in Fig. 3(b) can be expressed as follows.

$$\text{Loopgain} = G_{mfb}R_S G_{m1}R_o \qquad (3)$$

This architecture has the additional advantage of low common mode impedance due to the presence of the M_{fb} devices, hence no need to have any explicit common mode feedback CMFB loop [8]. Due to the additional feedback transistors, there is a small increase in the noise. When the input signal amplitude is increasing the THD degrades, because the operating point of the transistors will modulate along with the signal[13]. Fig. 3 shows the simulated linearity versus the input amplitude of both conventional architectures described above. As expected the total harmonic distortion (THD) degrades with input amplitude. However, as can be seen, the VGA with only degeneration resistance shows severe degradation compared to the counterpart 2(b), this is because of low loop-gain.

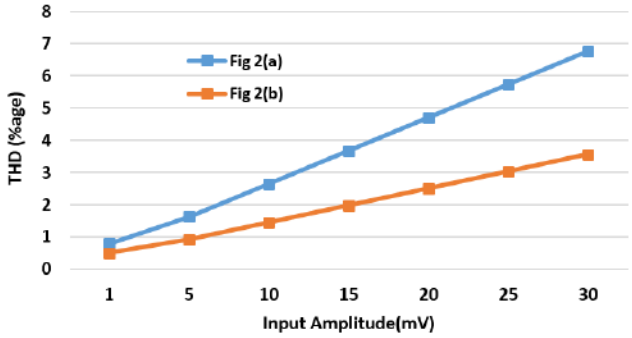

Fig. 3. Linearity of the existing VGA architectures

High sensitive bio-medical AFE linearity should be within around 2.5% for the maximum input signal amplitude; unfortunately none of the above-mentioned architectures are achieving this target. [3] Proposes a low noise and power efficient architecture with a wide range of adjustable gain, but it is has very poor linearity. [5] used a simple differential pair with a variable tail current source to tune the gain; unfortunately this has very poor linearity.

IV. Proposed VGA

As explained in the previous section, high linearity in a VGA is the primary requirement in ECG applications and medical electronic equipment generally, so increasing the loop gain over the existing circuit architectures is the main goal. Let us identify some of the ways to create feedback whilst referring to Fig. 2(b). By sensing the output voltage, the feedback signal can be applied to either differential pair source node (x) or bottom tail current source (I_B). [6] has chosen node x as shown in 3(b) but this will increase the loop-gain by a small amount compared to 3(a) because of the low impedance nature of the node x. One potential solution could be applying feedback to tail current source gate, such that it will amplify the feedback signal by its g_m.

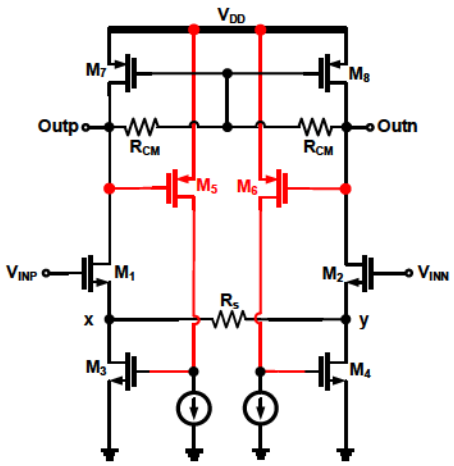

Fig. 4. Proposed VGA

Fig. 4 shows the proposed VGA, where M_1 and M_2 form the input differential pair, R_s forms degeneration resistance, and M_7 and M_8 serve as active-load devices[15]. The potential divider formed by the two resistors R_{CM} sense the output common-mode voltage (V_{CM}) and corrects the gate voltage of M_7 and M_8 such that V_{CM} will be regulated. Transistors M_5 and M_6 senses the output voltage and applies an amplified version to the gates of the tail transistors (M_3,M_4), and corrects at the tail current source gates of M_3 and M_4. The loop-gain can be expressed as follows[18].

$$LG = \frac{g_{m1}}{g_{ds1}+\frac{1}{R_{CM}}} \frac{g_{m5}}{g_{ds5}} \frac{g_{m3}}{g_{ds3}} \qquad (4)$$

Generally, the common-mode voltage sensing resistors are much larger in value than the transistor output impedance ($R_{cm}>1/g_{ds1}$), hence, the loop-gain can be approximated as follows.

$$LG = \frac{g_{m1}}{g_{ds1}} \frac{g_{m5}}{g_{ds5}} \frac{g_{m3}}{g_{ds3}} \qquad (5)$$

Equation (5) reveals that the proposed architecture's loop gain is g_{m5}/g_{ds5} times higher than with the conventional technique [7][17]. Due to the extra loop gain, the harmonic distortion will decrease significantly and HD_3 can be expressed as follows.

$$HD_3 = \frac{1}{\left(1+\frac{g_{m1}}{g_{ds1}+\frac{1}{R_{CM}}} \frac{g_{m5}g_{m3}}{g_{ds5}g_{ds3}}\right)^3} \qquad (6)$$

Unfortunately, a high loop gain decreases the stability of the all-pole feedback loop, so the stability limits must be studied with the help of the transfer-function [12][14]. Fig. 5 shows the differential mode equivalent circuit of Fig. 4, with each node capacitance and resistance. The transfer function can be expressed as follows.

$$LG = \frac{g_{m3}}{g_{m1}+\frac{2}{R_S}+sC_X} \frac{g_{m1}}{\frac{1}{R_O}+sC_O} \frac{g_{m5}}{\frac{1}{R_W}+sC_W} \qquad (7)$$

From the above transfer function, unity gain bandwidth (UGB), 2nd dominant pole and the 3rd dominant pole can be approximately expressed as g_{m3}/C_0, $1/R_WC_W$, and $2/R_SC_X$ respectively. For stable operation, a minimum phase margin of 60^0 must be maintained. By maintaining the 2nd and 3rd dominant pole frequencies much higher than UGB, we could achieve the required phase margin as expressed in (8). By increasing the load capacitance (Co), we could decrease the unity gain bandwidth for a given non-dominant pole location, which makes the VGA stable [9].

$$\frac{g_{m3}}{C_O} < \frac{2}{R_WC_W} < \frac{6}{R_SX} \qquad (8)$$

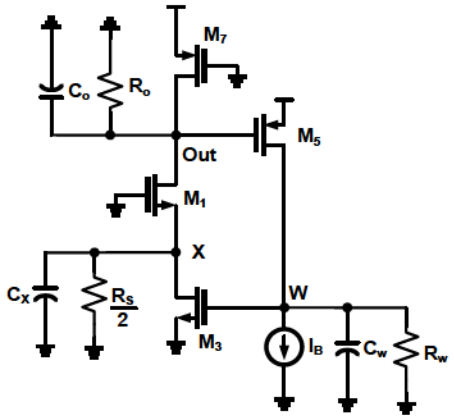

Fig. 5. Differential Equivalent of the Proposed VGA.

V. Simulation Results

The proposed VGA and the traditional IA have been implemented in 65nm CMOS TSMC technology, and post-layout simulations performed with Spectre simulator[20][19]. Fig. 6 shows the loop gain of the feedback system, and the design achieves 62dB at low frequencies, with a 54^0 phase-margin. The nominal gain of the IA is ~30dB, and the VGA gain varies from -5dB to 20dB (by varying R_s). Hence, the AFE total voltage gain range is 25dB to 50dB, which is more than sufficient to provide the required dynamic range for the front-end [2]. Fig. 7 depicts the frequency response of the AFE. It shows the lower cutoff frequency is 0.01Hz, due to the large pseudo resistor. The upper cutoff frequency is ~90KHz,

which is sufficient for all kinds of biological signal capture [11][21].

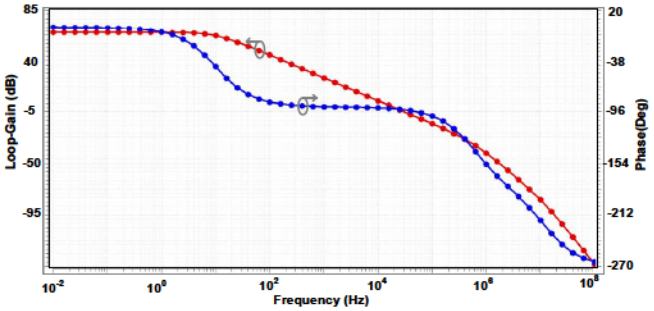

Fig. 6. Open loopgain of the VGA feedback.

To evaluate the linearity improvement of the proposed VGA, a two-tone test has been carried out by appling 9.5KHz and 10.5KHz signals to the IA input and observing the 3rd order intermodulation component amplitude located at 11.5KHz.

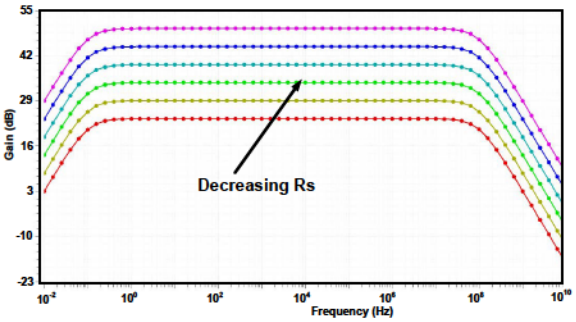

Fig. 7. The Frequency response of the VGA for different gain settings.

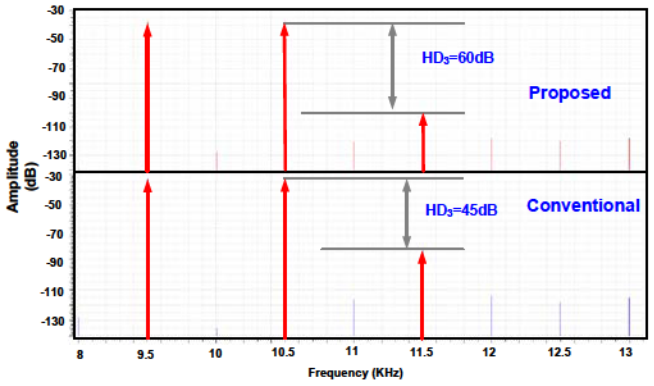

Fig. 8. Two-tone test spectrum for the proposed and conventional VGA.

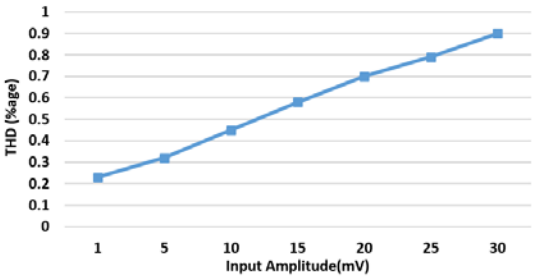

Fig. 9. THD vs input amplitude for the proposed solution.

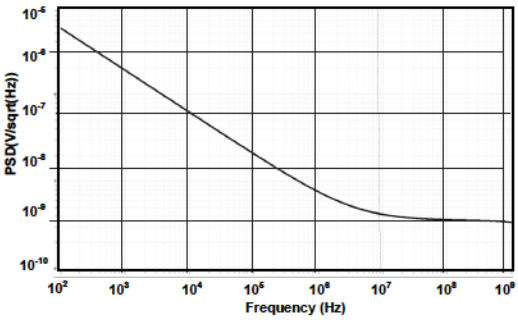

Fig. 10. Simulated Input referred PSD

Fig. 8 shows the frequency spectrum of the conventional architecture (Fig. 2(b), where the 3rd order component (11.5KHz) is -45dB below the main tone, whereas for the proposed VGA it is at -60dB. Hence, the proposed technique improves HD_3 by 15dB. Fig. 9 shows the THD of the AFE while sweeping the input signal. Due to the extra loop of the proposed architecture, the THD is less than 1% for the input range of 1-30mV pk-pk differential signal. Compared to the THD of existing VGA architectures [3][5] this is a significant improvement, and 5 times better across the input signal amplitude range. Fig. 10 shows the simulated power spectral density (PSD) of the noise, and shows the integrated rms noise is 6.7μV. Fig.11 shows the layout of the prototype which occupies 3108μm2.

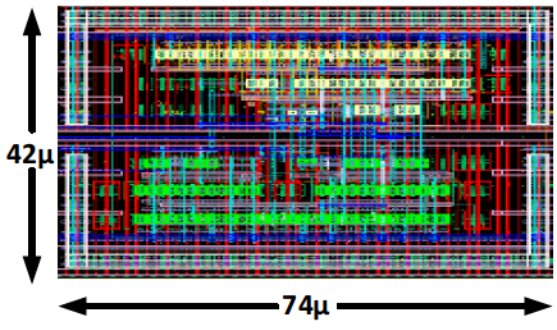

Fig. 11. The Layout of the proposed system

VI. Conclusion

In this paper, a linearization technique for the VGA has been proposed which relies on increasing loop-gain, and

hence the linearity. Compared to existing techniques, the proposed technique has ~5 times (15dB) improvement in the HD_3.

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