Design of a High Gain Silicon BJT and E-pHEMT Hybrid Matrix Amplifier with Optimum Filter Matching Technique

Pragash Sangaran [1,2*], Narendra Kumar[1], Claudio Paoloni[3]

[1] Department of Electrical Engineering, Faculty of Engineering, University of Malaya, Kuala Lumpur, Malaysia
[2] Innowave LLC, 5100 McDonell Ave, Oakland, CA 94619, USA
[3] Engineering Department, Lancaster University, Lancaster, LA1 4YW, UK
*pragash_g@hotmail.com

Abstract: Software Defined Radio (SDR) is an advanced wireless transmission paradigm that permits to support all the consumer wireless protocols such as 2G, 3G, LTE, Wi-Fi (2.4 GHz and 5GHz), Bluetooth and Zigbee, by software rather than hardware. A typical frequency band of operation is in the range 0.5 – 6 GHz. The challenge to bring a SDR system on portable devices is the availability of Ultra-wide band compact amplifiers with high gain over a wide frequency band. A novel hybrid Silicon BJT and E-pHEMT matrix amplifier with two rows and four columns (2 by 4) of transistors is designed realized and tested demonstrating 0.65–5.8 GHz frequency band to satisfy the SDR specifications. The novel optimum filter matching technique is applied to optimize the performance and overcome the limit of the hybrid approach. The proposed matrix amplifier exhibits an average gain of 37.5dB and average output power of 18dBm across 0.65GHz - 5.8GHz band with only 3V supply voltage. The gain is the highest in the state of the art for the frequency range. A bandwidth of 5.15 GHz, 20.3dBm one dB compression point at 1.35GHz, 10% to 16% power added efficiency and 1.2W DC power consumptions are obtained.

1. Introduction

The design of Power Amplifiers (PA) with simultaneously high gain and high bandwidth is a challenge due to device gain-bandwidth limitation. In the past, many amplifier topologies were proposed to overcome the gain-bandwidth limitation. In particular, one of the most promising topologies is the Matrix Amplifier (MA) [1, 2]. In the last decade no work has been reported in the field of MA even though the enormous benefit in comparison to many others power amplifier topologies. MA provides high gain and high bandwidth with smaller chip area than the other topologies. Probably, the lack of interest was due to the fact that wireless communication standards are usually narrow band. However, the evolution of networks and the need of high data rate are producing new wide band protocols for wireless communications. The software defined radio (SDR) [3] is evolving to receive and transmit new widely different radio protocols (2G, 3G, LTE, Wi-Fi (2.4 GHz and 5 GHz), Bluetooth and Zigbee). For the purpose, compact very wide band amplifiers, with high gain are needed to cover the different wireless bands and to be implemented in portable devices.

In the following, the state of the art of wideband power amplifications are described in the frequency band of interest for SDR.

The Distributed Amplifier (DA) is one of the most effective wide band amplifiers, built in many different configurations. Cascaded DAs in 0.13um CMOS technology exhibit 10dB gain across 2-16 GHz with 13 dBm output power at 1dB compression point (P1$_{dB}$) and 9% Power Added Efficiency (PAE) [4]. A pHEMT DA with feedback active load demonstrates 10.9dB gain across 1-5 GHz [5]. A 0.25um GaAs pHEMT Class J DA produces 10.5 dB gain, 30.7 dBm P$_{out}$ and 44 % PAE in the band of 1.5-10 GHz [6]. A 0.18um CMOS DA demonstrates 17.4 dB gain and 3.9 dBm P1$_{dB}$ and

0.5-3.3 % PAE in the 0.7-25.7 GHz band with P$_{dc}$ of 75.2 mW [7].

Significant work has been done in GaN technology in recent years. Non-term cascode DA using 0.15um GaN-SiC HEMT technology exhibits gain of 10 dB and P$_{out}$ of 1-2 W with P$_{dc}$ of 5.2 W across 0.1-45 GHz [8]. DA with novel integration technique is presented with pHEMT and GaN HEMT technology demonstrates 30 dB gain and 40 dBm P$_{out}$ across 0.1-2.4 GHz bandwidth and 30 % of PAE [9]. 0.25um GaN HEMT DA exhibits 12.8-13.7 dB gain, 12.3-14.1 dBm P$_{out}$ and 27-34 % PAE across 2-6 GHz bandwidth [10]. GaN-HEMT is a popular technology and used in four of the following work. 8-10.4 dB gain, 43-45 dBm P$_{out}$ and 56-70 % drain efficiency (DE) is achieved across 0.5-2.7 GHz band [11]. In [12], 9-14 dB gain, 10-15.5 dBm P$_{out}$ and 46-75 % PAE is achieved across 0.8-3.6 GHz band. 12 dB gain, 46.6-49.3 dBm P$_{out}$ and 45-85 % DE is achieved across 0.45-1.95 GHz with push pull amplifier [13]. GaN Doherty PA exhibits 43.1-44.4 dBm P$_{out}$ and 45.3-53.6 % of DE demonstrated across 1.5-2.4 GHz [14] whereas GaN Class-J PA exhibits 10.2-12.2 dB gain, 33.4 dBm P$_{out}$ and 27.5 % of PAE across 0.8-3.6 GHz [15].

Differential amplifiers offer wide bandwidth and high gain. Three configurations were proposed, with 10-11.5 dB, 10-19.5 dB and 10-18.7 dB gain across 2-39 GHz, 2-37 GHz and 2-36 GHz band respectively with 26 mW, 122mW and 70m W of P$_{dc}$ respectively [16].

All the amplifier topologies listed above provide good performance, however, more compact and powerful configuration are needed for modern, smaller size communication devices to include SDR, as smartphone or tablet.

The Matrix Amplifier is a compact wide band, and high gain topology with smaller size in comparison to distributed amplifiers and differential amplifiers, providing saving in chip cost.

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This paper proposes a novel high gain hybrid MA based on using simultaneously Silicon BJT and E-pHEMT technology in the same amplifier. The novel optimum filter matching technique is used to further improve the gain-bandwidth product in comparison to a conventional hybrid MA. The proposed MA exhibits an average gain of 37.5 dB and average P_{out} of 18 dBm in the band 0.65-5.8 GHz with 3V supply voltage. The gain is the highest among the state of the art devices in the same frequency range. The bandwidth is 5.15 GHz and $P1_{dB}$ is 20.3 dBm at 1.35 GHz. The PAE ranges from 10 % to 16 % and P_{dc} is 1.2 W. In Section 2, the principle of operation of a MA with conventional design method is presented. The design of hybrid MA with novel optimum filter matching is discussed in Section 3. Section 4 reports on the measurement results.

2. Principle of Operation of Matrix Amplifier

Fig. 1 shows the unilateral model of a FET. Fig. 2 shows the unilateral model of a BJT. A DA uses additive amplification to provide large bandwidth. A MA consists of two or more DA stacked together in a multiplicative manner. Both additive and multiplicative amplifications are obtained using a distribution of gain elements in a 2-D array [17].
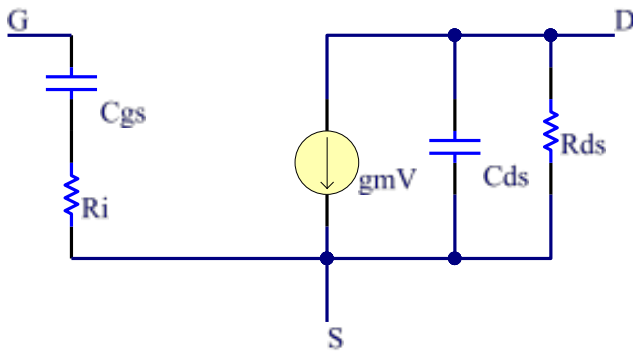

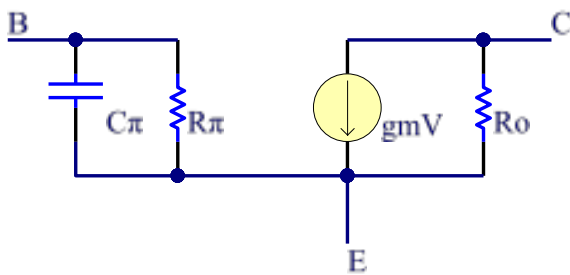**Fig. 1.** *FET unilateral high frequency model*

Fig. 2. *BJT unilateral, high frequency model*

The proposed MA has an input row of Silicon BJT and an output row of E-pHEMT. The second row is connected to the first row by output collector line of the BJT in first row connected to input gate line of the FET in the second row. Fig. 3 shows 2x4 Silicon BJT-pHEMPT MA in Stairing configuration. Stairing is a stair like shaped MA design technique which is accomplished by removing the first left section of the transistor at the center line as shown in Fig. 3.

Stairing improves the gain flatness without compromising gain or bandwidth [17]. Moreover, it reduces total cost and size of the layout.

The MA in Fig. 3 has three artificial transmission lines (TLs): input Transmission Line (input TL), center Transmission Line (center TL), and output Transmission Line (output TL). 3V drain supply voltage is used.

Based on the Matrix Amplifier theory [18], the three artificial transmission lines should have the same cutoff frequency for maximum gain-bandwidth product. The cutoff frequency is given by:

$$f_c = \frac{1}{\pi\sqrt{L_i C_i}} \tag{1}$$

C_i and L_i are the capacitance and inductance of each of the three artificial transmission lines. $C_i = C_\pi$ and $L_i = L_b$ for the input line, $C_i = C_{gs}$ and $L_i = L_c$ for the center line and, $C_i = C_{ds}$ and $L_i = L_d$ for the output line.

A series capacitance, C_{add} is connected to the input TL, to reduce the total capacitance value in the input TL and make it equal to the capacitance of output TLs. The inductor, L_i will remain the same for both input and output TLs.

$$L_i = L_b = L_d \tag{2}$$

The characteristic impedance of the input and output TLs are:

$$Z_o = \sqrt{\frac{L_b}{C_\pi + C_{add}}} = \sqrt{\frac{L_d}{C_{ds}}} = 50\Omega \tag{3}$$

The characteristic impedance of the center TL is not the same as characteristic impedance of the input and output TLs. The characteristic impedance of the center TL is expressed as:

$$Z_{oc} = \sqrt{\frac{L_c}{C_{gs}}} \neq Z_o \tag{4}$$

For the center TL, only the inductor value is optimized so that the centre TL cutoff frequency (f_c) equals to the f_c of the input and output TLs. Eq. 1 can be rearranged to obtain L_c;

$$L_c = \frac{1}{\pi^2 f_c^2 C_{gs}} \neq L_b \neq L_d \tag{5}$$

Neglecting transmission line losses and low frequencies, the gain of a MA with N transistor and k rows is approximately;

$$|A_V| = \left(\frac{N}{2}\right)^k \prod_k g_{mk} Z_{ok} \tag{6}$$

Where Z_{ok} is the impedance of the *k*-th line. The exponent *k* in (6) indicates the multiplicative property of the MA. The gain of an MA is approximately *k* times higher than that of a DA for identical line impedances [17].
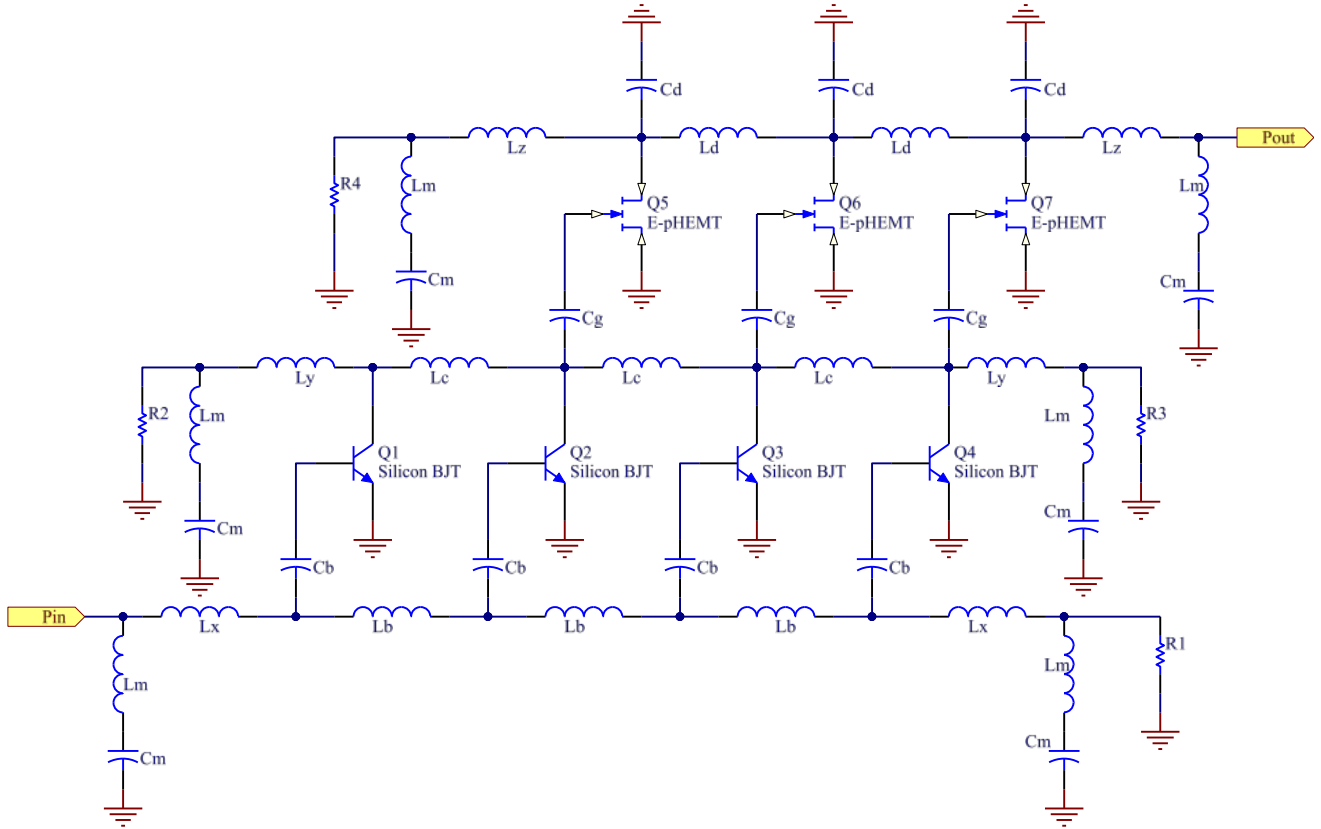
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Fig. 3. *2 x 4 Silicon BJT and E-pHEMT MA using stairing and optimum filter matching technique*

3. Design of MA with Optimum Filter Matching

The conventional MA design method is only suitable for MMIC implementation and not for hybrid MA circuit. This is because the availability of arbitrary values of L_c, L_d, L_b, and C_{add} is only possible in MMIC technology. In Hybrid integrated circuit implementation, only limited lumped discrete component values are available for inductors and capacitors. This prevents the PA designers to flexibly tune the cutoff frequency of the center TL to match the cutoff frequency of the input and output TLs. As a result, it is very hard to design a PA with optimum gain-bandwidth product. Due to the limitation of the lumped discrete components, an optimum filter matching technique is proposed in this work. The optimum filter matching is nothing but perfect match of fc of all three TLs. This technique helps to match the fc of the input TL to the fc of the center and output TL and therefore the phase shift per section on all three TLs are equalized. This permits the currents on the center TL and output TL to interfere constructively or add in phase and yields maximum possible gain-bandwidth product out of the MA.

This novel optimum filter matching technique is essential for success of hybrid MA design Optimum filter matching technique solves the PCB implementation problem for the MA.

The choice of the most suitable devices is a crucial design step for the success of the design. The device technology can be selected based on performance specifications including gain, output power, power-added efficiency, linearity, stability, noise figure and etc. E-pHEMT Avago ATF54143 and Silicon BJT Infineon BFP420 are

selected for the MA realization due to high gain, high linearity and high output power characteristics.

The Keysight ADS with Modelithics high precision component models [19] are used to design and simulate quiescent biasing point, stability, gain, output power, S-parameters and linearity of the MA. In particular, Murata 0402 GRM series Modelithics model and coilcraft 0402 inductor Modelithics model are used for the simulation of the design.

a. Optimum filter matching for MA

The intrinsic elements of the model for silicon BJT and E-pHEMT (Fig.2) are combined with lumped element inductors and capacitors to form three artificial TLs. These three TLs can be broken down into multiple individual lowpass filter sections. The Optimum filter matching technique is based on implementing matching elements at each stage of these individual filter sections. This implementation will enable designers to optimize and tune the three TLs to have a perfect cut-off frequency of f_c. This will result in the same phase velocity between the three TLs and therefore maximum gain-bandwidth product and output power.

In Fig. 3, the proposed MA with optimum filter matching technique has additional C_b, C_g and C_d as compared to conventional MA. These additional components help to equalize the f_c of center TL to f_c of the input and output TLs.

For the proposed theoretical analysis, the actual four column artificial TLs in Fig. 3 is simplified into two column artificial TLs as given in Fig. 4, Fig 5 and Fig 6 [20]. The current source of BJT and FET high frequency model has

been removed from Fig. 4, Fig. 5 and Fig. 6 for simplicity [21].

Fig. 4 shows the input TL high frequency equivalent circuit of the MA. The value of the C_π is the highest among all other intrinsic capacitors. The value of C_π is in the range of few picofarads to few tens of picofarads. Due to this, it is necessary to add C_b to the input TL or connect in series to the base of the BFP420 Silicon BJT. This makes the total capacitance at individual filter section equals to $C_b // C_\pi$. This significantly reduces the value of capacitance at the input TL and therefore the input TL f_c equals the f_c of the center and output TLs. Adding the additional matching capacitor C_b, helps to obtain optimum filter matching to the filter sections of the center and output TLs.

Fig. 5 shows the high frequency equivalent circuit of center TL of the MA. In the center TL, the additional matching capacitor of C_g is added. To note that C_{gs} is the biggest intrinsic capacitor next to C_π. By adding C_g, the total capacitance at individual filter section equals to $C_g // C_{gs}$. This significantly reduces the value of the capacitance at the center TL and therefore the center TL f_c equals the f_c of the input and output TLs. In the conventional method, the center TL is tuned by only tuning the L_c as explained earlier. This is practically not possible for hybrid MA due to the unavailability of arbitrary inductors values. Adding C_g to the center TL will make optimization of the filter section to match the f_c possible. L_c and C_g of the center TL will be tuned to achieve the cutoff frequency of f_c.
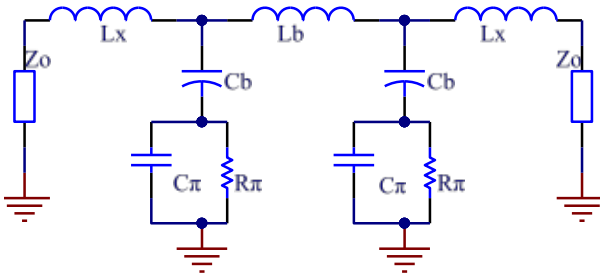

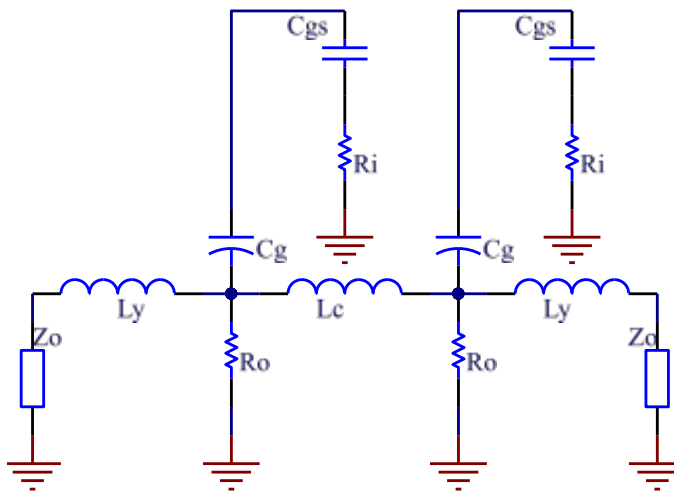**Fig. 4.** *MA input TL high frequency equivalent circuit*

Fig. 5. *MA center TL high frequency equivalent circuit*

Fig. 6 shows the output TL high frequency equivalent circuit of the MA. C_{ds} is the smallest intrinsic capacitor of the device as compared to C_{gs} and C_π. Due to this, a parallel matching capacitor C_d is necessary to increase the total capacitance in the output TL and therefore the f_c of the output TL equals the f_c of the center and input TL. By adding C_d, the total capacitance of the output TL at the individual filter section is equals to $C_d + C_{ds}$.

Apart from addition and optimization of matching capacitors in all the three artificial TLs, the inductors of the artificial transmission line are also optimized to achieve the cutoff frequency of f_c.
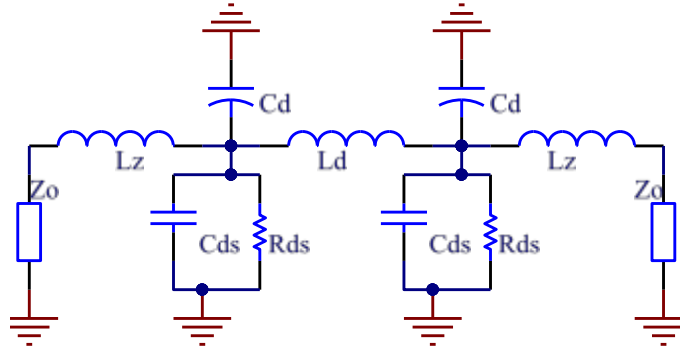

Fig. 6. *MA output TL high frequency equivalent circuit*

Overall cutoff frequency of Silicon BJT- E-pHEMT MA with novel optimum filter matching technique is given by;

$$f_c = \frac{1}{\pi\sqrt{L_b(C_b//C_\pi)}} = \frac{1}{\pi\sqrt{L_c(C_g//C_{gs})}}$$
$$= \frac{1}{\pi\sqrt{L_d(C_{ds}+C_d)}} \tag{7}$$

Unlike conventional method, the inductors of all three TLs are not equal;

$$L_b \neq L_c \neq L_d \tag{8}$$

C_π, C_{gs}, and C_{ds} are the intrinsic element of silicon BJT and E-pHEMT respectively. The characteristics impedance of the input and output TL is given by;

$$Z_o = \sqrt{\frac{L_b}{(C_b//C_\pi)}} = \sqrt{\frac{L_d}{(C_{ds}+C_d)}} = 50\Omega \tag{9}$$

The total capacitance in the center TL is $C_g // C_{gs}$. The inductance required to make phase velocity equal for input and output lines are;

$$L_c = \frac{1}{\pi^2 f_c^2 (C_g//C_{gs})} \tag{10}$$

The C_g can be optimized or tuned together with the L_c to achieve f_c and equal phase velocity between input and output TLs. The characteristics impedance of the center TL is;

$$\boldsymbol{Z_{oc}} = \sqrt{\frac{L_c}{(C_g//C_{gs})}} \tag{11}$$

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4. Experimental validation

The simulations of the MA were performed by ADS with Modelithics high precision component models. The initial design of the MA based on theoretical equation is verified using ADS circuit simulation. The layout was also simulated by ADS to validate the performance of the design including the parasitics of the Printed Circuit Board (PCB).

Finally, a PCB board is fabricated to validate the MA novel design is presented together with the layout simulation. Fig. 7 and Fig. 8 shows the MA design on a PCB board. The MA is implemented on two-layer Rogers 4350 PCB with RF on the top layer and DC on the Bottom layer. This is to minimize the EMI (electromagnetic interference) between RF and DC. Coplanar waveguide transmission lines are used as RF components interconnect. These implementation techniques are used to reduce the cost of the PCB.
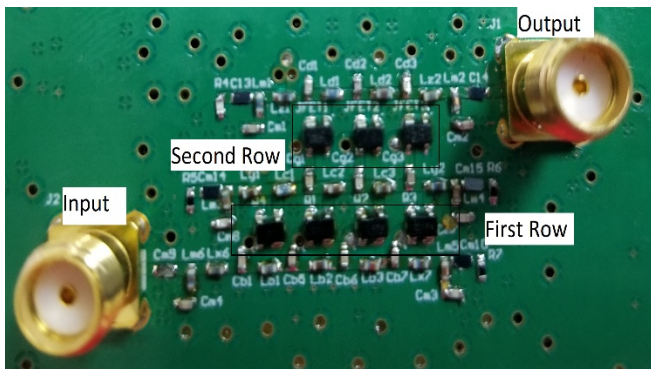

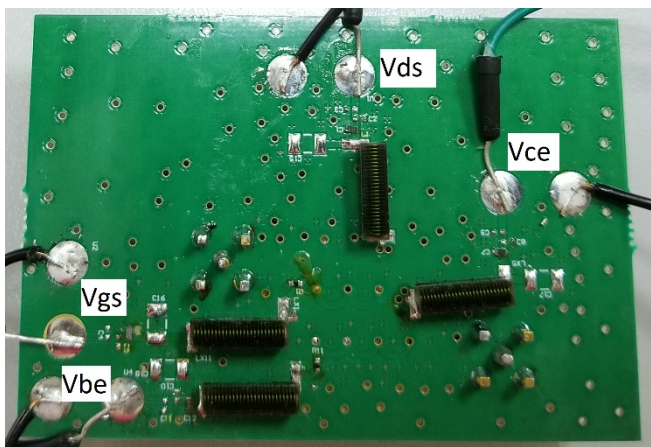**Fig. 7.** *Top layer of the MA PCB*

Fig. 8. *Bottom layer of the MA PCB board*

Fig. 9 shows the S-parameter of the MA in the band 0.65–5.8 GHz. Average input and output return loss, S11 and S22 of -10 dB were obtained across the band. Good agreement is obtained between simulation and the measurement.
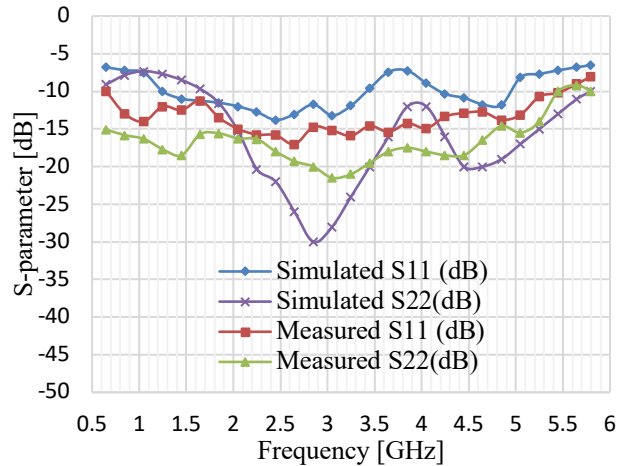

Fig. 9. *S-parameters of MA over the bandwidth operation*

Fig 10 shows the large signal gain of the MA. The measured large signal gain, 37.5dB +/- 1.5dB in the 0.65-5.8GHz band, is highest in the state of the art. The measurement and simulation exhibit very good agreement. Fig. 10 also shows the Power-added Efficiency (PAE) versus frequency of the MA. Measured PAE from 10 % to 15.9 % is obtained across the frequency range 0.65-5.8 GHz. Good correlation is obtained between simulation and the measured data across the operating bandwidth from 0.5-5.8 GHz. The relatively low efficiency of the amplifier could be due to the usage of broadband choke at the gate and base biasing. A different solution will be tested in the future to increase the efficiency. To note that the matrix amplifier operates in class AB.
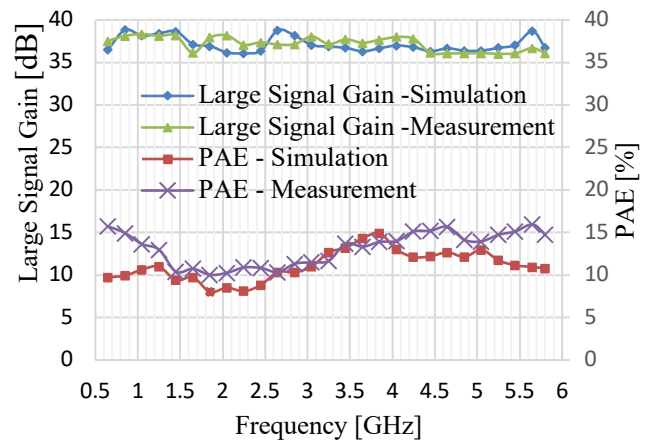

Fig. 10. *MA large signal gain and PAE across bandwidth operation*

Fig. 11 shows the output power of MA. An average output power of 18 dBm in the bandwidth for -20 dBm input power (Pin) is obtained. Good correlation is obtained between simulated and the measured output power (Pout).
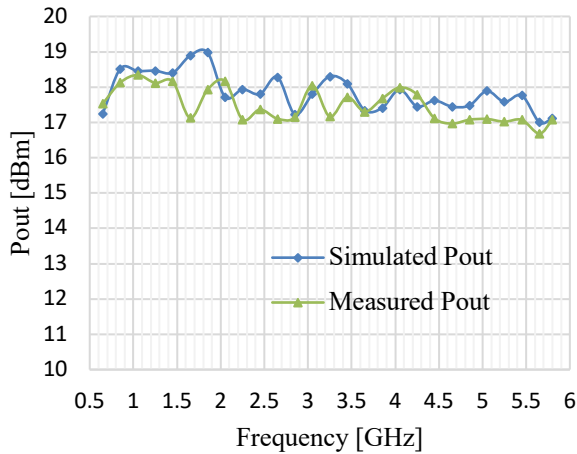
Fig. 11. *MA Output power across operating bandwidth*

As reference, Table 1 summaries the performance of the recently reported high gain and wide bandwidth amplifiers as compared to the presented MA. It is notable that the described hybrid MA exhibits the highest of gain in comparison to all the other recent works. It has one of the widest bandwidth. The gain of 37.5dB is highest in the state of the art. Moreover, the 3V supply voltage is the lowest among the other amplifiers. It permits a good output power (18dBm) across a wide bandwidth of operation. The achieved performance demonstrates that the presented MA is very promising for low voltage consumer SDR applications.

5. Conclusions

The design, simulation and fabrication of a hybrid Silicon BJT and E-pHEMT MA for the SDR applications are presented. The proposed MA exhibit an average gain of 37.5 dB +/- 1.5 dB in the 0.65- 5.8 GHz band which is highest in the state of the art. An average output power of 18 dBm with 3 V supply voltage, a 5.15 GHz bandwidth and 20.3 dBm one dB compression point at 1.35 GHz are obtained. The power added efficiency and DC power consumptions are 10% to 16% and 1.2 W respectively. The proposed optimum filter matching technique has been demonstrated and proven effective to improved gain-bandwidth product of the MA. This described MA has been demonstrated suitable for wideband applications, in particular for SDR radio solutions which covers consumer wireless protocols such as 2G, 3G, LTE, Wi-Fi (2.4 GHz and 5GHz), Bluetooth and Zigbee. Its high gain and efficiency make the presented MA a very promising candidate for enabling new generation of smartphones and tablets based on SDR. The discussed optimum filter matching technique is very effective in realization of high-performance MA in the PCB technology.

6. Acknowledgment

Table 1 Comparison of the hybrid MA with optimum matching technique to recent high gain and wide bandwidth amplifiers.

	[7]	[20]	[21]	[9]	[11]	[15]	[12]	[13]	**This Work**
Tech. [nm]	0.18 CMOS	0.18 CMOS	0.15 µm GaN-SiC HEMT	pHEMT + GaN HEMT	GaN-HEMT	GaN	GaN-HEMT	GaN HEMT	Silicon BJT + E-pHEMT
V_d[V]	-	-	28	28	28	28	28	28	3
Freq. [GHz]	0.7-25.7	0.7-43.9	0.1-45	0.1 - 2.4	0.5-2.7	0.8-3.6	0.8-3.6	0.45-1.95	0.65-5.8
BW [GHz]	25	43.2	44.9	2.3	2.2	2.8	2.8	1.5	5.15
P_{dc} [mW]	75	183	5200	-	-	-	-	-	1.2W
S21 [dB]	17	21	>10	30	8-10.4	10-12	9-14	12	37.5
$P1_{dB}$ [dBm]	>3.9	8.1	-	-	-	-	-	-	20
P_{out} [dBm]	-	-	30-33	40	43-45	33.4	10-15	46–49	18
Type	DA	DA	Non-Term Cascode DA	DA	PA	Class-J PA	PA	Push pull PA	MA with optimum filter matching
PAE [%]	0.5-3.3	-	-	-	56-70	25	46-75	40–70	10-16

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