52. IWK

Internationales Wissenschaftliches Kolloquium
International Scientific Colloquium

PROCCEDINGS | **10 - 13 September 2007**

FACULTY OF COMPUTER SCIENCE AND AUTOMATION

COMPUTER SCIENCE MEETS AUTOMATION

VOLUME II

TECHNISCHE UNIVERSITÄT
ILMENAU

Bibliografische Information der Deutschen Bibliothek
Die Deutsche Bibliothek verzeichnet diese Publikation in der deutschen Nationalbiografie; detaillierte bibliografische Daten sind im Internet über **http://dnb.ddb.de** abrufbar.

ISBN 978-3-939473-17-6

Impressum

Herausgeber:	Der Rektor der Technischen Universität Ilmenau Univ.-Prof. Dr. rer. nat. habil. Peter Scharff
Redaktion:	Referat Marketing und Studentische Angelegenheiten Kongressorganisation Andrea Schneider Tel.: +49 3677 69-2520 Fax: +49 3677 69-1743 e-mail: kongressorganisation@tu-ilmenau.de
Redaktionsschluss:	Juli 2007
Verlag:	 Technische Universität Ilmenau/Universitätsbibliothek Universitätsverlag Ilmenau Postfach 10 05 65 98684 Ilmenau www.tu-ilmenau.de/universitaetsverlag
Herstellung und Auslieferung:	Verlagshaus Monsenstein und Vannerdat OHG Am Hawerkamp 31 48155 Münster www.mv-verlag.de
Layout Cover:	www.cey-x.de
Bezugsmöglichkeiten:	Universitätsbibliothek der TU Ilmenau Tel.: +49 3677 69-4615 Fax: +49 3677 69-4602

Preface

Dear Participants,

Confronted with the ever-increasing complexity of technical processes and the growing demands on their efficiency, security and flexibility, the scientific world needs to establish new methods of engineering design and new methods of systems operation. The factors likely to affect the design of the smart systems of the future will doubtless include the following:

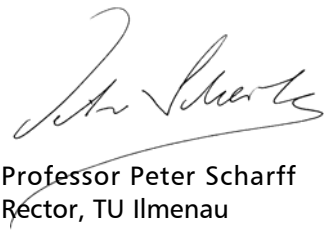
- As computational costs decrease, it will be possible to apply more complex algorithms, even in real time. These algorithms will take into account system nonlinearities or provide online optimisation of the system's performance.
- New fields of application will be addressed. Interest is now being expressed, beyond that in "classical" technical systems and processes, in environmental systems or medical and bioengineering applications.
- The boundaries between software and hardware design are being eroded. New design methods will include co-design of software and hardware and even of sensor and actuator components.
- Automation will not only replace human operators but will assist, support and supervise humans so that their work is safe and even more effective.
- Networked systems or swarms will be crucial, requiring improvement of the communication within them and study of how their behaviour can be made globally consistent.
- The issues of security and safety, not only during the operation of systems but also in the course of their design, will continue to increase in importance.

The title "Computer Science meets Automation", borne by the 52nd International Scientific Colloquium (IWK) at the Technische Universität Ilmenau, Germany, expresses the desire of scientists and engineers to rise to these challenges, cooperating closely on innovative methods in the two disciplines of computer science and automation.

The IWK has a long tradition going back as far as 1953. In the years before 1989, a major function of the colloquium was to bring together scientists from both sides of the Iron Curtain. Naturally, bonds were also deepened between the countries from the East. Today, the objective of the colloquium is still to bring researchers together. They come from the eastern and western member states of the European Union, and, indeed, from all over the world. All who wish to share their ideas on the points where "Computer Science meets Automation" are addressed by this colloquium at the Technische Universität Ilmenau.

All the University's Faculties have joined forces to ensure that nothing is left out. Control engineering, information science, cybernetics, communication technology and systems engineering – for all of these and their applications (ranging from biological systems to heavy engineering), the issues are being covered.

Together with all the organizers I should like to thank you for your contributions to the conference, ensuring, as they do, a most interesting colloquium programme of an interdisciplinary nature.
I am looking forward to an inspiring colloquium. It promises to be a fine platform for you to present your research, to address new concepts and to meet colleagues in Ilmenau.



Professor Peter Scharff
Rector, TU Ilmenau

Professor Christoph Ament
Head of Organisation

Table of Contents

C O N T E N T S

10 Mobile Communications

11 Education in Computer Science and Automation

52nd Internationales Wissenschaftliches Kolloquium
Technische Universität Ilmenau
10 – 13 September 2007

B. Däne

Modeling and Realization of DMA Based Serial Communication for a Multi Processor System

1. INTRODUCTION

Performance of communication is very important for multi processor systems. This paper will present a communication solution for a multi DSP (Digital Signal Processor) system using DSPs from *TMS320C67x* family [1] of *Texas Instruments*. On-chip serial high-speed ports and DMA (Direct Memory Access) units are used. Primary goals are small latency, small protocol overhead even for short messages and minimized influence on filter calculations and block transfers that isochronously run on the system. The on-chip serial ports, designed for point-to-point communication only, should be enabled for multi-point shared-medium communication using small hardware extensions only.

The design process has been carried out in model based manner. Hierarchical models represented hardware and software functions of communication process. Behavior of on-chip hardware has been determined, modeled and validated using existing documentation [2] and experimental results. In order to get quantitative performance results from simulation several communication scenarios have been modeled. These results have later been compared to practical results from the system realized.

So the project is a case study in model based design. It investigates the use of design and evaluation methods with a nontrivial practical example [3]. Extending another paper [4] this paper additionally discusses modeling of the DMA units. Modeling tool has been MLDesigner [5,6] of MLDesign Technologies Inc.

2. HARDWARE SETUP

Hardware is based on the multi DSP system described in [7], using five DSPs from *TMS320C67x* family. It already used a communication interface based on parallel memory busses. The goal was to implement additional serial communication based on on-chip duplex synchronous serial interfaces. These interfaces, named McBSP (Multi Channel Buffered Serial Ports), perform at a gross data rate of approximately 83 Mbit/s [2,8]. Multi channel feature is available by time multiplex of up to 128 logical channels.

External hardware structure was designed as a simple serial bus that shares one impedance-controlled line for each node's data, clock and frame impulse signals, respectively. This non-documented regime is enabled by software controllable tri-state properties of on-chip signal sources involved here. Protocol support or middleware supporting this regime was not available.

Access to control and data registers of McBSP units has to be done by DMA rather than CPU cycles due to CPU core performance loss when interrupting loops and accessing slow memory or peripherals [1]. Coordination between CPU core and DMA includes usage of interrupts in order to organize concurrent timing behavior.

Motivation for the additional serial communication feature with respect to the parallel bus already available is an independent channel for short but urgent messages and alarms rather than additional bandwidth. Parallel bus is used for isochronous block transfers that should not be affected by such messages and in turn should not introduce additional latency into them.

3. MODELING CONCEPT AND GOALS

As mentioned above the goal of the case study is studying and evaluating model based design methods with an real example rather than the technical solution itself. Especially timing analysis and quantitative performance measurement should be performed with the model for later comparison to practical results. One typical challenge for such projects is including not only components under design (here external hardware structure and a number of software modules) but also relevant parts of the embedding system (here on-chip compo-

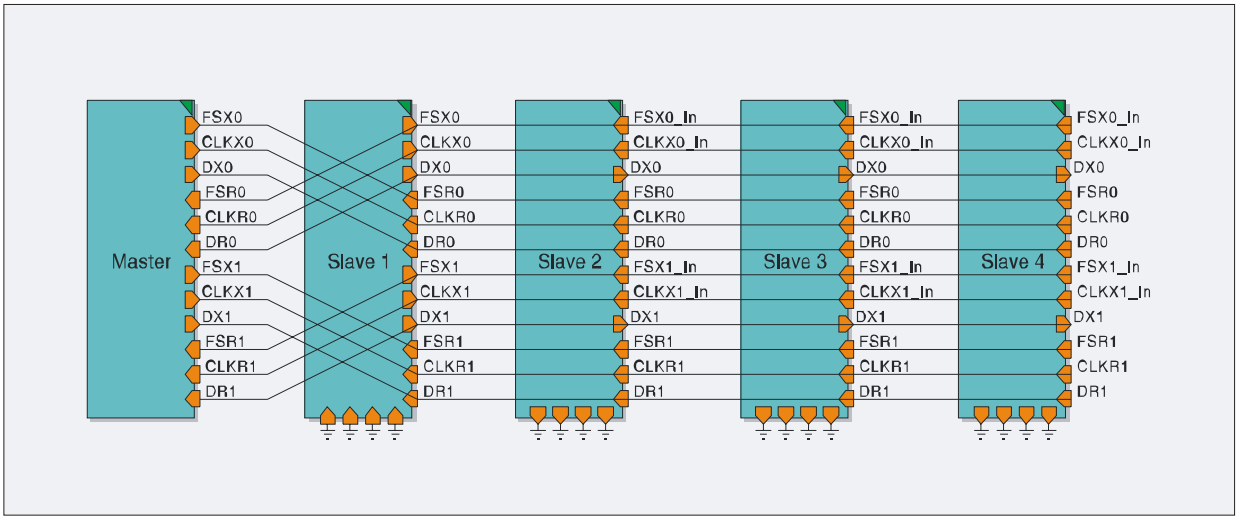


Fig. 1: Top level of model

nents and timing behavior of CPU core) into the model. Latter parts of the model are available from different sources using different representations and have to be integrated into one consistent model.

The model uses the DE (discrete event) domain [10] of the MLDesigner modeling tool mentioned above. The main paradigm of this domain is based on atomic messages between ports of blocks that may be structured hierarchically. This kind of domain also can be found in the open-source modeling tool Ptolemy Classic [11] from University of Berkeley that precedes the MLDesigner tool. Also included are blocks from the FSM (finite state machine) domain that has been substantially extended during development of MLDesigner [12].

Investigation of timing behavior and performance values in this case study mainly is based on simulation techniques. This requires equipping the model with communication scenarios and observation elements. Generating implementation components (especially software modules) directly from the model is not subject of this case study but will be considered in future work.

4. MODEL STRUCTURE

The structure of the realized model will be shown partly using some example modules. At top level the model structure resembles the overall hardware structure of the target system with five DSP nodes (see fig. 1). One node acts as master, the other four as slaves. Events of DE domain at this level mainly represent edges of binary electrical signals that are included in the bus structures. The inside models of the DSP nodes also derive from their block structure, including two duplex McBSP units and two DMA channels each. Another block per DSP node encapsulates software functions of this node. Events at this level represent signal edges, port accesses, abstract trigger events and others.

The software functions are modeled using elements of the FSM domain. Included are sequences for port access and interrupt management, simple protocol implementations and communication scenarios. Cycle accurate modeling at instruction level has not been used. Software functions instead have been modeled at the level of abstract operations with constant time consumption including several processor instructions each.

A large part of modeling effort lies in the blocks that refine DMA and McBSP units. Due to lack of some kind of model or design documents from the manufacturer this information had to be extracted from manuals and application notes [2,9,13,14]. Some open questions have been solved by isolated experiments with evaluation hardware. Contributing to the goals of this case study it has been shown that such an approach can lead to behavioral models of sufficient accuracy.

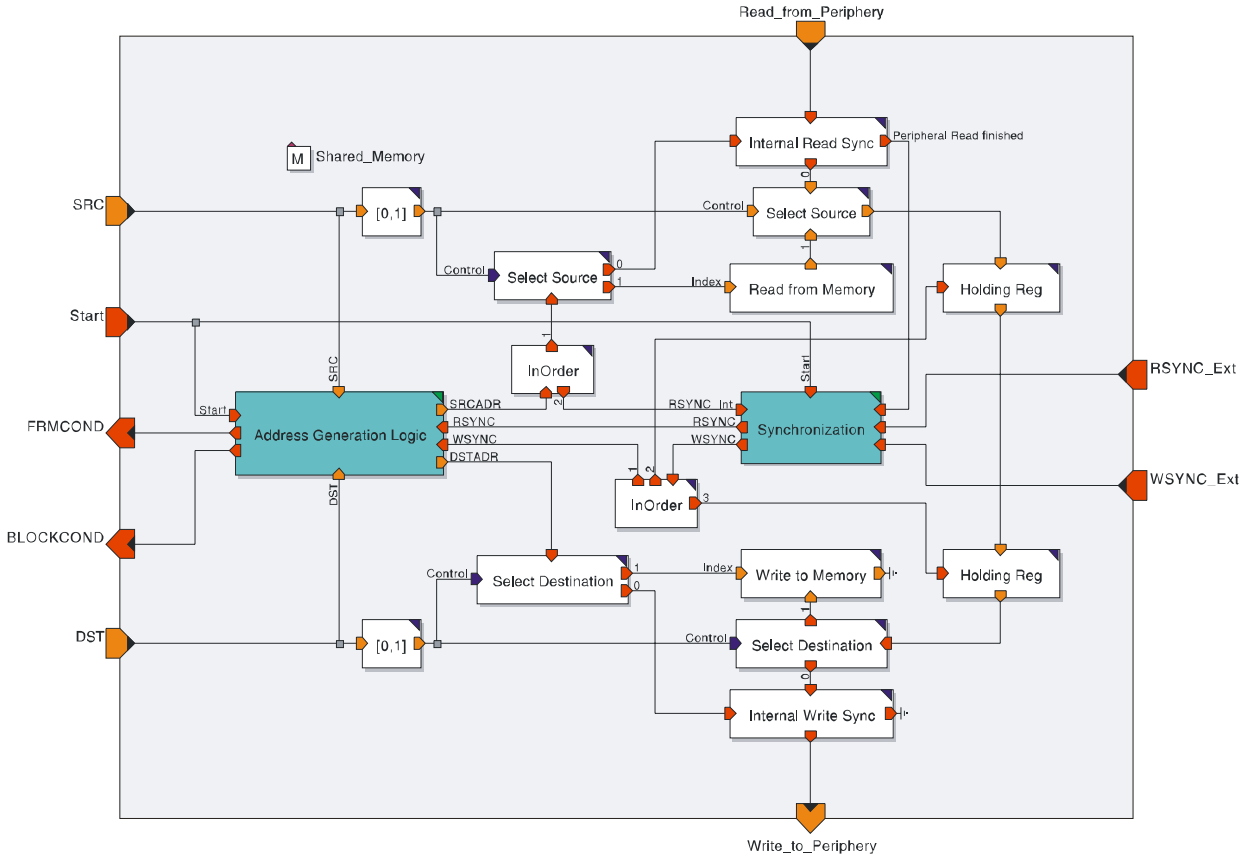


Fig. 2: Module for one DMA channel

For both DMA and McBSP units models with several hierarchical levels have been realized and tested. At bottom level all functions are built from basic elements (primitives) of DE domain. For example fig. 2 shows the inside of one DMA channel model. The signals at the border of the block correspond to logical conditions that start, synchronize and acknowledge transfers of the DMA channel. They have been derived from documentation and belong to interrupt conditions, control bits and others. Inside are blocks for organizing the operation, obtaining parameters such as addresses and block lengths and routing synchronization signals. The block “Address Generation Logic” (not shown) contains other modules for counting elements and address values with respect to element size and address counting mode.

As an example for a bottom level module fig. 3 shows the inside of the block “Synchronization”. Visible are logical functions for handling read and write cycles. The upper part generates trigger events (output port at right) that initiate read cycles, the lower part does so for write cycles. At left there are control inputs that may be assigned to several trigger sources. The block among other functions handles the start of the block transmission and the alternating of read and write cycles. The shaded elements represent options controllable by software that in real hardware appear as control registers. In the model the modeling tool’s parameter concept is used for this task.

5. RESULTS AND COMPARISON

The model and its functions with respect to expected behavior have been verified by simulation using prepared communication scenarios. Behavior has been observed by interactive model elements. Furthermore signal sequences of several external signals have been recorded for comparison. Later comparable communication scenarios have been investigated using the real target system. Sequences of same signals have

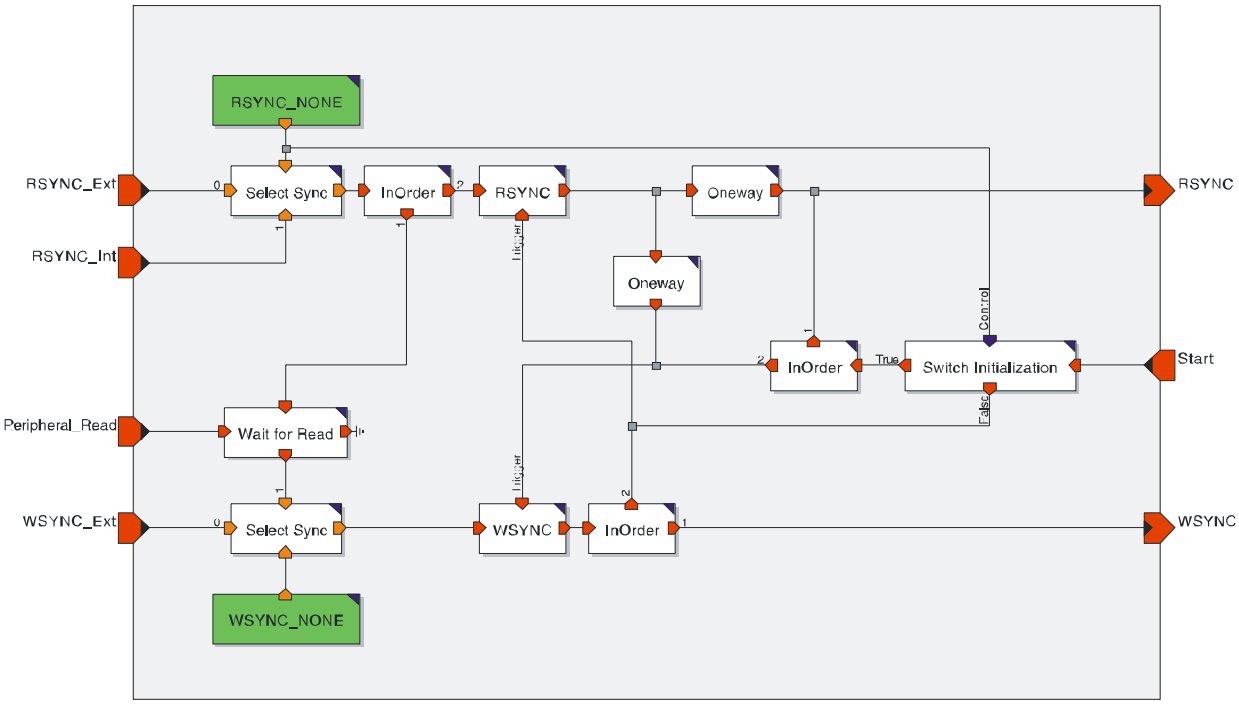


Fig. 3: Module “Synchronization” of one DMA channel

been recorded by logic analyzer. Comparison of both recordings showed good match. This fact serves as indication for the validity of the modeling approach.

Another significant part of the task was determining and comparing quantitative performance parameters. During simulation using the communication scenarios mentioned above net data rates and message latencies have been measured. While doing so several parameters such as block lengths and channel counts have been varied. Furthermore the tests have been carried out for two different members of the *TMS320C67x* DSP family, modifying the model according to their individual properties.

Measuring the same values with the real target system leads to good match with maximum divergence inside a five percent margin. Table 1 shows some values for both the C6701 device and the C6713 device. Note that different frequency division is used by these devices. Tests have been carried out for small and large block sizes and for single and multi channel modes. Data rates for multi channel modes are sum values for all channels. As expected small block sizes introduce a small overhead over large block sizes. Furthermore multi channel mode leads to some overhead over single channel mode.

However a systematical divergence towards too optimistic values is visible. This is caused by relatively course grain models of some software components that do not include time losses such as wait states or memory conflicts in internal data memory.

6. CONCLUSION

This case study demonstrates potentials and limits of this model based approach for planning and realizing a communication solution for an embedded multi processor system. The building of one consistent model using information that derived from different sources and that was available in different representation successfully has been carried out. Of-the-shelf-components for which no detailed design documents are available have been included in the model structure. Results from evaluating the model have been compared to experimental results from the real target system.

Further work will include refinement of the modeling process, leading to more precise prediction of quantitative values. Furthermore methods for generating actual hard- and software from parts of the model will be investigated and evaluated.

Configuration				Results		
Device	**Clock frequency** [MHz]	**Number of channels**	**Block size** [Bytes]	**Data rate from simulation** [Mbit/s]	**Data rate from measurement** [Mbit/s]	**Relative difference**
TMS320 **C6701**	167	1	32	51.6	50.7	+ 1.8%
			65536	52.9	52.8	+ 0.2%
		4	32	50.8	49.6	+ 2.4%
			65536	52.4	51.6	+ 1.5%
TMS320 **C6713**	300	1	32	68.7	67.2	+ 2.2%
			65536	71.1	71.2	− 0.1%
		4	32	68.0	65.2	+ 4.3%
			65536	71.2	70.4	+ 1.1%

Table 1: Data rates from simulation and from measurement

7. ACKNOWLEDGEMENTS

This work has been supported by Deutsche Forschungsgemeinschaft (DFG) under grant SFB 622.

Fig. 1, 2 and 3 are taken from this tool.

References:

[1] N. Dahnoun: Digital Signal Processing Implementation Using the TMS320C6000 DSP Platform. Prentice Hall 2000.

[2] C. Turner, R. Ma, B. Cobb: TMS320 C6000 and TMS320C5000 McBSP Features Summary. Application report SPRA638A. Texas Instruments Inc., Dallas, 2005.

[3] S. Herrig: Konzeption, Modellierung und Realisierung eines Kommunikationssystems für eine Multi-DSP-Architektur (Concept, Modeling and Realization of a Communication System for a Multi-DSP-Architecture). In German. Diploma thesis, TU Ilmenau/IA, Ilmenau 2005.

[4] B. Däne, W. Fengler: Modelling Hardware and Software for Fast Serial Interprocessor Communication. In: M. Adamski, L. Gomes, M. Węgrzyn, G. Łabiak (Eds.): DESDes'06 - Discrete Event System Design 2006. A Proceedings volume from the 3rd IFAC Workshop. Rydzyna, Poland, 26-28 September 2006. University of Zielona Góra Press, 2006, S. 155-160.

[5] V. Zerbe, U. Freund, H. Salzwedel: Mission Level Design of Control Systems. In: SCI/ISAS'99 Multiconference on Systemics, Cybernetics, Informatics, vol. 7, pp. 237-243. Orlando 1999.

[6] N. N.: MLDesigner Documentation (Draft), Version 2.5. MLDesign Technologies, Inc., Palo Alto, 2004.

[7] B. Däne, F. Berger: A Multiprocessor DSP System for a High Throughput Control Application. In: EDERS-2004: The European DSP Education and Research Symposium, 16th November 2004, Birmingham, UK.

[8] S. Anjanaiah, V. Soteriou: Using the TMS320C6000 McBSP as a High Speed Communication Port. Application report SPRA455A. Texas Instruments Inc., Dallas, 2001.

[9] D. Bell, E. Biscondi: TMS320C620x/TMS3206701 DMA and CPU. Data Access Performance. Application report SPRA614A. Texas Instruments Inc., Dallas, 2000.

[10] N. N.: Introduction to Discrete Event Modeling. MLDesign Technologies, Inc., Palo Alto, 2004.

[11] J. Buck, S. Ha, E. A. Lee, D. G. Messerschmitt: Ptolemy. A Framework for Simulating and Prototyping Heterogeneous Systems. Int. Journal of Computer Simulation, 22(4)1994, S. 155-182.

[12] H. Rath, H. Salzwedel: ANSI C Code Synthesis for MLDesigner Finite State Machines. In: H. Kern (Ed.): Synergies between information processing and automation: 49th International Scientific Colloquium at Ilmenau TU, 27.-30.9.2004. Shaker Verlag Aachen, 2004.

[13] N. N.: TMS320C6000 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide. User manual SPRU580D. Texas Instruments Inc., Dallas, 2004.

[14] N. N.: TMS320C620x/C670x DSP Program and Data Memory Controller/Direct Memory Access (DMA) Controller Reference Guide. User manual SPRU577A. Texas Instruments Inc., Dallas, 2004.

Author:

Dr.-Ing. Bernd Däne
TU Ilmenau
P. O. Box 100565
D-98693 Ilmenau
Phone: +49-3677-69-1433
Fax: +49-3677-69-1614
E-mail: bernd.daene@tu-ilmenau.de
Web: http://www.tu-ilmenau.de/ra