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High-Level Design of Asynchronous RSFQ Digital Circuits

INTRODUCTION

According to the authoritative forecast [1], the previously exponential growth of the clock frequency of the silicon chips will slow in the future. One of the most critical reasons for this is that the dominant part of the clock interval is taken by the recharging of the interconnects' capacitances by the output currents of the gates, and only a small part - by the intrinsic switching speed of the transistors. The speeding up of this recharging process rapidly increases the total dissipated power density, and this effect becomes much worse with the further miniaturization of the interconnects [2]. The latter has motivated the search for alternative techniques allowing more efficient digital information processing.

One of the prospective candidates for this is the **R**apid **S**ingle-**F**lux **Q**uantum (RSFQ) technique [3] based on **l**ow-**t**emperature **s**uperconductors (LTS). There, an entirely new approach for data coding is used - the binary information is carried by picosecond voltage pulses instead of by voltage levels. They are named ***S**ingle **F**lux **Q**uantum (SFQ)* pulses due to their quantized area:

$$\int_0^{\infty} U(t) \cdot dt = \Phi_0 , \qquad (1)$$

with Φ_0 = 2.07mV·ps – a fundamental physical constant named *the single flux quantum*. The switching element of this technique is the overdamped Josephson junction having nonlinear and nonhysteretic I-V curve. Currently, all superconductive digital circuits are based on the RSFQ technique. Within the modern roadmaps for electronics [1], this technique is considered as a promising alternative to the semiconductor logic due to the following unique features [3]:

- extreme low power consumption - the energy dissipated during one switching of a single Josephson junction is of order of 10^{-19} Joule, while the signals are communicated via superconductive (i.e. lossless) transmission lines. Thus, the problem with the extreme large power dissipation of the high-integrated semiconductor digital circuits [2] could be overcome;
- extreme high operation speed achieved with relatively large lateral dimensions - simple digital RSFQ circuits with micrometer features sizes operating over 100GHz have been demonstrated long ago [4-9];
- intrinsically digital data representation - due to the nature of the flux quantization (1), the different binary states are inherently defined.

Nevertheless, the maximum successfully reached complexity of an RSFQ digital circuit is less than 100 000 Josephson junctions. One of the main reasons for this are the relatively large feature sizes of the modern LTS RSFQ fabrication technologies, making the development of an ultra-fast large-scale synchronous RSFQ application unimaginable [10]. The only possibility to overcome this problem is the implementation of the asynchronous logic approach [11]. An asynchronous circuit [12] is a digital circuit, in which each component reacts to changes on its inputs as these changes arrive, and produces changes on its outputs when it concludes its computation. No clock signal is provided to synchronize the work of the circuit's components, and the coordination between them is performed by some kind of handshaking protocol. In this way, all problems originating from the global clocking of the large-scale synchronous digital circuits are solved.

As already demonstrated in [10], an efficient design of complex digital circuits is possible only at logic level. However, the supporting CAD tools for asynchronous digital design are quite deficient, while a logic-level simulator for asynchronous RSFQ digital circuits is not available at all. Therefore, the aim of this paper is to present our concept for development of a software tool for high-level design and simulation of asynchronous RSFQ digital circuits.

DATA CODING AND HANDSHAKING WITHIN THE ASYNCHRONOUS RSFQ DIGITAL CIRCUTS

About pulse-based data exchange (such is the SFQ data exchange, see (1)), the most reliable communication is provided by the **d**ual-**r**ail (DR) data coding [11-12]. It is schematically shown in Fig. 1.

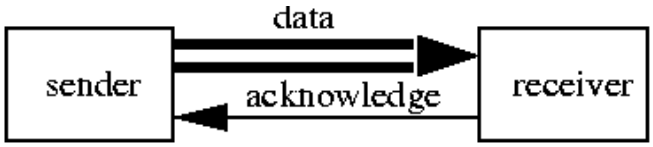


Fig. 1 Asynchronous dual-rail data exchange between two communicating units.

It uses two lines per bit of information that has to be communicated. The “true” line is used for transmitting logic “1”, whereas the “false” line is used for transmitting logic “0”. A separate line is providing only for the acknowledge signal. A pulse only in the “true” line is used for coding logical “1”; a pulse only in the “false” line is used for coding the logical “0”, while a simultaneous propagation of pulses in both “true” and “false” lines is forbidden. Note, that this communication is **d**elay-**i**nsensitive (DI), i.e. works correctly for any delays of the sender, the receiver, and the connecting lines. Another important advantage is that synchronous blocks can be included into the asynchronous architecture (the so-called globally asynchronous locally synchronous circuits). The latter is shown in Fig. 2. Due to its advantages, the DR information coding is the most popular for semiconductor asynchronous logic. Its popularity is even more pronounced within the RSFQ technique. Therefore, we have based our asynchronous RSFQ cell library [13] also on the DR data coding.

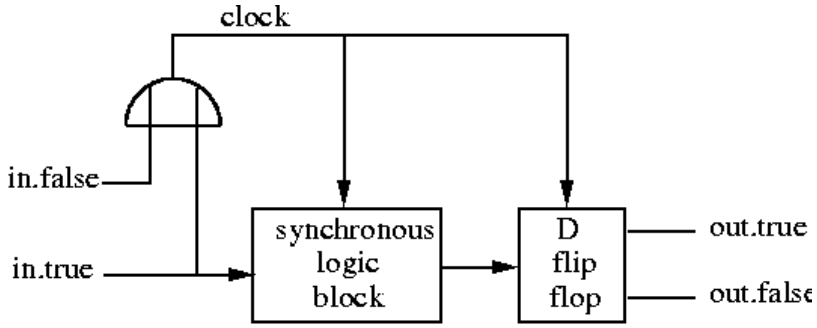


Fig. 2 Inclusion of a synchronous logic block within an asynchronous architecture based on the DR data coding.

If a complex asynchronous digital circuit should be designed to be DI, a handshaking feedback should connect each pair of communicating blocks. This is usually done by a Muller-C-element, whose electrical scheme and elements' values can be found in [13]. This, however, results into complicated circuit's topology and reduced operation speed, thus making the full-DI design impractical about large-scale circuits. Much simpler and faster circuits result, if the handshaking feedbacks are omitted always when possible. The latter is illustrated by the simple asynchronous circuit in Fig. 3. It contains two branches in parallel – NOR and NOT branch, and AND and NAND branch. To make it DI, one should use two additional Muller C-elements (see Fig 6(b)), increasing the circuit complexity with about 30% and reducing its speed with nearly the same factor.

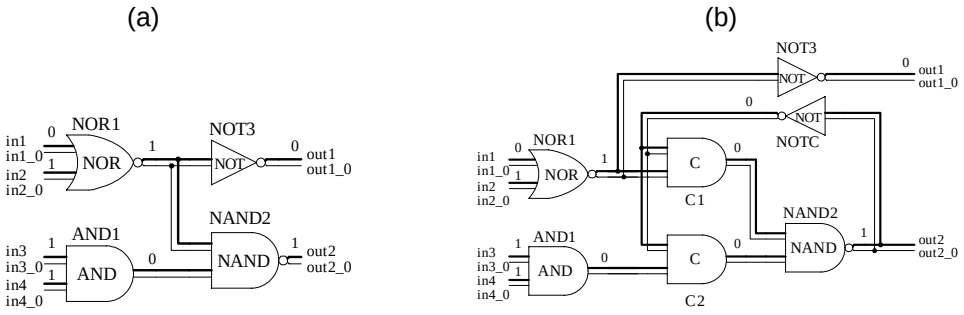


Fig. 3 Asynchronous DR digital circuit without (a) and with (b) handshaking feedbacks.

Being no more DI, the correct operation of the circuit in Fig. 3(a) depends on certain assumptions about the delay times of the composing gates, whose violation will cause erroneous behaviour. Such behaviour can be avoided already during the design phase, if proper handling of the time-domain characteristics of the gates can be performed. In [14], we have reported on our novel technique for manipulation of the RSFQ time-delays, while in [15] we present our efficient approach for statistical prediction of the RSFQ time-delay spread due to the spread of the technological parameters. In the next section of this paper, we describe our software tool for high-level simulation and verification of asynchronous RSFQ digital circuits, in which these both techniques have been successfully incorporated.

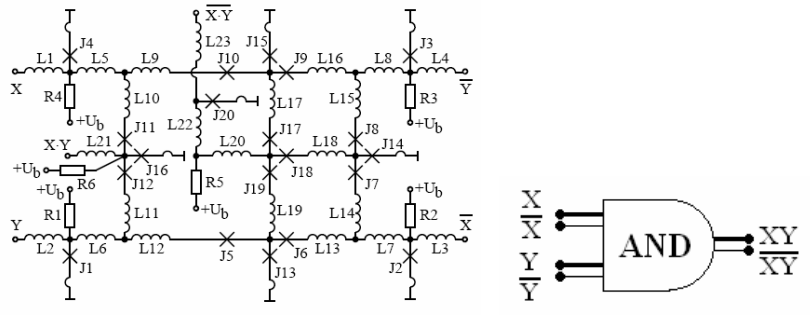
HIGH-LEVEL SIMULATION AND VERIFICATION OF ASYNCHRONOUS RSFQ DIGITAL CIRCUTS

The main problem prohibiting the straightforward high-level simulation and verification of complex asynchronous RSFQ digital circuits is the unique nature of the SFQ data

coding. As seen from (1), the SFQ data are carried by picosecond voltage pulses instead of voltage levels as by the classical semiconductors. However, all established tools for high-level design are addressed to the semiconductor electronics, i.e. are not compatible with the SFQ data coding.

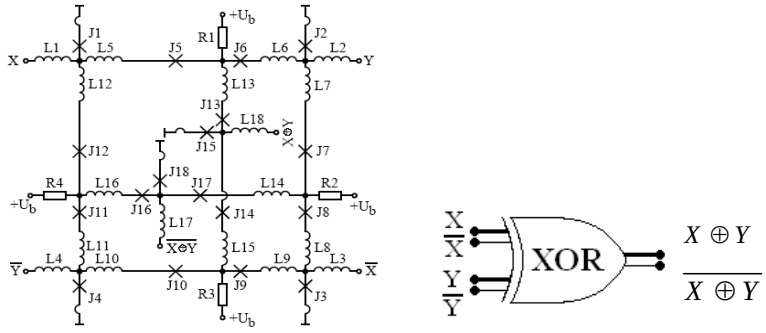
Our basic idea to solve this problem is to use a general purpose logic level description language for digital devices, and to adapt it to the specifics of the asynchronous RSFQ electronics. For this, we have chosen the **V**ery high speed integrated circuit **h**ardware **d**escription **l**anguage (VHDL) [16]. It is a part of the powerful commercial tool for logic-level simulation and verification of complex digital circuits ModelSim [17] and is mainly addressed to the level-based synchronous semiconductor electronics. We have elaborated a special approach for VHDL interpretation of DR SFQ data exchange and developed VHDL models of all components of our asynchronous RSFQ cell library [13].

Below, we illustrate this about two of the most complex gates – the DR AND and the DR XOR one. Their schematics, electrical symbols, and true tables are given in Fig. 4 and Fig. 5, respectively, while their elements' values and operation principles can be found in [13], [11].



X	1	1	0	0
$\overline{X}$	0	0	1	1
Y	1	0	1	0
$\overline{Y}$	0	1	0	1
XY	1	0	0	0
$\overline{XY}$	0	1	1	1
	1	2	3	4

Fig. 4 Electrical scheme, electrical symbol, and true table of the asynchronous DR RSFQ AND gate



X	1	1	0	0
$\overline{X}$	0	0	1	1
Y	1	0	1	0
$\overline{Y}$	0	1	0	1
$X \oplus Y$	0	1	1	0
$\overline{X \oplus Y}$	1	0	0	1
	1	2	3	4

Fig. 5 Electrical scheme, electrical symbol, and true table of the asynchronous DR RSFQ XOR gate

The time-domain behaviour of the both gates, which has been obtained from our high-level simulations, is shown in Fig. 6 and Fig. 7, respectively. They have also been simulated at low level with the freeware simulator for RSFQ circuits JSIM [18] and the resulting oscillograms are also shown in Fig. 6 and Fig. 7. The perfect agreement between the both sets of results demonstrates clearly the exactness of our approach for high-level modelling of the asynchronous RSFQ digital circuits.

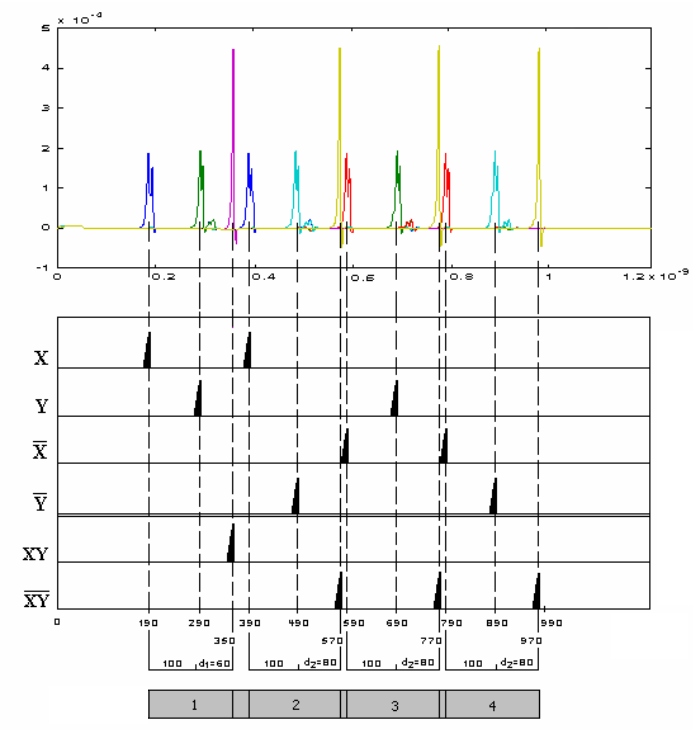


Fig. 6 Input-output signals of the DR RSFQ AND gate, obtained after simulations with JSIM (up) and the VHDL-modelling with ModelSim (down).

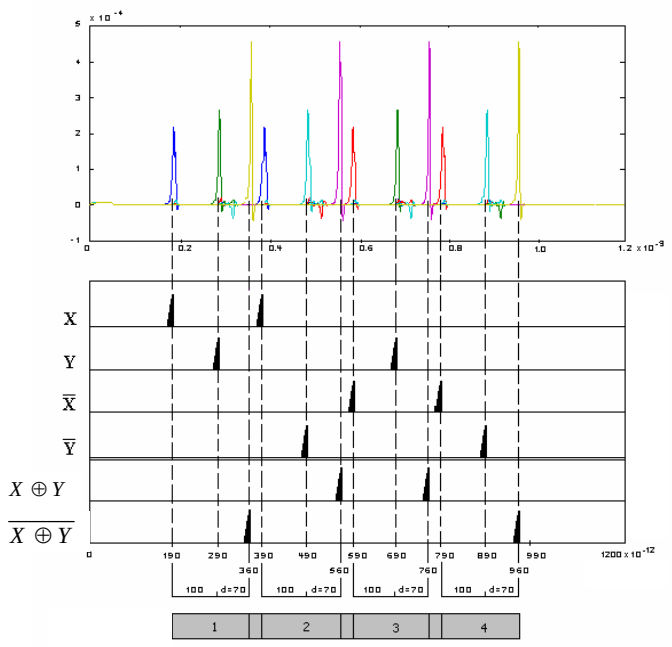


Fig. 7 Input-output signals of the DR RSFQ XOR gate, obtained after simulations with JSIM (up) and the VHDL-modelling with ModelSim (down).

CONCLUSIONS

We have used the general purpose high-level description language VHDL and elaborated a special approach for VHDL modelling of SFQ data exchange. It has been implemented into a software tool for high-level modelling and simulation of complex asynchronous RSFQ digital circuits. In this tool, we have also implemented our novel

technique for manipulation of the RSFQ delay times, allowing asynchronous design with reduced number of handshaking feedbacks. Once the complex circuit is designed, this tool checks for its delay-insensitivity using our novel approach for statistical prediction of the RSFQ delay times. Thus, reliable large-scale asynchronous RSFQ digital circuits with improved operation speed and simplified topology can be developed.

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