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Thermoelectric Microgenerators with Nanometric Films

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Abstract

A thermoelectric in-plane micro-generator with nanometric films has been fabricated using compatible standard semiconductor technologies (MEMS). The active material is a nanolayer polycrystalline silicon material laid on a dielectric membrane sustained by a silicon frame. Thermal properties of semiconductor nanostructures have recently attracted a lot of attention. This is primarily due to two major factors. The first one is a continuous scaling down of the feature sizes in microelectronic devices and circuits, which leads to an increase in power dissipation per unit area of semiconductor chip. Under such conditions, the influence of size effects on thermal conductivity becomes extremely important for device design and reliability.

Introduction

Hicks and Dresselhouse predicted a huge increase of figure of merit ZT if the dimensionality of the electron system in thermoelectric materials is reduced from 3D behavior in bulk materials to 2D behavior via nanoscal layers. Reduced dimensionality offers one strategy for increasing *ZT* relative to bulk values [1-2]. The use of low-dimensional systems for thermoelectric applications is of interest because low dimensionality provides: (1) a method for enhancing the density of states near E_F, leading to an enhancement of the Seebeck coefficient, (2) opportunities to take advantage of the anisotropic Fermi surfaces in multi-valley cubic semiconductors, (3) opportunities to increase the boundary scattering of phonons at the barrier-well interfaces, without as large an increase in electron scattering at the interface, (4) opportunities for increased carrier mobilities at a given carrier concentration when quantum confinement conditions are satisfied [3].

It has been suggested that the thermoelectric figure of merit $ZT=S^2\sigma/(k_{ph}+k_e)$ can be significantly enhanced in quantum wells and quantum wires because of strong carrier confinement (where S is the Seebeck coefficient, σ is the electric conductivity, k_{ph} is the lattice thermal conductivity, and k_e is the electronic thermal conductivity). An increase to the thermoelectric figure of merit may also come from the drop of the lattice thermal conductivity in low-dimensional structures due to the increased phonon-boundary scattering. Experimental evidence of the thermal conductivity drop in thin Si films has also been demonstrated [4]. Recently, Balandin and Wang and Khitun have shown that an additional increase to *ZT* can be brought by the spatial confinement of acoustic phonons in thin films (quantum wells) and quantum wire structures embedded within material of distinctively different elastic properties [5]. Thus, low-dimensional confinement of both carriers and phonons allows for more degrees of freedom in maximizing *ZT*.

Design of microgenerators

Simplified one-dimensional model of the microgenerator is showed in figure 1.

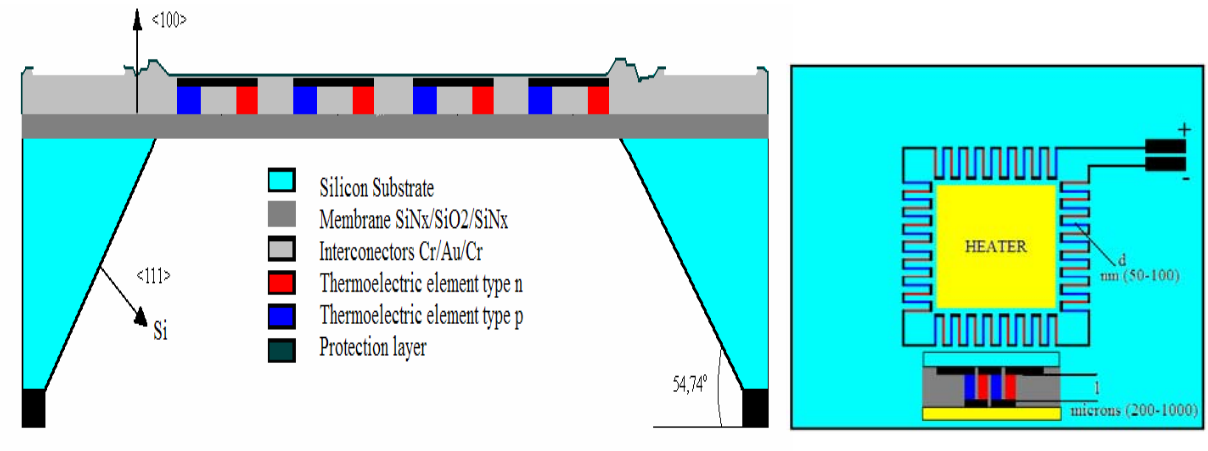

Fig.1. Cross-sectional view of a thermoelectric microgenerator

The optimal geometry of the micro-generator depends on the thermal properties and emissivity of the materials as well as on its working environment i.e. air or vacuum and on its operational mode. These investigations have been extended to a more realistic geometry of micro-generators and to more efficient thermoelectric materials, using a numerical model. The performance of such micro-generators is predicted for various materials and geometry combinations. The origin of this optimum arises from a competition between the temperature difference along the thermoelectric legs that will be higher with thinner legs and the electrical resistance of the device that increases when the thermoelement thickness decreases. If we assume the heating power to be proportional to the area covered by the heater, the optimum leg length calculated is the result of a competition between the heating power that increases when the heater surface increases, the increase of the thermal conductance (i.e. the decrease of the temperature rise along the thermoelectric legs) and the decrease of the electrical resistance when the thermoelectric leg length decreases.

The measurements have shown that the lateral thermal conductivity of a Si_3N_4 (150 nm) / monocrystalline Si (150 nm) / SiO_2 (300 nm) structure was about 1.5% of the conductivity of the bulk Si and was almost a constant in the temperature range from T=293 K to T=413 K. The total error for the measurements was estimated to be less than 20 %. Although the model presented here assumed a freestanding quantum well, the results can be extended to quantum wells with rigid boundaries. The lowest confined phonon modes in quantum well with clamped-surface boundary conditions are higher in energy than those in a free-standing quantum well, but the overall behavior and the decrease of the group velocities are very similar in both cases. Applied to a 150 nm wide Si well, this model gives k_{ph}=66.7 W/mK. For comparison, experimentally measured thermal conductivity of bulk Si is 148 W/m K. This is a significant drop although much less then that observed in the experiment. The temperature dependence of the calculated k_{ph} is very close to the measured one. In the figure 2 we show the dependence of lattice thermal conductivity with temperature for bulk silicon (300 mm) and thin film silicon (100 nm).

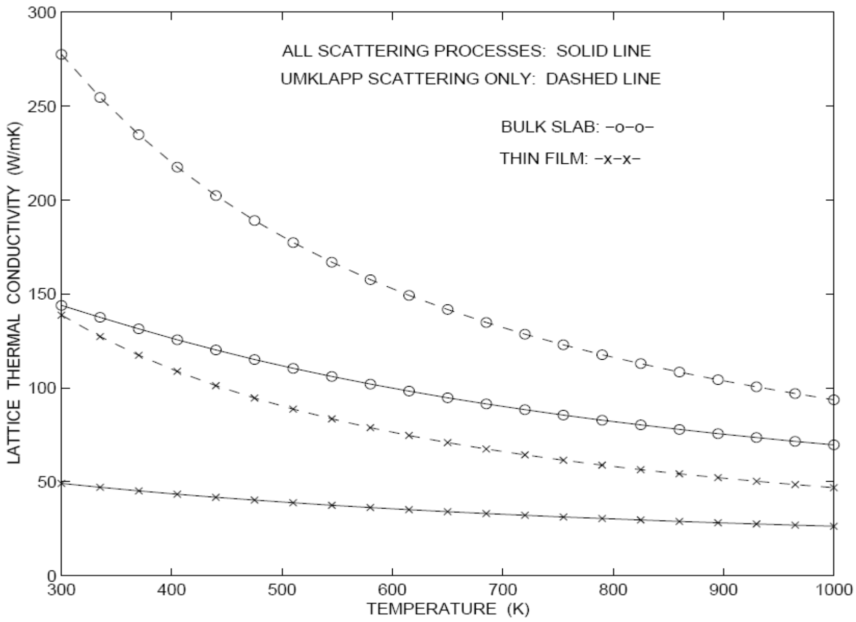

Figure 2 Lattice conductivity of silicon for bulk materials and thin film materials

Modes of working

Two modes of working are anticipated for the in-plane thermoelectric micro-generator. The first mode of working (i.e. mRTG) is when the heat source is on the membrane (Fig. 3a).The silicon frame that sustains the membrane is the cold side. A large temperature difference along the thermoelectric legs should be created with small heat sources because the thickness of the area covered by the thermoelectric leg is thin (1250 nm) and its thermal conductivity is low (3.9 $W.m^{-1}.K^{-1}$). This large temperature difference is interesting to get high efficiency. The second mode of working (i.e. BHPW) takes advantage of the large surface-to-volume ratio of the membrane to use it as a radiator, the hot side being the silicon frame (Fig. 2b). The heat source may be the heat generated by a living creature while the coolant could be simply air.

a) b)

Figure 3 Termogenerators with silicon nanometric films

The fabrication methods

Low stress-silicon nitride (Si_3N_4) and silicon dioxide (SiO_2) sandwich layers were deposited on a <100> oriented silicon wafer by low pressure chemical vapor deposition (LPCVD). I open a window that crosses multilayer Si_3N_4 /SiO2 /Si_3N_4 with plasma-chemical attack (RIE) corrode with reactive ions CF_4/O_2 with crosses a photo sensible lake mask. A polycrystalline silicon layer was deposited by LPCVD at 600°C and patterned by wet etching, to define the position of the thermoelectric legs on the front side of the wafer. Selected legs were implanted with boron (p-type) at 40 keV energy and with a flux 4, 5 x 10^{15} cm^{-2} while other legs were implanted with phosphorus (n-type) at 80 keV and with a flux 10^{16} cm^{-2}.

The polycrystalline film was annealed at 900°C. The micro-heaters and the interconnections were made by patterning a Cr/Au/Cr sandwich layer by lift-off. A silicon nitride passivation layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) and the electrical contacts were opened by plasma etching. The membrane was released by bulk etching using KOH. The film deposition procedures, film properties and measurement methods are described more precisely elsewhere.3-4 a top view of the micro-generator is shown in figure 1. It consists of a metallic micro-heater placed in the center of the membrane to simulate a heat source. The thermoelectric legs and the interconnections can be seen around the spiraled heater. A narrow metal strip is also made between the spiraled heater and the thermoelectric leg area. It is used to measure the temperature drop along the thermoelectric legs through the change of its electrical resistance.

Results

In the numerical simulation, the electrical current flowing in the thermo elements decreases the temperature drop along the thermoelectric legs. It is therefore advantageous to decrease the thermoelectric leg thickness to get a higher temperature rise along the thermo elements.

In the table 1 we show the results of silicon thermoelectric microgenerators with nanometric films. These results depend of many parameters such as: numbers of couples, thickness of films, gradient of temperature and dissipation (vacuum or air).

Table 1

Polisilicon	ε	K_T [mW/K]	d_T [nm]	ZT_m	ΔT [K]	ΔV [V]	W [mW]
L =1,6 x 1,6 mm 50 couples P = 1 mW	vacuum	180	150	0,014	8,0	0,13	0,090
	air	150	190	0,016	5,1	0,084	0,058
L =1,6 x 1,6 mm 500 couples P = 5 mW	vacuum	270	140	0,014	9,9	1,6	0,58
	air	200	240	0,018	4,2	0,70	0,24
L =1,6 x 1,6 mm 500 couples P = 10 mW	vacuum	270	140	0,014	20	3,3	2,3
	air	200	240	0,018	8,4	1,4	0,98

Conclusions

Decrease of the lattice thermal conductivity is important for further development of nanostructure-based thermoelectric devices. The decrease may also complicate the heat management problem for future deep-submicron silicon-based devices and circuits. The theoretical results presented in this paper favorably agree with the recent experimental investigation of the lateral thermal conductivity of quantum wells (thin films). It was shown that modification of the lattice thermal conductivity by confined phonon modes opens up a novel tuning capability of thermoelectric properties of heterostructures, and may lead to a strong increase of the thermoelectric figure of merit, in specially designed semiconductor nanostructures.

A compact silicon thermoelectric device may be able to produce as much as 100 mW with an output voltage of about 1.5 Volt, necessary for biasing a CMOS chip with different applications. Nevertheless, the electrical contact resistances have to be lowered to a satisfactory level, good thermoelectric materials have to be used and thermoelectric thick-film technology needs to be improved or developed to get films with good thermoelectric properties at an acceptable economical cost.

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