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A Simplified Space Vector Pulse With Modulation (SVPWM) Algorithm for Diode Clamoing Five Level Inverter With DC-Voltage Balancing

Introduction

Multilevel inverters have more advantages than the standard two level inverters. AC-link voltage harmonics are lower due to the increase of output voltage levels. The blocking voltage of each switch is also reduced [1],[2].

Performance of multilevel inverters depends on the PWM algorithm. The triangular-sinusoidal and the hysteresis PWM are dissuaded in the case of multilevel inverters because they can not deal with the major drawback of multilevel inverters which is the DC-link capacitor voltage balancing.

The space vector pulse with modulation has more advantages comparing to triangular-sinusoidal and hysteresis PWM. In space vector modulation we have more freedom to choice the sequences of the states of the inverter devices. This free choice can be used in order to minimize switching losses, to reduce output ripple or to obtain the input neutral point balancing.

Several works apply the SVPWM to the three level inverter like [3],[4] and [5]. These works use a typical SVPWM method, which approximate the output voltage by using the nearest three output vectors (the nodes of the triangle containing the reference vector in the space vector diagram of the inverter). When the reference vector changes from one region to another, it may induce an output vector abrupt change. In addition we need to calculate the switching sequences and switching time of the states at every change of the reference voltage location. Thus the computational complexity is greatly increasing with the increasing number of the reference vectors, and it is a main limitation of the application of this typical SVPWM.

In [6], A new simplified SVPWM for three level inverter is proposed. It consists of reduce the three level SVPWM to the conventional two level SVPWM. Indeed, the space vector diagram of the three level inverter can be thought that is composed of

six small hexagons that are the space vector diagrams of conventional two level inverter. From the location of the reference voltage vector, we select one of these hexagons. Afterwards we substrate the amount of the center voltage of the selected hexagon from the original reference voltage. By these two steps, the three level space vector plane is transformed to the two level space vector plane.

In [7], This method is extended to the case of five level inverter. The space vector diagram of a five level inverter is decomposed to six small hexagons that are the space vector diagrams of the three level inverter. In turn, each space vector diagrams of three level inverter is decomposed to six small hexagons that are the space vector diagrams of two level inverters.
In this work, we use this simplified method to control the five level inverter, and we show that we can use the redundant vectors of the space vector diagram of the inverter in order to ensure stabilisation of the input DC voltages of the inverter.

I. Svpwm for two level inverter

The SVPWM strategy is proposed in [8]. It consists of the generation of a specific sequence of states of the inverter. The reference voltage vector is defined as:

$$V^*=v_a^*.e^{j0}+v_b^*.e^{j2\pi/3}+v_c^*.e^{j4\pi/3} \quad (1)$$

where $v_a^*, v_b^*, \text{and } v_c^*$ are the reference stator voltages of phases a, b, and c.

The vector V^* can take eight positions in the complex plane according to values of the phases a, b, c switching signals Fa, Fb and Fc. Fig.1 gives the complex plane of the voltage and TableI gives the correspondence between the switching signals and the voltage vector position. Vectors v1-v6 divide the d-q plane into six sectors of 60° long. In turn, each sector is divided into N equal switching intervals. Each switching interval correspond to Ts=T/N seconds, where T is the period of output voltage. In each interval, the voltage reference vector is generated by combining the two vectors vx state X) and vy (state Y), limiting the sector which include the switching interval, in addition to a zero sequence voltage vz (state Z), which is v0 or v7:

$$V^*=d_x.v_x+d_y.v_y+d_z.v_z \quad (2)$$

The duty ratios dx, dy and dz of the states X, Y and Z are calculated as:

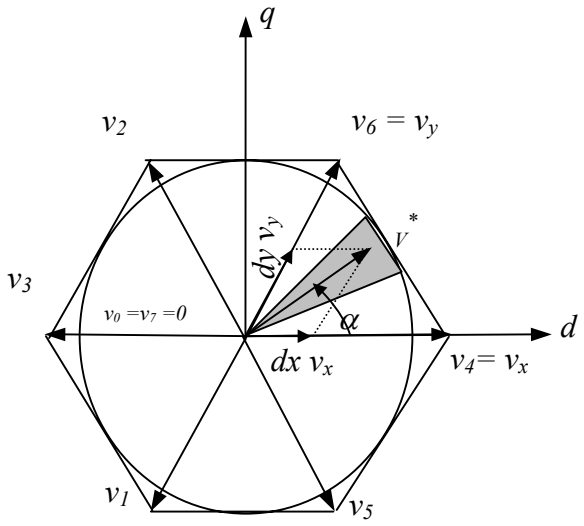


Fig.1. Space vector diagram of two level inverter.

$$d_x = M.\sin(\pi/6 - \beta)$$
$$d_y = M.\sin(\beta)$$
$$d_z = 1 - d_x - d_y \qquad (3)$$

where β is the center angle of the given switching interval measured with respect to the beginning of the sector.

Because of the free choice of Z between v0 and v7, the sequence of state in each switching interval can be made in different manners. The sequence YXZ2/XYZ1/YXZ2…… ,where Z1 and Z2 are complementary v0 and v7 , allows transition from one state to another by switching of one inverter leg only.

II. five level inverter sescription

Fig.2 shows a schematic diagram of a five level diode clamping inverter. Each phase of the inverter consists of eight switching devices and six clamping diodes. The DC supply consists of four capacities in series. Table 1 shows the switching states of each phase of the inverter. Since five kinds of switching states exists in each phase, the five level inverter has 53 = 125 switching states. Fig.3 shows the space vector representation of the output voltages [9].

The voltage vectors are identified as P2ON1, P1N1N1, etc. For example, in the case of P2ON1, the output terminals U,V, and W have the potentials 2E, 0, and –E respectively.

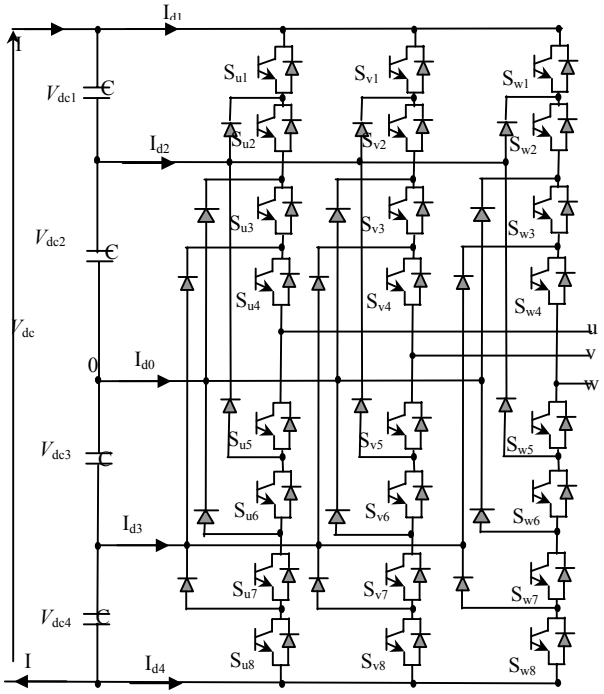


Fig.2. Circuit diagram of five level inverter

States / mode	*Sx1*	Sx2	Sx3	Sx4	Sx5	Sx6	Sx7	Sx8	V_{xo}
P_2	1	1	1	1	0	0	0	0	**2E**
P_1	0	1	1	1	1	0	0	0	**E**
O	0	0	1	1	1	1	0	0	**0**
N_1	0	0	0	1	1	1	1	0	**-E**
N_2	0	0	0	0	1	1	1	1	**-2E**

Table 1. Switching states of the five level inverter

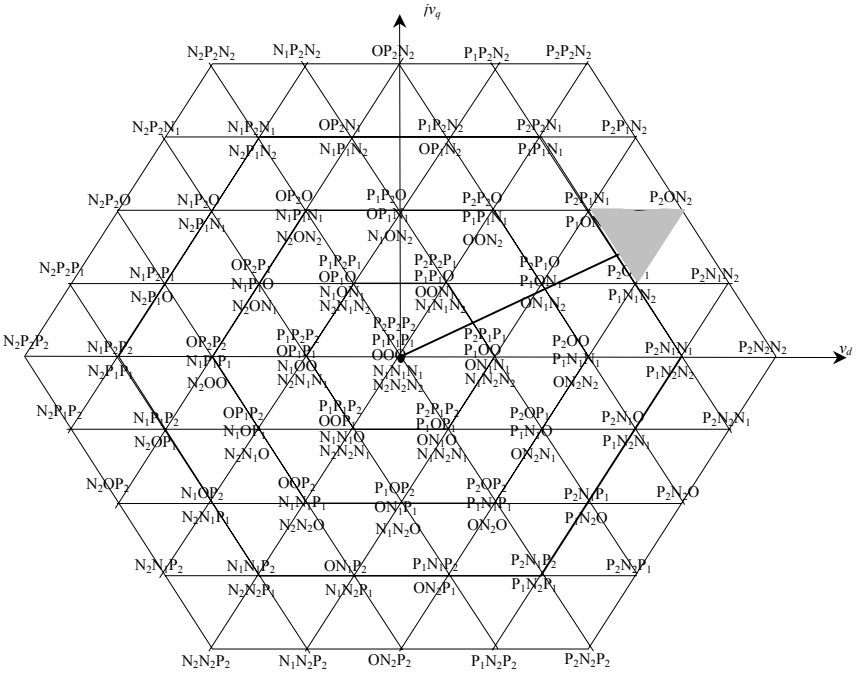


Fig. 3.Space vector diagram of five level inverter

III. simplified svpwm for five level inverter

The space vector diagram of a five level inverter can be thought that is composed of six small hexagons that are the space vector diagrams of the three level inverters [4]. Each of these six hexagons, constituting the space vector diagram of a three level inverter, centers on the six apexes of the medium hexagon as shown in fig.4 .

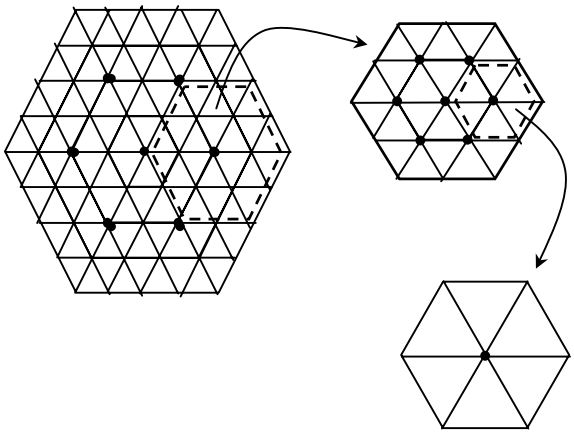


Fig.4. Simplification of a five level space vector diagram into two level space vector diagrams

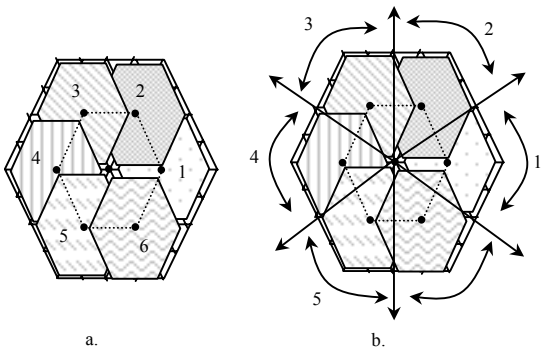


Fig. 5. Selection of hexagon's number

In turn, the space vector diagram of the three level inverter can be thought that it is composed of six small hexagons that are the space vector diagram of conventional two level inverter. These hexagons are centered on the six apexes of the inner hexagon as shown in fig.4.

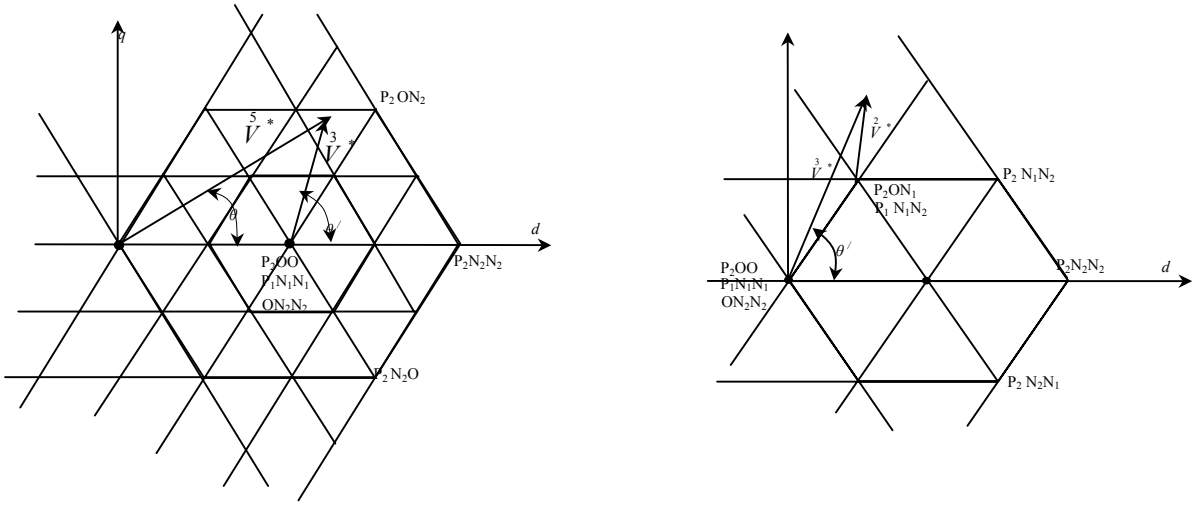
A. First correction of the reference voltage vector

By the location of a given reference voltage vector, one hexagon is selected among the six small hexagons that comprise the three level space vector diagram. There exist some regions that are overlapped by two adjacent small hexagons (fig.5.a). These regions will be divided in equality between the two hexagons as shown in fig.5.b. In this case the hexagon number s is selected as following:

$$\begin{aligned} \overset{3}{V}^{*} &= \overset{3}{v_d}^{*} + i\,\overset{3}{v_q}^{*} \\ &= \overset{3}{v}.e^{j\theta} \end{aligned}$$

$$s = \begin{cases} 1 & \text{if } \frac{-\pi}{6} < \theta < \frac{\pi}{6} \\ 2 & \text{if } \frac{\pi}{6} < \theta < \frac{\pi}{2} \\ 3 & \text{if } \frac{\pi}{2} < \theta < \frac{5\pi}{6} \\ 4 & \text{if } \frac{5\pi}{6} < \theta < \frac{7\pi}{6} \\ 5 & \text{if } \frac{7\pi}{6} < \theta < \frac{3\pi}{2} \\ 6 & \text{if } \frac{3\pi}{2} < \theta < \frac{11\pi}{6} \end{cases} \qquad (4)$$

Once the value of s is determined, the origin of the reference voltage vector is changed to the center voltage vector of the selected hexagon. This is done by subtracting the center vector of the selected hexagon from the original reference



a. b.

Fig.6. correction of reference vectors

S	$\overset{3}{V}_d^*$	$\overset{3}{V}_q^*$
1	$\overset{5}{V}_d^* - 2.E.\cos(0°)$	$\overset{5}{V}_d^* - 2.E.\sin(0°)$
2	$\overset{5}{V}_d^* - 2.E.\cos(\pi/3)$	$\overset{5}{V}_d^* - 2.E.\sin(\pi/3)$
3	$\overset{5}{V}_d^* - 2.E.\cos(2\pi/3)$	$\overset{5}{V}_d^* - 2.E.\sin(2\pi/3)$
4	$\overset{5}{V}_d^* - 2.E.\cos(\pi)$	$\overset{5}{V}_d^* - 2.E.\sin(\pi)$
5	$\overset{5}{V}_d^* - 2.E.\cos(4\pi/3)$	$\overset{5}{V}_d^* - 2.E.\sin(4\pi/3)$
6	$\overset{5}{V}_d^* - 2.E.\cos(5\pi/3)$	$\overset{5}{V}_d^* - 2.E.\sin(5\pi/3)$

Table2. Correction of reference voltage vectors.

vector. Fig.6.a shows the original reference voltage vector $\overset{5}{V}^*$ and the corrected reference voltage vector $\overset{3}{V}^*$ seen from the location of (P2OO), (P1P1N1), and (ON2N2) vectors. Table 2 gives the components of the corrected reference voltage $\overset{3}{V}^*$ in terms of the components of $\overset{5}{V}^*$ for the six hexagons.

B. Second correction of the reference voltage vector

From the location of this vector, one hexagon is selected among those that comprise the three level space vector diagram, as made in the first correction. Once the hexagon is determined, the origin of the reference voltage vector is changed to the center voltage vector of the selected hexagon.

Fig.6.b shows the corrected reference voltage vector $\vec{V}^{3*}$ and the reference voltage vector after second correction $\vec{V}^{2*}$, seen from the location of (P2N1N1) and (P1N2N2) vectors. The components of the corrected reference voltage vector is calculated like mentioned in Table 2, replacing $\vec{V}^{5*}$ by $\vec{V}^{3*}$ and $\vec{V}^{3*}$ by $\vec{V}^{2*}$.

C. Switching intervals

Once the final corrected reference voltage $\vec{V}^{2*}$ and the corresponding hexagon are determined, we can apply the conventional two level space vector PWM to the inverter. The reference voltage vector $\vec{V}^{2*}$ is generated by combining states X, Y, and Z. The states X and Y represent limits of the section in which the vector $\vec{V}^{2*}$ falls, while the state Z represents the center of the selected hexagon.

Because of the redundant voltage vectors of each state, we can choose X, Y, and Z in several manners. This choice is generally determined by two factors: Firstly, we choose X, Y, and Z in such a manner that the transition from one state to another involves switching of one device only, in order to decrease losses in the inverter. Secondly, we choose the states X, Y, and Z in order to control the neutral point potential of the DC- supply.

IV. Simulation results

In order to prove the validity of the proposed SVPWM method, we simulate the association of the five level inverter with an induction motor. We consider here that the input DC voltages are constants during the simulation. Table 3 gives the simulation parameters of the inverter and the motor. The simulation is made using Matlab-Simulink.. Fig.7 shows the output voltage of the inverter and its spectrum analysis.

SVPWM parameters	Modulation index m=0.8 DC supply voltage V_{dc} =800 V Number of switching intervals N=120
Induction motor parameters	R_s = 3.085 Ω; R_r = 4.85 Ω ; l_s = 0.274 H; l_r = 0.274 H; l_m = 0.258 H; p = 2; f = 50 Hz

Table 3. Simulation parameters

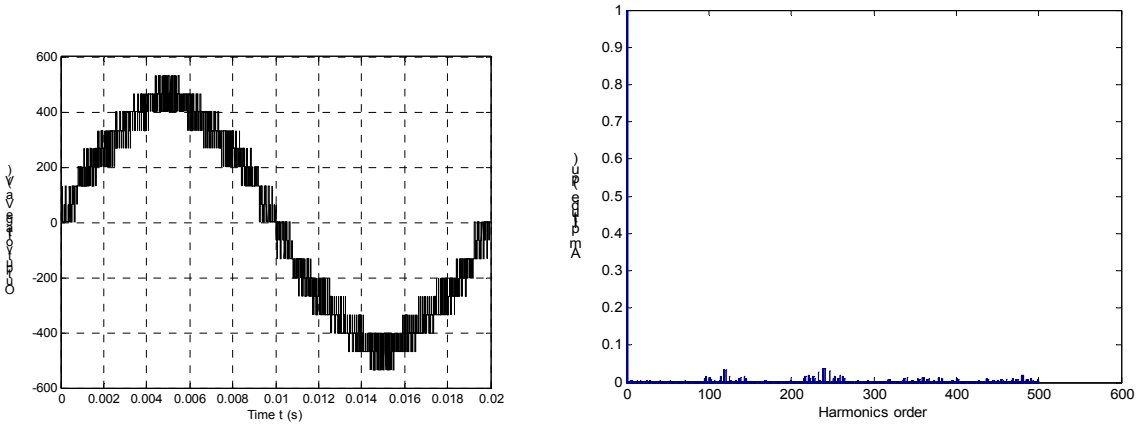


fig.7 Output voltage and its spectrum analysis.

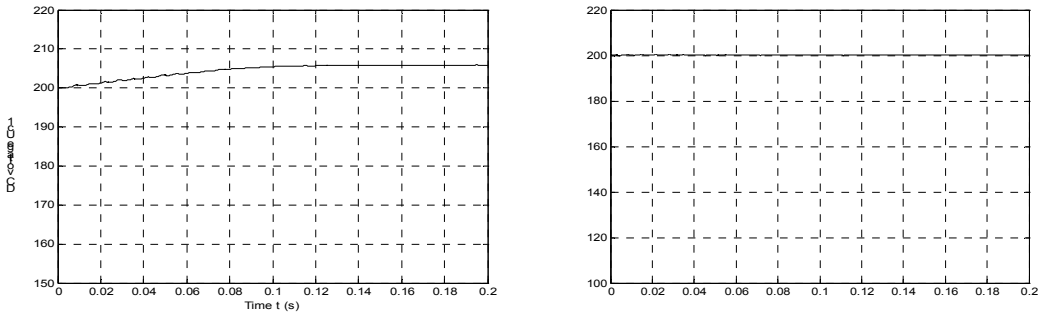
We show that the output voltage is closer to a sinusoidal signal. Its harmonics is centered around multiples of the number of sectors N (Here we choose N =120). So by choosing N as large as possible, we can push the harmonics of the output voltage to high orders. But this can cause high losses in the inverter.

V. DC voltage control

In the previous sections, it is assumed that the input DC voltages are constants. Actually, this assumption is not correct: If we will not taking some precautions, the neutral point potential will changing depending on the load current of the inverter.

A most accurate model of the input DC voltage of the inverter is given by following equations:

$$
\begin{aligned}
C\frac{dV_{dc1}}{dt} &= I - i_{d1} \\
C\frac{dV_{dc2}}{dt} &= I - i_{d1} - i_{d2} \\
C\frac{dV_{dc3}}{dt} &= I + i_{d3} + i_{d4} \\
C\frac{dV_{dc4}}{dt} &= I + i_{d4} \\
i_{d1} &= F_{11}.F_{12}.F_{13}.F_{14}.i_a + F_{21}.F_{22}.F_{23}.F_{24}.i_b + F_{31}.F_{32}.F_{33}.F_{34}.i_c \\
i_{d2} &= F_{12}.F_{13}.F_{14}.F_{15}.i_a + F_{22}.F_{23}.F_{24}.F_{25}.i_b + F_{32}.F_{33}.F_{34}.F_{35}.i_c \\
i_{d0} &= F_{13}.F_{14}.F_{15}.F_{16}.i_a + F_{23}.F_{24}.F_{25}.F_{26}.i_b + F_{33}.F_{34}.F_{35}.F_{36}.i_c \\
i_{d3} &= F_{14}.F_{15}.F_{16}.F_{17}.i_a + F_{24}.F_{25}.F_{26}.F_{27}.i_b + F_{34}.F_{35}.F_{36}.F_{37}.i_c \\
i_{d4} &= F_{15}.F_{16}.F_{17}.F_{18}.i_a + F_{25}.F_{26}.F_{27}.F_{28}.i_b + F_{35}.F_{36}.F_{37}.F_{38}.i_c
\end{aligned}
\tag{5}
$$



a. b.

fig. 8. DC voltage V_{c1} :

a. without using control algorithm
b. using control algorithm

where Vdc1 ,Vdc2 , Vdc3 and Vdc4 are capacitors voltages, id0, id1, id2 , id3 and id2 are input currents of the inverter, I is the left side current of the capacitors, and Fij (i=1,3, j=1,4) are commutation functions of switching devices (fig.2).

From this model, we can see that the capacitors voltages Vdc1, Vdc2, Vdc3 and Vdc4 depends on the states Fij of the inverter. i.e on the redundant vectors of the space vector diagram of the inverter. Some of these redundant vectors cause charging of the capacitances (and hence increasing voltages) and some others cause discharging of the capacitances (and hence decreasing of voltages).

In the space vector diagram of the inverter (fig.3) we call the lower redundant vectors: negative vectors, and the upper redundant vectors: positive vectors. For example: in the hashed region of fig.3, P1N1N1 and P1ON1 are negatives vectors, while P2ON1 and P2N1N1 are positive vectors.

We simulate the inverter and its DC supply using only the positive redundant vectors. Fig.8.a. gives the DC voltage Vdc1 in this case. We show that from the beginning the DC voltage Vdc1 change from its initial value (200V).

In order to keep the DC voltages in their initial values , we use an algorithm which change between positive and negative redundant vectors. depending on the values of Vdc1 Vdc2 , Vdc3 and Vdc4. We make a continuous sensation of the dc voltages. If (Vdc1 > 0 or Vdc4 > 0 or Vdc2 < 0 or Vdc3 < 0) we use positive redundant vectors, and if (Vdc1< 0 or Vdc4 < 0 or Vdc2 > 0 or Vdc3 > 0) we use negative vectors to generate The output voltage.

The simulation (fig.8.b) shows that the DC voltage Uc1 take constant value during all the simulation time. This results prove the efficiency of the proposed control method.

VI. Conclusion

In this paper, a simplification of the SVPWM applied to diode clamping five level inverter is studied. To make this simplification, the SVPWM for five level inverter is reduced into SVPWM for three level inverter. In turn, the SVPWM for three level inverter is reduced to SVPWM for two level inverter. This simplification reduced considerably the computation time. We can generalize this method to high order multilevel inverters. The flexibility of the SVPWM method, which is the free choice of switching sequences and redundant vectors, allows us to reduce the harmonics of the output voltage by choosing the adequate sequence of states in each switching interval. We also use this flexibility to ensure the balancing of the input DC voltages under any load conditions.

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