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# REAL-TIME OPERATION-BASED POWER CONSUMPTION ANALYSIS FOR PASSIVE UHF RFID TRANSPONDERS

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## ABSTRACT

This paper presents an operation-based power consumption model for passive RFID transponders. The digital section of the transponder is designed in compliance with ISO/IEC 18000-4/6 using a Faraday low-leakage standard cell library based on the UMC 0.13-$\mu m$ technology. The power consumption of the transponder is estimated under different operations, considering both static and dynamic power consumption. A methodology of real-time operation-dependent power consumption analysis is then proposed with classifying the command sets. The simulation results showed that the power consumption of the digital section of the transponder varies strongly over time depending on the operations. Finally a theoretical evaluation over the power saving with employing an automatic matching network before the power harvesting network is done.

***Index Terms***— RFID transponder, dynamic power consumption, tunable matching network

## 1. INTRODUCTION

RFID technologies are currently introduced in many application domains. In comparison to classical barcode based applications, transponder technologies can operate in the environments where optical tagging and reading methods are not very reliable. The wireless read-out of RFID transponders enables the indentification and tracking of moving objects and thereforenew real-time oriented process structures can be realised based on this technology. For long range detection, ultra-high/microwave operation frequency is applied to realize the wireless communication between reader and transponder through electromagnetic field. To reduce cost, the transponder is usually designed to be passive and no battery is embodyed. The reader has to provide the power supply for the transponder during the communication.

In passive far-field UHF/microwave RFID transponders, a power harvesting circuit is employed for converting a part of the collected RF power to DC power supply voltage. The transponder has different operations based on the received commands, i.e. compare, read/write memory, idle [1], and the current consumption is not constant but varies over time with respect to different operations. The impedance seen from the input of the power harvesting circuit varies with the change of the consumption current of the transponder. Therefore, an optimal matching network between the antenna and the power harvesting circuit for one operation cannot realize maximum power transfer for other operations.

State-of-art design [2] [3], however, devotes less investigation to the effect of the dynamic power consumption of the transponder on the overall power conversion efficiency. In former work [4], a methodology to analyse the power harvesting circuit with the focus on the effect of dynamic load current consumptions on the input impedance was proposed. The analysis showed that the overall power conversion efficiency was dramatically decreased at different current load with mismatching, e.g. from 30.1% to 2.3% as the load current changes from $1\mu A$ to $10\mu A$. The result suggests the necessity of optimising dynamically the impedance matching network between the antenna and the rectifier according to the transponder operation status.

For further improvement, the research is continued with investigating the power consumption variation of the transponder over time for different operation status, and theorectically evaluating the power saving with employing the automatic tunable matching network. In this work, the digital section of transponder was developed in compliance with ISO 18000-4/6 and the Faraday low-leakage standard cell library based on UMC 0.13-$\mu m$ technology was used to synthesize the designed circuit. We estimated the power consumption with Synopsys PrimeTime, aiming to examine the power consumption variation of the digital section in real time.

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This contribution is organised as follows: in Sect.2 we will introduce the background concerning the international air interface standards as well as the power consumption of digital circuits; in Sect.3 the design of digital section of the transponder and some power saving strategy is described; Sect.4 discusses the power consumption of individual blocks, as well as the power consumption variation in real-time. Besides, a theoretical analysis on power transmission link is given. Finally we give a conclusion and perspective for future research.

## 2. OVERVIEW

### 2.1. International Standard

ISO/IEC defines a series of RFID air interface standards from 18000-1 to 18000-7 for the item identification world. A diversity of RFID specifications is regulated. Several frequency bands have been assigned to RFID applications, such as 125KHz, 13.56MHz, 433MHz, 868MHz, $915MHz$ and 2.45GHz. Each frequency band has an individual parameter definition: modulation/demodulation, encoding/decoding etc.
ISO/IEC 18000-4 mode 1 and ISO/IEC 18000-6 type B define the same forward and return link parameters for passive tranponder operating. The commands are divided into the following functional groups: selection commands which define a subset of tags on the interrogating region to be identified or read/written to; identification commands which are used to perform to run the multiple tag identification protocol; data transfer commands which start the operation of reading from or writing to the tag memory [1].
Mandatory operations of transponder include: delimiter checking, command decoding, CRC checking, UID or data comparison, read/write memory, CRC code generating, frame building etc. For different commands tag performs different operations with different time cost. For example, with the 'Initialize' command, the tag shall go to the initial state without implementing comparison or memory access; with the 'Selection' command, the tag shall compare the received UID with its own UID, and then decide the further operation.

### 2.2. Power Consumption

For CMOS designs, the total power consumed by a circuit can be divided into two categories: static power and dynamic power. Static power is due to the reverse-biased diode leakage or source-to-drain sub-threshold leakage current when the transistors are not switching. The static power is also called leakage power and is dependent on the voltage, temperature, state of transistors. The leakage power is relatively constant and independent on the logic transitions. Dynamic power is the power consumed during the logic transition. Dynamic power contains two parts: one is from the charge or discharge the load capacitors during the voltage change, and the other is the short-time short cuicuit current between NMOS and PMOS. The value of dynamic power consumption is strongly dependent on the switching activities [5]. The mathematical expression of total power consumption is as follows:

$$P = \underbrace{V \times I_{leak}}_{P_{leak}} + \underbrace{\langle C \times V^2 \times f + V \times I_{sc} \rangle \times N}_{P_{dyn}} \quad (1)$$

where, $I_{leak}$ is the average leakage current; $I_{sc}$ is the mean short circuit current between NMOS and PMOS and is proportional to the operating frequency; $P_{leak}$ and $P_{dyn}$ are the leakage and dynamic power consumption respectively; $V$ is the supply voltage; $C$ is the average load capacitor; $N$ is the number of switching activities.
For passive RFID tags, the transmission data rate is around 40bit/s and the main operating frequency of designed digital section is set as 40kHz. With this operating frequency, the switching activities are not dense, hence a low dynamic power consumption. To bring down the static power consumption, the low leakage standard cells are used. To reduce the dynamic power consumption, clock gating technique is applied and the blocks not in use are totally stoped with no clock signal.

## 3. DESIGN OF UHF RFID TRANSPONDERS

In this work, the digital section of passive RFID transponders is designed and is synthesized with low-leakage standard cells from the Faraday library based on UMC 0.13-$\mu$m technology. The design contains the following functional blocks:

- Delimiter Check: which checks the start of the frame;
- CRC checking: check the received frame with CRC-16;
- Serial to Parallel converter: converts the received serial data to parallel, and store the command, address, data etc to corresponding buffers;
- command decoder: decode the command, and give the instructions to FSM;
- FSM: finite state machine, contains ready, ID, data exchange states;
- Comparator: compare the received data with the data in specific memory address;
- Collision Arbitration: includes an internal counter and pseudo random bit generator;
- Memory: synthesized with register arrays;

- Transmitter: includes CRC generating CRC-16 for the data to be transmitted; output register to store the output data.

The total area of the designed circuit is $89195\mu m^2$.

## 4. POWER CONSUMPTION ANALYSIS

In this design, we examine the power consumption of individual functional blocks and the variation of the total power consumption over time. With different commands, the tag has different operation time and different activate function blocks. We utilize the dynamic power management strategy–clock gating technique and employ the low-leakage standard cells for static power saving.

### 4.1. Power Consumption of Individual Blocks

A testbench has been designed: the input frame with the 'Selection' command. The simulation ran for 7ms, with which the UID of the designed transponder is sent back. After receiving the frame, the tag first does the CRC checking. If the CRC check is successful, the tag does serial to parallel conversion and stores the serial data to corresponding buffers. The command decoder decodes the data in command buffer, and sends an instruction to the finite state machine. The finite state machine enables the comparator to compare the received data with the data in the received memory address. When the data received matches with that of the targeted memory address, the tag sends back its UID. Table1 shows the data of the power consumption for different function blocks. With the employment of low-leakage standard cells, the leakage power is less than $3\%$ of the total power consumption, which is independent of switching activities and is constant over time. The dynamic power is dominant in total power consumption, which is proportional to the operation frequency and switch activities.
From table1 it can ben seen that more than $60\%$ is consumed by memory, comparator and transmitter. These blocks are designed with an enable signal and with automatic clock gating technique from Synopsys PrimeTime, the clock gates are automatically inserted by replacing the register enable signals with gated clocks, which greatly reduced the power consumption by the clock buffer tree and hence the total power consumption. The achieved result is comparable with the published data [6].

### 4.2. Power consumption Variation in time domain

Two simulations are done to investigate the power consumption variation over time: one input frame with 'Selection' command, address, data and correct CRC code; the other input frame with wrong CRC code. With a wrong CRC code, the further operations like comparison, memory access, CRC generating are not executed. The simulations are run with a step 0.5ms, and the power consumed by the tag is recorded. Fig.3 shows the power analysis over time. The solid line presents the power consumption of the tag when the CRC checking of the received frame is not correct, while the dash line presents the power consumption when CRC checking is correct. It can be seen that the power consumption of the tag strongly varies over time. The minimum power consumption is around $0.18\mu$W, while the maximum is $0.52\mu$W.

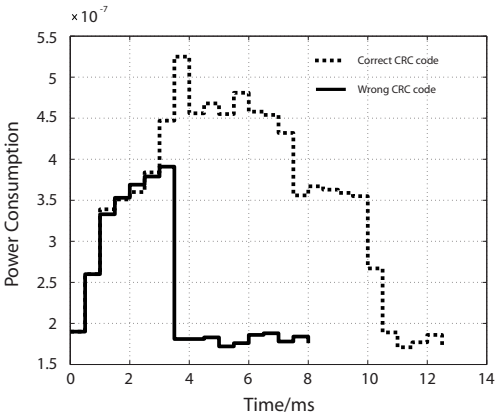


**Fig. 3**. Power Consumption Variation over time

### 4.3. Power Transmission Link

The matching network is designed for the maximum power consumption. With less power consumption, mismatch happens, and the power transmission still ensure the power requirement at the tag. However, the power conversion efficiency is strongly reduced. We take the 'Selection' command with correct CRC checking as an example. Assuming the overall power conversion efficiency(including the power transfer efficiency of the matching network) is $30\%$ [4], and with a maximum power consumption of $0.52\mu$W, the received power of the antenna has to be at least $1.73\mu$W for abtaining a maximum load current. When the transponder operates consuming less power, for example, $0.18\mu$W, the power utilization efficiency is only $10\%$. In this case, if a matching network is tuned with a feedback control signal, and a reader with automatically adpative emitted power, a considerable portion of power will be saved.
Fig.4 shows the power transmission link between reader and tag. We assume the power emitted from reader is $P_r$, the reader antenna gain is $G_r$, the transmission distance is $d$, the tag antenna gain is $G_t$, overall power conversion efficiency including the power trans-

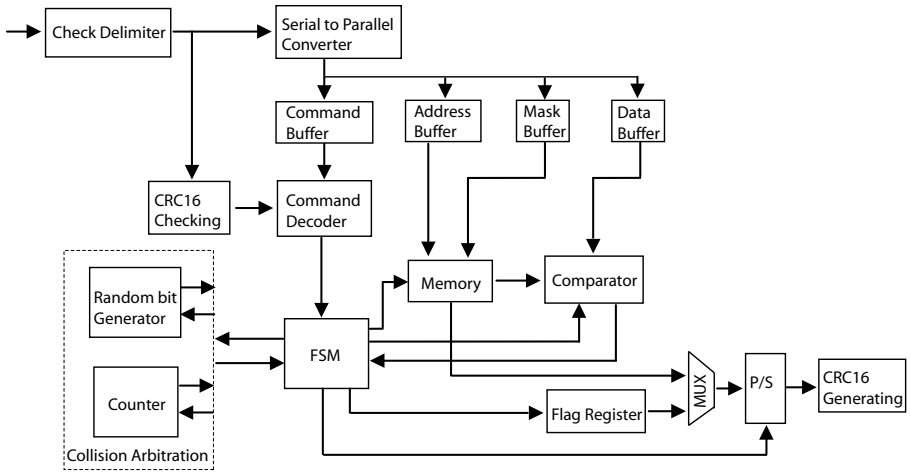


**Fig. 1**. Block Diagram of Digital Section of Transponder

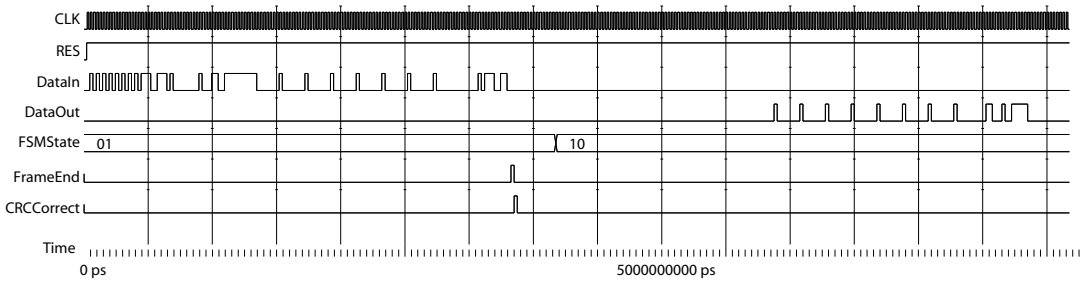


**Fig. 2**. Waveform of Tag Simulation

| Hierarchy | Dynamic Power/W | Leak Power/W | Total Power/W | Percentage |
|---|---|---|---|---|
| **Digital Core** | **3.954e-7** | **1.04e-8** | **4.06e-7** | **100** |
| Delimiter Check | 1.034e-8 | 6.68e-11 | 1.04e-8 | 2.6 |
| S/P converter | 6.01e-8 | 6.72e-10 | 6.08e-8 | 15 |
| CRC checking | 2.197e-8 | 9.96e-11 | 2.21e-8 | 5.4 |
| Command Decoder | 1.18e-8 | 1.97e-10 | 1.20e-8 | 3 |
| Comparator | 9.08e-8 | 2.34e-9 | 9.31e-8 | 22.9 |
| Collision Arbitration | 3.55e-8 | 1.43e-10 | 3.56e-8 | 8.8 |
| Memory | 7.91e-8 | 6.15e-9 | 8.53e-8 | 21 |
| Transmitter | 7.79e-8 | 7.02e-10 | 7.85e-8 | 19.4 |
| FSM | 2.19e-9 | 2.22e-11 | 2.22e-9 | 0.5 |
| Flag Register | 5.7e-9 | 1.85e-11 | 5.72e-9 | 1.4 |

**Table 1**. Power Consumption of Individual Blocks

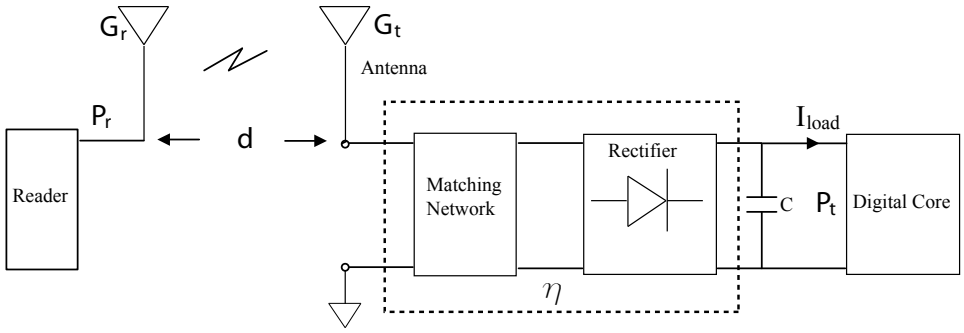


**Fig. 4**. Power Transmission Link

fer effciency of the matching network and the power conversion efficiency of the power harvesting network is $\eta$, the power consumption of the tag is $P_t$ and the operation frequency is $f_c$. The power transmission link can be expressed with the following equation:

$$\begin{aligned} P_t = \quad & P_r + 147.6 - 20log(d) - 20log(f_c) \\ & +10log(G_r) + 10log(G_t) + 10log(\eta) \end{aligned} \quad (2)$$

For simplicity, we assume that an omnidirectional antenna for both reader and tag is employed and the antenna gain is 1. The distance is set as 10m and the operation frequency is set as 2.45GHz for calculation. The optimal overall power conversion efficiency is set as $30\%$. Without employing the adaptive power emission at reader and automatic matching network at tag, the power emitted from reader has to fulfill the maximum power consumption of the transponder. With the above assumptions, maximum value of $P_t$ equals $0.52\mu$W, which results a $P_r$ = 1.8W. To execute the 'Selection' command, the average emitted power is 1.8W. With employing the adaptive power emission at reader and the automatic matching network at tag, we assume the power transfer efficiency of the matching network is optimised for all load power consumptions. The reader emits power adaptively according to the tag's needs, with the maximum emitted power 1.8W, and minimum emitted power 0.625W. To execute the 'Selection' command, the average emitted power is 1.2W, which saves $33\%$ emission power.

## 5. CONCLUSION

In this work, the digital section of the passive transponder is designed in compliance with ISO/IEC 18000-4/6. The power consumption of the transponder is estimated under different operations, considering both static and dynamic power consumption. The real-time operation-dependent analysis of the power consumption is then done and the simulation result is analyzed, with suggestion of employing a tunable matching network in order to maximize the overall power conversion efficiency. The achieved result can be used to aid the design of a feedback controller for automatic impedance matching.

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