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DESIGN OF INTEGRATED RAPID SINGLE FLUX QUANTUM CIRCUITS FOR FABRICATION IN A NIOBIUM-BASED FOUNDRY PROCESS

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ABSTRACT

The article describes the activities aimed at bringing superconductive high-speed electronics towards maturity. Integrated circuits based on the effects in superconducting materials have become feasible for some years already. The main focus lies on the so-called Rapid Single-Flux-Quantum (RSFQ) electronics which allows the combination of high operation frequencies (well above 20 GHz) with very low energy consumption when logical states are changed. Thus, this circuit technology exhibits a promising potential for realising energy-efficient modules for signal processing and computing. Recently, a dedicated design infrastructure has been developed in Europe. Closely associated is a foundry for digital RSFQ integrated circuits so that the fabrication of integrated circuits is viable. In the contribution, the basic features of the RSFQ circuit design are addressed with special emphasis on implementation on the wafer scale.

Index Terms— low-power digital electronics, superconductivity, integrated circuits, RSFQ

1. INTRODUCTION

The Rapid Single Flux Quantum (RSFQ) technology provides for a promising option for realizing integrated circuits and systems exhibiting very high processing speed in combination with very low power consumption. Their operation principle implies the particular representation of binary information by means of short transient voltage pulses. Thus, the development of-RSFQ circuits and systems requires a comprehensive design approach, supported by appropriate methods and tools.

2. CIRCUIT DESIGN BASICS

RSFQ circuit structures are basically composed of Josephson junctions, as the active circuit constituents, placed within inductive loops. The latter ones are dimensioned such that the product of their inductance value and the threshold current of the Josephson junctions is constant. Therefore, taking care for dimensioning these inductances with respect to the Josephson junction represents a major task within the entire design process.

By dimensioning Josephson junctions and arranging them together with inductances, structures for propagating and storing the information can be created. The processing of information is based on a special coding scheme as the state of a logical “1” is attributed to the appearance of a transient voltage pulse. It has been shown for quite a time that simple circuits can be operated at clock frequencies beyond approximately 30 GHz [1, 2]. In order to manage the transition from the laboratory to a production process, a regime of concerted collaboration between circuit design and fabrication process has to be established. In the case of European RSFQ circuits, fabrication takes place at the FLUXONICS foundry [3, 4].

3. DESIGN AND FABRICATION AT FLUXONICS FOUNDRY

In the frame of the European FLUXONICS network [5], a foundry for RSFQ circuits was established and a well-tested cell library of basic RSFQ gates was made available. The FLUXONICS Foundry provides a complete design and fabrication infrastructure including a library of designs for basic gates, design support and the complete fabrication process. The ISO 9000:2001 certified technology is a robust standard niobium based trilayer process (critical current density J_c = 1kA/cm^2) with two wiring layers and a ground plane. The library serves as a key to access the field of RSFQ electronics and provides also general as well as detailed descriptions for this technique. The cell-based design is the most straight-forward solution for a common design process in digital electronics. Our library includes the interface cells between RSFQ and semiconductor electronics as well as all general cells for data transmission, distribution and combination. All elements are analyzed experimentally and can be integrated into larger circuits without further re-optimizations.

4. INTERACTION OF DESIGN CENTRE AND FABRICATION SITE

The maturity of the design flow has been proven by a number of design and fabrication runs performed by the integrated framework of FLUXONICS Foundry. For this purpose, test circuits, composed of basic library cells, have been created. They comprise interface blocks to and from flux-quantum circuits – so-called DC/SFQ and SFQ/DC converters, Josephson transmission lines (JTL), signal splitters, signal mergers, toggle flip-flops (TFF) and delay flip flops and demonstrate the composition of larger functional elements, such as a 4-bit counter and a 4-bit shift register. Circuits are extensively tested including on-chip 30GHz tests enabled by a ladder -type clock multiplier as well as by bit-error-rate measurements. Figure 1 shows the architecture for the high-speed test circuit for the 4-bit counter. A DC/SFQ converter is used to trigger the high-speed ladder-type clock generator. Signal spitters are used to multiply the trigger pulse and confluence buffers combine all five pulses into one line. The intrinsic cell delays result in a generation of a pulse chain with about 30 GHz clock-frequency. Three counter bits are realized by TFFs operating as a ripple counter. Each input trigger pulse increases the counter state by 5. The result is reduced modulo 8 and the overflow pulse is observed by a switching of the output voltage. The circuit has been fabricated by using the mature technology of the European Fluxonics Foundry located at IPHT Jena [3]. Figure 2 shows the correct sequence of counter state and the expected output voltage and a screen-shot of the correct experimental result.

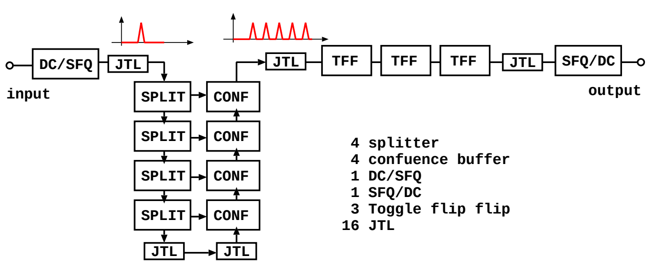

Fig. 1. The cell-based architecture of the test circuit includes six different logic cells. The circuit realization includes about 100 Josephson junctions.

The present results point at the potential of designing integrated RSFQ circuits in a manner that allows for the fabrication of robust circuits in the FLUXONICS Foundry. Possible implications of such an accomplishment are outlined in [6].

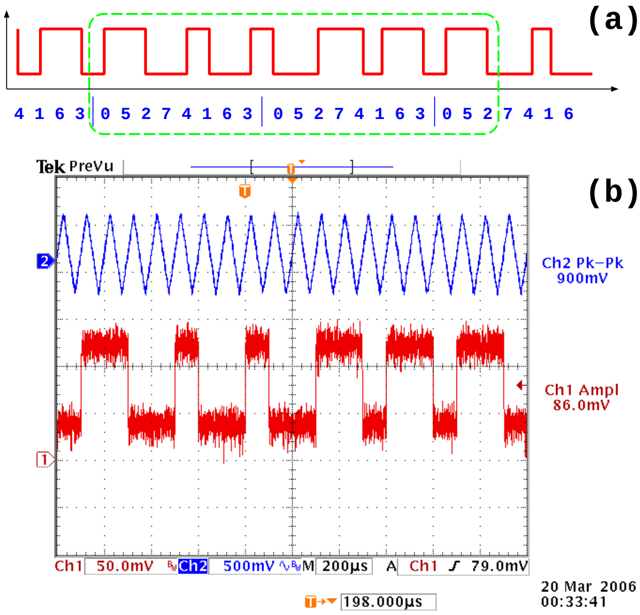

Fig. 2. Illustration of the state transition in the counter (a) and experimental results (b) of the fabricated circuit.

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