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ION IRRADIATION DISLOCATION ENGINEERING FOR SILICON LIGHT EMITTING DEVICES

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ABSTRACT

A study of the formation of dislocation loops in (100) Si wafers, by implantation of boron or silicon, and correlation to the photoluminescence and electro-luminescence of the formed diodes is presented. Boron ion energy was varied from 10-80 keV, and silicon from 75-175 keV. The implanted fluences were from $5x10^{14}$ to $1x10^{15}$ ions/cm^2. After irradiation the samples were annealed for 30 sec to 60 min at 950^{o}C. It was found that the applied ion implantation/thermal processing induces interstitial perfect and faulted dislocation loops sitting in {111} Si habit planes. The loops are located around the projected ion range, but they stretch in depth approximately to the end of range. Their size, distribution and density depend strongly on the used ion species, the applied ion energy, and on post irradiation thermal processing. The measured EL efficiency of the diodes can be directly correlated to the density and distribution of the loops.

Index Terms – Silicon, electroluminescence, LED, ion implantation, dislocation loops, TEM

1. INTRODUCTION

Dislocation loops and other linear defects in silicon were studied extensively as a residual damage after ion implantation doping of silicon [1-6]. Nucleation, growth and transformation of these defects were studied systematically, with the aim to understand and possibly minimize or eliminate their effects on the performance of electronic devices. Defects formed during post-implantation annealing consist mainly of {113} rod-like defects, faulted and perfect dislocation loops. After annealing at 900^{o}C and higher temperatures only extrinsic perfect and faulted loops exist, having {111} habit planes and Burgers vectors a/2<110> and a/3<111>, respectively. They are located around the projected ion range, in cases when there is no pre-amorphization of silicon by ion implantation [6].

Recent developments in Si based light emitting devices raised a new interest in dislocation loops. It was demonstrated that efficient light emitting diodes operating at room temperature can be produced by dislocation engineering in silicon, using standard ULSI procedures involving ion implantation of boron and a subsequent thermal processing [7]. The role of boron implantation is to induce the formation of dislocation loops, as well as to provide p-type doping in the n-type silicon substrate. Interstitial dislocation loops induce a local strain that increases the silicon band gap at their outer edge by up to 0.75 eV, thus enabling spatial confinement of the injected carriers and suppressing their diffusion to non-radiative recombination centers in favor of radiative transitions [8]. For optimal performance, the formation of dislocation loops should be controllable and they should be localized properly in a device structure [9-11].

This paper presents a study of how dislocation loops in silicon can be engineered by applying an appropriate ion implantation and thermal processing. They were formed in (100) Si wafers, by implantation of boron or silicon ions. The varied processing parameters were the ion species, the ion energy, fluence, and the target temperature during irradiation, as well as post-implantation thermal treatment. The interest was to form them at depths above the p-n junction, which is crucial for efficient dislocation engineered Si light emitting diodes (DELEDs) [10]. Hence, amorphisation of silicon was avoided by implanting boron to a fluence below the amorphisation threshold and silicon at elevated temperatures. The distribution of dislocation loops was correlated to the photoluminescence (PL) and electroluminescence (EL) of the formed diodes.

2. EXPERIMENTAL DETAILS

The substrates used were phosphorous doped (2-7 Ωcm) 4 inch n-type (100) silicon wafers. They were implanted with B^+ and Si^+ ions in a 200 kV Danfysik ion implanter, at 7^o off normal incidence, to avoid channeling. Boron ion energy was varied in the range from 10 to 80 keV, at a fluence of $1x10^{15}$ ions/cm^2, the implantations being performed at room temperature. Silicon ion energy was in the range from 75 to 175 keV, implanted at 100 and 200^{o}C, to $5x10^{14}$ and $1x10^{15}$ ions/cm^2. TRIM [12] calculations gave the projected ion range R_p from 39 to 275 nm for boron ions and 112 to 256 nm for silicon ions. After

implantation the samples were treated by rapid thermal annealing (RTA) in a nitrogen ambient, for 30 s to 60 min, at 950^{o}C.

Structural characterization of Si samples, prepared for plan-view and cross-sectional imaging, was done by transmission electron microscopy (TEM), using Philips EM 400 T and CM 200 microscopes. For plan-view imaging we used a off-axis four-beam imaging condition near [001] Si, which allows simultaneous observation of both perfect and faulted dislocation loops, having different Burgers vectors, as described previously [9]. Cross-sectional imaging was done near the [110] Si zone axis. We also used channeling Rutherford backscattering spectroscopy (RBS), with a 1.5 MeV He^{+} ion beam, to study the damage distribution in Si.

The diodes were formed by depositing an Al contact on the front p-side and a AuSb contact on the back side of the n-Si substrate, and a selective etching to isolate the p-n junction. A window was left open on the back side of the diodes to measure the electroluminescence. The surface area of the diodes is $8x10^{-3}$ cm^2. Their schematic presentation and a more detailed description of the fabrication procedure is given elsewhere [8]. EL measurements were performed under forward bias, with the current density of 2 A/cm^2, detecting the light emission by a liquid nitrogen cooled germanium p-i-n detector, in a conventional 0.5 m spectrometer. Temperature dependence of EL was measured in the range from 80-300 K, the samples being mounted in a continuous flow liquid nitrogen cryostat. Prior to EL experiments we have measured the current-voltage characteristics of the diodes.

3. RESULTS

The effect of boron ion energy on the formation of dislocation loops was studied on Si wafers implanted at 10-80 keV, to $1x10^{15}$ ions/cm^2 (the energy being increased in steps of 10 keV) and consequently annealed for 20 min at 950^{o}C. The influence of annealing time was analyzed on Si wafers implanted with boron at 30 keV to $1x10^{15}$ ions/cm^2, annealed for 30 s to 60 min at 950^{o}C. For the later samples the corresponding PL and EL responses were investigated. The effect of silicon ion energy, fluence and the target temperature was analyzed on Si wafers implanted at 75 and 175 keV to $5x10^{14}$ and $1x10^{15}$ ions/cm^2, at 100 or 200^{o}C. Finally, it was demonstrated that dislocation loops can be formed in silicon on insulator (SOI) structures by a similar processing.

3.1. The effect of boron ion energy

TEM analysis has shown that after boron implantation and the applied annealing, 20 min at 950^{o}C, all samples contain only extrinsic dislocation loops. Other possible linear defects were dissolved at these annealing conditions. The dislocation loops have {111} habit planes and are either prefect or faulted. An example is presented by a high resolution cross-sectional TEM image in Figure 1, taken along [110] from a sample implanted at 20 keV. The image shows cross sections of two neighbouring dislocation loops, lying in two different {111} planes parallel to the e-beam. The shorter loop (f) is seen as a whole, while from the longer loop (p) we only see one end, as it stretches much further to the left of the view field. Both loops induce stress in the surrounding Si lattice, which is seen as an increased darkness that spreads laterally, parallel to the loops. The smaller loop is a faulted Frank dislocation loop as it exhibits a stacking fault sequence, and the longer one is a perfect dislocation loop.

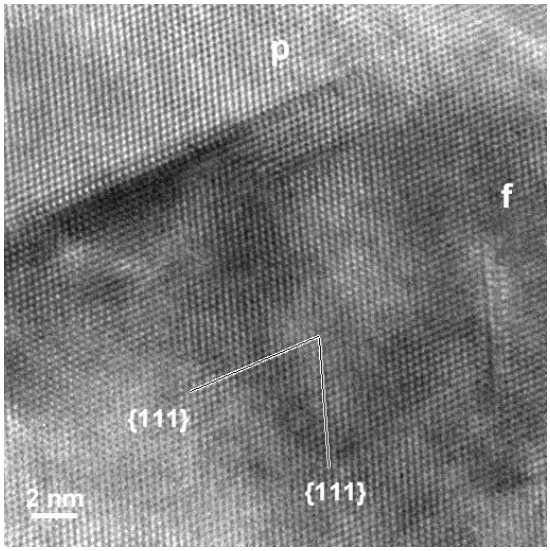

Figure 1 High resolution TEM image of Si sample implanted with 20 keV boron, taken along [110] Si. Labels denote a perfect (p) and a faulted (f) dislocation loop.

The depth distribution, the shape and size of the loops depend strongly on the applied ion energy. A series of bright field cross-sectional TEM images taken from samples implanted with boron at energies ranging from 10 keV to 80 keV is presented in Figure 2. All images were taken along the [110] Si zone axis. Oval shapes are seen due to circular dislocation loops inclined to the imaging direction, and trace lines of loops lying in planes parallel to [110], but also some irregular shapes originating from large irregularly shaped perfect loops as will be seen from plan-view images. As the ion energy is increased, the loops enlarge in size and are buried deeper in the Si substrate. Marked as *h* and *D* in the figure are the mid depth and the innermost edge of the loop layer. They both increase linearly with the ion implantation energy [9].

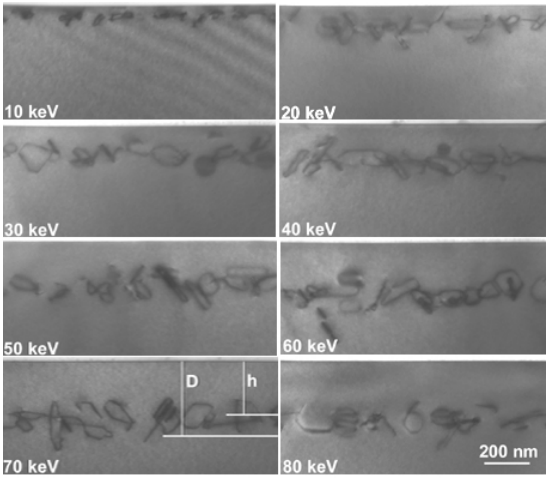

Figure 2 Bright field cross-sectional TEM images taken along [110] Si of samples implanted with boron at 10-80 keV.

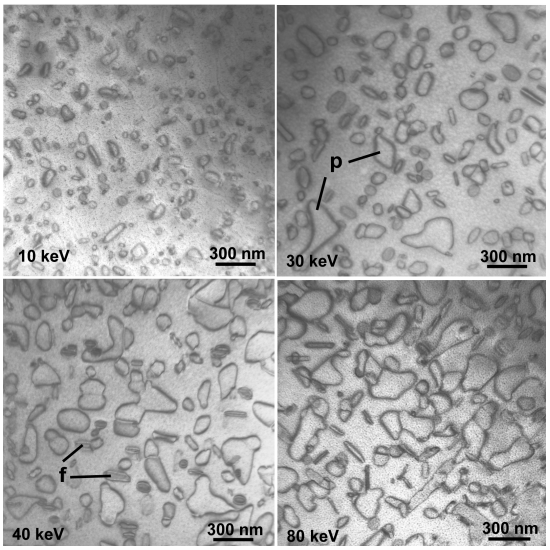

Figure 3 Bright field plan-view images taken under off-axis four-beam imaging conditions near [001] Si, of samples implanted at different boron energies. Markers indicate perfect (p), and faulted (f) dislocation loops.

Plan-view bright field TEM images are shown in Figure 3. The samples were thinned from the back, and the images were taken from thicker areas, where the loops were not partly cut off by thinning. The images illustrate how the loops develop with increasing the ion energy. In the 10 keV implanted sample the loops appear the smallest, with a mean size of ~30 nm for faulted and ~75 nm for perfect loops, although some perfect loops grow up to ~200 nm. For higher implantation energies perfect loops grow much larger. Examples of perfect and faulted dislocation loops are indicated by markers. For the ion energy of 40 keV the maximum size of perfect dislocation loops tends to saturate at ~500 nm, and for higher energies only the number of these large loops increases. Apart from large perfect loops, in high energy implanted samples we still observe much smaller faulted loops. We also observe some prismatically shaped perfect loops, elongated along <110> directions, but generally perfect loops are irregularly shaped.

The results of channeling RBS analysis (not presented here) show that the initial radiation damage in as-implanted samples is fully recovered after annealing, leaving only an increased backscattering yield arising from dislocation loops [9].

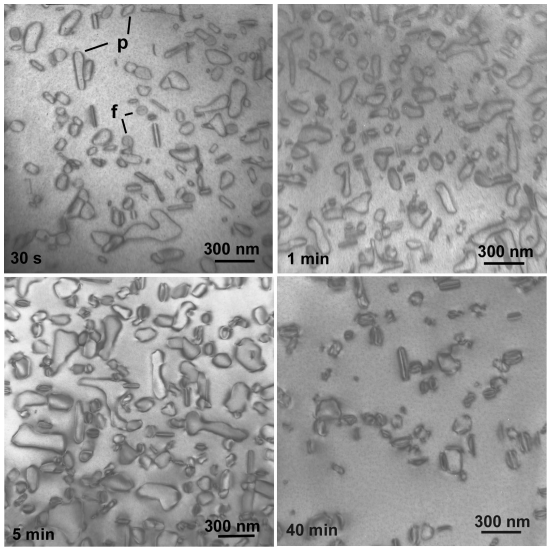

Figure 4 Plan-view bright field TEM images of Si samples annealed for different times.

3.2. The effect of annealing time

Bright field plan-view TEM images of samples implanted with boron at 30 keV to $1x10^{15}$ ions/cm^2, and consequently annealed for 30 s, 1, 5 and 40 min, are shown in Figure 4. After 30 s annealing we observe dislocation loops ranging from ~ 25 nm up to ~ 400 nm. The smaller loops are either faulted or perfect, and the irregularly shaped large ones are all perfect dislocation loops (examples are indicated by markers). Annealing for 1 min yields a higher density of both types of loops, their size being close to those formed after 30 s annealing. A prolonged annealing to 5 min yields a higher number of large perfect loops, of up to ~ 500 nm, coexisting with smaller loops of ~ 25 to ~ 150 nm. With further increase of the annealing time, perfect loops reduce in size, and also the total number of both types of loops reduces. However, the faulted loops increase in size. The image taken from the sample annealed for 40 min shows perfect loops of up to ~ 190 nm and faulted loops of up to ~ 200 nm.

Figure 5 shows bright field cross-sectional TEM images of samples annealed for 30 s, 10 and 40 min, taken near [110] Si. In the sample annealed for 30 s the loops are distributed from the surface to approximately the end of boron range (~ 200 nm). For 10 min annealing the loops are more uniform in size, and confined around the projected boron range (110 nm). In the sample annealed for 40 min there are loops located around the projected ion range, but also some of them diffuse to the surface.

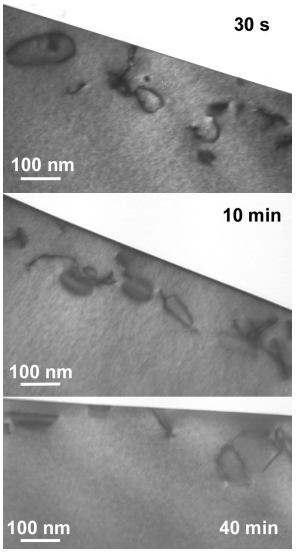

Figure 5 Cross-sectional bright field TEM images, taken along [110] Si, of samples annealed for different times.

Figure 6 plots the density of dislocation loops (a), the estimated areal coverage by the loops (b), and the estimated total circumference of the loops (c), as a function of annealing temperature. It is seen that the maximum number of loops is reached after annealing for 1 min. The maximum areal coverage, of ~ 55% is reached after 5 min annealing. However, when comparing the circumference of the loops, the total border line length after 1 min annealing is much closer to that achieved after 5 min annealing, and drops considerably after annealing for 10 min. For these statistics we have analyzed a total area of 4x4 μm^2, containing above 1000 loops for the highest population. To determine the areal coverage and circumference we assumed a circular shape of the loops, lying in {111} Si planes. These planes are inclined by 35.3^o to the [001] Si zone axis. Hence, circular loops appear as having an oval shape, elongated along <110> directions, their longer dimension corresponding to the actual diameter. An estimated error in these calculations is up to ~ 20% for denser populations, though the plotted graphs give an indication of the general trend.

Room temperature electroluminescence spectra of the fabricated Si DELEDs show a distinct peak at 1.1 μm, corresponding to the phonon-assisted silicon band-edge emission [11]. No other luminescence features are observed. However, the EL efficiency varies with the annealing processing of the Si wafers, and the measurement temperature (80-300 K). Current-voltage measurements show that the turn-on voltage is below 1 V, the characteristics of similar diodes being presented elsewhere [8]. The estimated position of the p-side of the depletion region is at a depth of ~350 nm, meaning that the loops are located within the p-type region of the junction.

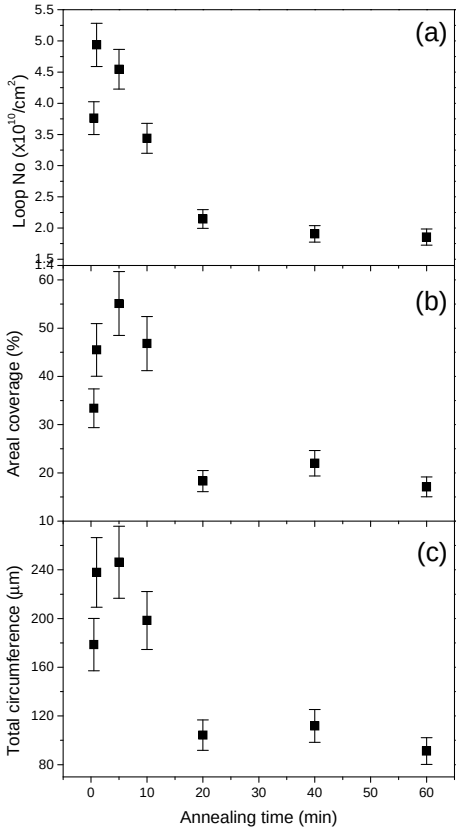

Figure 6 The number of dislocation loops (a), the areal coverage by the loops (b), and the total circumference of the loops (c) from an analyzed area of 4x4 μm^2, as a function of annealing time.

Room temperature EL integrated intensity of silicon DELEDs as a function of annealing temperature is plotted in Figure 7. It is seen that EL efficiency follows the trend presented for the dislocation loop density (Figure 6). The maximum EL intensity was achieved from the sample annealed for 3 min. This annealing time is within the range where we reach the highest population of dislocation loops and an optimal areal coverage of around 50%. PL measurements were carried out on all the samples and show a trend with annealing identical to the EL measurements. The strain field of the dislocation loops decays to close to zero at the junction depth (≥ 350 nm) and so the junction height and injection is

independent of the presence or absence of the dislocation loops. Diffusion of boron during prolonged annealing may influence the junction depth, though the peak p-doping is maintained in the range of 10^{19} cm^{-3}.

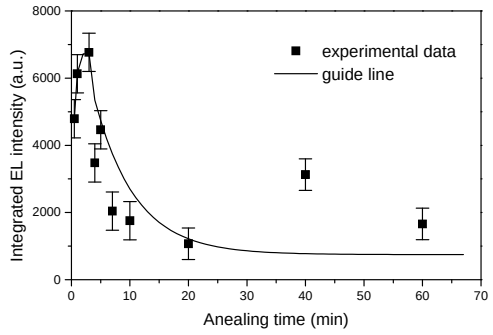

Figure 7 Room temperature integrated EL intensity of silicon DELEDs as a function of annealing time. The solid line is a guide for the eyes.

Figure 8 plots the integrated 1.1 μm peak EL intensity of silicon DELEDs as a function of the measurement temperature. The plots show that the highest EL intensity, in the whole temperature interval, is achieved from the sample annealed for 1 min. The next highest EL intensity comes from the sample annealed for 5 min. It can also be seen that the biggest increase of EL with measurement temperature comes from the samples annealed for 1 and 5 min, having the highest density or the largest areal coverage by dislocation loops.

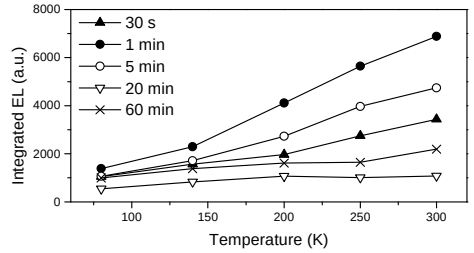

Figure 8 Integrated 1.1 μm peak EL intensity of silicon DELEDs as a function of measurement temperature.

3.3. Dislocation loops induced by Si implantation

TEM analysis of samples implanted with 75 and 175 keV silicon ions at 200°C, and annealed for 30 s, is presented in Figure 9. Bright-field cross-sectional images are from samples implanted to $1x10^{15}$ ions/cm^2, at 75 keV (a), and 175 keV (b) Compared to the samples implanted with boron, the depth distribution of the loops here is rather scattered, although they are basically concentrated around the projected ion range. Again, the loops are formed deeper for the higher implantation energy. However, in (a) we see that some of them stretch much deeper into the substrate. Plan-view images were taken from the samples implanted with 75 keV silicon to $5x10^{14}$ ions/cm^2 (c) and $1x10^{15}$ ions/cm^2 (d). The shape of loops appears to be much more elongated than in samples implanted with boron, although we still have perfect and faulted dislocation loops. Their longer dimension is above 500 nm. It is also seen that higher implantation fluence yields a higher density of loops.

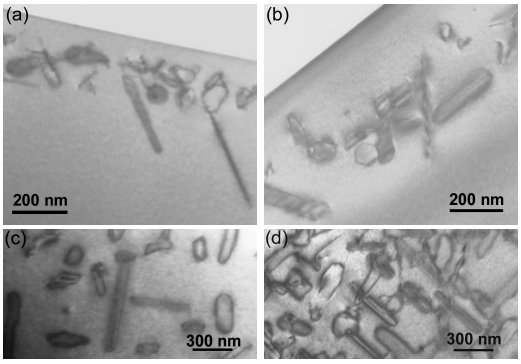

Figure 9 TEM analysis of samples implanted with silicon at 200°C: (a) cross-section, 75 keV to $1x10^{15}$ ions/cm^2; (b) cross-section, 175 keV to $1x10^{15}$; (c) plan-view, 75 keV to $5x10^{14}$ ions/cm^2; (d) plan-view, 75 keV to $1x10^{15}$ ions/cm^2.

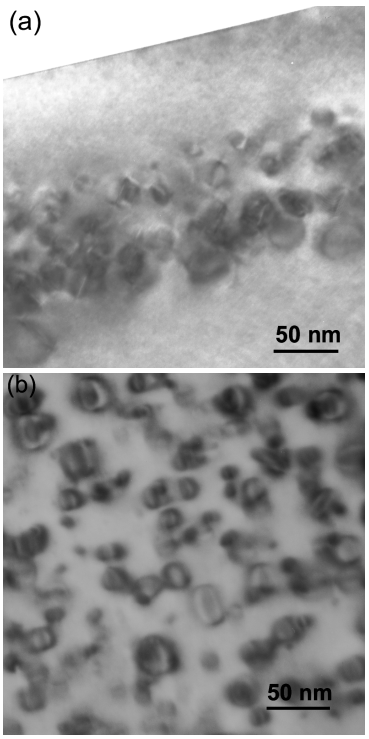

Figure 10 Cross-sectional (a) and plan-view (b) TEM images of sample implanted with silicon, at 100°C, at 75 keV, to $5x10^{14}$ ions/cm^2.

In Figure 10 we present an example of much smaller dislocation loops, generated by implantation of 75 keV silicon at 100°C, to $5x10^{14}$ ions/cm^2, and post-implantation annealing at 950°C for 15 s. This processing resulted in a large number of very small densely packed dislocation loops. The loops are confined much closer to the ion range then in the case presented for implantation at 200°C. In the plane-view image we see that they are all smaller than 50 nm in diameter, and again we see perfect and faulted dislocation loops.

3.4. Dislocation loops formed on SOI Structures

Dislocation loops could also be formed in SOI structures, by implantation if boron at 30 keV, to $1x10^{15}$ ions/cm^2 and a subsequent annealing for 20 min at 950°C. Bright field cross-sectional images of such structure are shown in Figure 11. The insulating SiO_2 layer of ~1.2 μm was buried at ~1.8 μm from the Si surface. Post-implantation annealing recovers radiation damage in the top Si layer, leaving a buried layer of dislocation loops similar as in the case of the analyzed Si wafers.

4. DISCUSSION

Studies of ion implantation induced dislocation loops in Si indicate that they are extrinsic in nature, formed from Si interstitials generated in collision cascades. By a categorization introduced by Jones et al, [6] our case belongs to type I damage, when the Si substrate is not amorphised, but the implanted fluence is above a critical value of ~$2x10^{14}$ ions/cm^2. Introduction of foreign atomic species induces an increased local density in the host material. Simulations of the crystal damage, using the TRIM code, indicate that interstitials are generated deeper in the substrate and vacancies closer to the surface [5]. Majority of induced interstitials and vacancies recombine upon post-irradiation annealing, but there are excess Si interstitials due to the introduced doping species, which preferably occupy substitutional sites in the lattice. The excess Si interstitials nucleate in the form of {113} rod type defects, and faulted and perfect dislocation loops in {111} Si planes, depending on the annealing time and temperature. For longer annealing times and higher temperatures, the presence of extrinsic defects reduces, the excess interstitials either being incorporated in the main crystal matrix, or diffusing to the surface. Studies of the Si surface proximity on evolution of dislocation loops upon annealing suggest that it acts as a sink for Si interstitials [13].

In the experiments presented here, 30 keV boron ions can be considered as shallow implants, the loops being located around the projected ion range of 110 nm, and spreading to the Si surface. Post-implantation processing by RTA at 950°C, induces the highest loop density and areal coverage after 1-5 min. Also, the most efficient EL is achieved from DELEDs produced from Si wafers annealed within this time interval. According to the mechanisms suggested for the formation of dislocation loops, these conditions are reached when practically all excess Si interstitials are trapped by the loops. For a shorter annealing (30 s) there are excess interstitials not bounded by the loops, which can act as point defect centers for non-radiative recombinations. For a prolonged annealing, dislocation loops first coalesce in form of larger loops (5 min), and then (≥ 10 min) gradually decrease in size and density. Being relatively close to the surface, it can be assumed that the loops are dissolved partly by incorporation of Si interstitials in the basic crystal matrix, and their simultaneous diffusion to the surface.

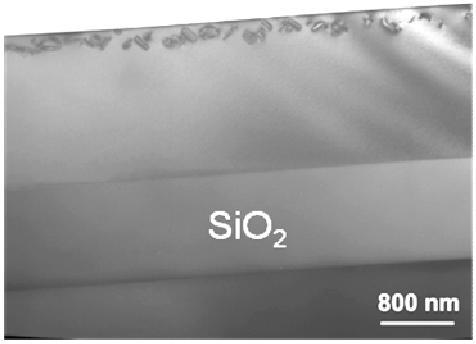

Figure 11 Cross-sectional TEM image of dislocation loops formed on SOI structure.

EL measurements indicate that the most efficient spatial confinement of charge carriers is achieved by smaller and denser dislocation loops. Previous studies gave an estimate of the local stress induced by interstitial loops, calculated using the standard elastic theory of dislocations and the known values of the Poisson's ratio and the Young's modulus for silicon [7]. The induced stress increases the band gap in the vicinity of the outer loop edge by up to ~ 0.75 eV. This applies to both faulted and perfect dislocation loops, the later not having stacking faults, but introducing an extra layer in the Si crystal matrix. The model is presented schematically in Refs. [7&8], proposing that the carrier confinement occurs between the strain barrier resulting from the edges of the loops and the depletion region edge. The present work confirms this theory, showing that dense smaller loops, giving a larger total length of the edge circumference, are dominant for efficient EL. This is illustrated, for example, by comparing the samples annealed for 1 and 10 min. The sample annealed for 1 min has a higher density of dislocation loops, while the areal coverage is slightly higher in the sample annealed for 10 min, but the total circumference length of the loops is again higher in the sample annealed for 1 min. A larger loop circumference can also explain a non-expected higher EL intensity of the

sample annealed for 40 min, compared to those annealed for 20 and 60 min. The absence of thermal quenching, i.e. the anomalous increase of EL intensity with the measurement temperature, indicates that optimal annealing induces the loop distribution that enables a maximum carrier confinement, in minimizing their diffusion to non-radiative recombination centers.

5. CONCLUSIONS

The influence of the main ion irradiation parameters on the formation of dislocation loops in silicon was demonstrated. By varying the ion species, the ion energy, fluence, irradiation temperature, and post-irradiation annealing, it is possible to form various shapes, concentration and distribution of dislocation loops. Correlation of structural and EL analysis of silicon DELEDs shows a dominant role of dislocation loop density and areal coverage on light emission efficiency. The optimal conditions for 30 keV boron implants were achieved for 1-5 min annealing, when the number of loops reaches a maximum of ~$5x10^{10}$ /cm^2 and the areal coverage around 50%. These findings confirm the model that spatial confinement of charge carriers at the edge of the loops is crucial for preventing their diffusion to non-radiative recombination centers, and stimulating radiative transitions at the silicon band edge.

6. ACKNOWLEDGMENTS

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