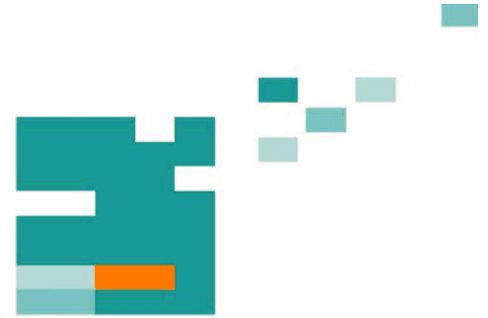**55. IWK**

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RESOURCE-FRIENDLY CONFIGURATION INTERFACE FOR IMAGE SENSORS ON FIELD PROGRAMMABLE GATE ARRAYS

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ABSTRACT

The usage of field programmable gate arrays (FPGA) for image processing relieves the computer system significantly. E.g. filter operations can be realized in the camera itself. The biggest effort of this setup is the possibility of parallelization of filter algorithm calculations. In order to change filter parameters it is necessary to control the FPGA via an integrated interface. An adjustment to different requirements can be accomplished thereby without complete reconfiguration. Due to its simple structure and the fact that it is already included in most image sensors an inter-integrated circuit bus (I²C-bus) is qualified for transmitting control commands to the FPGA.

This investigation focuses on a new intellectual property core (IP-core), which provides an effective I²C-controller for intelligent camera systems. The controller operates as I²C-slave and is functional without an integrated microcontroller. Due to this fact, it is manufacturer independent, because it is designed in basic very high speed integrated circuit hardware description language code (VHDL-code). Thereby the integration in existing VHDL-projects is easy. The controller has the ability to restart itself in the case of errors which assures a high level of reliability.

Index Terms - FPGA, I²C-slave, image sensor, VHDL, image processing

1. INTRODUCTION

In general an image processing system consists of a camera unit, a computer and a data transmission in between. In such a system, the computer has to handle the whole image data stream. There is the possibility to use an FPGA to reduce the computation tasks on the computer. It can either be placed directly in the camera unit or, as a preprocessing card, in the computer. If placed in camera unit, the FPGA will be arranged directly between image sensor and transmission interface [Fig. 1.]. Therefore the complete image data stream has to pass the FPGA. On such FPGAs parallelized algorithms can be implemented. Thus filter operations or complex image manipulations can

computed in real-time. Common PCs are not qualified for such tasks because of their sequential working structure. A camera integrated FPGA enables a more complex data-processing and can reduce the data-volume that must be transferred.
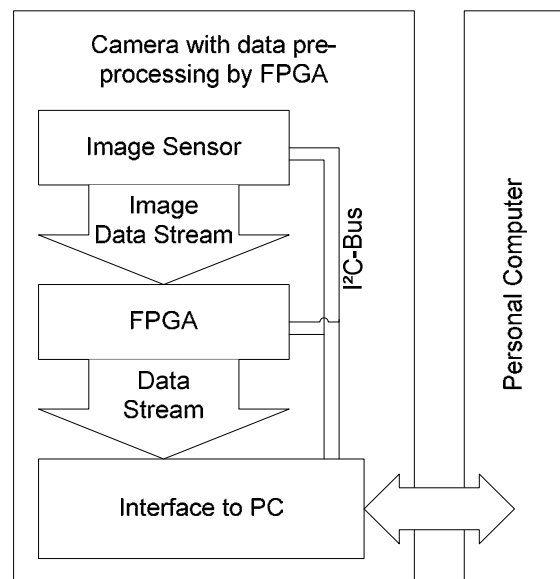

Figure 1. FPGA in camera unit

The use of FPGAs also has a disadvantage. A complete configuration is more complex and time-consuming, than loading a program on a computer. A new configuration, e.g. for different filter tasks, requires complex boot functions. Small variations, like changing filter coefficients or switching functions on or off, can accomplished easily without a reset of the camera. To permit such features, the FPGA has to be equipped with a control interface.

In order to minimize the implementation expenditure and the resource consumption, it is recommended to use a simple interface. The data rate must be small enough to transfer the control commands asynchronous to the image data stream. In this case the I²C-bus is the best selection. It only needs two physical wires and has no protocol-overhead. Even though it's not the most efficient bus, but it is license-free usable and already implemented in many integrated circuits (IC). The I²C-bus is already used for intern communication in the most camera systems.

Hence a connection of the FPGA to the I²C-bus in hardware is simple.

2. THEORY OF FPGA-DESIGN AND I²C-BUS

FPGAs are ICs that consist of physical input/output blocks and a two dimensional array of general purpose logic blocks. These logic blocks or slices consist mainly of a look-up table (LUT) and an output which can be operated in clocked or pipelined mode, according to the position of an output multiplexer [Fig. 2.]. The position of the multiplexer and the mapping of the LUT of every logic block can be programmed. The connections between logic blocks can be routed individual. In order to reduce the logic block consumption and add functionality, most FPGAs are extended with programmable hardware circuits like memory blocks or microcontrollers. Static, hardware implemented circuits are called hard-core. Through interconnected logic blocks realized circuits are called soft-core. The information about the structure of a soft-core is called IP-core. This information is usually programmed in a hardware description language like VHDL.
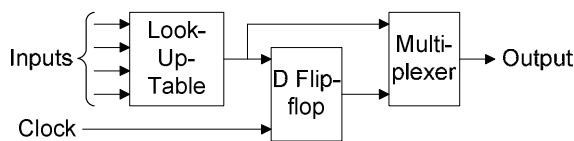

Figure 2. Simplified structure of an FPGA logic block

That means: FPGAs are not programmed with software in terms of a sequential program but they are configured with a specific hardware design, consisting of one or more IP-cores. The Construction of a hardware design is speed up by the usage of free available or licensed IP-cores.

The I²C is a serial bus, which was developed in the 1980s mainly for the system-intern communication of ICs. One master and up to 112 slaves can participate on the bus. There is one clock signal line (SCL) and one data signal line (SDA). Both wires are bi-directional. They are set up on high by pull-up-resistors. Each bus-participant can set the line down to null. Controllers are sending sequential every byte bit-by-bit on the SDA line. After each byte that has been transferred, an acknowledge-bit of the receiver follows. The first byte is always sent from the master and contains the address of one of the slaves. Also the master sets the clock at SCL.

3. STATE OF THE ART

Several IP-cores, like Xilinx-XPS-IIC-core or different open source cores, which provide I²C-controller functionality, are available. In these cores the master function is of great importance. Due to this fact, the resource consumption is high, even though only a slave-controller is necessary.

Furthermore the implementation of such IP-cores is often inconvenient or linked to the usage of soft-core processors or special buses. For example the existing Xilinx XPS IP core works only as part of the MicroBlaze microprocessor. MicroBlaze is a 32 bit reduced instruction set computer (RISC)-architecture. It is powerful but restricted to Xilinx FPGAs. The new IP-core shall be all-purpose. It shall run independent, but still offer the chance to be easily connected to a micro processor design.

4. CONCEPT OF RESOURCE-FRIENDLY I²C-SLAVE-CORE

Task is to design a control interface for image sensors on FPGAs. The configuration of the camera integrated FPGA by the I²C-bus can be carried out on computer. For receiving control signals, a mere slave-controller suffices. Moreover the I²C-bus in camera module already exists. Therefore an I²C-master must exist as well. Hence it is possible for new I²C-slave-controller to abandon on the master function.

The fundaments of the I²C-slave-controller are a state machine [Fig. 3.], the production of indicator signals and the storage of data in the input and output registers. These parts are implemented in VHDL. The state machine manages on seven stages only. If a faulty signal is detected, a reset of the state machine from any stage is the result. This happens in order to prevent the bus from getting in an undefined state. The set of the indicator signals occur synchronized, to compensate troubles and delays in the run-time.
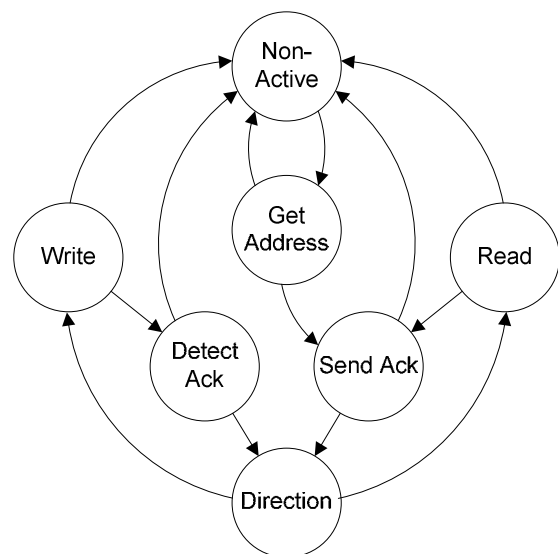

Figure 3. State machine of I²C-slave-controller

The I²C-slave-controller possesses input and output registers for intern connection. It must be supplied with a clock signal. Optional there is an interrupt- and a reset signal. Those simplify the connection to the soft-core processor.

5. EXPERIMENTAL SETUP

For the development of the IP-core, two FPGA-evaluation-boards from Xilinx are used [Fig. 4.]. Those boards offer an ideal condition for debugging and supervising of the bus-system, because I²C-bus wires are already connected to the FPGA in hardware. SDA and SCL of both boards are connected to each other. For monitoring both bus lines are additionally monitored by an oscilloscope. On one evaluation-board a commercial I²C design is implemented. This design is pre-assembled by some Xilinx software-tools and includes a MicroBlaze processor combined with Xilinx-XPS-IIC-core driven as master. On the other evaluation-board different versions of the I²C-slave-core are implemented on the FPGA. Open wiring and the possibility of observing the signal levels on the oscilloscope offered ideal conditions for detecting and correcting errors in VHDL-code.

Figure 4. Two Virtex5 evaluation-boards

6. EVALUATION

When the I²C-slave-controller is operating stable at the evaluation board and data transmission runs reliably, the I²C-slave-controller is evaluated on another hardware platform. The hardware is similar to the one on which the I²C-slave-controller should be used later. It consists of a modular designed charge-coupled device (CCD)-camera unit with an integrated FPGA-module. The camera unit is connected to the computer by universal serial bus (USB). The image data from the image sensor has to pass through the FPGA. The USB-interface sends it to the computer afterwards. The USB controller also transforms the control commands from the host computer to I²C-bus and works as I²C master. Simple filters are implemented on the FPGA and are applied to image data. Furthermore the I²C-slave-controller is implemented. Received control commands are emitted as filter parameters. The change of the displayed images confirmed the successful transfer of the commands to the FPGA and their local converting.

7. DISCUSSION

How expected, the I²C-controller needs less system resources than controllers including the master function. In stand-alone configuration [Fig. 5.], the requirements of logic slices vary between 41 and 171, depending on the number of bytes to receive or send[1].

Attention must be paid to the fact, that the maximum transfer size of the I²C-slave-controllers is limited to 16 bytes, when no soft-core processor is used.
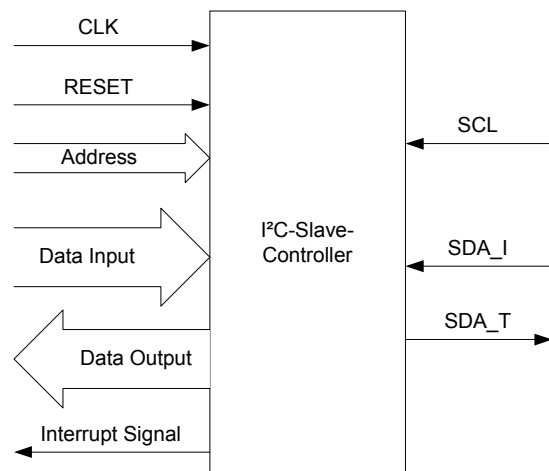
Figure 5. Controller connection plan

The controller will be optimized during synthesis again, when only a brief transfer size is needed: The need for slices decreases. However, always the entire IP-core is implemented when using a soft-core processor because the syntheses tool does not check which input and output registers are used by the software running at the processor. Furthermore a soft-core processor always needs a program memory. The I²C-slave-controller as a configuration interface of the image sensor only has to receive easy control-commands. Therefore a soft-core processor is non essential in most cases.

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[1] Data have been gathered on a Virtex5.

The I²C-slave-controller is very reliable. Even though the I²C-bus is driven by low clock rates and the wires are short, there is the possibility of incorrect signals, for example, when the camera unit restarts. The controller reset itself, if an error occurs. In case a participant of the I²C-bus remains in a condition, where it sets one of the two signal lines to null, no other participant will be able to send messages any longer. In worst case by resetting the controller data will be lost and must be resent. However the bus can still be used without a restart of the camera module. Even a short-term disconnection to the signal line or the consciously sending of none I²C conform signals does not result in a blockade of the bus by the I²C-slave-controller. This is important in order to ensure a reliable and steady working process.

The I²C-slave-controller can be used at platforms of different manufacturers without the usage of special libraries, because it is native VHDL-code. In addition, VHDL allows further customizing or increments, without necessity of extensive and expensive software. For test applications the I²C-slave-controller can be used for eavesdropping of messages. It is sufficient to use the same address for both Slaves and declare the SDA pin as an input instead of a bidirectional port. Thereby the acknowledge-bit of the FPGA cannot be send. The bus stays unaffected.

8. CONCLUSION AND OUTLOOK

The advantage of the new I²C-slave-controller is its independent operating, high reliability, simple connections and low resource requirements. This combination is not only ideal for FPGAs in image sensors, but wheresoever's easy control-commands shall be sent to an FPGA.

At the moment, the I²C-slave-controller is only evaluated on Xilinx FPGAs. Although there are no concerns about the functionality, an evaluation on FPGAs of other manufacturers is pending.